EECS 470 Fall '25

Homework 1

Due Wednesday September 10th by 11:59 pm on Gradescope.com. **Late homeworks are not accepted.**

Name: _____ unique name: _____

Upload a PDF of your legible answers to the course Gradescope page. ***Assignments that are difficult to read will lose at least 50% of the possible points and we may not grade them at all.*** This is an individual assignment; all work should be your own.

- If you use references other than the text and class notes, be sure to cite them!
- This assignment is graded out of 30 points.
- Remember you may drop one homework assignment score.
- Please state any assumptions.

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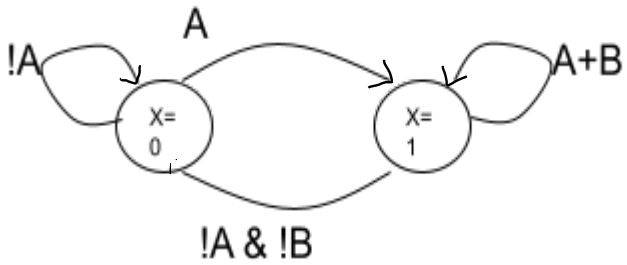
1. **Understanding Pipelines.** Consider the following code segment:

```
Loop:DADDI R2, R2, #4   ; R2=R2+4
     DSUB R4, R3, R2 ; R4=R3-R2
     LD R1, 0(R2) ; R1=MEM[R2+0]
     DADDI R1, R1, #1   ; R1=R1+1
     SD 0(R2),R1 ; MEM[R2+0]=R1
     BNEZ R4, Loop   ; if(R4!=0) goto Loop
```

   a. Show the timing of the instruction sequence of the 5-stage RISC pipeline discussed in class. Assume there is no forwarding but that a read and write in the same clock cycle "forwards" through the register file. Your answer should be drawn like figure C.5 from the 5th edition of the text (see link to book on course website). Memory accesses take one cycle. How many cycles does a single iteration of this loop take to execute (i.e. what is the latency between starting execution of the first load and completion of the branch)? **[3]**

   b. As part "a" but assume normal forwarding and bypassing. Assume the branch is predicted not-taken. **[3]**

2. **Digital Logic Design.** Consider the following Moore-type state-machine:



Draw a circuit diagram which implements this state-machine. You are to use only 2-input AND, OR and XOR gates, inverters, and D flip-flops. The inputs are not available in inverted form. Be sure to include a clock input. You should minimize the number of logic gates required. **[3]**

3. **Cache Design.** Consider a 1MB 8-way set-associative cache with 64-byte lines. Both the virtual and physical address spaces are 40-bits in size (see chapter 2 in text if you need to review caches).
    - **a.** How may **bits** are used for the tag comparison, set index, and byte offset respectively **[2]**
    - **b.** How many **bytes** (total) are used to store the tags for this cache (just the address tag bits, do not include additional flags like valid, writable, readable, or dirty0? **[1]**
    - c. What would your answer to b) be if the cache were fully-associative? Direct-mapped? **[2]**

4. **ISA Design.**
    - **a.** Give **two** examples of characteristics that distinguish RISC from CISC architectures. **[2]**
    - **b.** State **two disadvantages** of having very large (1000's of entries) register files. **[2]**

5. **Power.** AMD is working to improve the energy-efficiency of its next-generation server processor. The baseline processor consumes 100W. They are considering adding a new low-power mode that shuts off 75% of the on chip caches. The low power mode incurs a 15% performance hit, but reduces power consumption to 75W.
    - a. Should they add the new low power mode? Why or why not (justify your answer **quantitatively**) **[3]**

6. **Multicore.** Data Centers R'Us is evaluating new multicore processors to run their Web 2.0 eCommerce application software. Suppose that the code to run a transaction is 90% parallelizable (such that performance scales linearly with the number of cores), but 10% is serial (can only run on one core). The company is evaluating three chips:
    (1) a **single-core** chip that draws 80W of power;
    (2) a 100W **quad-core** chip where each core is 20% slower than the single-core chip;
    (3) a 135W **8-core** chip where each core is 35% slower than the single-core chip.

    - **a.** Suppose the eCommerce application runs at 100 transactions per second on a single-core chip. How many transactions per second does it achieve on quad-core? The 8-core? Which chip achieves the highest performance? **[2]**
    - **b.** On average how much energy (Joules) per transaction is required by each chip? Which chip is most energy efficient? Recall that energy equals power multiplied by time **[3]**

7. **Averaging Methods.** According to Tom's Hardware (http://www.tomshardware.com), the Intel Core 2 Extreme QX6850 is 1.42 times faster than the AMD Athlon 64 X2 6000+ on the PCMark 2005 (CPU) benchmark, 1.13 times faster on the PCMark 2005 (Mem) benchmark, and 1.77 times faster on the Quake IV THG Timedemo.
    - **a.** Which averaging method (arithmetic, harmonic, or geometric) should be used to summarize the speedup of the Intel chip over the AMD chip, and why? **[2]**
    - **b.** Calculate average speedup. **[2]**