EECS470 Homework 2 Answers

1)

Instruction	Decode (D)	Execute (X)	Writeback (W)
Loop: LD 0(R1),F2 (2)	1	3	4
I0: ADDD F0,F2,F4 (3)	4	7	8
I1: DIVD F2,F0,F6 (10)	8	18	19
I2: LD 8(R1),F2 (2)	19	21	22
I3: MULTD F2,F6,F10 (5)	22	27	28
I4: ADDD F2,F2,F2 (3)	28	31	32
I5: ADDD F2,F4,F2 (3)	32	35	36
I6: SD 8(R1),F10 (1)	36	37	38
I7: ADDI R1,#16,R1 (1)	38	39	40
I8: SUB R4,R1,R20 (1)	40	41	42
I9: BNZ R20, Loop (1)	42	43	44
Loop 2	44		

The loop takes 44 cycles to complete.
*Okay if they wrote 43 cycles

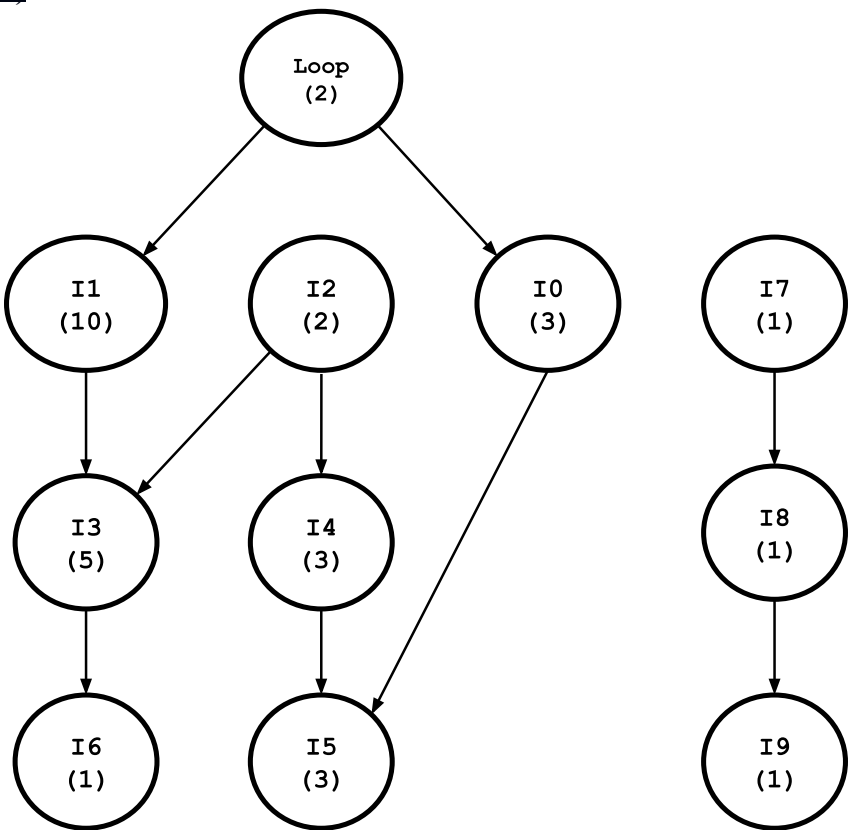
2)

Assuming multiple writebacks per cycle:

Instruction	Dispatch (D)	Issue (S)	Exec (X)	Writeback (W)
Loop: LD 0(R1),F2 (2)	1	2	4	5
I0: ADDD F0,F2,F4 (3)	2	5 (RAW F2)	8	9
I1: DIVD F2,F0,F6 (10)	3	6 (S hazard)	16	17
I2: LD 8(R1),F2 (2)	5 (WAW F2)	7 (S hazard)	9	10
I3: MULTD F2,F6,F10 (5)	6	17 (RAW F6)	22	23
I4: ADDD F2,F2,F2 (3)	10 (WAW F2)	11	14	18 (WAR F2)
I5: ADDD F2,F4,F2 (3)	18 (FU hazard)	19	22	24 (W hazard)
I6: SD 8(R1),F10 (1)	19	23 (RAW F10)	24	25
I7: ADDI R1,#16,R1 (1)	20	21	22	26 (W hazard)
I8: SUB R4,R1,R20 (1)	26 (FU hazard)	27	28	29
I9: BNZ R20, Loop (1)	27	29 (RAW R20)	30	31
Loop 2				

The loop takes 31 cycles to complete.

3)



4) The minimum latency is 18 cycles. (Loop → I1 → I3 → I6)
Give partial credit if answer matches longest path shown in previous problem