

Homework 4

Due November 7th by 11:59pm.

Name: _____ unique name: _____

Remember you may drop one homework assignment.

1) Consider a local correlated predictor with 2-bit saturating counters for entries in a **global** pattern history table (PHT), and 7-bits of the PC as index to the **per-pc** branch history table (BHT). The designers of the machine with this PAg predictor are looking at the following branch sequence:

T T T N T T T T N N T T T N T T T T N N T T T N.....

a) How many bits must each branch history register contain to achieve 100% accuracy in the steady state operation

b) Draw a diagram of the system.

e. The most astute of the 0x1eaf group remembers the GSHARE predictor from EECS 470. A quick analysis shows that by changing the parameters, the GSHARE can outperform both the GAp and PAg designs on the workloads. How large would the GSHARE predictor be given the following parameters?

18-bits of PC
18-bits of History
2-bit predictors

d. Finally, The 0x1eaf team is now asked to evaluate a new set of workloads for the design they chose, there are several benchmarks with a nested for-loop, but each benchmark has different sized inner loops (and a really large outer loop count). What is the largest size inner for-loop that each design can predict correctly in the steady-state (after it is warmed-up). You can assume that no other branch aliases to the same location for the PAg design.

i) PAg

ii) GAp

iii) GSHARE

4) **[TEAM PROBLEM]** Your entire team should each turn in the same answer to this question.

Write a “long” (thousands of instructions *executed*, it may be shortish in terms of instructions in the program) RISC-V test vector (test program) that would help you figure out:

- a. If your X-way superscalar processor meets the goal of getting an IPC greater than X-1.
- b. If your processor meets the expected IPC when executing a chain of dependent instructions.
- c. If your load-store queue can correctly handle back-to-back stores and loads to the same address.

In each case provide not only the test vector, but explain how looking at performance counters (e.g., instructions retired, branch mispredicts, stall counters, etc) would help you know if your design was meeting the stated goal.