EECS 470 Worksheet: Lab 1

Due on Gradescope by Friday, 9/5 at 11:59pm

This worksheet is your deliverable for the lab assignment. Answer the questions, then talk to an instructor during lab or office hours to get the check-off and submit it on Gradescope. In Gradescope we will only be checking the signature, not the answers.

Feel free to download this worksheet from the website if you want to work on it with a tablet.

1. Combinational

Which basic logic gate does this module implement?

AND OR NAND NOR XOR

2. For-loop

Briefly describe what the given module accomplishes. Then, describe how you could change the structure to reduce the latency of producing the output. (Hint: the current structure has O(n) complexity, but you can do better...)

3. State Machine

3.1. Sequential Clock/Reset

Why do we need a clock and reset in this module but not the previous modules?

3.2. State Diagram

Draw the state transition diagram for this module.
Include the enable signal as an input and write the prediction output at each state.

4. Register File

4.1. Synthesis

If this module were synthesized, how many 1-bit D flip-flops would be required to implement it?

4.2. Comprehension

Briefly describe what internal forwarding is in the context of the module. Then, describe a way internal forwarding could be implemented in hardware?

5. Hardware Schematic to SystemVerilog

Write synthesizable SystemVerilog that implements the behavior of the hardware schematic given in the lab 1 assignment.

6. Accessing CAEN

Show the instructor that you can access CAEN and clone Project 1 from GitHub.

Instructor signature and date:
(or unique code if virtual)