EECS 598: Ultra-Low-Power CMOS Circuit Design (up to 4 Credits)
Time: Wednesday and Friday 2:00 to 3:30 pm

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Following the trajectory of the Moore's Law, the integration density of VLSI chips has grown exponentially from two thousand transistors per chip in the early Seventies (i4004) to over one billion transistors (Itanium) in 2009. During this time, CMOS VLSI design has witnessed multiple generations of evolution as the CMOS circuit design focus gradually shifted from Silicon real estate (in the late 70's) to timing closure (in the late 80's), to power aware (in the late 90's), and then to process variations (reliability) at sub-100 nm transistor dimensions. This course envisages studying energy-aware CMOS circuit design techniques that are currently being used in building low-power (at nominal supply voltage) and ultra-low-power (in subthreshold region) VLSI systems. Students interested in taking this course must have basic background in CMOS design (equivalent to EECS 312) and are expected to know circuit equations for minimization of power consumption as well as energy-delay optimization. The course will mainly focus on various aspects of subthreshold CMOS circuit design as outlined below.

Outline: i) Analysis of inverter operating in subthreshold mode for voltage transfer characteristics, noise margin, and energy-delay; ii) Energy minimization and energy space contour optimization; iii) Fan-out and noise margin considerations in sub-Vt design of trans-receiver circuits, and word/bit line drivers; iv) Ultra-low-power SRAM design, estimation of lower-bound of data-retention voltage, and dependence of DRV on PVT parameters; v) SRAM static and dynamic noise margin, read/write error margins, and multi-configurations of SRAM cells; vi) Analysis of sub-Vt logic families -- pseudo NMOS, PTL, CPL, and CVSL; vii) Subthreshold design of phase-locked loop and delay-locked loop, viii) Subthreshold DRAM design, ix) Subthreshold memory interface logic, x) Leakage current modeling of CMOS transistors and methods for reduction of leakage currents; xi) Theory of body biasing and ultra-dynamic voltage scaling; x) Brief introduction to subthreshold analog design; xi) Guest lectures on mixed-signal subthreshold system design.

Evaluation Criteria: i) Team homework problems (40%), ii) Critiquing of papers and presentation in class (15%), and iii) An end-of-the-term project (45%) which may include a) sub-threshold circuit design, analysis and simulation, or b) a small subthreshold chip design.

Text Book: The course will mainly rely on instructor's class notes and numerous archival papers on subthreshold circuit design, while the following two reference books on CMOS circuits will be helpful for students to acquire background information for homework and the class project.

Reference Book:

1. Sub-Threshold Design for Ultra Low-Power Systems by A. Wang, B. H. Calhoun, and A. P. Chandrakashan.

Prerequisites: EECS 312 or EECS 427 or Instructor's consent.

Credit Hours: 3 credits without chip design and 4 credits with chip design.