A Low-Power Transmitter for Sensor Networks

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Die photo and block diagram of the transmitter.

The aim of this research is to develop a new architecture for a wireless transmitter with an emphasis in performing much of the analog functions, which are typically required, in the digital domain. The proposed transmitter architecture performs direct modulation by varying a phase-locked loop (PLL) divide ratio. We developed a synthesizer that utilizes a novel, all-digital phase detector in place of the conventional analog-intensive phase detector, charge pump, and loop filter blocks. In addition, the design uses a digital dual-modulation scheme that alleviates the tradeoff between loop bandwidth and switching speed. These techniques were developed as part of a prototype 14mW 2.2GHz MSK transmitter with a transmission rate of 927.5kbit/s. This novel scheme was presented at ISSCC 2007. This project is supported by the Engineering Research Centers Program of the National Science Foundation under award number EEC-9986866.