End of the CMOS Scaling Roadmap ADCs

Jorge Pernillo and Michael P. Flynn

Our goal is to investigate new approaches to analog-to-digital conversion that are suited for end-of-the-roadmap CMOS, and which also deliver orders-of-magnitude improvements in speed and energy efficiency. We break analog-to-digital conversion down to its essence and simplify the process of analog-to-digital conversion to its most basic form. This allows us to take advantage of the tremendous digital capability of nanometer processes and then implement the analog circuitry in the simplest way. We propose an ADC structure that is comprised of low-precision comparators aided by digital processing. The architecture incorporates redundancy to cancel mismatch and offset. This project is supported by an Intel Ph.D. Fellowship.