Self-Calibrating Moderate Resolution Analog-to-Digital Converters

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The accuracy of SAR analog-to-digital converters is deteriorated by mismatch in the DAC capacitor array. Our goal is to identify an optimization algorithm that can be implemented on-chip to calibrate the capacitor array to yield the best ADC performance. The optimization algorithm is modeled in MATLAB to determine the effects of different algorithm parameters. Monte Carlo simulations are used to measure the effectiveness of the algorithm and compare the performance of both the calibrated and unmodified ADC’s. The algorithm will be implemented with the help of a calibration engine, a SRAM array, and calibration logic. The figure shows a Monte Carlo simulation of 100 10-bit capacitor arrays. Moderate resolution, low-power ADCs are required for digitization of sensor outputs and for digitizing baseband signals in the wireless transceiver. The SAR ADC architecture is a good candidate for digitizing wireless IF or baseband signals. This work complements the work on CMOS transceivers and on ADCs at the WIMS Center. A low-power SAR ADC would be very useful for sampling IF signals in a sensor network wireless receiver. This project is supported by a GEM Fellowship, Analog Devices, and by the Engineering Research Centers Program of the National Science Foundation under NSF award number EEC-9986866.