A Silicon-Based Crossbar Ultra-High-Density Non-Volatile Memory

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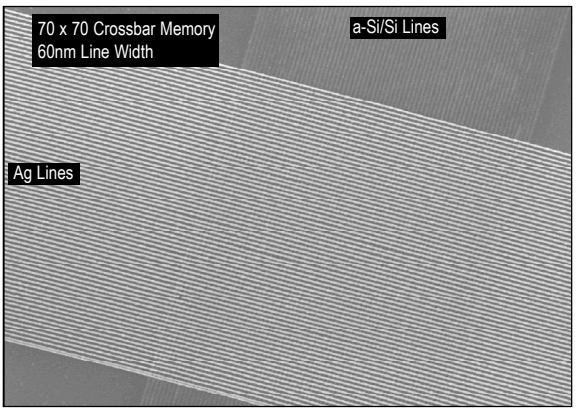
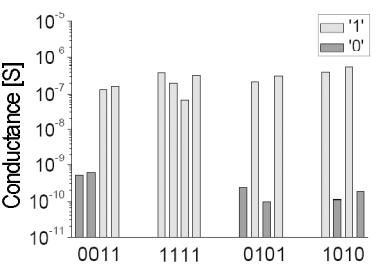


A 5kb crossbar memory with density of 5Gb/cm^2.

The ever-increasing demand of non-volatile memory will lead to pursuit of terabit density (10^{12} bits per cm^2) that is likely beyond the capability of current technology. This project seeks to develop ultra-high-density, non-volatile memories using a crossbar structure, in which the memory components are two-terminal hysteretic resistive switches formed by two arrays of metal wires crossing each other and sandwiching a storage medium. Unlike previous attempts based on molecules that suffer from issues such as low yield, slow switching speed, and low on/off ratio, a silicon-based, fully CMOS compatible crossbar memory was achieved using nanoscale two-terminal hysteretic resistance switches. The prototype single-cell devices show scaling potential beyond 50 x 50nm^2, switching speed <5ns, endurance >10^6, and retention ~1 year. Full control of the device parameters was obtained that lead to ultra-low programming current (10nA) and rectifying current-voltage characteristics in the on state. This system offers the potential to integrate the novel crossbar architecture with reliable CMOS processing technology. A 5kb memory with density of 5Gb/cm^2 was demonstrated, and density >40Gb/cm^2 is expected in the near future. Further studies on the hybrid crossbar/CMOS system may lead to not only stand-alone, high-density memory devices, but also reconfigurable and fault tolerant computing schemes using potentially faulty nanodevices. This project is supported by the National Science Foundation under award number CCF-0621823.



A 4 x 4 array configured into different states.