Investigation of Diffusion Rounding for Post-Lithography Analysis

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Due to aggressive scaling of device feature size to improve circuit performance with smaller size in sub-wavelength lithography regime, diffusion as well as poly gate shape is no longer rectilinear as shown in the above figure. Diffusion rounding occurs where the diffusion shapes are not perfectly rectangular, including common L- and T-shaped diffusion layouts to connect to power rails. In this study, we investigate the impact of the non-rectilinear shape of diffusion (i.e., sloped diffusion or diffusion rounding) on circuit performance (delay and leakage) using TCAD simulation. Simple weighting function models for $I_{on}$ and $I_{off}$ to account for the diffusion rounding effects are proposed. TCAD simulation results show that diffusion rounding has an asymmetric characteristic for $I_{on}$ owing to the differing significance of source/drain on device threshold voltage. Therefore, we can model $I_{on}$ and $I_{off}$ as a function of slope size and location of the slope. The proposed models match well with TCAD simulation results, with less than 2% and 6% error in $I_{on}$ and $I_{off}$, respectively. The plot shows the accuracy of the proposed models for different slope sizes from 10nm to 40nm. As can be seen, the proposed models capture the effect of diffusion rounding well in both $I_{on}$ and $I_{off}$ across different slope sizes. This project is supported by Microelectronics Advanced Research Corporation research program of the Defense Advanced Research Projects Agency under award number SA4242-79952.