A Synthesizable Ultra-Wideband Transmitter

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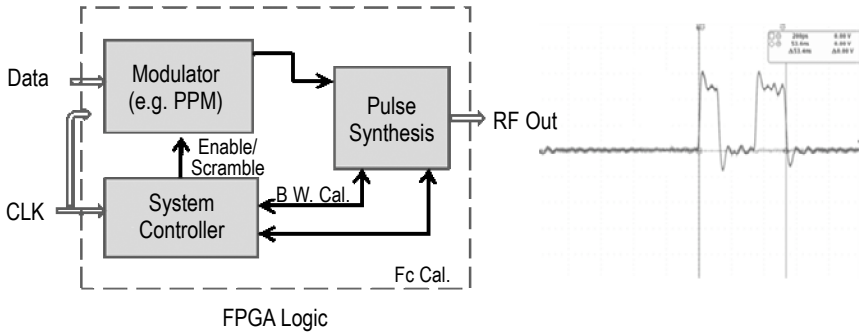

FPGA architecture of UWB transmitter and RF output signal.

This project seeks to develop an all-digital UWB transmitter which is synthesizable. First, all-digital transmitter architectures utilize many of the advantages of pulse-UWB systems, enabling low cost, low energy/bit, and high integration. A synthesizable architecture provides flexibility in the design flow and eliminates time-consuming processes such as custom layout. As a prototype, an all-digital UWB transmitter is being implemented on an FPGA device (Xilinx Virtex-II). All the functional blocks in this transmitter will be described in verilog code, then synthesized and place-and-routed by standard design tools. The bandwidth and center frequency of the RF output signal are digitally tunable to adapt to various requirements of application. Also, any variation induced by process, temperature, and routing is calibrated by the controller. Since this transmitter is synthesized and routed by CAD tools, the calibration has a critical role in this synthesizable architecture. After all the functionality of this architecture is verified, this all-digital UWB transmitter will be implemented in a 65nm CMOS technology. This project is supported by the University of Michigan, College of Engineering Start-Up Funds.