

A mixed-signal sensor interface microinstrument

Keith L. Kraver^{a,*}, Matthew R. Guthaus^a, Timothy D. Strong^a, Peter L. Bird^a,
Geun Sig Cha^b, Wolfgang Höld^c, Richard B. Brown^a

^aDepartment of Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor, MI 48109, USA

^bChemical Sensor Research Group, Department of Chemistry, Kwangwoon University, Seoul, South Korea

^cInformation Appliance Division, National Semiconductor Corporation, D-82256 Fürstfeldbruck, Germany

Abstract

A single-chip implementation of a microinstrumentation system is presented. The chip incorporates voltage, current, and capacitive sensor interfaces; a temperature sensor; a 10-channel, 12-bit analog-to-digital converter; and an 8-bit microcontroller with a 16-bit hardware multiplier and a 40-bit accumulator. Serial and parallel interfaces allow digital communication with a host system. Fabricated in a standard 0.35 μm digital CMOS process, the die occupies 3.8 mm \times 4.1 mm, operates from a nominal supply voltage of 3 V, and draws 16 mA when fully powered (850 μA standby current). To facilitate testing of the prototype, extra pads are bonded out to package pins. The chips are packaged in 132-pin ceramic pin-grid-array packages. © 2001 Elsevier Science B.V. All rights reserved.

Keywords: Sensor interfaces; Microinstrumentation; Mixed-signal design; Embedded microcontroller

1. Introduction

Sensor interfaces have been identified as critical to the development of the MEMS field [1]. Multi-chip sensor/interface-circuit solutions have been developed [2], and interface electronics have been integrated with sensors [3]. This paper presents a single-chip microinstrument: a mixed-signal microcontroller with an analog-front-end including voltage, current, and capacitive sensor interfaces; signal amplification; and analog-to-digital conversion circuitry. The only sensor integrated on this chip measures temperature, but other sensors and actuators could be included. However, for many applications in which the MEMS devices cannot be made with CMOS process steps, or in which sensor lifetime is limited, the most efficient system partitioning allocates all or most of the electronics to a microinstrument chip separate from the sensor.

Recent advances in mixed-signal chips that target sensor applications have been reported. Cirrus Logic developed an integrated circuit (IC) that combines an input multiplexer, a programmable gain instrumentation amplifier, a high resolution ADC, and a serial interface to communicate with an external microcontroller [4]. The programmability of gain settings and filtering cutoff frequencies facilitates a variety of sensor interface circuits. Designed in a 0.6 μm CMOS

process, the chip requires a 5.0 V supply. Analog Devices released a data acquisition (DAQ) IC that includes a temperature sensor, a pair of digital-to-analog converters, and an 8052 microcontroller core in addition to the blocks in the Cirrus Logic chip [5] — a single-chip data acquisition system. The Analog Devices IC, the MicroConverterTM, supports multiple communication bus protocols, contains flash EEPROM for data and program storage, and is specified to operate with a supply voltage down to 3.0 V. Another reported single-chip DAQ system includes support for the IEEE 1451 standard transducer interface in addition to the basic architecture of the Analog Devices IC [6]. This chip, designed in a 0.6 μm CMOS process (with embedded EEPROM), operates down to a supply voltage of 2.7 V and facilitates in-circuit emulation. This paper describes a mixed-signal microcontroller which was designed specifically for use with solid-state sensors. The presented microinstrument increases the integration level over the ICs reported above by combining multiple sensor interface circuits, the data acquisition system, and the microcontroller on a single die.

This mixed-signal microinstrument, named the MS-8, is optimized, from instruction set definition to analog functionality, to economically support embedded sensor applications. The MS-8 supports these applications by increasing integration at the chip level, supporting in-circuit emulation techniques, employing system power reduction methodologies, and enhancing data acquisition and signal processing

* Corresponding author.

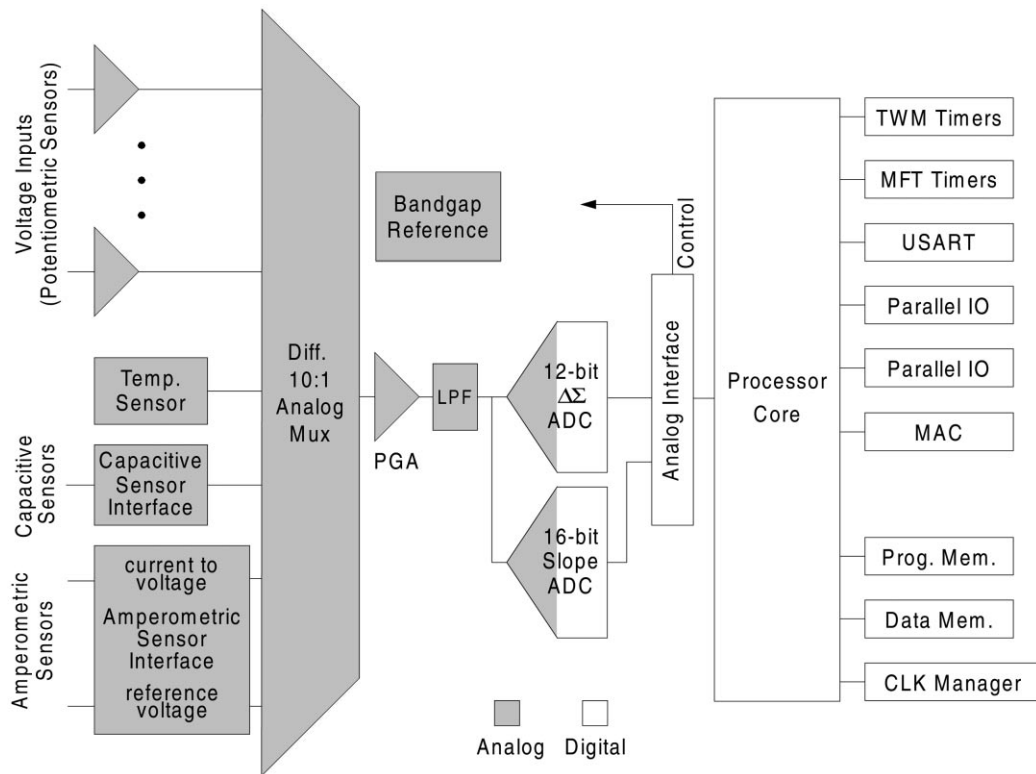


Fig. 1. MS-8 block diagram. The analog (shaded) and digital (unshaded) sections communicate through the analog interface block, treated as a peripheral by the processor core.

capabilities beyond simple microcontrollers. Also, a minimal version of the microinstrument can be implemented with as few as eight pins. See the block diagram in Fig. 1 [7].

To allow in-circuit emulation, the MS-8 includes hardware support for a single breakpoint or trace event; a single-pin development system interface; and instructions for halting the processor, single stepping through instructions, and reading/writing system registers. Single-cycle interrupt response and direct memory access (DMA) capabilities facilitate usage of the MS-8 in time-critical applications, and a 16-bit \times 16-bit hardware multiply, 40-bit accumulate block provides significant signal processing capability for a small microcontroller. To minimize power dissipation, data paths were limited to 8-bit widths, and the chip was designed to operate with a 3.0 V supply, in a 0.35 μ m CMOS process. In addition, a clock manager provides programmability of the clock frequency for the digital and analog circuits, and each analog block can be individually powered down under software control. This paper describes the digital and analog functionality of the MS-8 and presents sensor measurements taken with the microinstrument.

2. Digital core and peripherals

The right side of Fig. 1 depicts the digital portion of the MS-8, which includes the processor core, peripherals, and

memory [8]. The instruction set architecture (ISA) of the MS-8 is a blend of reduced instruction set computer (RISC) and complex instruction set computer (CISC) architectures. Instruction lengths vary in length, ranging from one to four bytes to increase code density, but the architecture is load/store to decrease control and data path complexity. The instruction encoding assigns the most frequently used instructions fewer bytes, decreasing the size of the program. Another benefit of the load/store architecture is that compilers can efficiently implement ANSI C. The simplified control and data path logic conserves power by not implementing unused or infrequently used addressing modes. This, coupled with increased code density decreases the overall power.

Program memory in this prototype version of the MS-8 consists of a 512 byte boot ROM and a 4KB RAM; a 512 byte RAM provides data storage. For application and testing versatility, both RAMs can be used as either instruction or data storage. In addition, off-chip memories can occupy sections of the 20-bit address space. Complete support for a single external memory segment is included on-chip; no board-level logic is required.

The MS-8 has a standard bus specification that allows third party soft IP peripherals to be easily integrated. The MS-8 interrupt arbitration is done with a distributed scheme using wired-OR signaling over the address and data bus. This reduces the number of signals between modules by

reusing existing wires and distributes the priority arbitration logic among all peripherals. Therefore, a system with only a few peripherals will not have the entire priority arbitration logic wasting area in the core.

To reduce dynamic power consumption, the MS-8 has a programmable clock manager (CLKMAN) that can divide the global clock frequency by up to 16, select a slow external clock, or put the system to sleep until a certain event occurs. While in the sleep mode, the global clock is stopped to all units except the timer/watchdog manager and the analog section. The clock manager also generates a four-phase non-overlapping clock for the $\Delta\Sigma$ ADC and other switched-capacitor circuits.

The parallel input/output (PIO) peripheral reads/writes 8-bit parallel data using the DMA functionality of the core. The PIO is programmed with an address and a number of bytes. After configuration, the PIO transfers or receives the data, signaling an interrupt at the end of the final byte.

The multiply accumulate unit (MAC) is capable of performing a single cycle multiply and accumulate. The two operands are 16-bit registers, and the accumulator is a 40-bit register. Without the MAC, a 16-bit \times 16-bit multiply accumulate would take many cycles to complete using a Booth (or similar) multiply scheme. In the MS-8 architecture, the Booth scheme would require multi-byte addition instructions, because the data path is only 8 bits. However, using the MAC, with its parallel multiplication, a multiply and an accumulate complete in a single cycle.

The analog interface block (AIB) peripheral includes 11 control registers and five data registers for the analog circuits. Control registers store configuration settings including which units to turn off, gain settings, and analog-to-digital (ADC) converter resolution. Data registers buffer samples from the ADCs and can be configured to generate interrupts after each conversion.

The universal synchronous/asynchronous receiver/transmitter (USART) performs synchronous or asynchronous serial communication. Programmable baud rates range from 4800 bps to 2.5 Mbps at a system frequency of 40 MHz. The serial protocol uses a single start bit and a programmable stop bit of 1, 1.5 or 2 bits. The USART also has programmable support for odd, even, or no parity.

The multifunction timer (MFT) employs two independent 16-bit counters, which can be used together for pulse-width modulation or as independent timers, or for input event capture. The clock sources include the pre-scaled system clock, the slow system clock, or a gated external clock for determining pulse widths. Each timer has a programmable interrupt level.

The timer/watchdog manager (TWM) is similar to the MFT except that the latter only has a single 16-bit counter. This timer operates on a pre-scaled system clock and is not stopped during sleep mode. The timer is used to generate wake-up events when the system is put to sleep and to recover from system faults. The TWM can also use synchronized external events as wake-up signals.

3. Analog core

The analog front-end (AFE), outlined in the left half of Fig. 1, includes a multiplexor which selects from an array of buffered voltage inputs (for potentiometric chemical sensors), the temperature sensor, a capacitive sensor interface (for pressure and acceleration sensors), and an amperometric chemical sensor interface. Signal conditioning provided by the programmable gain amplifier (PGA) makes the interface generic and increases the dynamic range of the system. A passive low-pass filter and a 12-bit analog-to-digital converter (ADC) complete the AFE. The analog functionality is further described in the remainder of this section.

The overriding goal for this prototype was to keep the design simple. This concept is reflected in the choice of architectures for the interface and signal processing circuits and the pervasive use of a general purpose opamp. For example, the analog core employs single-ended circuits, which have the benefit of power reduction, but are more susceptible to digital circuit induced substrate noise. Keeping the design simple reduced the design time and provided a baseline of performance upon which future versions can improve.

3.1. Temperature sensor

As shown in Fig. 2, the temperature sensor is comprised of a proportional to absolute temperature (PTAT) current source, represented by the circle, and a transimpedance amplifier. The PTAT current source, shown in Fig. 3, generates a current that is proportional to the thermal voltage, kT/q . M1–M4, Q1–Q2, and R_1 produce a current according to

$$I_1(T) = \frac{1}{R_1} \frac{kT}{q} \ln(A),$$

where A is the emitter area ratio of Q2 to Q1. Transistors M5, M6, and Q3 provide feedback to reduce the effects of the finite output resistance of M4; C_c compensates the feedback

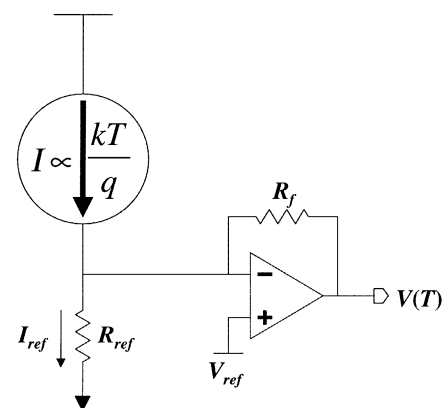


Fig. 2. Simplified schematic of the temperature sensor. The temperature sensor outputs a voltage derived from a current proportional to the thermal voltage.

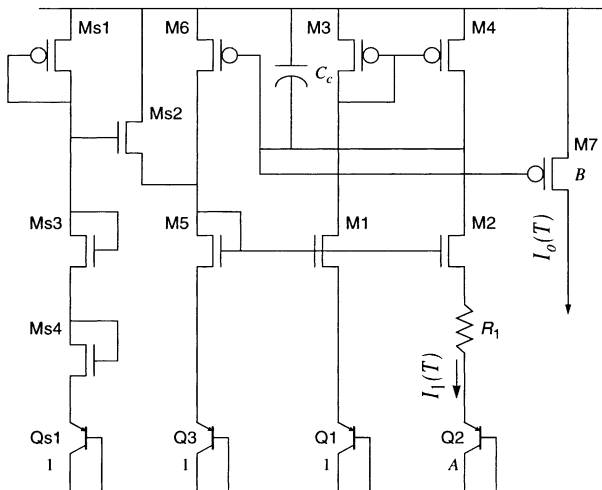


Fig. 3. Current source used in the temperature sensor. The output current is proportional to absolute temperature (kT/q).

loop to ensure stability. Ms1–Ms4 and Qs1 direct the circuit to the correct operating point upon startup. Since $(W/L)_{M3} = (W/L)_{M4} = (W/L)_{M6} = 1/B(W/L)_{M7}$, $I_0(T) = BI_1(T)$.

The temperature sensor in Fig. 2 compares the PTAT current to a reference current and generates a voltage according to

$$V(T) = -B \frac{R_f}{R_1} \ln(A) \frac{kT}{q} + V_{ref} \left(1 + \frac{R_f}{R_{ref}} \right),$$

where V_{ref} is a temperature-independent voltage generated by the on-chip bandgap reference. The values of the constants and resistors are chosen to set the output voltage in the middle of the supply range for room temperature and to set the gain. Note that since all resistors are constructed from p+ diffusion and appear in ratios in the above equation, temperature coefficients cancel. Temperature range and sensitivity are competing characteristics controlled by the gain of the programmable gain amplifier, discussed in Section 3.4.

This type of temperature sensor is employed in the MS-8 for two reasons. First, the PTAT current source also supplies bias current to the other analog circuit blocks, making double use of the circuit with its associated power dissipation and area. Second, the linear nature of the output voltage response makes calibration straightforward.

3.2. Sensor interfaces

The primary function of sensor interface circuitry is to read and amplify the transducer output signals. As described below for capacitive sensors, the readout operation can involve the conversion of a capacitance signal to an electrical signal (voltage). Some sensors require, or their performance can be improved by, closed loop operation, where

the interface circuitry provides actuation to the sensor in addition to readout. The remainder of this section describes the interface circuitry included in this implementation of the MS-8.

3.2.1. Voltage buffers

The buffered voltage inputs provide a high-impedance interface for potentiometric sensors (and other voltage signals) and accommodate rail-to-rail signals (0–3.0 V). Potentiometric chemical sensors have output impedances on the order of 100 MΩ; therefore, they require readout circuitry with high input impedance. A CMOS rail-to-rail opamp configured as a voltage follower provides the necessary high input impedance buffer. The opamp is described later. Buffers not in use can be powered down selectively.

3.2.2. Capacitive sensor readout

The capacitive interface circuit converts a capacitance to a voltage. Capacitive-based pressure sensors and accelerometers experience a capacitance change in response to an applied force [2]. In the readout circuit shown in Fig. 4 [9], a switched-capacitor charge integrator compares the resulting sensor capacitance to a reference capacitor to produce a voltage as follows:

$$V_{out} = V_A \left(\frac{C_S - C_{ref}}{C_f} \right) + V_{ref},$$

where C_S and C_{ref} are the sensor and reference capacitors, respectively; V_A is the amplitude of the clock, ϕ ; and V_{ref} is the on-chip reference voltage. This architecture was chosen because of the circuit’s insensitivity to input parasitic capacitances and ease of implementation. Note that the circuit provides ports for up to four capacitive sensors. As the equation shows, the readout circuit generates a voltage linearly proportional to the sensor capacitance.

When ϕ transitions to the high state, the reset switch on the integrator is closed and the opamp charges the sensor capacitance. When ϕ falls, the feedback capacitor, C_f integrates a charge proportional to the difference between the sensor and reference capacitors. The MS-8 provides several

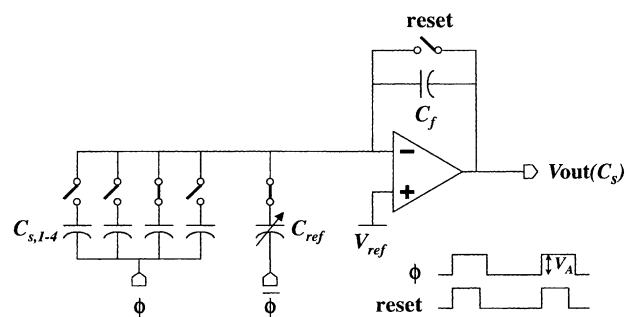


Fig. 4. Simplified circuit diagram of the capacitive readout circuit. The circuit facilitates recording of up to four external capacitive sensors and has a programmable reference capacitor bank.

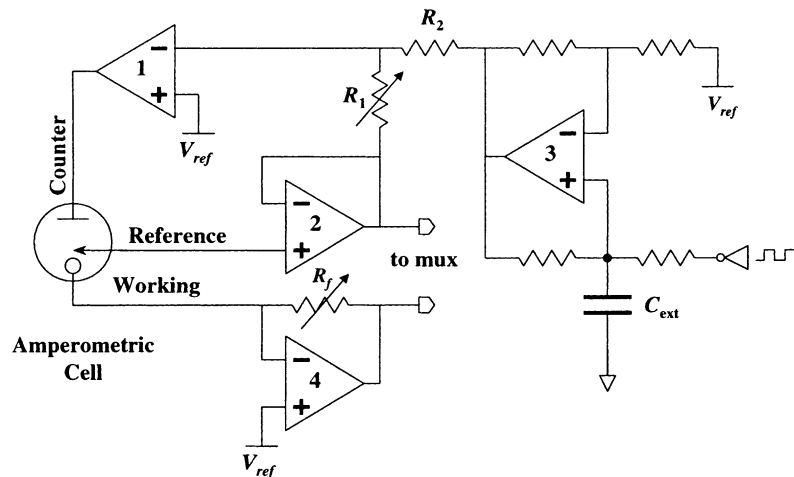


Fig. 5. Simplified diagram of the amperometric sensor interface circuit and off-chip sensor. The circuit applies a triangular wave to the sensor to facilitate cyclic voltammetry, or can use any externally supplied voltage to drive the amperometric cell.

options for the reference capacitor: an on-chip programmable capacitor array, an external capacitor, or a combination of both. The internal capacitor array has capacitors in the range of 250 fF to 15 pF in the steps of 250 fF. This granularity is insufficient for general applications, but is suitable for demonstration of the prototype: the reference capacitor should be close in value to the sensor capacitance so as to not saturate the output voltage.

3.2.3. Amperometric sensor interface

Amperometric sensors are frequently employed to detect dissolved gases or uncharged molecules in liquid. As shown in Fig. 5, these sensors typically include three electrodes: counter, reference, and working [10]. The sub-circuit containing opamps 1 and 2 and resistors R_1 and R_2 form a potentiostat circuit which employs feedback to regulate the voltage applied across the reference and working electrodes, independent of the current through the cell. In this version of the MS-8, a simple triangular wave generator, consisting of opamp 3 and the external capacitor, C_{ext} , generates an applied voltage suitable for cyclic voltammetry. For other types of amperometry, the user can stop the clock under program control and provide an external voltage in place of the capacitor to excite the sensor with arbitrary waveforms. For example, Kissinger and Heineman [11] describe many types of amperometry, including differential pulse and square-wave. The next generation MS-8 will include a digital-to-analog converter to generate arbitrary waveforms without the use of an off-chip capacitor. Current sensing occurs at the working electrode with a simple transimpedance amplifier which generates a voltage proportional to the cell current (opamp 4). To accommodate sensors having differing current magnitudes, R_f can be programmed through the AIB or supplied off chip. The prototype has only two resistor settings, 3.75 and 242 k Ω , suitable for currents in the range of 400 μ A to 100 nA (with the use of the PGA). More on-chip resistor values are needed to facilitate a wider range

of sensors — most of the measurements reported herein were with an external resistor.

3.3. Analog multiplexor

The 10:1 differential analog mux consists of two 10:1 single-ended muxes. Each of the previously mentioned mux inputs feeds a channel of both single-ended muxes. With this connection scheme, the mux provides maximum versatility in selecting inputs. The AIB contains a register and logic for configuring the mux under program control.

Measurements appear to indicate crosstalk (capacitive coupling) between channels. To combat this problem, the next generation MS-8 will ground the mux channels not selected.

3.4. Programmable gain amplifier

The programmable gain amplifier ideally boosts the input signal to the full-scale range of the analog-to-digital converter. In this implementation of the MS-8, the PGA is designed after the standard three-opamp, two-stage instrumentation amplifier (see Fig. 6). The first stage provides

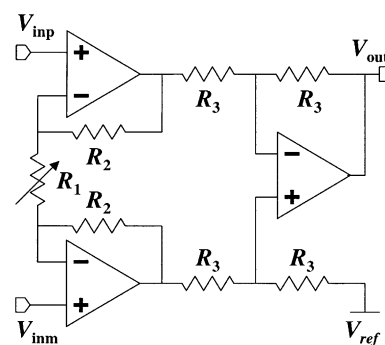


Fig. 6. Programmable instrumentation amplifier. Gain is set by an on-chip programmable resistor (R_1).

high input impedance, common-mode rejection, a differential input, and programmable gains of 1–61 in steps of 10 V/V. Testing with actual sensors has revealed that smaller gain steps are needed to realize the full dynamic range of the system. Stage two of the amplifier provides low output impedance, differential to signal-ended conversion, and level shifting. Use of the low noise, rail-to-rail opamp (described later) in both stages increases the dynamic range of the PGA. At the output of the PGA, a simple low-pass filter reduces amplifier distortion and aliasing (resulting from the analog-to-digital converter sampling process). A control register in the AIB stores the gain settings.

The drawbacks of the three-opamp architecture include area and power penalties. These penalties are exacerbated by the fact the opamp is designed for general purpose use and is thus larger and consumes more power than required for this application.

3.5. Bandgap reference

The bandgap reference, based on the kT/q current source of Fig. 3, supplies bias current and a voltage reference for the analog circuitry. An opamp in a negative feedback configuration provides voltage gain to boost the reference voltage to mid-rail and buffering to drive the reference to the $\Delta\Sigma$ ADC, programmable gain amplifier, temperature sensor, potentiostat, and off chip. To avoid start-up transient behaviors, the bandgap circuit is powered even in low-power mode; the buffer, however, has power-off support.

3.6. Analog-to-digital converters

Two selectable data converters produce a digital representation of the analog signal. The single-slope ADC has higher resolution than the $\Delta\Sigma$ ADC but is more susceptible to substrate noise. Because of this limitation, the single-slope converter will be useful for studying noise-reduction methods in this mixed-signal environment. The ramp voltage for the converter is generated by supplying a fixed current, derived from the bandgap reference, to an off-chip capacitor.

The first-order $\Delta\Sigma$ ADC (the primary data converter) is shown in Fig. 7. $\Delta\Sigma$ modulators trade bandwidth for resolution, which makes the architecture suitable for this application, which requires moderate to high resolution data conversion of low frequency sensor outputs. In addition, the combination of integration and the feedback reduces in-band substrate noise produced by the switching activity of the digital circuits. The $\Delta\Sigma$ architecture also relaxes precision requirements on the analog circuitry, which makes this type of ADC suitable for design in a digital process [12].

A counter in the AIB filters and decimates the oversampled, single-bit ADC output. The default counter width is 12 bits, but the user can configure the counter to any width up to and including 16 bits. The AIB stores both the counter output and the single-bit oversampled output, allowing the

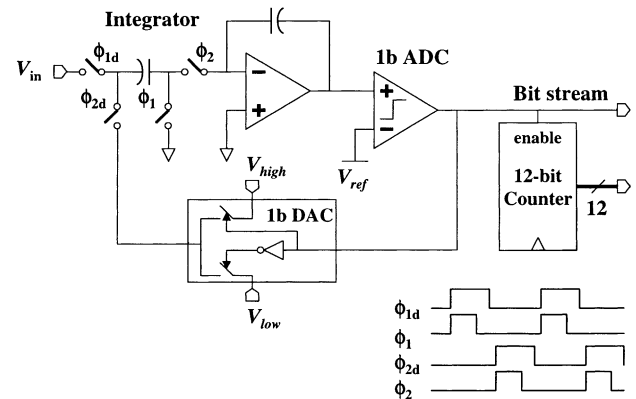


Fig. 7. Simplified diagram of the first-order $\Delta\Sigma$ modulator. Filtering is provided by the counter or with software and the MAC peripheral.

processor core to provide the filtering and decimation, if desired by the user. The counter requires minimal area, but forces an oversampling ratio of 2^n for n -bit data, which is not an efficient use of power and puts stringent demands on the unity gain frequency and slew rate of the opamp in the integrator. More sophisticated decimation schemes could be implemented in the microcontroller core.

Under program control, the clock manager divides the system clock to generate the sampling clock and permits the user to vary the sampling frequency according to the application. In addition, the clock manager generates the four clock phases shown in Fig. 7. This clocking scheme reduces the impact of switch-induced charge injection at the high impedance nodes.

3.7. Rail-to-rail opamp

The custom opamp of Fig. 8, based on a topology in [13], was designed for use in the analog circuits described previously. Since in some cases the opamp drives the signal off chip (e.g. the reference voltage and test points), the opamp is designed to drive 200 pF loads. To maximize dynamic range in this low-voltage environment, the opamp processes rail-to-rail input signals and drives rail-to-rail output signals. Transistors M30–M32 maintain constant input transconductance, g_{mi} over the input common mode range by maintaining the sum of the currents in the two input differential pairs (M1–M4) constant. A constant g_{mi} reduces distortion and makes the Miller compensation more efficient in terms of capacitor area and overall power dissipation. The transistors in the input differential pairs and output stage (M26 and M27) operate in weak inversion to reduce input referred noise and offset and to maximize input- and output-stage transconductance for a given current. M19–M24 provide class AB biasing to the output stage to reduce power.

This opamp is designed to have low input referred offset voltage and noise over the full input common mode range, a temperature range of -40 to 85°C , and a supply range of 2.5–3.3 V. Since the opamp drives off-chip signals, the output stage consumes around 75% of the total power to

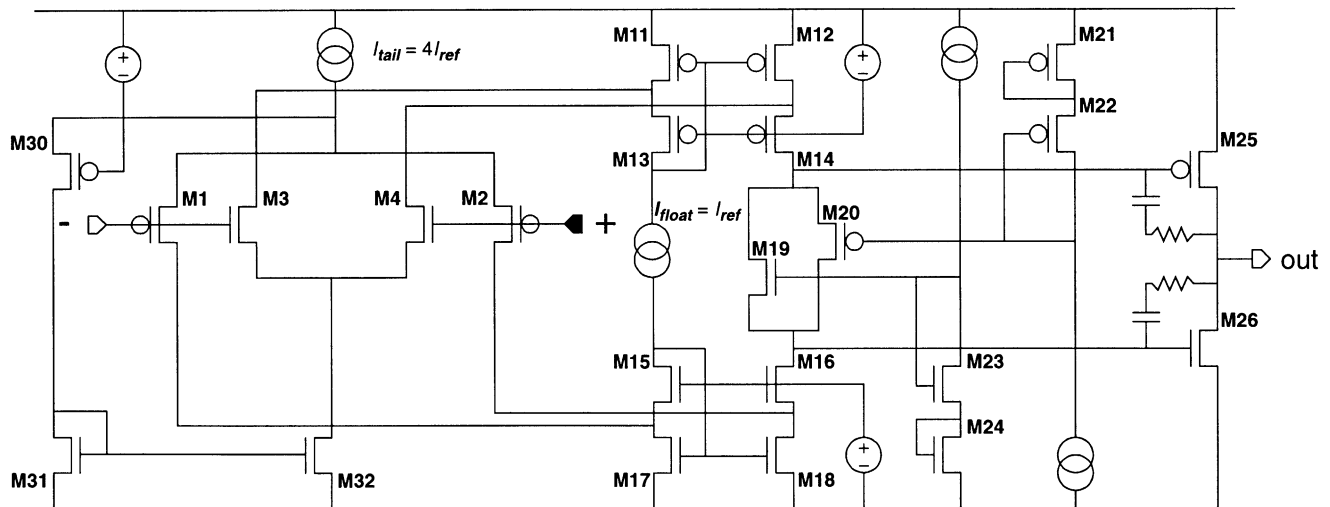


Fig. 8. Simplified schematic of the rail-to-rail opamp without bias circuits. The input differential pairs (M1–M4) and output stage (M25 and M26) operate in weak inversion to reduce input referred noise, offset, and power.

provide sufficient unity gain phase margin. As mentioned before, this opamp is used throughout in the analog circuit blocks, even where load capacitance is minimal. A more efficient design, in terms of area and power, would be realized by employing a custom amplifier for each block.

The MS-8 does not include any offset control in the readout channels, which could potentially lead to saturation if high gains are employed. But, as mentioned above, the opamp is designed to have a low offset and measurements reveal that the offset drift with temperature is also low relative to a 3.0 V supply (see Section 5.1). Future implementations of the MS-8 will likely provide offset cancellation, especially for lower voltage operation.

4. Physical design

Fig. 9 is a die photomicrograph of the MS-8. The major components visible are the RAMs, ROM, analog circuitry, and the microcontroller core. The die is approximately $3.8 \text{ mm} \times 4.1 \text{ mm}$. Nearly one-quarter of the core area, $1.39 \text{ mm} \times 1.42 \text{ mm}$, is dedicated to the analog circuits. RAM and ROM memory cells occupy a little less than half of the core. The die was fabricated in a $0.35 \text{ }\mu\text{m}$ digital CMOS process and contains over 300,000 transistors. For testing purposes, 103 signal pins and 12 power pins were bonded out. However, some applications would require as few as eight pads to be bonded to pins.

The memory drivers are placed as far from the analog circuits as possible to reduce substrate coupling effects. In addition, the analog core has ample substrate contacts surrounding the sensitive circuitry, and dedicated V_{DD} and ground connections to further combat switching noise. Finally, enforcing greater-than-minimum metal-to-metal spacings for sensitive signals reduces crosstalk between interconnect lines (at the expense of area).

5. Experimental results

The MS-8 digital core was verified to be functional at 40 MHz, 3.0 V, and room temperature using an HP82000 digital tester. While simulations predict static current draw around 3.3 mA (full power) and $15 \text{ }\mu\text{A}$ (standby), measurements reveal 16 mA and $850 \text{ }\mu\text{A}$ currents, respectively. Table 1 shows simulated power for each analog circuit block and the total measured power. Note that most of the unexpected power dissipation is from the digital circuits. The authors suspect leakage in the RAMs. The discrepancy between the simulated and measured power in the analog core is also under investigation.

Initial testing of the AFE demonstrates the usefulness of the device in embedded sensor applications. The USART supports bidirectional serial communications between the MS-8 and a laptop computer running LabView (National Instruments); programs were downloaded to the chip and digital samples from the ADC were transferred to LabView for recording and analysis over this serial link. The remaining sections report initial results of measurements of potentiometric and amperometric chemical sensors, pressure sensors, and the temperature sensor. All the sensor interfaces and digital components have been verified to be functional. The opamp has also been characterized; the results of which are described first.

5.1. Opamp characterization

Table 2 shows the typical opamp characteristics. These measurements were taken under nominal conditions (room temperature, 3.0 V supply) from opamps packaged separately. The open-loop gain, slew rate, and unity gain bandwidth are sufficient to enable oversampling ratios on the ADC above 2^{12} and sampling rates in excess of 1 MHz, according to [12].

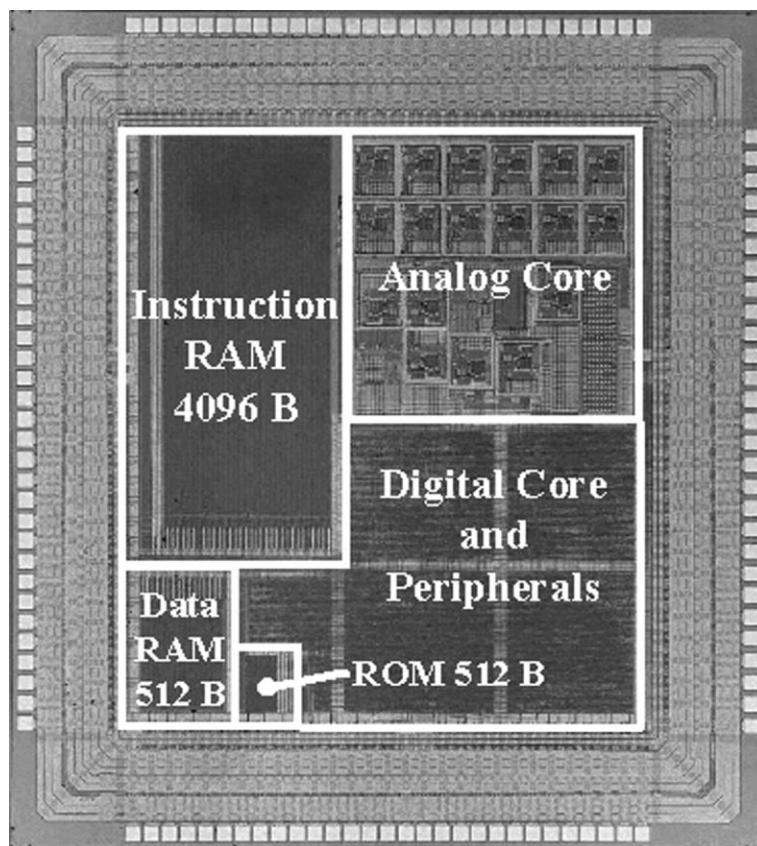


Fig. 9. MS-8 die photomicrograph. The chip was fabricated in a 0.35 μm national semiconductor process and measures 3.8 mm \times 4.1 mm.

5.2. Potentiometric sensor results

Fig. 10 shows the calibration curve for over seven decades of KCl concentration for a solid-state potentiometric sensor selective to potassium ions (K^+) [14]. A commercial double-junction reference electrode was used for the reference. The inset contains the time response of the sensor; each step represents a 10-fold increase in potassium concentration. An external electrode connected to the on-chip reference generator sets the potential of the solution to 1.5 V to keep the signal in the range of the interface circuitry. The sensor has a linear response from around the minimum detectable limit of

10^{-5} M to about 1 M, as shown in the figure. Using the microcontroller to linearize the response with a higher-order fit would extend the detection range. Theory predicts a slope of 59 mV per decade; non-idealities in the sensor and gain error in the PGA are possible reasons for the slope discrepancy.

5.3. Amperometric sensor results

In a class of amperometry called chronoamperometry, a voltage is applied between the working and reference electrodes of sufficient potential to cause oxidation or reduction

Table 1
Measured and simulated power dissipation for the analog core^a

Unit	Simulated (μW)	Measured (μW)	Conditions (f_{sample})
Buffer	540		
Temperature sensor	570		
Capacitive sensor interface	550		100 kHz
Amperometric sensor interface	2160		
Bandgap (buffered)	540		
PGA	1620		
$\Delta\Sigma$ ADC	736		1 MHz
All units on	9416	9154	
All units off	45	420	

^a Note that the bandgap reference circuit always remains powered.

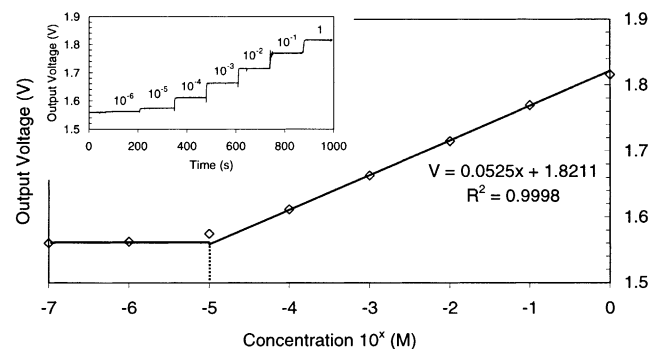


Fig. 10. K^+ calibration curve. The background solution is 0.05 M trizma base (Sigma, St. Louis, MO) adjusted to pH 7.4 with H_2SO_4 . The PGA gain is set to 1 V/V.

Table 2
Typical measured characteristics of the CMOS opamp^a

Symbol	Parameter	Conditions	Measured
V_{OS}	Offset voltage		500 μ V
	Offset drift		0.7 μ V/ $^{\circ}$ C
PSRR+	Positive power supply rejection ratio	$V_{cm} = V_{DD}/2$	70 dB
PSRR–	Negative power supply rejection ratio	$V_{cm} = V_{DD}/2$	80 dB
CMRR	Common mode rejection ratio	$V_{cm} = V_{DD}/2$	70 dB
A_O	Open-loop gain	$R_L = 2$ k Ω	90 dB
SR	Slew rate		0.7 V/ μ s
GBW	Gain-bandwidth	$C_L = 200$ pF; $R_L = 2$ k Ω	2.5 MHz
I_S	Supply current		200 μ A
ϕ_m	Phase margin	$C_L = 200$ pF; $R_L = 2$ k Ω	75 $^{\circ}$
e_n	Input referred	1 kHz	<35 nV/ $\sqrt{\text{Hz}}$
	Voltage noise	100 kHz	<16 nV/ $\sqrt{\text{Hz}}$

^a Results shown are for nominal conditions: 3 V supply and room temperature.

currents. Fig. 11 shows the response of the sensor for an ascorbic acid concentration of 0.02 M. Ascorbic acid has an oxidation potential of approximately 0.6 V for platinum electrodes. Therefore, the on-chip potentiostat was configured to apply a square wave with a peak-to-peak voltage of 0.8 V between the reference and working electrodes. After charging currents subside, the sensor output current follows the relation

$$i \propto K \frac{C}{\sqrt{t}},$$

where C is the concentration, t the time, and K is a constant [10]. The spikes in Fig. 11 represent charging and discharging currents. If the measurement is always taken at the same point on the curve, the output current will be linear with concentration. Fig. 12 plots the sensor output for ascorbic acid concentrations from 10^{-6} to 0.1 M. As expected, the response is linear.

5.4. Pressure sensor results

The initial test of the capacitive interface circuit was performed with an 8.2 pF external reference capacitor and

known capacitances to represent the sensor; see Fig. 13. As expected, the figure shows that the output voltage has a linear response to capacitance.

Capacitive pressure sensors, however, demonstrate a non-linear relationship between pressure and capacitance. Fig. 14 shows the results of a micromachined pressure sensor undergoing a pressure sweep from as low as 10 to around 1350 Torr. The sensor used is based on work by Chavan and Wise at the University of Michigan [15]. This particular non-bossed sensor experiences a change in capacitance of only 340 fF over the pressure range.

An attempt at a linear curve fit reveals that the sensors do not respond linearly to pressure. A quadratic fit, however, produces an excellent calibration curve; the MS-8 can support the linearization of transducer output signals using the MAC unit.

5.5. Temperature sensor results

To test the temperature sensor, the MS-8 and test-board were placed in an oven. The temperature was ramped slowly from room temperature, 22 $^{\circ}$ C, to 80 $^{\circ}$ C, as measured by a mercury thermometer. At each temperature, the chip was

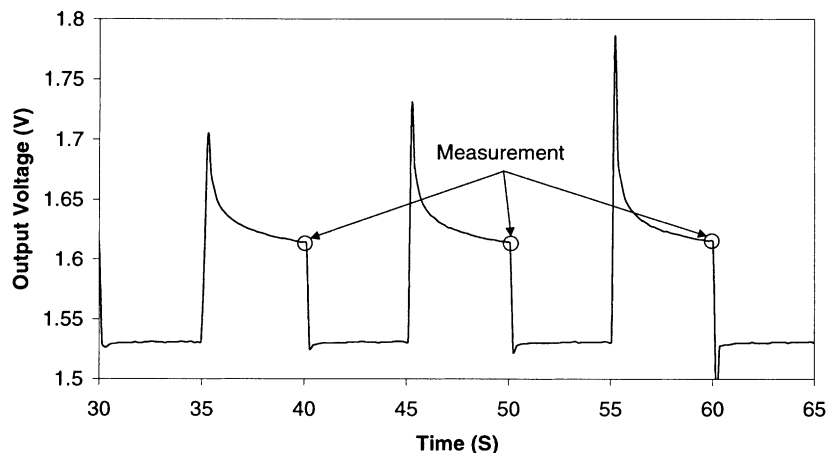


Fig. 11. Output current (converted to voltage) of an amperometric sensor in a 0.02 M ascorbic acid solution. A square wave with amplitude 0.8 V_{pp} was applied to the sensor. The circles denote measurement intervals. The background solution is a standard phosphate buffer with a pH of 7.6.

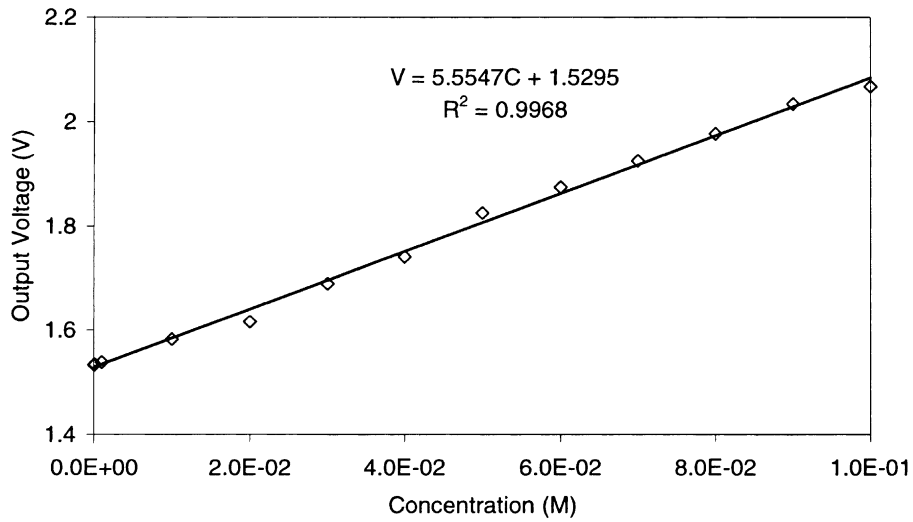


Fig. 12. Ascorbic acid calibration curve for an amperometric sensor. The response is linear over six decades of ascorbic acid concentration.

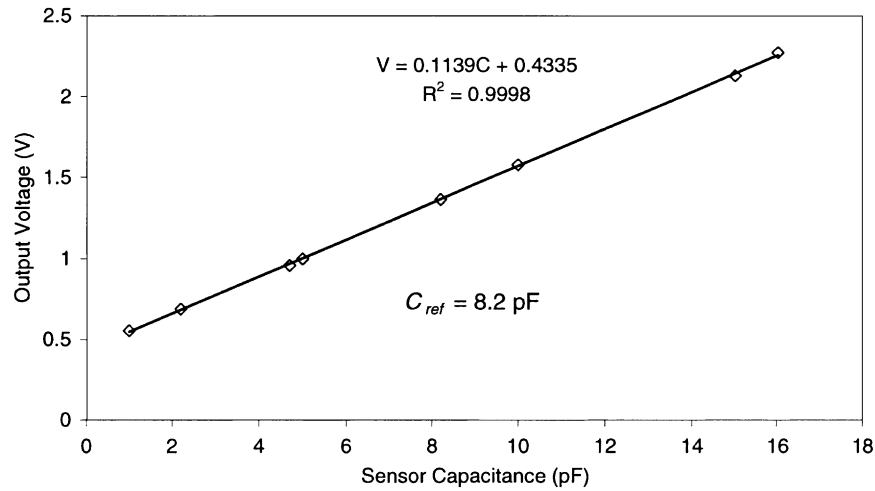


Fig. 13. Capacitive sensor readout circuit test. Fixed capacitors ranging from 1 to 16 pF were used in this test. The PGA gain is set to 1 V/V.

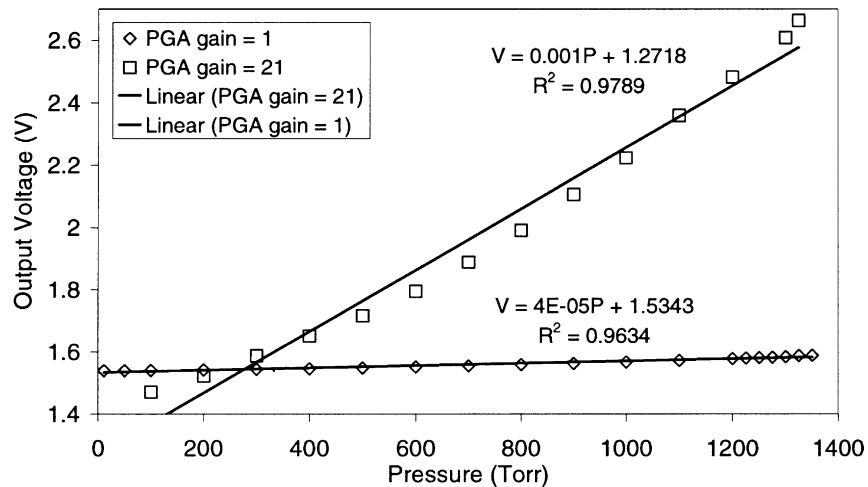


Fig. 14. Capacitive pressure sensor response to a pressure sweep. The plot compares the results for two PGA gain settings: 1 and 21.

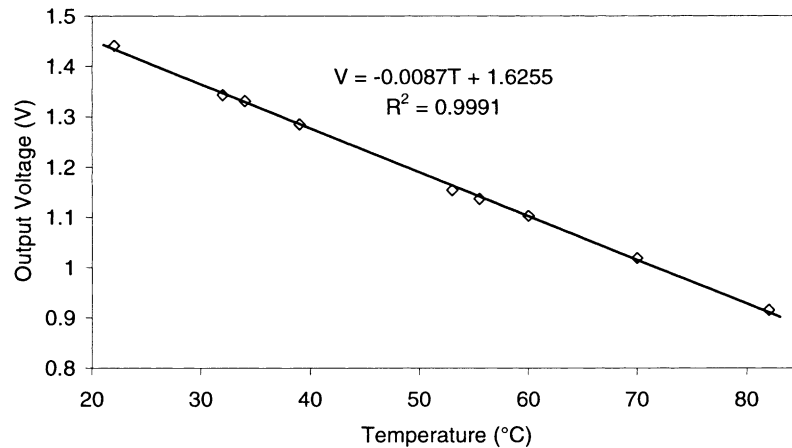


Fig. 15. Temperature sensor response from 25 to 80°C with the PGA gain set to 11 V/V.

allowed to reach equilibrium within the oven environment before a digital voltage reading was recorded. Fig. 15 shows, as expected, that the temperature sensor output voltage has a linear relationship to temperature.

6. Conclusions

The MS-8 described here is the first implementation of an on-going project that coordinates efforts among analog designers, compiler writers, and low-power digital designers to develop a low-power, low-cost, and multipurpose sensor interface and data acquisition system. This single-chip microinstrument contains a programmable analog front-end capable of interfacing to a variety of sensors. The integrated microcontroller and peripherals support digital filtering and compensation of sensor outputs, timing control for sampling multiple sensors, and communication with a host system. The usefulness of the MS-8 in embedded sensor applications is evidenced by the initial results presented.

Acknowledgements

The authors acknowledge the financial support from National Semiconductor Corporation and the technical support from these individuals: E. Dietz, H. Verhoeven and D. Vieira of National Semiconductor for discussions concerning the design of the opamp and review of the analog layout; M. Lortz and M. Embacher from National Semiconductor for support with the physical design; A. Drake from the University of Michigan for assistance with digital testing; and Andy DeHennis from the University of Michigan for providing the pressure sensors.

References

- [1] K.D. Wise (Ed.), Scanning the issue, Proc. IEEE Integrated Sens., Microactuators, Microsyst. (MEMS) 86 (Special Issue) (1998) 1531–1533.
- [2] A.V. Chavan, A. Mason, U. Kang, K.D. Wise, Programmable mixed-voltage sensor readout circuit and bus interface with built-in self-test, IEEE ISSCC Digest of Technical Papers, February 1999, pp. 136–137.
- [3] H.D. Goldberg, The batch fabrication of integrated chemical sensor arrays, Ph.D. Dissertation, The University of Michigan, Ann Arbor, MI, 1993.
- [4] A. Bindra, Ultra-low-noise data-acquisition IC tackles multiple sensors, Electron. Design 47 (22) (1999) 59–60, 62.
- [5] Analog Devices, Inc., ADuC824 data sheet, <http://products.analog.com/products/info.asp?product=ADUC824>.
- [6] T. Cummins, E. Byrne, D. Brannick, D.A. Dempsey, An IEEE 1451 standard transducer interface chip with 12-b ADC, two 12-b DACs, 10-KB flash EEPROM, and 8-b microcontroller, IEEE J. Solid-State Circuits 33 (12) (1998) 2112–2120.
- [7] P.L. Bird, R.B. Brown, T.N. Mudge, L. Hong, B. Khailany, M.R. Guthaus, MS-8 design specification, Technical Report, The University of Michigan, Ann Arbor, MI, 1999.
- [8] R.B. Brown, P.L. Bird, M.R. Guthaus, K.L. Kraver, B. Khailany, MS-8 microarchitecture, Technical Report, The University of Michigan, Ann Arbor, MI, 1999.
- [9] S.M. Sze (Ed.), Semiconductor Sensors, Wiley, New York, 1994.
- [10] A.J. Bard, L.R. Faulkner, Electrochemical Methods, Wiley, New York, 1980.
- [11] P.T. Kissinger, W.R. Heineman (Eds.), Laboratory Techniques in Electroanalytical Chemistry, Marcel Dekker, New York, 1984.
- [12] B.E. Boser, B.A. Wooley, The design of sigma-delta modulation analog-to-digital converters, IEEE J. Solid-State Circuits 23 (6) (1998) 1298–1308.
- [13] R. Hogervorst, J.H. Huijsing, Design of Low-Voltage, Low-Power Operational Amplifier Cells, Kluwer Academic Publishers, Boston, 1996.
- [14] H.J. Yoon, J.H. Shin, H. Nam, G.S. Cha, T.D. Strong, R.B. Brown, Solid-state ion sensors with a liquid junction-free polymer membrane-based reference electrode for blood analysis, Sens. Actuators B 64 (2000) 8–14.
- [15] A.V. Chavan, K.D. Wise, A batch-processed vacuum-sealed capacitive pressure sensor, in: Proceedings of the International Solid-State Sensors and Actuators Conference (Transducers'99), Vol. 2, Chicago, IL, 16–19 June 1997, pp. 1449–1452.

Biographies

Keith L. Kraver received the BS degree in electrical engineering from Arizona State University in 1995. He received an MS in electrical

engineering (VLSI) in 1997 from the University of Michigan and is currently a PhD candidate. His research interests include low-voltage and low-power analog circuit design, mixed-signal design, and deep-submicron analog circuits.

Matthew R. Guthaus received his BSE in computer engineering and MSE in electrical engineering from the University of Michigan in 1998 and 2000, respectively. He is currently pursuing his PhD in electrical engineering at the University of Michigan. His research interests include low-power architecture, algorithm specific microprocessors, and computer-aided design of integrated circuits.

Timothy D. Strong received his BS degree in electrical engineering from Michigan Technological University in 1992. After working for 3 years in microprocessor design and verification at IBM, he began graduate studies at the University of Michigan. He received an MS in electrical engineering in 1997 and is currently a PhD candidate. His current research is in IC fabrication and integrated chemical sensing via ion-selective electrodes and cyclic voltammetry.

Peter L. Bird received the MS and PhD degrees from the University of Michigan in 1982 and 1987. He worked as the principle hardware and software architect for Applied Dynamics International, helping to design and implement a development system for high speed embedded controllers. He worked as the principle architect for the Advanced Computer Research Institute (ACRI), a French start-up company established to develop a high performance, heterogeneous multi-processor system. He is currently adjunct professor of electrical engineering and computer science at the University of Michigan where he is responsible for the senior level course in compiler design and implementation. His research interests include language design and implementation, application of parsing techniques to software engineering problems, and computer architectures for high performance and embedded systems. He holds a US patent for a high performance memory system.

Geun Sig Cha received his BS degree from Korea University in 1977 and his PhD in analytical chemistry from the University of Michigan in 1989. He continued his research at the University of Michigan as a joint research fellow in the Department of Chemistry and Electrical Engineering and Computer Science until January 1991. He is now an associate professor of analytical chemistry in the Department of Chemistry at Kwangwoon University. His current research interests involve the development of polymer membrane-based ion-, bio- and gas-sensors and the design of enzyme-linked competitive and non-competitive binding assay methods.

Wolfgang Höld was born on 30 May 1965 in Guenburg, Germany. He received the Dipl. Ing. in electrical engineering (focus on communication electronics) in 1989 from the Technical University, Augsburg, Germany. In 1989, he joined National Semiconductor, Germany, as a product engineer for 4- and 8-bit microcontrollers. From 1990 to 1994, he held positions in product engineering and design engineering for microcontrollers at National Semiconductor, Santa Clara, CA. In 1994, he established a design center for microcontrollers at the National Semiconductor European Headquarters, Germany. The design center focused on 8- and 16-bit microcontroller cores and communication modules. His current interests and activities include developing best design practices for HDL coding and design reuse standards. He is presently responsible for the 16-bit Compact-RISCTM CPU, including product development.

Richard B. Brown received his BS and MS degrees in electrical engineering from Brigham Young University in 1976. He then worked in computer design and instrumentation until returning to school in 1981. He received an electrical engineering PhD at the University of Utah in 1985. His dissertation was on integrated solid-state chemical sensors, which included development of a custom MOS fabrication process and integration of multiple transducers with analog and digital circuitry. In September 1985, he joined the Department of Electrical Engineering and Computer Science, University of Michigan, where he serves as associate chair. His areas of current research are SOI circuits, mixed-signal integrated circuits, and solid-state chemical sensors.