

A LOW-POWER GENERIC INTERFACE CIRCUIT FOR CAPACITIVE SENSORS

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ABSTRACT

This paper presents a low-power generic interface circuit compatible with smart microsystems and capable of interfacing with a large variety of capacitive sensors. The interface chip is highly programmable, can communicate with an external microcontroller over a standard sensor bus, supports sensor self-test, and includes a temperature sensor. The circuit can interface with up to six external sensors and contains three programmable internal reference capacitors in the range of 0.15-8pF. The chip measures 3.2mm x 3.2mm in a standard 3 μ m single-metal double-poly p-well process, dissipates less than 2.2mW from a single 5V supply and can resolve input capacitance variations of less than 1fF.

INTRODUCTION

Smart microsystems combining a large mix of sensors, actuators and electronic circuitry are of increasing demand in a wide range of applications, including those in distributed sensing and control systems, industrial process automation, instrumentation, and environmental monitoring. Capacitive microsensors are very attractive for these microsystems due to their low power, high sensitivity, and self-test capabilities [1]. However, the base capacitance and sensitivity of these capacitive sensors can vary over a wide range, which must be covered by the interface circuit. Hence, there is a growing need for a low power generic interface for use with capacitive sensors in smart microsystems. Although there have been numerous readout circuits introduced for capacitive sensors [2-3], to date a generic interface has not been reported. Such an interface circuit should be able to read out various capacitive microsensors with a wide range of base capacitance and sensitivity, communicate with the main microsystem controller, support self-test and self-calibration, support multi-ranging for a single sensor, dissipate low power, and occupy very small area with no external components. This paper introduces such an interface circuit.

The interface chip is currently being utilized in the microsystem for environmental monitoring shown in Fig. 1 [1]. The following sections provide a description of the interface chip and its functions. First, the current microsystem which employs the interface chip is briefly described. Then, the interface chip architecture is presented, followed by a description of its major building blocks. Finally, measurement and test results for the fabricated chip are presented.

MICROSYSTEM DESCRIPTION

The microsystem utilizes an open architecture with a standard sensor bus [1], which allows the system to be populated with various sensors and actuators as required by the

application. For instance, the currently developed microsystem accommodates sensors for a variety of environmental parameters, including temperature, barometric pressure, humidity, and acceleration [1]. The heart of the microsystem is a microcontroller unit (MCU) that provides the system intelligence and allows for data storage as well as software routines for each sensor to perform in-module sensor calibration, digital compensation, and self-test. The MCU communicates with the front-end transducers via the sensor interface chips and a nine-line sensor bus as illustrated in Fig. 1. The interface chip is a critical component of this overall system because it allows a standard microcontroller to communicate and collect data from a variety of sensors. Once sensor data has been collected and calibrated in-module, it can be stored or transmitted out through either a hardwired serial I/O port or an on-board telemetry device.

The sensor bus is a central part of the microsystem architecture, which provides access to multiple sensors/actuators while using a minimum number of interconnects without any loss of functionality. The sensor bus consists of nine lines: three for power, two handshaking lines used with a clock and serial data line for synchronous serial communication, a data output line, and a data valid/interrupt signal [1]. The three power leads are the system supply, ground reference, and a switched reference voltage for devices that can be turned off during a low-power system sleep mode. For synchronous communication with the front-end devices, a chip enable and data strobe provide handshaking for use with a programmable-frequency clock and a serial data line. The last

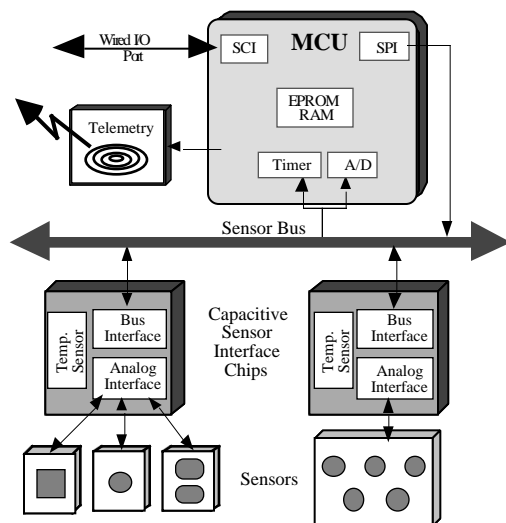


Figure 1: Block diagram of a multi-parameter sensing microsystem.

two lines of the sensor bus are for sensor data output, which can be an analog level or a frequency-encoded bitstream, and data valid which signals the MCU when valid data is present on the data out line. Data valid is also used as an interrupt from the front-end devices that can initiate an event triggered sensor readout.

INTERFACE ARCHITECTURE

Figure 2 shows the block diagram of the interface chip. This chip utilizes a low-noise front-end charge integrator to read out the difference between the sensor capacitance and a reference capacitor [3]. Communication with the MCU is performed over the sensor bus and is handled by the bus interface unit. Serial data transmitted over the bus is received, decoded, and applied to control the other circuit blocks illustrated in Fig. 2. The input multiplexer enables the chip to interface with up to six sensors. Furthermore, the chip can be digitally programmed to operate with one of three external/internal reference capacitors. The on-chip reference capacitors are laser trimmable in a range of 0.15pF to 8pF. Programmability of the reference capacitors allows the chip to interface with capacitive sensors having a wide range of base capacitance and also provides offset control.

The chip analog signal path consists of an input multiplexer, the input charge integrator, a gain stage, an output sample/hold circuit, and an output multiplexer. The gain stage can be programmed on-line to any of its three gain settings. These gains can be used to accommodate input sensors with different sensitivities or for multi-ranging a single sensor and are set by laser trimming the on-chip capacitors. The overall readout sensitivity can be varied from 0.23 mV/fF to 73.5 mV/fF using both digital programming and laser trimming, which gives an effective gain variation from 1 to 312. The output multiplexer provides access to the sensor bus for both the capacitive readout circuitry and the on-chip temperature sensor. The interface chip additionally supports self-test and self-calibration. A 3b on-chip DAC can be utilized to generate a variable-amplitude two-phase clock for driving the sense and reference capacitors in each input charge integration cycle. The variable amplitude clock can also be used to apply a varying electrostatic force to the sensor for self-test and self-calibration.

CIRCUIT BUILDING BLOCKS

The readout circuit is a switched-capacitor circuit consisting of a low-noise charge integrator, a digitally-programmable gain stage and a sample/hold circuit as shown in Fig. 3. Since the

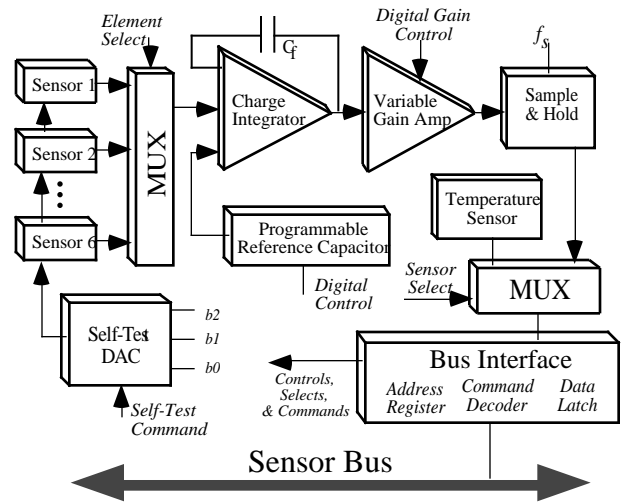


Figure 2: Diagram of the capacitive sensor interface chip showing the major circuit blocks.

circuit operates from a single supply, an internal analog ground reference level, half way between the supply level and ground, is generated on-chip and is shown as V_{ref} in Fig. 3. Clock switching noise is reduced by using sized dummy switches at the high-impedance nodes; a fully differential circuit is not utilized to save power and die area. The control clocks of the dummy switches are slightly delayed so that better charge compensation occurs when the actual switches are turned off completely.

The input switches are controlled so that at each instant only one of the sense capacitors (C_s) and one of the reference capacitors (C_{ref}) are connected to the circuit. During ϕ_1 , the reset switch of the charge integrator is closed and C_s is charged through the charge integrator output. Once ϕ_1 goes low, a packet of charge proportional to the difference between C_s and C_{ref} is integrated on the feedback capacitor of the first stage (C_{f1}). Meanwhile, the second stage integrator is in reset mode and either C_{g1} , C_{g2} , or both C_{g1} and C_{g2} charge to the output level of the first stage. The gain of the second stage is determined by the ratio of the total capacitance switched into its input to the feedback capacitance (C_{f2}). Clock phases ϕ_3 and ϕ_4 are slightly delayed ϕ_1 and ϕ_2 clocks which become active only when gain 1 or 3 is selected. Similarly, ϕ_5 and ϕ_6 are delayed ϕ_1 and ϕ_2 clock phases that are active only when

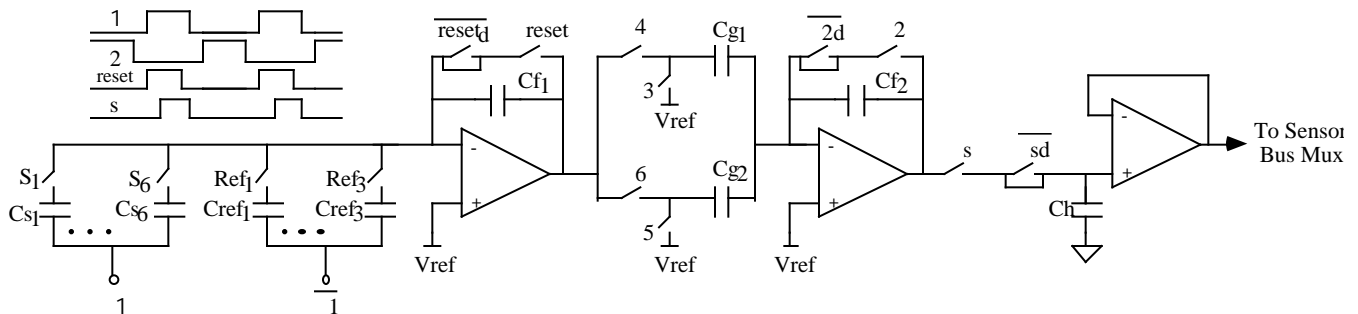


Figure 3: Schematic diagram of the switched-capacitor readout circuit.

digital gain 2 or 3 is set. Therefore, the gain of the second stage is selected by controlling switching of C_{g1} and C_{g2} at its input. During ϕ_3 (ϕ_5) clock phase, the charge stored on C_{g1} and C_{g2} capacitors is integrated on C_{f2} . Finally, the output of the second stage is sampled and held at the input of the third stage during ϕ_6 .

Figure 4 shows the schematic of the opamp used in the switched-capacitor circuit. The opamp is designed to provide low noise and good high frequency PSRR with low power dissipation, and to drive capacitive loads over a wide range. Transistors M1-M5 form the input differential stage, with large PMOS transistors (M1-M2) used to reduce noise. The main gain stage is a class AB cascode output stage consisting of M8-M11. The dominant pole is determined by the load capacitance, which alleviates the need for a compensation capacitor and effectively improves the high frequency PSRR. The load capacitance can vary over a wide range without causing stability problems and is driven efficiently by the class AB output stage.

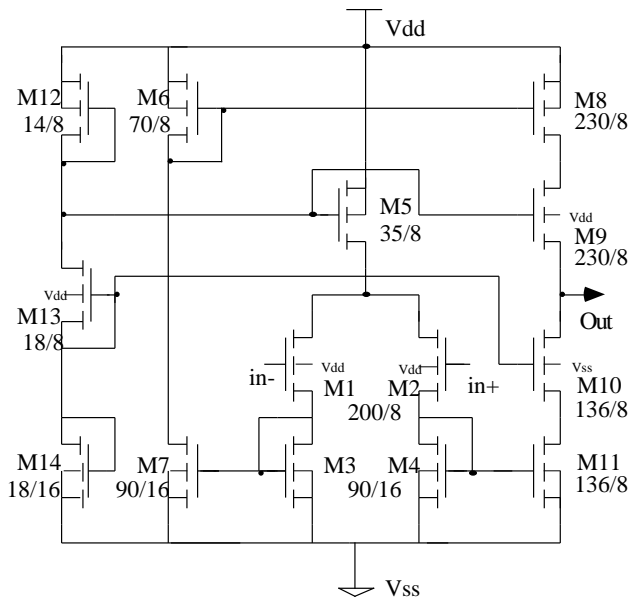


Figure 4: Schematic diagram of the low noise operational amplifier used in the readout circuit front-end.

The self-test DAC consists of three switched current mirrors driving an on-chip polysilicon resistor. The DAC output changes the amplitude of the clock when a control line is set. The temperature sensor is an on-chip oscillator with a temperature-dependent output frequency.

The bus interface circuitry consists of a series of shift registers that load input data, a laser-programmable 4b chip address comparator, command and element address decoders, and a 4b data latch accessed by a specific write command. The sensor bus data format provides a 5b element address to access up to 32 element addresses. On the interface chip three of these element address bits are used to select one of the six capacitive sensors or the on-chip temperature sensor while the remaining two bits are decoded as reference capacitor select lines.

TEST RESULTS

The chip has been fabricated using a standard $3\mu\text{m}$, single metal, double poly p-well CMOS process at the University of Michigan. Figure 5 shows a photograph of the chip, which measures $3.2\text{mm} \times 3.2\text{mm}$ and dissipates less than 2.2mW from a single 5V supply. Approximately 85% of the power dissipation is due to the quiescent currents of the five opamps integrated on the chip. Table 1 summarizes the chip specifications. Test results have shown full circuit functionality with an input capacitance resolution of less than 1fF and a maximum readout clock rate of 50kHz . Although carefully sized dummy switches are used in the switched-capacitor circuit, the resolution is still limited by the clock switching noise rather than kT/C and input amplifier flicker noise. Figure 6 shows the output of the charge integrator with a 6pF reference capacitor as the sensor capacitance is varied from 3pF to 8pF . Figure 7 illustrates the output of the readout circuit as the input capacitance changes in 0.5pF steps. Programmability of the gain is illustrated in Fig. 8, where the measured output is plotted for various digital gain settings.

The temperature dependence of the readout circuit offset and sensitivity has been measured over the range from 0 to 60°C . The circuit sensitivity is not significantly affected by its operating temperature and in all measurements the temperature dependence of the output voltage has been dominated by that of offset. The main source of offset temperature dependence is due to amplification of the first stage opamp offset in the second gain stage. The maximum temperature dependence of offset is equivalent to less than $0.16\text{fF}/^\circ\text{C}$ input-referred capacitance. Note that the temperature dependence of the readout circuit does not adversely affect the performance of the overall microsystem since temperature compensation is performed in-module by the system microcontroller of the system.

The microsystem shown in Figure 1 has been implemented with two interface chips used to link a Motorola 68HC11 MCU to sensors for pressure, humidity, and acceleration [1]. The low power and capacitive readout capabilities of the interface chip make it a vital part of this battery-powered microsystem, which provides a prototype for long-life, wireless, distributed multi-parameter sensing systems.

CONCLUSIONS

In this paper a generic interface circuit for capacitive sensors has been presented. The chip can interface with a large variety of capacitive sensors, is highly programmable, supports communication over a standard sensor bus with a microcontroller, and supports self-test. The chip dissipates less than 2.2mW from a single supply, can operate with readout clocks as high as 50kHz and resolves input capacitance variations of less than 1fF .

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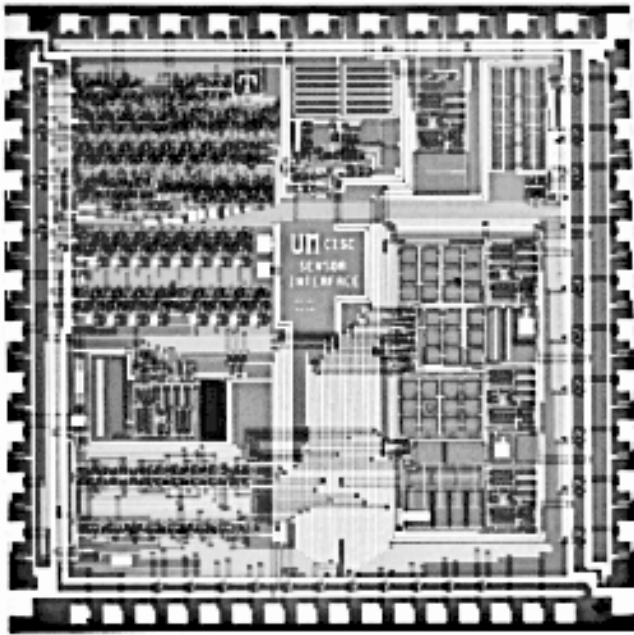


Figure 5: Photograph of the capacitive interface chip.

Table 1: Summary of the interface chip specifications.

Number of sensing channels	6 Capacitive + Temperature
Reference capacitor channels	3 internal/external, Internal capacitor programmable 0.15pF-8pF
Chip address	4 bits
Sensitivity 1 [mV/fF]	0.23-22.3
Sensitivity 2 [mV/fF]	0.23-50.9
Sensitivity 3 [mV/fF]	0.47-73.5
Resolution	< 1fF input capacitance
readout clock	< 50 kHz
DAC	3 bits for self-testing
Supply	Single 5V
Power dissipation	< 2.2 mW
Temperature Dependence of Offset	< 0.16 fF/°C (input referred capacitance variation)

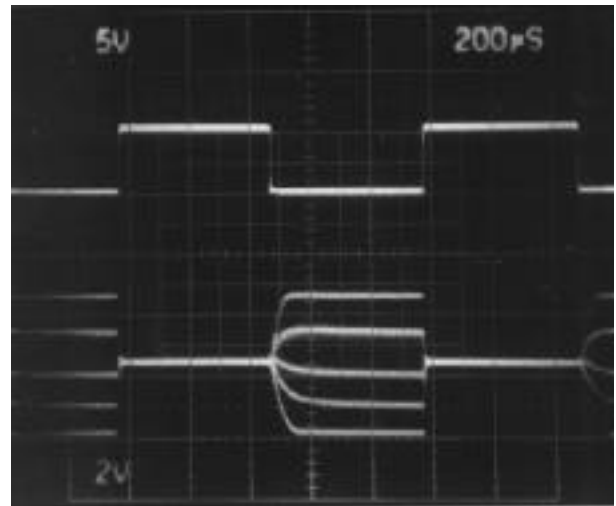


Figure 6: Upper trace: Reset control of the input charge integrator; Lower trace: Output of the charge integrator with a 6pF reference capacitor as the sensor capacitance changes from 3pF to 8pF.

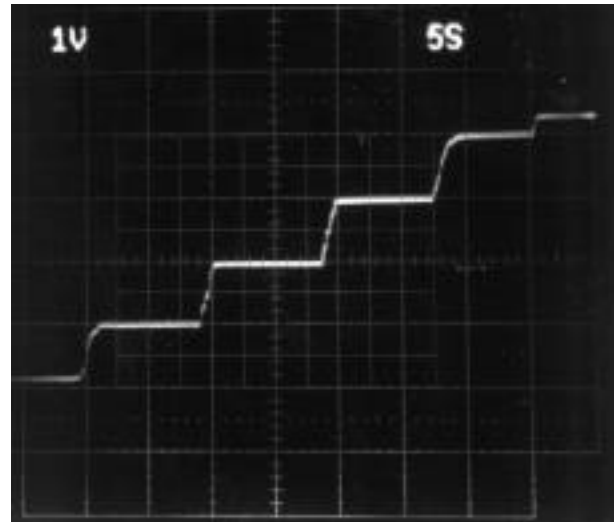


Figure 7: Readout circuit output as the input capacitance changes in 0.5pF steps; No laser trimming for gain adjustment was performed and the lowest second-stage gain is selected.

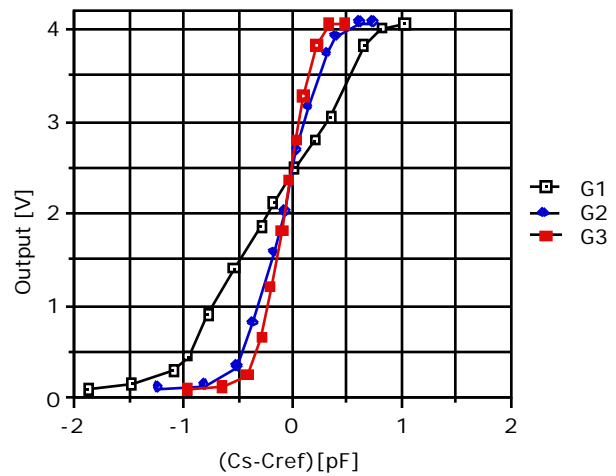


Figure 8: Measured output of the chip as a function of the input capacitance for different second-stage gain settings.