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InP- AND GaN-BASED DEVICES AND MMICs FOR SIGNAL CONTROL AND GENERATION

by

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A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
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To my parents, my fiancée Denise, and my friends,
all of whom have helped and supported me
during the time of my graduate studies and,
hopefully,
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TABLE OF CONTENTS

LIST OF FIGURES

Figure

LIST OF TABLES

Table

CHAPTER 1
INTRODUCTION

1.1. Status of Compound Semiconductor RF Technology

Compound semiconductor technology has in the past served specialized applications dealing primarily with defense systems. Its commercial potential became more evident over the last decade with the increased interest in wireless applications, such as cellular and automotive electronics. Over this period, shipments of III-V-based devices and integrated circuits (IC) have grown four times to almost $10 billion dollars [1]. Despite the fact that this represents only a small fraction of the semiconductor market where silicon remains the key technology, the expansion of compound-semiconductor applications to commercial systems confirms their vitality and uniqueness. Transition of GaAs- and InP-based technology from research laboratories into commercial sector was prompted by the decrease of government funding and commercialization of microwave and millimeter-wave spectra, which occurred in early 1990s. Shift from performance-driven low-volume military applications to cost-driven high-volume commercial applications was accompanied by departure from labor-intense hybrid technology. Monolithic microwave integrated circuit (MMIC) technology was much more compatible with the low-cost minimum-assembly requirements of the high-volume commercial production and was, therefore, intensively pursued. The use of high-performance devices, such as high-electron mobility transistors (HEMTs) and heterojunction bipolar transistors (HBTs) was on the other hand limited, since it required expensive epitaxial layers. First commercial applications favored low-cost GaAs MESFET MMICs, which were made using ion-implantation techniques and offered performance competitive with and often superior to RF Si electronics. However, strong competition in the commercial market and

declining costs of epitaxial growth have revived strong demand for high-performance MMICs employing GaAs- and InP-based HEMTs and HBTs [2]. In fact, today, GaAs-based HBTs is the leading technology for cellular-handset power-amplifier applications [1].

This growth of compound-semiconductor analog electronics is expected to continue in the future, as there is an increasing demand for larger communication bandwidths and higher frequency of operation. Among high-volume emerging applications where compound semiconductor RF technology has a unique role are local multiple-point distribution systems (*LDMS*) at *28GHz* [3], next-generation communication and imaging systems at *94GHz* [45], and W-band automotive radars at *77GHz* [6]. At these frequencies, InP-based HEMT electronics has advantages over GaAs in terms of output power, power-added-efficiency, and noise. InP-based HBTs are also expected to compete with GaAs-based technologies for cellular handset applications since they allow lower voltage operation and improved power-added-efficiency. Provided that cost is not prohibitively high, it is expected that InP-based MMIC technology will find significant commercial application for microwave, millimeter- and sub-millimeter-wave systems projected for the next decade [2].

The 1990s have also been the witness to the emergence of wide bandgap GaN-based semiconductors with increased electrical strength as viable power device technology. Thus, GaN-based HEMTs demonstrated unattainable by conventional III-V materials power density of *12W/mm* [7]. Moreover, the use of wide bandgap materials not only allows increased output power, but also extends the temperature tolerance and the radiation hardness [8]. Due to their unique high-power high-frequency characteristics, GaN-based devices are expected to dominate high-power microwave applications [9]. These include base stations for wireless and satellite communications, automotive electronics and defense applications.

This thesis deals with compound semiconductor devices and circuits for signal control and generation applications. The materials considered for this purpose include both InP- and GaN-based semiconductors as outlined in detail in the next sections.

1.2. Role of Signal Control and Generation Circuits in W-band Automotive Radars

Millimeter-wave circuits such as switches, phase shifters, amplifiers, and oscillators demonstrating good performance over larger bandwidths are desired for various applications such as emerging W-band collision-warning, collision-avoidance, and adaptive cruise-control systems (CWS, CAS, ACC) system for the automotive industry [6]. Commercial success of automotive radars is largely contingent upon the development of a monolithic millimeter-wave integrated circuit technology suitable for mass production. Monolithic transmitter-receiver modules integrating power and low-noise amplifiers, mixers, and oscillators operating up to W-band frequency are currently being developed [6, 10]. Such MMICs employ high-performance InP- or GaAs-based HEMTs for signal amplification while microwave diodes are used for signal generation, mixing, and switching.

A simplified schematic of a W-band automotive transmitter-receiver front-end module for pulse Doppler configuration is demonstrated in Figure 1.1 following [11]. This design employs a single microwave signal generator (MSG) to provide both transmit (TX) and local oscillator (LO) signals for mixer down-conversion. The signal generation function is implemented using a millimeter-wave oscillator. Two single-pole double-throw (SPDT) transceiver switches are used to reconfigure the module between "transmit" and "receive" positions. A steering-beam single-pole triple-throw (SP3T) switch is used to select an antenna corresponding to one of the three scanning beams. When the front-end is in the "transmit" (TX) state, the TX signal from the oscillator is directed the selected antenna, while the mixer diode is isolated from all three antennas and the MSG. In the "receive" (RX) state, the transceiver switches connect LO and RX signals to the mixer diode, while the transmission path is blocked. The isolation of the SPDT switches provides the measure of how well the TX or the LO signals are blocked from leaking to undesired ports. The insertion loss is used to characterize power loss in the TX and RF signals incurred due to presence of the switches in the signal path. Low insertion loss ($<1dB$) and high isolation ($>30dB$) are desired for optimal performance.

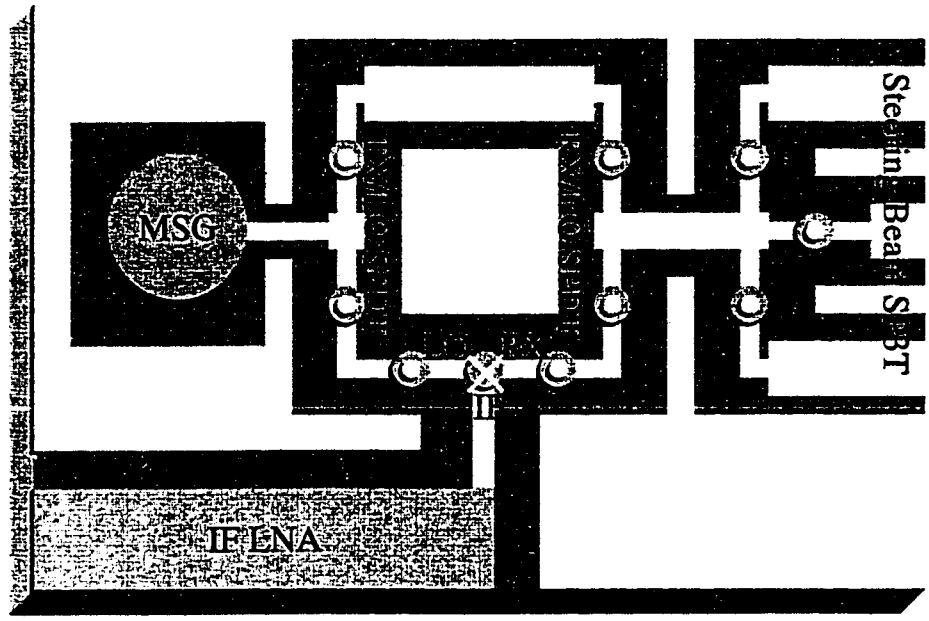


Figure 1.1. Block diagram of a W-band automotive front-end module

During the operation, the microwave signal generator is coherently switched between the TX and LO frequencies while the transceiver switches are changed between the TX and RX configurations. The TX signal is sent to a target via one of the selected antennas. After it is reflected from the target, the RF signal is received by the antenna and coherently down-converted by a mixer diode to IF frequencies.

The resolution of the pulse-Doppler radar largely depends on the modulation rate (switching time) of the transceiver switches. Faster switching is required for reduction of "blind range", which measures minimum distance for successful operation. Switching time of *1-2ns* is considered acceptable for automotive applications at present time.

The far range of the radar can be limited the maximum power of the transmitted signal. The transceiver and steering beam switches used in the automotive radars are required to provide switching operation up to high power levels of *13-16dBm* [6, 11].

Viable semiconductor devices for implementation of high-power low-loss and high-isolation transceiver switches include microwave PIN diodes and switching FETs. Chapter 4 of this thesis deal with InP-based PIN MMIC switches, while Chapter 6 presents development of wide-bandgap GaN-based HFETs for high-power monolithic switching applications in an attempt to respond to the automotive requirements of low-loss, high-isolation, and high-power switching.

It should be noted that the task of high-power signal generation at W-band is also very challenging. Among various solutions are HEMT- and HBT-based MMICs [10, 12], as well as high-power low-noise Gunn diode oscillators [11]. While the power and frequency capabilities of MMIC oscillators are constantly improving, microwave diode oscillators remain semiconductor devices of choice for W-band and beyond generators. However, the output power available from conventional GaAs- and InP-based Gunn diodes is shown to decrease sharply beyond *100GHz* [13]. An application of GaN-based Gunn diodes for high-power signal generation at W-band and higher frequencies is addressed in Chapter 7.

1.3. Semiconductor Devices for Control Applications

Monolithic millimeter-wave transceivers integrate signal generators, power amplifiers, down-conversion mixers, low-noise amplifiers, and transceiver switches. High-performance GaAs- and InP-based HEMTs can be used to develop all of the above functions [10], while microwave diodes are best suited for signal generation, down-conversion, and switching applications [6]. Thus, W-band signal generators are often realized using Gunn diodes, while monolithic PIN diode switches are predominantly used for control applications at this frequency.

In general, microwave control circuits can employ FETs (such as MESFETs, MISFETs, and HEMTs), Schottky diodes, or PIN diodes as switching elements. The advantages and disadvantages of using these types of devices are listed in Table 1.1.

MESFETs and HEMTs represent the mainstream millimeter-wave MMIC technology and, thus, FET-based transceiver switches can be easily integrated on the same chip with transmit and receive MMICs. Because the operation of FETs is based on majority carriers with short lifetimes, they generally demonstrate high switching speeds. However, the high resistance of the channel results in large insertion loss and small isolation. The channel resistance is reduced in HEMTs due to the increased 2DEG mobility and charge density in these heterostructure devices, but performance at millimeter-wave frequencies is still poor due to their large OFF-state capacitance inherent in three-terminal devices.

Table 1.1. Microwave diodes and FETs in microwave control circuits

Devices	Advantages	Disadvantages
MESFETs, MISFETs, and HEMTs	• Compatible with MMIC technology • Majority carriers operation (fast switching)	• High channel resistance • Low cutoff frequency
Schottky Diodes	• Ease of integration with FETs • High cutoff frequency • Majority carrier operation	• Low power capability
PIN Diodes	• High cutoff frequency • High power-handling capability • Low ON-state resistance • Layer structure compatible with HBTs and optoelectronics	• Minority carrier operation • Layer structure not compatible with FETs
MEM Switches	• Very low insertion loss • Very high isolation • Low DC power consumption	• Very slow switching • High control voltage • Short lifetime

The power-handling capability of MESFETs and HEMTs is limited by the small breakdown voltage of the Schottky-gate diode and the channel. Excellent microwave power results recently demonstrated using wide bandgap semiconductors [7] suggest a possibility of increasing the power-handling capabilities of FET switches by employing GaN-based HFETs due to increased channel electrical strength, high electron mobility, and excellent 2DEG properties. Wide-bandgap metal-insulator-semiconductor FETs (MISFETs) can be used to further improve power characteristics due to an increased electrical strength of the insulator of the MIS gate. Overall, FETs are best suited for low-frequency low-power applications where insertion losses are not critical while GaN-based HFETs and MISFETs are promising candidates for high-power microwave applications. Use of FET switches at high frequency requires resonance of the OFF-state capacitance with an inductive component. Approaches of this type, combined with the high-breakdown features of GaN-based HFETs offer a possibility of high-power millimeter-wave switches using wide bandgap GaN-based semiconductors with high chemical resistance, thermal stability, and radiation hardness [14].

Schottky diodes are easily integrated with active FET-based circuits because the layer structure and fabrication steps are very similar. Diodes with very small OFF-state

capacitance are feasible, but a combination of low breakdown voltage and small area leads to poor power-handling capability. Schottky diodes are best employed in high-speed low-power control circuits.

Microwave PIN diodes combine the advantages of low ON-state resistance and low OFF-state capacitance which leads to very high cutoff frequencies and offers low insertion loss and high isolation performance up and beyond W-band frequencies. High breakdown voltage of PIN structures lends itself to high power-handling capability offered by PIN diodes. However, switching of PIN diodes between the ON and the OFF states occurs by injection and removal minority carriers in and out of the I-layer. Since the switching operation involves minority carriers with long lifetimes, the modulation speeds of PIN diodes is fundamentally slower than in Schottky diodes or FETs. Compound semiconductors demonstrate shorter minority-carrier lifetimes, which allows significantly faster recovery times in GaAs- and InP-based PIN diodes (*~1-2ns* [15]) compared with Si-based PIN diode switches (*~100ns* [16]) that is sufficient for most practical radar applications. While PINs and HEMTs use different layer structures, the two devices can be successfully integrated on the same substrate [17]. Moreover, switching PIN diodes can be fabricated as part of standard GaAs or InP-based HBT technology, which extends the range of their applications [18].

Microelectromechanical systems (MEMs) operating using electrostatic and mechanical-tension forces have recently been applied to microwave and millimeter-wave switching [19, 20]. While MEMs do not truly qualify as semiconductor control devices, early results with MEM switches are promising and demonstrate very low insertion losses (*~0.2dB*), and high isolation (*~30dB*) up to *40GHz*. MEMs also consume miniscule DC power (*~1μW*), but have severe limitations in terms of switching speed (*<1MHz*), actuation voltages (*>10V*), and reliability (*~10^6* switching operations). Further improvements of MEM switches in these areas are expected to take place as this novel technology is matured.

Overall, switching PIN diodes offer the unique combination of high cutoff frequency, low loss, high power-handling and adequate switching-rate capabilities. FETs on the other hand are best employed for lower-power applications. Power handling of

FET switches can be improved by using wide bandgap materials such as GaN in the channel or employing an insulating gate such as in MISFET designs. Both types of devices are addressed in this thesis: PIN diodes are described in Chapters 2 and 3 of this thesis, while wide bandgap GaN-based HFETs and MISFETs are presented in Chapter 6.

1.4. Review of Microwave PIN Diode Switches

High power-handling capability, high cutoff frequency, and low insertion loss won PIN diodes a well deserved central place in the design of microwave control circuits, such as attenuators [21], transceiver switches [4, 16], and phase shifters [22].

In historical perspective, Ge- and Si-based PIN diodes were used for microwave switching as early as in 1956 [23, 24]. Circuits were implemented in a hybrid fashion and successful operation up to millimeter-wave frequencies was demonstrated by 1980s [25]. However, Si devices became less attractive since they were incompatible with the emerging GaAs-based MMIC technology [26]. First successful fabrication of switching GaAs-based PIN diodes was reported in 1983 [27]. In the next several years, various millimeter-wave GaAs PIN diode switches were reported based on different fabrication methods including ion-implanted [16], hybrid-mounted [28], and epitaxially-grown vertical PIN structures [15, 29]. The latter showed superior performance due to the higher quality of the PIN structures and lower parasitics, and quickly replaced FETs as switching elements of choice at millimeter-wave frequencies.

Since single-pole single-throw (SPST) and single-pole double-throw (SPDT) switches are essential elements in design of transmitter-receiver modules, research and development of monolithic PIN switches was continuous all the way through the 90s as demonstrated by the results of Figure 1.2. The diagram, presented in the figure, provides a roadmap of important stages in development of microwave PIN diode switches. Reported in the literature performance of PIN diode switches was plotted on the diagram as a function of frequency. This diagram uses as a measure of performance on/off switching ratio (isolation [dB] *less* insertion loss [dB]). Such definition favors isolation over insertion loss, since high isolation is harder to achieve in a MMIC environment while most MMIC switches have insertion loss between *1* and *2dB*. Each reported result is

marked by a three-lines-long legend. The first line lists the name of the company or research lab where the switch was made and the year it was reported. The second line states what monolithic technology — microstrip (MS) or coplanar (CPW) was used in switch design, and what semiconductor was used for fabrication of the switches. Presented data include results obtained with beam-lead Si PINs diodes, GaAs PIN diodes, and InP-based InGaAs PINs of this work. The third line of the captions describes the design of the switch (SPST or SPDT) and number of diodes employed in an SPST arm.

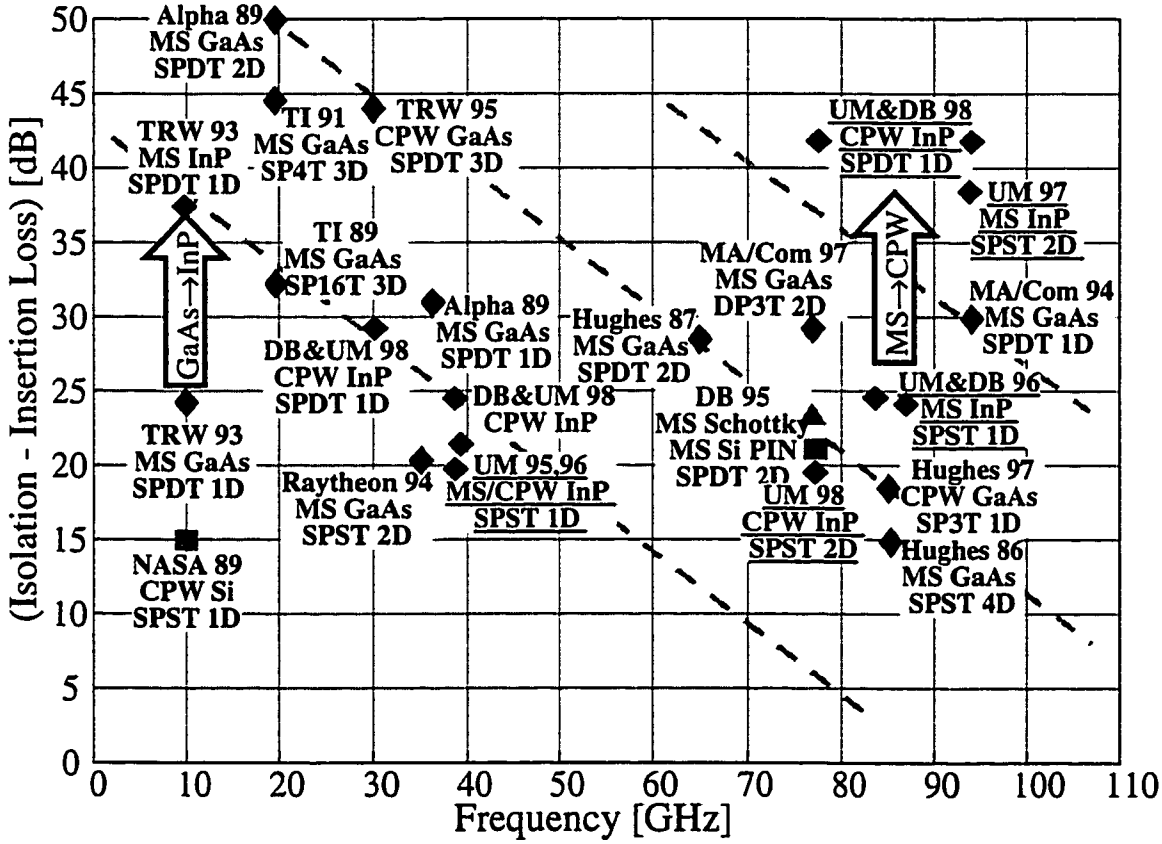


Figure 1.2. Performance-frequency diagram demonstrating development of monolithic PIN diode switches.

Consideration of the switch design and the number of diodes employed are important since, for reasons which will be explained later in this thesis, the isolation in a switch with multiple throws is *~6dB* higher than in a single-throw switch and the isolation of an SPST with two diodes (SPST-2D) is roughly twice that of an SPST-1D. Therefore, the performance of an SPST-1D switch with an on/off switching ratio of *24dB* is roughly equivalent to that of an SPST-2D with *48dB* or that of an SPDT-1D with *30dB*.

At the beginning of this work, most research and development work on monolithic microwave switches concentrated on GaAs-based microstrip PIN diode switches [4, 22], while InP-based PIN diodes have been primarily explored for optoelectronic circuits, such as receiver OEICs [17]. Thus, a state-of-the-art microstrip transceiver SPDT switch employing epitaxial GaAs PIN diodes was reported in 1994 and demonstrated *1dB* insertion loss and *30dB* isolation at *94GHz* [4]. However, there are a number of applications where InP-based InGaAs PIN diodes can be more suitable than the conventional GaAs-based PINs. For example, the compatibility of InGaAs PIN diodes with high-frequency InP-based electronics offers several additional advantages for the realization of millimeter-wave functions, such as the possible integration of switching PIN diodes with InP-based HBTs and HEMTs. Thus, integrated photoreceivers with HBT- and HEMT-based amplifiers have been demonstrated using InGaAs PIN photodiodes [17, 30]. The higher operation frequencies achievable with the use of InP-based electronics opens the road to building new imaging-radar systems, as well as to minimizing the size and therefore the cost of automotive collision avoidance systems.

InGaAs also has a high electron mobility ($\geq 10{,}000 cm^2/Vs$) and, thus, InGaAs PIN diodes can offer reduced series resistance resulting in low-loss and high-isolation switches. Moreover, the low (*0.78eV*) bandgap of InGaAs is useful for achieving low turn-on voltage, which reduces DC power consumption and offers a better match with the low-power InP-based electronics. X-band InGaAs PIN switches fabricated using the InP-based HBT process confirmed these expectations and demonstrated superior compared with GaAs-based PIN switches performance at only half the power consumption [31]. The insertion loss for InGaAs PIN switch was *0.89dB* while the isolation exceeded *35dB* compared with *0.82dB* and *25dB* of GaAs circuit, as shown with an arrow in Figure 1.2.

Up until the 1990s, all reported monolithic PIN diode switches were designed using microstrip technology [4,15-22,31]. Coplanar-waveguide technology offered smaller parasitics and lower-cost processing, but it lacked good circuit elements and models. A first report on coplanar PIN switches using beam-lead diodes was published as early as 1989 [32], but not until 1995 had the coplanar GaAs PIN diode switch been realized [33]. The first results on InGaAs/InP-based PINs at millimeter-wave frequencies

were obtained in the course of this work [34], and excellent switching characteristics up to *40GHz* were demonstrated using a coplanar InGaAs PIN SPST switch, described in detail in Chapter 3. This, and further applications of InGaAs PIN diodes to the design and realization of monolithic integrated PIN switches for millimeter-wave operation are marked by underlined captions in Figure 1.2 and are presented in Chapter 4.

A W-band SPST microstrip InGaAs PIN diode switch was developed and demonstrated state-of-the-art performance of *1.3dB* insertion loss and *25dB* isolation at *83GHz* [35]. A high-isolation version of this microstrip SPST switch employing two InGaAs PIN diodes demonstrated a record isolation of *>35dB* at *94GHz* [36]. Based on recent advances in electromagnetic simulators, coplanar circuit models became available for circuit design, and W-band coplanar InGaAs PIN diode SPDT transceiver switches were demonstrated in 1998 with isolation of more than *43dB* at *77GHz* and *94GHz*. [37]. A combination of the low ON-state resistance and a low-inductance of coplanar InGaAs PIN diodes, developed in this work, resulted, in this case, in the highest isolation reported for any W-band PIN switches (see Figure 1.2).

Overall, millimeter-wave InP-based InGaAs PIN diode switches appear to have superior characteristics to that of conventional GaAs-based designs while offering compatibility with high-frequency InP-based HEMT and HBT electronics as desired for emerging W-band radars and imaging systems. This type of switches is extensively investigated in Chapters 3 through 5 of this thesis, which present work on their MMIC implementation at various frequencies as well as studies of their DC, high-frequency, power, and switching properties.

1.5. GaN-Based NDR Diodes for Microwave Signal Generators

Microwave signal generators are essential elements of a millimeter-wave front-end transceiver module as was shown in Section 1.2. Active microwave diodes based on negative differential resistance (NDR) effect are primary devices for high power and low-noise signal generation at millimeter-wave frequencies. Thus, GaAs- and InP-based Gunn diodes based on transferred-electron effect have been successfully employed for microwave and millimeter-wave signal generation up and even beyond W-band

frequencies [13, 38]. However, power and frequency capabilities of Gunn diodes made with conventional III-V compound semiconductors are limited, especially at millimeter-wave frequencies.

On the other hand, studies of the fundamental properties of wide bandgap III-V nitrides indicate that velocity-field characteristics in these materials also exhibit negative differential resistance (NDR). Although further confirmation is needed regarding the presence of NDR in GaN, NDR oscillators made with this wide bandgap semiconductor appear to offer several advantages over conventional III-V compounds. These include increased electrical strength and a higher threshold field, which leads to increased output power in GaN-based devices. Table 1.2 summarizes some of these properties in an attempt to show the superior features of GaN-based electronics. A record output power density for any microwave FET of *7W/mm* was recently obtained with GaN-based devices [7] in support of the discussed advantages of wide bandgap GaN-based materials.

Table 1.2. Semiconductor material parameters and microwave signal generator figure of merit for GaAs, InP, and GaN [38, 39]

Material	F_{TH}, [KV/cm]	F_B [MV/cm]	v_{SAT}, [cm/sec]	v_{PEAK}, [cm/sec]	$Pf^2Z=F_B^2v_{PEAK}^2/4$ [39] [normalized to GaAs]
GaAs	3.5	0.4	0.6×10^7	1.5×10^7	1
InP	10.5	0.5	1.2×10^7	3×10^7	36
GaN	~80-150	2	2×10^7	2.9×10^7	2000-7000

A first analysis of the use of GaN for NDR diode realization is reported in this thesis. Presented in Chapter 6 results discuss the microwave potential of GaN-based signal generators in terms of the expected frequency and power characteristics of GaN NDR oscillators as a function of bias, doping, frequency, and termination impedance of the resonant cavity.

1.6. Objective and Scope of the Thesis

The main objective of this thesis is to advance the development of InP- and GaN-based devices and MMICs for microwave and millimeter-wave applications. For this purpose, switching InP-based InGaAs PIN diodes were developed. Their high-frequency characteristics were studied and device and epitaxial layer design were optimized for

millimeter-wave control applications. A low-parasitics high-impedance microstrip and coplanar InP-based MMIC technology was developed in order to enhance performance of InP-based millimeter-wave PIN diode switches. W-band SPST and SPDT transceiver switches were designed and fabricated, and record performance was demonstrated at *77GHz* and *94GHz*. An automatic on-wafer W-band load-pull system was developed for this purpose and was employed to evaluate the large-signal characteristics of InP-based PIN diodes and W-band MMICs directly at their design frequency. The concept of GaN-based microwave signal generators was proposed and the first analysis of the expected frequency and power capabilities of GaN NDR diode oscillators is presented.

The thesis starts with the description of the fundamental characteristics of switching PIN diodes presented in Chapter 2. The physics of DC and high-frequency characteristics of InGaAs PIN diodes are presented together with the developed numerical simulation approach based on the quasi three-dimensional drift-diffusion method. Chapter 3 starts by optimization of the PIN diode design and epitaxial layers for W-band switching applications, performed on the basis of the developed simulation techniques. The optimization study is followed by description of fabrication technology developed to fabricate monolithic integrated InGaAs PIN diodes. DC and small-signal high-frequency characteristics of the fabricated devices are presented, and small-signal equivalent-circuit parameters of InGaAs PIN diodes are extracted for use in circuit design.

Design, fabrication, and characterization techniques used to realize W-band amplitude- and phase-control MMICs are presented in Chapter 4. Both microstrip and coplanar InP-based MMIC technologies were developed and applied for fabrication of W-band switches and phase-shifters. Record-high isolation of *>40dB* and low insertion loss of *1.1-1.7dB* was demonstrated using InP-based low-parasitics coplanar InGaAs PIN SPDT switches designed for transceiver applications at *77* and *94GHz*. The evaluation of PIN diode switching and power-handling capabilities is presented in Chapter 5. The design of an automated on-wafer W-band load-pull measurement system and its application to characterization of large-signal characteristics of W-band InP-based PIN switches are also included in Chapter 5.

Potential of GaN-based heterojunction field-effect transistors (HFETs) for microwave switching applications is addressed in Chapter 6. A study of the large-signal performance of AlGaN/GaN power HFETs is presented and a notable scalability of these devices as desirable for design of MMICs is demonstrated. AlN/GaN MIS approach is also explored in this chapter and good interface properties and promising electrical characteristics obtained from AlN/GaN MISFETs are presented for the first time.

The first analysis of the use of GaN for NDR diode realization is presented in Chapter 7. The physical basis of operation, frequency-capability, and design of GaN NDR diodes are discussed first, followed by simulated small- and large-signal characteristics of GaN-based NDR diode oscillators. Presented results demonstrate the high potential of GaN-based signal generators for millimeter-wave applications in terms of the expected frequency and power characteristics. Finally, Chapter 8 summarizes the conclusions and presents suggestions for future studies.

CHAPTER 2
FUNDAMENTAL CHARACTERISTICS OF SWITCHING PIN DIODES

A PIN diode is a p-n junction diode with a lightly doped semiconductor layer (I-layer) inserted between the P and N layers. Ion-implantation techniques have been used to form planar PIN diodes [40], but PIN layers formed by epitaxial growth techniques, such as MOCVD or MBE, offer precise thickness and doping control [41]. Consequently, most microwave PIN diode layers today are grown by epitaxial techniques and fabricated on vertical mesas as shown in Figure 2.1. A high-doped thick N layer is grown first with thickness and doping optimized to reduce the lateral access resistance R_N. A non-intentionally- or a low-doped thick I-layer is grown next. These layers lead to presence of resistive and capacitive elements as indicated in Figure 2.1. Typical I-layers have small n-type conductivity caused by crystal defects and impurities. Thicker and lower-doped I-layers are used in high-frequency high-power switching PIN diodes in order to reduce the OFF-state capacitance C_D and, thus, increase the OFF-state impedance as well as raise reverse breakdown voltage. The top P-layer is high-doped and thin in order to reduce the vertical access resistance R_P.

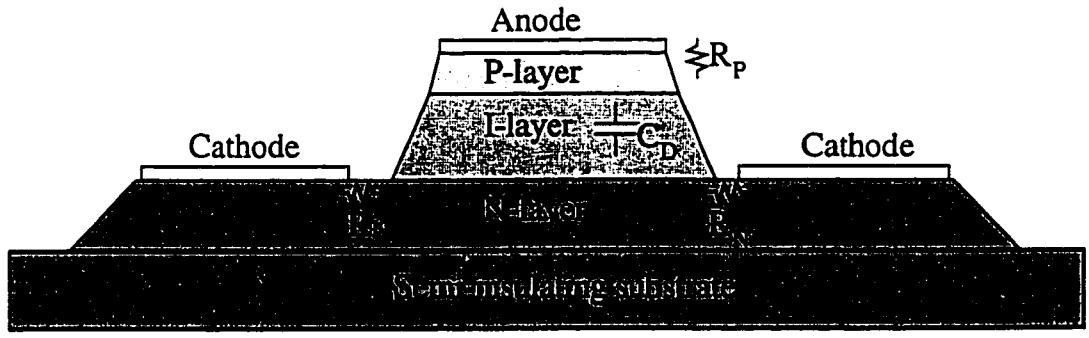


Figure 2.1. Cross-section of an epitaxially-grown switching microwave PIN diode

The following sections describe the DC and high-frequency characteristics of InGaAs PIN diodes and present the simulation approach used for their optimization.

2.1. Design and Operation of InGaAs PIN Diodes

The band diagram of a typical switching InGaAs PIN diode at equilibrium is shown in Figure 2.2a. A *1μm*-thick I-layer in the band diagram is shown to have low n-type doping (N_I=$5\times10^{15}cm^{-3}$) as occurs in non-intentionally-doped (*nid*) InGaAs layers. The PIN diode bandstructure features two junctions, one of which is formed between a *0.2μm*-thick high-doped P-layer (P_P=$1.5\times10^{19}cm^{-3}$) and the I-layer; the other is formed between the I-layer and a *1μm*-thick high-doped N-layer (N_N=$1.5\times10^{19}cm^{-3}$).

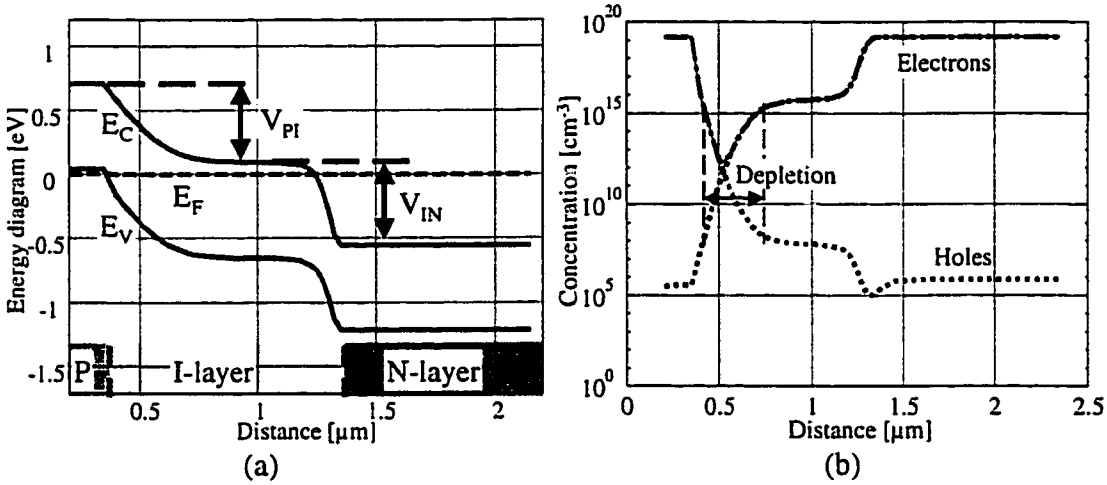


Figure 2.2. InGaAs PIN diode in equilibrium: (a) band diagram (b) carrier-concentration profiles

The potential barriers V_{PI} and V_{IN} formed at the corresponding junctions are shown in Figure 2.2a. The P and N-layers are highly doped and, thus, Boltzman approximation can not accurately describe carrier statistics in these layers. The appropriate expressions for built-in voltages V_{PI} and V_{IN} make use of the following approximation for the Fermi-Dirac distribution $F_{1/2}(\eta) \cong 4\eta^{3/2}/3\sqrt{\pi}$ [42] and are given in (2.1) and (2.2), respectively.

$$V_{PI} = \left(3\pi^2 P_P\right)^{\frac{2}{3}} \frac{\hbar^2}{2qm_h} + E_g - \frac{k_b T}{q} \log\left(\frac{N_C}{N_I}\right) \tag{2.1}$$

$$V_{IN} = \left(3\pi^2 N_N\right)^{\frac{2}{3}} \frac{\hbar^2}{2qm_e} + \frac{k_b T}{q} \log\left(\frac{N_C}{N_I}\right) \tag{2.2}$$

where P_P, N_N, N_I are doping levels in the respective layers, m_h and m_e are hole and electron effective masses, and N_C is the conduction band density of states in the I-layer.

The value of built-in voltage V_{IN} calculated using expression (2.2) differs quite significantly from the value obtained using Boltzman approximation (2.3).

$$V_{IN}^{NON-DEGENERATE} = \frac{k_b T}{q} \log\left(\frac{N_N}{N_I}\right) \tag{2.3}$$

Thus, a built-in potential of only $0.2eV$ is calculated using Boltzman statistics for an InGaAs PIN diode with $N_N=1.5\times10^{19}cm^{-3}$ and $N_I=5\times10^{15}cm^{-3}$. A more accurate value of $V_{IN}=0.64eV$ is calculated using expression (2.2), which accounts for degenerate carrier statistics.

The P and N-layers are highly doped and bandgap narrowing takes place in these layers. The dependence of bandgap of the outer layers on the doping was calculated using the following approximation reported in [42]:

$$E_G^{DEGENERATE} = E_G - 1.6\times10^{-8}\sqrt[3]{N} \tag{2.4}$$

where N is replaced with P_P and N_N doping (in cm^{-3}) for the P and N-layers, respectively. Thus, bandgap of intrinsic InGaAs ($0.75eV$) shrinks down to $0.71eV$ for high-doped material ($N_N=1.5\times10^{19}cm^{-3}$) and the corresponding intrinsic carrier concentration n_i doubles from $6.5\times10^{11}cm^{-3}$ to $1.3\times10^{12}cm^{-3}$.

Due to the built-in voltage between the P and I-layers V_{PI}, the I-layer is partially depleted even under equilibrium conditions as shown in Figure 2.2b. The depletion occurs mostly in the low-doped I-layer and the effective depletion width W_{DEP} can be calculated using expression (2.5)

$$W_{DEP} = \sqrt{\frac{2\varepsilon}{q}(V_{PI} - V)\left(\frac{1}{N_I} + \frac{1}{P_P}\right)} \tag{2.5}$$

where ε is the dielectric constant of InGaAs. A depletion width of $0.45\mu m$ is calculated for the InGaAs PIN diode with $N_I=5\times10^{15}cm^{-3}$ and $P_P=1.5\times10^{19}cm^{-3}$ at zero bias $V=0V$.

2.1.1. Reverse Blocking (OFF-state).

DC I-V characteristics of switching PIN diodes have the same rectifying properties as that of regular p-n diodes. When a negative bias is applied, it adds to the built-in voltage and the potential barriers for current flow are increased as shown in

Figure 2.3a. Here, the depletion width expands over the whole width of the I-layer as shown in Figure 2.3b.

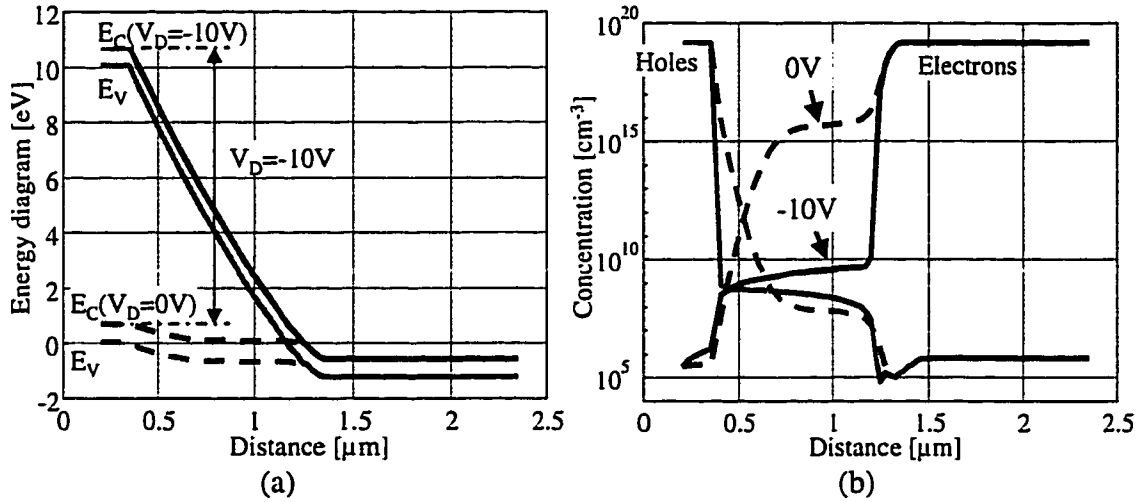


Figure 2.3. InGaAs PIN diode band-diagram and carrier profiles in the OFF-state

The minimum value of negative bias at which the depletion region expands over the whole width of the I-layer is called punch-through voltage (V_{PT}):

$$V_{PT} = \frac{qW_I^2 P_P N_I}{2\varepsilon_S \varepsilon_0 (P_P + N_I)} - V_{PI} \qquad (2.6)$$

where W_I is the width of the I-layer.

The depletion width and, thus, depletion capacitance, remain nearly constant for a negative bias larger than V_{PT}. Punch-through voltage of *2.7V* was calculated using expression (2.6) for the InGaAs PIN diode design described in the previous section.

2.1.2. Forward Conduction (ON-state).

When a positive bias is applied, it compensates the built-in potentials. The ON-state band diagram (*V=0.65V*) is shown in Figure 2.4a. When the electric barriers are lowered, the electrons and holes from the outer P and N-layers diffuse into the I-layer as shown in Figure 2.4b.

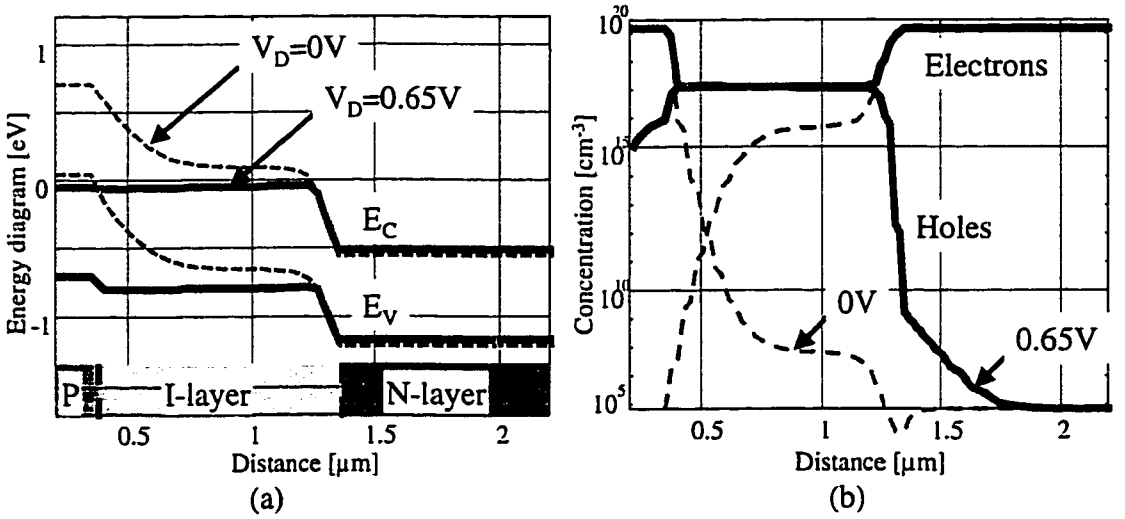


Figure 2.4. InGaAs PIN diode band-diagram and carrier profiles in the ON-state

For a forward bias of *0.65V*, the concentration of injected carriers in the I-layer N_{INJ} is $\sim 3\times 10^{17} cm^{-3}$. The depletion region disappears. The diode is in the low-impedance ON-state and conducts a large ON-state current.

2.2. DC Characteristics of InGaAs PIN Diodes

The above-presented band-diagram-based considerations can be used to evaluate the current-voltage characteristics of the InGaAs PIN diodes under constant bias conditions. The DC I-V characteristics of the InGaAs PIN diodes can further be used for evaluation of the bias-dependence of equivalent circuit elements and applied for large-signal modeling of the diodes. The reverse leakage and reverse voltage breakdown are discussed first, followed by the forward current-voltage characteristics. The subsequent sections are concerned with the recombination and diffusion regions, which exist in all p-n junction diodes, as well as the high-level injection effects, which are specific to PIN diodes.

2.2.1. Reverse Leakage Current

When the diode is in the OFF-state, the current through the diode is blocked and only a small OFF-state current is conducted. The OFF-state current is due to leakage of

carriers generated in the depleted layer and carriers generated in and diffused from the regions immediately adjacent to the depleted layer as described by equation (2.7):

$$J_L = \frac{qn_i W_{DEP}(V)}{\tau_{SC}} + \frac{qD_P n_i^2}{L_P N_N} + \frac{qD_N n_i^2}{L_N P_P} \tag{2.7}$$

where n_i is the intrinsic carrier concentration, W_{DEP} is the width of the depletion region (see equation (2.5)), and τ_{SC} is the space-charge generation lifetime of a deep defect level in InGaAs. The leakage current density of the switching InGaAs PIN diode is largely dominated by space-charge generation in the depleted layer, which is given by the first term in equation (2.7). The τ_{SC} dependence on the recombination level energy E_R and minority-carrier hole and electron lifetime τ_P and τ_N is given by expression (2.8) [43]

$$\tau_{SC} = \tau_P e^{\frac{(E_R - E_i)}{V_T}} + \tau_N e^{\frac{(E_i - E_R)}{V_T}} \tag{2.8}$$

where E_I is the intrinsic Fermi level ($E_I = 0.42eV$ for InGaAs). For a principal deep level $E_R = E_C - 0.321eV$ reported for InGaAs in [44] expression (2.8) simplifies to $\tau_{SC} \approx \tau_P + \tau_N$.

Theoretical and measured leakage current in a InGaAs PIN diode with the layers described in previous section and a diameter of $5\mu m$ are shown in Figure 2.5 by circles and dashed lines, respectively. By fitting the theoretical leakage current to the measured data, a space-charge generation lifetime $\tau_{SC} \approx \tau_P + \tau_N$ of $1.4ns$ was estimated for nid-InGaAs layers.

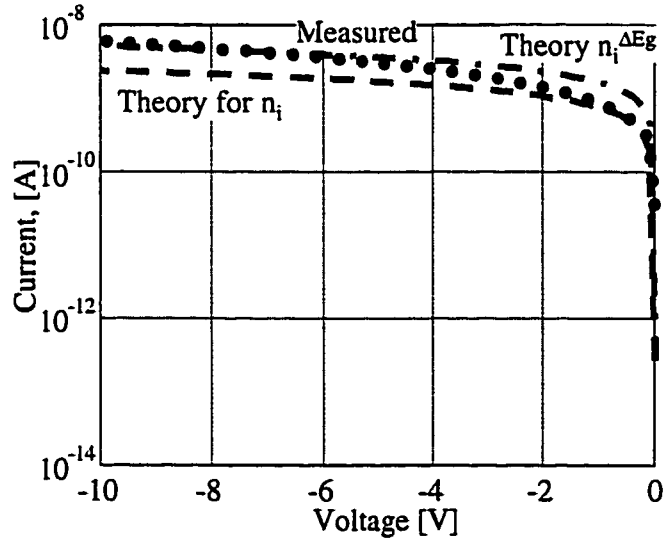


Figure 2.5. Experimental and theoretical leakage current of InGaAs PIN diodes

An increase of the measured leakage current for higher negative bias ($V > -2V$) is attributed to spreading of the depletion region from the low-doped I-layer into the higher-doped outer layers. The high-doped P- and N-layers have narrower bandgap and higher intrinsic concentration than the I-layer (see expression (2.4)), which leads to an increase of leakage current. The increased leakage current calculated by taking into account a higher intrinsic concentration ($n_i^{\Delta Eg}$) is also plotted in Figure 2.5 as a dashed-and-doted line and showed good agreement with experimental data for large negative bias.

2.2.2. Reverse Breakdown

If the reverse bias is increased further, reverse breakdown occurs, the I-layer looses its blocking properties and a large reverse current starts to flow. The reverse breakdown is caused by the presence of a large electric field in the depletion region. The peak field F_{MAX} depends on doping and bias as shown in (2.9):

$$F_{MAX}(V_D) = \sqrt{\frac{2qP_P N_I (V_{PI} - V)}{\varepsilon (P_P + N_I)}} \approx \sqrt{\frac{2qN_I (V_{PI} - V)}{\varepsilon}} \tag{2.9}$$

where P_P and N_I are the doping levels, V is the bias, and ε is dielectric constant of InGaAs. The distribution of the electric field in the depletion region of a PIN diode is given by equations (2.10) when the peak electric field F_{MAX} is smaller than the punch-through field $F_{PT} = qN_I/\varepsilon W_I$, and by equations (2.11) when $F_{MAX} > F_{PT}$.

$$F(x) = \begin{cases} \dfrac{qP_P(x + x_P)}{\varepsilon} & for\ x < 0 \\ \dfrac{qN_I(x_I - x)}{\varepsilon} & for\ 0 < x < W_I \end{cases} \tag{2.10}$$

$$F(x) = \begin{cases} \dfrac{qP_P(x + x_P)}{\varepsilon} & for\ x < 0 \\ \dfrac{qN_I(W_I - x)}{\varepsilon} + \dfrac{qN_N x_N}{\varepsilon} & for\ 0 < x < W_I \\ \dfrac{qN_N(W_I + x_N - x)}{\varepsilon} & for\ x > W_I \end{cases} \tag{2.11}$$

where x_P, x_I, and x_N are depletion widths in the corresponding layers calculated using (2.12):

$$for\ F_{MAX} < F_{PT} \begin{cases} x_P = \dfrac{F_{MAX}\varepsilon}{qP_P} \\ x_I = \dfrac{F_{MAX}\varepsilon}{qN_I} \\ x_N = 0 \end{cases}$$

$$for\ F_{MAX} > F_{PT} \begin{cases} x_P = \dfrac{F_{MAX}\varepsilon}{qP_P} \\ x_I = W_I \\ x_N = \dfrac{(F_{MAX} - F_{PT})\varepsilon}{qN_P} \end{cases} \qquad (2.12)$$

Profiles of electric field corresponding to different reverse biases calculated for the InGaAs PIN diode described in the previous section are shown in Figure 2.6. Due to high doping levels of the P- and N-layers, x_N and x_P are much smaller than x_I and, thus, a high field is present mostly in the low-doped I-layer as shown in Figure 2.6.

When the reverse bias is *–20V*, the peak field F_{MAX} increases to *~170KV/cm*. Carriers accelerated by this high electric field attain large enough energy to generate new electron-hole pairs by impact ionization. When F_{MAX} exceeds the breakdown field F_B, carriers generated by impact ionization initiate an avalanche process of multiplication, which results in a rapid increase of current.

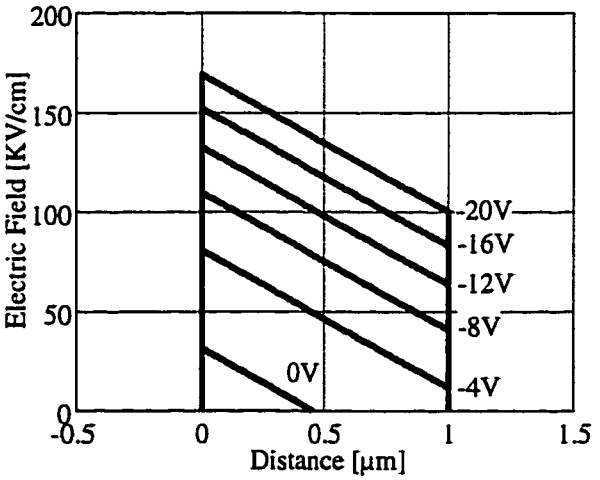


Figure 2.6. Distribution of electric field in the InGaAs PIN diode for reverse bias of *0, -4, -8, -12, -16,* and *-20V* (V_{PT}=*-2.7V*).

The avalanche breakdown current is calculated using ionization coefficients. The ionization coefficients are defined as the number of electron-hole pairs created by an electron or hole in the course of travelling distance x and have the following dependence on the electric field [43]:

$$\alpha_n(V,x) = A_n e^{-\left(\frac{F_{CR}}{F(V,x)}\right)^{\nu_n}}$$
$$\alpha_p(V,x) = A_p e^{-\left(\frac{F_{CR}}{F(V,x)}\right)^{\nu_p}} \tag{2.13}$$

where $F(V, x)$ is the distribution of electric field, and F_{CR}, A_n, ν_n, A_p, and ν_p are the fitting parameters.

Carriers travelling through the high-field depletion region generate a number of new electron-hole pairs determined by equation (2.13). In their turn, newly generated carriers also can generate electron-hole pairs. The multiplication coefficient $M(V,x)$ is defined as

$$M(V,x) = \frac{e^{\int_0^x (\alpha_n(V,z)-\alpha_p(V,z))dz}}{(1-\alpha(V,x))} \tag{2.14}$$

where $\alpha(V,x)$ is called the impact ionization integral and is defined in (2.15).

$$\alpha(V,x) = \int_0^x \alpha_p(V,y) \times e^{\int_0^y (\alpha_n(V,z)-\alpha_p(V,z))dz} dy \tag{2.15}$$

The multiplication coefficient $M(V,x)$ shows how many carriers are created within distance x of the p-n junction biased with reverse bias V. When the bias is increased to the reverse breakdown voltage, the peak field in the depletion region approaches the breakdown field F_B, the impact ionization integral $\alpha(V,x)$ approaches unity, $M(V,x)$ approaches infinity, and avalanche breakdown occurs. The avalanche current density is calculated from the leakage current density $J_L(V)$ using (2.16):

$$J_{AV}(V) = J_L(V) \times \int_{-x_p(V)}^{x_l(V)+x_N(V)} M(V,x)dx \tag{2.16}$$

The equations (2.7)-(2.16) were used to simulate avalanche breakdown for the InGaAs PIN diode described above. The InGaAs fitting parameters for the ionization

coefficients of equations (2.13) were unknown, so the GaAs parameters were used as starting points. The following InGaAs parameters were determined by fitting the simulation results to the experimental data obtained from a *5-μm* diode with the same layer design: $F_{CR}=500KV/cm$, $A_n=3\times10^5cm^{-1}$, $v_n=1.6$, $A_p=2.2\times10^5cm^{-1}$, and $v_p=1.75$.

The calculated impact ionization integral and reverse current are shown in Figure 2.7. The impact ionization integral $\alpha(V,x)$ approached unity when the reverse bias was increased to $V\approx-20V$ in agreement with the experimental data also shown in Figure 2.7. Based on the performed studies, a breakdown field F_B of *180KV/cm* is estimated for low-doped I-InGaAs ($N_I=5\times10^{15}cm^{-3}$). The difference between the calculated and measured reverse I-V characteristics is due to spreading of the depletion region from the low-doped I-layer into the higher-doped outer P and N layers as discussed in Section 2.2.1

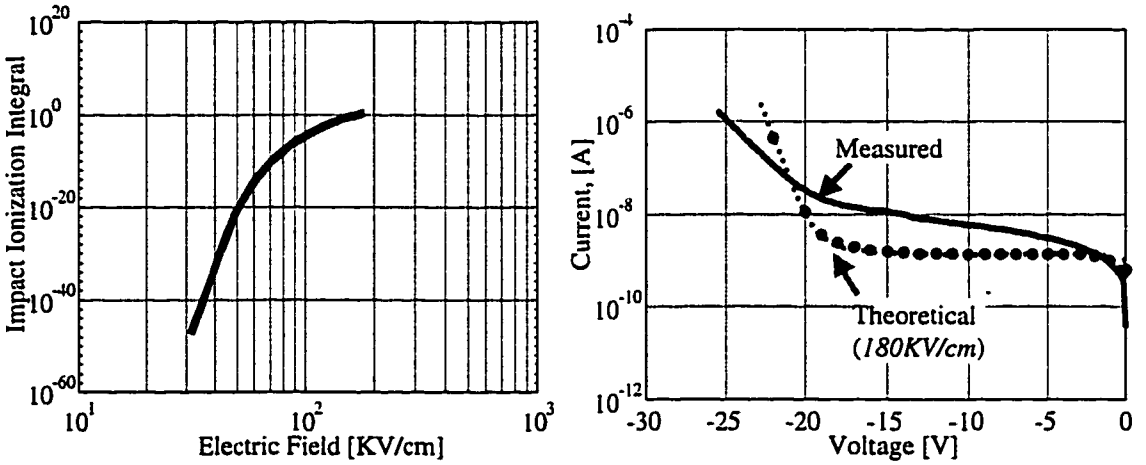


Figure 2.7. Impact ionization integral and I-V characteristics for avalanche breakdown of the InGaAs PIN diode.

2.2.3. Forward I-V Characteristics

When the positive bias is small, carrier injection into the undepleted part of the I-layer is insignificant. The current is due to carrier recombination in the depleted part of the I-layer (depletion region) as described by equation (2.17).

$$J_R(V)=\frac{qn_iW_{DEP}(V)}{2\tau_{SHR}}\left(e^{\frac{V}{2V_T}}-1\right) \qquad (2.17)$$

where n_i is the intrinsic carrier concentration, W_{DEP} is the depletion width, and τ_{SHR} is the Shockley-Read-Hall recombination lifetime. For the case of low carrier injection in the I-layer of the PIN diode, $\tau_{SHR} \approx \tau_{SC} \approx \tau_P + \tau_N$ according to equation (2.8) and references [43, 44]. Shockley-Read-Hall recombination lifetime dependence on injection level is discussed in details in the next section. The ideality factor of the ON-state I-V characteristics in the recombination region is *2*.

When the bias is increased, the minority carrier injection becomes significant. The current occurs by recombination of injected minority carriers with majority carriers. The recombination takes place within the minority-carrier diffusion region, the extent of which is determined by the diffusion properties of minority carriers. Thus, for minority holes injected into the I-layer, the dependence of the hole concentration P_{INJ} on the distance from the junction x and the forward bias V is given by equation (2.18):

$$P_{INJ}(V,x) = p_I \times e^{\frac{V}{V_T}} \times e^{-\frac{x}{L_P}} \tag{2.18}$$

where $p_I = n_i^2/N_I$ is the concentration of minority holes in the I-layer and $L_P = \sqrt{D_P \tau_P}$ is the hole diffusion length. A similar expression is valid for minority electrons in the P-layer. The total diffusion current density consists of hole- and electron-diffusion current components and given by equation (2.19):

$$J_{DIFF}(V) = \left(\frac{qn_i^2 L_P q}{N_I \tau_P \tanh(W_I/L_P)} + \frac{qn_i^2 L_N}{P_P \tau_N \tanh(W_P/L_N)} \right) \left(e^{\frac{V}{V_T}} - 1 \right) \tag{2.19}$$

where τ_P and τ_N are the minority carrier lifetimes for holes and electrons, respectively . The hyper-tangential terms provide corrections for PIN diodes with short layer widths ($W_P < L_N$ and $W_I < L_P$). In a PIN diode $N_I << P_P$ and, thus, the hole-diffusion current (described by the first term of equation (2.19)) is much larger than the electron-diffusion current. The ideality factor of the I-V characteristics in the diffusion current region is *1*.

2.2.4. High-Level Injection

When the concentration of injected carriers in the I-layer exceeds the background level N_I, the concentration of injected holes and electrons must become approximately

equal in order to preserve charge neutrality in the I-layer. Under these conditions, a current increase is accompanied by an increased injection of carriers, which requires only a very small change of the forward bias. This effect is called conductivity modulation and is responsible for low ON-state resistance of PIN diodes [43]. The high-injection voltage drop across the I-layer V_m is independent of the current density and depends only on a ratio of W_I and the high-level injection ambipolar diffusion length L_A according to expression (2.20) [43]:

$$V_m = \begin{cases} 3V_T\left(\frac{W_I}{L_A}\right)^2 \text{ for } W_I < L_A \\ \frac{3\pi V_T}{8} e^{\frac{W_I}{L_A}} \text{ for } W_I > L_A \end{cases} \tag{2.20}$$

where $L_A = \sqrt{(2D_N D_P)/(D_N + D_P)\tau_{HL}}$ and τ_{HL} is the high-level injection lifetime. τ_{HL} is comprised of Shockley-Read-Hall (τ_{SHR}), Auger (τ_{AUG}), and radiative band-to-band (τ_R) carrier lifetimes as shown in expression (2.21):

$$\frac{1}{\tau_{HL}} = \frac{1}{\tau_{SHR}} + \frac{1}{\tau_{AUG}(n_{INJ}^2)} + \frac{1}{\tau_R(n_{INJ})} \tag{2.21}$$

The carrier-lifetime dependence on the carrier concentration in I-InGaAs is shown in Figure 2.8. Under high-injection conditions ($N_{INJ} > 1\times10^{16}cm^{-3}$), the Shockley-Read-Hall lifetime τ_{SRH} can be approximated by $\tau_P+\tau_N$. The Auger lifetime $\tau_{AUG} = 1/(C_{AUG}N_{INJ}^2)$ does not become significant until injected carrier density N_{INJ} exceeds $1\times10^{19}cm^{-3}$ (calculated using $C_{AUG}=5\times10^{-30}cm^6/sec$ reported for InGaAs in reference [42]). Radiative transitions with lifetime $\tau_R \approx 1/(2B_R N_{INJ})+\tau_0$ (where B_R is known as the Einstein coefficient for radiative transitions) provide the main recombination mechanism in InGaAs for carrier concentration N_{INJ} between 1×10^{17}cm^{-3} and $1\times10^{19}cm^{-3}$. For case of high-level injection, τ_R approaches τ_0.

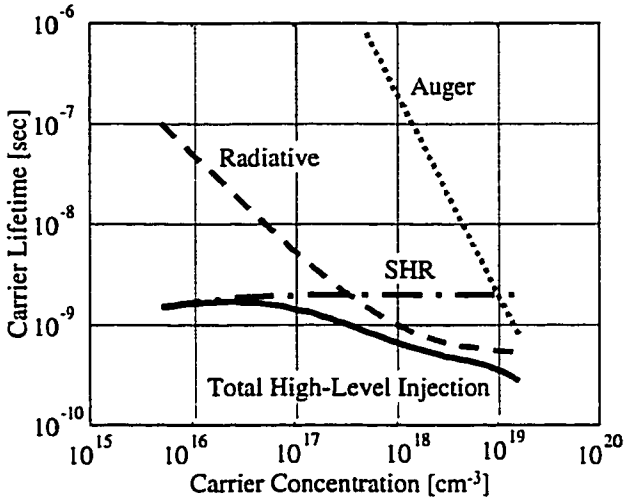


Figure 2.8. Dependence of carrier lifetimes on carrier concentration in I-InGaAs

The high-level injection current density is determined by the rate of high-level recombination in the I-layer and, thus, can be calculated using expression (2.22):

$$J_{HL}(V) = \frac{qW_I N_{INJ}(V)}{\tau_{HL}(V)} = \frac{qW_I n_I}{\tau_{HL}} e^{\frac{(V-V_m)}{2V_T}} \tag{2.22}$$

where $N_{INJ}(V)$ is the concentration of injected carriers in the I-layer, and $(V\text{-}V_m)$ is the voltage drop across the PI and IN junctions. The ideality factor of the I-V characteristics in the high-injection region is 2.

Under low-injection conditions, the forward current density consists of the sum of space-charge recombination and diffusion components J_R+J_{DIFF}. As more carriers are injected into the I-layer, the space-charge current is eliminated and the growth of diffusion current becomes limited by high-injection effects. The following mathematical expression was used to calculate the total forward current density J_{TOT}:

$$\frac{1}{J_{TOT}} = \frac{1}{J_R + J_{DIFF}} + \frac{1}{J_{HL}} \tag{2.23}$$

For large values of the forward current, the voltage drop across the parasitic contact resistance R_S becomes significant and limits its exponential growth. The external bias V_{EXT} is related to the internal bias V by equation (2.24):

$$V_{EXT} = V + \rho_C J_{TOT} \tag{2.24}$$

where $\rho_C = R_S \times \pi D^2/4 \approx 1\times10^{-7}\Omega cm^2$ is the specific contact resistivity and D is the diameter of the diode.

The I-V characteristics of a 10μm-diameter InGaAs PIN diode were calculated using equations (2.17)-(2.24) and by replacing unknown InGaAs radiative lifetime constants with GaAs parameters $\tau_0 \approx 0.5ns$ and $B_R \approx 10\times10^{-10}cm^3/sec$ [42]. The results are shown in Figure 2.9. Space-charge recombination, diffusion, and high-injection regions of the I-V characteristics are indicated, and current saturation due to the parasitic resistance is visible in the high current region.

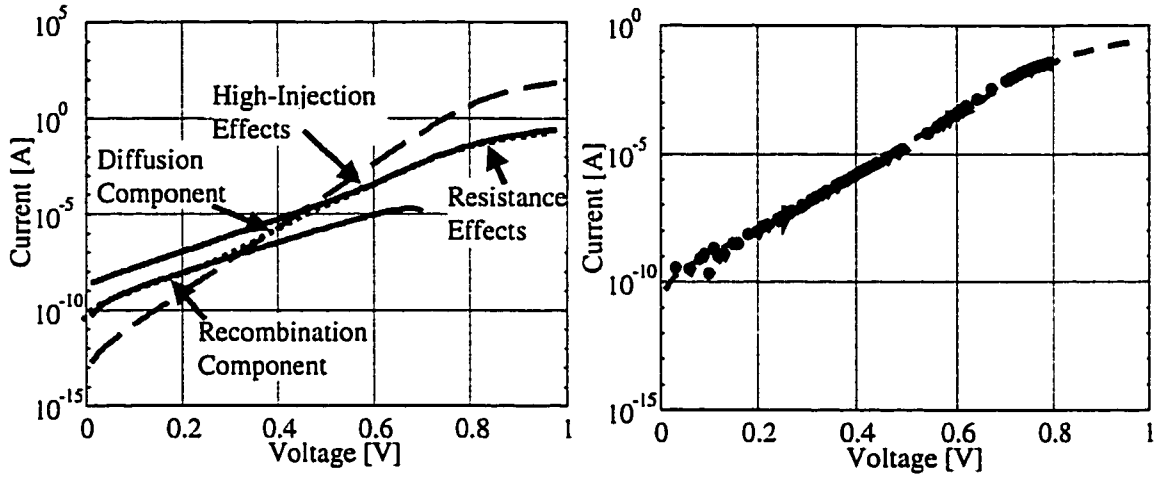


Figure 2.9. I-V characteristics of InGaAs PIN diodes: a) different components of the ON-state current, b) comparing of theoretical and measured results

Theoretical I-V characteristics of an InGaAs PIN diode were also compared with measured I-V characteristics of an InGaAs PIN with the same design. A good agreement between the theory and experiment was obtained by adjusting InGaAs radiative lifetime constants ($\tau_0=0.3ns$, $B_R=80\times10^{-10}cm^3/sec$). The results are also shown in Figure 2.9. The radiative lifetime constants of InGaAs found by fitting theoretical and experimental characteristics are in general agreement with material properties expected for high-quality epitaxially grown I-InGaAs layers.

2.3. High-Frequency Characteristics of InGaAs PIN Diodes

The previous section concentrated on the characteristics of switching PIN diodes under constant control bias. However, the behavior of switching PIN diodes with respect to an AC signal is equally important for their application in microwave control circuits.

2.3.1. Modeling of High-Frequency Characteristics

The difference between DC and AC characteristics is caused by a finite response time of carriers to varying electric field. Thus, current flow may occur by particle flow and by charge displacement. The displacement current becomes more important as the frequency increases. The frequency at which the conductance and displacement components of the total current are equal is called dielectric relaxation frequency f_{DR}. Dielectric relaxation frequency is found by setting susceptance $B = \omega \times A \times \varepsilon / W$ equal to conductance $G = q \times N \times \mu \times A / W$ and is given by equation (2.25):

$$f_{DR} = \frac{q \times N \times \mu}{2 \times \pi \times \varepsilon} \tag{2.25}$$

where N is doping, μ is the mobility of the majority carriers, and ε is the dielectric constant. The doping dependence of f_{DR} calculated for n-InGaAs is shown in Figure 2.10.

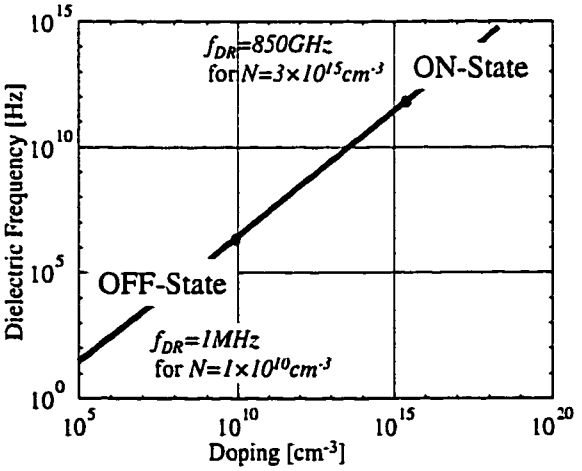


Figure 2.10. Dielectric relaxation frequency in InGaAs and frequency dependence of conductance mechanism in I-InGaAs (N_I=$5\times10^{15}cm^{-3}$)

During the OFF-state operation of the InGaAs PIN diode, the I-layer is depleted of carriers and their concentration levels are less than $10^{10}cm^{-3}$ (see Figure 2.3). Under such

conditions, the main conductance mechanism for AC signal with frequency $>1MHz$ (see Figure 2.10) is by charge displacement and is characterized by the depletion layer capacitance. This low-f_{DR} feature of the OFF-state switching PIN diodes sets them apart from FETs, which characteristics show significant displacement current through the OFF-state capacitance under high frequency operation. Additional components, such as inductors need to be incorporated in FET switches to resonate out the capacitance and improve isolation.

The typical background doping level of I-InGaAs is $3\text{-}5\times10^{15}cm^{-3}$. For this minimum value of the I-layer doping the dielectric relaxation frequency has a very high value of $\sim 800GHz$. Thus, for all practical applications, $f << f_{DR}$, susceptance can be neglected, and the majority-carriers admittance of the undepleted I-layer is due to conductance only (as in the ON-state PIN diode). Thus, the ON-state PIN diodes also offer improved ON-state characteristics compared with the ON-state FETs, which characteristics show ON-state displacement currents due to distributed effects in these three-terminal devices [45, 46].

During the ON-state operation of the PIN diode, non-equilibrium minority carriers are present in the I-layer and stored in the cathode and anode layers (see Figure 2.4). The frequency response of the minority carriers is determined primarily by their lifetime which leads to frequency-dependent impedance characteristics of the ON-state PIN diodes [47].

The steady-state equations of InGaAs PIN diodes developed in the previous sections can be used to evaluate linear small-signal AC characteristics of the ON-state diode. The voltage and current are assumed to have small-signal AC components: $V(t) = V_{ON} + ve^{j\omega t}$ and $I(t) = I_{ON} + ie^{j\omega t}$. The ON-state diffusion equation for AC components is of the same form as for DC components (2.19), but has frequency-dependent carrier lifetimes $\tau_N^* = \tau_N / \sqrt{1 + j\omega\tau_N}$ and $\tau_N^* = \tau_N / \sqrt{1 + j\omega\tau_N}$ [48]. The ON-state admittance $Y_{ON}(\omega)$ is found by from the AC components of current and voltage:

$$Y_{ON} = \frac{i}{v} = \frac{\left(I_N\sqrt{(1 + j\omega\tau_N)} + I_P\sqrt{(1 + j\omega\tau_P)}\right)}{V_T} = \frac{I_{ON}\sqrt{(1 + j\omega\tau_{HL})}}{V_T} \qquad (2.26)$$

Minority carrier lifetime in the ON-State InGaAs PIN diode was evaluated in the previous section and is *~0.3ns*. Thus, at microwave frequencies (*>1GHz*), $\omega\tau_{HL} >> 1$ and expression (2.26) simplifies to

$$Y_{ON} = G + jB = \frac{I_{ON}\sqrt{\omega\tau_{HL}/2}}{V_T} + j\frac{I_{ON}\sqrt{\omega\tau_{HL}/2}}{V_T} \qquad (2.27)$$

The frequency-dependent susceptance term of (2.27) gives rise to well known "charge storage" effects and is characterized by diffusion capacitance.

The transit time of the minority carriers through the I-layer should be also considered. The transit time through the ON-state I-layer is analogous to that of the base transit time in a bipolar transistor and is given by the following equation:

$$\tau_T = \frac{W_I^2}{D} \qquad (2.28)$$

where W_I is the width of the I-layer and D is the diffusion coefficient. The ON-state current is comprised of electron and hole components and, thus, the frequency response of both carriers should be considered. Electron and hole transit-time frequencies $f_T = 1/\tau_T$ for InGaAs PIN diodes with variable I-layer width are shown in Figure 2.11.

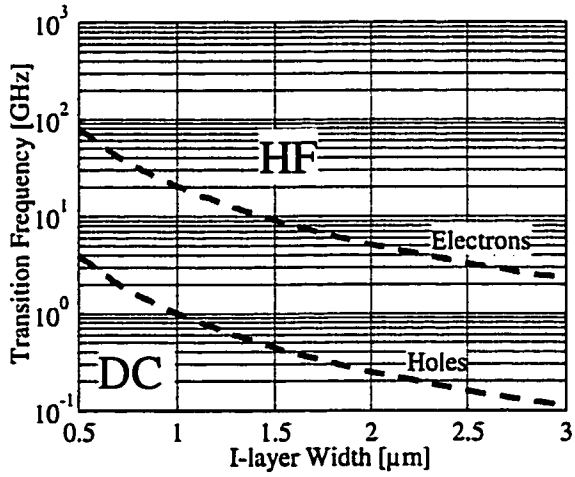


Figure 2.11. Electron and hole transit-time frequencies of InGaAs PIN diodes

If the signal varies with frequency much smaller than the transit-time frequency, the carriers always remain in the steady-state conditions and DC I-V characteristics can be used to describe the ON-state impedance of the diode. As the frequency of operation is increased, the transit-time delays become significant and cause inductive behavior of the

ON-state impedance [47], also known as negative capacitance of "reclaimable charge" [49]. Thus, the results of Figure 2.11 show that for *1μm*-thick InGaAs PIN diodes the ON-state inductive behavior is possible for frequencies below *1GHz*. It should be noted that electron response is faster (*~20GHz* or *~50ps* for *1-μm* InGaAs PIN diode) and, thus, fast turn-on and turn-off transients are still possible due to electron currents.

The ON-state impedance at frequencies exceeding f_T can be found under assumption that carriers' densities remain unaffected by high-frequency excitation (charge-control approximation), which leads to small-signal equivalent circuit presented in the next section.

2.3.2. Small-Signal Equivalent Circuit of Switching PIN Diode

A small-signal equivalent circuit modeling a InGaAs PIN diode is shown in Figure 2.12. The intrinsic part of the equivalent circuit is composed of bias-dependent elements associated with the I-layer and bias-independent resistances R_P and R_N of the P- and N-layers, respectively. The depleted part of the I-layer is modeled by a parallel circuit of depleted layer resistance R_D and depletion capacitance C_D. The undepleted part of the I-layer is represented by resistance R_U. Diffusion capacitance C_{DIF} is used to model non-equilibrium minority-carriers present in the ON-state diode.

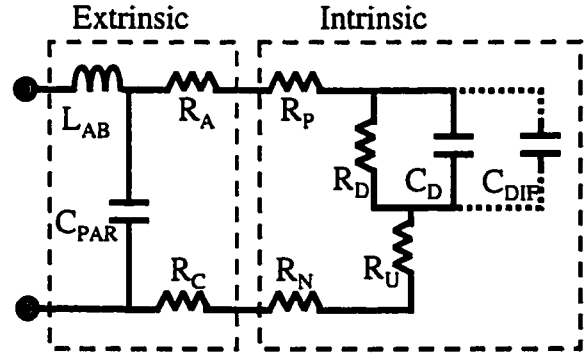


Figure 2.12. Complete small-signal equivalent circuit of the PIN diode

The extrinsic part includes bias-independent parasitic elements as follows: anode contact resistance R_A, cathode resistance R_C, airbridge inductance L_{AB}, and pad capacitance C_{PAR}. Skin-effect resistance is negligible compared with the other parasitic

resistance components due to relatively small conductivity of the I-layer and miniature size of the switching diodes.

Switching microwave PIN diodes are designed to operate in two discrete states: the ON-state and the OFF-state. When the diode is turned on, the carriers from the P and N layers fill the I-layer. The depletion layer resistance decreases and the depletion layer capacitance increases, both effects leading to dissolution of the R_DC_D network. Moreover, non-equilibrium minority carriers provide additional charge-storage conductance, which is described by diffusion capacitance $C_{DIF} = I_{ON} / V_T \sqrt{\tau_{HL}/2\omega}$. Diffusion capacitance and charge-storage conductance were evaluated for an InGaAs PIN diode in the ON-state ($I_{ON}=10mA$) as a function of frequency and the results are shown in Figure 2.13.

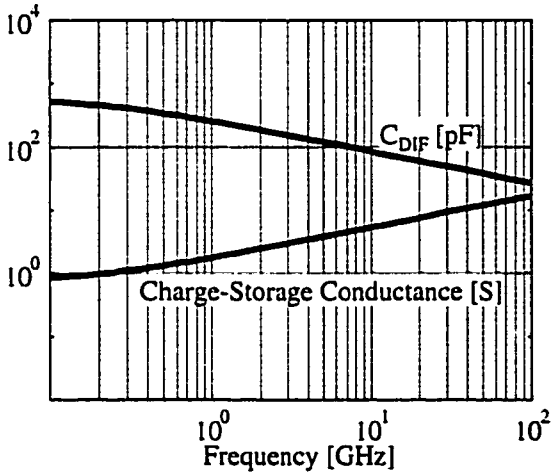


Figure 2.13. Frequency dependence of the diffusion capacitance and charge-storage conductance evaluated for the ON-state InGaAs PIN diode

While diffusion capacitance decreases with frequency as $1/\sqrt{\omega}$ (due to reduced response of minority carriers at higher frequency), its value at $100GHz$ is still very high ($15pF$) and the charge-storage conductance actually increases with frequency as shown in Figure 2.13. Overall, the R_DC_D network representing the depleted part of the I-layer is eliminated from the high-frequency ON-state equivalent circuit of the PIN diode.

Increased concentration of carriers in the I-layers causes further reduction of the undepleted I-layer resistance R_U, which occupies all of the I-layer. Overall, the ON-state high-frequency characteristics of a PIN diode are that of a small ON-state resistance $R_{ON}=R_U^{ON}+R_P+R_N+R_A+R_C$. A practical ON-state InGaAs PIN diode equivalent circuit is

shown in Figure 2.14. Millimeter-wave switching PIN diodes have an ON-state resistance of *1-3Ω*, a parasitic capacitance of *5-10fF*, and a parasitic inductance L_{AB} of *5-50pH*, depending on the diode size and design of the interconnect lines.

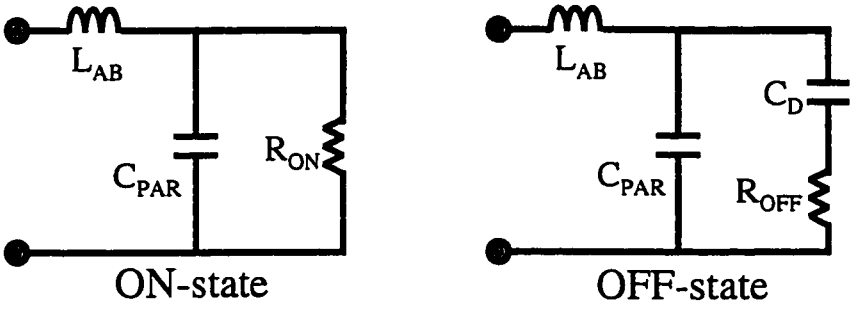


Figure 2.14. ON-state and OFF-state equivalent circuits of the InGaAs PIN diode

The practical OFF-state equivalent circuit is shown in Figure 2.14. In this case, the bias is negative and the I-layer is depleted of carriers, which widens the depletion layer and decreases the depletion capacitance C_D. The OFF-state PIN diode high-frequency characteristics are primarily determined by the OFF-state capacitance C_{OFF} $=C_D+C_{PAR}$. R_{OFF} consists of the access resistance of the PIN diode R_S (where $R_S=R_P+R_N+R_A+R_C$) and the resistance of the undepleted part of the I-layer R_U^{OFF}. Depending on the size of the diode, the depletion capacitance of switching PIN diodes varies between *10fF* and *50fF*, while typical R_{OFF} values are of the order of several ohms.

2.3.3. Bias-Dependence of PIN Diode Equivalent Circuit Elements

The equations developed to describe steady-state characteristics of the InGaAs PIN diode ((2.17)-(2.24) for ON-state and (2.9)-(2.12) for OFF-state) can be used to evaluate the bias-dependence of the PIN diode equivalent-circuit elements R_U^{ON}, R_U^{OFF}, and C_D^{OFF}. The microwave resistance of the I-layer of the ON-state InGaAs PIN diode R_U^{ON} is calculated from its low-field conductivity $\sigma = q\mu_A N_{INJ}$:

$$R_U^{ON} = \frac{W_I / A}{2q\mu_A N_{INJ}} \tag{2.29}$$

By taking advantage of the relationship between the concentration of injected carriers and the ON-state current (see expression (2.22)), R_U^{ON} becomes:

$$R_U^{ON} = \frac{W_I^2}{2\mu_A I_{ON} \tau_{HL}} \tag{2.30}$$

The total ON-state resistance of the InGaAs PIN diode R_{ON} also includes resistances R_P and R_N of the P- and N-layers, respectively; and R_A and R_C of anode and cathode contacts, respectively:

$$R_{ON} = \frac{W_I^2}{2\mu_A \tau_{HL} I} + \frac{W_P}{q\mu_P P_P} + \frac{W_N}{q\mu_N N_N} + \rho_C \frac{A_A + A_C}{A_A A_C} \tag{2.31}$$

The OFF-state capacitance of the PIN diode C_D^{OFF} is calculated as a parallel-plate capacitance of the depleted I-layer (W_{DEP}), and the OFF-state resistance R_U^{OFF} of the undepleted I-layer (W_I-W_{DEP}) is calculated from its conductivity.

$$C_{OFF} = \frac{\varepsilon A}{W_{DEP}} \tag{2.32}$$

$$R_{OFF} = \frac{(W_I - W_{DEP})}{q\mu_I N_I} + \frac{W_P}{q\mu_P P_P} + \frac{W_N}{q\mu_N N_N} + \rho_C \frac{A_A + A_C}{A_A A_C} \tag{2.33}$$

Intrinsic equivalent-circuit elements for a $5\mu m$-diameter InGaAs PIN diode with $1\mu m$-thick I-layer doped at $5\times10^{15} cm^{-3}$ were calculated using equations (2.30)-(2.33) and the results are shown in Figure 2.15.

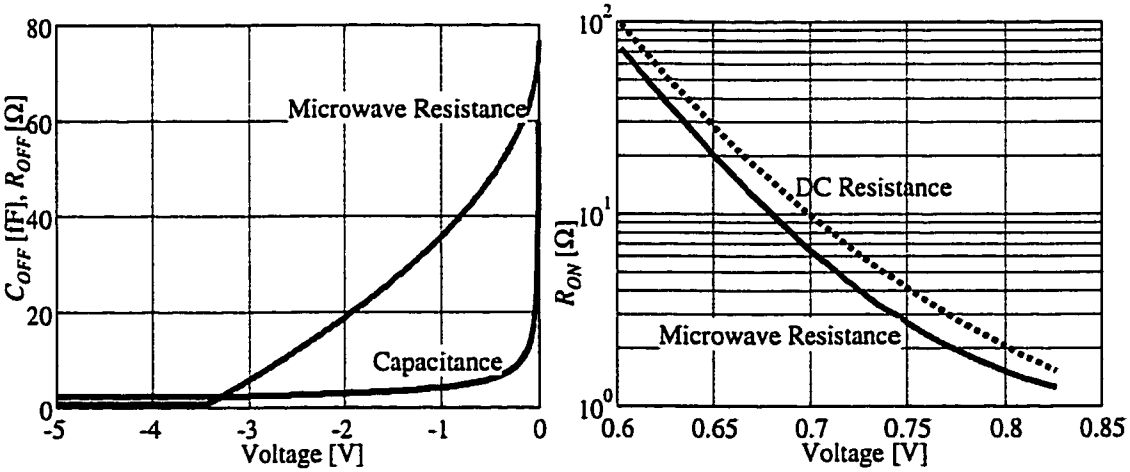


Figure 2.15. High-frequency characteristics of the InGaAs PIN diode as a function of control bias: a) OFF-state and b) ON-state

The diode had an ON-state resistance of $R_{ON}=1.3\Omega$ (including a 0.8Ω parasitic resistance), an OFF-state resistance R_{OFF} of $\sim0.9\Omega$, and an OFF-state capacitance C_{OFF} of

2.5fF (not including the parasitic pad capacitance). An incremental DC resistance calculated from I-V characteristics is also shown in Figure 2.15 to demonstrate its difference from the microwave resistance as discussed in Section 2.3.1

The values of the intrinsic equivalent-circuit elements R_{ON}, R_{OFF}, and C_{OFF} are very small. In a practical switching PIN diode, these elements can be influenced or even dominated by the extrinsic parasitic elements such as the contact resistance and the parasitic pad capacitance of an airbridge. Analytical expressions the PIN equivalent-circuit elements require many approximations and may lead to erroneous predictions, especially for the ON-state impedance. Numerical simulations of semiconductor devices based on drift-diffusion equations allow studies of their DC and high-frequency characteristics with improved accuracy and additional physical insight [49]. Such physical-based simulator for InGaAs PIN diodes developed in order to account for parasitic effects and improve modeling of the high-frequency InGaAs PIN characteristics is presented in the next section.

2.4. Numerical Simulations of InGaAs PIN Diodes

Drift-diffusion simulations were employed to allow a deeper insight into the operation of a practical device as well as improved modeling of the device operation and parasitic effects. This numerical simulation approach was later used to obtain a more accurate prediction of the high-frequency characteristics (see Sections 2.4.3 and 2.4.4) and to optimize InGaAs PIN diodes for switching applications (see Section 3.1).

2.4.1. Simulations Approach and Modeling of InGaAs PIN diodes

The InGaAs PIN diodes were simulated using a hydrodynamic approach available in a commercial simulator (Medici). A two-dimensional cross-section of the InGaAs PIN developed for use in the simulations is presented in Figure 2.16. The cross-section was defined in a manner consistent with structures obtained by etching as used in fabrication of microwave PIN diodes. Implementation of a practical cross-section allowed accurate simulation of such effects as parasitic pad capacitance and spreading resistance.

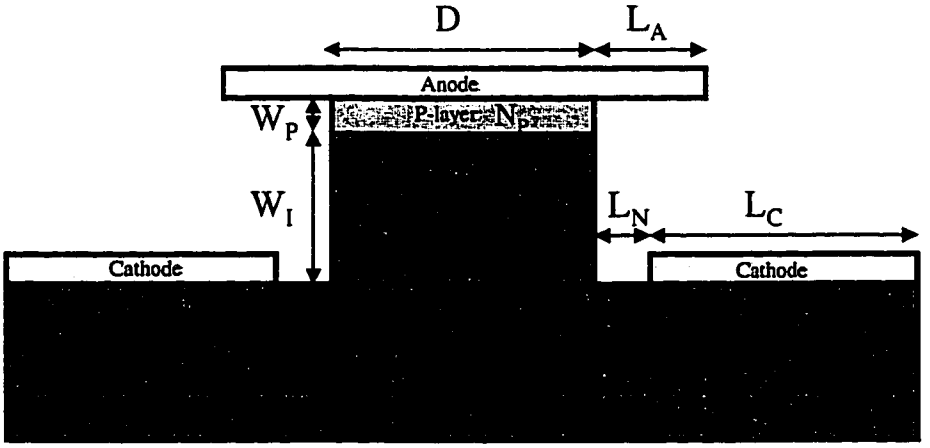


Figure 2.16. Two-dimensional cross-section of InGaAs PIN diode

The PIN diode consisted of the following layers: P- (W_P=0.15μm, P_P=1.5×10^{19}cm^{-3}), I- (W_I=1μm, N_I=5×10^{15}cm^{-3}), and N-layer (W_N=1μm, N_N=1.5×10^{19}cm^{-3}). The PIN mesa had a diameter D=10μm with anode contact on the top. The anode mesa was composed of the P- and I-layers and rested on the top of the N-layer. The cathode contact placed on the top of the N-layer had a width L_C=10μm and was offset by L_N=2μm from the anode mesa. The anode contact overhang L_A was added to account for the parasitic capacitance of the leads.

Since InGaAs material parameters were not available in the simulator database, in-house physics-based material models for InGaAs were developed through literature review and fitting simulations to the experimental results. The following physical effects were accounted for: Fermi-Dirac carrier statistics, bandgap narrowing, doping-, temperature-, and field-dependent mobility characteristics; impact ionization, and concentration-dependent carrier recombination by Shockley-Read-Hall, direct band-to-band, and Auger mechanisms.

The coefficients for the corresponding physical effects were obtained from previously published data [42] and by fitting to the experimental characteristics as described in the previous section. In the case of bandgap narrowing, parameters were not available and the default values for GaAs were assumed [42].

For simulation purposes, the PIN diode cross-section was divided into a fine two-dimensional mesh of spatial nodes. A special feature of the device simulator was employed to extend the two-dimensional cross-section mesh into a quasi-three-

dimensional mesh using a system of cylindrical coordinates, which accounted for variable volume of inner and outer nodes [50].

2.4.2. DC and High-Frequency Characteristics of InGaAs PIN diodes

The two-dimensional boundaries of the depletion regions in the InGaAs PIN diode simulated under equilibrium conditions are shown in Figure 2.17a). The DC I-V characteristics of the InGaAs PIN diode were obtained by calculating the diode current I_D corresponding to steady-state solutions under various bias conditions. The simulated DC I-V characteristics were compared with the experimental data recorded from a InGaAs PIN diode of the same design. Good agreement was achieved for both ON-state conduction and OFF-state blocking as illustrated in Figure 2.17b).

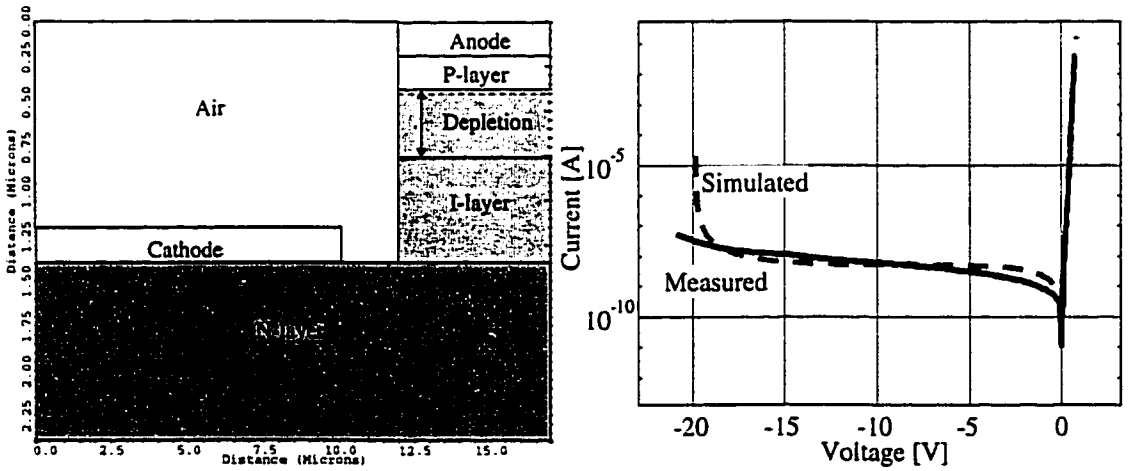


Figure 2.17. Results of two-dimensional numerical simulations of InGaAs PIN diodes: a) boundaries of depletion region at equilibrium, b) I-V characteristics

Two-dimensional numerical simulations were also used to study the high-frequency characteristics of the InGaAs PIN diodes. For this purpose, previously obtained solutions of DC simulations were subjected to a small-signal AC analysis. During the AC analysis a sinusoidal input of given frequency was applied to the device and the corresponding harmonic currents and voltages at all terminals were calculated [50]. The latter were used to evaluate high-frequency *S*- and *Y*-parameters.

The *S*-parameters provide standard means for high-frequency characterization of microwave devices. The S_{11}-parameter of the PIN diode measures the reflection of the

high-frequency signal from the PIN when it terminates a standard *50Ω*-transmission line. The information provided by the complex value of the S_{11}-parameter is sufficient for successful application of InGaAs PIN diodes in microwave control circuits. The S_{11}-parameters of the nominal design of the InGaAs PIN diode were simulated for different bias conditions and frequency between *1GHz* and *100GHz*. The results for Zero-state (*V=0V*), ON-state (*V=0.83V*), and OFF-state (*V=-10V*) are shown in Figure 2.18.

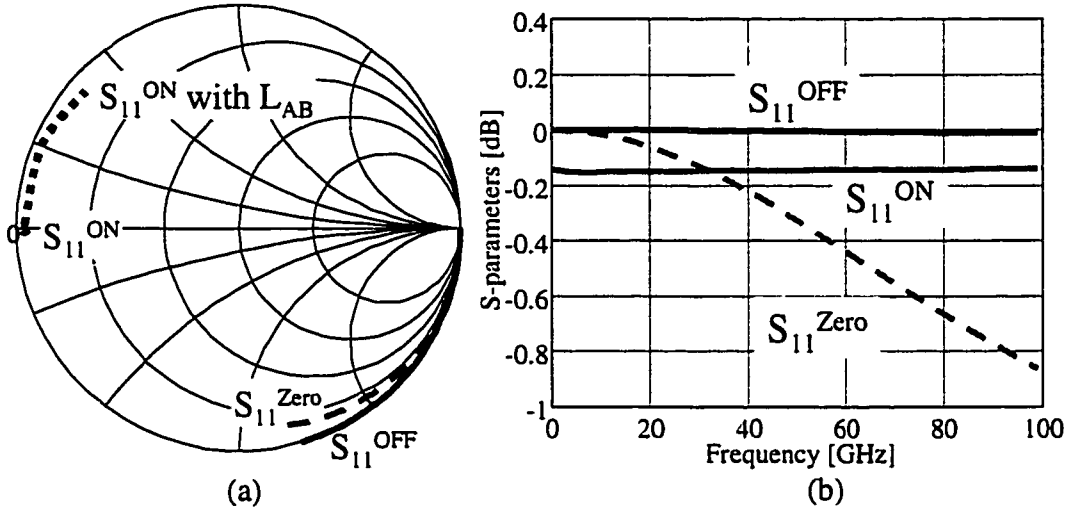


Figure 2.18. Simulated S_{11}-parameter of the InGaAs PIN diode

The complex nature of *S*-parameters is best represented by plotting them on the Smith chart (see Figure 2.18a). Reflection coefficients from an ideal ON-state (S_{11}^{SHRT}=*-1*) and an ideal OFF-state (S_{11}^{OPEN}=*1*) diode would be located on the very left and the very right of the Smith chart, respectively. Imperfect characteristics of a switching PIN diode are reflected by deviations of $S_{11}^{ON/OFF}$ from the ideal positions.

The position of the OFF-state reflection coefficient S_{11}^{OFF} of the InGaAs PIN diode is nearly ideal at low frequency, but the capacitive nature of the OFF-state PIN leads to increase of the phase of S_{11}^{OFF} when the frequency increases as shown in Figure 2.18a. The Zero-state reflection coefficient S_{11}^{Zero} demonstrates an even larger imperfection at high-frequency operation when the amplitude of the reflected signal decreases from *0dB* to *-1dB* (see Figure 2.18b) due to leakage through the Zero-state capacitance C_{Zero}. The imperfection of the ON-state reflection coefficient S_{11}^{ON} is due to a finite value of the ON-state resistance R_{ON}, which causes a reflection loss of *~0.2dB* for

all frequencies. The phase deviation also occurs in the ON-state PIN diodes if parasitic inductance L_{AB} is taken into account as illustrated by Figure 2.18a.

2.4.3. Frequency Dependence of InGaAs PIN Diode Impedance

The numerical simulations were used to investigate the ON-state impedance of the InGaAs PIN diodes and evaluate the frequency range of the developed equivalent circuit model (see Figure 2.14). This allowed verification of the validity of assumption that the junction network $R_D C_D$ can be removed from the ON-state equivalent circuit. For this purpose, the admittance of the ON-state InGaAs was extracted at different frequencies from *0.1GHz* for *1THz*. The results of the study are illustrated in Figure 2.19.

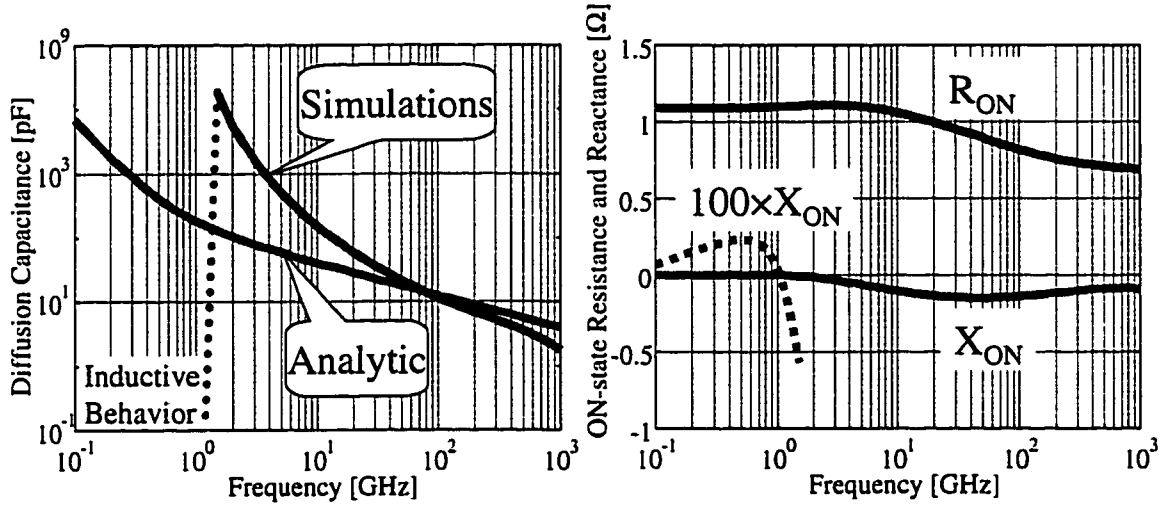


Figure 2.19. Frequency dependence of diffusion capacitance and the ON-state impedance of an InGaAs PIN diode

The diffusion capacitance was calculated using the simple analytical expression (2.27) and showed good agreement with the simulated value for frequencies above *20GHz*. However, for frequencies between *1GHz* and *20GHz*, the analytical theory underestimated the value of diffusion capacitance, and at lower frequency, it was erroneous since it did not predict inductive current-lagging effects.

The real part of the ON-state impedance (R_{ON}) was much larger than the reactive part (X_{ON}) for all frequencies. An accurate equivalent-circuit model of switching PIN diode for millimeter-wave frequencies may also include an ON-state capacitance C_{ON}, but

special care needs to be taken to account for the frequency-dependent nature and bandwidth limitations of such equivalent circuit.

The dispersion of the OFF-state equivalent-circuit elements was also investigated and the results are shown in Figure 2.20. The OFF-state capacitance did not vary over the entire frequency range, while the OFF-state resistance R_{OFF} increased slightly at very low frequencies, but remained constant for all practical frequencies between *1* and *200GHz*.

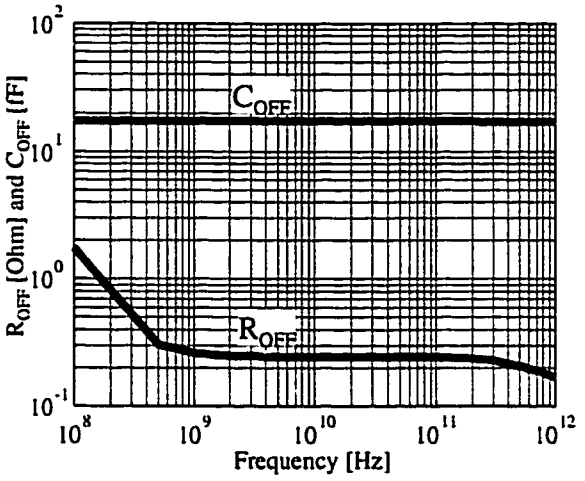


Figure 2.20. Frequency dependence of the OFF-state InGaAs PIN equivalent-circuit elements

Overall, for the frequency range of interest, between *1GHz* and *100GHz*, little or no variations were observed in the values of the InGaAs PIN equivalent-circuit elements. Therefore, the developed high-frequency equivalent circuits can be used to model InGaAs PIN diodes. The equivalent-circuit parameters R_{ON}, R_{OFF}, and C_{OFF} were further employed for study and optimization of the InGaAs PIN diodes switching characteristics.

2.4.4. Bias-Dependent Equivalent-Circuit Elements of InGaAs PIN diodes

The equivalent circuit elements R_{ON}, R_{OFF}, and C_{OFF} as a function of bias were extracted from the simulated *Y*-parameters at *10GHz* and the results are shown in Figure 2.21 for an InGaAs PIN diode design of Sections 2.4.1 and 2.4.2. At first, the ON-state resistance R_{ON} rapidly decreases as the I-layer is filled with carriers, but R_{ON} becomes saturated when the diode is fully turned on. The OFF-state capacitance C_{OFF} decreases when the negative bias is increased to $V_{PT} \approx -3V$ because the depletion region width

spreads through the entire I-layer. At higher negative bias, the OFF-state capacitance C_{OFF} stays constant because the I-layer is already completely depleted. A minimum R_{ON} of *0.9Ω* (including the parasitic contact resistance of *~0.5Ω*) and a minimum C_{OFF} of *17.6fF* (including the parasitic pad capacitance) were found for this InGaAs PIN at the ON- (*V=0.83V*) and OFF-states (*V=-10V*) biases, respectively.

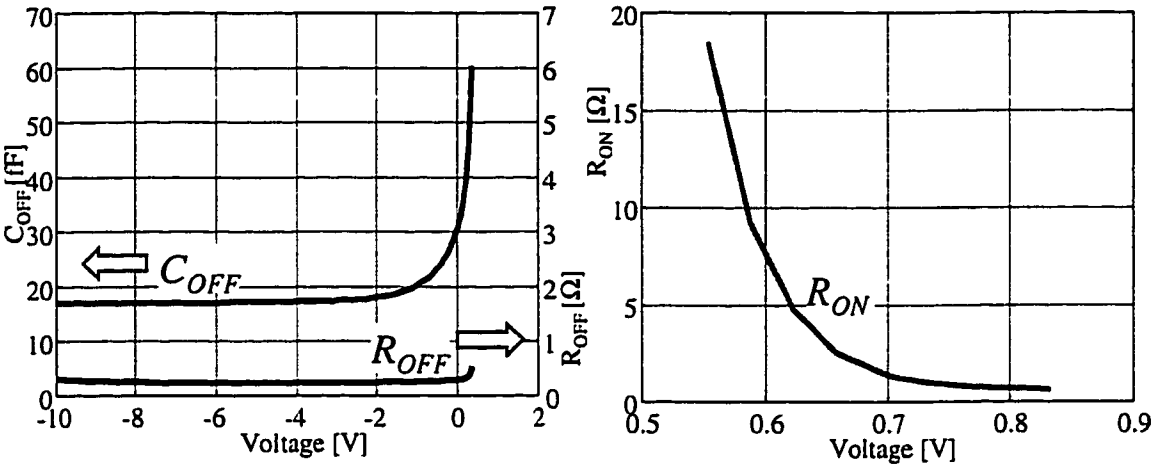


Figure 2.21. Bias d ependence of InGaAs PIN diode equivalent-circuit elements.

A parasitic capacitance C_{PAR} of *7fF* was extracted for an airbridge overhang L_A of *10μm*. The value of C_{PAR} was extracted from the dependence of the total OFF-state capacitance C_{OFF} on L_A as illustrated in Table 2.1. Thus, the depletion capacitance C_D of *10μm*-diameter InGaAs PIN diode was *10.6fF*.

Table 2.1. Extraction of the value of parasitic capacitance C_{PAR}

L_A [μm]	0	3	5	7	9	10	11
C_{OFF} [fF]	**10.6**	12.7	13.8	15.1	16.7	**17.6**	18.4
C_{PAR} [fF]	**0**	2.1	3.2	4.5	6.1	**7.0**	7.8

Switching PIN diodes are optimized to have minimum ON-state impedance and maximum OFF-state impedance at the frequency of operation. Because PIN diodes are resistive in the ON-state and capacitive in the OFF-state, it suggests that ON-state resistance R_{ON} and OFF-state capacitance C_{OFF} should be minimized. The developed numerical high-frequency simulation approach was further used for optimization of

InGaAs PIN diode design for W-band switching applications as described in the following chapter.

2.5. Conclusions

Analytical equations were used to calculate DC current-voltage characteristics of InGaAs PIN diodes and to model the depletion region width, reverse breakdown, and high-level injection effects. These effects are important for high-frequency modeling of PIN diodes because the breakdown voltage V_{BR} determines RF-power handling of switching PIN diodes, while the depletion region width W_{DEP} and high-level carrier lifetime τ_{HL} affect their small-signal high-frequency characteristics.

A breakdown field of *180KV/cm*, a low-level SHR lifetime of *1.4ns*, and a high-level radiative lifetime of *0.3ns* were evaluated for I-InGaAs by comparing theoretical and experimental I-V characteristics of InGaAs PIN diodes.

A small-signal equivalent circuit for practical InGaAs PIN diodes was introduced and theoretical bias-dependent expressions for intrinsic equivalent circuit elements were developed. It was found that due to the small values of the intrinsic elements, an accurate equivalent circuit of a practical InGaAs PIN diode has to include the extrinsic parasitic elements.

A physical-based numerical simulator for InGaAs PIN diodes was developed in order to improve the insight into the operation of a practical switching diode. Quasi-3D InGaAs PIN diode cross-sections were developed to obtain a more accurate modeling of the parasitic effects and, thus, perform accurate simulations of the high-frequency characteristics. These numerical simulations allowed a more precise evaluation of the OFF-state capacitance (including the parasitic capacitance), the ON-state diffusion capacitance (including current-lagging inductive effects), and the ON-state resistance for a practical InGaAs PIN diode. The developed simulations approach was next used for optimization of InGaAs PIN diodes for switching applications as described in Chapter 3.

CHAPTER 3
InGaAs PIN DIODES FOR MILLIMETER-WAVE MONOLITHIC INTEGRATED CONTROL CIRCUITS

Traditionally, most monolithic microwave switches employed GaAs-based PIN diodes [51, 52]. However, the first results obtained using X-band InGaAs PIN diode switches showed increased isolation and reduced power consumption compared with the conventional GaAs circuits [53]. Moreover, InP-based InGaAs PIN diodes are compatible with high-speed InP-based electronics, which offer excellent performance at W-band and up to D-band frequencies as desired for current and next-generation automotive radars. However, suitability of InGaAs PIN diodes for frequencies above X-band was not explored and low-parasitic MMIC technology desired for high-performance millimeter-wave InP-based PIN diode switches was lacking. This chapter addresses development of InGaAs PIN diodes for W-band switching applications and presents studies of their switching characteristics.

Optimization studies of switching InGaAs PIN diodes for millimeter-wave applications using a numerical-simulation approach are presented in Section 3.1. The epitaxial layer design and the lateral dimensions were optimized to obtain higher switching cutoff frequencies and improved switching characteristics at W-band. The MMIC technology developed for realization of the millimeter-wave InGaAs PIN diodes is presented in detail in Section 3.2. Low and high frequency characteristics of the fabricated InGaAs PIN diodes are described in Sections 3.3 and 3.4. The results of high-frequency S-parameter characterization were used to extract the InGaAs PIN diode equivalent circuits for use in the circuit design.

3.1. Optimization of InGaAs PIN Diodes for Millimeter-Wave Applications

PIN diode switches can be designed with series or shunt PIN diodes as the switching elements. When the frequency of operation is increased, the performance of the series PIN switch is greatly affected by the leakage of signal through the OFF-state capacitance, which directly reduces the isolation of the switch. On the other hand, this OFF-state leakage has lesser effect on the shunt PIN switch because this small leaked signal is deducted from the large transmitted signal. Consequently, most millimeter-wave PIN switches are designed to use PIN diodes connected in shunt.

A commonly-used figure of merit for microwave PIN diodes is the switching cutoff frequency f_{CS}, which measures the minimum insertion loss of shunt PIN switches due to the intrinsic characteristics of the PIN diodes [54]. However, the f_{CS} approximation is only valid for frequencies smaller than *1/10* of its value, does not account for presence of parasitic elements nor provides any measure of the maximum isolation. In order to optimize the design of a practical switching InGaAs PIN diode for W-band switching applications, the insertion loss and isolation of a shunt PIN switch were calculated from the high-frequency equivalent circuit of the PIN diode, which included parasitic elements L_{AB} and C_{PAR} typical for MMIC technology. Then the results of two-dimensional numerical simulations were used to establish dependencies between the InGaAs PIN diode design and the switch performance and, thus, to find the optimal InGaAs PIN design for millimeter-wave switching applications.

3.1.1. Characteristics of Shunt PIN Diode Switches

The schematic of the considered shunt PIN diode SPST switch is shown in Figure 3.1. The switch connects the input and the output port by a transmission line shunted in the middle by a PIN diode with impedance Z_D. The characteristic impedance of the transmission line and the impedance of the input and output ports have the same value Z_0. The switching action is based on the difference between the ON- and the OFF-state impedance of the PIN diode. The shunt SPST switch transmits when the diode is in the high-impedance OFF-state and reflects when the diode is in the low-impedance ON-state.

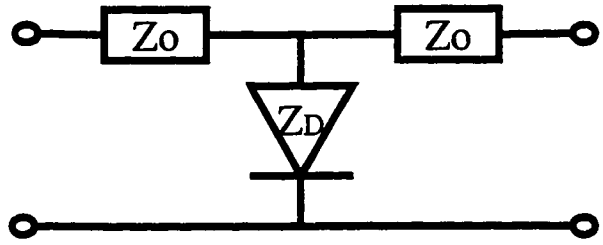


Figure 3.1. Schematic of a shunt PIN diode SPST switch

When the diode is turned on, its ON-state impedance Z_{ON} is made up of the ON-state diode resistance R_{ON} and the parasitic capacitance C_{PAR} connected in series with the parasitic inductance L_{AB}. The ON-state capacitance C_{ON} is frequency dependent. It has larger value at lower frequencies and is reduced at higher frequencies (*~100pF* at *10GHz* and *~30pF* at *100GHz*) as was discussed in Chapter 2. Overall, C_{ON} adds only a small reactive component to the impedance of the diode. The equivalent circuit of the ON-state PIN diode is shown in Figure 3.2a.

If $|Z_{ON}|$ is much smaller than Z_O, the diode represents a "short" and the signal is shunted to the ground and reflected to the input port. A signal flow through the diode results in power dissipation in the ON-state resistance R_{ON}. A voltage drop across the ON-state impedance Z_{ON} generates a small secondary signal propagated to the output. The ratio of power delivered to the output in the absence of the diode to output power transmitted with the diode in the ON-state is defined as isolation of the shunt switch. Small values of R_{ON} and large value of C_{ON} help to improve switch isolation and reduce power losses.

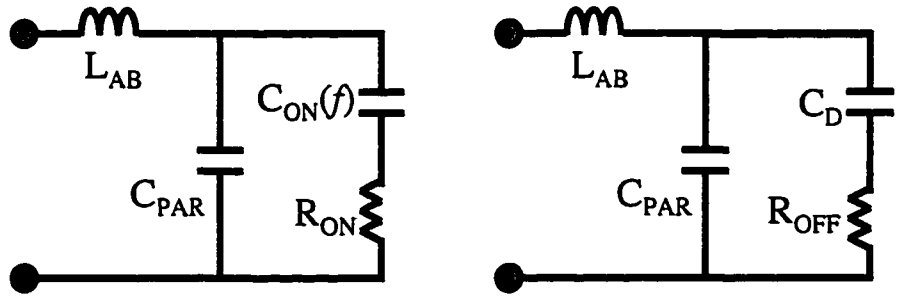


Figure 3.2. Millimeter-wave equivalent-circuit of switching InGaAs PIN diode in the ON- and in the OFF-state

The OFF-state PIN diode equivalent circuit is shown in Figure 3.2b. Z_{OFF} is determined primarily by its total OFF-state capacitance C_{OFF}, which consists of the

intrinsic capacitance C_D and the parasitic capacitance C_{PAR}. If $1/\omega C_{COFF}$ is much larger than Z_O, the diode represents an "open" circuit and the signal passes by to the output port. However, as the frequency of operation increases, Z_{OFF} decreases and, at millimeter-wave frequencies, only diodes with very small C_{OFF} can be used. For example, a diode with a C_{OFF} of $33fF$ will have Z_{OFF} of 50Ω at $94GHz$. Small-size diodes with low C_{OFF} and high Z_{OFF} are necessary to prevent millimeter-wave signal from leaking across the OFF-state capacitance. This leakage causes loss in shunt PIN switches. Insertion loss of a shunt PIN switch is defined as the ratio of power delivered to the load in the absence of the PIN diode to power delivered to the load with the diode in the OFF-state. Both insertion loss and isolation are normally expressed in dB.

If the impedance of the PIN diode in the OFF (Z_{OFF}) and in the ON (Z_{ON}) states is known, insertion loss and isolation of a shunt SPST PIN diode switch can be calculated using simple voltage-divider formulas [54]. It is assumed that radiation and transmission line losses are small and the losses are caused only by the PIN diode. Then the insertion loss (L) and isolation (I) of the switch are given by (3.1) and (3.2), respectively.

$$L = 20 \times log\left(\left|1 + \left(\frac{Z_0}{2 \times Z_{OFF}}\right)\right|\right) \tag{3.1}$$

$$I = 20 \times log\left(\left|1 + \left(\frac{Z_0}{2 \times Z_{ON}}\right)\right|\right) \tag{3.2}$$

The intrinsic figure of merit of the PIN diodes — switching cutoff frequency f_{CS} was also calculated following [54] using expression (3.3):

$$f_{CS} = \frac{1}{2\pi C_{OFF}\sqrt{R_{ON}R_{OFF}}} \tag{3.3}$$

For the purpose of this study, the characteristic impedance of the transmission line Z_O was set to 50Ω and the frequency f to $94GHz$. A typical for the MMIC technology parasitic inductance L_{AB} of $5pH$ was also included in the analysis. The intrinsic elements of the InGaAs PIN diode R_{ON}, R_{OFF}, and C_D, as well as the parasitic capacitance C_{PAR} were obtained by numerical simulations.

3.1.2. Numerical Simulations of InGaAs PIN Diodes

The simulation approach was described in detail in Chapter 2. High-frequency characteristics of InGaAs PIN diodes were evaluated based on steady-state solutions of coupled Poisson and current-continuity equations within a quasi-three-dimensional diode model. A two-dimensional cross-section of an InGaAs PIN diode used in the simulations is shown in Figure 3.3. It was defined in a manner consistent with the technology used for fabricating switching InGaAs PIN diodes. The nominal InGaAs PIN diode design had the following parameters: $W_P=0.15\mu m$, $W_I=1\mu m$, and $W_N=1\mu m$ - the thickness of P, I, N-layers, respectively; $N_P=1.5\times10^{19}cm^{-3}$, $N_I=5\times10^{15}cm^{-3}$, $N_N=1.5\times10^{19}cm^{-3}$ - the doping of P, I, N layers, respectively; $D=10\mu m$ - the diode diameter; $L_N=2\mu m$ - the separation between the I-layer and the cathode; $L_C=10\mu m$ - the width of the cathode; and $L_A=10\mu m$ - the overhang of the airbridge.

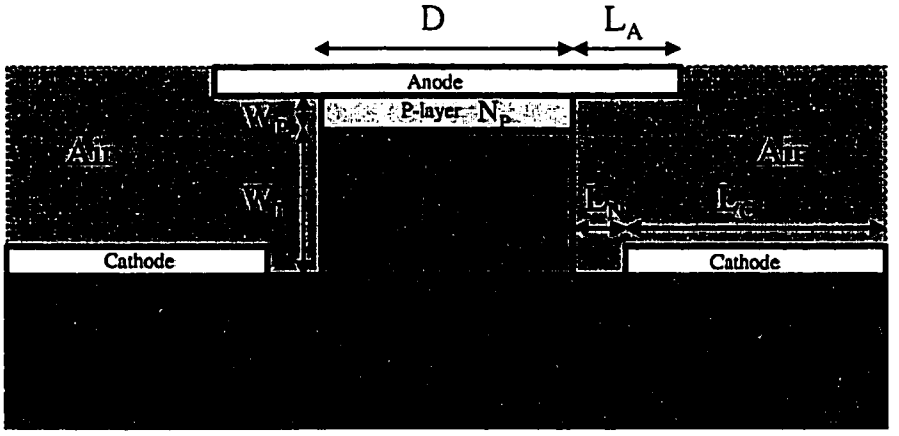


Figure 3.3. Cross-section of InGaAs PIN used for device optimization.

First, intrinsic equivalent circuit elements R_{ON}, C_{ON}, R_{OFF}, and C_D were extracted from simulation results as a function of bias for the nominal InGaAs PIN diode design and the results are shown in Figure 3.4. An R_{ON} of 0.82Ω, an R_{OFF} of 0.32Ω, and a C_D of $10.2fF$ were found for biases $V_{OFF}=-5V$ and $V_{ON}=0.7V$, respectively. The W-band ($94GHz$) value of the ON-state diffusion capacitance C_{ON} was $13pF$ and, therefore the junction elements were shunted out and eliminated from the equivalent circuit in good agreement with theoretical expectations of Chapter 2. A parasitic pad capacitance $C_{PAR}=7fF$ due to coupling between anode and cathode contacts was also extracted.

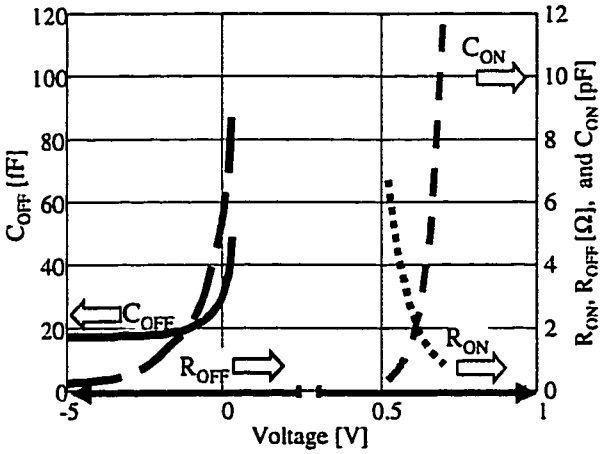


Figure 3.4. Simulated bias dependence of R_{ON}, C_{ON}, R_{OFF}, and C_{OFF}

Secondly, bias-dependent ON- and OFF-state impedance of the PIN diode were set up for the PIN diode equivalent circuits specified in Figure 3.2 as shown in the following expression:

$$Z_{OFF/ON} = j\omega L_{AB} + \cfrac{1}{j\omega C_{PAR} + \cfrac{1}{R_{OFF/ON} + \cfrac{1}{j\omega C_{DION}}}} \tag{3.4}$$

Finally, the bias dependence of the insertion loss and isolation of the shunt InGaAs PIN diode SPST switch at *94GHz* was calculated by substituting the expressions for Z_{ON} and Z_{OFF} into equations (3.1) and (3.2). The results are shown in Figure 3.5.

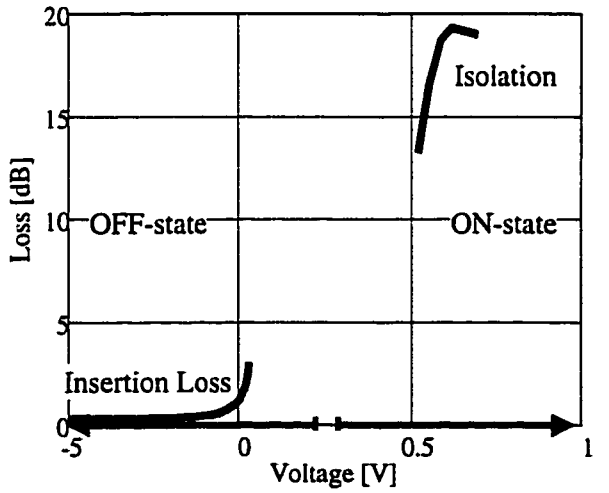


Figure 3.5. Bias dependence of insertion loss and isolation of the InGaAs SPST switch at *94GHz*

The insertion loss reached a minimum value of *0.3dB* for a negative bias larger than *-3V*; therefore, V_{OFF}=*-5V* was selected as the OFF-state bias for design optimization study. The isolation saturated at a maximum value of *19dB* for an ON-state bias larger than *0.6V*, and V_{ON}=*0.7V* which was selected for the ON-state bias. These two bias points were kept constant for all following simulations.

3.1.3. Optimization of InGaAs PIN Diodes for Shunt W-band SPST Switches

The thickness and the doping of the PIN-layers and the diameter of the PIN diode were varied in order to find an optimal design of the switching InGaAs PIN diode for W-band applications. The thickness of the I-layer (W_I) was optimized first.

When W_I was varied from *0.5* to *2.5μm*, the OFF-state capacitance C_{OFF} was reduced from *37* to *10fF*. The value of insertion loss depends primarily on the OFF-state capacitance C_{OFF} and it reduced sharply from *1.3dB* to *0.3dB* when W_I was increased from *0.5μm* to *1μm* as shown in Figure 3.6. At the same time, the isolation remained at *19dB*, corresponding to a small increase of the ON-state resistance R_{ON} from *0.6* to *0.8Ω* and an unchanged high value of C_{ON} of *~13pF*. The further increase of W_I from *1μm* to *2.5μm* led to an additional decrease of isolation by *1.5dB* and an only slight improvement of insertion loss by *0.15dB*.

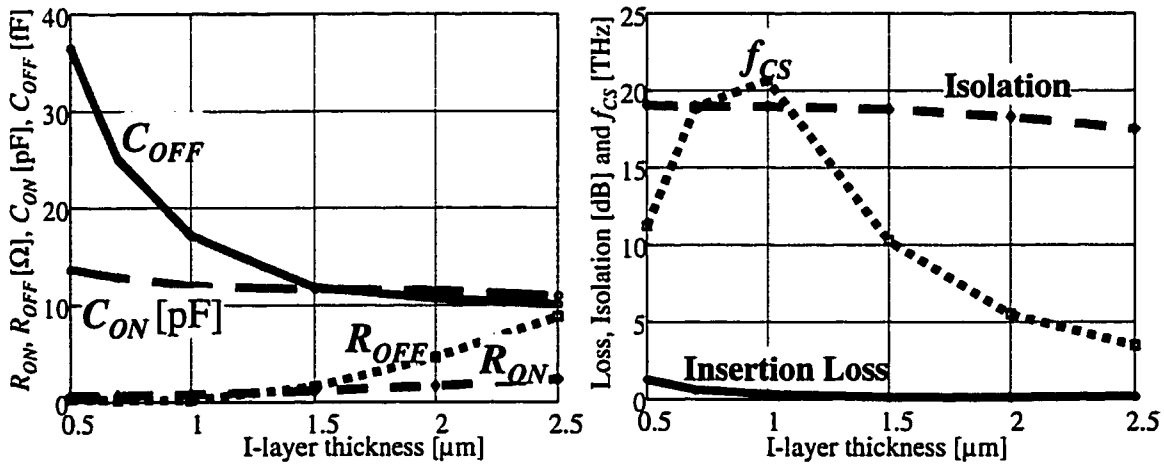


Figure 3.6. Influence of the I-layer thickness on the high-frequency characteristics of InGaAs PIN diode and the performance of a shunt PIN SPST at *94GHz*

Intrinsic figure of merit f_{CS} was also calculated as a function of W_I and the results are also shown in Figure 3.6. f_{CS} calculated for InGaAs PIN diode designs with the I-layer thickness between *0.75* and *1.0μm* exceeded *19THz*, but its value was only *~11THz* for designs with a *0.5μm*- and *1.5μm*-thick I-layers due to degradation of C_{OFF} and R_{OFF} for thinner and thicker layers, respectively. Based on the results of Figure 3.6, an InGaAs PIN diode with a *1μm*-thick I-layer was selected for further studies because it offered a combination of small insertion loss (*~0.3dB*), large isolation (*~18dB*), and high switching cutoff frequency (*~20THz*).

The reduction of the insertion loss for I-layers thicker than *1.5μm* was prevented by the selected value of the I-layer doping (N_I=$5\times10^{15}cm^{-3}$), which limited the maximum depletion width in the I-layer at the OFF-state bias V_{OFF}=*-5V* to *~1.5μm*. The value of N_I chosen for the nominal design of the InGaAs PIN diode was selected to correspond to a minimum value for I-InGaAs grown by MOCVD and MBE (N_I~$5\times10^{15}cm^{-3}$) [55].

The insertion loss and isolation of the InGaAs PIN switch were also calculated for the conditions when W_I was kept constant at *1μm* and N_I was varied between $5\times10^{15}cm^{-3}$ and $3\times10^{16}cm^{-3}$. It was found that isolation remained constant at *19dB*, while insertion loss increased by only *0.3dB* to *0.6dB* for N_I of $3\times10^{16}cm^{-3}$. This low sensitivity of insertion loss and isolation to the variations of the I-layer doping for the InGaAs PIN diode design with a *1μm*-thick I layer helps to reduce the impact of possible variations of N_I during the growth.

The influence of the doping of the N- and P-layers is demonstrated in Figure 3.7. When the N-layer doping (N_N) was decreased from 1.5×10^{19} to $1\times10^{18}cm^{-3}$, an increase in the access resistance of the N-layer caused R_{ON} to double from *0.8* to *2Ω*. Most of the degradation occurred for conditions when N_N was reduced below $5\times10^{18}cm^{-3}$. The switching cutoff frequency fell from *20* to *7THz* (reflecting an increase in R_{ON} and R_{OFF}), but the isolation decreased only by *~1dB* and the insertion loss was not affected.

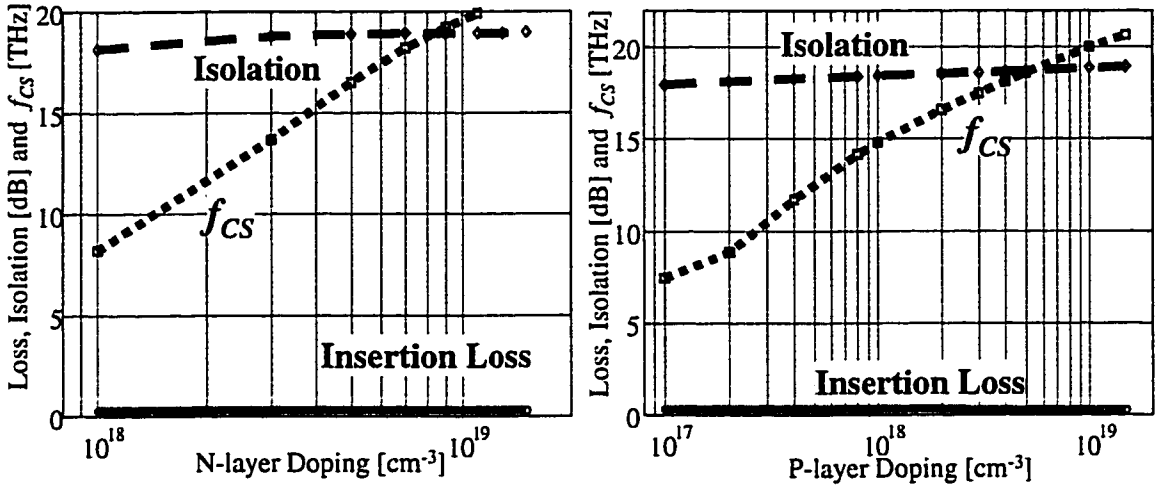


Figure 3.7. Influence of the P- and N-layer doping on the performance of a shunt InGaAs PIN diode SPST switch at *94GHz*

While a similar behavior was observed due to the change of the P-layer doping (P_P), its impact on the isolation and switching cutoff frequency was much less pronounced, due to a smaller access resistance of the P-layer. Thus, a degradation of isolation by *1dB* was observed only when P_P was reduced all the way down to $1\times10^{17}cm^{-3}$ and most of the degradation took place for $P_P<1\times10^{18}cm^{-3}$.

The small degradation of the switch performance (*~1dB*) compared with the large degradation of f_{CS} (*65%*) reflects a situation when the switch performance is limited more by the parasitic elements (L_{AB} and C_{PAR}) than by the intrinsic device characteristics. For example, the maximum value of *19dB* for switch isolation is determined by selection of a parasitic airbridge inductance $L_{AB}=5pH$ (selected on the smaller side of a *0-30pH* range typical for MMIC technology). Such limitation of the InGaAs PIN diode switch performance by parasitic elements is due to the high frequency of operation (*94GHz*) and excellent switching characteristics of the optimized diodes. Therefore, the simulated switch performance was affected only for those designs, which represented significant degradation of intrinsic device characteristics and had f_{CS} of less than *10THz*.

Thus, the simulations showed that the high-frequency performance of InGaAs PIN diodes was not significantly affected by the growth variations of P_P and N_N as long as their values continued to exceed $5\times10^{18}cm^{-3}$. This was important for realization of InGaAs PIN diode layers and allows relaxation of doping requirements during the growth.

Simulations were performed to optimize the thickness' of the P and N layers, W_P and W_N, respectively. The results plotted in Figure 3.8 showed that while the thickness of the P-layer W_P should be minimized, the N layer should be thicker than $1\mu m$ in order to maintain high value of isolation and f_{CS}. The degradation of performance for InGaAs PIN designs with thin N layers is caused by an increase of the spreading access resistance of the N-layer as can be seen from the InGaAs PIN diode cross-section in Figure 3.3.

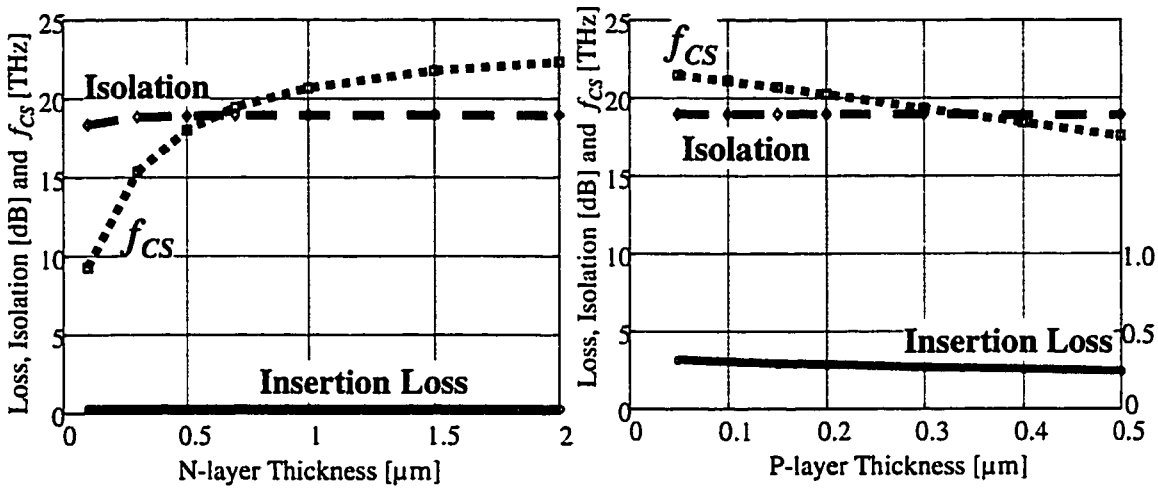


Figure 3.8. Influence of the P and N layer thickness' on the performance of a shunt InGaAs PIN diode SPST switch at *94GHz*

Changing the separation between the I-layer and the cathode showed only a slight increase of resistances for PIN diode designs with L_N as large as $5\mu m$, which allowed relaxation of fabrication requirements.

The influence of the size of the InGaAs PIN diode was studied last. When the diode diameter D was increased, the ON-state resistance was reduced, and the OFF-state capacitance was increased. When D was varied between $2\mu m$ to $20\mu m$, R_{ON} was reduced from *17* to 0.3Ω while C_{OFF} was increased from *4* to *52fF* shown in Figure 3.9. The switching cutoff frequency f_{CS} had a maximum value of *24.5THz* for InGaAs PIN diodes with diameter of $2\mu m$.

An optimal value of the trade-off between R_{ON}, R_{OFF}, and C_{OFF} is dictated by the application frequency. Large-size diodes with small resistances are best suited for low millimeter-wave range while small-size diodes with small capacitance are best employed for higher-frequency applications, such as W-band radar switches. To demonstrate the

importance of the application frequency for choosing the diode size, the isolation and the insertion loss of a shunt InGaAs PIN diode SPST switch were calculated not only at *94GHz*, but also at *35GHz*. The results are shown on the right of Figure 3.9.

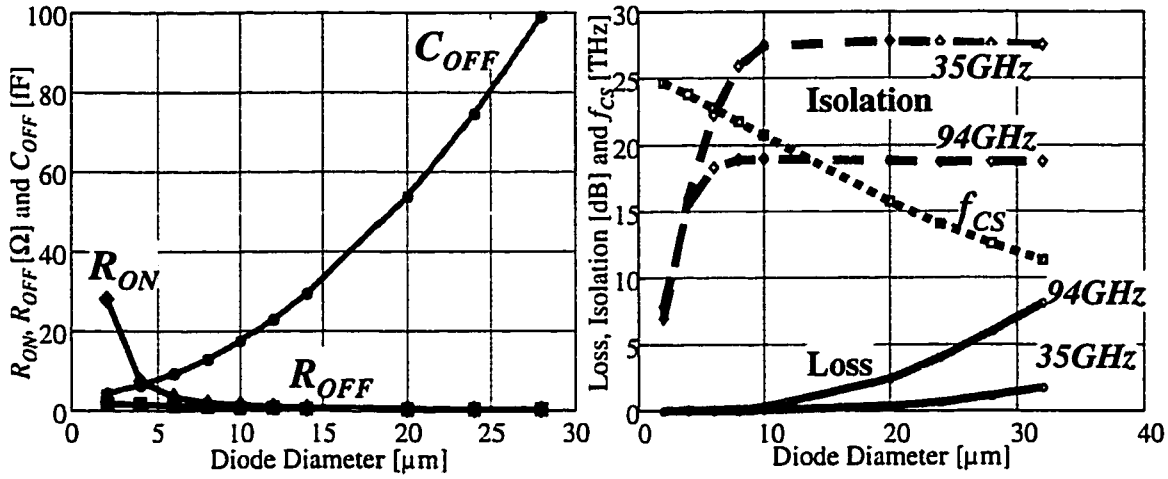


Figure 3.9. Influence of the InGaAs PIN diode diameter on the high-frequency characteristics of the InGaAs PIN diode and the performance of a shunt InGaAs PIN diode SPST switch at *94GHz* and *35GHz*

When the diode diameter was increased from *2* to *20μm*, the insertion loss of the *94-GHz* switch was degraded from *0.02dB* to *2.4dB* and the isolation was improved from *7dB* to *19dB*. The simulations showed that isolation saturated at a high value of *~19dB* for diodes larger than *8μm*. Increasing of the PIN diode diameter beyond *10μm* led to a rapid degradation of insertion loss due to increased C_{OFF}. Consequently, InGaAs PIN diodes with *8-* and *10-μm* diameters were selected for design of W-band PIN switches. While the *5μm*-diameter diodes had higher f_{CS} values, the simulations showed that the isolation level provided by the smaller diodes is not acceptable for switching applications.

The results of a similar study performed for Ka-band switches operating at *35GHz* are also shown in Figure 3.9. Due to the lower frequency of operation, the design of InGaAs PIN diode with *~20μm* diameter was optimal leading to high isolation of *27dB* and low insertion loss of *0.35dB*.

The results of the simulations discussed in this section enhanced understanding of the relationship between the design of PIN diodes and the performance of PIN diode switches. It was found that for selected bias conditions the insertion loss of the investigated W-band InGaAs PIN diode switch can be significantly improved and the

isolation only slightly degraded for designs with the I layer thickness of ~*1μm*. Increasing the thickness of the I layer much above *1μm* did not lead to an improved performance because of the background doping of InGaAs. At the same time, the high isolation and the low insertion loss can be preserved by keeping the doping of the N and P layers above a critical level of $5\times10^{18}cm^{-3}$. InGaAs PIN diodes with *8* to *10μm* diameters were found best suited for W-band switching applications. While the switching-cutoff-frequency figure of merit was useful for optimization of most of the PIN diode design parameters, it did not predict reduced isolation for the small-size (<*8μm*) diodes.

Simulations predicted that a W-band SPST switch employing *50-Ω* transmission lines and an optimized InGaAs PIN diode would have small insertion loss (*0.3dB*) and high isolation (*19dB*) at *94GHz*.

3.2. InGaAs PIN Diode Technology

InGaAs PIN diodes described in this work were made of $In_{0.53}Ga_{0.47}As$ lattice-matched to InP. The InGaAs layers were grown epitaxially on InP substrates. Both Molecular-Organic Chemical Vapor Deposition (MOCVD) and Molecular Beam Epitaxy (MBE) techniques have been employed for growth of InGaAs PIN diodes. MBE-grown GaAs PIN diodes were also fabricated for comparison purposes.

All diodes were fabricated on the top of semi-insulating substrates using planar monolithic millimeter-wave integrated circuit (MMIC) technology. The details of the growth and fabrication are given below.

3.2.1. Growth of InGaAs PIN layers

The MOCVD InGaAs PIN layers were grown using an in-house EMCORE GS3200 system. The susceptor with the sample was rotated at *100rpm*, which led to good thickness and compositional uniformity of the epitaxial InGaAs layers. TMIn and TMGa were used as group III sources, while 100% AsH_3 was employed as a group V source. Disilane (Si_2H_6) and DEZn were employed for n-type and p-type doping, respectively. All layers were grown at low pressure (*60torr*). The details of InGaAs PIN diode layers are

given in Table 3.1. Such selection of thickness' and doping levels was used to reduce the ON-state resistance and the OFF-state capacitance as discussed in *Section 3.1.3*.

Table 3.1. MOCVD-grown InGaAs PIN Diode Layers

Layer Name	Material	Thickness [μm]	Doping Type	Carrier Concentration [cm^{-3}]
P	$In_{0.53}Ga_{0.47}As$	*0.15*	p-type	1.5×10^{19}
I	$In_{0.53}Ga_{0.47}As$	*1.0*	n-type	*nid*
N	$In_{0.53}Ga_{0.47}As$	*1.0*	n-type	1.5×10^{19}
Substrate	InP	*400*	semi-insulating	NA

First, the 1μm-thick N layer was grown with a carrier density of $1.5\times10^{19}cm^{-3}$. According to numerical simulations described in *Section 3.1.3*, satisfactory performance of W-band InGaAs PIN diodes was achieved for N layers with thickness $W_N>0.5\mu m$ and doping $N_N>5\times10^{18}cm^{-3}$. Not only did making the N layer thicker and higher-doped further improve the performance of diodes, but it also increased the margin of error for growth and fabrication.

The doping for the N layer was achieved by using a disilane source. The empirical relationship between the dopant flux and resulting carrier concentration was linear up to $1.5\times10^{19}cm^{-3}$. The violation of a linear dependence suggested possible saturation of the dopant and degradation of crystal quality, reflected by poor morphology of grown layers. Thus, the maximum doping achievable within high-quality growth conditions was selected for growing the InGaAs N layer.

Next, the *1μm*-thick I layer was grown. The optimization study in Section 3.1.3 suggested that diodes with *1*- to *1.5μm*-thick I layers are best suited for W-band switching applications. The non-intentionally-doped (*nid*) InGaAs layers had n-type conductivity with carrier concentration $N_I=3\text{-}5\times10^{15}cm^{-3}$.

Special attention was paid to the optimization of the transition from the N layer to the I layer. SIMS characterization of InGaAs/InP layers showed [56] that a dopant tail was present in the transition from an N^+ subcollector layer to an N^- collector layer and led to the reduction of the effective collector layer thickness. This problem was related to the long time constant associated with the double dilution doping line of the MOCVD system. If the dopant dilution-mixing tank had not been replenished at the new

concentration level during growth interruption between the N^+ and N^- layers, the doping profile of the N^- layer was severely affected. To avoid this problem, the mixing tank was evacuated during the growth interruption and sharper dopant transitions were achieved.

The P layer was grown last with a thickness W_P of *0.15μm* and a doping level N_P of $1.5 \times 10^{19} cm^{-3}$. Diethilzinc was used as the p-type dopant. Such high carrier-activation level of Zn in InGaAs was achieved by lowering the growth temperature. While the n-type N and I layers were grown at a *570°C*, the p-type P layer was grown at a lower temperature of *530°C* to enhance maximum Zn incorporation and reduce Zn outdiffusion into the underlying I layer.

The InGaAs PIN diode layers were also grown using solid-source MBE (see Table 3.2). The growth rate was *0.7μm/hr*, and a *380Å*-thick undoped AlInAs buffer was used between the InP substrate and the diode layers. In order to obtain an abrupt doping profile from the N to I layer and to assure a low background doping in the I InGaAs layer, the growth temperature was kept at a low value of *450°C*.

Table 3.2. MBE-grown InGaAs PIN Diode Layers

Layer Name	Material	Thickness [μm]	Doping Type	Carrier Concentration [cm^{-3}]
P	$In_{0.53}Ga_{0.47}As$	*0.15*	p-type	1.4×10^{19}
I	$In_{0.53}Ga_{0.47}As$	*1.0*	n-type	*nid*
N	$In_{0.53}Ga_{0.47}As$	*1.0*	n-type	1.4×10^{19}
Substrate	InP	*400*	Semi-insulating	NA

For comparison purposes, a solid-source MBE system was also used to grow GaAs-based PIN diode layers to the doping and thickness specifications of Table 3.3. GaAs PIN diode layers were grown in semi-insulating GaAs wafers with AlAs/GaAs super-lattice (*10×*) and I-GaAs buffer layers. To reduce the outdiffusion of the n-type dopant, the doping concentration of the N layer was reduced to $5 \times 10^{18} cm^{-3}$ and the growth temperature of the I and P GaAs layers was lowered to *480°C*.

Table 3.3. MBE-grown GaAs PIN Diode Layers

Layer Name	Material	Thickness [μm]	Doping Type	Carrier Concentration [cm^{-3}]
P	GaAs	*0.15*	p-type	1×10^{19}
I	GaAs	*1.0*	n-type	*nid*
N	GaAs	*1.0*	n-type	5×10^{18}
Substrate	GaAs	*400*	semi-insulating	NA

All PIN layers were processed using planar semiconductor technology described in the next section.

3.2.2. Fabrication of InGaAs PIN Diodes

OFF-state capacitance and ON-state resistance of switching InGaAs PIN diodes needed to be minimized to achieve W-band switching capabilities. For this purpose, the diodes were fabricated on small isolated mesas. The electrical connections with the PIN diodes were made using low-parasitics interconnects, airbridges and via-holes. A detailed description of the PIN diode fabrication process is given below.

The first step in fabricating the devices was the deposition of anode contacts. The anodes had circular shapes with diameters varying between *5* and *20μm*. The anodes were deposited directly on the top P layer using liftoff process employing a positive photoresist. Immediately prior to the deposition of the anodes, native oxide was etched in *Buffered HF* acid (*BHF*).

The ohmic contacts to p-type InGaAs were optimized in [56] and were made of *Pt/Ti/Pt/Au* (*50/250/250/2000Å*)) metal layers. The metal deposition was performed in vacuum (*~10^{-6}torr*) using an evaporator chamber with e-beam heating of the pure metal targets and in-situ real-time thickness control. After the deposition, InGaAs PIN diode wafers were lifted off in acetone. At this stage, the anode contacts were left non-annealed until later.

The second fabrication step was the etching of device mesas. A photoresist mask was used to protect the device mesa. The etching was performed in an $H_3PO_4:H_2O_2:H_2O$ with a typical etch rate of *100Å/sec*. The device mesas were etched until the P and the I layer were removed and the N layer was exposed.

The desired etch depth ($1.15\mu m$) was several times larger than that for a typical HBT or HEMT mesa etch. Thus, the lateral undercutting of the mask edge was of special concern. The distance of the lateral undercut was approximately equal to the etching depth, it could, however, be greatly increased by the presence of native oxide. Native oxide underneath the photoresist mask was also etched by an H_3PO_4-based solution, but at a faster rate; which enhanced the lateral undercutting of masked areas. An oxide etch in *BHF*, immediately followed by N_2-ambient bake and photoresist deposition were used to de-oxidize the surface and minimize the lateral undercut.

Etch depth was monitored by a DEKTEK profile meter, which had precision of $0.1\mu m$. The complete removal of the P and I layers was confirmed by electrical measurement of surface breakdown. The surface breakdown voltage was measured using two needle probes placed $\sim 50\mu m$ apart on the surface and connected to a Tektronix curve tracer. The typical surface breakdown voltages observed in InGaAs PIN diodes are given in Table 3.4.

Table 3.4. Surface Breakdown of InGaAs PIN layers

Layer Name	P	I	N
Surface Breakdown [V]	0.2-0.4	3-5	0.5-1

The device mesa etch completion was confirmed by the reduction of the surface breakdown voltage associated with moving of the etched surface from the I to N layer. A microscope photograph, shown in Figure 3.10a, depicts an InGaAs PIN diode after the device mesa etching had been completed.

The etching of the isolation mesa followed the etching of the device mesa. The isolation mesa etch was about 1μm deep so that the InGaAs N layer was completely removed and the semi-insulating InP substrate was exposed. Only a rectangular mesa made of N layer surrounding the device mesa remained after the isolation step was done. The fabricated diode is shown in Figure 3.10b. The duration of the isolation etch was monitored by visual observation of wafer coloring. The difference in indexes of refraction and colors between InGaAs and InP layers resulted in appearance of interference patterns and abrupt color changes as the InGaAs layers were etched away.

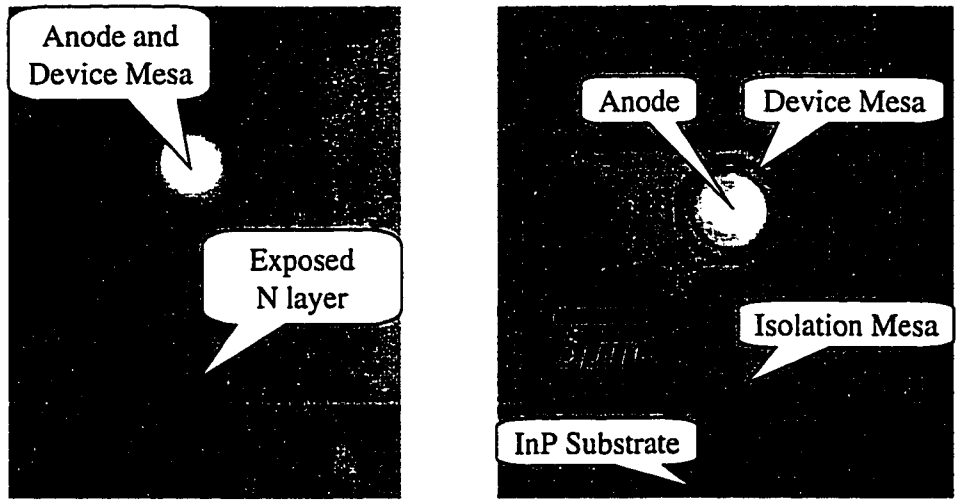


Figure 3.10. Optical microscope photographs of InGaAs PIN diodes during fabrication: (a) after device mesa etch and (b) after isolation mesa etch

The final confirmation of achieved isolation was made by measuring surface breakdown voltage on the top of the exposed InP wafer, which normally exceeded *25V*.

During the next step, cathode contacts were deposited on top of the N layer surrounding the device mesa. An SEM photograph of InGaAs PIN diode indicating the PIN layers, anode, and cathode is shown in Figure 3.11.

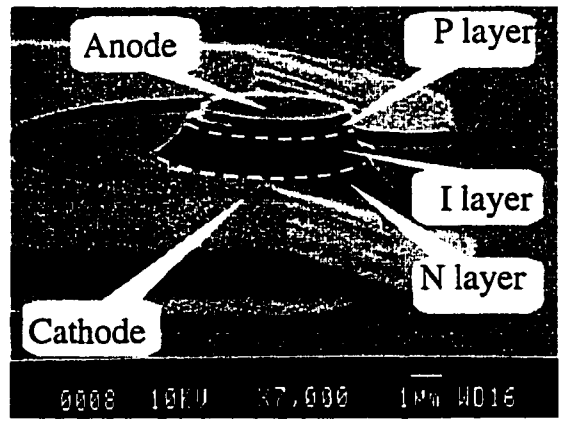


Figure 3.11. SEM photograph of a partially fabricated InGaAs PIN diode

Ti/Pt/Au (*250/250/2000Å*) metals were used as n-type ohmic contacts. At this point both anode and cathode contacts were exposed to a high-temperature anneal in order to lower the specific contact resistance. Annealing was performed for *7sec* at *400°C* in Ar_2 ambient to reduce surface degradation.

Transmission line measurements (TLM) technique was used for characterization of InGaAs PIN diode ohmic contacts. Typical TLM characteristics are shown in Figure 3.12. The effect of the annealing step on the N ohmics is shown in Figure 3.12. The sheet resistance R_{SH}≈150Ω/sq of the N layer was not affected by the annealing step as illustrated by the constant slope of the TLM characteristics. On the other hand, the specific contact resistivity R_{SP} was reduced by the anneal from 1×10^{-5} to $4\times10^{-6}\Omega cm^2$.

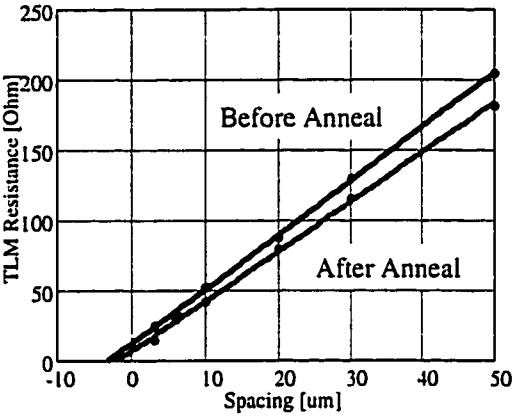


Figure 3.12. Typical TLM Characteristics of InGaAs n-type ohmic contacts

In the next step, the PIN diodes were connected to the rest of the circuit with interconnect lines and airbridges. Interconnect lines were *0.5μm*-thick and composed of *Ti/Au* (*500/4500Å*) metals. Connections to the cathode contacts were made by depositing interconnects directly over the outer parts of the contact pads as shown in Figure 3.13a.

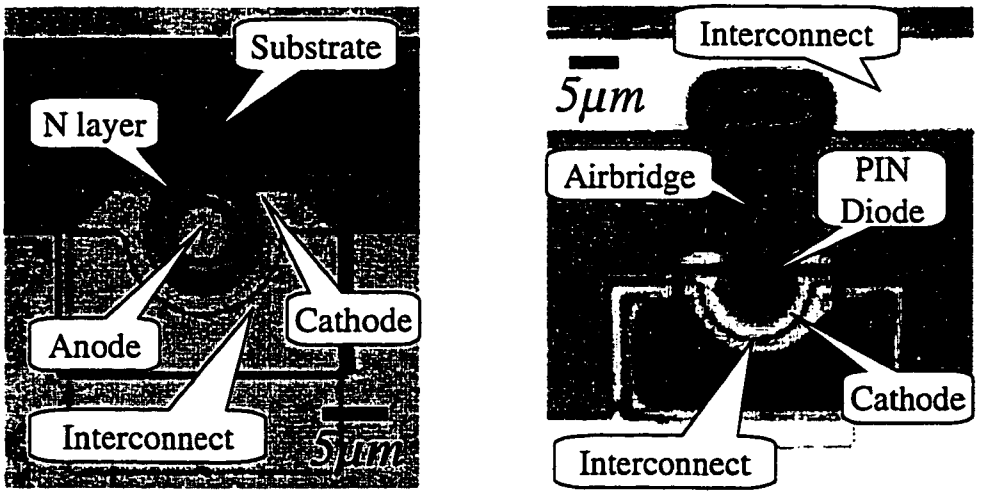


Figure 3.13. Optical microscope photograph of InGaAs PIN diodes during fabrication (a) after interconnect deposition and (b) after airbridge plating

Low-parasitics airbridge technology was used to access the anode contacts on the top of the PIN diode mesas. The airbridge fabrication employed a double-step process. During the first step, airbridge pillar patterns were opened in the photoresist mask and the seed metals *Ti/Au/Ti* (*250/1000/500Å*) were deposited. No lift-off was performed. During the second step, airbridge patterns were opened above the pillars, the top *Ti* layer of the seed metals was removed by *BHF*, and the *3μm*-thick *Au*-airbridges were electroplated in a cyanide-based *Au*-solution. Structurally stable airbridges with *Au* of good morphology were plated for the conditions when the plating rate was *0.1μm/min* and current density was *~1mA/cm²*.

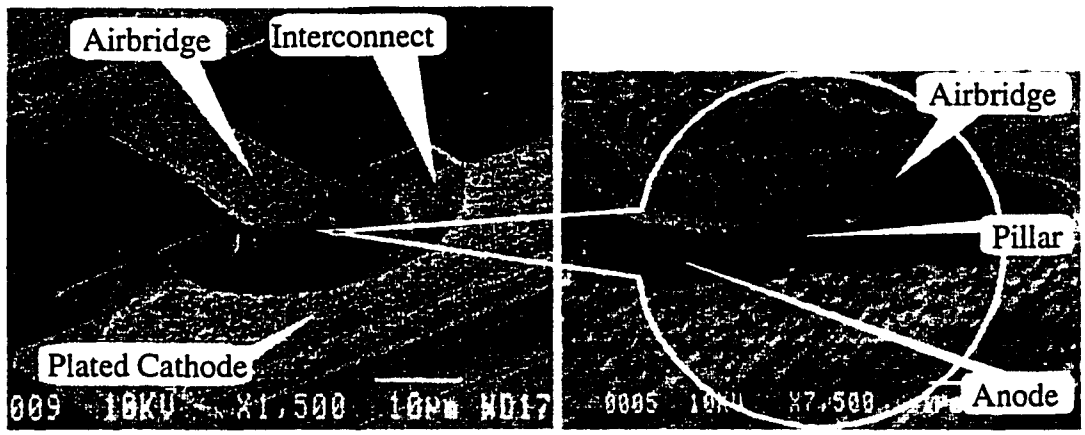


Figure 3.14. SEM photograph of a fabricated InGaAs PIN diode

Figure 3.14 shows a scanning electron micrograph of a fully fabricated InGaAs PIN diode and a close-up which allows distinguishing the airbridge, its pillar, and the anode. Parts of cathodes were also Au-plated to improve step coverage over the isolation mesas.

3.3. Low-Frequency Characterization of Switching InGaAs PIN Diodes

InGaAs PIN diodes were fabricated on wafers *A*, *B*, and *C*. The PIN layers on wafers *A* were grown by MOCVD (UofM), on wafer *B* by MBE (external supplier), and on wafer *C* also by MOCVD (UofM). GaAs PIN diodes were also fabricated on wafer *D* grown by MBE (external supplier) for comparison. The specifications for all layers were listed in Section 3.2.1 in Table 3.1, Table 3.2, Table 3.3, respectively. The diodes were fabricated using the technology described in Section 3.2.2.

The performance of the fabricated InGaAs PIN diodes was measured by means of various electrical tests, such as DC current-voltage (I-V) characterization, low-frequency capacitance-voltage (C-V) measurements, and high-frequency small-signal S-parameter characterization.

Applying numerous characterization techniques allowed obtaining detailed information about the InGaAs PIN layers, as well as evaluating the OFF-state capacitance and the ON-state resistance of the diodes at different biasing conditions as desired for microwave switching applications.

3.3.1. DC Characterization

The first characterization of the InGaAs PIN diodes was performed by analyzing reverse and forward bias I-V characteristics of the devices and test structures. The quality of the fabricated switching PIN diodes can be quickly estimated from the values of turn-on voltage V_{ON}, ideality factor n, reverse leakage current I_{OFF}, and reverse breakdown voltage V_{BD}. An ideal switching device has zero turn-on voltage, zero reverse leakage current, and infinite reverse breakdown. The turn-on voltage V_{ON} of a practical PIN diode is determined primarily by the built-in voltage of the p-n junction and is proportional to the bandgap energy of the semiconductor. A higher than usual turn-on voltage can be an indication of poor material or contact quality [57]. A PIN diode in the OFF-state conducts small leakage current I_{OFF} and has a finite reverse breakdown V_{BD}. If the background concentration of the I layer is high, the leakage current is increased, and the reverse breakdown voltage is reduced.

I-V characteristics of the fabricated diodes were measured using a semiconductor parameter analyzer *HP4145* and saved on the computer. Typical I-V characteristics for InGaAs PIN diodes from wafers *A*, *B*, and *C* are shown in Figure 3.15.

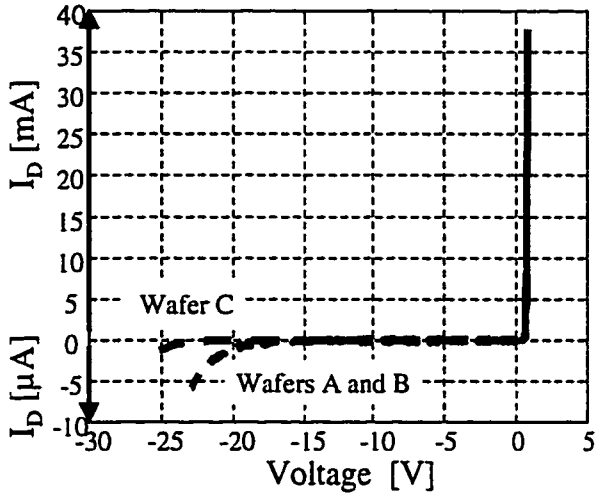


Figure 3.15. I-V characteristics of InGaAs PIN diodes

The following definitions were used to analyze experimental data:

turn-on voltage V_{ON} was defined as the forward bias at which the forward current density was $10A/cm^2$;

ideality factor n was calculated in the region of the I-V characteristics with maximum I-V slope, for forward bias between *0.5V* and *0.6V*;

reverse breakdown V_{BD} was defined as the voltage where the slope of the reverse current (log scale) abruptly changed its value (see Figure 3.18).

However, the ON-state resistance of the InGaAs PIN diodes could not have been extracted from the DC I-V characteristics since under high-injection conditions ($N_{INJ}>N_I$) conductivity-modulation effects reduce the differential resistance of the I layer to a very low value. The evaluation was further complicated by the presence of an S-shaped I-V curve with a region of negative differential resistance (NDR) as shown in Figure 3.16. Such NDR I-V characteristics have also been reported for GaAs PIN diodes [57], but no explanation for this phenomenon was given. Pulsed I-V characterization of InGaAs PIN diodes was performed in the course of this work in order to understand the origin of these characteristics and allowed identification of thermal nature of the NDR in PIN diodes. When InGaAs PIN diodes were biased using short (*300nS*) voltage pulses, the slope of their I-V characteristics remained positive as illustrated in Figure 3.16. When the pulse width was increased to $1\mu s$, self-heating of the forward-biased p-n junction led to appearance of an S-shaped I-V curve with a region of negative differential resistance. The

self-heating was even more pronounced for the case of DC characterization which employed long averaging time of *10ms*. It should be noted that the self-heating was observed only at extremely high levels of current density (*>100KA/cm*^{2}) far above normal operating conditions.

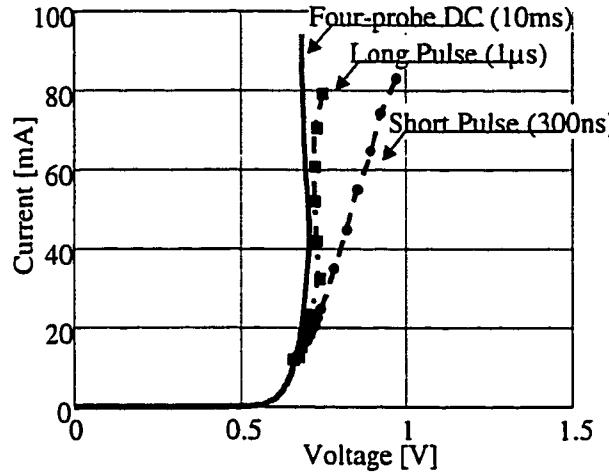


Figure 3.16. I-V characteristics of InGaAs PIN demonstrating thermal nature of the experimentally observed negative differential resistance

The results of DC analysis are listed in Table 3.5. InGaAs PIN diodes from all three wafers demonstrated a low turn-on voltage of *~0.43V* indicating that high-quality PIN layers were grown by both MOCVD, as well as MBE growth techniques. The bandgap of InGaAs is smaller than the bandgap of GaAs (*0.75eV* vs. *1.42eV*) leading to lower turn-on voltages for InGaAs than GaAs PIN diodes as can be seen by comparing the results in Table 3.5.

Table 3.5. List of InGaAs PIN wafers and extracted DC I-V parameters

Parameters	Wafer *A*	Wafer *B*[1]	Wafer *C*[2]	Wafer *D*
Turn-on Voltage, V_{ON} [V]	*~ 0.46*	*0.41 ± 0.04*	*0.43 ± 0.04*	*~ 1.1*
Ideality Factor, *n*	*~ 1.2*	*1.46 ± 0.22*	*1.45 ± 0.21*	
Reverse Breakdown, V_{BD} [V]	*~ 15*	*~ 19*	*~ 20*	*~ 30*

[1] Statistics obtained by measuring 18 devices.

[2] Statistics obtained by measuring 12 devices.

The ideality factor of the InGaAs PIN diodes was also extracted from the experimental I-V characteristics. The ideality factor of the PIN diodes from wafer A ($n \approx 1.2$) differs significantly from the ideality factors of the devices from wafers B and C ($n \approx 1.45$). A probable reason is the different carrier concentrations in the I layers of wafer *A* and wafers *B* and *C*. The ideality factor was extracted at low injection conditions when the concentration of carriers injected in the I layer (N_{INJ}) was smaller than the background concentration N_I. Under low injection conditions, the I layer is still highly resistive and the current of the PIN diode can be expressed using the following dependence on the applied voltage V_A:

$$I(V_A) = I_{SAT}\left(e^{\frac{q(V_A - I \times R_I)}{n_1 kT}} - 1\right) = I_{SAT}\left(e^{\frac{qV_A}{n_2 kT}} - 1\right) \tag{3.5}$$

where I_{SAT} is the reverse saturation current, R_I is the resistance of the I layer, n_1 is the ideality factor, and n_2 is an effective ideality factor which includes effects of R_I. A fraction of V_A falls across R_I and reduces the effective voltage applied to the p-n junction. If the background concentration of the I layer resistance is reduced, the I layer resistance is higher, and the effective ideality factor n_2 is increased. Thus, a PIN diode with a lower background concentration of the I layer has a higher ideality factor than a PIN with a higher concentration. To confirm this trend, numerical simulations described in Section 3.1.2 were also used to evaluate the dependence of n on the doping of the I-layer N_I. The results are shown in Figure 3.17 together with the experimental data.

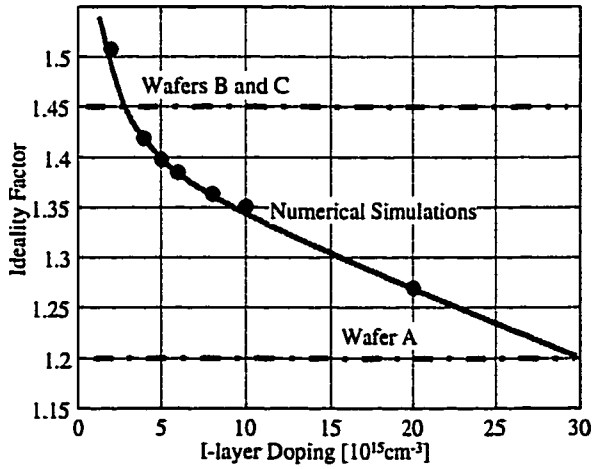


Figure 3.17. Dependence of Ideality Factor on the doping of the I layer

The results indicated that the I layer concentration on wafers *B* and *C* was in the desired range ($N_I<5\times10^{15}cm^{-3}$) while the I layer concentration on wafer *A* was much higher ($\sim3\times10^{16}cm^{-3}$). This conclusion was further supported by high leakage and small breakdown observed for PIN diodes from wafer *A*, and by C-V characterization.

The reverse I-V characteristics of InGaAs PIN diodes from wafers *B* and *C* had high reverse breakdown (*~20V*) and low leakage current density ($0.01A/cm^2$) (see Figure 3.18). On the other hand, diodes from wafer A had much higher leakage currents ($0.5A/cm^2$). It was also attributed to a higher concentration in the I layer in agreement with a discussion on basic properties of PIN diodes from Chapter 2.

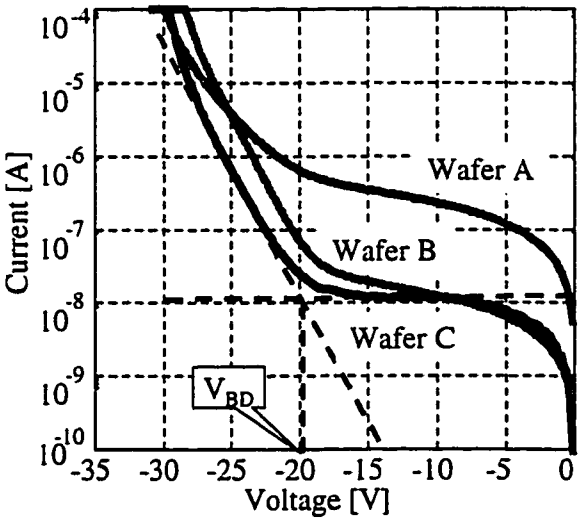


Figure 3.18. Reverse I-V characteristics for InGaAs and GaAs PIN diodes

3.3.2. Study of Reverse Breakdown

The reverse breakdown voltage of PIN diodes was measured as a function of ambient temperature in order to identify what mechanism was responsible for the breakdown. In case of tunneling, the breakdown voltage should decrease with increasing temperature because more carriers with higher energy are available for inter-band tunneling. On the other hand, in case of impact-ionization, the breakdown voltage should increase with temperature because phonon scattering is increased and a higher electric field is required to accelerate carriers to avalanche conditions. During experiments, the

breakdown voltage increased when the temperature was increased for InGaAs PIN diodes as shown in Figure 3.19 for devices from wafers *B* and *C*.

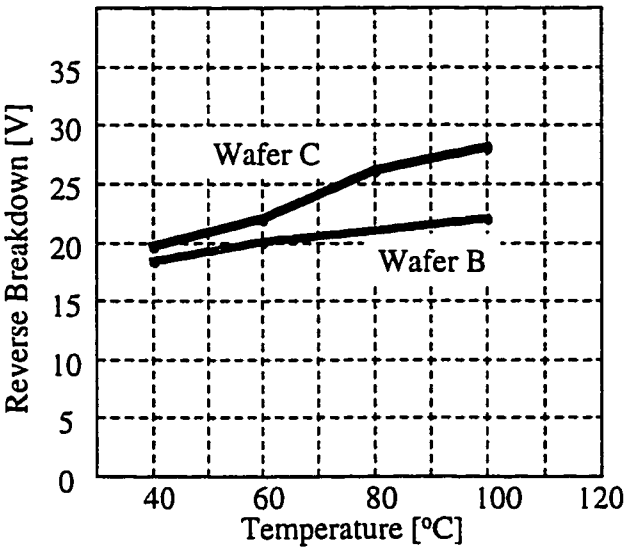


Figure 3.19. Breakdown of InGaAs PINs as a function of temperature

A positive temperature dependence of the breakdown voltage showed that the impact ionization mechanism was responsible for the breakdown. It is possible to evaluate the peak electric field at the breakdown voltage using the following expression:

$$F_P \approx \sqrt{\frac{2qN_I(V_{PI} - V_{BD})}{\varepsilon}} \tag{3.6}$$

where N_I is the carrier concentration in the I layer, V_{BD} is the breakdown voltage, V_{PI} is the built-in voltage of the PI junction, and ε is the dielectric constant of InGaAs. Using equation (3.6), the peak electric field at breakdown F_P of *~180KV/cm* was estimated for InGaAs PIN diodes. This value of F_P provides an estimate for critical breakdown field F_B in I-InGaAs which is in good agreement with recent studies of impact ionization in InGaAs/InP HBTs [58] (F_B<*200KV/cm*).

3.3.3. Low-Frequency C-V Characteristics

Carrier concentration profiles of InGaAs PIN diodes were extracted from capacitance-voltage measurements. The C-V measurements were performed using an *LCR* meter, which measured the small-signal low-frequency impedance of the PIN diodes

using a *100-KHz 25-mV* test signal. The C-V characteristics of *50μm*-diameter test PIN diodes from wafers *A*, *B*, and *C* are shown in Figure 3.20a). Devices from wafers *B* and *C* had similar characteristics, while devices from wafer *A* manifested a significantly higher capacitance, which did not saturate for reverse bias as large as *-10V*. The variation between wafers became less significant at high bias when a larger portion of the I layer was depleted. This difference between the C-V characteristics was due to variations in the carrier concentration in the I-layer.

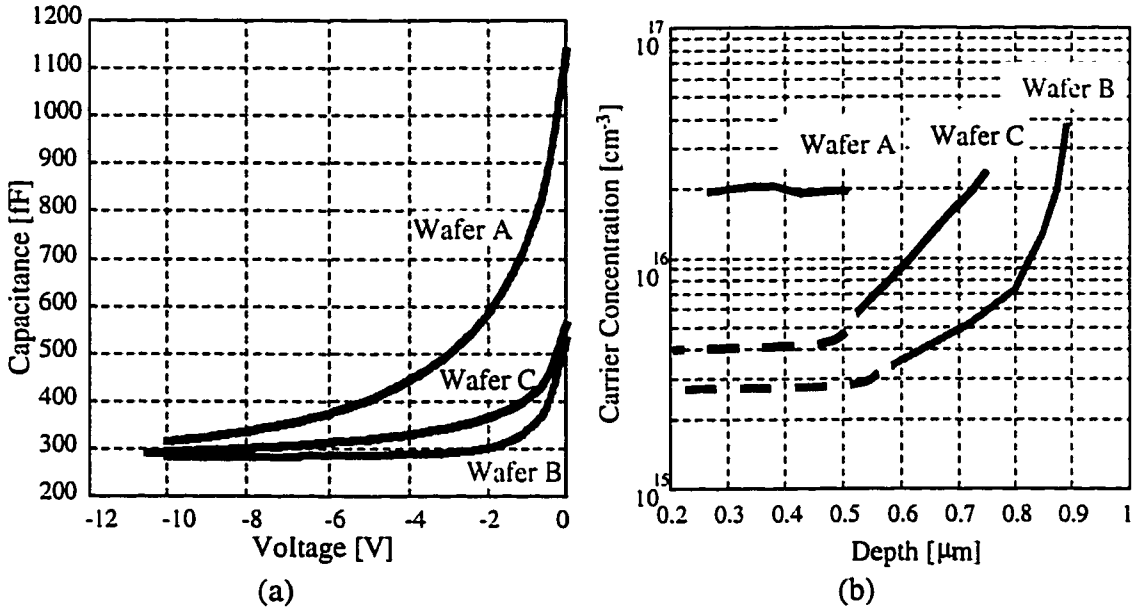


Figure 3.20. a) C-V characteristics of InGaAs PIN diodes; b) concentration profiles extracted from the C-V characteristics.

Carrier concentration profiles were extracted from the C-V characteristics (shown in Figure 3.20b) using the following expression:

$$N_I(V) = \frac{1}{\frac{d\left(\frac{1}{C(V)^2}\right)}{dV}\frac{q\varepsilon A^2}{2}} \qquad (3.7)$$

$$x(V) = \frac{\varepsilon A}{C(V)}$$

where A is the diode area and ε is the dielectric constant. Large-area (A=*2000μm*) test diodes were used for C-V characterization since their parasitic pad capacitance was negligible compared with the intrinsic depletion capacitance of the actual diodes.

The background carrier concentration of the I layer from wafer *A* was uniform at a high value of $2\times10^{16}cm^{-3}$, while the I layer concentrations on wafers *B* and *C* had small minimum values of $3\text{-}5\times10^{15}cm^{-3}$. The I layer concentration on wafers *B* and *C* also showed noticeable variation with the distance indicating dopant outdiffusion typical in epitaxial growth. This feature was more obvious in wafers B and C since they had lower background concentration N_I. The minimum of N_I was located closer to the p/i-junction side of the PIN layer, and the concentration increased toward the i/n-junction side. This increase of N_I was attributed to the delayed incorporation of the n-type dopant during the switching between heavy-doped N and low-doped I layers as discussed in Section 3.2.1. The design thickness of the I layer was $1\mu m$, but in the actual layers, it was reduced by the n-type doping tail. The effective thickness and doping of the I layer were extracted from the C-V measurements and listed in Table 3.6.

Table 3.6. List of InGaAs PIN diode wafers and extracted C-V parameters

Parameters	Wafer *A*	Wafer *B*	Wafer *C*
$C_{ZERO}(V=0V)$ [fF/μm^2]	*0.505*	*0.236*	*0.250*
$C_D(V=-10V)$ [fF/μm^2]	*0.140*	*0.126*	*0.130*
N_I ($x=0.5\mu m$) [cm^{-3}]	$\sim2\times10^{16}$	3×10^{15}	5×10^{15}
W_I [μm]	*0.7456*	*0.9201*	*0.8643*

The low-frequency OFF-state depletion capacitance C_D was calculated for $10\mu m$-diameter InGaAs PIN diodes fabricated on wafers *A*, *B*, and *C* based on the data in Table 3.6. The values of C_D varied between *9.8* and *10.9fF* in good agreement with a simulated value of *10.6fF* (see Section 3.1.2). This agreement between the experimental low-frequency and the simulated high-frequency capacitance was possible due to a high dielectric relaxation frequency f_{DR} of *880GHz* in InGaAs (see Section 2.3.1 of Chapter 2).

DC and low-frequency characterization performed on InGaAs PIN diodes were used to obtain information about InGaAs PIN layers and InGaAs material parameters, to analyze the fabrication results, and to evaluate switching characteristics of PIN diodes. The latter was also directly evaluated using high-frequency S-parameter characterization described in the next section.

3.4. High-Frequency Characterization of Switching InGaAs PIN Diodes

InGaAs PIN diodes were integrated with coplanar waveguides forming simple SPST switches and their bias-dependent S-parameters were measured by on-wafer probing between *0.5* and *40GHz*. Series-connected InGaAs PIN diodes were chosen for this testing as, for this frequency range, series SPST configuration allowed easier extraction of small-signal equivalent circuit elements. Switches with *10μm* and *5μm*-diameter InGaAs PIN diodes were analyzed.

3.4.1. Small-Signal Characteristics of Series InGaAs PIN SPST Switches

The schematic of a series PIN diode SPST switch is shown in Figure 3.21. When the PIN diode is turned on, it can be thought of as a small resistance, which connects ports *"1"* and *"2"*. In this case, the switch is transmitting, S_{21} measures its insertion loss, and S_{11} measures its return loss. In the OFF-state, the diode acts as a small capacitance isolating ports *"1"* and *"2"*. In this case, switch is reflecting, S_{21} measures isolation, and S_{11} measures reflection loss.

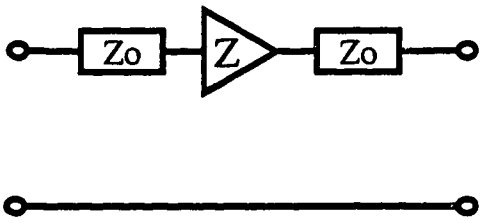


Figure 3.21. Schematic of a series PIN diode SPST switch

The equivalent circuits of the InGaAs PIN diodes have been discussed in Section 3.1.1 and are shown in Figure 3.2. The ON-state equivalent circuit includes the ON-state resistance R_{ON}, airbridge inductance L_{AB}, and parasitic capacitance C_{PAR}. When the diode is turned off, the I layer is depleted and the resistance R_{ON} is replaced by the I layer capacitance C_D and the OFF-state resistance R_{OFF}. The OFF-state impedance is determined primarily by the OFF-state capacitance C_{OFF} and is composed of the depletion capacitance C_D and the parasitic capacitance C_{PAR}.

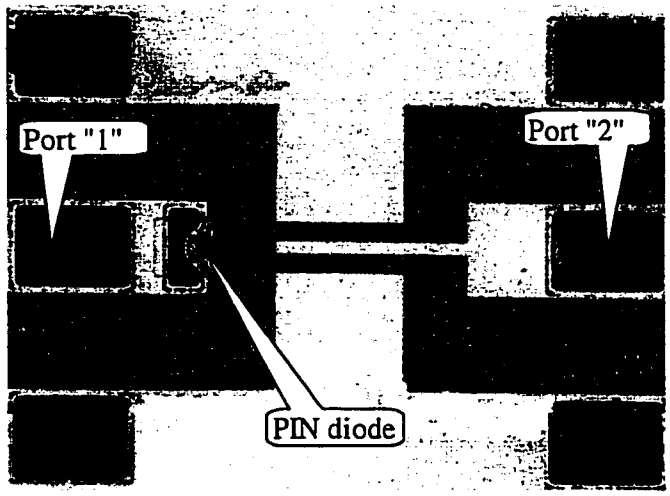


Figure 3.22. Photograph of a InGaAs PIN diode series SPST switch

A fabricated InGaAs PIN diode series SPST switch is shown in Figure 3.22. The diodes were switched from the ON-state (V_D=*0.75V*) to the OFF-state (V_D=*-10V*) and their S-parameters were measured for frequencies between *2* and *40GHz*. The S-parameters of series SPST switches using *10* and *5μm*-diameter InGaAs PIN diodes are shown in Figure 3.23.

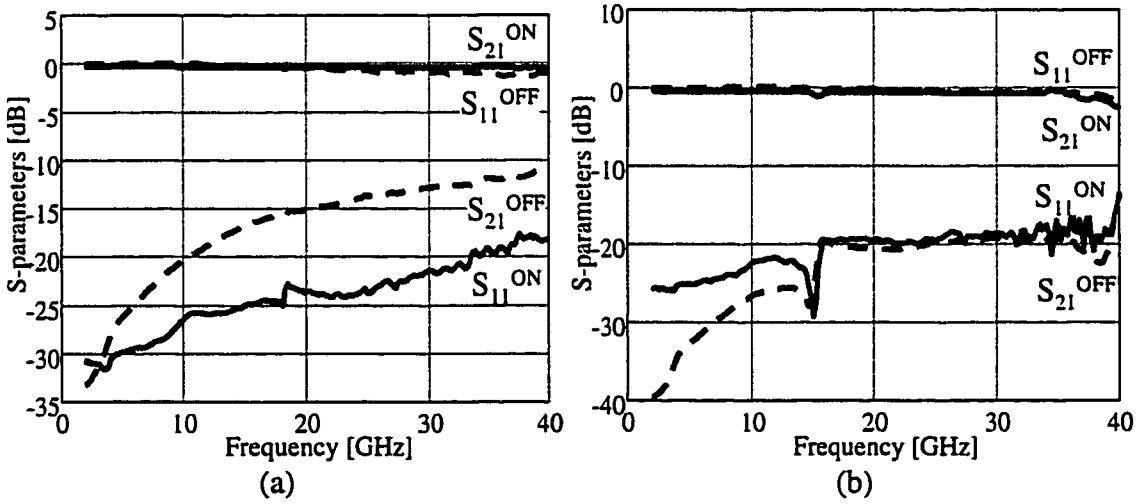


Figure 3.23. S-parameters of InGaAs PIN diode series SPST switches with (a) 10μm-diameter and (b) 5μm-diameter diodes

Series InGaAs PIN SPST switches using both *10* and *5μm*-diameter diodes demonstrated excellent switching action for up to millimeter-wave frequencies. The insertion loss of *10μm* SPST was less than *0.5dB* and the return loss was better than *18dB* for frequencies up to *40GHz*. The return loss was less than *1.2dB* and the isolation was

larger than *11dB*. The insertion loss of *5μm* SPST was less than *2dB*, the return loss was better than *14dB*, the return loss was less than *1.5dB*, and the isolation was larger than *19dB* for frequencies up to *39GHz*.

The ON-state resistance of the *10μm*-diameter InGaAs PIN was smaller than that of the *5μm*-diameter diode which was reflected by its smaller insertion loss (*0.5* vs. *2dB*), smaller reflection loss (*1.2* vs. *1.5dB*), and better matching (*18* vs. *14dB*). On the other hand, the OFF-state capacitance of the *5μm*-diameter diode was smaller which caused improved isolation (*19* vs. *11dB*) for the SPST with the *5μm*-diameter diode.

It is possible to evaluate the impedance of the InGaAs PIN diode from the measured S-parameters by considering the schematic of series PIN SPST switch in Figure 3.21. Then, the transmission coefficient is simply given by (3.8) where Z is replaced Z_{ON} for the ON-state or Z_{OFF} for the OFF-state diode.

$$S_{21} = \frac{1}{1 + \frac{Z}{2Z_0}} \tag{3.8}$$

S-parameters of SPST switches included radiation and transmission line losses, as well as phase increase and resonant amplitude variations due to distributed features of the circuit layout. However, these features should not be reflected in the discrete PIN diode equivalent circuit evaluated using (3.8).

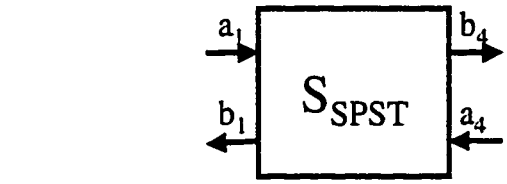
To improve accuracy of analytical extraction of PIN diode equivalent circuit, a discrete-device S-parameters extraction technique utilizing cascaded networks theory was developed. The application of this technique allowed the calculation of S-parameters of InGaAs PIN diodes with minimal influence of circuit features and extrinsic parasitics.

3.4.2. Extraction of S-parameters of Discrete InGaAs PIN Diodes

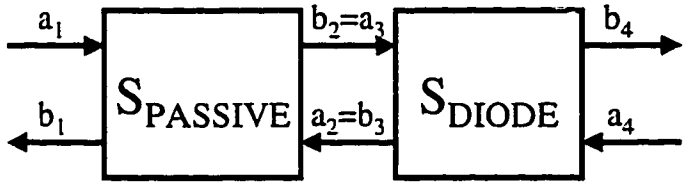
The discrete-device S-parameters extraction technique developed in this work made use of a passive structure with the same layout as that of the analyzed InGaAs PIN diode SPST switches. The S-parameter matrix of the SPST switch was represented as a cascade of the S-parameter matrices of the passive structure and the discrete PIN diode (see Figure 3.24). According to [59], the S-parameters of a cascaded network (S^{SPST})

switch can be expressed in terms of the S-parameters of its components (S^{PASS} and S^{PIN}) as shown in (3.9)

$$\left(S\right)_{SPST} = \left(\begin{array}{c|c} S_{11}^{PASS} - \dfrac{S_{12}^{PASS} S_{11}^{PIN} S_{21}^{PASS}}{S_{22}^{PASS} S_{11}^{PIN} - 1} & -\dfrac{S_{21}^{PASS} S_{12}^{PIN}}{S_{22}^{PASS} S_{11}^{PIN} - 1} \\ \hline -\dfrac{S_{21}^{PIN} S_{21}^{PASS}}{S_{22}^{PASS} S_{11}^{PIN} - 1} & S_{22}^{PIN} - \dfrac{S_{21}^{PIN} S_{22}^{PASS} S_{12}^{PIN}}{S_{22}^{PASS} S_{11}^{PIN} - 1} \end{array}\right) \tag{3.9}$$



(a)



(b)

Figure 3.24. PIN diode S-parameter extraction: (a) S-parameters of SPST switch (b) S-parameters of the cascaded networks of the passive structure and the discrete InGaAs PIN diode

The S-parameters of the discrete PIN diode in terms of the S-parameters of the SPST switch and the S-parameters of the passive structure were found by solving (3.9) and the solution is given in (3.10)

$$\left(S\right)_{PIN} = \left(\begin{array}{c|c} \dfrac{S_{11}^{SPST} - S_{11}^{PASS}}{\left(S_{11}^{SPST} - S_{11}^{PASS}\right) S_{22}^{PASS} + S_{12}^{PASS} S_{21}^{PASS}} & -\dfrac{S_{12}^{SPST}}{S_{21}^{PASS}}\left(S_{22}^{PASS} S_{11}^{PIN} - 1\right) \\ \hline -\dfrac{S_{21}^{SPST}}{S_{12}^{PASS}}\left(S_{22}^{PASS} S_{11}^{PIN} - 1\right) & S_{22}^{SPST} + \dfrac{S_{21}^{PIN} S_{22}^{PASS} S_{12}^{PIN}}{\left(S_{22}^{PASS} S_{11}^{PIN} - 1\right)} \end{array}\right) \tag{3.10}$$

where S_{11}^{PIN} coefficient should be calculated first.

A computer script implementing the formulas of (3.10) was used to extract the characteristics of the discrete InGaAs PIN diodes from the S-parameters of the SPST switches. The results of such extraction performed for a *10μm*-diameter InGaAs PIN diode in the ON and OFF-states are shown in Figure 3.25. The frequency dependence of

the SPST insertion loss contained many irregularities (such as linear phase increase and small resonant-like variations of magnitude), which were due to the distributed features of the switch as shown by $S_{21}^{SPST\text{-}ON}$ in Figure 3.25a. However, the frequency dependence of the extracted transmission coefficient of the discrete PIN diode ($S_{21}^{PIN\text{-}ON}$) was uniform indicating that the influence of the distributed features of the SPST switches was successfully removed. The removal of distributed effects was confirmed by the constant zero phase of $S_{21}^{PIN\text{-}ON}$ for up to *40GHz* as shown in Figure 3.25b. On the other hand, an accumulation of phase of the OFF-state PIN diode transmission coefficient $S_{21}^{PIN\text{-}OFF}$ in Figure 3.25b was due to the OFF-state capacitance of the PIN diode. The phase of $S_{21}^{PIN\text{-}OFF}$ excluded the influence of distributed circuit elements, which contributed to the phase of the transmission coefficient of the SPST switch $S_{21}^{SPST\text{-}OFF}$. Corrections to the magnitude of $S_{21}^{SPST\text{-}OFF}$ (isolation) were insignificant and were not included in Figure 3.25a).

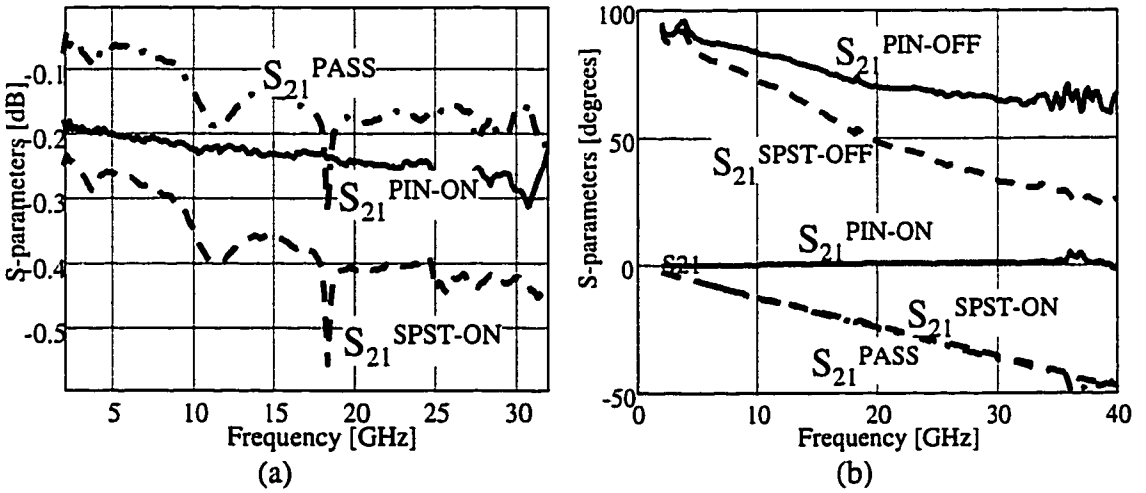


Figure 3.25. S-parameters of the InGaAs PIN SPST switch (dashed line), passive structure (dash-dot line), and discrete InGaAs PIN (solid line)

3.4.3. Equivalent Circuits of InGaAs PIN Diodes

The S-parameters of discrete InGaAs PIN diodes were extracted from S-parameters of the InGaAs PIN diode SPST series switches following the procedure described above. The insertion loss and the isolation of discrete InGaAs PIN diodes was *0.3* and *0.6dB* and *13.2* and *19.5dB*, for *10μm*- and *5μm*-diameter diodes, respectively.

The values of high-frequency impedance of the InGaAs PIN diodes in the ON (Z_{ON}) and OFF-state (Z_{OFF}) as a function of the S-parameters were calculated from equation (3.8). Then, the intrinsic equivalent-circuit elements R_{ON}, C_{ON}, R_{OFF}, and C_{OFF} are obtained from their respective impedance values using the following formulas:

$$R_{OFF\,ON} = \mathrm{Re}[Z_{OFF\,ON}] = \mathrm{Re}\left[2Z_0\left(\frac{1}{S_{21\,PIN-OFF\,ON}} - 1\right)\right] \tag{3.11}$$

$$C_{OFF\,ON} = -\frac{1}{\omega \times \mathrm{Im}[Z_{OFF\,ON}]} = -\frac{1}{\omega \times \mathrm{Im}\left[2Z_0\left(\frac{1}{S_{21\,PIN-OFF\,ON}} - 1\right)\right]} \tag{3.12}$$

The values of the equivalent circuit elements at different ON- and OFF-state biases were calculated for millimeter-wave frequencies between *20* and *35GHz*. Frequency dependence of the extracted bias-dependent elements is shown in Figure 3.26.

The extracted values of the determining elements R_{ON} and C_{OFF} showed only weak variations with frequency, confirming that the extracted values have proper physical meaning. The ON-state resistance was practically independent of frequency, while a slight decrease of the OFF-state capacitance with frequency can be attributed to measurement and extraction errors. As expected, the ON-state resistance R_{ON} decreased for larger ON-state bias, as shown in Figure 3.26(a). The OFF-state capacitance C_{OFF} decreased when the OFF-state bias was made more negative and remained saturated at its minimum value when the I-layer was fully depleted, as shown in Figure 3.26(b).

The S-parameters of the InGaAs PIN diodes are not very sensitive to variations of R_{OFF} and C_{ON}, and thus, extraction of these elements was not as reliable as that of R_{ON} and C_{OFF}. For example, extracted values of R_{OFF} approached zero for frequency less then *10GHz* (see Figure 3.26c) indicating uncertainty in the extraction of this equivalent-circuit element. The ON-state diffusion capacitance C_{ON} showed a logarithmic decrease with frequency in agreement with theory and simulations presented in Section 2.3.2 of Chapter 2. The values of C_{ON} corresponding to intended applications at W-band were found by extrapolation to *94GHz* as indicated in Figure 3.26(d). For an ON-state bias of *0.75V*, the W-band C_{ON} was *~10pF* in excellent agreement with theory and simulations.

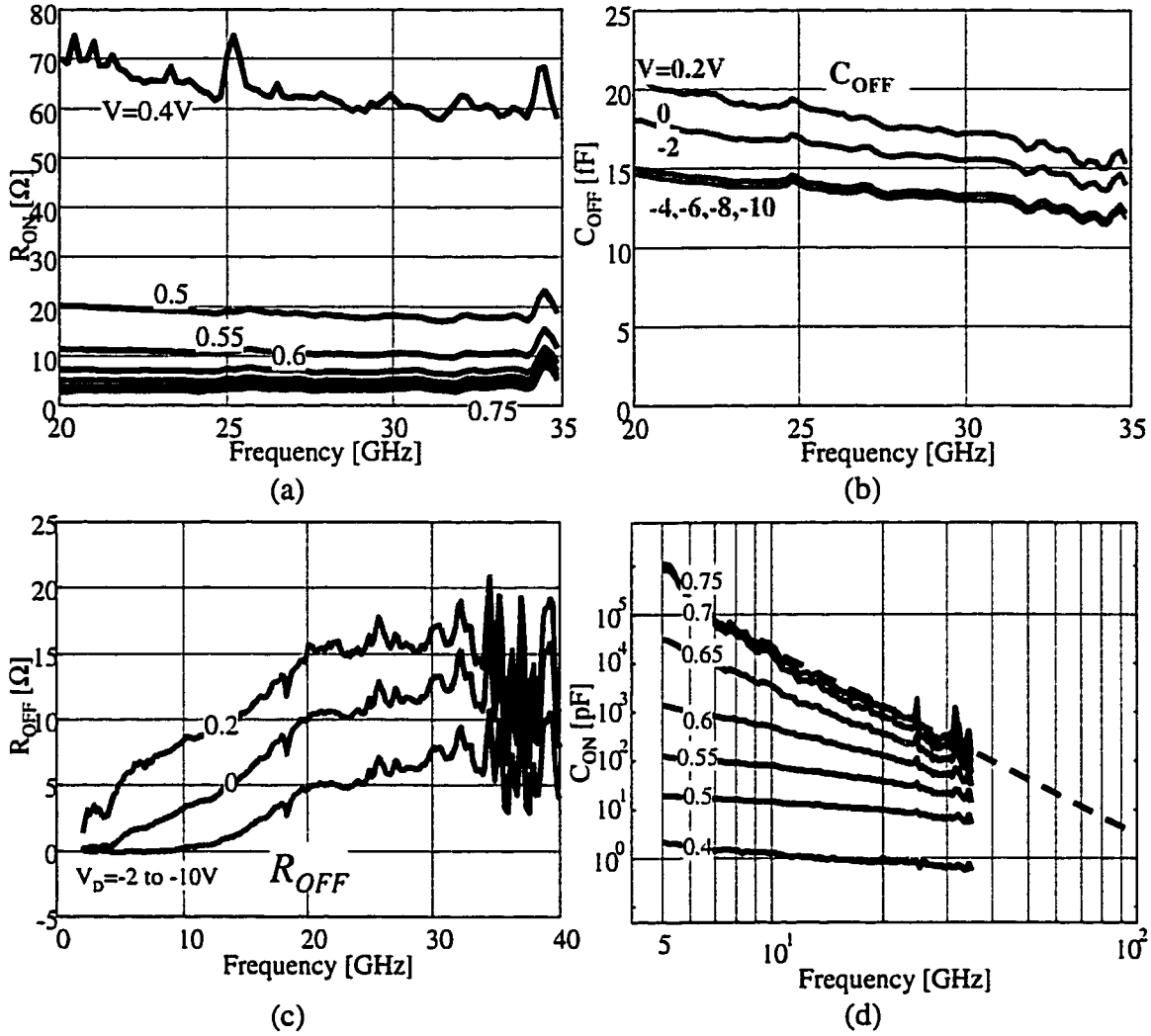


Figure 3.26. Frequency-dependent equivalent-circuit elements of a *10μm*-diameter InGaAs PIN diode: a) R_{ON}, b) C_{OFF}, c) R_{OFF}, and d) C_{ON}.

Bias-dependent values of R_{ON}, C_{OFF}, and R_{OFF} were obtained by averaging over the frequency range between *20* and *35GHz*. The results for *10* and *5μm*-diameter diodes are shown in Figure 3.27 using separate scales for the OFF- and ON-state voltages. This figure also includes bias-dependence of C_{ON} extrapolated for use at W-band frequencies.

The experimental results for both types of PINs showed excellent agreement with the expected trends (see Figure 3.4). The ON-state resistance R_{ON} dropped steeply once the bias exceeded the turn-on voltage of *0.4V* and the I-layer was filled with carriers. The OFF-state capacitance C_{OFF} decreased to its minimum value for negative bias larger than *–3V* since the I-layer were fully depleted under these conditions. R_{OFF} is associated with the resistance of undepleted I-layer and, as expected, R_{OFF} was minimal for large negative

bias, when the I-layer was fully depleted. The W-band ON-state diffusion capacitance C_{ON} had a high value of *1pF-10pF* consistently with the theoretical predictions.

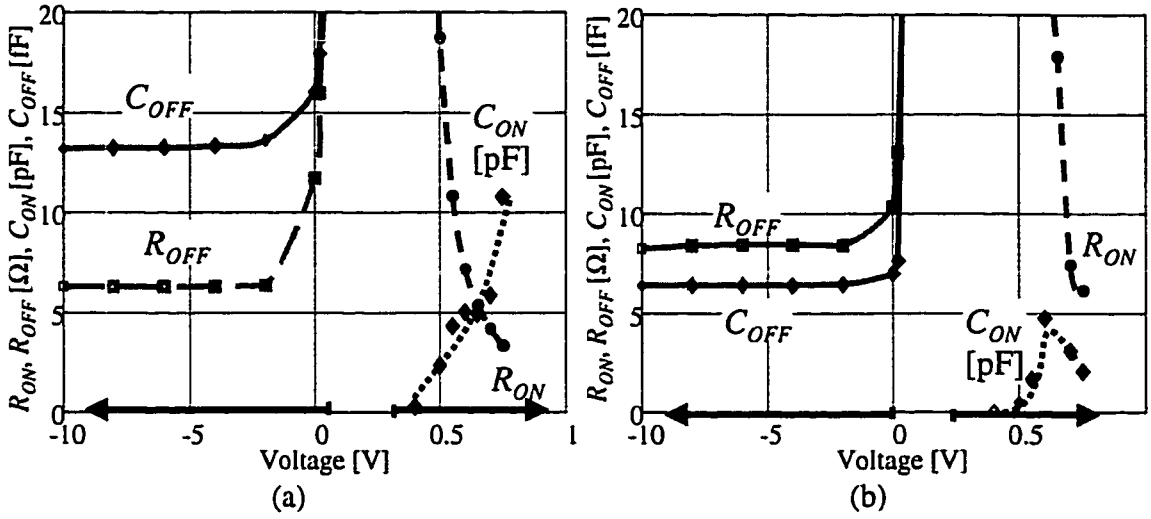


Figure 3.27. Bias dependence of equivalent-circuit elements of a) *10μm*-diameter and b) *5μm*-diameter InGaAs PIN diodes

The *10μm*-diameter InGaAs PIN diode had a minimum R_{ON} of *2.8Ω* and a minimum C_{OFF} of *14.3fF*. The intrinsic capacitance C_D was calculated by multiplying the unit OFF-state capacitance (see Table 3.6) by the diode area $A=78\mu m^2$ and was *9.9fF*. This allowed evaluation of the parasitic capacitance, which was equal to *4.3fF*. The *5μm*-diameter InGaAs PIN diode had $R_{ON}=6.1\Omega$ and $C_{OFF}=6.4fF$. The intrinsic capacitance C_D was *2.5fF* and the parasitic capacitance was *3.9fF*. As expected a larger PIN demonstrated larger OFF-state capacitance (*10fF* vs. *2.5fF*) and smaller ON-state resistance (*2.8Ω* vs. *6.1Ω*), while the values of parasitic capacitance were comparable (*3.3fF* vs. *3.9fF*).

The OFF-state capacitance of InGaAs PIN diodes showed good agreement between extracted from measurements (*14.3fF* and *6.4fF*) and simulated values (*17.5* and *7.5fF*) for *10μm*- and *5μm*-diameter diodes, respectively. The slightly larger values for simulated capacitance are due to an overestimation of the parasitic capacitance (*7fF* vs. *4fF* for *10μm*-diameter PIN). The ON-state resistances extracted from the measurements (*2.9* and *6.1Ω*) were larger than predicated by simulations (*0.9* and *3.5Ω*) for *10μm*- and *5μm*-diameter diodes, respectively. Smaller values for simulated resistance can be explained by the presence of the additional parasitic contact resistance in the fabricated InGaAs PIN diodes ($\rho_C \sim 1\times10^{-6}\Omega cm^2$).

The switching cutoff frequency figure-of-merit f_{CS} were also evaluated for the fabricated diodes in order to evaluate the millimeter-wave potential of the developed InGaAs PIN diode MMIC technology. Extrinsic values of the equivalent-circuit elements R_{ON}, C_{OFF}, and R_{OFF} were employed for this purpose. InGaAs PIN diodes demonstrated extrinsic f_{CS} with high values of *~4THz*. It should be noted that the extraction of R_{OFF} was not very accurate and, thus, the quoted values are conservative estimates. High switching cutoff frequency of the InGaAs PIN diodes indicates their high potential for millimeter-wave switching applications.

The bias dependence of the switching characteristics of InGaAs PIN diodes measured at *30GHz* is shown in Figure 3.28. When the InGaAs PIN is in the OFF-state (V_D<*0.4V*), the I-layer is depleted and the signal is blocked off by the OFF-state capacitance C_{OFF}. When the diode is biased in the ON-state (V_D>*0.5V*), the I-layer is filled with carriers and the signal is conducted through the ON-state resistance R_{ON}.

Transition between the ON- and OFF-states occurs within very small control bias variation (~0.2V) and different voltage scales in Figure 3.28 were used to allow better visualization. These low values of ON-state bias indicate reduced DC power consumption and control bias supply requirements of InGaAs PIN diodes when compared with GaAs PINs [60].

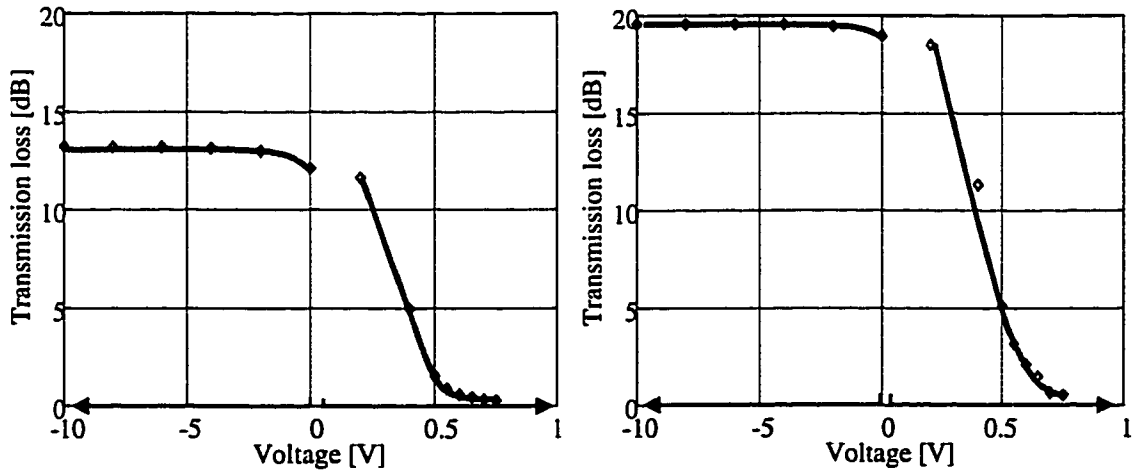


Figure 3.28. Measured bias-dependence of switching characteristics of InGaAs PINs for a) *10μm*-diameter and b) *5μm*-diameter diodes

Finally, the value of parasitic airbridge inductance was also evaluated from the frequency dependence of the S_{21}^{ON}-parameter of the InGaAs PIN diode SPST switch with

a 5μm-diode as shown in Figure 3.29. Thus, an *8μm*-wide and *35μm*-long airbridge had L_{AB} of *~30pH.*

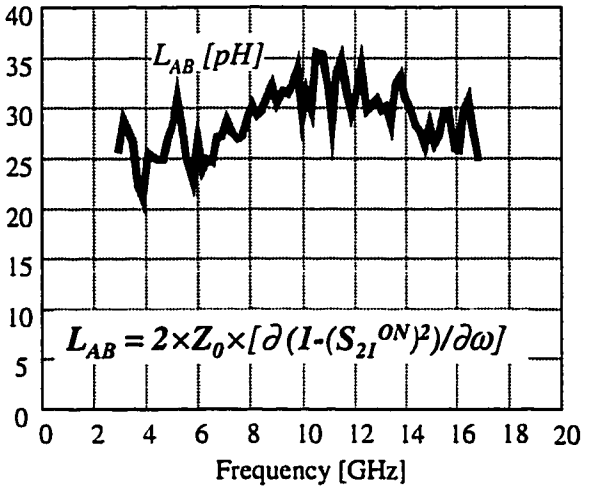


Figure 3.29. Evaluation of airbridge inductance from measured S-parameters

3.5. Conclusions

Design and operation of millimeter-wave switches were considered and related to the high-frequency characteristics of PIN diodes. Numerical simulations of InGaAs PIN diodes were used to investigate high-frequency characteristics of InGaAs PIN diodes and to optimize InGaAs PIN diode designs in respect to the application frequency. A W-band InGaAs PIN design employed *1μm*-thick I-layer and had a diameter of *10μm.*

Millimeter-wave MMIC process technology for InP-based InGaAs PIN diodes was presented. InGaAs PIN diodes layers grown by MOCVD and MBE epitaxial techniques showed good device characteristics. The diodes were fabricated using wet etching and lift-off metalization techniques. Low-parasitics airbridges were used for connecting the diodes with the rest of the circuit. Ka-band single-pole single-throw (SPST) InGaAs PIN switches were fabricated using coplanar-waveguide technology.

Low-frequency analysis techniques were employed for characterization of InGaAs PIN layers and the fabrication process. A correlation between the I-layer background concentration, ideality factor, and reverse leakage current was established. A mechanism of reverse breakdown in InGaAs PIN diodes under study was identified and a breakdown field F_B of *180KV/cm* was evaluated for *nid* InGaAs. Measured low-frequency C-V

characteristics were in excellent agreement with simulations, and were used for calculations of the I-layer doping profiles.

Small-signal S-parameters of series SPST InGaAs PIN switches were measured and demonstrated good switching characteristics with insertion loss of *0.5dB* and isolation of *19dB* for frequencies up to *40GHz*. S-parameters of discrete InGaAs PIN diodes were extracted from the switch characteristics using a specially developed technique. Small-signal equivalent circuit elements of InGaAs PIN diodes were calculated from the discrete device S-parameters and showed good agreement with the simulated values.

CHAPTER 4
InP-BASED PIN DIODE SIGNAL-CONTROL MMICs FOR W-BAND APPLICATIONS

The family of signal-control circuits includes switches, phase-shifters, limiters, and attenuators. This chapter concentrates mainly on applications of switching InP-based PIN diodes for monolithic millimeter-wave switches. Classification of microwave switches and basics of millimeter-wave switch design are introduced in Section 4.1. Generally, PIN diode switches employ one or several series or shunt PIN diodes as the switching elements. Discussion in this chapter is limited to design of shunt InGaAs PIN diode switches as applicable to W-band signal-control MMICs. Basic characteristics of W-band InGaAs PIN diode SPST switches are presented in Section 4.2.

Design, realization, and characterization of microstrip SPST InGaAs/InP PIN diode switches are described in Sections 4.3. These circuits required development of low-parasitics backside-via technology on InP. W-band InGaAs PIN diode SPDT transceiver switches made using novel coplanar-waveguide technology are presented in Section 4.4. InGaAs PIN diodes were also employed for design and realization of W-band MMIC phase-shifters and the results are included in Section 4.5.

4.1. Semiconductor Microwave and Millimeter-Wave Switches

The family of amplitude and phase-controlled circuits includes switches, current-limiters, phase-shifters, and attenuators. The switches are classified by the number of poles and throws. Most millimeter-wave switches are designed in single-pole single-throw (*SPST*), *SP2T*, and sometimes in *SP3T* configurations because of the growing problem of parasitics at high-frequency operation. The *SP2T* or *SPDT* switch is also called a transceiver switch and is often employed in transmitter-receiver applications to

change the signal path between reception and transmission configurations. Automotive radar systems also employ steering-beam switches, such as *SP3T*, to scan multiple antennas in the front of the car. However, functionality of *SPDT* or *SP3T* switches is determined by switching characteristics of component *SPST* switch arms. Thus, development of high-performance *SPST* switches is essential for successful realization of multi-throw transceiver and steering-beam switches.

PIN diode switches can be designed to use series or shunt PIN diodes as the switching elements. For applications operating from DC to low microwave frequencies, series PIN switches offer higher isolation than shunt PIN switches. However, the isolation of the series switch is greatly reduced at higher frequency because of increased signal leakage through the combination of the OFF-state depletion and parasitic capacitance of the diode. On the other hand, the isolation of the shunt switch is determined by its *ON*-state resistance and parasitic inductance, thus, it is not degraded as much at higher frequency. This difference in operation capabilities of series and shunt SPST PIN switches is illustrated in Figure 4.1.

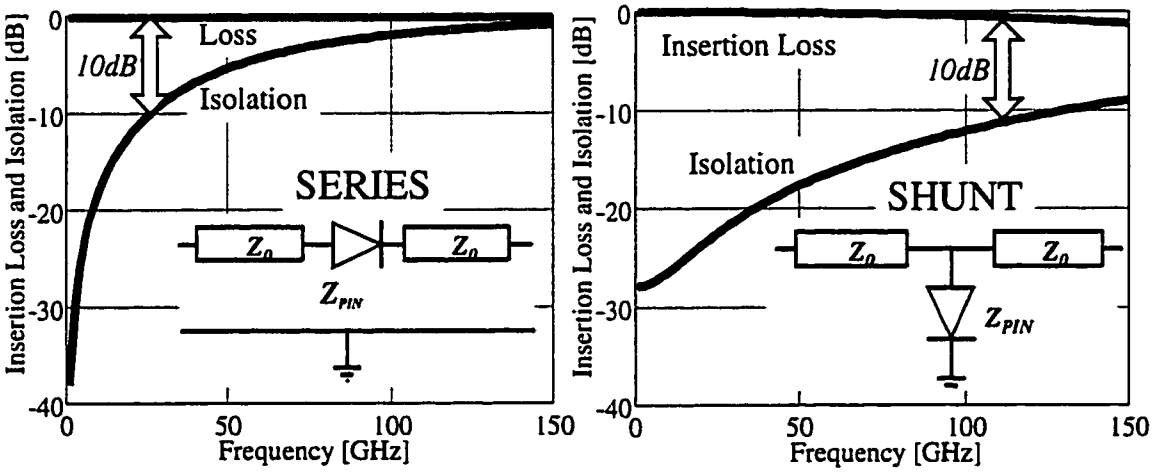


Figure 4.1. Performance of the series and shunt PIN diode switches

The frequency dependence of the isolation and the insertion loss is shown for series and shunt connection of a typical switching PIN diode (R_{ON}=*1Ω*, R_{OFF}=*1Ω*, C_{OFF}=*20fF*, and L_{AB}=*10pH*) with a *50-Ω* transmission line. The difference between transmitted and isolated signal decreases with frequency and a *10-dB* separation between insertion loss and isolation occurs at *~25 GHz* and *~120GHz* for series and shunt

switches, respectively. This difference exists because the effect of the high-frequency capacitive leakage is more pronounced in series switches where it is added to the small isolated signal, while in shunt switches it is deducted from the large transmitted signal. Consequently, most millimeter-wave PIN switches are designed to use PIN diodes connected in shunt.

The development of InP-based PIN diode switches achieved in the course of this work is illustrated in Figure 4.2. First, high-frequency characterization of monolithic InGaAs PIN diodes implemented using coplanar and microstrip technology revealed their good switching characteristics at millimeter-wave frequencies (insertion loss of *~1dB* and isolation of *~20dB* for up to *40GHz*). Next, W-band InGaAs PIN SPST switches were designed and fabricated using low-parasitics InP-based microstrip technology and demonstrated low insertion loss of *1.3dB* and high isolation of *25dB*. A high-performance *94-GHz* microstrip SPST switch was also demonstrated using two shunt InGaAs PIN diodes in the signal path for improved isolation (*>35dB*). Finally, low-parasitics coplanar InGaAs PIN MMIC technology (PIN-CPW) was developed and applied to develop W-band InP-based PIN transceiver (SPDT) switches with low loss of *1.1dB* and record isolation of *43dB* at *77GHz* and *94GHz*.

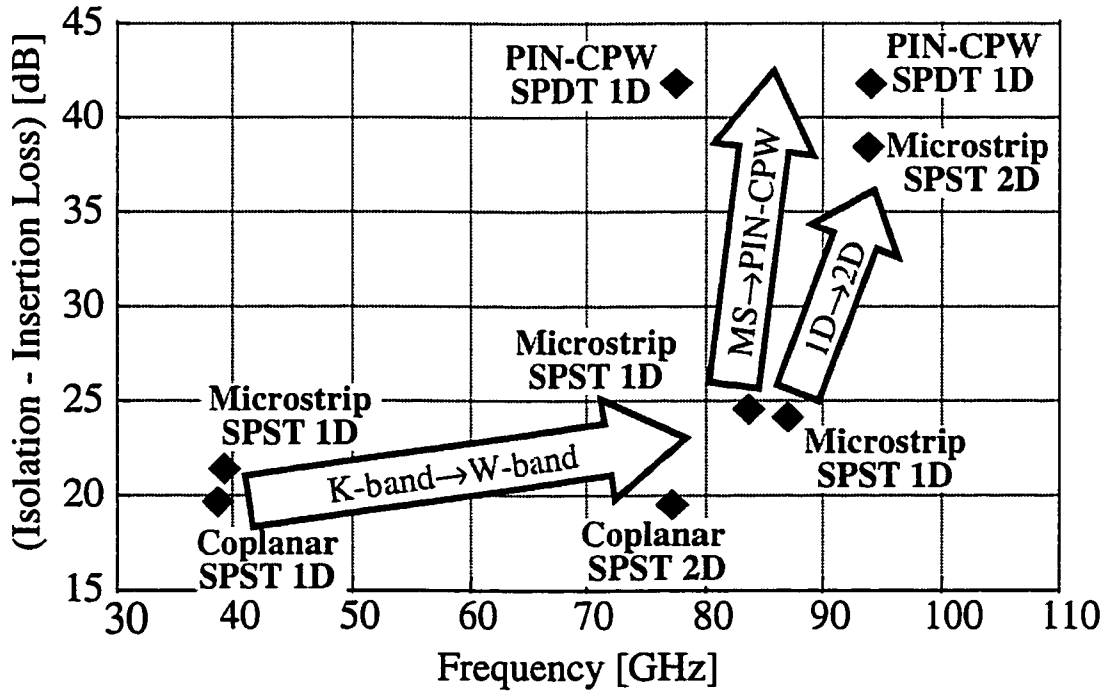


Figure 4.2. Flow-chart highlighting development of InP-based PIN diode switches

4.2. Design of W-band InGaAs PIN Diode SPST Switches

A schematic of a W-band shunt PIN diode SPST switch is shown in Figure 4.3. The switch consists of a transmission line with characteristic impedance Z_0 shunted in the middle by the InGaAs PIN diode. The length of the two transmission-line sections L is selected to correspond to a quarter-wavelength at the design frequency inserted in order to improve switch performance as explained next. On the outside, the switch is connected to the load impedance of the testing ports Z_L=50Ω.

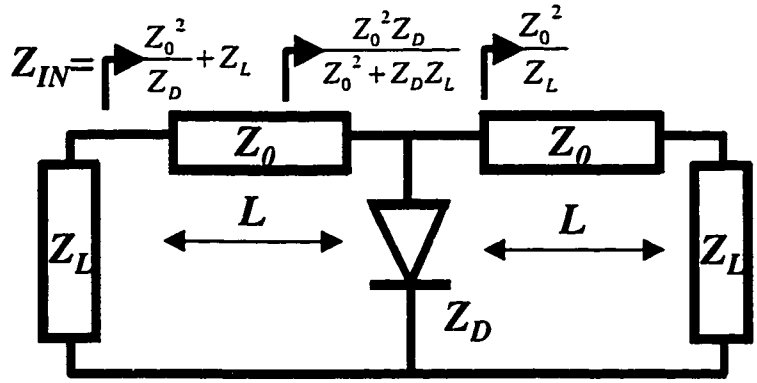


Figure 4.3. Schematic of a W-band shunt PIN diode SPST switch

The operation of the switch can be understood by treating the diode as an impedance block Z_D. The input impedance of the switch Z_{IN} is equal to Z_0^2/Z_D+Z_L (after taking into account impedance transformation by the quarter-wavelength section). In the *ON*-state, the PIN impedance Z_D^{ON} is much smaller than the characteristic impedance Z_0. Thus, the *ON*-state input impedance $Z_{IN}^{ON} \approx Z_0^2/Z_D^{ON}$ is much greater than Z_L, causing the input signal to be reflected from the input port. Only a small portion of the input signal is transmitted to the output. A ratio of this small output signal to the signal transmitted in the absence of the diode is called isolation and is measured by the S_{21}-parameter of the switch when the PIN diode is in the *ON*-state. The *ON*-state S_{11}-parameter measures the reflection loss of the switch.

Transmission of the signal through the SPST takes place when the PIN diode is in the high-impedance *OFF*-state. In this case, Z_D^{OFF} is transformed by a quarter-wavelength section into $Z_{IN}^{OFF} \approx Z_L$, which provides matching to the input port. Thus, most of the input signal is injected into the switch and transmitted to the output port. The insertion

loss is caused by mismatch at the input port and is characterized by the *OFF*-state S_{21}-parameter. The *OFF*-state S_{11}-parameter is called the return loss and provides a measure of its matching with the outside impedance $Z_L=50\Omega$.

The frequency dependence of isolation, insertion, return, and reflection losses of the SPST switches of Figure 4.3 can be calculated using the *ABCD* transmission matrix [61]. The *ABCD* matrix of a W-band InGaAs PIN SPST switch was found by multiplication of the *ABCD* matrices of the quarter-wavelength sections and the shunt-mounted PIN diode:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{SPST} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Z_0,L} \times \begin{bmatrix} 1 & 0 \\ Y_D & 1 \end{bmatrix} \times \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Z_0,L} \tag{4.1}$$

where the *ABCD* matrix of the quarter-wavelength section was given by

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Z_0,L} = \frac{1}{\sqrt{1-\tanh(j\beta L)^2}} \begin{bmatrix} 1 & Z_0 \tanh(j\beta L) \\ Y_0 \tanh(j\beta L) & 1 \end{bmatrix} \tag{4.2}$$

and β was the propagation constant of the transmission line. The scattering parameters of the switch were found using expressions (4.3) and (4.4):

$$S_{11} = \frac{\frac{B}{Z_L} - C \times Z_L}{A + \frac{B}{Z_L} + C \times Z_L + D} \tag{4.3}$$

$$S_{21} = \frac{2}{A + \frac{B}{Z_L} + C \times Z_L + D} \tag{4.4}$$

The dependence of the W-band InGaAs PIN diode SPST switch performance on the switch design, frequency, and PIN diode parameters was studied using equations (4.1)-(4.4).

The *ON* and *OFF*-state impedance of the InGaAs PIN diodes were calculated using equivalent circuits of Figure 4.4, which included the ON-state capacitance for improved accuracy at W-band frequencies.

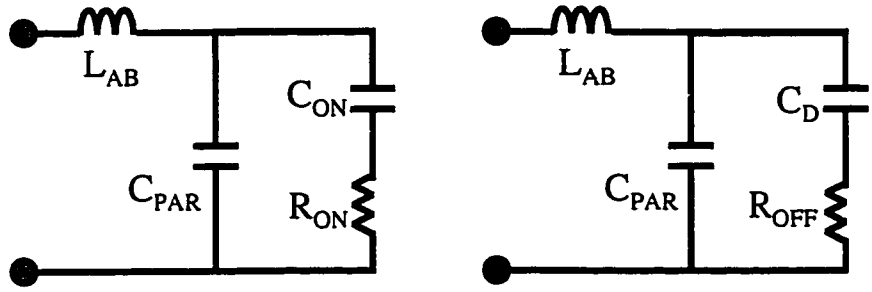


Figure 4.4. InGaAs PIN diode equivalent circuit in ON- and OFF-state

Equivalent-circuit elements for *5μm*- and *10μm*-diameter InGaAs PIN diodes used for design of W-band switches in this work are listed in Table 4.1. Their values were predicted by numerical simulations and showed excellent agreement with the values obtained by extraction from measured S-parameters as described in Chapter 3.

Table 4.1. W-band equivalent-circuit elements of InGaAs PIN diodes

PIN Diameter [μm]	R_{ON} *[Ω]*	C_{ON} *[pF]*	R_{OFF} *[Ω]*	C_D *[fF]*	C_{PAR} *[fF]*
5	*5*	*3*	*20*	*3*	*4*
10	*3*	*13*	*8*	*10*	*5*

For the purpose of this computation, an airbridge inductance with a typical for MMIC technology value of *10pH* was used. The switch employed two quarter-wavelength transmission-line sections with characteristic impedance of *95Ω*. The propagation constant of the transmission line

$$\beta = \omega \times \sigma / c \tag{4.5}$$

where ω is the radian frequency, σ is the effective dielectric constant of the transmission line, and c is the speed of light was determined from a given characteristic impedance Z_0 using relationship

$$\sigma = Z_{VAC}/Z_0 \tag{4.6}$$

where $Z_{VAC}=377\Omega$ is the characteristic impedance of free space [62]. The transmission lines were assumed lossless. The length of transmission-line sections was *140μm*, which resulted in the frequency of operation $f_0 = c/(2\pi \times L \times \sigma)$ of *87GHz*.

Performance of this W-band InGaAs PIN diode SPST switch as a function of frequency was calculated using equations (4.1)-(4.4) and the results are shown in Figure

4.5. The switch manifests a high isolation of *22dB* and a small reflection loss of *~0.4dB* for all frequencies between *70* and *100GHz*. The minimal insertion loss of *0.2dB* and maximal return loss of *35dB* are observed as expected at the design frequency of *87GHz*.

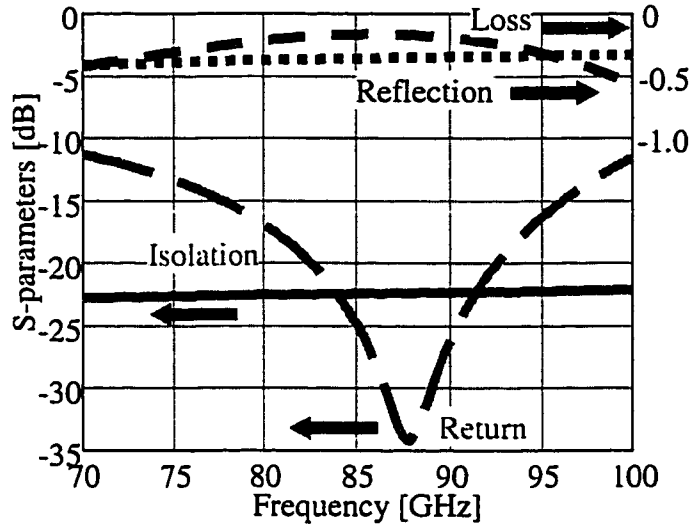


Figure 4.5. Calculated performance of a W-band InGaAs shunt PIN SPST

The design of W-band InGaAs PIN diode SPST switches was optimized by monitoring the performance of the switches at the design frequency while varying the key design parameters of the switch: the length L and the characteristic impedance Z_0.

Thus, to optimize a W-band InGaAs PIN diode SPST switch for automotive applications, the calculation frequency was fixed at *77GHz*, Z_0 was fixed at *95Ω*, and L was varied between *50* and *250μm*. The results are shown on the left graph of Figure 4.6. While the isolation and the reflection loss of the switch steadily improved as L increased from *50* to *250μm*, the return loss and the insertion loss at *77GHz* were optimized when L was *165μm*. Analogous design technique was used to optimize detailed layouts of practical W-band InGaAs PIN diode switches later in the project.

A valuable insight into the W-band PIN switch performance tradeoffs was obtained by investigating the influence of the characteristic impedance of the quarter-wavelength sections Z_0 while adjusting the length of the quarter-wavelength sections L to maintain matched operation at *87GHz*. The results demonstrated that increasing Z_0 from *30Ω* to *100Ω* leads to a *15dB* improvement of isolation and a *1.5dB* improvement of reflection loss as shown in the right graph of Figure 4.6. The insertion loss improved

from *0.8* to *0.2dB* when the characteristic impedance was increased from *30* to *70Ω*, but was slightly increased to *0.3dB* for Z_0=*100Ω*. The optimal return loss of better than *35dB* occurred for Z_0=*85Ω*.

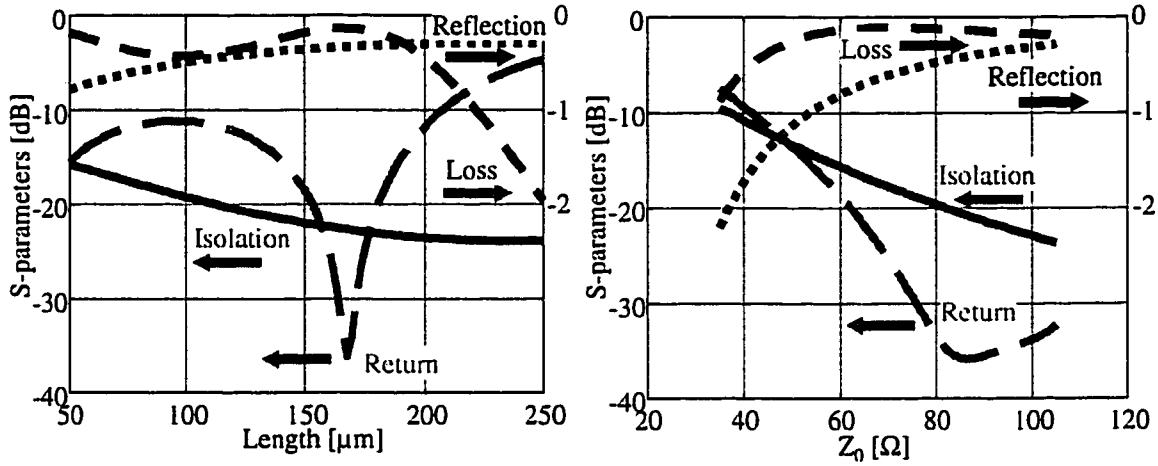


Figure 4.6. Optimization of W-band InGaAs PIN diode SPST design.

Performance improvement for W-band PIN diode switches with high characteristic impedance Z_0 can be explained in terms of the *ON*-state input impedance $Z_{IN}^{ON} \approx Z_0^2 / Z_D^{ON}$. When Z_0 was increased, the difference between Z_{IN}^{ON} and the outside impedance Z_L was enhanced resulting in larger reflection coefficient, and thus, higher isolation and reduced reflection loss.

It should be noted that the performed calculations did not account for increased losses associated with high-impedance transmission lines. Nevertheless, the advantages of employing high-impedance transmission lines in W-band PIN diode SPST switches were expected to outweigh increased transmission-line losses. Consequently, practical monolithic InGaAs PIN diode switches were designed using transmission lines with high characteristic impedance varying between *80* and *95Ω*.

4.3. Microstrip InGaAs PIN Diode Switches

Traditionally, most research and development work on monolithic microwave switches concentrated on GaAs-based microstrip PIN diode switches [63, 64]. However, InP-based InGaAs PIN diodes offer compatibility with high-speed InP-based HEMTs desired for automotive applications operating at *77GHz* and especially the emerging

140GHz range. Moreover, InP-based InGaAs PIN diode SPDT switches operating at X-band showed improved performance compared with the GaAs implementation [65].

First results on the application of InGaAs PINs for millimeter-wave switching were obtained in the course of this work, and excellent switching characteristics up to *40GHz* were demonstrated as described in Chapter 3. This section presents further details on the development of InGaAs PIN diode MMICs for millimeter-wave switching applications and addresses their first monolithic application to W-band MMIC switches using InP-based microstrip technology.

4.3.1. Development of InP-based Microstrip Technology

Circuits with microstrip lines require backside processing in order to fabricate ground plane and backside via holes. A wet-etched InP backside via-hole technology was employed using a Ti masking technique specially developed for this purpose, which allowed control of the via-hole dimensions. Details of the InP via-hole process are presented in Figure 4.7.

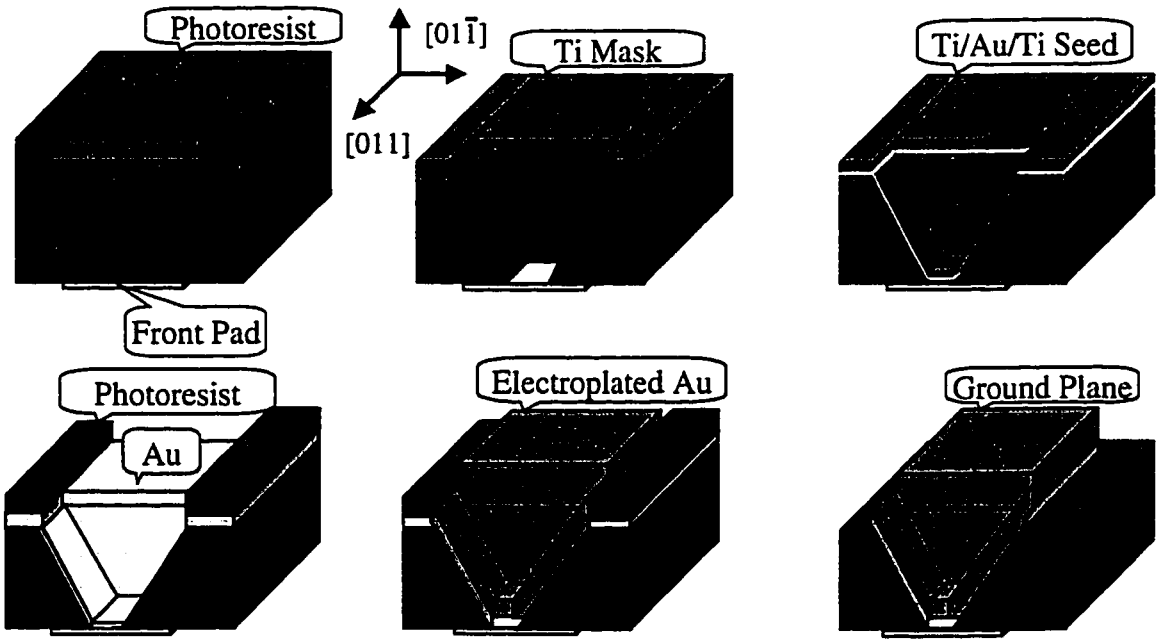


Figure 4.7. Step-by-step depiction of InP backside via-hole technology

After the front-side processing was completed, the wafer was mounted on a glass slide with the front side down. A lapper was used to thin the wafer to *100μm*. A thin layer

of *Ti* was evaporated on the backside surface to be used as a mask during the via-hole etch. *50μm×250μm* via-hole patterns were aligned to the front-side circuits using infrared illumination. The *Ti* metal was removed from the opened patterns, and the vias were etched using concentrated *HCl*. This anisotropic etchant produced vertical walls in $[011]$ and *45°*-sloped walls in $[01\bar{1}]$ crystal planes of InP wafer, which led to *50μm×50μm* openings on the front surface directly under the interconnect pads. The via-hole process was completed by electroplating the backside with a *10μm*-thick *Au* layer.

Two backside via holes were used to form a transition from a coplanar on-wafer test pad to a microwave transmission line. An InP-based microstrip "through" line was fabricated using four InP backside via holes as shown on the top left of Figure 4.8. The S-parameters of the InP microstrip "through" line were measured for frequencies between *2-40GHz* and *70-100GHz*. The measured S-parameters are shown by solid lines on the right graph of Figure 4.8. A resonance frequency of *70GHz* was determined by the length of the structure, which for this case were *500μm*.

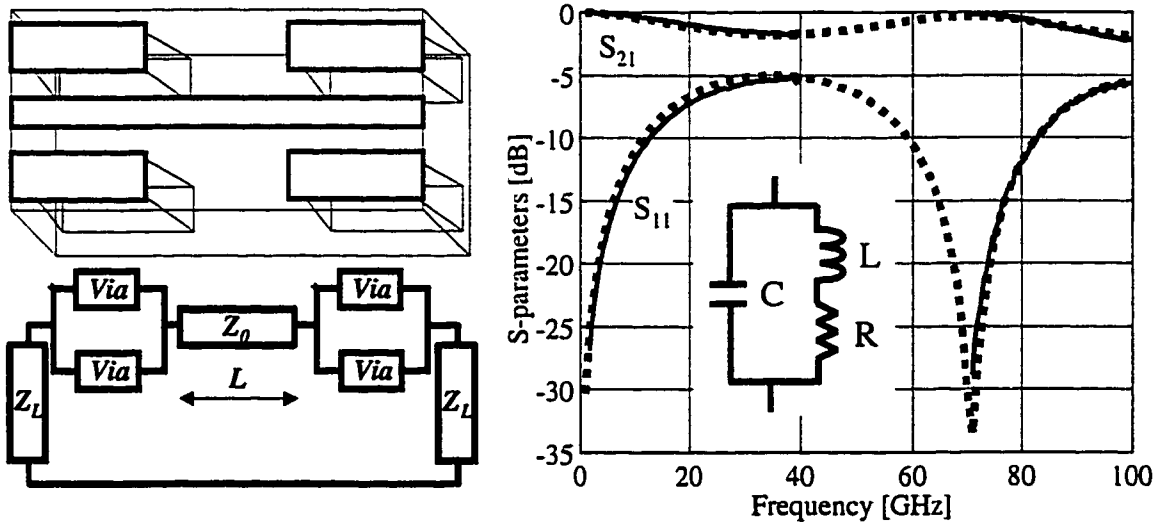


Figure 4.8. Schematics and S-parameters of the InP microstrip "through" lines: measured (solid lines) and calculated (dashed lines)

Electrical characteristics of the InP microstrip "through" line were modeled using an equivalent circuit shown on the bottom left of Figure 4.8. The via-hole equivalent circuit consisted of an inductance L_{VIA} and a resistance R_{VIA} shunted by a capacitance C_{VIA}. The S-parameters of the structure were calculated using its *ABCD* transmission matrix.

Calculated S-parameters are plotted on the right graph of Figure 4.8 with dashed lines. Good agreement between measured and calculated characteristics was observed for all combinations of via-hole equivalent-circuit parameters as long as they did not exceed their critical values: $L_{VIA} < 8pH$, $R_{VIA} < 0.2\Omega$, and $C_{VIA} < 10fF$. These maximum values were selected to represent InP backside via holes for the purpose of switch design.

4.3.2. Design of Microstrip PIN Diode Switches

W-band *SPST* switches employing InGaAs PIN diode as switching elements were designed using *HP EEsof* microwave simulator *Libra*. The microstrip technology was chosen because design libraries for distributed microstrip elements were readily available within the simulator.

In order to improve accuracy of the PIN diode equivalent circuit at high frequency it was extended to include short transmission line sections corresponding to interconnect lines. The airbridge inductance L_{AB} was replaced by a scalable model, which was developed using electromagnetic simulations by *HP EEsof Momentum* and verified by S-parameter characterization. Including transmission-line elements in the PIN diode model permits a more careful treatment of distributed effects, which become substantial at millimeter-wave frequencies [64].

The *Libra* schematic of a W-band SPST InGaAs PIN diode switch is shown in Figure 4.9. The switch consisted of two quarter-wavelength microstrip sections shunted in the middle by the InGaAs PIN diode. The quarter-wavelength sections connected the diode to the input and output $50\text{-}\Omega$ ports realized by coplanar-waveguide microwave-probe pads. High-impedance microstrip lines ($Z_O=95\Omega$) were employed in order to maximize the isolation of the switch.

A biasing network with a radial stub was also integrated on-chip. The radial stub acted as a low-pass filter ($f_{3dB}=40GHz$) and was used to isolate the low-frequency bias from the high-frequency signal.

Four backside vias on the edges of the circuit formed coplanar-to-microstrip transitions (two per transition) and one via in the middle of the circuit provided high- and low-frequency ground for the shunt PIN diode.

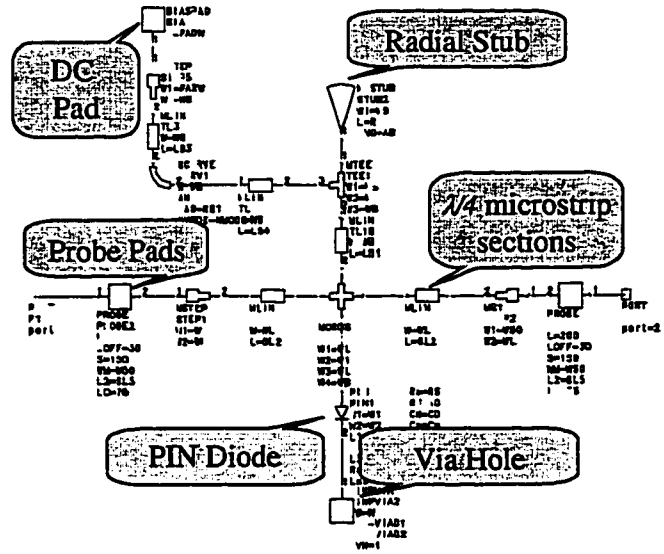


Figure 4.9. *Libra* schematics of a microstrip W-band SPST switch with a single shunt InGaAs PIN diode

The final step of the W-band InGaAs PIN SPST design process was optimization of the switch layout. The length and the characteristic impedance of all microstrip sections were varied, and the layout with the best combinations of high isolation and low insertion loss were selected. The simulated S-parameters of an optimized W-band InGaAs PIN diode SPST switch are shown in Figure 4.10. The *OFF*-state diode impedance Z_{OFF} was matched to the characteristic impedance Z_O at the frequency *83GHz*, where the minimum insertion loss of *0.9dB* was achieved. The isolation was better than *24dB* over the entire frequency range between *75GHz* and *90GHz*.

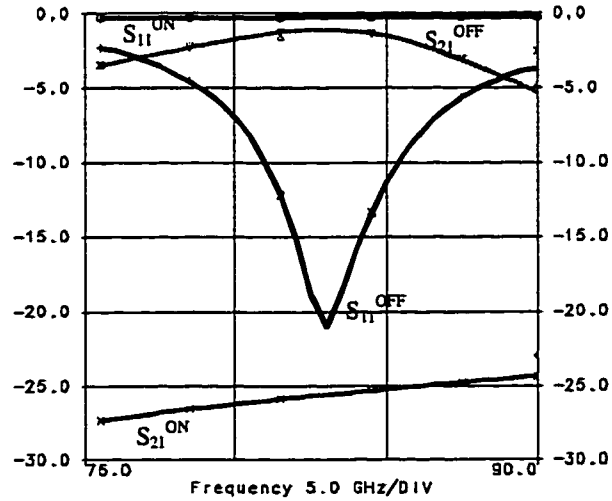


Figure 4.10. Simulated S-parameters of a W-band InGaAs PIN diode SPST

Once finalized, the layout of the switch was computer generated using custom layout scripts developed especially for InGaAs PIN MMICs and compatible with the compound-semiconductor fabrication technology at the University of Michigan. Fully scalable layout scripts were used for all passive and active (PIN diodes) components. In this manner, automatically generated layouts were immediately suitable for lithographic fabrication masks used in fabrication and allowed fast and painless modifications of circuit layouts for optimal performance.

The performance of SPST switches with different designs was evaluated in order to evaluate tradeoffs in the W-band InGaAs PIN diode switch design. The first switch employed a single shunt InGaAs PIN diode (single-diode design). The second switch used double-diode design with two shunt InGaAs PIN diodes (its schematic is shown in Figure 4.11) to improve isolation.

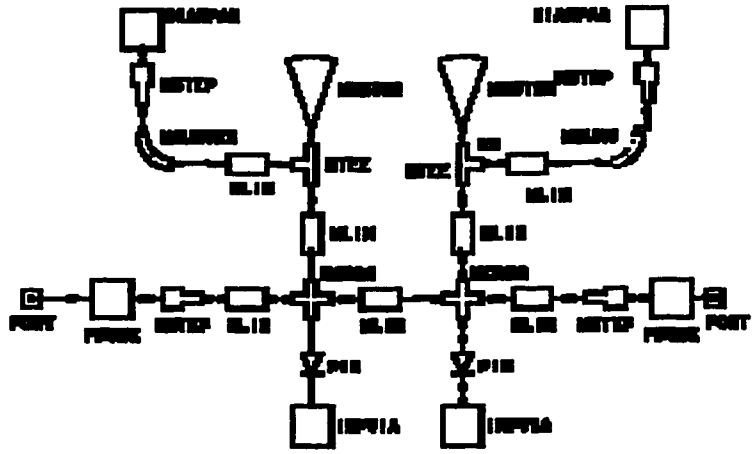


Figure 4.11. Schematic of a SPST with two shunt InGaAs PIN diodes

Single-diode and double-diode SPST switches were designed for operation at *94GHz* using *5μm*-diameter InGaAs PIN diodes. Their switching characteristics were calculated using the *ABCD*-matrix approach and the results are shown in Figure 4.12.

While the isolation of the single-diode switch was limited to *~22dB*, the calculations showed better than *40dB* isolation for a double-diode design. As expected, high-isolation properties of the double-diode design were accompanied by increased insertion loss.

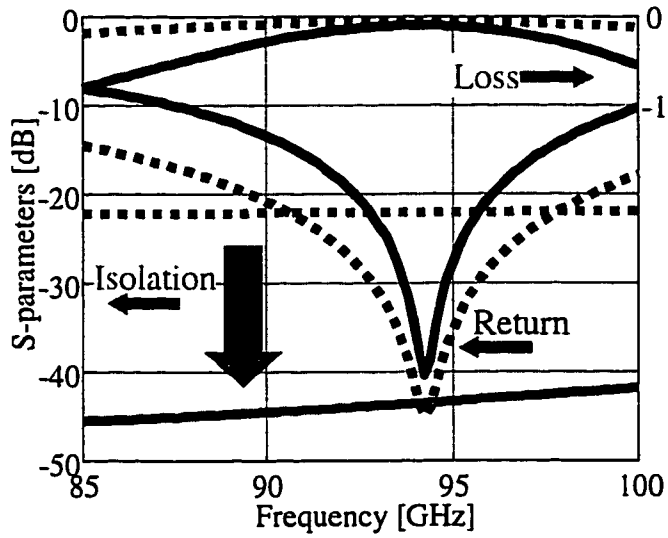


Figure 4.12. Comparison of single-diode (dashed) and double-diode (solid) *94GHz* InGaAs PIN SPST switches employing 5μm-diameter diodes

4.3.3. Characterization of Microstrip SPST Switches

Performance of microstrip InGaAs PIN diode switches was measured by on-wafer S-parameter characterization directly at W-band. The measurement were performed by the *HP8510B* network analyzer with a millimeter-wave option, *WR-10* waveguides, and *W-band* coplanar probes. The setup was capable of measuring on-wafer S-parameters between *70* and *105GHz*. On-wafer calibration was used to account for losses and phase delays in all components.

One of the fabricated and characterized W-band microstrip InGaAs PIN diode SPST switches is shown in Figure 4.13. This switch employed a single shunt *10μm*-diameter InGaAs PIN diode and operated at *83GHz*. It had two high-impedance (Z_O=*85Ω*) quarter-wavelength-long microstrip sections, which were connected to *50Ω* probe pads. Low-parasitics InP backside via holes were used to provide DC and RF ground. The backside via holes were aligned with the interconnect pads on the front side of the circuit as indicated in the photograph. A biasing network with a radial-stub was integrated on-chip.

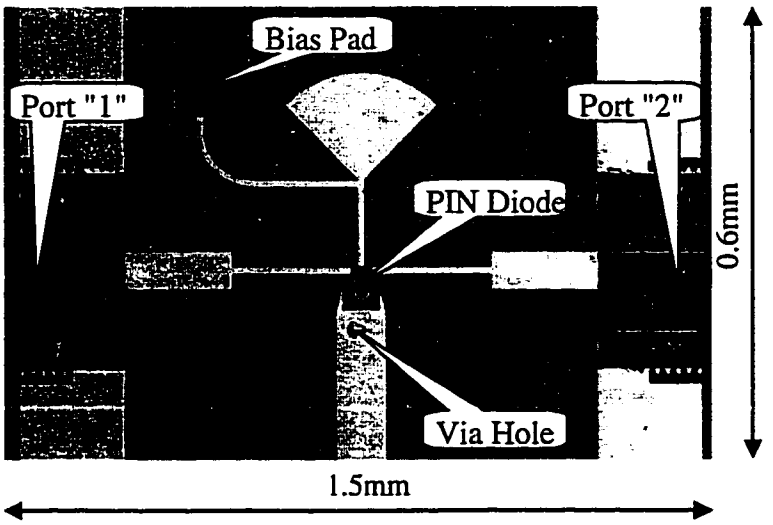


Figure 4.13. Photograph of an InGaAs PIN diode SPST switch

W-band S-parameters from on-wafer measurements of the switch in the *ON*-state (V_D=*0.65V*, I_D=*8mA*) and the *OFF*-state (V_D=*-5V*, I_D=*-2μA*) are shown in Figure 4.14. When the diode was in the *OFF*-state, its *OFF*-state impedance Z_{OFF} was comparable with Z_O. At the optimal frequency of *83GHz*, the input impedance of the switch matched the test port impedance Z_L=*50Ω* and the injected signal passed through the switch with only a small loss of *1.3dB*. The voltage standing-wave ratio (*VSWR*) under matched conditions had a low value of *1.12*. When the diode was turned on, its *ON*-state impedance Z_{ON} was much smaller than Z_O and was transformed into high impedance at the input port. The input signal was reflected back and only a small portion of the signal leaked to the output port (high isolation of *25dB* at *83GHz*).

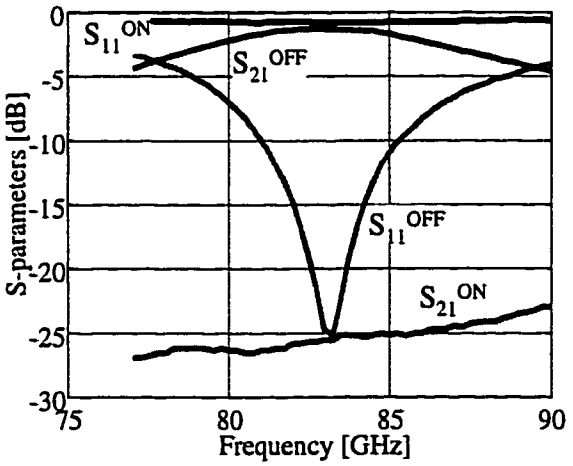


Figure 4.14. Measured S-parameters of W-band InGaAs PIN SPST switch

Microstrip W-band InGaAs PIN diode SPST switches had biasing networks integrated on-chip. The biasing network was designed to allow low-frequency bias to be applied through the biasing pad to the PIN diode while preventing high-frequency signal leaking from the switch to the biasing pad. Proper operation of the biasing network was verified by measuring the switching characteristics while changing the termination impedance on the biasing pad between "capacitive" and "inductive" loads. The two cases corresponded to cases when the biasing pad was left "open" or was touched with a long and narrow DC probe tip, respectively. S-parameters of an *87GHz* InGaAs PIN SPST switch measured under these two different loading conditions are shown in Figure 4.15.

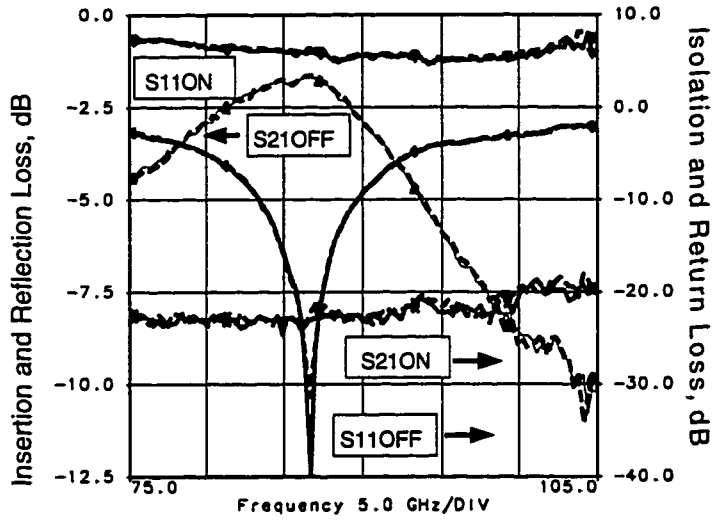


Figure 4.15. S-parameters of 87GHz InGaAs PIN diode SPST measured with the "capacitive" (solid) and "inductive" (dashed lines) loading of the biasing pad

This switch demonstrated *~22dB* of isolation and *~1.5dB* of insertion loss. A very good matching was demonstrated by this switch as indicated by minimum return loss of *–40dB* (a VSWR of *1.02*) at *87GHz*. No variations in the switching characteristics were detected when the biasing pad loading was varied between "capacitive" and "inductive".

W-band single-diode SPST switches with a single InGaAs PIN diode had high isolation of *22-25dB* in good agreement with predicted performance. Employing a double-diode SPST design with two InGaAs PIN diodes was expected to improve isolation at the expense of slightly increased insertion loss. A double-diode SPST switch employing two *5μm*-diameter InGaAs PIN diodes and designed to operate at *94GHz* was fabricated. A single-diode SPST switch was also fabricated using the same diode design

and identical dimensions of the microstrip quarter-wavelength sections. Photographs of the two switches are shown in Figure 4.16.

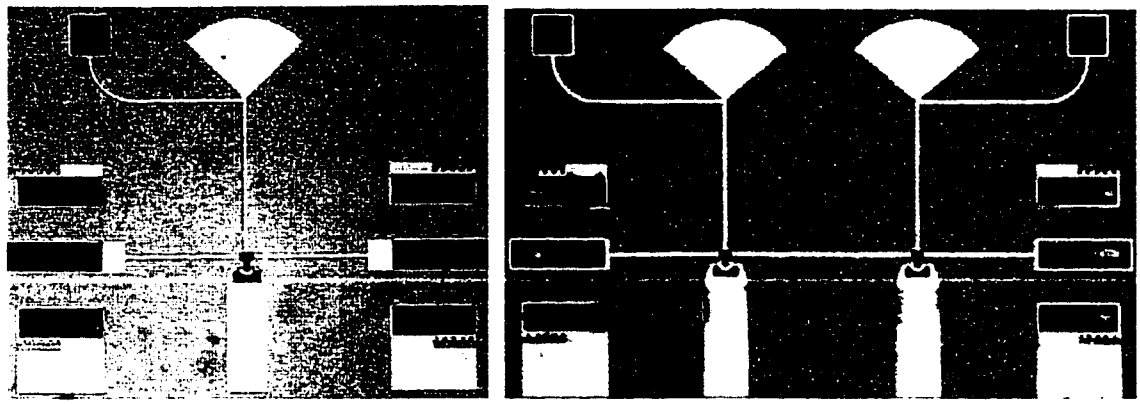


Figure 4.16. Photographs of the single-diode and double-diode InGaAs PIN diode SPST switches.

The second InGaAs PIN diode in the double-diode switch was placed at approximately half-wavelength distance from the first diode as shown in Figure 4.17. When the diodes were turned on, the low impedance $Z_0^2 Z_D/(Z_0^2 + Z_D Z_L)$ at the plane of the second diode was reduced to $Z_0^2 Z_D/(2Z_0^2 + Z_D Z_L)$ at the plane of the first diode. The input impedance Z_{IN} of the double-diode switch is then given by:

$$Z_{IN} = 2 \times Z_0^2 / Z_D + Z_L \tag{4.7}$$

The *ON*-state input impedance of the double-diode design $Z_{IN}^{ON} \approx 2 \times Z_0^2 / Z_D^{ON}$ is twice that of the single-diode design, which results in improved isolation for the double-diode switch since it causes larger mismatch at the input.

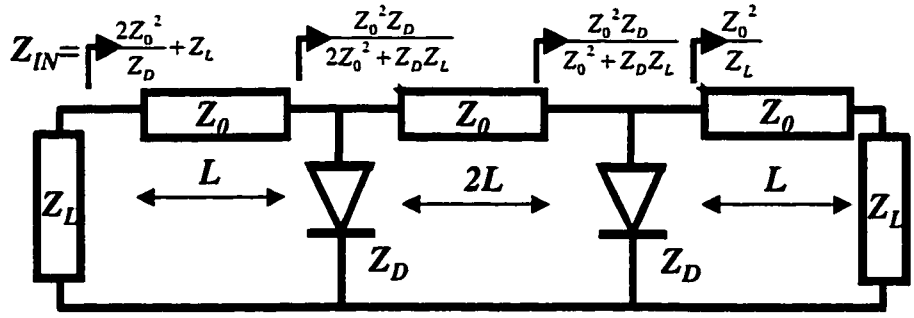


Figure 4.17. Schematic of double-diode PIN diode SPST switch.

Transmission of the signal through the double-diode SPST takes place when the PIN diode is in the high-impedance *OFF*-state. Then, Z_D^{OFF} transformed by a quarter-wavelength section into $Z_{IN}^{OFF} \approx Z_L$ provides matching to the input port, and most of the input signal is injected into the switch and transmitted to the output port. The insertion loss of the double-diode switch is slightly increased compared with the single-diode case due to transmission through two rather one diode. This feature is accounted for by equation (4.7), which includes a factor of *2* in front of the PIN-diode term.

W-band on-wafer S-parameter measurements showed that the single-diode *87GHz* SPST switch had a high isolation of *23dB*, and a low insertion loss of *1.3dB* (see the left graph of Figure 4.18). The double-diode SPST switch had an insertion loss of *2.2dB* at *93GHz*, while its isolation improved significantly and was greater than *35dB*, as shown on the right graph of Figure 4.18. As was expected from the theory, the isolation of the double-diode SPST switch was almost double the isolation of the single-diode switch. At the same time, an increase of the insertion loss was minimal due to the low ON-state resistance of the InGaAs PIN diodes of this work.

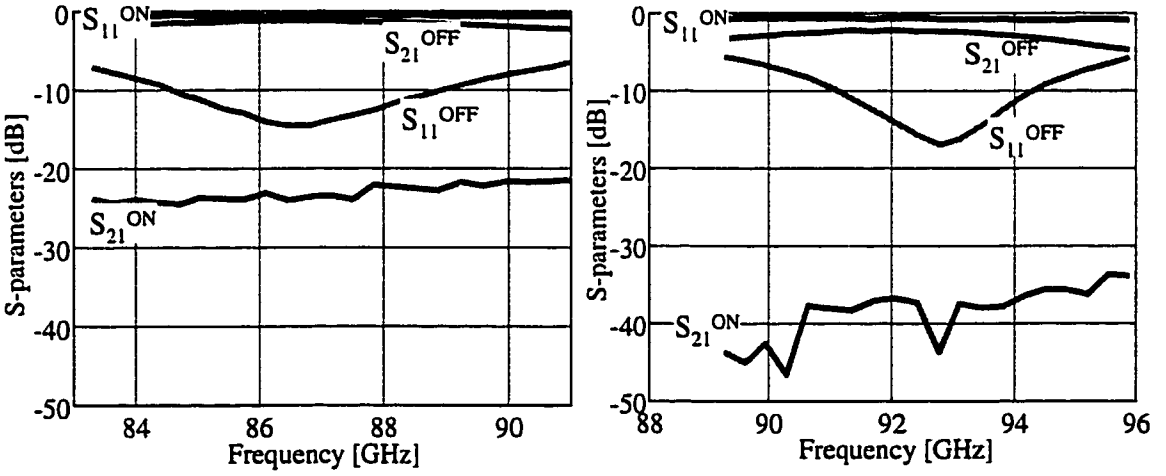


Figure 4.18. Performance of the (a) single- and (b) double-diode SPSTs

The dependence of the switching characteristics of the developed InGaAs PIN SPST switches on the bias voltage is shown in Figure 4.19. When the bias was less than the turn-on voltage of the InGaAs PIN diode V_{ON}=*0.4V*, the switch was transmitting. A minimal insertion loss of *1.2-1.3dB* per switch was achieved with a negative *OFF*-state bias greater than *-3V*. Further increasing the *OFF*-state bias (as far as the breakdown

voltage of InGaAs PIN V_{BD}=-20V) does not help to reduce the insertion loss, but allows improvement of power handling capabilities as will be discussed in Chapter 5.

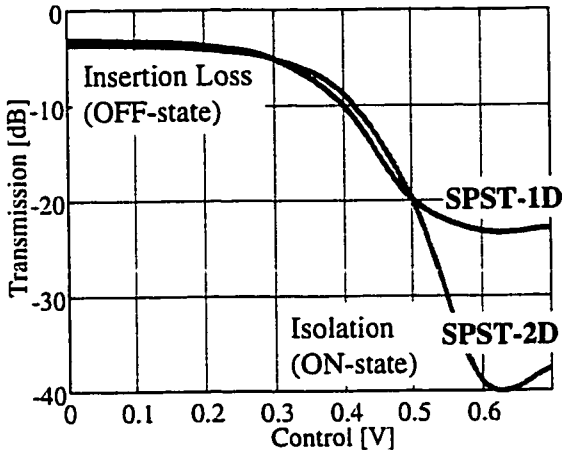


Figure 4.19. Dependence of the switching characteristics of InGaAs PIN diode SPST switches on the control bias voltage.

Signal transmission was turned off when the control bias exceeded *0.5V* and maximal isolation was achieved for an *ON*-state bias of *0.6-0.7V*. An application of a larger *ON*-state bias causes larger *ON*-state current, thus, results in significant increase of DC power consumption. Tradeoff between performance and DC power consumption of W-band InGaAs PIN switches is shown in Figure 4.20.

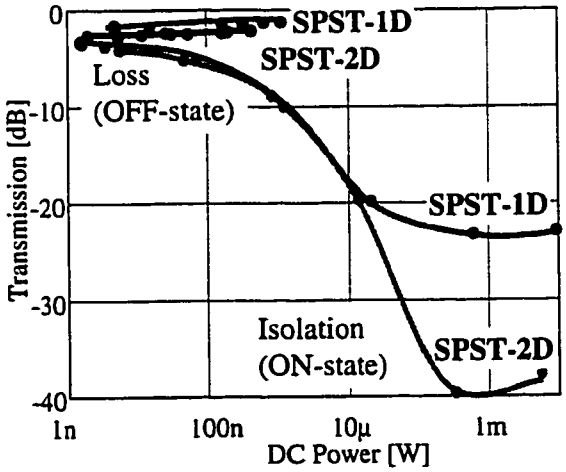


Figure 4.20. Tradeoff between DC power consumption and performance for W-band InGaAs PIN single-diode (SPST-1D) and double-diode (SPST-2D) SPST switches.

Both insertion loss and isolation of W-band InGaAs PIN diode SPST switches were improved when the diodes were biased harder, consuming more DC power. The *OFF*-state power consumption varied between *1nW* and *1μW* depending on the value of the *OFF*-state bias (*-1V* and *-10V*, respectively). Power consumption in the *ON*-state was much higher than in the *OFF*-state (*0.1-10mW*) due to high *ON*-state current of the PINs.

Nevertheless, excellent isolation of *25dB* for single-diode and *>35dB* for double-diode InGaAs PIN SPST switches was obtained at W-band frequencies with less than *1mW* of power consumption. This power consumption is five to ten times smaller than reported for state-of-the-art GaAs PIN switches [63].

Overall, record-breaking performance for W-band monolithic integrated SPST switches (isolation of *>35dB* and insertion loss of *1.3dB*) was realized using InGaAs PIN diodes with low DC power consumption (*<1mW*) and employing low-parasitics InP-based microstrip technology.

While the DC power consumption demonstrated by InP-based PIN diode switches is significantly higher than *~1μW* offered by micromechanical (or MEMs) switches [66], it is still only a small fraction of the total power consumed by a typical transceiver (*~100mW*). Moreover, MEMs require very high actuation voltages (*10-20V*) [66], incompatible with low-power electronics, while InP-based PIN diodes have very low turn-on voltages of *0.4V*.

4.4. Coplanar InGaAs PIN Diode Switches

Historically, most MMICs were developed using microstrip transmission-line technology. Coplanar-waveguide MMIC technology eliminates the need for backside via holes, which reduces fabrication complexity, and offers smaller parasitics, which leads to improved circuit performance. However, the application of coplanar MMIC technology to W-band circuits has been slowed by the lack of accurate models of coplanar-waveguide junctions and discontinuities.

Recent advances in electromagnetic simulators, such as *HP EEsof Momentum*, allowed fast and accurate computations of high-frequency S-parameters for arbitrary coplanar structures; and design libraries for coplanar elements were developed. Thus, in a

recent work, W-band coplanar GaAs PIN diode SP3T switches designed using the *method-of-moments* simulator to obtain S-parameters of coplanar discontinuities demonstrated *20dB* isolation at *77GHz* [67]. The GaAs PIN diode used in that work had a switching cutoff frequency of *1.6THz*. It was expected and proved by the results presented in this section that InGaAs PINs of this work having enhanced frequency capability of *4THz* would offer improved switching characteristics, combined with reduced power consumption and compatibility with InP-based high-frequency electronics.

A *method-of-moment* simulator was also used in this work to study the limitations of coplanar switch performance (as described in the next section) and to obtain scattering parameters of coplanar elements for which Libra models were not available, such as tee junctions and step discontinuities.

The key features of the *coplanar* InGaAs PIN diode switches compared with *microstrip* InGaAs PIN diode switches described in the previous section were elimination of backside vias and introduction of air-coplanar transitions for mounting of the PIN diodes. These innovations were expected to lead to reduced parasitics and, thus, improved performance for W-band InGaAs PIN diode switches.

4.4.1. Development of Low-Parasitics Coplanar PIN Diode MMICs

Coplanar-waveguide MMIC technology employed for fabrication of W-band InGaAs PIN diode switches used the same fabrication steps as the discrete InGaAs PIN diode technology described in Chapter 3. Both ground planes and signal line of a coplanar-waveguide were formed with the interconnecting metal. Airbridges connecting opposing ground planes were placed along long coplanar-waveguide sections and at their discontinuities to suppress any parasitic mode excitation as shown in Figure 4.21.

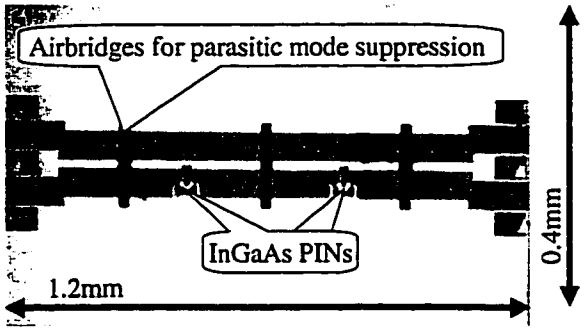


Figure 4.21. A photograph of coplanar W-band InGaAs PIN-diode SPST switch

Ka-band coplanar and microstrip InGaAs PIN diode SPST switches were fabricated using the same wafers, and their photographs are shown in Figure 4.22. The coplanar switch had an InGaAs PIN diode mounted in shunt, across one side of a coplanar waveguide, as shown in Figure 4.22. The microstrip switch had a PIN diode mounted in shunt with a microstrip line through a backside via hole.

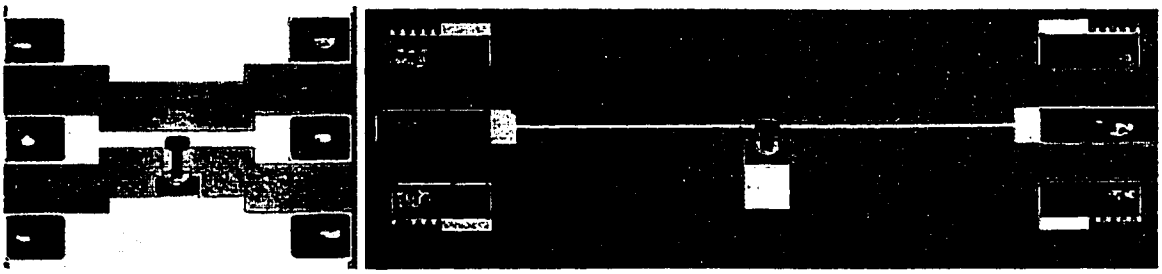


Figure 4.22. Coplanar and microstrip Ka-band switches employing shunt-mounted InGaAs PIN diodes.

Figure 4.23 shows the S-parameters of these switches measured by on-wafer characterization between *2* and *40GHz*. The coplanar switch demonstrated much smaller insertion loss (*0.1dB* vs. *1.1dB*) as well as larger bandwidth (*15GHz* vs. *8GHz* @ S_{11}^{OFF}=-*10dB*) when compared with the microstrip switch.

These improvements were attributed to smaller parasitics of the coplanar switch, made possible by elimination of backside via holes and reduced transmission-line losses of coplanar-waveguide sections. An insertion loss of a coplanar-to-microstrip transition L_{CPWMS}=*0.2dB* can be evaluated from the insertion losses of the microstrip SPST switches with one ($L_{SPST\text{-}1D}$) and two ($L_{SPST\text{-}2D}$) InGaAs PIN diodes described in Section 4.3.3:

$$L_{SPST-1D} = 2 \times L_{CPWMS} + L_{PIN} = 1.3dB$$
$$L_{SPST-2D} = 2 \times L_{CPWMS} + 2 \times L_{PIN} = 2.2dB \quad (4.8)$$
$$L_{CPWMS} = (2 \times L_{SPST-1D} - L_{SPST-2D})/2 = (2 \times 1.3 - 2.2)/2 = 0.2dB$$

Thus, the *1-dB* improvement of the insertion loss for the coplanar SPST switch comes from *0.4dB* due to elimination of the backside via holes while another *0.6dB* can be attributed to lower losses of coplanar-waveguide transmission lines.

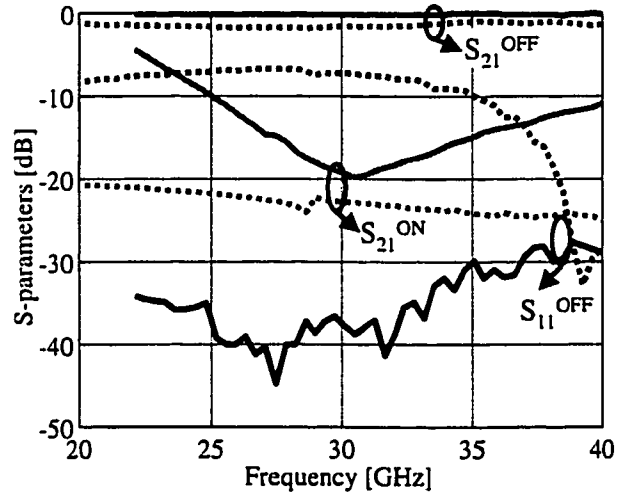


Figure 4.23. Measured characteristics of coplanar (solid lines) and microstrip (dotted lines) Ka-band InGaAs PIN diode SPST switches.

However, the isolation of the coplanar SPST switch was *~20dB*, making it comparable to that of the microstrip SPST switch. This modest value of isolation for coplanar SPST switches of this design was caused by asymmetric mounting of InGaAs PIN diodes (see Figure 4.22).

The transition between the PIN diode and coplanar waveguide had to be optimized in order to improve the switch isolation characteristics. Since microwave circuit simulator *HP EEsof Libra* modeled all transitions as ideal, a *method-of-moments* electromagnetic simulator (*HP EEsof Momentum*) was used to analyze characteristics of various PIN-CPW transitions. The simulator was used to obtain S-parameters of PIN-CPW transitions and to extract values of their corresponding parasitic inductance and capacitance.

Investigated designs included asymmetric-shunt, symmetric-shunt, and series transitions as shown in Figure 4.24. The parasitic inductance of the asymmetric-shunt, asymmetric-shunt, and series transitions were *96pH, 11pH*, and *3.6pH* respectively, while their parasitic capacitance remained constant at *~15fF*.

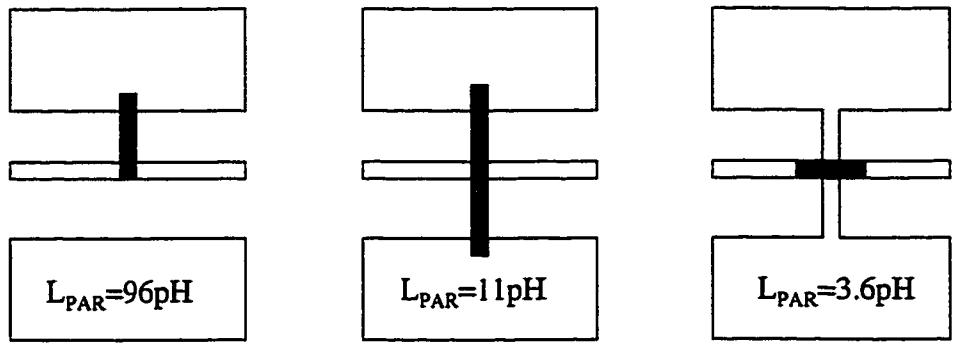


Figure 4.24. Schematics of investigated PIN-CPW transitions:
(a) asymmetric-shunt, (b) symmetric-shunt, and (c) series transition.

Reductions of parasitic inductance from *96* to *11pH* and from *11* to *3.6pH* corresponded to *20-dB* and *10-dB* increases of isolation for coplanar switches, designed using these respective PIN-CPW transitions.

Based on the results of this study, a low-inductance PIN-CPW transition was developed in order to improve switch isolation characteristics. A three-dimensional view and a photograph of the fabricated structure are shown in Figure 4.25.

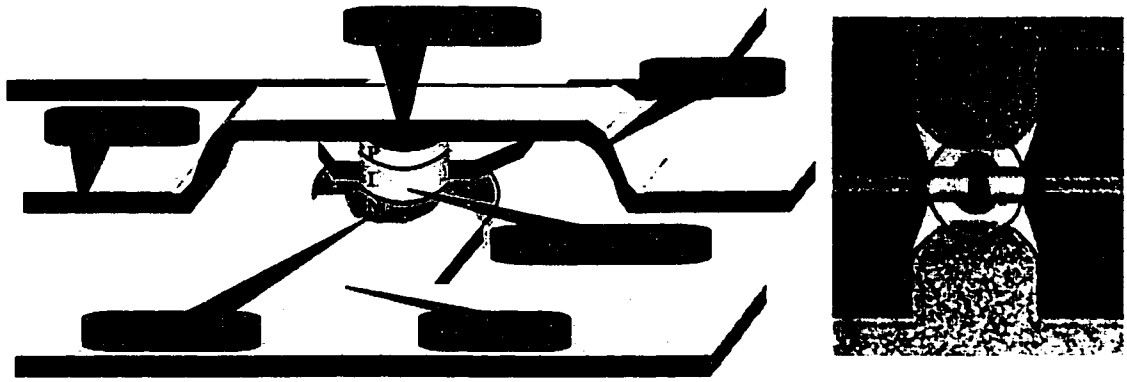


Figure 4.25. Design schematic and photograph of the developed low-inductance PIN-CPW transition

A high-impedance air-coplanar signal line was connected to the anode contact on the top of the PIN diode mesa while wide coplanar ground lines were used to access the cathode contacts on both sides of the mesa.

An equivalent circuit of the InGaAs PIN-CPW diode is shown in Figure 4.26. It consisted of an *OFF*-state capacitance $C_{OFF}=6fF$, *OFF*-state resistance $R_{OFF}=5\Omega$, the high-frequency *ON*-state capacitance $C_{ON}=8pF$, *ON*-state resistance $R_{ON}=2\Omega$, and the parasitic capacitance $C_{PAR}=5fF$.

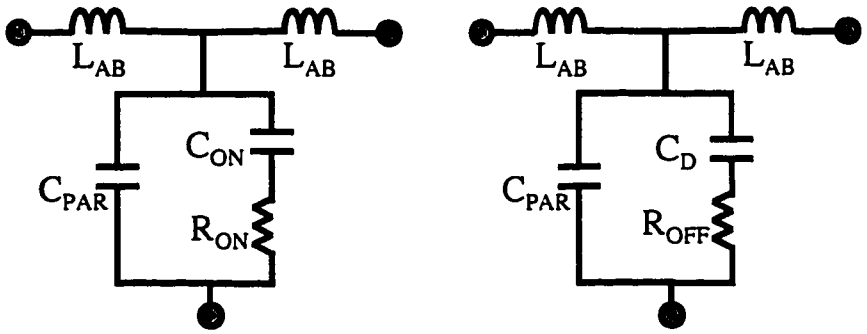


Figure 4.26. Equivalent circuit of an InGaAs PIN diode with a low-inductance PIN-CPW transition

The key feature of the PIN-CPW transition is that the airbridges were designed to function as two short sections of coplanar-waveguide transmission line. As shown by the results of Figure 4.24, such design of PIN-CPW transition allowed minimization of parasitic inductance from *11pH* to *4pH* and led to an *~10-dB* increase of isolation for coplanar PIN switches.

Overall, the development of optimized transitions from a coplanar-waveguide to a switching InGaAs PIN diode allowed low-parasitics shunt mounting of the diodes in coplanar monolithic circuits as necessary for high-performance millimeter-wave switching applications.

4.4.2. Design of Coplanar W-band SPDT PIN Diode Switches

Low-parasitics coplanar PIN MMIC technology was employed to design transmit-receive InGaAs PIN diode SPDT switches in order to improve their performance and reduce fabrication complexity. The schematic of a transmit-receive SPDT switch is shown in Figure 4.27. Its design contains two SPST switch arms. Each SPST arm

employs a shunt InGaAs PIN diode and two quarter-wavelength coplanar-waveguide sections with high characteristic impedance Z_0, as marked in Figure 4.27. The impedance of all three outside ports (Z_L) was 50Ω.

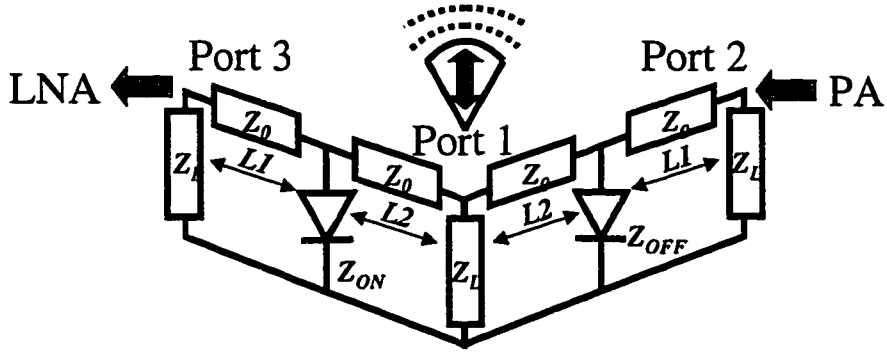


Figure 4.27. Schematic of InGaAs PIN diode SPDT switch

In practice, the switch is employed with the antenna feeding the input port (port "1") and a power amplifier (*PA*) and low-noise amplifier (*LNA*) connected to the output ports (ports "2" and "3", respectfully). The switch operates by either transmitting the signal from port "2" to port "1" or by receiving the signal from port "1" to port "3". During transmission, the InGaAs PIN of the SPST switch connecting ports "1" and "2" is turned off (the *OFF*-state SPST), and the InGaAs PIN of the SPST switch connecting ports "1" and "3" is turned on (the *ON*-state SPST). This case is shown in Figure 4.27. During reception, the bias is reversed, thus, one of the PIN diodes is always on and the other is always off.

The switching characteristics of the transceiver switch were calculated using *ABCD* transmission matrix method. First, input admittance of the detached SPST arms in the *ON*- and *OFF*-states was calculated from their respective *ABCD* matrices:

$$Y_{IN}^{ON/OFF} = \frac{C^{ON/OFF} \times Z_L + D^{ON/OFF}}{A^{ON/OFF} \times Z_L + B^{ON/OFF}} \tag{4.9}$$

Next, the transmission matrix of the SPDT switch was calculated along the SPST switch arm connecting ports "1" and "2" (SPST [1,2]), while substituting the other SPST between ports "1" and "3" (SPST [1,3]) with its input admittance Y_{IN}^{13} as shown in expression (4.10):

$$\underset{SPDT(1,2)}{\begin{bmatrix} A & B \\ C & D \end{bmatrix}} = \begin{bmatrix} 1 & 0 \\ Y_{IN}^{13} & 1 \end{bmatrix} \times \underset{Z_0,L2}{\begin{bmatrix} A & B \\ C & D \end{bmatrix}} \times \begin{bmatrix} 1 & 0 \\ Y_D & 1 \end{bmatrix} \times \underset{Z_0,L1}{\begin{bmatrix} A & B \\ C & D \end{bmatrix}} \tag{4.10}$$

When the SPST [1,2] is in the *OFF*-state and the SPST [1,3] is in the *ON*-state the S_{21}-parameter of the transmission matrix of (4.10) is used to calculate the insertion loss of the SPDT switch. The isolation of the SPDT switch is measured by the same S_{21}-parameter when the bias is reversed (i.e. SPST [1,2] is in the *ON*-state and the SPST [1,3] is in the *OFF*-state). Scattering parameters S_{11} and S_{22} provide information on input and output matching respectively. Output crosstalk is characterized by the S_{21}-parameter of transmission matrix between ports "2" and "3" set up as the following:

$$\underset{SPDT(2,3)}{\begin{bmatrix} A & B \\ C & D \end{bmatrix}} = \underset{Z_0,L1}{\begin{bmatrix} A & B \\ C & D \end{bmatrix}} \begin{bmatrix} 1 & 0 \\ Y_{ON} & 1 \end{bmatrix} \underset{Z_0,L2}{\begin{bmatrix} A & B \\ C & D \end{bmatrix}} \begin{bmatrix} 1 & 0 \\ Y_L & 1 \end{bmatrix} \underset{Z_0,L2}{\begin{bmatrix} A & B \\ C & D \end{bmatrix}} \begin{bmatrix} 1 & 0 \\ Y_{OFF} & 1 \end{bmatrix} \underset{Z_0,L1}{\begin{bmatrix} A & B \\ C & D \end{bmatrix}} \tag{4.11}$$

Switching characteristics of the InGaAs PIN diode SPDT switch of Figure 4.27 were calculated and the results are shown in Figure 4.28. The switch was designed for operation at *77GHz* and employed *8μm*-diameter InGaAs PIN-CPW diodes. Based on the results of the calculations, coplanar W-band InGaAs PIN diode SPDT switches were expected to demonstrate low insertion loss of *~1dB*, while their isolation and crosstalk were to improve to over *40dB*.

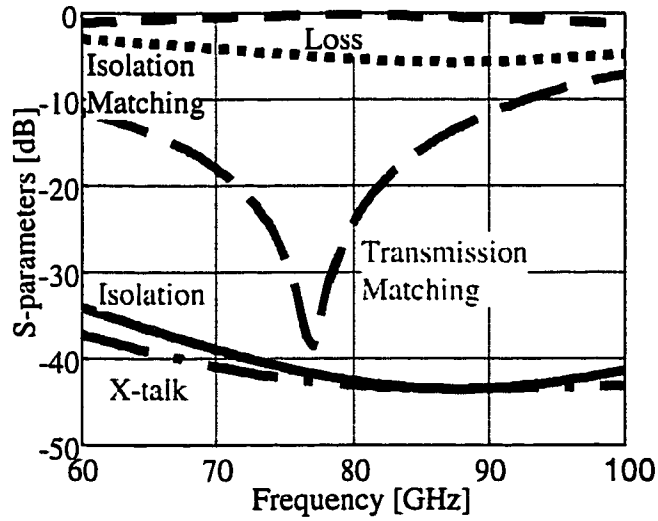


Figure 4.28. Calculated performance of an InGaAs PIN diode SPDT switch

It should be noted that an additional *6dB* of isolation is available in an SPDT compared with an SPST switch, since matched output is always available in the double-throw design. An absence of the matched output in an SPST switch leads to doubling of the voltage amplitude at the blocking *ON*-state PIN, which reduces maximum isolation by *6dB* compared with the SPDT case where a matched output is present [68].

Practical coplanar W-band InGaAs PIN diode switches were designed using the *HP EEsof* microwave simulator. Switches employed low-parasitics *8μm*-diameter InGaAs PIN-CPW diodes. Custom equivalent-circuits and layout-generating scripts were developed for coplanar-waveguide components and InGaAs PIN-CPW diodes and allowed automatic generation of fabrication-ready circuit layouts. An automatically generated fabrication-ready layout of a coplanar *77GHz* InGaAs PIN diode SPDT switch is shown in Figure 4.29.

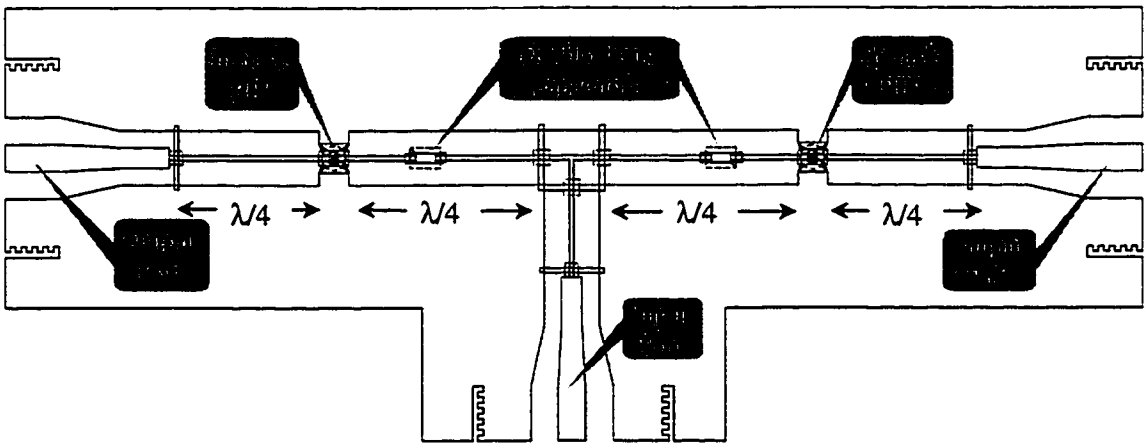


Figure 4.29. Layout of coplanar *77GHz* InGaAs PIN diode SPDT switch automatically generated by *HP EEsof Libra/Academy* simulator.

The switch consisted of one input and two output arms joined together with a coplanar-waveguide T-junction. The switch arm between the input and the active port had a PIN diode biased in the OFF-state, while the switch arm between the input and the isolated port had an ON-state diode. Independent biasing of the switch arms was made possible by inserting DC-blocking capacitors in series with the transmission lines.

The *HP EEsof Momentum* electromagnetic simulator was used to obtain S-parameters describing coplanar-waveguide discontinuities and T-junctions. Output arms were made of coplanar InGaAs PIN diode SPST switches with high-impedance coplanar

waveguides (Z_0). The characteristic impedance of the input arm was also selected to be Z_0 in order to improve symmetry of the power-divider properties of the T-junction.

To minimize possibilities of exciting parasitic high-frequency modes in the coplanar waveguides, the ground-to-ground spacing did not exceed *100μm* while the width of the ground planes was *225μm*. The minimum width of the signal line was limited to *8μm* by the fabrication requirements. Therefore, the maximum allowed characteristic impedance of coplanar waveguides was *84Ω* and this value was employed for switch design.

As mentioned ealier, two DC-blocking capacitors of *0.5pF* each were inserted between the diodes and the T-junction. The capacitors allowed independent biasing of the diodes and DC isolation of the input port. SPDT switches with complete on-chip biasing networks have also been designed, allowing independent biasing of the diodes and providing DC isolation for all three ports.

Design of coplanar-waveguide W-band InGaAs PIN diode transceiver switches was finalized by performing a thorough optimization of all waveguides, discontinuities, and blocking DC capacitors for best performance at the design frequency.

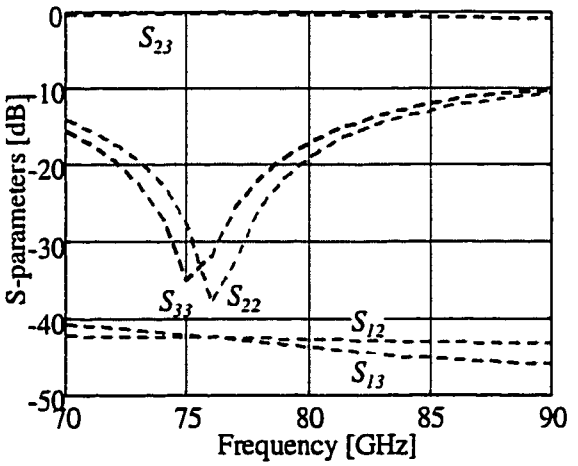


Figure 4.30. Simulated S-parameters of a coplanar SPDT switch designed for operation at *77GHz*

Simulated performance of a 77GHz coplanar InGaAs PIN diode SPDT switch is shown in Figure 4.30. The simulations predicted broadband performance with insertion loss of less than *1dB* and isolation in excess of *40dB* between *70* and *90GHz*. Input and output matching was better than *-20dB* over *5GHz* bandwidth. The improved

characteristics of the switch are due to reduced parasitics of the developed coplanar technology, such as the low inductance of PIN-CPW diodes and the absence of parasitic inductance of backside via holes.

Finally, designed coplanar W-band InGaAs PIN diode SPDT switches were fabricated at Daimler-Chrysler and characterized at the University of Michigan.

4.4.3. Characteristics of Coplanar W-band SPDT InGaAs PIN Switches

A photograph of the fabricated coplanar *77GHz* InGaAs PIN diode SPDT switch is shown in Figure 4.31. The chip size was *2mm×0.8mm*. On-wafer W-band S-parameter measurements of the SPDT switches were performed using three *Pico*-probes and a *HP8510B* network analyzer with millimeter-wave option. The network analyzer was calibrated to the reference planes of the W-band microwave probes. The third port of the SPDT switch was connected to a W-band probe loaded with a *WR-10* waveguide termination. Independent on-wafer S-parameter measurements of a coplanar "through" standard with such termination showed that the return loss was larger than *20dB*, making it an acceptable substitute for a matched third output port.

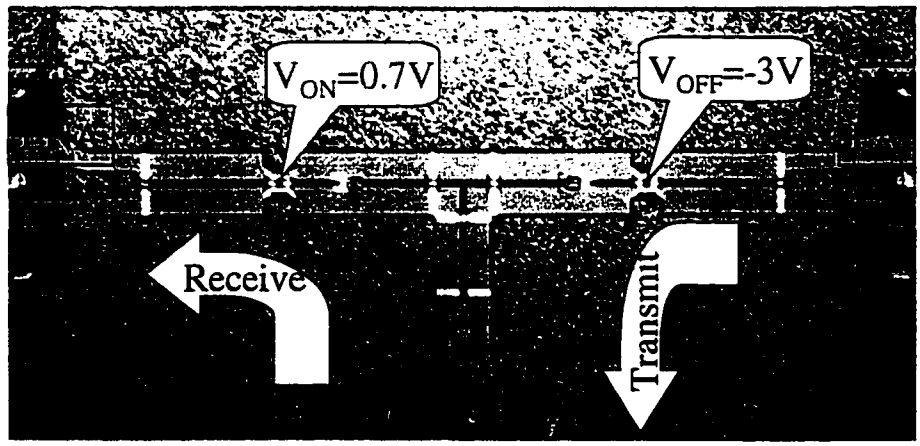


Figure 4.31. Photograph of fabricated coplanar *77GHz* InGaAs PIN diode SPDT transmit-receive switch

An SPDT transceiver switch is said to *transmit* when the signal is directed from port "2" (*PA*) to port "1" (*Antenna*) and to *receive* when the signal is directed from port "1" (*Antenna*) to port "3" (*LNA*), as marked in Figure 4.31.

Insertion loss of the *77GHz* InGaAs PIN SPDT transceiver switch was evaluated when testing probes were connected to ports "1" and "2" and a matched termination was connected to port "3". The InGaAs PIN diode between ports "1" and "2" was biased into a low-impedance *ON*-state (V_{ON}=*0.7V*), while the other diode between ports "1" and "3" was biased into a high-impedance *OFF*-state (V_{OFF}=*-5V*) as marked in Figure 4.31. In this configuration, the "PA" port was linked to the "Antenna" port, while the "LNA" port with the *ON*-state diode was isolated.

Insertion loss was measured by S_{12} and S_{21} for the *"transmit"* and *"receive"* directions, respectively, and the results are shown in Figure 4.32a). The switch demonstrated minimum loss of *1.6dB* for the *"transmit"* and *1.9dB* for the *"receive"* direction. Low insertion loss of less than *2dB* was observed over a *3-GHz* and *2-GHz* bandwidth for "transmit" and "receive" directions, respectively.

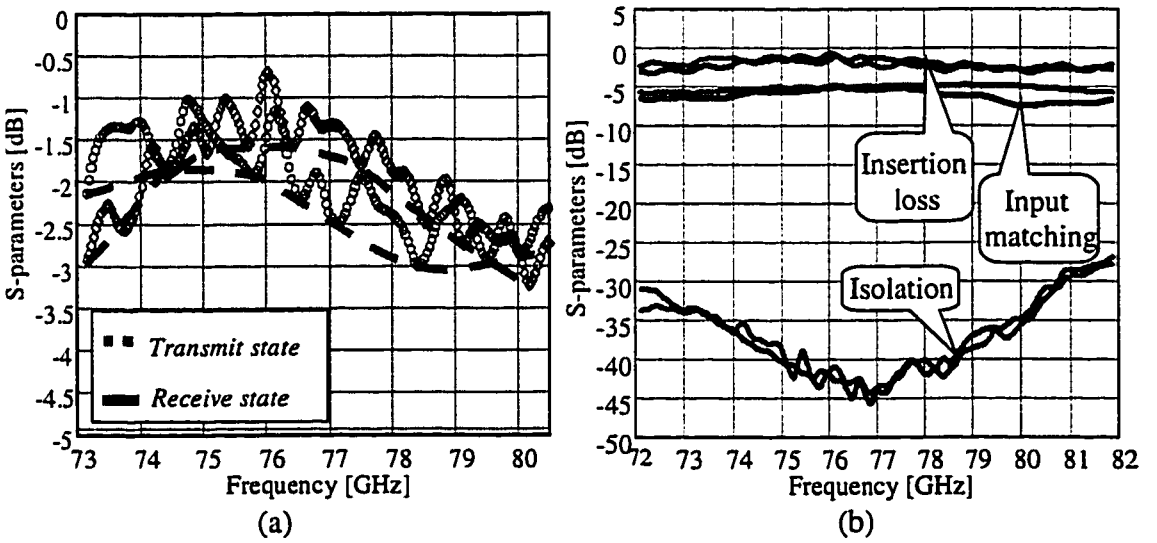


Figure 4.32. Insertion loss (a) and isolation (b) of *77GHz* InGaAs PIN diode SPDT switch measured for the *"receive"* and *"transmit"* directions

Isolation of the *77GHz* InGaAs PIN SPDT transceiver switch was evaluated when the diode between ports "1" and "2" was on and the diode between ports "1" and "3" was off. The isolation between the input and the output ports was larger than *40dB* over a *3.5GHz* bandwidth for both directions, and exceeded *43dB* at *77GHz* as shown in Figure 4.32b). This is the highest reported value for isolation achieved by a monolithic transceiver switch at W-band frequencies.

On-wafer S-parameter characterization of switch also revealed that matching characteristics differed from the design values and were as high as *-5dB* as indicated in Figure 4.32b). Among possible reasons for such discrepancy is the accuracy of the equivalent-circuit model of the InGaAs PIN diodes. Thus, the parasitic pad capacitance C_{PAR} is strongly dependent on the specific technology used in the fabrication of MMICs. The impact of the parasitic capacitance on the performance of InGaAs PIN diode SPDT switches was studied using Libra and the results are shown in Figure 4.33. This analysis showed that while isolation and insertion loss (indicated by S_{13} and S_{23}, respectively) are not affected by variations in the value of parasitic capacitance, even a small change of C_{PAR} leads to significant degradation of matching characteristics (S_{33} and S_{22}, respectively). Thus, results presented in Figure 4.33b) show that matching characteristics simulated by Libra are similar to experimental data (see Figure 4.32b) for only a small change of parasitic capacitance between *5* and *15fF*.

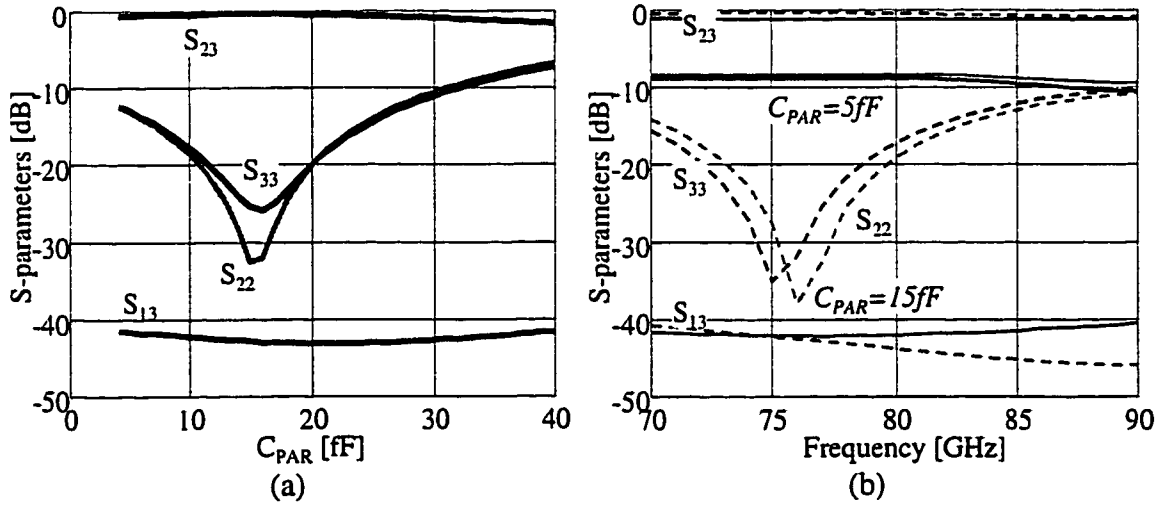


Figure 4.33. Impact of the parasitic PIN-diode capacitance on performance of a coplanar *77-GHz* InGaAs PIN diode SPDT switch

The crosstalk between port "2" (*PA*) and port "3" (*LNA*) of the SPDT switch was studied by measuring on-wafer S-parameters between these two ports (S_{23}) and using matched termination for port "1" (*Antenna*). The results are shown in Figure 4.34. During the operation of the transceiver switch, one diode is always on and another diode is always off. Measured under such conditions, the crosstalk was less than *-30dB* over a *10-GHz* bandwidth from *75* to *85GHz*.

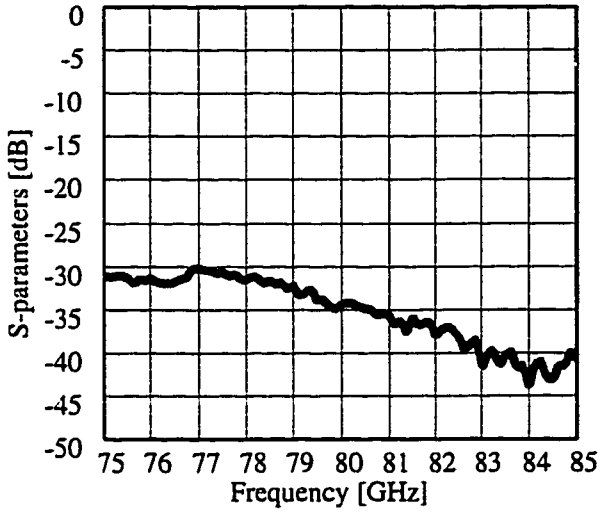


Figure 4.34. Output crosstalk of 77GHz InGaAs PIN diode SPDT switch.

A *94-GHz* InGaAs PIN diode SPDT switch was designed and fabricated with integrated on-chip biasing network, which employed DC blocking capacitors and quarter-wavelength impedance transformers. A photograph of the switch photograph is shown in Figure 4.35. The *94-GHz* SPDT switch also had very high value of isolation (*>40dB*) and low insertion loss (*~1.7dB*) similar to the *77-GHz* switch. The introduction of the biasing network also provided auxiliary structures for optimization of input matching, which was better than *20dB* for the *94-GHz* SPDT switch.

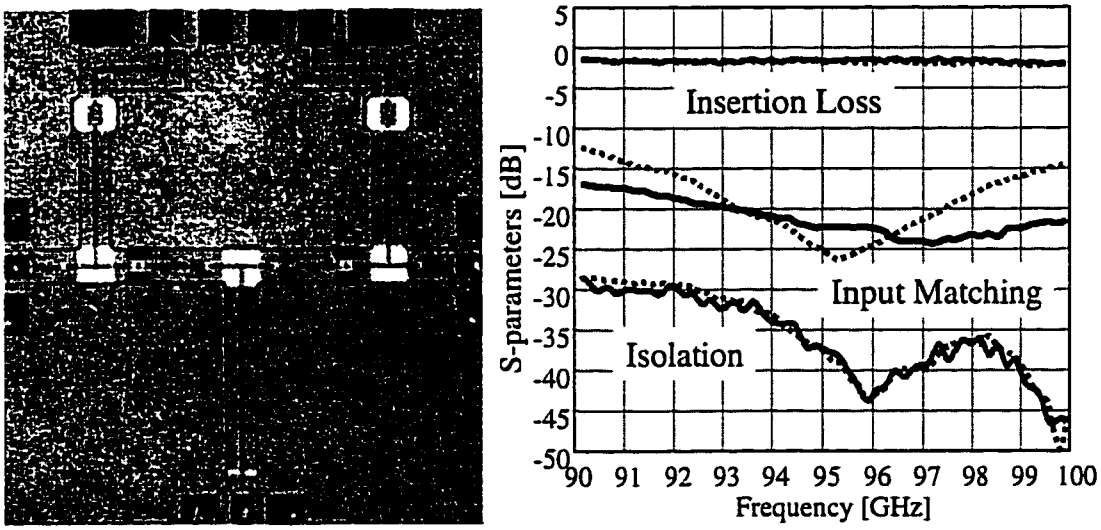


Figure 4.35. Photograph and characteristics of *94-GHz* InGaAs PIN diode SPDT transceiver switch with on-chip integrated biasing networks.

The low insertion loss (*1.6dB*), small crosstalk (*<-30dB*), and record-high isolation (*>40dB*) achieved by coplanar W-band InGaAs PIN SPDT switches are attributed to the low resistance and small parasitic inductance of the developed coplanar InGaAs PIN diodes.

4.5. W-band InGaAs PIN Diode Phase Shifters

Microwave phase shifters are employed in a variety of communication and radar applications. Since development of microwave monolithic integrated circuit technology, monolithic phase shifters with frequencies up to V-band have been demonstrated [61]. The two types of phase shifters employing switching diodes are *transmission-type* and *reflection-type*. High-performance switching InGaAs PIN diodes developed in this work were employed for realization of phase-shifting functions at W-band frequencies using both types of phase shifters. Design, operation, and characteristics of transmission-type loaded-line W-band InGaAs PIN diode phase shifters fabricated using InP-based microstrip technology are presented first. Coplanar-waveguide InGaAs PIN MMIC technology was used to realize reflection-type phase shifters with constant *time-delay* (such that the phase shift has linear dependence with frequency) and constant *phase-shift* (such that the phase shift is independent of frequency) properties.

4.5.1. Design and Operation of W-band Loaded-Line Phase Shifters

A design schematic of a loaded-line phase shifter is shown in Figure 4.36. The phase shifter consisted of the main transmission line of characteristic impedance Z_0 shunted by two transmission-line stubs. Each of the shunting stubs had one switching PIN diode connected in series. The diodes were used to control the effective impedance of the main transmission line depending on their state. When the diodes were in the OFF-state, the shunting stubs were terminated with a capacitive loading and the effective impedance Z_{EFF} of the main transmission line was reduced. In the ON-state, the diodes provided inductive termination and the effective impedance Z_{EFF} of the main transmission line was increased.

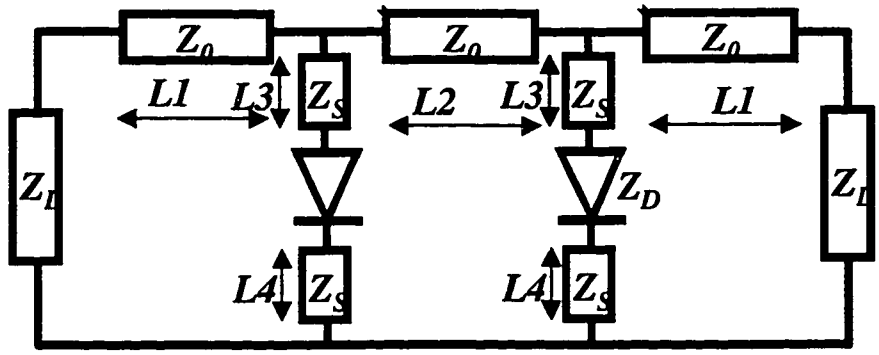


Figure 4.36. Schematics of a loaded-line InGaAs PIN diode phase shifter

The propagation constant of the transmission line $\beta = \omega \times \sigma / c$ depends on the characteristic impedance of the transmission line $\sigma = 377/Z_0$ as discussed in detail in Section 4.2. Thus, when Z_{EFF} is increased by turning the diodes *on*, the propagation constant is reduced, signal propagation is slowed, and the phase of the output signal is increased. When the diodes are *off*, the effective impedance is reduced, the propagation constant is increased, and the phase is reduced. This feature allows control of the phase of the signal transmitted by a loaded-line phase-shifter by varying the bias applied to the PIN diodes.

The design of the InGaAs PIN loaded-line phase shifter was optimized to produce *90-degree* phase shift at the frequency of *94GHz*. For this purpose, high-frequency characteristics of the loaded-line phase shifters of Figure 4.36 were calculated using the *ABCD* transmission matrix method, which allowed evaluation of the complex transmission coefficient S_{21}. The phase shifter was designed using *5μm*-diameter InGaAs PIN diodes (see Table 4.1). The characteristic impedance of the main transmission line (Z_0) and the shunting stubs (Z_S) was *50Ω* and *60Ω*, respectively, in order to minimize the insertion loss of the circuit. The dimensions of the transmission-line sections *L1*, *L2*, *L3*, and *L4* (see Figure 4.36) were chosen by optimizing the insertion loss and phase-shift of the circuit at the design frequency.

Thus, the lengths of loaded-line sections *L1=200μm* and *L2=280μm* were selected to provide maximum transmission of the signal at the design frequency of *94GHz*. The lengths of shunting stubs *L3* and *L4* were used to obtain desired phase-shifting properties. For this purpose, the length of the shunting stub between the diode and the main transmission line *L3* was varied between *40* and *90μm*, while the length of

L4 was kept fixed at *35μm*. The results are shown in Figure 4.37 and indicate that low insertion loss for the ON- and OFF-states (S_{21}^{ON} and S_{21}^{OFF}, respectively) occurs for the shunting stubs with *L3* between *50μm* and *82μm*.

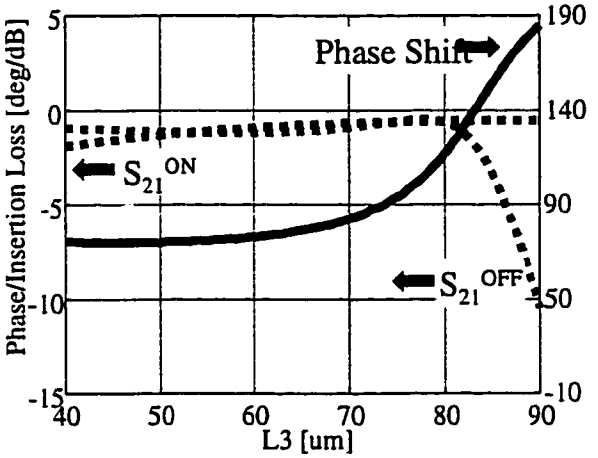


Figure 4.37. Design of the shunting stub length (*L3*) for a *90-degree* phase shift of *94GHz* InGaAs PIN loaded-line phase shifter

The phase shift between the OFF- and the ON-state transmission is also shown in Figure 4.37. When *L3* is varied between *46* and *82μm*, the phase shift is increased from *70* to *120 degrees*. The design goal of a *90-degree* shift was obtained for *L3=75μm*. Frequency-dependent S-parameters and phase-shifting characteristics of the InGaAs PIN diode loaded-line phase shifter optimized for *90-degree 94-GHz* operation are shown in Figure 4.38.

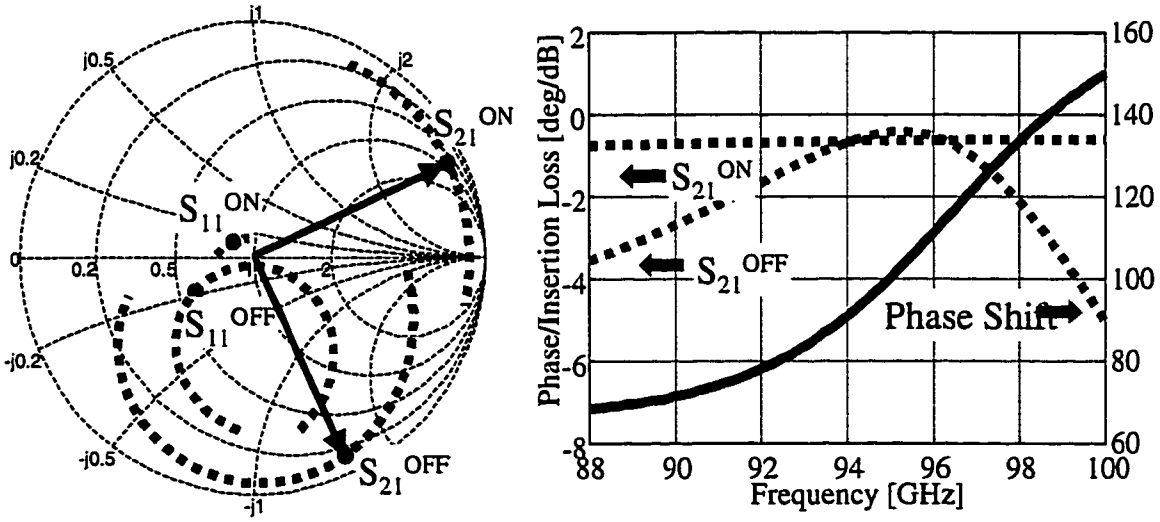


Figure 4.38. Calculated high-frequency characteristics of a *94GHz 90-degree* InGaAs PIN diode loaded-line phase shifter

The calculations predicted a low insertion loss of *~1dB* and a small return loss of *–20dB* and a *90-degree* phase-shift at the design frequency of *94GHz*.

4.5.2. Characteristics of Microstrip W-band Loaded-Line Phase Shifters

Microstrip W-band InP-based InGaAs PIN loaded-line phase shifters were designed using the microwave simulator *Libra*. A photograph of a fabricated circuit designed for operation at *94GHz* with a *90-degree* phase shift is shown in Figure 4.39.

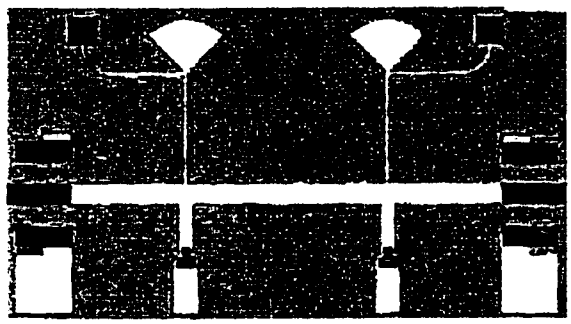


Figure 4.39. Photograph of microstrip *94-GHz* InGaAs PIN diode loaded-line 90-degrees phase shifter with on-chip integrated biasing networks.

The phase shifter design consisted of a section of *50-Ω* microstrip transmission line shunted at the ends through *60-Ω* stubs with two 5μm-diameter InGaAs PIN diodes. The circuit employed six InP backside vias for DC and high frequency grounding as well as on-wafer integrated biasing networks.

Experimental characteristics of the InGaAs PIN loaded-line phase shifter at W-band are shown in Figure 4.40. The figure demonstrates a *90-degree* phase shift at 93GHz. The return loss and the insertion loss at the same frequency were *13dB* and *3dB*, respectively.

The high value of the experimentally observed insertion loss (*~3dB* vs. *~1dB* as was predicted for intrinsic circuits in the previous section) was attributed to the influence of parasitic elements, such as via-hole and airbridge inductances. Microwave and electromagnetic simulations of the phase-shifter characteristics performed using *Libra* and *Momentum* allowed incorporation of distributed effects of via holes and airbridges. Phase-shifter characteristics obtained by such simulations showed good agreement with the experimental data as shown by dashed lines in Figure 4.40. Similar loaded-line phase

shifters designed using GaAs PIN diodes and operating at a lower frequency were reported and demonstrated *~2dB* insertion loss for a *90*-degree phase shift at *35GHz* [64].

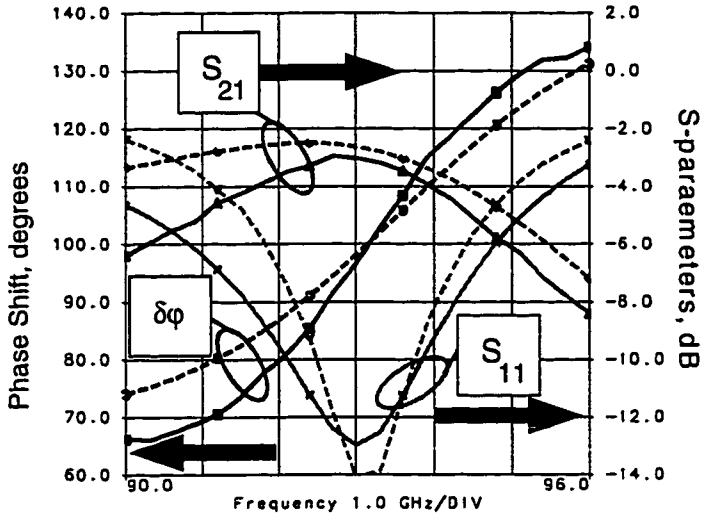


Figure 4.40. Experimental (solid lines) and simulated (dashed lines) characteristics of microstrip *94-GHz* InGaAs PIN diode loaded-line *90-degrees* phase shifter.

4.5.3. Coplanar W-band Reflection-Type InGaAs PIN Diode Phase Shifters

Low-parasitics coplanar-waveguide InGaAs PIN diode MMIC technology employed for fabrication of high-performance W-band SPDT switches was also applied for realization of reflection-type phase shifters. A W-band reflection-type phase shifter consisted of a section of high-impedance coplanar waveguide terminated with a shunt InGaAs PIN diode. The phase shift was given by the change in the reflection coefficient between the ON- and OFF-state of the diode since the phase of the OFF-state reflection coefficient (Γ_{OFF}) increased proportionally to the OFF-state capacitance of the diode C_{OFF}:

$$\phi_{OFF} = \arg(\Gamma_{OFF}) = \arg\left(\frac{(Y_0 - j\omega C_{OFF})}{(Y_0 + j\omega C_{OFF})}\right) = -\arctan\left(\frac{2\omega C_{OFF}}{Y_0}\right) \approx -\frac{2\omega C_{OFF}}{Y_0} \quad (4.12)$$

while the phase of Γ_{ON} increased proportionally to the feed-line inductance L_{AB}:

$$\phi_{ON} = \arg(\Gamma_{ON}) = -\arg\left(\frac{(Z_0 - j\omega L_{AB})}{(Z_0 + j\omega L_{AB})}\right) = -\arctan\left(\frac{2\omega L_{AB}}{Z_0}\right) \approx -\frac{2\omega L_{AB}}{Z_0} \quad (4.13)$$

Thus, by adjusting C_{OFF} and L_{AB}, reflection-type PIN-diode phase shifters can be modified to operate as constant *phase-shift* (constant phase difference between switching states) or constant *time-delay* (phase difference between switching states has a linear dependence on frequency) circuits.

W-band coplanar reflection-type phase shifters were fabricated using *5μm*- and *10μm*-diameter InGaAs PIN diodes. InGaAs PIN diodes were used to terminate a high-impedance (*84Ω*) coplanar transmission line, the diodes were mounted across both sides of a coplanar waveguide to provide low-inductance ground. The length of the coplanar-waveguide feed line (*120μm*) was selected to provide constant *time-delay* or constant *phase-shift* characteristics.

Figure 4.41 shows calculated and measured characteristics of reflection-type InGaAs PIN phase shifters, which employed *10μm*-diameter diodes. The theoretical results were calculated using transmission-matrix theory and the equivalent circuits for InGaAs PIN diodes (see Table 4.1). The experimental results were obtained by on-wafer W-band S-parameters characterization between *80* and *100GHz*. The insertion loss in both switching states was less than *2dB* for frequencies up to *97GHz*, while the phase shift increased linearly with frequency from *140* to *160 degrees* between *80GHz* and *93GHz*, characteristic for constant *delay-time* circuits.

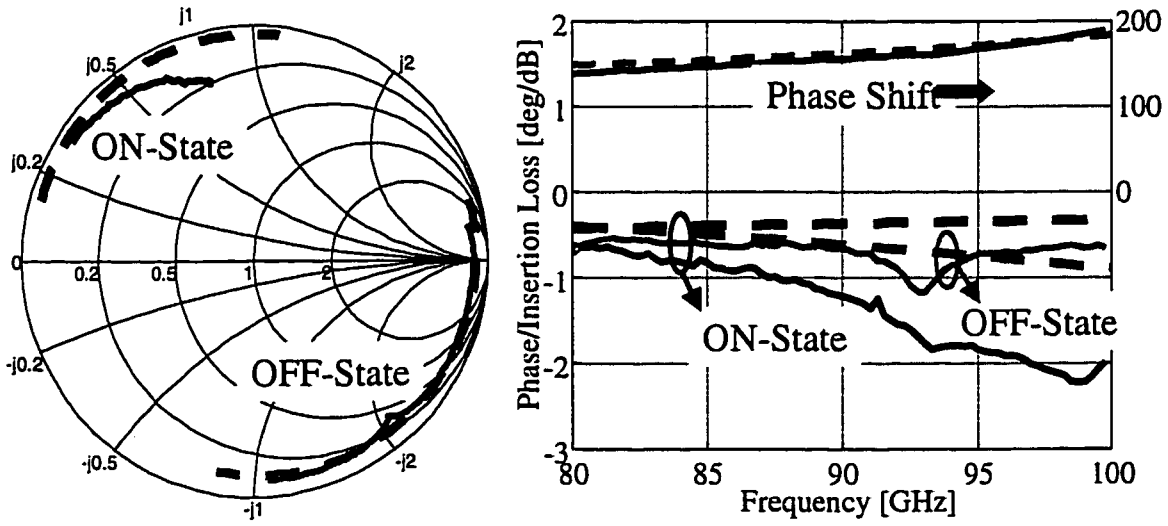


Figure 4.41. Calculated (dashed lines) and measured (solid-lines) characteristics of W-band InGaAs PIN *time-delay* phase shifters.

An excellent agreement between calculated and measured results was observed for the value of the phase shift and the OFF-state insertion loss. The insertion loss for the ON-state was higher in the experimental case, possibly due to the losses of the long airbridge used in this design.

Results of Figure 4.41 indicate that constant *phase-shift* properties can be achieved for reflection-type InGaAs PIN diode phase shifters if the OFF-state capacitance C_{OFF} is reduced by using smaller-size PIN diodes. Thus, reflection-type phase shifters with *5μm*-diameter InGaAs PIN diodes demonstrated a constant phase shift of *~110 degrees* for the entire frequency range between *80GHz* and *100GHz* as shown in Figure 4.42. The insertion loss in both switching states was less than *2dB* for frequencies up to *93GHz*.

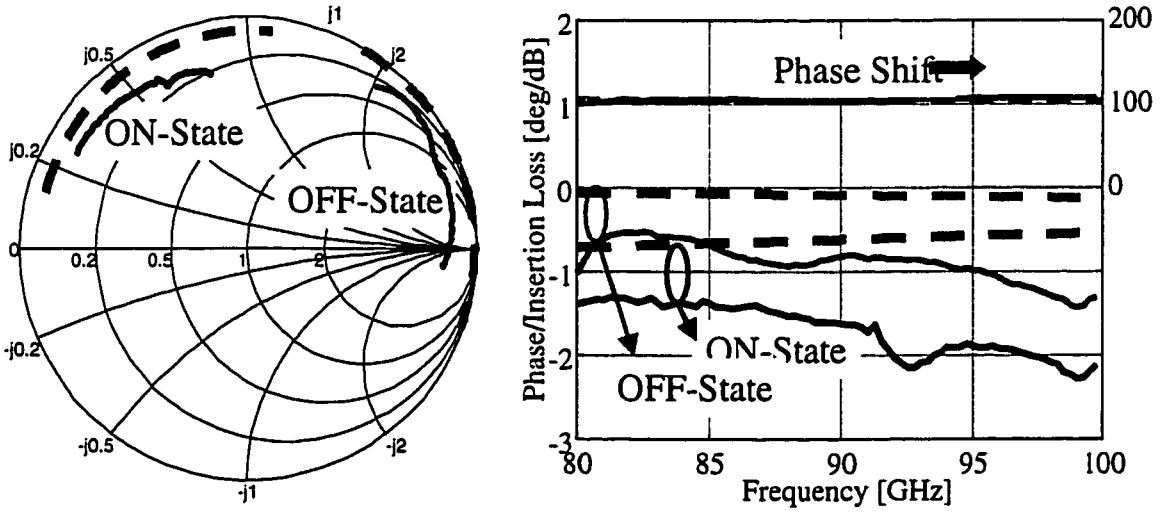


Figure 4.42. Calculated (dashed lines) and measured (solid-lines) characteristics W-band InGaAs PIN constant *phase-shift* phase shifters.

Overall, constant *time-delay* and constant *phase-shift* reflection-type phase shifters operating at W-band frequencies were realized using coplanar InGaAs PIN diode MMIC technology and demonstrated low insertion loss (*<2dB*) and wide operational bandwidth (up to *20GHz* or *20%*). Previously, a Ku-band PIN-diode reflection-type phase shifter had been demonstrated at a lower frequency of *28GHz* with *1.5dB* insertion loss and *2GHz* bandwidth [69]. Exceptionally good performance of W-band InGaAs PIN phase shifters of this work, compared with results reported in the literature, is due to excellent switching

characteristics of InGaAs PIN diodes and low-parasitics of InP-based coplanar MMIC technology.

4.6. Conclusions

W-band InP-based microstrip and coplanar MMICs using InGaAs PIN diodes as switching elements were designed with the help of *HP EEsof Libra* and *Momentum* simulators. Fabrication of these circuits required development of low-parasitics backside-via technology on InP. A low-inductance transition between a switching InGaAs PIN diode and a coplanar-waveguide was developed and allowed low-parasitics shunt mounting of the diodes in coplanar monolithic circuits.

Experimentally determined high-frequency performance for a variety of W-band InGaAs PIN diode switches and phase-shifters implemented in microstrip and coplanar waveguide InP-based MMIC technology was presented.

Microstrip SPST switches realized using InP-based PIN diodes demonstrated high isolation of *35dB* and low insertion loss of *1.3dB* for design frequencies between *83* and *94GHz*. Excellent performance of the InGaAs PIN diode switches was accompanied by reduced DC power consumption of *<1mW*.

Low-parasitics coplanar InGaAs PIN diode technology was developed and applied to design and fabrication of *77* and *94GHz* InGaAs PIN SPDT transceiver switches. Coplanar W-band SPDT switches employing low-parasitics InGaAs PIN-CPW transitions demonstrated low insertion loss of *1.6dB*, small crosstalk of *-30dB*, and the highest reported for a W-band MMIC switch isolation of *43dB*.

Loaded-line W-band InGaAs PIN diode phase shifters were fabricated using InP-based microstrip technology and demonstrated a *90-degree* phase shift at *93GHz*. Coplanar technology was used to realize W-band reflection-type InGaAs PIN diode phase shifters with constant time-delay and constant phase-shift properties. Reflection-type phase shifters demonstrated low insertion loss (*<2dB*) and wide bandwidth of *>10GHz*.

CHAPTER 5
CHARACTERIZATION OF POWER-HANDLING AND SWITCHING-RATE CAPABILITIES OF InGaAs PIN DIODES

Microelectronic devices capable of operation at frequencies of *77GHz* and above are necessary for the development of automotive collision-prevention systems and other emerging W-band radar applications [70]. InP-based InGaAs PIN diode SPDT transceiver switches developed in this work and presented in the previous chapter demonstrated excellent characteristics at these frequencies.

High-isolation and reduced DC power consumption properties of InP-based PIN switches are due to higher electron mobility and smaller bandgap of InGaAs compared with GaAs. However, the smaller bandgap of InGaAs also manifests itself in an earlier onset of self-biasing effects and a smaller breakdown voltage, which affects power handling of InGaAs PIN diodes. Large-signal characteristics of InP-based PIN diode switches need to be evaluated at W-band and lower frequencies in order to determine the power-handling capabilities of InGaAs PIN diodes.

The modulation bandwidth of the W-band InGaAs PIN diode switches also needs to be investigated. The PIN diode ON/OFF switching time is associated with a minority-carrier lifetime. The switching time of *1-2ns* has been reported for GaAs PIN diodes [71] and it is expected to be similar for InGaAs PIN diodes. Pulsed high-speed time-resolved measurements are employed to evaluate the switching rates of InGaAs PIN diodes.

5.1. Development of W-Band Automatic On-Waver Load-Pull System

Emerging commercial and military radar systems operate at the W-band frequency of *77GHz* and above. Accurate small-signal as well as large-signal models and good understanding of electrical characteristics are necessary in this frequency range for

optimal design of amplifiers, switches, and other W-band radar system components. An application of the W-band load-pull characterization technique to millimeter-wave devices would improve understanding of their high-frequency large-signal behavior and help in the design of integrated transceivers. Currently employed techniques are based on either extrapolation of characteristics measured at lower frequencies or on manual testing, which is often limited in range and resolution.

An automated W-band on-wafer large-signal characterization system was developed for the first time in the course of this work. It was applied to perform load-pull and power saturation measurements of W-band monolithic InP-based InGaAs PIN diode switches in order to evaluate their power handling capabilities directly at the application frequencies.

5.1.1. W-band Load-Pull System Components

The developed W-band on-wafer large-signal characterization system consisted of a control computer, electromechanical W-band tuner, network analyzer, W-band testset, the RF and the LO sources, frequency multiplier, and two power sensors. The RF source was used to generate *15-22GHz* signal, which was then upconverted by a frequency multiplier to produce W-band testing signal at frequencies between *75* and *110GHz*. The source setup also included an isolator for source isolation and protection, an attenuator for input power control, and a mechanical *EH*-tuner for input matching. A schematic of the connected setup is shown in Figure 5.2.

A *10-dB* waveguide directional coupler was used to monitor the input power (P_{IN}). Both input and output power were monitored by W-band mixers driven by the LO source, which was phase-locked with the RF source. The benefits from the use of mixers as power meters include their frequency selectivity and expanded dynamic range.

Since the frequency multipliers were not intended to operate as high-power sources, the maximum input power at the *DUT* level for the setup of Figure 5.1 was *-2dBm*. Free-running W-band IMPATT and Gunn-diode oscillators with increased power capabilities were employed to generate a high-power testing signal. However, the

frequency of the free-running oscillators had to be stabilized in order to use them in the measurement system.

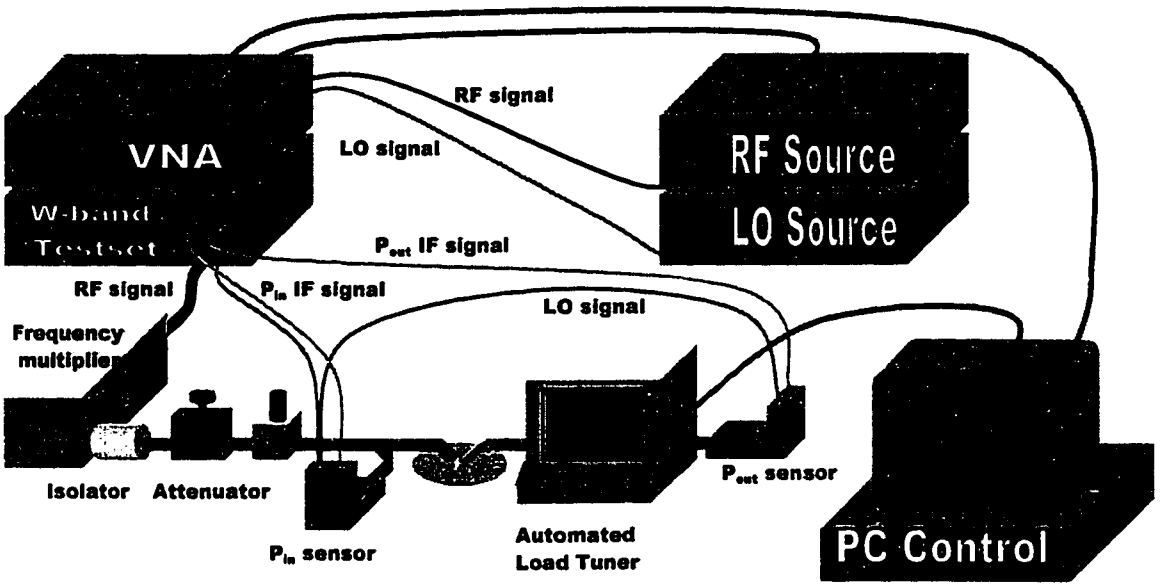


Figure 5.1. Schematics of an automated W-band on-wafer load-pull system

A stable high-power W-band source developed for this purpose consisted of a free-running high-power oscillator connected to the input port of a *10-dB* waveguide directional coupler. The frequency of the high-power source was stabilized by the injection-locking technique. Thus, a W-band multiplier was connected to the coupled port so it would inject a low-power high-stability reference signal into the output of the free-running oscillator. The direct port of the coupler served as the main output.

Output power spectra of the input signal obtained under free-running and injection-locked conditions are shown in Figure 5.2. While the locking range was small, it was still possible to adjust the output frequency of the high-power source by independent tuning of the free-running oscillator followed by locking at the new output frequency. Once locked, developed high-power W-band sources maintained their output frequency over wide dynamic range of power levels as also shown in Figure 5.2.

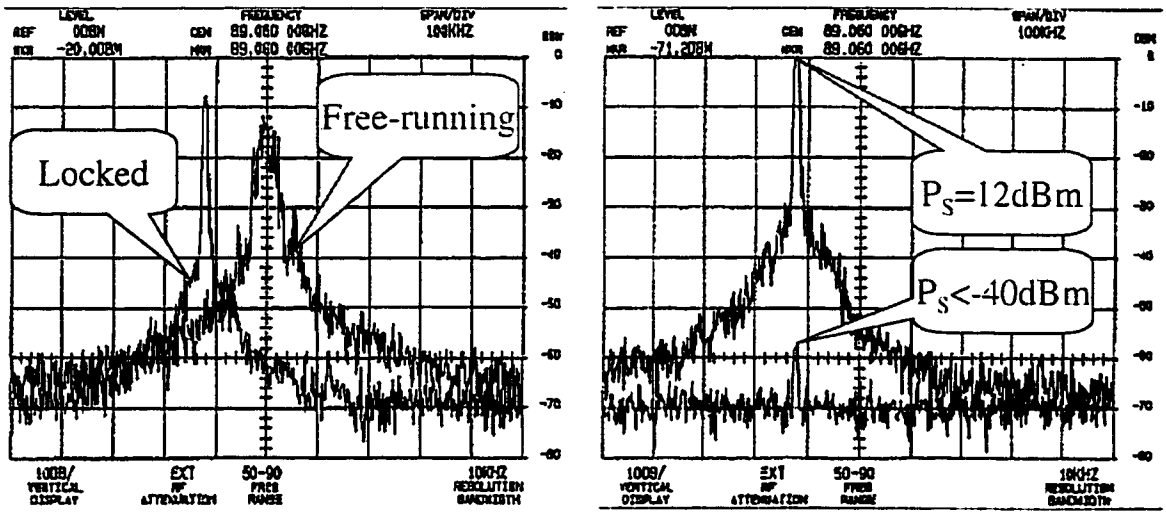


Figure 5.2. Injection-locking of free-running IMPATT oscillator

Load-pull conditions were achieved with the specially developed W-band high-precision computer-controlled *FOCUS* electromechanical tuner [72]. The control computer measured power, gain, efficiency, and DC-bias as a function of input power and load impedance as set by the load tuner [73]. The tuner uses a *WR-10* waveguide with a non-contact slug moving in, out, and along the waveguide slot to generate controlled amplitude and phase variations. The vertical resolution of slug movement is *0.9μm* and the horizontal step is *1.5μm*. Obtainable VSWR exceeds *10:1*, and reaches up to *19:1* in most parts of the *75*-to-*110GHz* band. The tuner has excellent repeatability and is capable of tuning to *2,500,000* impedance points at *94GHz*.

During measurements the W-band tuner, frequency multiplier, and W-band mixers were connected with *WR-10* waveguide sections and mounted on an *Alessi* probe station using specially developed fixtures for reduced losses. The on-wafer probing was possible by means of W-band *PICO* probes. A photograph of the developed system with all W-band components is shown in Figure 5.3.

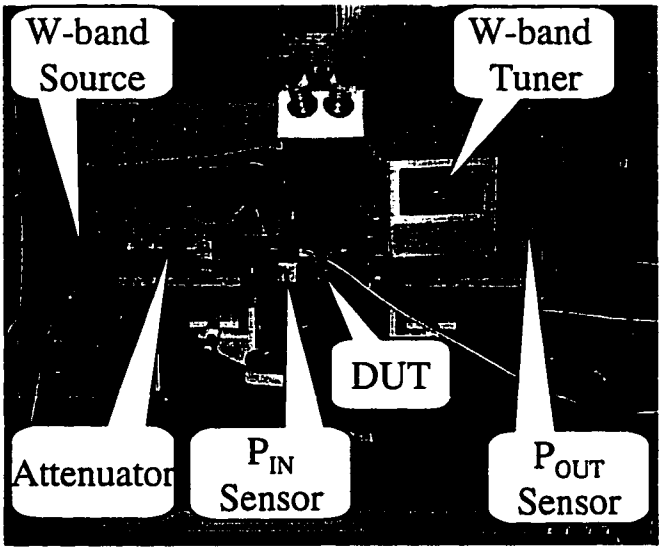


Figure 5.3. Photograph of the automated W-band on-wafer load-pull system

5.1.2. On-Wafer Calibration of W-band Load-Pull System

The purpose of the system calibration was to measure phase shifts and losses between the device under test (*DUT*), the load tuner, and the power meters in order to obtain measurements corrected to the probe tips. The part of the setup which required calibration and its power-flow schematics is shown in Figure 5.4. All systems blocks indicated in the figure had *WR-10* waveguide connectors.

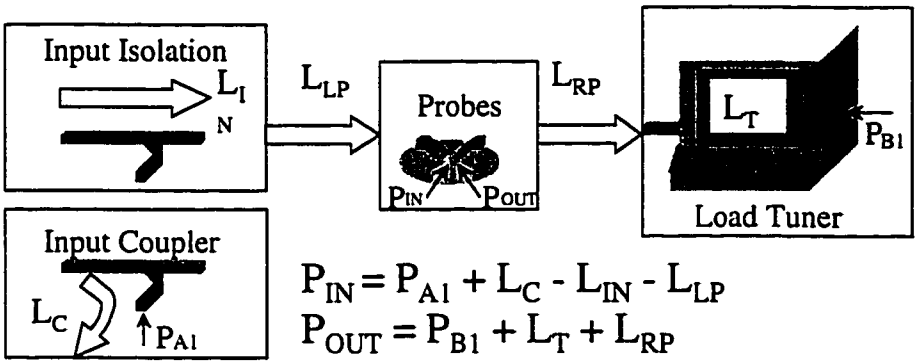


Figure 5.4. Power-flow schematics of the calibrated part of the load-pull system

The calibration was performed as follows. First, the W-band S-parameter characterization setup was assembled on a test bench and calibrated to the level of the *WR-10* waveguide outputs. Then the S-parameters of "Input Isolation" (input-to-output-port) and "Input Coupler" (input-to-coupled-port) system blocks were measured (see

Figure 5.4). It is important to note that although the calibration of the "Input Coupler" block required repositioning of the small-signal calibration setup for measurement with the waveguide ports oriented at *90* degrees, the calibration of the small-signal setup was preserved. This fact was carefully verified and was attributed to low sensitivity of the waveguide S-parameter calibration coefficients to phase variations in the cables between the network analyzer and the W-band frequency multipliers.

Next, the S-parameters of the "Load Tuner" block were measured and recorded for varying impedance conditions produced by computer-controlled movement of the tuner slug. There are *361* calibration points uniformly covering the Smith chart. The locations of the calibration points and the tuner loss measured at each point $L_T(Z_L)$ are shown in Figure 5.5 for *77-GHz* calibration. The tuner demonstrated low insertion loss (*~1dB*), which helped to enhance the measurement accuracy.

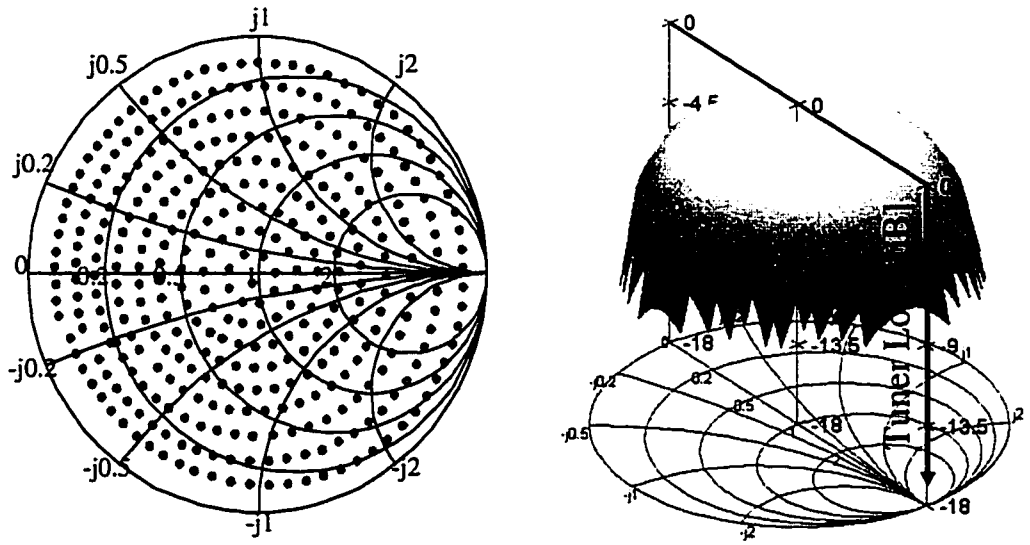


Figure 5.5. Calibration of the W-band Electromechanical Tuner at *77GHz.*

Next, the small-signal W-band S-parameter characterization setup is reassembled on the probe station and re-calibrated to the level of the *WR-10* waveguide outputs. The W-band microwave probes ("Test Fixture" block) are connected to the calibrated waveguide outputs and the S-parameters of the probes are measured using on-wafer calibration standards. Once all blocks are calibrated, the complete system is assembled in its final configuration following the schematics of Figure 5.4.

The value of input (P_{IN}) and output power (P_{OUT}) at the DUT level is calculated from power-meter readouts P_{A1} and P_{B1} using equations given below:

$$P_{IN} = P_{A1} + L_C - L_{IN} - L_{LP} \quad (5.1)$$

$$P_{OUT} = P_{B1} + L_T(Z_L) + L_{RP} \quad (5.2)$$

where L_C, L_{IN}, L_{LP}, $L_T(Z_L)$, and L_{RP} are the losses in the corresponding blocks as indicated in Figure 5.4. At *77GHz* the losses were L_C=*6.5dB*, L_I+L_{LP}=*3.7dB*, and L_{RP}=*2.1dB*.

P_{A1} and P_{B1} were monitored by the W-band power sensors, which consisted of W-band mixers preceded by W-band isolators for matching purposes. The choice of the mixers as power sensors was based on their high linearity, wide dynamic range, and frequency selectivity, as was confirmed by independent characterization. Prior to performing computer-controlled measurements, a manual high-precision W-band power meter was used to characterize the conversion losses of the mixers, which, at *77GHz*, were *-10.6dB* and *-8.7dB*, correspondingly. During measurements, the values of P_{A1} and P_{B1} were corrected automatically by computer.

In order to verify the calibration, constant loss contours of a through-line were evaluated and demonstrated low distortion and high uniformity as shown in Figure 5.6. Maximum transmission was found for load conditions close to the center of Smith chart. The loss between the load tuner and *DUT* decreases the maximum load impedance Γ_L visible by the device and therefore the maximum radius of load-pull contours to *~0.7*.

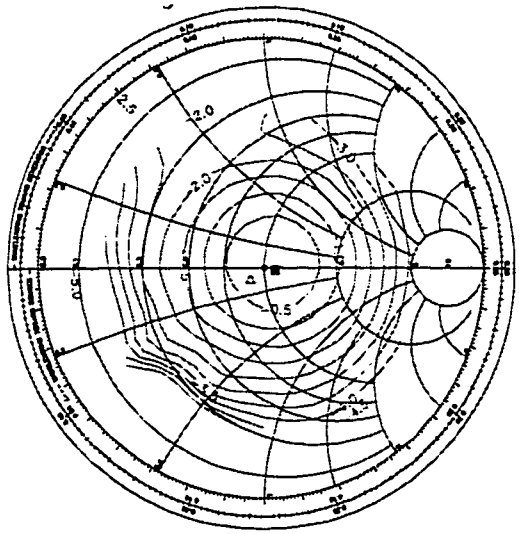


Figure 5.6. Constant loss contours measured for a "through" calibration standard

5.2. W-band Load-Pull Characterization of InGaAs PIN Diode and MMICs

InP-based switching PINs offer several important advantages over GaAs-based technology, namely: substrate compatibility with high-performance InP-based HEMTs, low ON-state resistance and reduced DC power consumption due to high electron mobility and small bandgap of InGaAs. However, the smaller bandgap of InGaAs also manifests itself in an earlier onset of self-biasing effects and a smaller breakdown voltage, which affects their power handling. In this section the power-handling capability of InGaAs PIN diodes is investigated and compared to that of GaAs PIN diodes. The trade-off between power handling, high frequency performance, and bias conditions is considered. Large-signal characteristics of W-band InGaAs PIN diode monolithic switches were measured using a W-band load-pull characterization system.

5.2.1. Coplanar W-band InGaAs PIN Diode SPST Switches

The investigated W-band InGaAs PIN diode monolithic integrated SPST switches were fabricated using InP-based coplanar-waveguide technology presented in Section 4.4 of Chapter 4. The switches employed two shunt-connected $5\mu m$-diameter PIN diodes spaced by $\lambda/4$ for improved performance. A photograph of the fabricated SPST switch is shown in Figure 4.21.

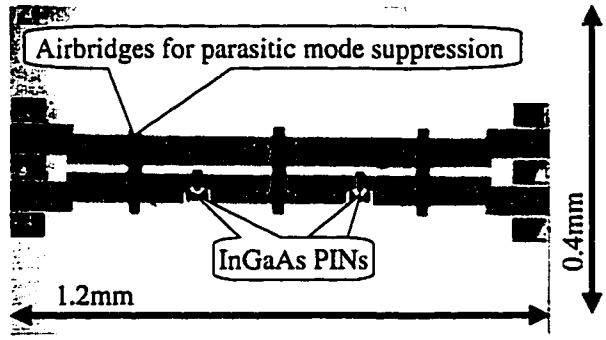


Figure 5.7. A photograph of coplanar W-band InGaAs PIN-diode SPST switch

Small-signal S-parameters of the fabricated InGaAs PIN diode switches were measured on-wafer at W-band frequencies as shown in Figure 5.8. The insertion loss and the return loss of the switch were measured by the scattering parameters S_{21} and S_{11} when

the diodes were in the OFF-state with bias V_D=-3V. The isolation and the reflection loss were measured by S_{21} and S_{11} when the diodes were in the ON-state (V_D=0.6V,I_D=0.9mA).

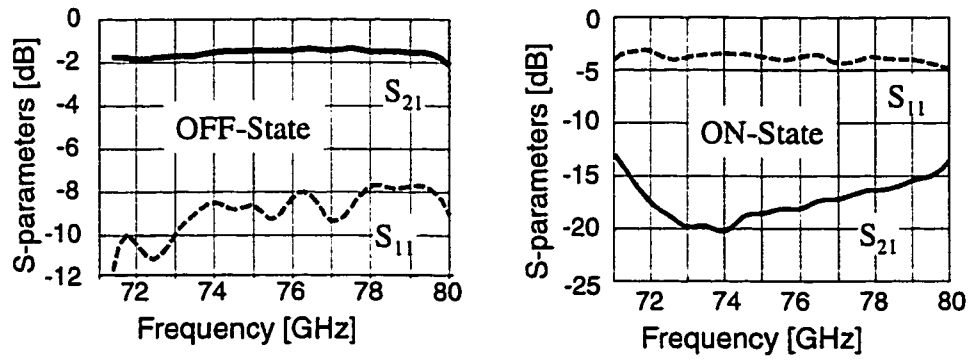


Figure 5.8. S-parameters of InGaAs PIN SPST switch in the OFF-state.

A low insertion-loss value of *1.4dB* was demonstrated at *77GHz*. The insertion loss was less than *2dB* for frequencies between *71* and *80GHz*, while corresponding return loss was around *8dB*. The maximum isolation was *17.2dB* at *77GHz* and better than *13dB* between *70* and *80GHz*.

5.2.2. Load Pull Characterization of InGaAs PIN SPST Switches at W-band

A developed automated on-wafer large-signal characterization system was used to evaluate constant loss contours for the described coplanar InGaAs PIN SPST switches at the W-band frequency of *77GHz* under different biasing conditions. First, constant-loss contours of the SPST switches were evaluated when PIN diodes were in the "zero" (V_D=0V) and in the OFF-state (V_D=-3V) as shown in Figure 5.9. Under such biasing conditions, the impedance of the InGaAs PIN diodes was high and, thus, the shunt PIN SPST switches were transmitting the input signal to the output port with only a small insertion loss. When the PIN diodes were biased with V_D=0V, the optimum load impedance Z_{MIN}=40-j8.4Ω was located close to the design goal of 50Ω. The corresponding minimum insertion loss was *1dB* as indicated in Figure 5.9.

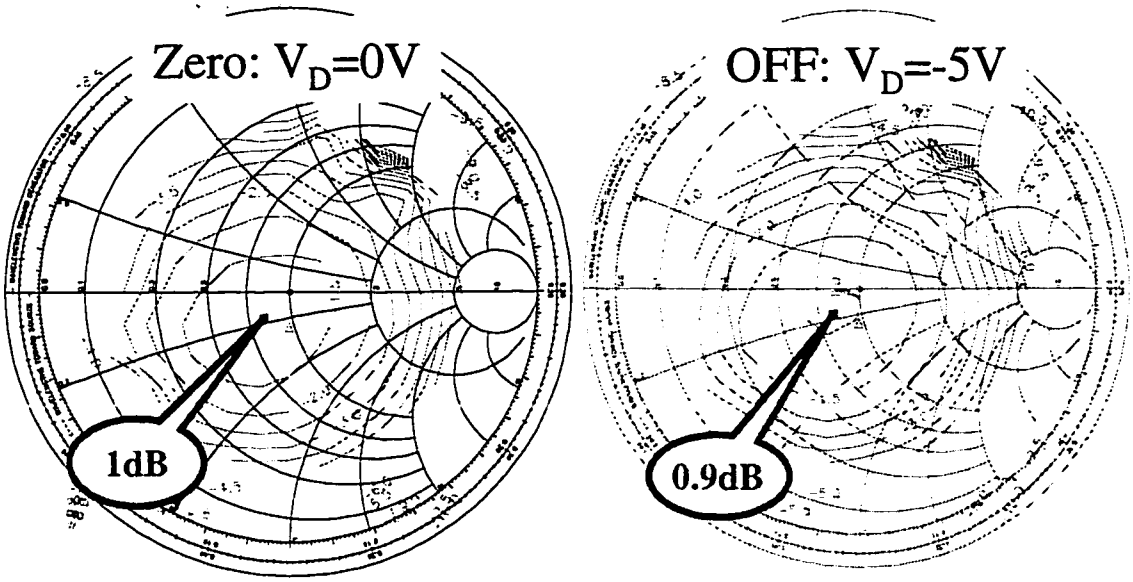


Figure 5.9. W-band constant-loss contours for OFF-state InGaAs PIN SPST.

The constant-loss contours grew wider and the minimum insertion loss improved to *0.9dB* when the diodes were biased with a larger OFF-state bias of *–5V*. The results confirmed that the OFF-state impedance of *5μm*-diameter PINs employed in this switch was dominated by its parasitic pad capacitance as was suggested earlier by the extracted parameters of the small-signal equivalent circuit for these devices.

When the diodes were biased in the low-impedance ON-state (*0.5V*, *50μA*), the location of minimum-loss impedance Z_{MIN} started to move away from the center of the Smith chart as shown in Figure 5.10. As the ON-state resistance was further reduced, the optimal impedance moved to the edge for increased ON-state bias of *0.7V (7mA)*. At the same time, the isolation at the center of Smith chart improved from *11* to *18dB*. However, the minimum ON-state isolation was *15.4dB* at Z_{MIN} *=14.7-j15.3Ω*. Thus, *18dB* of isolation at *50Ω* were contributed by two components, *15.4dB* from the diodes and *2.6dB* due to the mismatch with the minimum-loss load impedance Z_{MIN}.

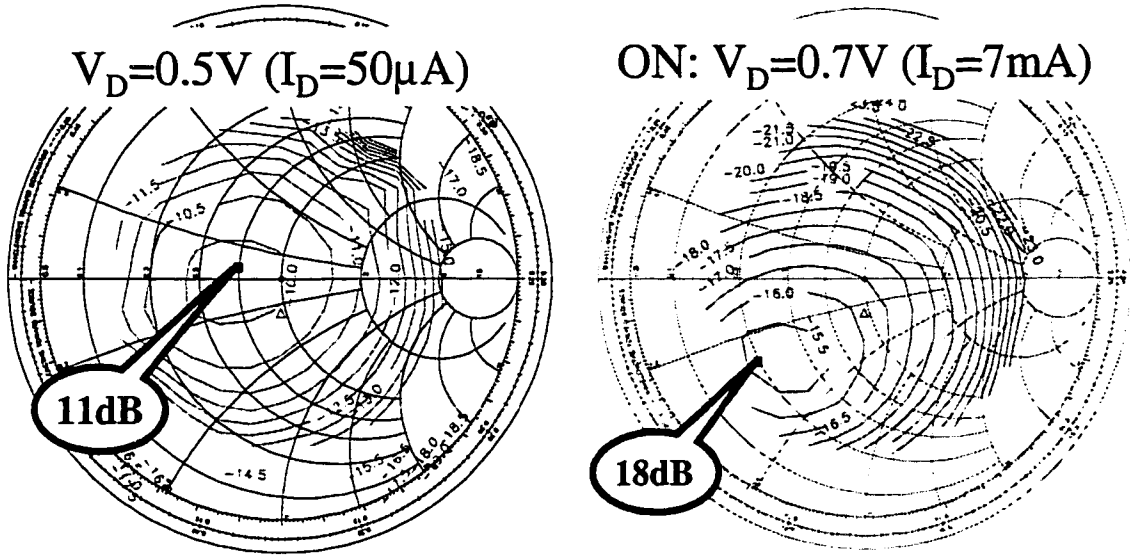


Figure 5.10. W-band constant-loss contours for ON-state InGaAs PIN SPST.

Dependence of the InGaAs PIN diode large-signal characteristics on the input power was also investigated. For this purpose, the loss of the switches was studied as the function of input power level as it was varied by *18dB* from the small-signal P_{IN}=*–25dBm* to the large-signal P_{IN}=*-7dBm* conditions. The latter was limited by the maximum power available from the *77GHz* source (P_A=*0dBm*). No difference was found between the small- and the large-signal constant-loss contours evaluated for different biasing conditions, indicating that a larger input power level was necessary for investigation of InGaAs PIN diodes. The results showed good agreement with the W-band S-parameter characterization results presented in Section 5.2.1.

However, the maximum power available from the *77GHz* source corresponded to *–7dBm* of input power at the *DUT* level, and was insufficient for evaluation of power-handing capabilities of InGaAs PIN diodes. A high-power *MITATT* source was, however, available at *102GHz* and was employed for studying power-handling capabilities of W-band InGaAs PIN SPST switches as described in the next section.

5.3. Power-Handling Capabilities of Switching InGaAs PIN Diodes and MMICs

The power-handling capabilities of InGaAs PIN switches were studied in order to evaluate their suitability for automotive applications, which employ high transmission-

power scanning signals (*7* to *13dBm* [70]). The developed W-band on-wafer large-signal characterization system with a high-power *102GHz* source was used for this purpose.

5.3.1. Power-Handling Capabilities of W-band InGaAs PIN SPST Switches

The power handling of the OFF-state PIN diode is of most importance because the OFF-state PIN diode is subject to self-biasing, which is the primary cause of degradation. Thus, large-signal characteristics were investigated by monitoring the insertion loss and the self-biasing current through the InGaAs PIN diodes as a function of the input power P_{IN} and the OFF-state bias V_D. The results are shown in Figure 5.11. As the input power was increased, the diodes were self-biased into the ON state, which manifested itself in an increase of current through the devices and degradation of insertion loss. The input power at which the self-biasing current reached $10\mu A$ corresponded to the input power at which the insertion loss started to increase, and this input power was defined as the power-handling capability P_{SB}.

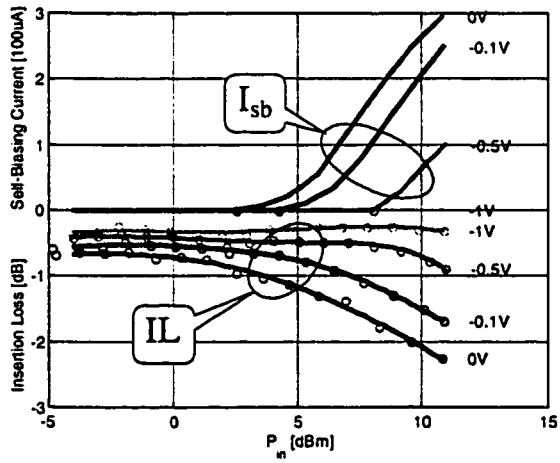


Figure 5.11. Insertion loss (*IL*) and self-biasing current (I_{SB}) of InGaAs PIN switch measured at *102GHz* as a function of input power and bias conditions.

At the zero OFF-state bias (V_D=*0V*), measured insertion loss degraded from *0.6dB* to *2.4dB* when power was increased from *–4* to *12dBm*. The zero-bias power-handling capability P_{SB} was *3dBm*, while a *1-dB* increase of the insertion loss occurred for P_{IN}=*6dBm*. The self-biasing effects induced by the presence of large-signal RF signal can be delayed or even eliminated by biasing the diodes with a negative OFF-state bias. Thus,

P_{SB} improved from *3* to *7dBm* for a very small negative bias V_D=*-0.5V*. Moreover, when diodes were biased with an OFF-state bias of only *-1V* no increase of the insertion loss or self-biasing current was detected for up to the maximum available source power of *12dBm*. At the same time, the small-signal power level insertion loss was improved from *0.6* to *0.3dB* due to the reduction of the PIN depletion capacitance.

The results of power-handling characterization of InGaAs PIN diode switches may be explained by considering conditions necessary for developing self-biasing effects in the InGaAs PIN diodes under study as illustrated in Figure 5.12.

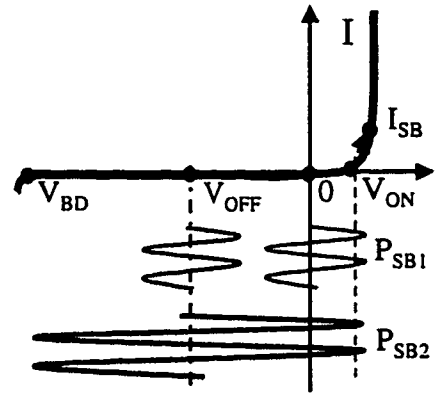


Figure 5.12. Relation between power-handling capabilities, self-biasing effects, and biasing conditions of InGaAs PIN diode switches

According to the I-V characteristics, self-biasing effects were initiated when the RF voltage *V(t)* clipped the PIN turn-on voltage V_{ON}. The amplitude of the RF voltage is determined by the input power $V_{RF} = P_{SB}^{1/2} \times Z_O$, while the instantaneous values of the RF voltage are given by $V(t)=V_{OFF}+V_{RF}\times sin(\omega t)$. Therefore, the power handling (P_{SB}) is given by:

$$P_{SB} = V_{RF}^2/Z_O = (|V_{OFF}|+|V_{ON}|)^2/Z_O \qquad (5.3)$$

where V_{ON} is the turn-on voltage, V_{OFF} is the OFF-state bias, and Z_O is the characteristic impedance of the transmission line. When the OFF-state bias is increased a larger RF voltage amplitude (and thus larger P_{SB}) is required for developing self-biasing effects as is reflected by the measurement results.

The results of the self-biasing study are summarized in Figure 5.13 together with the theoretical values calculated using equation (5. 3). The experimentally obtained

power-handling capability was in excellent agreement with the calculated values as shown in the figure.

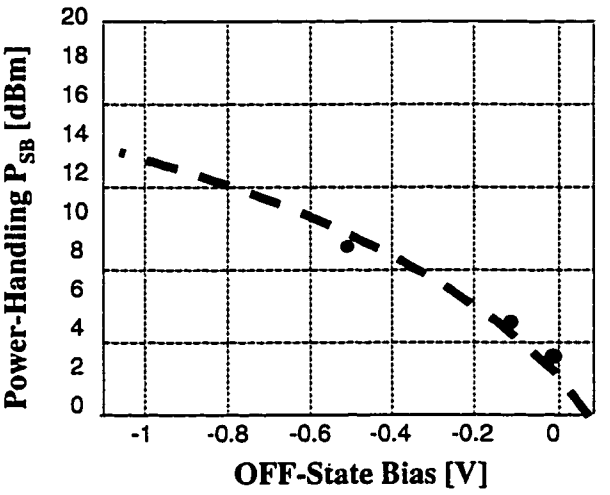


Figure 5.13. Calculated and measured power handling (P_{SB}) of InGaAs PIN SPST switches at *102GHz*.

5.3.2. Large-Signal Characteristics of W-band InGaAs PIN SPDT Switches

Large-signal characteristics of the high-performance coplanar W-band InGaAs PIN SPDT transceiver switches made using low-parasitics InGaAs PIN-CPW diodes were also investigated using the W-band load-pull system in order to determine their power-handling capabilities directly at the design frequencies. The design and small-signal W-band characteristics of these switches are presented in detail in Chapter 4.

Large-signal characteristics of the InGaAs PIN diode SPDT switch measured at *102GHz* under different bias conditions as a function of the input power level are shown in Figure 5.14. The degradation of the insertion loss was investigated first. For this purpose the ON-state diode (*D2*) was biased with a practical ON-state bias (V_{D2}=*0.7V*). When the OFF-state diode (*D1*) was biased very close to the PIN turn-on voltage of *0.4V* (V_{D1}=*0.3V*), increasing input power above *+1dBm* caused the OFF-state diode to self-bias toward the ON-state, which resulted in an increased insertion loss.

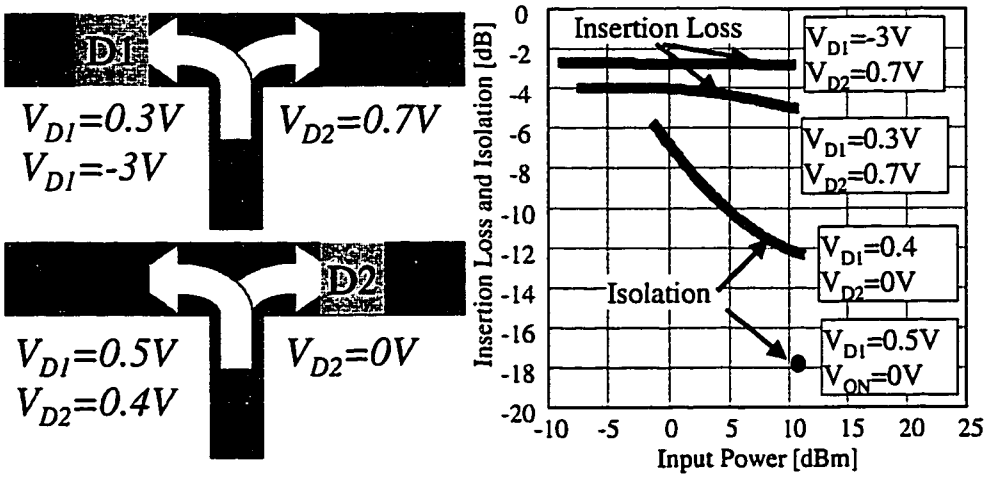


Figure 5.14. Power dependence of insertion loss and isolation of InGaAs PIN diode SPDT switch for different bias conditions.

However, under normal OFF-state biasing conditions ($V_{D1}<0V$), no degradation of the insertion loss was observed for input power levels up to *11dBm*; the latter was limited by the maximum power available from the W-band source.

Under practical biasing conditions ($V_{D1}=0.7V$, $V_{D2}=-3V$), the investigated coplanar W-band InGaAs PIN SPDT switches demonstrated small-signal isolation in excess of *40dB*. Limited dynamic range of the large-signal W-band characterization system prevented measurements of such high values of isolation. Thus, when the ON-state diode was biased with a small ON-state bias just above the turn-on voltage ($V_{D1}=0.5V$), the isolation at the maximum source power corresponding to $P_{IN}=11dBm$ was *18dB*. Measurements at a lower P_{IN} were impossible due to limitations of the W-band power meter. However, it was possible to study the effect of input power on the switch isolation by biasing the ON-state diode just below the turn-on voltage ($V_{ON}=0.4V$). Increasing the input power turned the diode ON and improved the switching characteristics in agreement with the results obtained at lower frequency for discrete InGaAs PIN diodes, which are presented in the next section.

A comparison between OFF-state power-handling capability of coplanar W-band SPDT and SPST switches fabricated with the same low-parasitics InGaAs PIN-CPW technology is shown in Figure 5.15. The OFF-state diodes in both switches were biased using a *positive* OFF-state $V_{OFF}=+0.2V$, which was intentionally selected near the PIN

diode turn-on voltage of *0.4V* in order to allow a more meaningful measurement. The ON-state diode in the SPDT switch was biased at the practical ON-state bias V_{ON}=*+0.7V*.

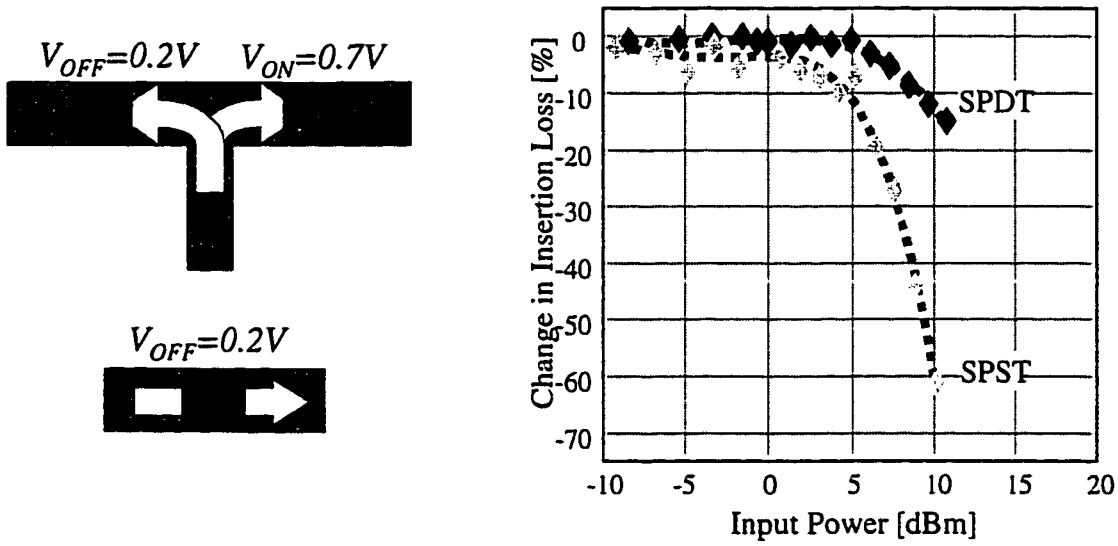


Figure 5.15. Comparison of power-handling capabilities of SPST and SPDT InGaAs PIN diode switches.

When the input power was increased from *–9* to *10dBm* the OFF-state diode of both switches was self-biased by increased input power, which resulted in the degradation of the insertion loss as shown in Figure 5.15. The degradation of the insertion loss in the SPDT switch was smaller and occurred at a higher input power than in the SPST switch. An analysis of the SPDT switch showed that when the input power level was increased, the ON-state diode was self-biased stronger into ON-state conditions, resulting in a reduced rate of degradation of the insertion loss for this circuit.

Overall, the switches demonstrated high OFF-state and ON-state power handling up to *13dBm*. The OFF-state power-handling capability was improved when the OFF-state bias was increased.

5.3.3. Power-Handling Capabilities of Switching InGaAs PIN Diodes

Power-handling capabilities of InGaAs and GaAs PIN diodes were compared using on-wafer power characterization at X-band frequencies where higher-power sources were available. For this purpose, coplanar SPST switches of identical design fabricated using shunt InGaAs and GaAs PIN diodes as switching elements were characterized by

monitoring the insertion loss degradation as a function of biasing conditions and input power level. The results of the study are shown in Figure 5.16.

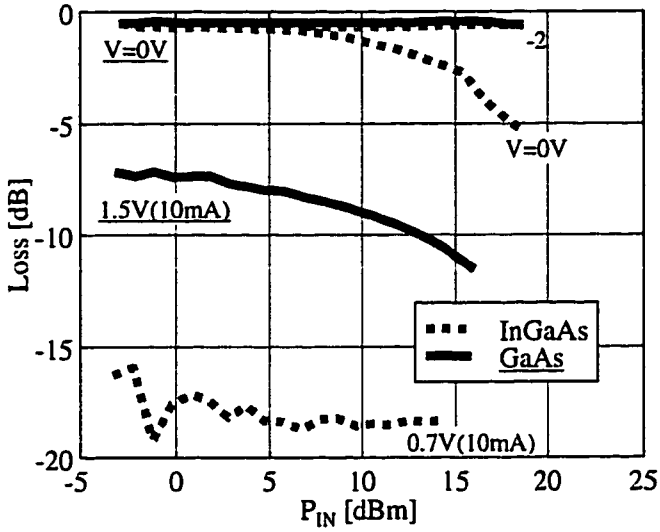


Figure 5.16. Large-signal characteristics of InGaAs and GaAs PIN SPST switches measured at *8GHz*.

The InGaAs switch biased with V_D=*0V* started to self-bias into the ON state when the input power reached *3dBm* while for the GaAs switch the self-biasing was initiated at a larger input power level P_{SB}=*13dBm*. This difference in the zero-bias power handling is caused by a smaller turn-on voltage of the InGaAs diode (*0.4V*) compared with the GaAs case (*1.1V*). The problem of the low turn-on voltage was easily compensated by applying a small negative OFF-state bias to the InGaAs switch, which then demonstrated P_{SB} in excess of *19dBm* for V_D=*-2V*.

Moreover, the InGaAs PIN diode switch demonstrated much higher isolation (by as much as *10dB*) under both low- and high- input power conditions. For purpose of fair comparison, equal ON-state currents (*10mA*) rather than equal ON-state voltages (*0.7* and *1.5V* for InGaAs and GaAs respectively) were used, which still resulted in reduced power consumption and superior performance demonstrated by InGaAs PIN switch.

The large-signal characteristics of the broadband SPST switches employing *10μm*-diameter InGaAs PIN diode in series with a microstrip transmission line were analyzed at *10GHz* to determine the power-handling capabilities of the discrete InGaAs PIN diodes. The results of the study are shown in Figure 5.17.

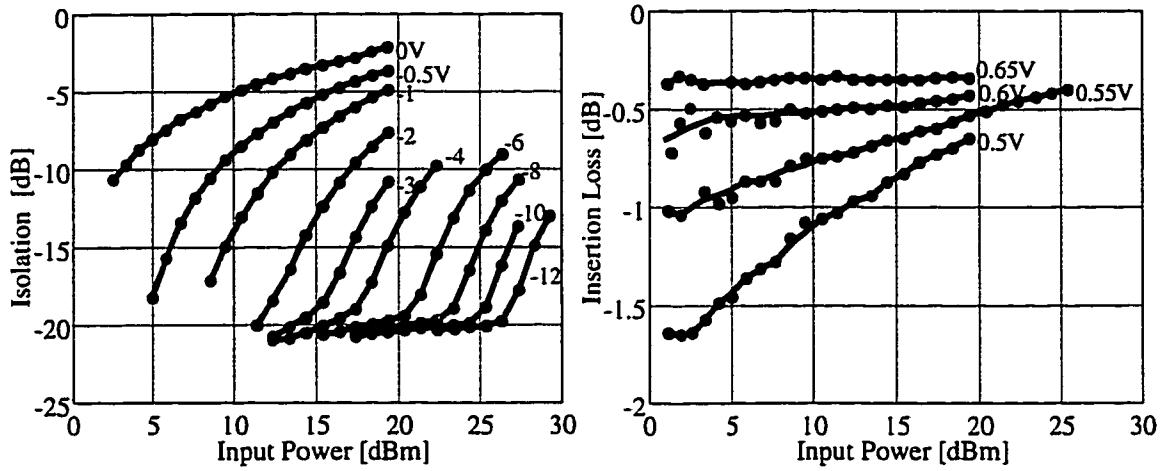


Figure 5.17. Large-signal switching characteristics of series InGaAs PIN diodes

As the OFF-state bias was increased, the OFF-state power-handling capabilities of the investigated InGaAs PIN diodes increased as expected. A *10μm*-diameter InGaAs PIN diode demonstrated a very high OFF-state P_{SB} of *26dBm* at V_{OFF} *of -12V* as shown in Figure 5.17. As the input power was increased, a larger negative bias had to be applied to the OFF-state series PIN diode to preserve its high isolation.

On the contrary, the insertion loss of the series ON-state diode was improved at a higher input power (see Figure 5.17), as the diode was self-biased stronger into the ON-state, resulting in a smaller ON-state resistance and lower insertion loss. A *10μm*-diameter InGaAs PIN diode biased with a low ON-state bias of *0.55V* was measured for up to *26dBm* and demonstrated a *0.5-dB* reduction of the insertion loss, compared with the low- input-power conditions. When the diode was biased at a practical ON-state bias of *0.65V*, the insertion loss of the diode was measured for up to *20dBm* of input power and its value remained constant for all power levels.

The results of the study of InGaAs PIN diodes demonstrated that the power handling of InGaAs PIN switching diodes is adequate for automotive applications (*>20dBm*).

5.4. Evaluation of InGaAs PIN Diode Switching Rates

In this section, another characteristic of high importance for the InGaAs PIN switches' suitability for automotive applications, namely their switching-rate capability,

is addressed. Automotive radars should be able to send and receive a scanning signal many times per second in order to provide an apt response to changing traffic situations. Changes between transmit- and receive- states are performed at a switching rate, which is determined by the response time of the switching elements. State-of-the-art GaAs-based PIN diodes have been reported to have *1-2ns* switching times [74]. Switching times in InGaAs PIN diodes are, however expected to be shorter due to enhanced Auger recombination and higher electron mobility in this material.

In this study, the switching-rate capability of InGaAs PIN diodes was evaluated for the first time by measuring response times of InGaAs PIN diode switches for ON-to-OFF (fall time) and OFF-to-ON (rise time) switching sequences. A combination of high-speed signal-pattern generator and oscilloscope was used for this purpose. The pattern generator was used to generate the input switching signal and the oscilloscope was used to record the resulting voltage waveforms. Shunt InGaAs PIN diode SPST switches were fabricated using coplanar MMIC technology. Switches employing InGaAs PIN diodes with diameters varying from *5* to *15μm* were used in the characterization.

5.4.1. Switching-Time Measurement Setup

The tests were performed under ON-state DC bias and superimposed high-speed pulses. The basics of the testing procedure is shown in Figure 5.18, where the input and output pulses are indicated by $V_i(t)$ and $V_o(t)$, respectively. The diodes under test (*DUT*) were connected in shunt between the pattern generator and the oscilloscope. The pattern generator provided both the bias and switching signal to the diodes. The switching signal was also used to trigger the oscilloscope.

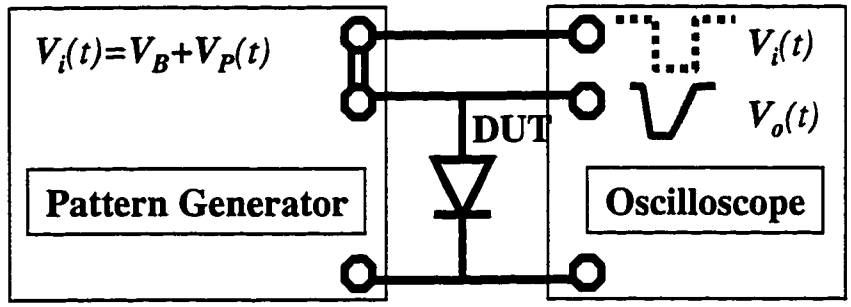


Figure 5.18. PIN switching characterization using a setup consisting of a digital pattern generator, DUT, and high-speed digitizing oscilloscope.

The waveforms of the input and output signals $V_i(t)$ and $V_o(t)$ were recorded by the oscilloscope and the corresponding data were saved on a computer for subsequent analysis. The bias voltage V_B was varied between *-2V* and *+1V*, and the pulse V_P was varied between *-0.5V* and *-2V*, where the minus sign is used to indicate the ON-to-OFF direction of the switching pulse. The switching signal was a square pulse with width τ which was varied between *100ps* and *100ns*. The intrinsic rise/fall time of the generated pulses was *~100ps* and the high-speed digitizing oscilloscope had *50-GHz* bandwidth, which was adequate for the intended tests. The operation of the measurement setup can be explained by examining the operation of the PIN for the three cases shown in Figure 5.19.

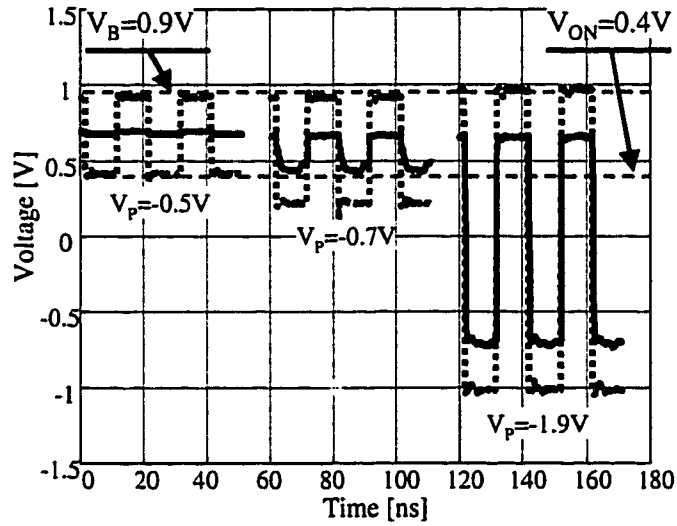


Figure 5.19. Input (dashed line) and output (solid line) voltage waveforms were obtained in the switching experiment with V_B=*+0.9V*, V_P=*-0.5*, *-0.7*, and *-1.9V*.

The input and output signals were obtained using the setup of Figure 5.18 and the results are shown in Figure 5.19. The figure also shows the levels of the bias V_B=*0.9V* and the PIN turn-on voltage V_{ON}=*0.4V*, the value of which defines the transition between ON and OFF-states. When the pulse V_P was *-0.5V*, the InGaAs PIN diode was in the ON-state at all times ($V_i(t)>V_{ON}$), and the signal was not transmitted. This was confirmed by the absence of output pulses for this case as shown on the left of Figure 5.19. When V_P was increased to *-0.7V*, the InGaAs PIN diode was turned OFF for a part of the pulse duration. There were output pulses for this case as shown in the middle of Figure 5.19. However, the shape of the output pulses was distorted due to the switching delays caused by the

diode. The switching time was visibly reduced for the third case when a larger V_P of *-1.9V* was used as shown on the right of Figure 5.19.

The recorded waveforms were analyzed by computer programs. Switching times were extracted from the waveforms according to standard *IEEE* algorithms [75]. Rise (*fall*) time τ_R (τ_F) was defined as the time it takes for voltage to rise (*fall*) from *10%* (*90%*) to *90%* (*10%*) of the pulse amplitude. The rise time corresponded to InGaAs PIN switching from OFF to ON-state and the fall time corresponded to switching from ON to OFF-state for the shunt PIN switches under study.

5.4.2. Influence of Pulse Amplitude on Switching Times

The dependence of switching times on the pulse amplitude was investigated for small (*5μm*-diameter) and large (*15μm*-diameter) InGaAs PIN diodes and is shown in Figure 5.20. The rise times τ_R and the fall times τ_F were evaluated for the conditions when the pulse amplitude $V_A \equiv |V_P|$ was varied between *0.7V* and *1.9V* while the bias voltage V_B was kept constant at *0.9V*.

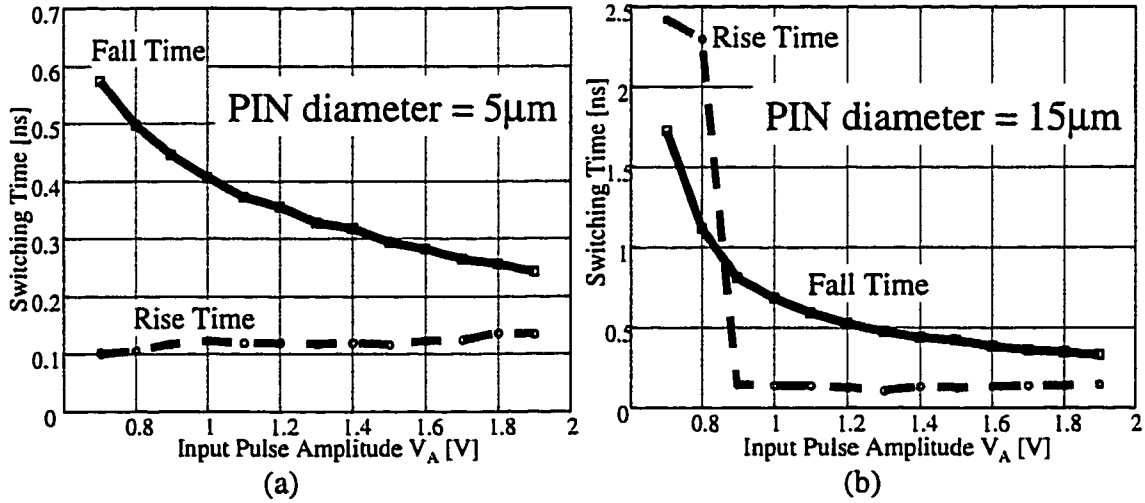


Figure 5.20. Dependence of switching times on the pulse amplitude for (a) small and (b) large InGaAs PIN diodes.

The fall time decreased gradually when the pulse amplitude was increased in agreement with theoretically expected trends. During the ON-to-OFF switching, electrons and holes are swept out of the I-layer by a pulse of negative amplitude. The larger the pulse amplitude, the more carriers are removed during the initial "sweep-out" stage of

switching, and the shorter is the switching time. The fall time can be related to the magnitude of the switching pulse by:

$$\tau_F \approx \tau \log(1 + I_{ON}/I_R) \tag{5.4}$$

where τ is the ambipolar minority-carrier lifetime, I_{ON} is the ON-state current, and I_R is the reverse sweep current, which is proportional to the pulse amplitude V_A since forward and reverse currents are limited by the same input resistance of the oscilloscope. The ambipolar minority-carrier lifetimes of *~1.4ns* and *~1ns* were evaluated for the I-layer of InGaAs using the relationship between τ_F and V_A in large and small InGaAs PIN diodes, respectively.

The rise time dependence on the pulse amplitude for small InGaAs PIN diodes is shown in Figure 5.20(a). The injection of carriers into the I-layer during the OFF-to-ON switching occurred very fast as demonstrated by the short rise times (τ_R*<150ps*). The fast switching was due to the high electron mobility of InGaAs and the small thickness of the I-layer used in these diodes, which results in shorter charging and transit times.

The rise time dependence on V_A for large InGaAs PINs is shown in Figure 5.20(b). When the pulse amplitude V_A was larger than *1V* the rise time was also very short τ_R*<150ps*. However, when the pulse was smaller than *1V*, the number of carriers supplied by the pulse was not sufficient to reach the ON-state by injection. In this case, the steady-state carrier distribution in the I-layer was established through a slower process assisted by diffusion and space-charge generation also known as conductivity-modulation lag [76]. The latter is illustrated by an increase of the rise time to τ_R*=2.4ns* for the case of large InGaAs PINs and small pulse amplitude (V_A*<1V*) as shown in Figure 5.20(b).

5.4.3. Dependence of Switching Time on Diode Size

The switching time dependence on diode diameter is illustrated in Figure 5.21 for switching with small and large pulses. When the switching pulse was small (V_A*=0.9V*), the number of carriers supplied by the pulse was not sufficient to fully turn on diodes with a diameter larger than *10μm*. The rise time of the large diodes was limited by the conductivity-modulation constant (τ_R*=2.4ns*) as shown in Figure 5.21(a). On the other

hand, the carrier supply was sufficient for diodes smaller than *10μm*, which allowed fast turn-on by carrier injection with τ_R<*150ps*.

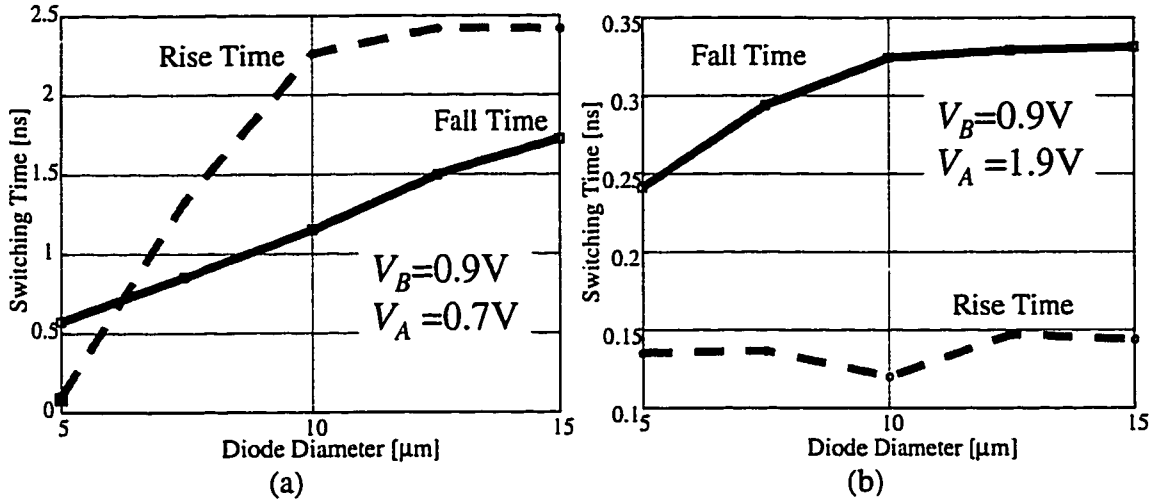


Figure 5.21. Dependence of switching times on InGaAs PIN diode size for (a) small and (b) large pulse conditions.

When the pulse was large (V_A=*1.9V*), the carrier supply was adequate to reach ON-state by injection even in larger diodes and the rise time was limited by the input pulse (τ_I ~ *100ps*) as shown in Figure 5.21(b).

The fall time τ_F was also limited by the supply of carriers in the case of small-pulse switching (V_A=*0.9V*). The decrease of τ_F from *1.8ns* to *0.6ns* shown in Figure 5.21(a) was due to increased current density in smaller diodes. When the pulse was increased to *1.9V* (Figure 5.21b), the fall time decreased until it became limited by the ambipolar minority-carrier lifetime τ. The lifetime was evaluated using (5.4) and τ=*1.4ns* was found for diodes with diameters larger than *10μm*. This value is believed to be the bulk lifetime of the I-InGaAs and is in good agreement with the lifetime obtained by fitting to DC characteristics as was discussed in Chapter 3. The lifetime was decreased to τ=*1ns* in smaller diodes. The decrease is attributed to an increased role of surface recombination. The observed decrease of the minority-carrier lifetime can be correlated with the changes in the slope of the R-I^{-1} (resistance-current^{-1}) characteristics shown in Figure 5.22. The slope increases for diodes with small diameters indicating better conductivity, which also leads to an increased current density, referred to earlier. Such an

increase has been suggested to indicate presence of surface effects [77] and suggests a possibility of employing small-size PIN diodes in high-speed switching applications.

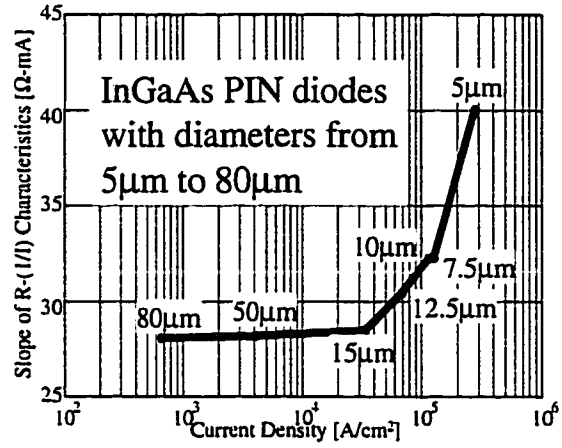


Figure 5.22. The dependence of the slope of R-1/I characteristics on the diode size for InGaAs PIN diodes.

The high-rate switching capability evaluated by the above experiments on InGaAs PIN diodes was validated by characterizing a coplanar Ka-band SPST switch made with a shunt *5μm*-diameter InGaAs PIN diode. *100ps*-wide *1.8V*-large pulses (V_B=*1V*) were used for these tests. The input and output waveforms obtained during the switching experiment are shown in Figure 5.23.

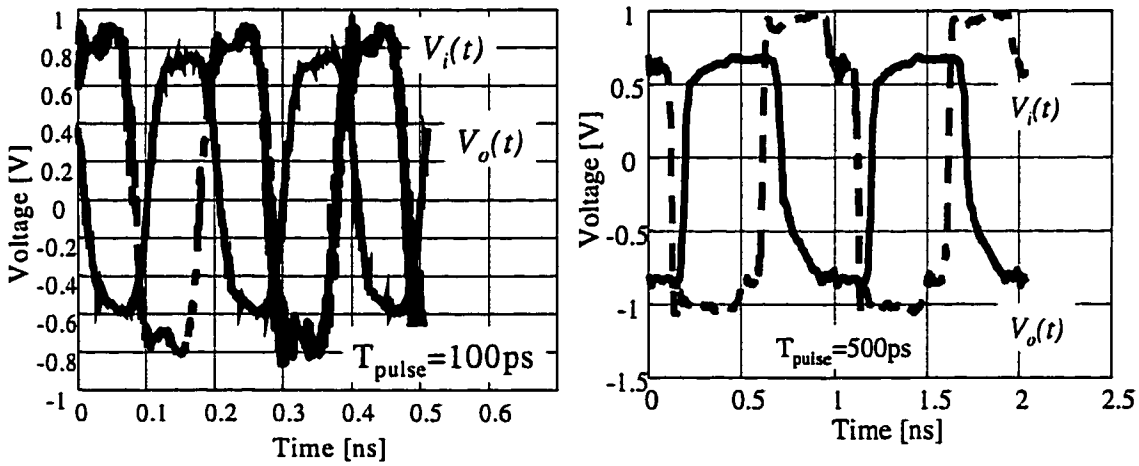


Figure 5.23. Input $V_i(t)$ and output $V_o(t)$ waveforms of *5μm*-diameter InGaAs PIN diode SPST switch at high-switching rate of *5Gps* and *1Gps*.

When diodes were driven with a *5GHz* signal the rise and fall time were *41ps* and *86ps*, respectively. Such fast switching was obtained at the cost of sacrificing some of the

insertion loss and isolation because the ON and OFF-states could not reach steady-state conditions for the duration of the *100ps*-long pulses. When the pulse width was increased to *500ps*, corresponding to a high switching rate of *1Gps*, the diodes were fully turned on and off within the duration of the pulse.

Overall, InGaAs PIN diodes appear to present short switching times (fall time τ_F=*250ps* and rise time τ_R=*130ps*). Switching in large diodes is limited by bulk time constants, while faster switching in small diodes is due to increased surface effects. These features lead to high switching-rate capability of *5Gps* for InGaAs PIN diodes.

5.5. Conclusions

An on-wafer large-signal characterization system has been developed for W-band frequency applications. The system is computer-controlled and employs a high-precision electromechanical W-band tuner. It is intended for load-pull and power saturation characterization of millimeter-wave devices, as necessary for the development of power amplifiers, switches, and other components for W-band applications. Its application to obtaining constant-loss contours as well as power saturation characteristics of InGaAs PIN diode switches is demonstrated at the W-band frequencies of *77GHz* and *102GHz*.

W-band InGaAs PIN diode switches did not demonstrate any degradation of large-signal characteristics for input powers up to the maximum available from a W-band source power of *+12dBm* at *102GHz*. Power-handling capability of W-band InGaAs switches was comparable to that of GaAs and exceeded *20dBm* when the InGaAs switch was biased with a practical OFF-state bias of *–2V*. A discrete *10μm*-diameter InGaAs PIN diode measured at *10GHz* demonstrated a high isolation of *20dB* and a low insertion loss of *0.5dB* under a very high input power of *26dBm*.

Experimentally measured power-handling capabilities of InGaAs PIN switching diodes confirmed their excellent suitability for high-power (>*20dBm*) high-frequency (>*77GHz*) signal-control applications.

The switching time characteristics of InGaAs PIN diodes were studied using high-speed signal-pattern generator. The switching mechanisms were identified and related to material properties. The bulk ambipolar carrier lifetime in the I-layer of InGaAs PIN

diode was estimated to be τ=*1.4ns*, in good agreement with earlier estimates, and was *~1ns* in small-size diodes due to surface effects. Ka-band InGaAs PIN diode switches with *5μm*-diameter diodes demonstrated very short switching times (*130ps* and *250ps*) and allowed operation with a high switching rate of *5Gbps*.

CHAPTER 6

GaN-BASED HETEROJUNCTION FETs FOR SWITCHING APPLICATIONS

While excellent switching characteristics have been demonstrated in the previous chapters using InP-based PIN diodes, monolithic integration of InGaAs PIN diodes with the InP-based HEMT MMICs requires adjustments in growth and fabrication technology. FET-based switches, on the other hand, can be easily integrated on the same chip with transmit and receive MMICs employing FETs or HEMTs. Section 6.1 of this chapter addresses basic design and characteristics of FETs employed for switching applications.

While FET switches made with conventional III-V semiconductors offer ease of integration with the mainstream MMIC technology, their poor power-handling capabilities limit their use in high-power switching applications, such as automotive and imaging radars. Power-handling capabilities of FET switches can be improved by use of wide bandgap GaN-based materials due to greater electrical strength and higher carrier saturation velocity in nitrides compared with conventional III-Vs. High-power potential promised by these materials is addressed in Section 6.2 and appears to be supported by excellent microwave power characteristics recently demonstrated by GaN-based heterojunction field-effect transistors (HFETs) [78].

While excellent power results have been reported on AlGaN/GaN HFETs, no systematic analysis regarding small- and large-signal characteristics for power GaN-based HFETs or their scalability was available. Section 6.3 presents a study of switching characteristics, large-signal performance, and scalability of AlGaN/GaN power HFETs with gate widths up to *1mm*, as desirable for their power MMIC applications.

Most of the effort on GaN-based electronics is currently focused on development of HFETs, which use Schottky-barrier gate contact for charge control. However, the power capability of GaN-based HFETs can be further enhanced by means of increasing

the Al fraction in the donor layer. The AlN/GaN MIS approach explored in this work opens the possibility of utilizing devices with a very wide bandgap material under the gate and thus obtaining good microwave power performance. Section 6.4 reports, for the first time, good interface properties of AlN/GaN heterostructures and very promising electrical performance obtained from AlN/GaN HFETs built on these epitaxial layers.

6.1. Design and Operation of Switching FETs

A cross-sectional schematic of a switching field-effect transistor (FET) is shown in Figure 6.24. The device has three contacts: source, drain, and gate, which are deposited on the top of a thin n-type conductive channel layer. The drain and source are ohmic contacts, while the gate contact is isolated from the channel by a depletion region as shown in the figure. Important design parameters of the FET include its gate length L, the gate width W, the channel thickness t_{CH}, and the channel doping N.

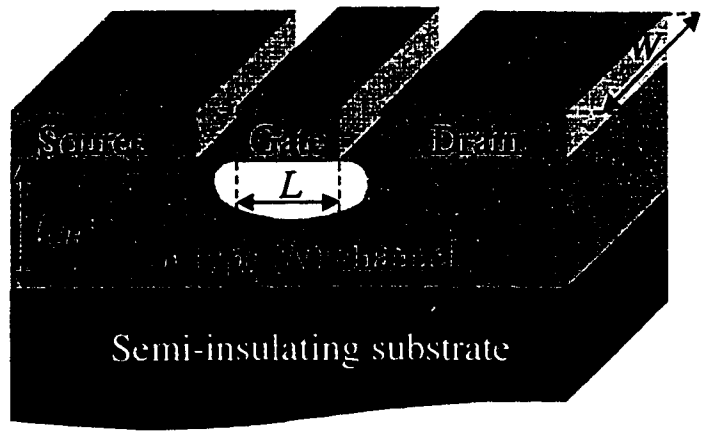


Figure 6.24. Schematics of a switching FET in the ON and OFF states with their corresponding small-signal equivalent-circuit elements.

The switching action of the FET is based on the possibility of controlling conductivity of the channel between the source and drain contacts by the gate bias. When the gate bias is zero or positive ($V_{GS} \geq 0V$), the depletion region underneath the gate contact is narrow and the channel resistance is small (ON-state). An application of a negative V_{GS} causes the depletion region to grow and, thus, the thickness of the conductive channel is reduced. The minimal gate-source voltage at which the channel is completely pinched off (OFF-State) is called the threshold voltage or V_T.

6.1.1. Basic Characteristics of Switching FETs

Since FETs are majority-carrier devices, high-frequency and low-frequency I-V characteristics follow same general trends (ignoring for a moment ballistic overshoot effects possible in short-gate devices). Typical I_D-V_{DS} characteristics as a function of the control bias V_{GS} are shown Figure 6.25. If the input power of the high-frequency signal is low, then the $\tilde{V}_{DS}$ amplitude (V_{DS}) is also small, and the I-V characteristics are ohmic.

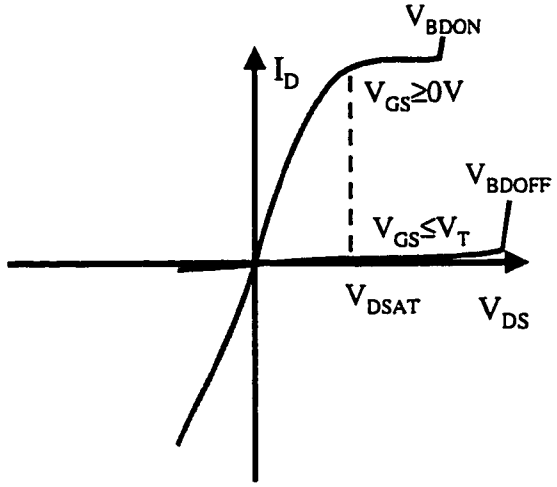


Figure 6.25. I_D-V_{DS} characteristic of a switching FET shows the difference in the channel resistance under the ON- and OFF-state biasing conditions.

At high input power (high V_{DS}), the lateral electric field in the channel (drain-to-source) is increased and the electron velocity becomes saturated due to increased scattering of high-energy electrons. At the same time, an increase of V_{DS} also leads to additional expansion of the depletion region near the drain (and eventual channel pinch-off) since a part of the drain-source bias is also applied across the gate and drain contacts. These effects of velocity saturation and channel pinch-off are responsible for the saturation of drain current at drain bias above V_{DSAT} as shown in Figure 6.25.

In the short-gate devices, transport of electrons through the high-field area of channel may occur ballistically. This means that electron transit through the channel velocity happens in a shorter time than it takes high-energy electrons to scatter and settle at the steady-state saturation velocity v_{SAT}. This energy-relaxation time τ_{ER} is estimated to be $\sim 10ps$ for GaAs [79], which means that ballistic effects become important for gate lengths $L < v_{SAT} \times \tau_{ER} \approx 0.7\mu m$. Velocity overshoot effects are predicted for GaN-based

FETs with gate lengths $L<0.3\mu m$ [80] due to higher saturation velocity ($2\times10^7 cm/sec$) and shorter energy-relaxation times ($1.5ps$) as discussed in detail in Chapter 7.

When the input power increased even further, the presence of very high electric field in the channel leads to an uncontrollable increase of the drain current and breakdown of normal operation. Typically, the ON-state breakdown occurs via impact-ionization effects since there are many carriers in the channel. In the OFF-state, the channel is depleted and the breakdown occurs at a higher V_{DS} as shown in Figure 6.25.

Normal small-signal operation of a switching FET takes place is the ohmic region of the I_D-V_{DS} characteristic. The slope of the I-V characteristics in this region is determined by the conductivity of the channel σ:

$$I_D = qNA\times v = qNA\times\mu\times F = qNA\times\mu\times\frac{V_{DS}}{L} = \sigma\times V_{DS} \tag{6.5}$$

where N is the electron concentration in the channel; $v=\mu\times F$ is the electron velocity, which, under the low-field conditions, is given by product of the lateral electric field $F=V_{DS}/L$ and the electron mobility μ; L is the gate length; and $A=W\times t(V_{GS})$ is the channel area given by product of the device width W and the thickness of the undepleted part of the channel $t(V_{GS})$. The latter is a function of the control bias V_{GS} and is given by expression (6.6):

$$t(V_{GS}) = t_{CH} - \sqrt{\frac{2\times\varepsilon\times(-V_{BI}-V_{GS})}{q\times N}} \tag{6.6}$$

where t_{CH} is the total channel thickness, ε is the dielectric constant, V_{BI} is the built-in potential barrier at the channel-gate interface. When the channel is open ($V_{GS}>0$), R_{CH} is small, and when channel is pinched-off ($V_{GS}\leq V_T$), the channel resistance is at its maximum as illustrated in Figure 6.25. The threshold voltage V_T can be found using equation (6.7) if the channel thickness t_{CH}, the channel doping N, and the built-in potential barrier are known:

$$V_T = -\frac{q\times N\times t_{CH}^{\ 2}}{2\times\varepsilon} - V_{BI} \tag{6.7}$$

6.1.2. Design of FET Switches

FETs can be employed as series and shunt switching elements (see Figure 6.26), or as a combination of the two as was demonstrated in [81]. Under either configuration, the gate is connected to the bias supply via a low-pass filter (shown as a biasing inductor in Figure 6.26). Such connection is used to prevent leakage of high-frequency signal ($\tilde{V}_{DS}$) from the gate, while allowing application of the DC or low-frequency control bias (V_{GS}) to the gate. V_{GS} is used to switch the FET between low-impedance ON-state ($V_{GS} \geq 0$) and the high-impedance OFF-state ($V_{GS} \leq V_T$). The drain-source bias of switching FETs is kept at zero ($V_{DS}=0$).

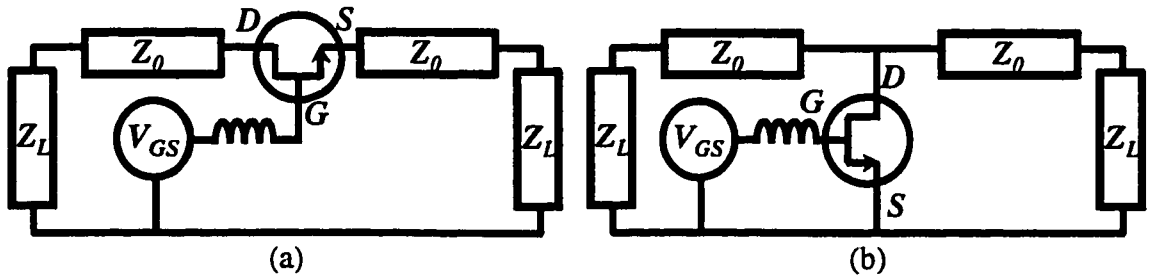
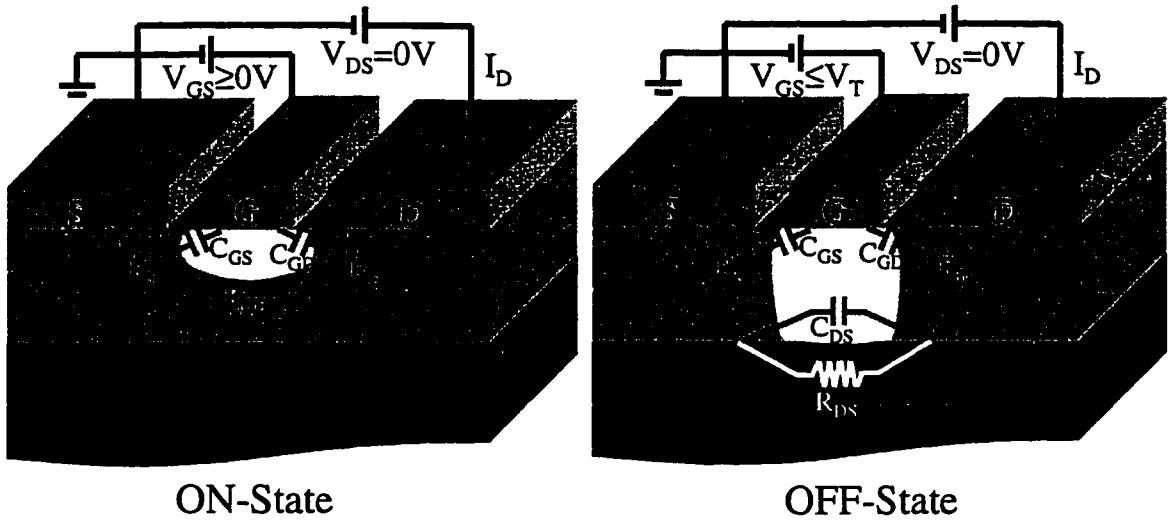


Figure 6.26. SPST FET switches with a) a series FET and b) a shunt FET.

The small-signal high-frequency equivalent circuits of switching FETs are shown in Figure 6.27 for the ON and OFF-states, respectively. The ON-state equivalent circuit includes the ON-state channel resistance R_{CH}, the drain and source access resistances R_D and R_S, respectively, and the gate-source and gate-drain depletion capacitances C_{GD} and C_{GS}, respectively. In the OFF-state equivalent circuit, the ON-state channel resistance R_{CH} is replaced with the OFF-state channel resistance R_{DS} and the OFF-state feedback capacitance C_{DS}.



ON-State OFF-State

Figure 6.27. Schematics of a switching FET in the ON and OFF states with their corresponding small-signal equivalent-circuit elements.

6.1.3. Power-Handling Capabilities of FET Switches

The power-handling capabilities of FET switches are determined by the saturation voltage in the ON-state and by the breakdown voltage in the OFF-state. Thus, to maintain the channel pinch-off conditions of the OFF-state, the large-signal $\tilde{V}_{DS}$ drive ought not to force instantaneous value of $\tilde{V}_{GS} = V_{GS} - \tilde{V}_{DS}/2$ outside the normal OFF-state biasing conditions (i.e. $-V_{BDOFF} < \tilde{V}_{GS} < V_T$). Assuming that an optimal control bias was selected $V_{GS}=(V_T-V_{BDOFF})/2$, the maximum OFF-state RF power handled by a FET switch is given by:

$$P_{OFF} = \frac{(V_{DSMAX})^2}{Z_0} = \frac{(V_{BDOFF} - |V_T|)^2}{2Z_0} \approx \frac{V_{BDOFF}^{\ 2}}{2Z_0} \qquad (6.8)$$

The breakdown of the GaN-based FETs is larger than in conventional III-Vs since the impact-ionization rates in GaN channel are smaller than in GaAs as reflected by their respective critical fields (*400KV/cm* for GaAs and *2MV/cm* for GaN). Thus, OFF-state power handling of FET switches made with GaN-based semiconductors can be as much as *25* times higher than in GaAs switches.

The low-resistance properties of the ON-state FET ($V_{GS}=0V$) are preserved as long as $\tilde{V}_{DS}$ remains within the ohmic region of the I_D-V_{DS} characteristics. The ON-state current saturation can occur either due to the pinch-off of the channel ($V_{DSAT}=V_T$) or due to velocity saturation ($V_{DSAT}=F_{TH}\times L$). Velocity-saturation effects are due to the v-F characteristic, which dictates that electron velocity is saturated at v_{SAT} for fields F above the threshold F_{TH}.

$$V_{DSAT} = \min\begin{cases} V_T \\ F_{TH}\times L \approx \dfrac{v_{SAT}\times L}{\mu} \end{cases} \tag{6.9}$$

GaN-based FETs also offer improved power handling in the ON-state since increased electrical strength of GaN allows design of devices with larger channel doping (N) and higher channel thickness (t_{CH}), while GaN-based HFETs offer significantly larger 2DEG charge density N_S. GaN also is reported to have higher threshold field F_{TH}=*80-150 KV/cm* vs. *3.5KV/cm* for GaAs [82]. Overall, these properties lead to greater V_T and V_{DSAT} in accordance with equations (6.7) and (6.9) and, thus, increased ON-state power handling for GaN-based devices. Experimental results in support of these considerations are presented in Section 6.3.2.

6.2. Power Capabilities of GaN-Based FETs

Most of the effort on FET-based electronics is currently focused on development of HFETs or HEMTs, which take advantage of enhanced mobility of the two-dimensional electron gas (2DEG) and high charge density present in the channel of these heterojunction FETs. The HFET approach was especially beneficial for GaN-based FETs since the properties of AlGaN/GaN heterostructure are strongly influenced by pyroelectric and piezoelectric effects. Thus, the use of Al-rich AlGaN for the heterostructure has been shown to result in higher electron mobility and increased surface density of the 2DEG at the interface of AlGaN and GaN. Electron mobility in 2DEG is higher than the bulk and is less sensitive to the dislocations due to the higher energy of the electrons in the 2DEG [83]. Moreover, electron mobility is reported to increase when the electrons energy at Fermi level gets higher. This effect has been successfully exploited in AlGaN/GaN

HEMTs with Al fractions up to *50%* where mobility up to *1,900cm²/Vsec* has been measured and maximum frequency of oscillations up to *170GHz* has been achieved [83].

Not only the 2DEG electron mobility, but also the 2DEG charge density (N_S) grows with Al fraction as the stress between AlGaN and GaN builds up and the conduction-band discontinuity increases [84]. Thus, N_S can be expected to reach a maximum value of $3x10^{13}cm^{-2}$ for AlN barrier as suggested by a trend line of Figure 6.28 plotted for experimental values of N_S of reference [83]. These values of the 2DEG charge density are significantly higher than what is available with conventional III-V semiconductors due to larger piezoelectric effects and higher electrical strength of III-V nitrides.

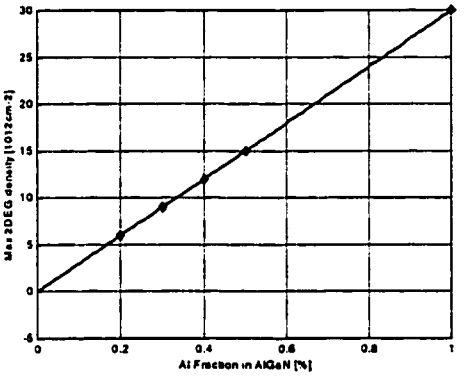


Figure 6.28. 2DEG charge density vs. Al fraction in AlGaN/GaN HFETs

An analysis of the microwave power potential of GaN-based HFETs was performed by comparing their microwave power capabilities to that of GaAs-based devices. The power capability of different semiconductor materials can be compared using figures of merit that evaluate their power handling capabilities. Thus, Johnson's figure of merit

$$JFOM = (F_B v_{SAT}/\pi)^2 \tag{6.10}$$

measures the maximum capability to energize carriers by electric field [85], while Shenai's figure of merit measures the power handling in terms of generated heat [86]:

$$QFI = \lambda\sigma_a \tag{6.11}$$

where λ is the thermal conductivity and σ_a is the conductance of the channel.

To illustrate the advantages of nitride technology these figures of merit calculated for GaN and normalized with respect to GaAs are presented in Table 6.1. Whereas the ability of GaN to energize carriers is *100* times better than that of GaAs, its power handling in terms of generated heat varies depending on the choice of substrate. Thus, Shenai's figure of merit *QF1* is designed to evaluate the power handling under the assumption that the generated heat is removed through a substrate made of the same material as the device. However, this is not the case for GaN-based HFET technology, which is being developed on sapphire and SiC substrates with thermal conductivity of *0.3W/cm/K* and *4.5W/cm/K*, respectively vs. *1.3W/cm/K* for GaN.

Table 6.1. High-Power Capability Figures of Merit for GaN Normalized to GaAs

Semiconductor Figures of Merit (FOMs) Normalized to GaAs	GaAs	GaN grown on	
		Sapphire	SiC
Capability to energize carriers (Johnson's $JF = (F_B v_{SAT}/\pi f)^2$)	*1*	*100*	
Thermal power handling with native substrate ($QF1 = \lambda\sigma_a$)	*1*	*22*	
Thermal power handling with hetero substrate ($QFS = \lambda_{SUB}\sigma_a$)	*1*	*5*	*76*

An extended definition of Shenai's figure of merit: $QFS = \lambda_{SUB}\sigma_a$ can be utilized to evaluate the power handling in GaN-based devices by taking into account the thermal conductivity of the substrate material. While a power-handling improvement of *22* (compared with GaAs) is predicted by *QF1* for GaN-based HFETs, *QFS* shows that, in the case where GaN-based devices are grown on sapphire or SiC, the possible improvement is *5* or *76* times, respectively.

The above considerations are confirmed by excellent power-device results achieved with GaN-based HFETs, which are attributed to increased electrical strength as well as improvements of the electron mobility and high charge density obtained in the GaN-based heterojunction field-effect transistors. Figure 6.29 shows how results obtained on GaN-based HEMTs compare with the results obtained on conventional III-V materials.

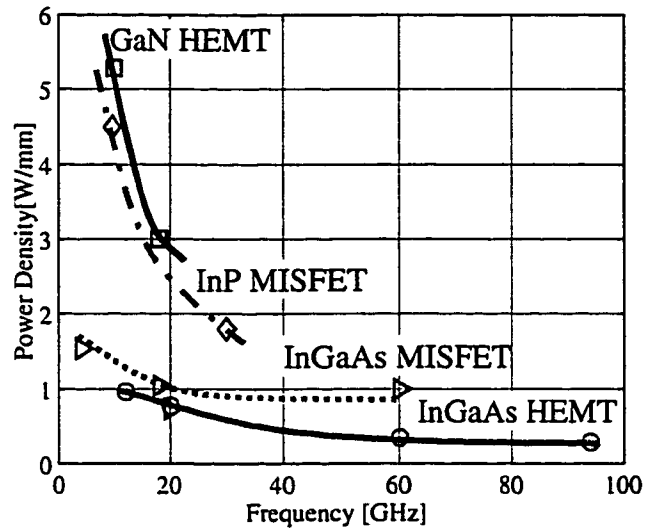


Figure 6.29. Output Power density vs. frequency for GaN- and III-V-based FETs.

Wide-bandgap GaN-based semiconductors demonstrate increased output power density due to a larger breakdown field (F_B=*2MV/cm* vs. *0.4MV/cm* for GaAs) and higher carrier saturation velocity (v_{SAT}=2×10^7*cm/sec* vs. 0.7×10^7*cm/sec* for GaAs). Thus, AlGaN/GaN HEMTs grown on SiC substrates demonstrated record power density at X-band (*7W/mm @ 10GHz*) [78], while AlGaN/GaN HEMTs grown on sapphire had *3W/mm* at millimeter-wave frequency of *18GHz* [87]. The authors of the latter also observe that remarkable improvements in performances were obtained through adoption of high Al contents in the AlGaN layer [88], which is in agreement with the arguments regarding high charge density for Al-rich AlGaN/GaN heterostructures. Moreover, the use of wide bandgap semiconductors in power MMICs not only increases the output power, but also extends the temperature tolerance and the radiation hardness of the circuits. The latter is corroborated by recently demonstrated operation of GaN-based HFETs at *750°C* [89]. Overall, AlGaN/GaN HFET appear to be excellent candidates for high-power microwave switches and amplifiers.

6.3. Power Performance and Scalability of AlGaN/GaN HFETs

Excellent small- and large-signal results have been achieved with GaN-based HFETs. However, previous reports indicate that the power density of small test devices (gate width <*0.1mm*) is not realized in larger power devices (*W* of ~*1mm*) [78]. The

results of large-signal characterization of power GaN-based HFETs, presented in this section, demonstrate notable scalability in terms of both output power and output impedance with the gate width. Such scalability studies are important for high-power switching MMIC devices in order to confirm that the amount of power expected from a large-size component is not limited by parasitic effects such as phasing, temperature etc.

The design, DC, and small-signal high-frequency characteristics of GaN-based HFETs are presented in Section 6.3.1. The bias and gate width dependence of the large-signal characteristics are described in Sections 6.3.2 and 6.3.4, while correlation between DC, RF, and power performance are reported in Section 6.3.5.

6.3.1. DC and Small-Signal High-Frequency Characteristics

The AlGaN/GaN HFETs under study consisted of an $Al_{0.3}Ga_{0.7}N$ *50Å*-thick donor layer followed by *30Å*-thick $Al_{0.3}Ga_{0.7}N$ spacer, and a *5000Å*-thick GaN channel. An unintentionally doped *250Å*-thick $Al_{0.3}Ga_{0.7}N$ cap was used for improved contact characteristics, while a GaN thick buffer was employed for improved quality of the materials, which were grown on sapphire substrates. RF-assisted MBE was used for growth and the grown layers are shown in Figure 6.30. Growth and fabrication details are reported in Ref. [90] and [91].

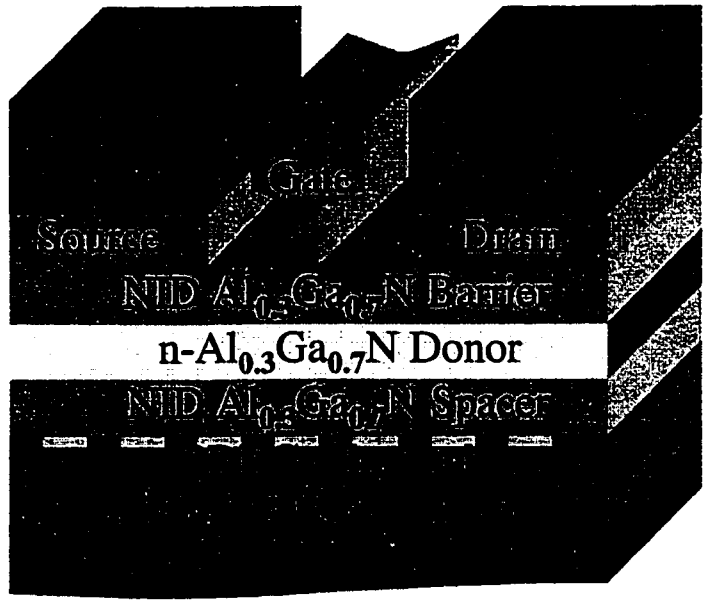


Figure 6.30. Schematics of AlGaN/GaN HFET layers

Power devices with *2*, *4*, *8*, and *10* *100μm*-wide gate fingers (maximum width of *1 mm*) and a drain-source spacing of *2μm* have been investigated. The thermal effects were reduced by employing *30μm*-thick Au-plated heat sinks.

Typical I_D-V_{DS} and transfer characteristics of AlGaN/GaN HFETs are shown in Figure 6.31a and Figure 6.31b for a devices with *200μm* gate width. The maximum drain current shown for these devices was *500mA/mm* while their transconductance (g_m) was *100mS/mm*. g_m reached maximum for V_{GS}=*-5V* (V_{DS}=*7V*) while both the I_D and g_m remained generally unchanged for V_{DS} between *9* and *25V* when V_{GS} was *-5V*.

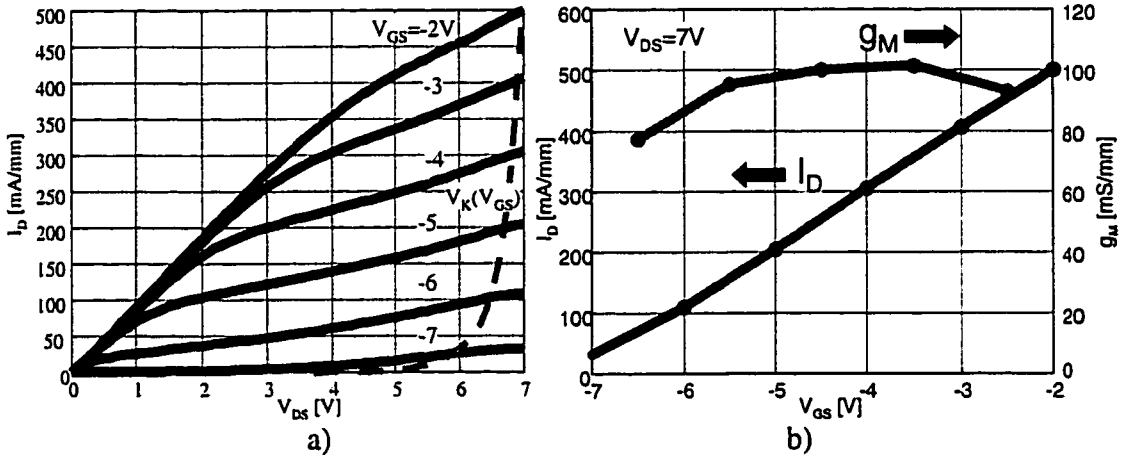


Figure 6.31. I_D-V_{DS} (a) and transfer characteristics (b) of AlGaN/GaN HFET with *200μm* gate width

Current-compliance limitation of the semiconductor-parameter analyzer used for obtaining these data did not allow application of gate voltages larger than *–2V*. The device pinch-off voltage was *–8V*. The ON-state drain-source breakdown was found to be higher than *50V* while drain current saturation occurred at saturation voltage (V_{DSAT}) as shown in Figure 6.31a.

Small-signal S-parameters of AlGaN/GaN HFETs with varying gate widths were measured between *0.5* and *25.5GHz*. The current-gain cutoff frequency (f_T) and maximum oscillation frequency (f_{MAX}) extrapolated from the S-parameters for different bias conditions are shown in Figure 6.32.

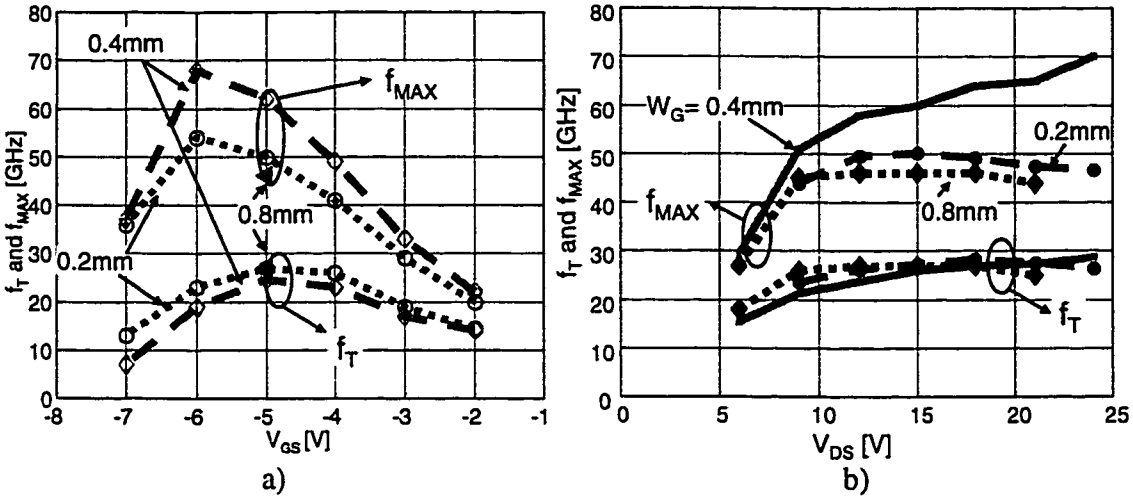


Figure 6.32. Bias dependence of f_{MAX} and f_T for AlGaN/GaN HFETs with various gate widths

The figure shows that f_T and f_{MAX} were maximized for V_{GS} between *–4* and *-6V* (V_{DS}=*15V*). f_T and f_{MAX} slowly increased with drain-source voltage for V_{DS}>*5V* when V_{GS} was fixed at *-5V*. f_T was *27GHz* for most devices while f_{MAX} varied between *45* and *70GHz*.

Small-signal S-parameters were also used to extract equivalent-circuit elements under optimal biasing conditions (V_{DS}=*15V* and V_{GS}=*-5V*). The small-signal equivalent circuit used for extraction is shown in Figure 6.33 and is very similar to the equivalent circuit of a switching FET presented in Section 6.1.2. However, under active biasing conditions, the FET equivalent circuit has one additional element representing the amplifying function of the FET — a voltage-controlled current source $g_m V_{GS} e^{j\omega\tau}$, where g_m is the transconductance and τ is the phase factor added by the transit-time delay.

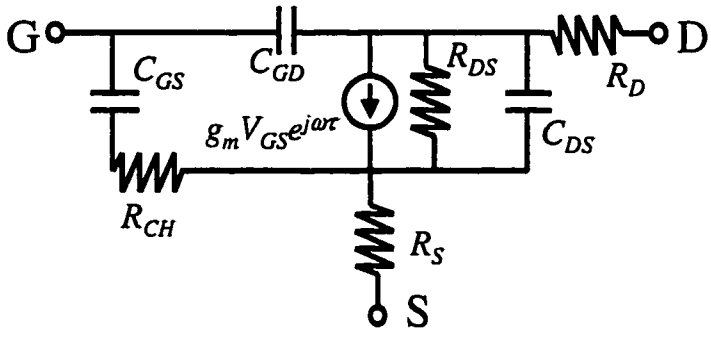


Figure 6.33. Small-signal equivalent-circuit of common-source AlGaN/GaN HFET

The values of equivalent circuit elements obtained by circuit optimization in microwave simulator Libra are listed in Table 6.2. The contact resistance of *0.5Ωmm* obtained from TLM measurements [90] was in agreement with the high-frequency source and drain resistance (R_D and R_S) obtained by fitting the S-parameter data.

Table 6.2. High-Frequency Small-Signal Equivalent Circuit Parameters of HFETs (V_{DS}=*15V* and V_{GS}=*-5V*)

Width [μm]	I_D [mA]	g_m [mS]	C_{GS} [fF]	C_{GD} [fF]	C_{DS} [fF]	R_{DS} [Ω]	R_{CHI} [Ω]	τ [ps]
200	*36*	*19*	*106*	*25*	*95*	*1095*	*10*	*1.7*
400	*52*	*35*	*220*	*47*	*187*	*391*	*7*	*2.4*
800	*130*	*83*	*412*	*102*	*297*	*136*	*1.7*	*1.9*

The extrinsic RF transconductance demonstrated notable scaling with the gate width ($g_m \approx$ *100mS/mm*) and agreed well with the transconductance extracted from DC measurements across a wide range of gate-source voltages as shown in Figure 6.34.

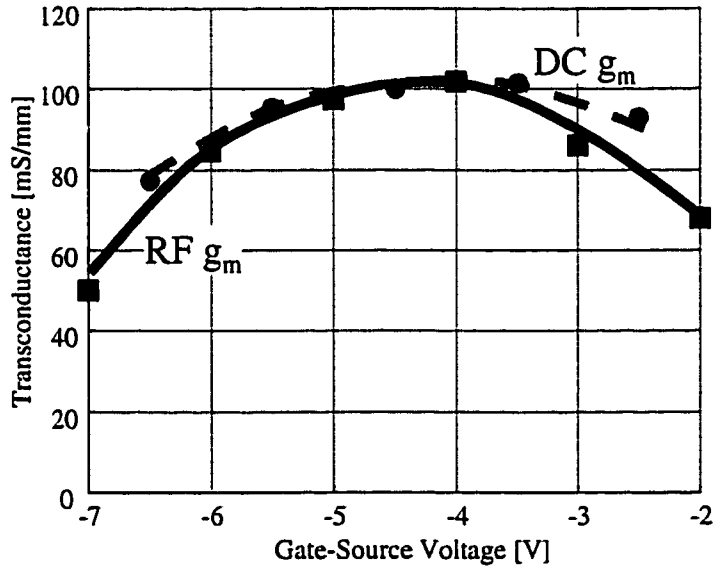


Figure 6.34. Dependence of DC and RF transconductance on V_{GS} for *0.2mm* AlGaN/GaN HFETs

Although the exact features of the devices at intermediate frequencies are not known at this stage, the agreement between the DC and RF values of transconductance suggest the presence of limited frequency dispersion under small-signal excitation. g_m dispersion with frequency is usually associated with the presence of traps in the channel

or at the channel-barrier interface as shown in previous reports on other types of heterostructure FETs [92]. The variations in the time response of traps may cause transconductance values under RF excitation, which are smaller than under DC conditions. The excellent agreement of DC and high-frequency transconductance values, observed in this study, supports the fact that the investigated AlGaN/GaN HFETs grown by RF-assisted MBE demonstrate minimum small-signal dispersion effects, as discussed more extensively in Section 6.3.5. Characteristics of this type are of prime importance in obtaining good high-frequency and power performance from GaN-based HFETs.

It was also observed that the output drain-source capacitance C_{DS}, the input gate-source capacitance C_{GS}, and the feedback drain-source capacitance C_{GD} scaled linearly with the gate width. The values of C_{GD}, C_{GS}, and C_{DS} capacitance are *120fF/mm*, *540fF/mm*, and *440fF/mm* respectively. This good scalability of these devices is very important for their switching applications.

6.3.2. Switching Characteristics of GaN-based HFETs

High-frequency switching characteristics of GaN-based HFETs were evaluated by converting the S-parameters measured for devices in common-source configuration to the common-gate S-parameters. This transformation of the S-parameters is made automatically by *HP EEsof Libra* microwave simulator. The common-gate S-parameters of a *0.2-mm* AlGaN/GaN HFET measured in the ON-(V_{GS}=*0V*) and OFF-state (V_{GS}=*-8V*) are shown in Figure 6.35. In the ON-state, these devices showed low minimum insertion loss of *~1dB* and a small corresponding return loss of about *-20dB*. In the OFF-state, the maximum isolation was *~25dB*, while reflection loss was less than *0.2dB*. While the bandwidth for discrete devices was small (isolation decreased to *–10dB* at *5GHz*), switches made of AlGaN/GaN HFETs can be used at higher frequencies by employing transmission-line quarter-wavelength impedance-transformer sections as described in Chapter 4 for InP-based PIN diode switches.

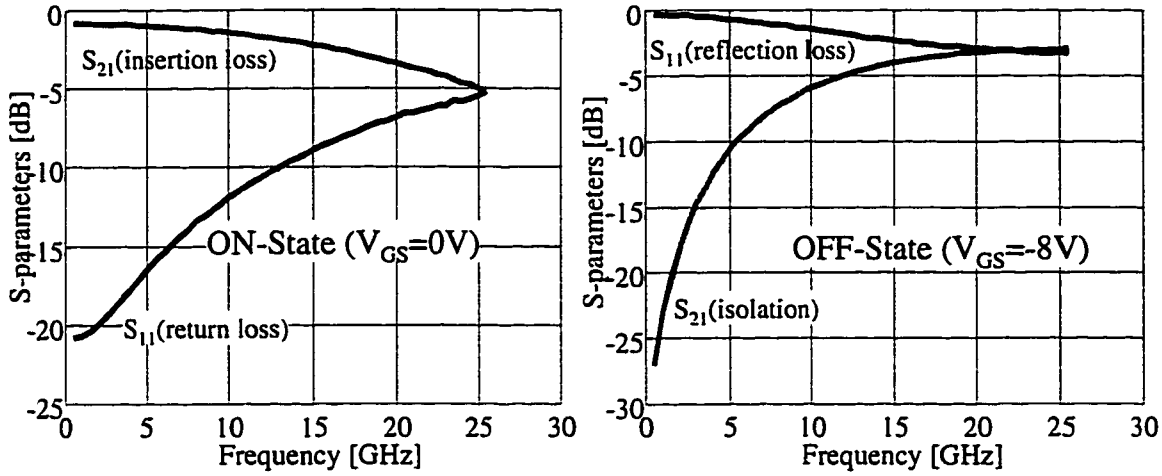


Figure 6.35. Common-Gate S-parameters of GaN-based HFETs

High-frequency switching characteristics of GaN-based HFETs were modeled using equivalent circuits models introduced in Section 6.1.2. The values for equivalent-circuit elements were found by fitting experimental and simulated S-parameters and the results are shown in Figure 6.36. GaN-based HFETs had R_{ON} of 6Ω and C_{OFF} of $127fF$, corresponding to switching-cutoff-frequency figure of merit f_{CS} of ~$200GHz$. Parasitic gate-source and gate-drain capacitances were $C_{GS}=55fF$ and $C_{GD}=170fF$, respectively.

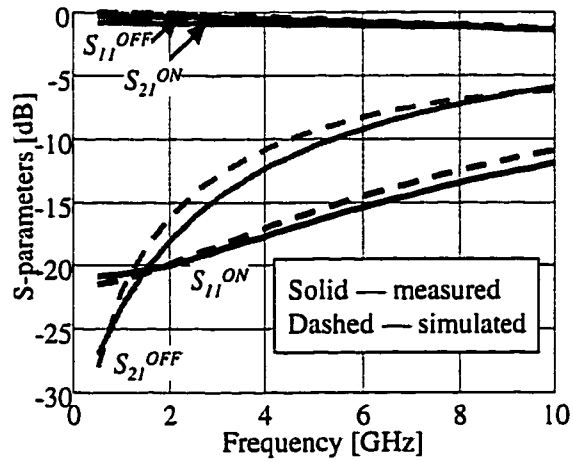


Figure 6.36. Measured and simulated S-parameters of GaN-based HFETs

X-band power saturation measurements were performed in order to compare power-handling of GaN-based and InP-based HFETs. For this purpose, a single-port load-pull technique was employed. A schematic of the single-port load-pull setup is shown in Figure 6.37. The setup consists of a signal source (P_S), input and output power sensors (P_{IN} and P_{OUT}, respectively), a circulator, an electromechanical tuner, a probe station with

the device under test, and a DC bias supply V_{GS} with high input resistance R_G. The circulator was used to separate the input and the reflected signals and allow independent measurements of the input power P_{IN} and the reflected power P_{OUT} as indicated in the schematic. The purpose of the high-resistance element R_G=*5KΩ* at the input of the bias supply was to prevent leakage of the test signal through the gate.

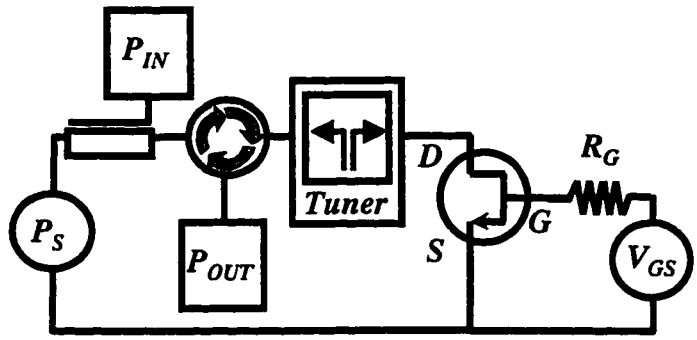


Figure 6.37. Automatic On-wafer Reflection Load-Pull Characterization Setup

The load-pull system was calibrated for on-wafer measurements following a procedure similar to the one outlined in Section of 5.1.2 and applied to characterize monolithic GaN-based AlGaN/GaN HFETs. High-performance InP-based HEMTs fabricated at the University of Michigan [93] were also tested for comparison purposes. The InP-based HEMT layers consisted of InGaAs channel (*15nm*) sandwiched between two InAlAs spacers (*3nm*), followed by delta-doped planes and two InAlAs barriers. Gates were *0.2μm*-long and *2x45μm*-wide. Devices demonstrated g_M=*750mS/mm*, I_{DSS}=*280mA/mm*, and V_{DSAT}≈*0.7V*, and switching cutoff frequency f_T of *~150GHz*.

During power saturation measurements, the tuner was positioned at *50Ω* and the reflected power P_{OUT} was measured as a function of the input power P_{IN} at *8GHz*. The results obtained for InP-based and GaN-based HFETs in the ON-state (V_{GS}=*0V*) and normalized to *1mm*-gate width are shown in Figure 6.38. Under the small-signal conditions (P_{IN}<*10dBm/mm*), the large-signal input impedance Z_{IN} of the devices-under-tests remained constant as demonstrated by a linear P_{OUT}-P_{IN} dependence for both InP- and GaN-based HFETs.

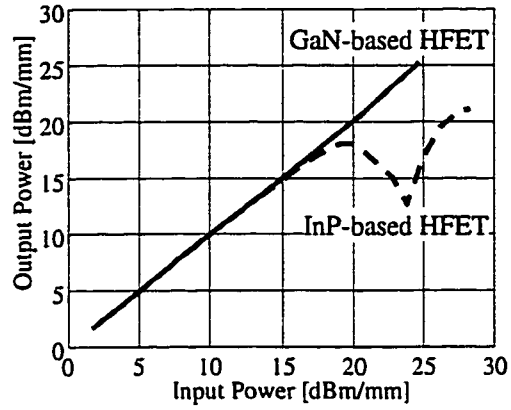


Figure 6.38. Saturation power characteristics of InP- and GaN-based HFETs

As the input power level was increased to *>10dBm*, Z_{IN} of the InP-based HFETs was affected by the large swings of the input voltage (see Section 6.1.3) since the input voltage amplitude V_{IN} exceeds V_{DSAT} for P_{IN}*>10dBm*:

$$V_{IN} = \sqrt{P_{IN} \times Z_0} \tag{6.12}$$

where Z_0=*50Ω* is the characteristic impedance of the characterization system. Due to increased electrical strength of GaN-based HFETs, V_{DSAT} in these devices is *~7V* and, thus, the P_{OUT}-P_{IN} characteristics remains linear for P_{IN} up to *25dBm/mm* as demonstrated by Figure 6.38.

These considerations were corroborated by experimental evaluation of Z_{IN} as a function of the input power for GaN- and InP-based HFETs. The large-signal input impedance was found by evaluating constant-loss contours for the output power reflected from the HFETs. The minimum-reflection tuner position corresponds to the complex conjugate matching between the tuner impedance Z_T and the input impedance of the device $Z_{IN}=Z_T^*$.

The constant-loss contours evaluated for InP- and GaN-based HFETs under small- and large-signal conditions are shown in Figure 6.39. Under small-signal conditions (P_{IN}=*2dBm/mm*), the input impedance of InP-based devices is located on to the left side of the Smith chart corresponding to an input resistance R_{IN} of *~18Ω*. The small-signal input impedance of GaN-based HFET was located closer to the center of the Smith chart and corresponded to a higher input resistance of *~35Ω*. Larger resistance of GaN-based HFETs is due to smaller electron mobility in this material as discussed in Section 6.1.1.

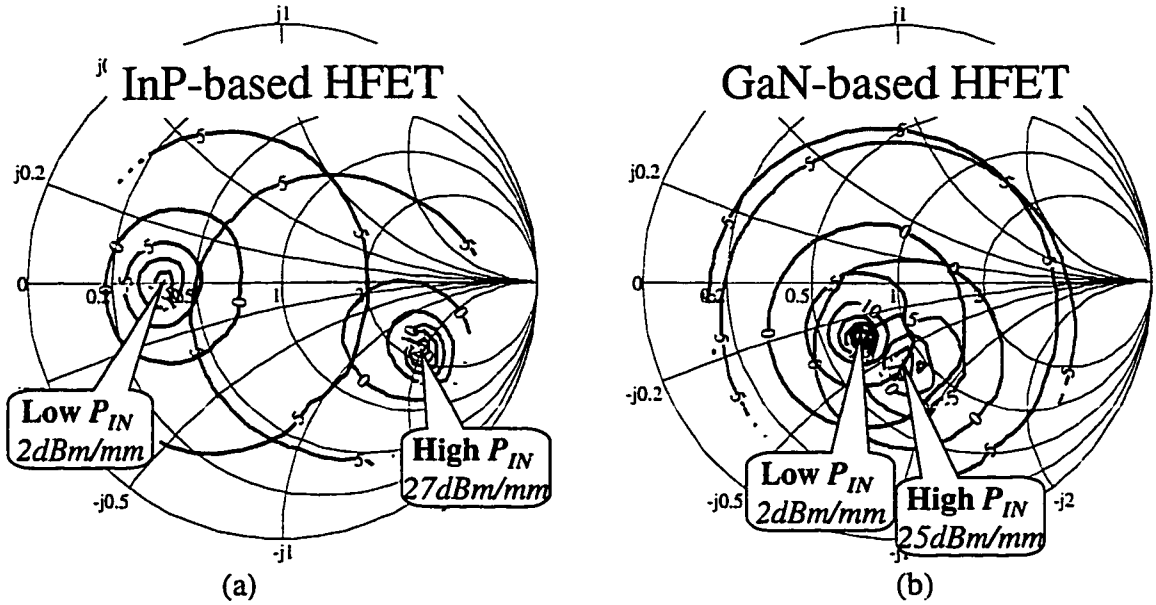


Figure 6.39. Constant-loss contours evaluated for (a) InP- and (b) GaN-based HFETs under small- and large-signal conditions.

However, R_{IN} of InP-based HFETs was severely degraded (*~115Ω*) and constant-loss contours were distorted under large-signal conditions (P_{IN}=*25dBm/mm*) as shown in Figure 6.39a). At the same time, R_{IN} of GaN-based HFETs increased only slightly to *~41Ω* and their constant-loss contours remained uniform and circular as shown in Figure 6.39b).

The results of Figure 6.39a) also explain the non-linear behavior of InP-based HFETs observed in Figure 6.38. The minimum of P_{OUT} at P_{IN}=*24dBm/mm* corresponds to the conditions when R_{IN} of the InP-based HFET is degraded from its small-signal value of *18Ω* to *~50Ω* and, thus, provides matching termination to the input signal source. The output power increases again as R_{IN} increases to *115Ω* at higher input power levels.

Overall, GaN-based HFETs demonstrated improved power-handling capabilities (>*25dBm/mm*) compared with InP-based devices (*~10dBm/mm*). The following sections present experimental results obtained with GaN-based HFETs using two-port load-pull characterization setup (as described in Chapter 5), which allowed more accurate and detailed analysis of their large-signal characteristics and scalability.

6.3.3. Bias Dependence of Large-Signal Characteristics

An automatic on-wafer load-pull system with electromechanical tuners has been employed to obtain P_{OUT}-P_{IN} characteristics of GaN-based HFETs at *8GHz*. Both source and load tuners were positioned to obtain best matching conditions and, thus, maximum gain at an input power level corresponding to *~1dB* gain compression. The bias-dependence of output power, power-added-efficiency, and gain was investigated first as a function of gate bias for fixed drain bias V_{DS}=*21V*. Devices with *1-mm* gate width demonstrated maximum output power (*30dBm*), PAE (*28%*), and gain (*17.6dB*) when the gate bias was set to *–6.75V* as shown in Figure 6.40. Limitations imposed by current handling of the microwave probes and bias tees used in characterization did not allow increasing the gate bias (V_{GS}) above *-6V* as this led to drain current in excess of *500mA*. The maximum output power and large-signal performance is therefore expected to be higher than described by the results of Figure 6.40.

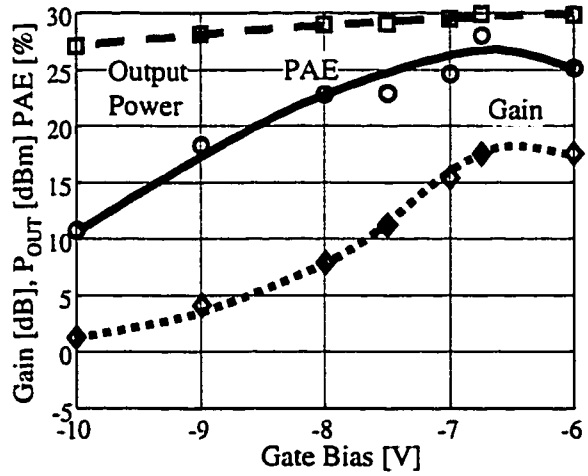


Figure 6.40. Dependence of gain, output power, and power-added-efficiency on gate bias of AlGaN/GaN HFET with *1-mm* gate width

The dependence of output power, PAE, and gain of *1-mm* gate devices on the drain-bias was also investigated and shown in Figure 6.41. For these tests, the gate bias was kept constant at *-5V*. Maximum PAE (*32%*) was obtained for drain bias of *15V*, while maximum output (*30dBm*) occurred at *18V*. Thermal effects are suggested as a cause for reduced efficiency and output power at a drain bias exceeding *18V*.

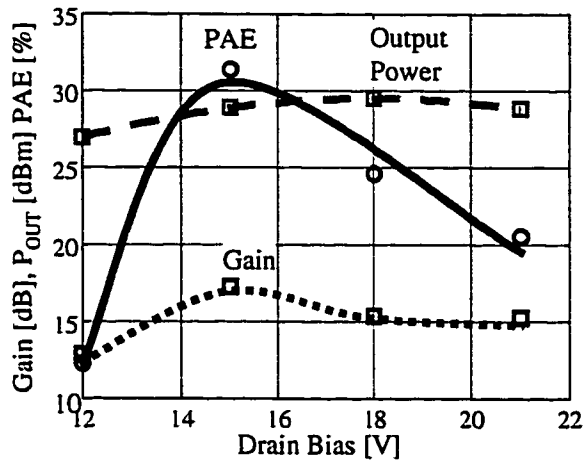


Figure 6.41. Dependence of gain, output power, and power-added-efficiency on drain bias of AlGaN/GaN HFET with *1-mm* gate width

6.3.4. Gate-Width Dependence of Large-Signal Characteristics

The dependence of power performance on the gate width was investigated using AlGaN/GaN HFETs with *2*, *4*, *8*, and *10 100μm*-wide gate fingers. All devices were first biased for maximum gain at an input power level corresponding to *~1dB* gain compression and load terminations corresponding to small signal matching conditions. Then the source and load tuners were adjusted to improve matching and maximize the gain.

P_{OUT}-P_{IN} characteristics of devices with different gate widths are shown in Figure 6.42. Biasing conditions, gain, output power, and power-added-efficiency are listed in Table 6.3. Typical power gain of *17dB* and output power density of *1W/mm* were obtained for devices with *200μm* to *1000μm* gate widths at *8GHz*. The largest output power of *29.9dBm* (*1W/mm*) with associated gain of *4dB* was obtained for devices with *1-mm* gate width.

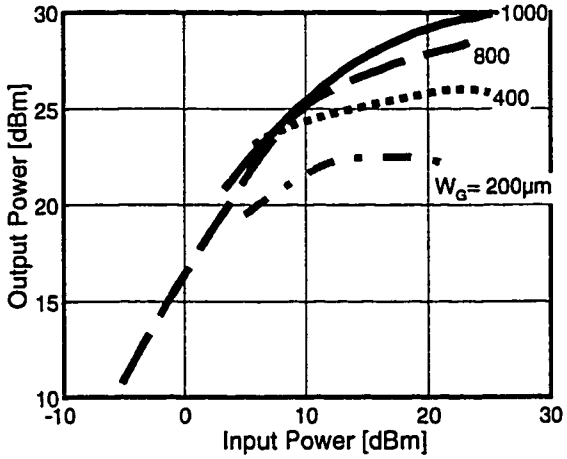


Figure 6.42. Power saturation characteristics of AlGaN/GaN HFETs as a function of gate width

Table 6.3. Power Saturation Characteristics of AlGaN/GaN Power HFETs for Various Gate Widths

Width [µm]	V_{DS} [V]	I_D [A/mm]	V_{GS} [V]	Gain [dB]	$P_{IN\text{-}1dB}$ [dBm]	$Max\ P_{OUT}$ [dBm]	P_{OUT} [W/mm]	$PAE_{\text{-}1dB}$ [%]
200	*15*	*170*	*-4.5*	*15.9*	*-0.8*	*22.5*	*0.89*	*30.3*
400	*12*	*222*	*-4.5*	*17.4*	*3.2*	*26.0*	*1.00*	*28.9*
800	*12*	*186*	*-5.0*	*15.9*	*10.3*	*28.5*	*0.87*	*31.5*
1000	*18*	*168*	*-6.75*	*17.6*	*7.3*	*29.9*	*0.99*	*28.1*

The scalability of AlGaN/GaN HFET power characteristics is illustrated in Figure 6.43. Devices with wider gates showed delayed onset of gain compression, as demonstrated by higher input power at *1dB* gain compression ($P_{IN\text{-}1dB}$) for gate widths up to *800µm*. When the width was increased from *200µm* to *800µm*, $P_{IN\text{-}1dB}$ was increased from *-1* to *10dBm*, P_{OUT1dB} was increased from *20* to *25dBm*, and P_{OUTMAX} is increased from *23* to *30dBm*. The output power density (*~1W/mm*), power-added-efficiency (*~30%*) and gain (*~17dB*) remained constant. P_{IN1dB} and P_{OUT1dB} showed a small decrease in *1-mm* devices compared with *800-µm* HFETs. This is attributed to the limitations in current handling described earlier, which did not allow operation of the *1-mm* devices at their maximum power capacity.

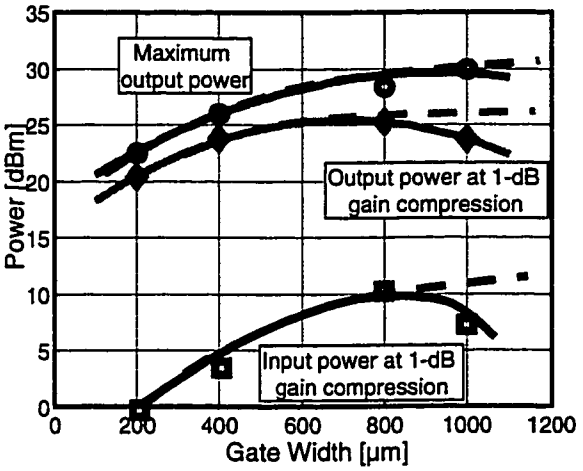


Figure 6.43. Scalability of AlGaN/GaN HFET power characteristics shown by the dependence of output and input power at *1-dB* gain compression on gate width

Constant output power (P_{OUT}) and constant power-added efficiency (*PAE*) contours of AlGaN/GaN HFETs were evaluated using the load-pull system. These measurements allowed determination of loading conditions for maximum output power as necessary for circuit design applications. The contours of AlGaN/GaN HFET with *800-μm* gate under high input power conditions (P_{IN}=*22dBm*) are shown in Figure 6.44.

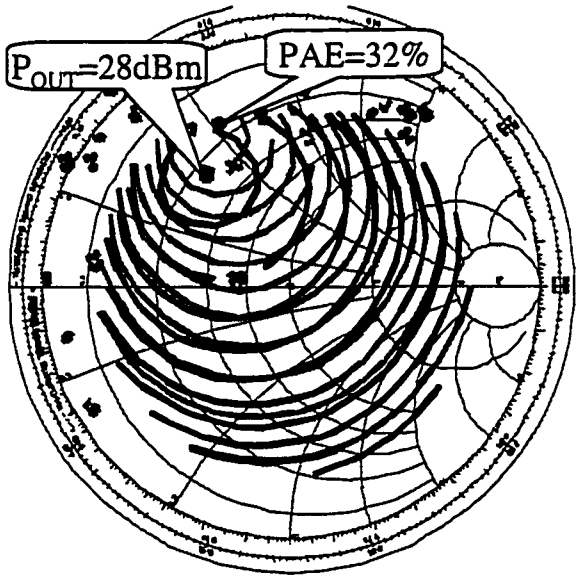


Figure 6.44. Constant output power (P_{OUT}) and constant power-added efficiency (*PAE*) contours for AlGaN/GaN HFET with *800μm* gate width under P_{IN}=*22dBm*, V_{DS}=*12V*, V_{GS}=*-5V*.

The contours were found to remain circular up to power levels corresponding to severe gain compression (*~10dB*). Moreover, when the load impedance was positioned

for maximum P_{OUT}=*28dBm*, the value of (*30%*) was close to its maximum value of *32%*, and the two optimal loads were located near each other on the Smith chart. This positive feature does not necessarily occur in all devices and suggests a possibility of *Class A/AB* power amplifier realization without a considerable tradeoff between output power and power-added-efficiency.

6.3.5. Correlation Between DC, RF, and Power Characteristics

Source-pull and load-pull techniques were used to determine the large-signal output impedance of the AlGaN/GaN HFETs. The output impedance of the devices was determined by the position of the complex conjugate of the optimal load on the Smith Chart. The dependence of the optimal loads under large-signal conditions on the gate width is shown with squares in Figure 6.45. They are in good agreement with the positions of optimal loads under small-signal conditions calculated from small-signal S-parameters and indicated in Figure 6.45 with circles. When the gate width is increased from *200μm* to *1mm*, the optimal load moved as expected along a line corresponding to increased output capacitance and decreased output resistance.

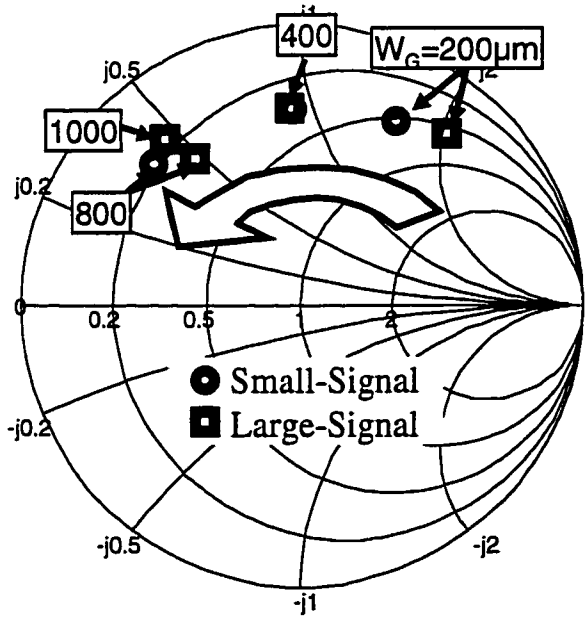


Figure 6.45. Dependence of small- and large-signal output impedance of AlGaN/GaN HFETs on gate widths

It was observed that not only the small- but also the large-signal output capacitance scaled linearly with the gate width. This good scalability is very important for circuit design applications. Moreover, the large-signal output capacitance and resistance were in good agreement with the small-signal values extracted by fitting to S-parameters as shown in Figure 6.46.

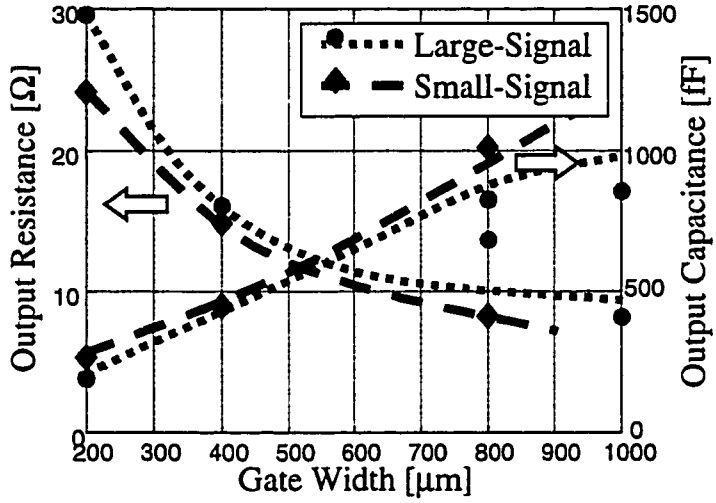


Figure 6.46. Small- and large-signal values of the output capacitance and output resistance as a function of gate width

It is also important to note that the AlGaN/GaN HFETs of this study demonstrated the same value of transconductance $g_m \approx 100mS/mm$, both at DC and RF, which suggests the absence of undesirable frequency dispersion effects. As mentioned earlier, this positively impacts the high frequency and power performance. To validate this prediction, the output power density obtained during load-pull characterization ($RF\ P_{OUT}$) was compared with the output power density predicted from DC measurements ($DC\ P_{OUT}$).

The maximum allowed voltage V_{MAX} and current I_{MAX} swings considered for this purpose were based on the biasing conditions used for evaluation of the reported power characteristics:

$$V_{MAX}=2\times V_{DS}-V_{DSAT} \tag{6.13}$$

where V_{DS} and V_{DSAT} are the drain-source bias and the saturation voltage of the HFET, respectfully; and

$$I_{MAX}=2\times I_D \tag{6.14}$$

where I_D is the value of the drain current under large-signal excitation obtained during RF power measurements. The use of a large-signal experimental value of I_D for representing the amplitude of the RF swing is justified by the dependence of P_{OUT} on V_{GS} (see Figure 6.40). P_{OUT} is decreased for larger negative V_{GS} indicating that the RF swing of I_D is affected by the biasing conditions. The experimental value of I_D is therefore a better choice than a value of I_{DSS} based on extraction from DC measurements only.

The dependence of I_D on P_{IN} for AlGaN/GaN HFETs with various gate widths is shown in Figure 6.47. The biasing conditions at low P_{IN} varied between *150mA/mm* (*Class AB*) for *0.2-mm*, *230mA/mm* (*Class A*) for *0.4-mm*, and *75mA/mm* (*Class B*) for *1-mm* HFET, respectively. When the input power is increased, I_D increases toward $I_{DSS}/2$, as expected, for devices biased in Class AB and Class B, while it remains constant for the device in *Class A*. The decrease of I_D at high power levels is attributed to thermal effects since the input power level where thermal effects become dominant (see Figure 6.47) scales with the device area.

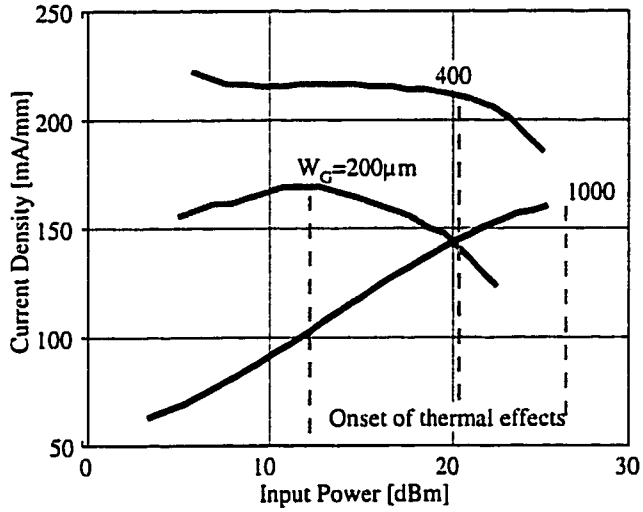


Figure 6.47. Dependence of self-biased drain current on input power measured during power saturation measurements of AlGaN/GaN HFETs with various gate widths

These conditions allowed calculation of *DC* P_{OUT}:

$$DC\ P_{OUT}=I_{MAX}\times V_{MAX}/8 \qquad (6.15)$$

The results of the comparison are presented in Table 6.4. The values of the RF output power density are very close to the DC output power density.

Table 6.4. Comparison of DC Predicted and RF Measured Output Power Density of AlGaN/GaN HFETs

Width [μm]	V_{DS} [V]	I_D [A/mm]	$RF\text{-}P_{OUT}$ [W/mm]	$DC\text{-}P_{OUT}$ [W/mm]	$RF\text{-}P_{OUT}/DC\text{-}P_{OUT}$ [%]
200	*15*	*170*	*0.89*	*0.97*	*91*
400	*12*	*222*	*1.00*	*0.94*	*105*
800	*12*	*186*	*0.87*	*0.79*	*109*
1000	*18*	*168*	*0.99*	*1.16*	*85*

The results show an exceptionally good correlation of AlGaN/GaN HFET DC, RF, and power characteristics and demonstrate their excellent potential for power applications.

Overall, excellent scalability of small- and large-signal characteristics and good correlation between DC, RF, and power characteristics was demonstrated for AlGaN/GaN HFETs with gate widths up to *1mm*, as necessary for monolithic switching applications of these devices.

6.4. Development of AlN/GaN MISFETs

GaN-based MISFETs have not drawn adequate attention so far, but these devices also offer high breakdown and increased drain-current capability, which are determining factors in power FET performance and make them very attractive for power applications. Moreover, insulator layer with small dielectric constant underneath the gate allows reducing OFF-state capacitance in MISFET and may lead to higher cutoff frequency than in a HFET.

Advantages of insulated-gate approach were previously demonstrated with GaAs-based and InP-based technology. Quantum-well AlGaAs/InGaAs/GaAs MISFETs [94] were developed and achieved a record high-power high-frequency operation *1W/mm* power density at *60GHz*. It was found that an increase of current density led to increase in output power, while frequency response was also improved due to reduced role of parasitic capacitance when the channel charge was increased. A record power density of *4.2W/mm* at X-band was also obtained using InP MISFETs [95]. However, conventional III-V semiconductors lack an insulator that would provide a high-quality interface to the

semiconductor. High interface state density in GaAs- and InP-based MISFETs ($N_{SS}>10^{12}cm^{-2}eV^{-1}$) leads to degradation of device performance, specifically to a reduction of transconductance and limitations in the reliability.

Recently, SiO_2/GaN and SiN/GaN structures have been fabricated and characterized [96, 97]. The reported results showed that the insulator-GaN interface may have a relatively low interface state density in the lower range of $10^{11}cm^{-2}eV^{-1}$. AlN also has the potential to be good insulating material. It is also expected to form epitaxially grown high-quality heterostructures to GaN. Moreover, the use of Al-rich AlGaN for the heterostructure has been shown to result in higher electron mobility and increased surface density of the 2DEG, which has been successfully exploited in AlGaN/GaN HFETs. However, this high 2DEG density in the channel is associated with the presence of high electric field. The required field F has to be of the order of $1MV/cm$ to reach N_S of $5x10^{12}cm^{-2}$ and as high as $F=2MV/cm$ for $N_S=1x10^{13}cm^{-2}$ [83]. The need for high field makes employing Schottky-gate impractical because of its limited reverse breakdown strength. Insulated-gate approach of AlN/GaN MISFETs allows minimization of the gate current and increase of the gate-drain breakdown by introducing wider bandgap semi-insulating AlN layer between the channel and the gate metal.

It should be noted that, AlGaN and GaN have mismatched lattice constants, and increasing Al fraction should be combined with respective decrease of the AlGaN thickness in order to minimize number of dislocations. Thus, the thickness of AlGaN barrier should be kept below critical thickness, and recent reports suggest that its thickness should be *2-4nm* [98]. Therefore, power GaN-based Heterojunction FETs will benefit from employing a thin AlN barrier layer maximizing 2DEG mobility and 2DEG density, as necessary for faster frequency response and higher current capabilities. For this purpose, AlN/GaN heterostructures were grown by MOVPE at the University of Michigan and AlN/GaN MISFETs were fabricated as described in Section 6.4.1. Interface characteristics of AlN/GaN MISFETs were evaluated using C-V characterization techniques detailed in Section 6.4.2. Finally, electrical performance of the fabricated devices is presented in Section 6.4.3.

6.4.1. Growth and Fabrication of AlN/GaN MISFETs

The AlN/GaN layers have been grown by MOVPE at the University of Michigan in a home-built horizontal quartz reactor. Substrates were placed on a graphite susceptor, which is heated by RF power generator. Growth was performed at low pressure (*60torr*) on c-plane sapphire substrates using *TMGa*, *TMAl*, and NH_3 as precursors. The layers were, starting from the sapphire substrate, a thin low-temperature (*515°C*) grown GaN buffer layer, a *0.5μm*-thick non-intentionally-doped GaN channel, and a thin AlN barrier layer. All layers except for the low-temperature buffer were grown at *1120°C*. Using the low-temperature GaN-buffer approach, high-temperature grown undoped bulk GaN and AlN layers were smooth, transparent, and uniform, as can be seen in Figure 6.48.

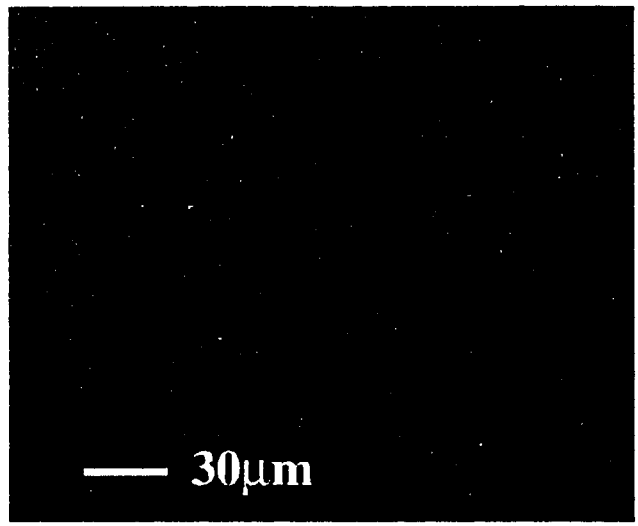


Figure 6.48. High-contrast Nomarsky photographs of AlN/GaN layers.

The AlN/GaN layer design was optimized by evaluating the mobility dependence on AlN layer thickness as obtained by Hall measurements and the results are shown in Figure 6.49. When the growth time of AlN was *450sec* corresponding to a thickness of *~110Å* for the AlN layer, the electron mobility was $320cm^2/Vs$ and the associated surface charge density was $2\times10^{13}cm^{-2}$. This growth time was used for growing the device layers employed in the study as it represents the best conditions for good interface properties and the best carrier-density conditions in the channel.

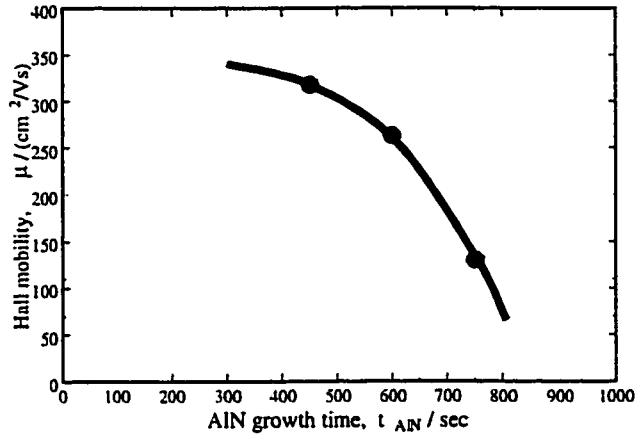


Figure 6.49. Dependence of electron mobility on the growth time of the AlN barrier layer.

Technology for fabrication of GaN-based FETs was developed and optimized during this work. It was based on dry (RIE) etching for device isolation and high-temperature rapid thermal annealing for ohmic metalization. The process flow of AlN/GaN MISFET fabrication is shown in Figure 6.50.

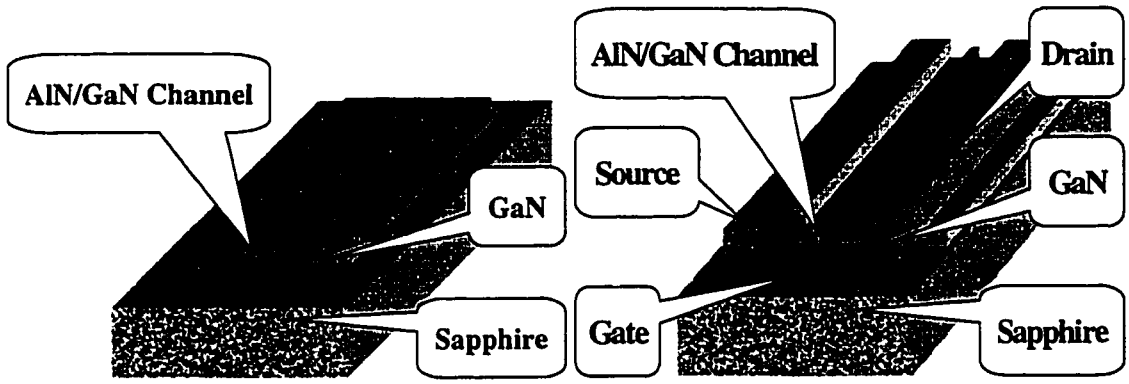


Figure 6.50. Process flow of the AlN/GaN MISFET fabrication.

First, device mesas were fabricated on AlN/GaN MIS layers using Cl-based dry etching for device isolation. The mesas were formed by removing all AlN and GaN layers down to the sapphire substrate outside the active device areas, which were covered by a photoresist mask. A standard photoresist mask offered sufficient protection for shallow etching (*~0.5μm*) required in the GaN FET fabrication. Moreover, the photoresist mask was undercut during the etching, forming mesas with outward-sloped walls, beneficial for continuous metallization of the mesa steps. The dry etching was performed in a low-pressure RIE chamber (*15mT*) with a mixture of CCl_2F_2 and Ar_2 flowing at *12sccm*. This

etching process is characterized by a controllable GaN etch rate of *50nm/min* and is currently used for GaN-based device fabrication at the University of Michigan.

The ohmic contact pads were obtained by lift-off process using image-reversal photoresist. Lift-off was assisted by ultrasonic treatment. *Ti/Al/Ti/Pt* metals were used for ohmic contacts. The metals were deposited directly on the top AlN layer. To reduce contact resistance, the ohmic contacts were annealed for *30sec* at *800°C* in nitrogen. A sheet resistance R_{SH} of $860\Omega/sq$ and a specific contact resistivity ρ_C of $4\times10^{-7}\Omega cm^2$ were evaluated by TLM analysis.

Gate contacts were made using *Pt/Ti/Au* metals. Optical lithography was used to define *2μm*-long gate patterns. The development time in *NaOH*-based optical photoresist developer was optimized in order to minimize possible damage to the AlN barrier layer. A short oxide etch was performed immediately prior to gate and ohmic deposition using hot *HCl* solution. An SEM photograph of a fabricated device is shown in Figure 6.51

Figure 6.51. SEM photograph of a GaN-based FET grown and fabricated at the University of Michigan

Overall, GaN-based FET fabrication technology employing Cl_2-based dry etching techniques was developed and applied for realization of GaN-based HFETs on AlN/GaN MIS layers grown by MOVPE at the University of Michigan.

6.4.2. Interface Characteristics of AlN/GaN MISFETs

Success of AlN/GaN MISFET approaches critically depends on developing material with good structural properties and low density of interface states. Moreover, results reported so far suggest that interface roughness is very important to the electrical performance of GaN-based devices [84] and is probably related to inter-diffusion at the AlN/GaN interface [99]. AlN/GaN interface properties can be evaluated by such techniques as C-V characterization.

A schematic of the AlN/GaN band diagram is shown in Figure 6.52. The band diagram in Figure 6.52a is devised following MIS theory of [100] and [101]. An electron affinity of $\chi_S=4.1eV$ for GaN, a work function $\Phi_M=4.5eV$ for a gate contact (typical for *Pt* metalization), and a conduction-band discontinuity of $2.1eV$ were used based on the data from reference [102].

This band diagram predicted that the n-type GaN channel underneath the thin AlN barrier layer would depleted at zero gate bias ($V_{GS}=0V$). Thus, a negative charge $-Q_M$ would be accumulated on the gate, and a positive fixed charge of Si donors Q_D would be present in the GaN channel at equilibrium as shown at the bottom of Figure 6.52a. However, such description did not correspond to the experimental data presented later in this section, which showed that the GaN channel is not depleted at equilibrium. The discrepancy can be explained by the presence of spontaneous polarization charge. In addition, a piezoelectric charge arising from the lattice mismatch between AlN and GaN can also be present at the interface if the accumulated strain is not relaxed through cracks and dislocations of the AlN layer. According to recent studies of polarization effects in AlGaN/GaN HFETs [103], a positive charge Q_{Pz} is induced at the AlGaN/GaN interface while an equal negative charge $-Q_{Pz}$ is present at the top of the AlGaN barrier layer. An energy-band and charge-distribution schematics of AlN/GaN MIS layers accounting for polarization effects based on bandgap-alignment considerations are shown in Figure 6.52b.

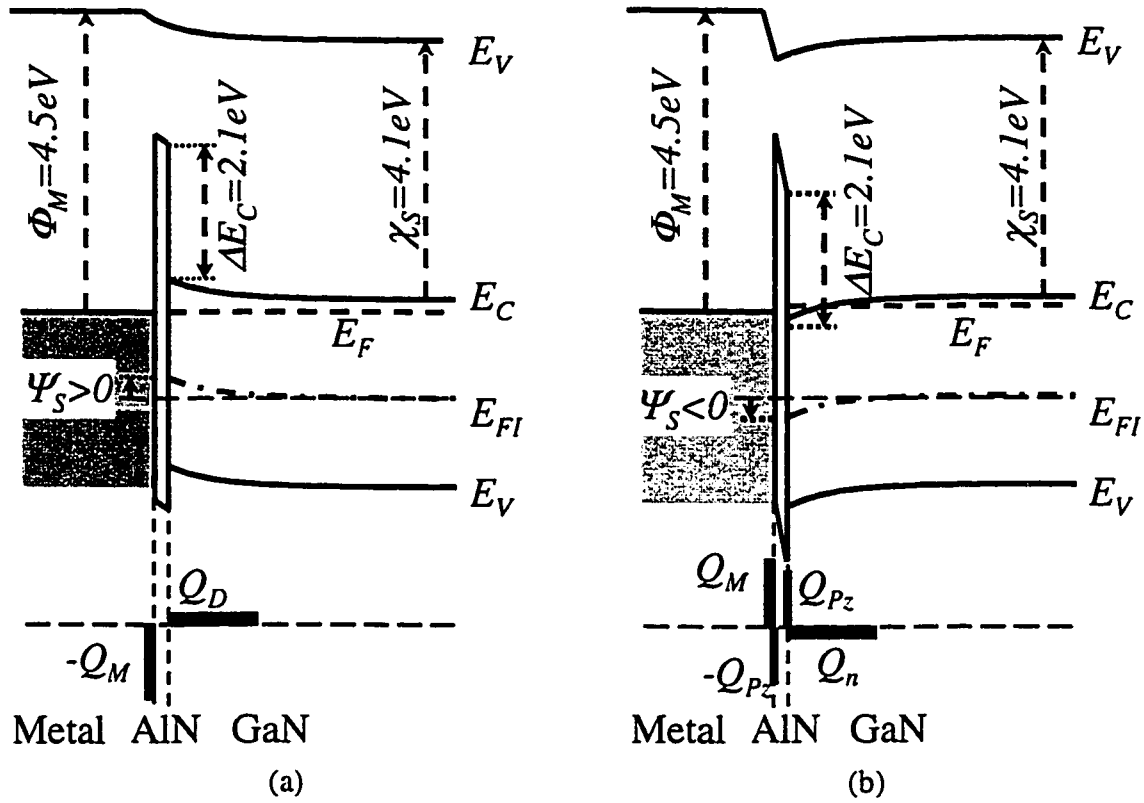


Figure 6.52. A schematic of energy band diagram and charge distributions in AlN/GaN MIS structure without (a) and with (b) polarization effects.

High polarization fields in the AlN/GaN layers are shown to induce electron accumulation in the GaN channel in agreement with experimental results. For the purpose of the presented analysis, the polarization effects were taken accounted for by assuming a uniform polarization field F_{PZ} inside of the AlN layer. This polarization field produced a bias-independent potential $V_{PZ}=F_{PZ}\times t_{AlN}$.

The C-V characteristics of the AlN/GaN MIS structures were calculated based on the one-dimensional solution of the Poison's equation as described in [101]. Thus, the surface charge Q_S is given by:

$$Q_S = \frac{\sqrt{2}\times\varepsilon_S}{\beta\times L_D}\sqrt{\left(e^{-\beta\times\Psi_S}+\beta\times\Psi_S-1\right)+\frac{n_i^2}{N^2}\times\left(e^{\beta\times\Psi_S}-\beta\times\Psi_S-1\right)} \qquad (6.16)$$

where ε_S is the dielectric constant of GaN, $\beta=q/k_B\times T$ is a normalization factor, and $L_D=\sqrt{\varepsilon_S/(N\times\beta\times q)}$ is the Debye length for electrons in the GaN channel. The n_i^2/N^2 term of expression (6.16) stands for inversion carriers (holes for an n-type GaN

channel) which are generated under large negative bias when the channel is in deep depletion and Ψ_S crosses the Fermi level E_F. However, generation time of minority carriers may be much larger than the period of the test signal. In such case, the minority-carrier population is never formed. This is especially typical for wide-gap semiconductor MIS structures such as SiO_2/SiC [104] and AlN/SiC [105], because the generation rate of the minority holes and the intrinsic carrier concentration n_i are extremely low in these materials. In the case of SiC, establishment of thermal equilibrium in the inversion region is reported to take years [106]. Thus, the inversion term can be neglected from the expression for the AlN/GaN surface-charge capacitance C_S:

$$C_S = \frac{dQ_S}{d\Psi_S} = \frac{\varepsilon}{\sqrt{2} \times L_D} \times \frac{\left(1 - e^{-\beta \times \Psi_S}\right)}{\sqrt{e^{-\beta \times \Psi_S} + \beta \times \Psi_S - 1}} \tag{6.17}$$

Finally, the total MIS capacitance was calculated as a series combination of the surface-charge capacitance C_S and the fixed capacitance of the AlN layer $C_I = \varepsilon_{AlN}/t_{AlN}$

$$C = \frac{C_S \times C_I}{C_S + C_I} \tag{6.18}$$

Finally, the gate bias V is related to the surface potential Ψ_S by the following expression:

$$V = \Psi_S + \frac{Q_S}{C_I} - V_{PZ} + \Phi_M - \chi_S \tag{6.19}$$

where the (Q_S/C_I-V_{PZ}) term is the total voltage drop across the AlN layer.

Large test AlN/GaN MIS diodes with an area of $300\mu m^2$ were fabricated for interface characterization as described in Section 6.4.1. The C-V characteristics of AlN/GaN diodes were measured using an LCR meter and a test signal with *200KHz* frequency and *25mV* amplitude. The C-V characterization of AlN/GaN diodes revealed MIS-like behavior as shown by the results of Figure 6.53. The minimum capacitance C_{MIN} evaluated from these characteristics was only an *8%* of the maximum capacitance C_I corresponding to the capacitance of the AlN insulator. This indicated that excellent charge modulation was possible in the AlN/GaN MIS structure.

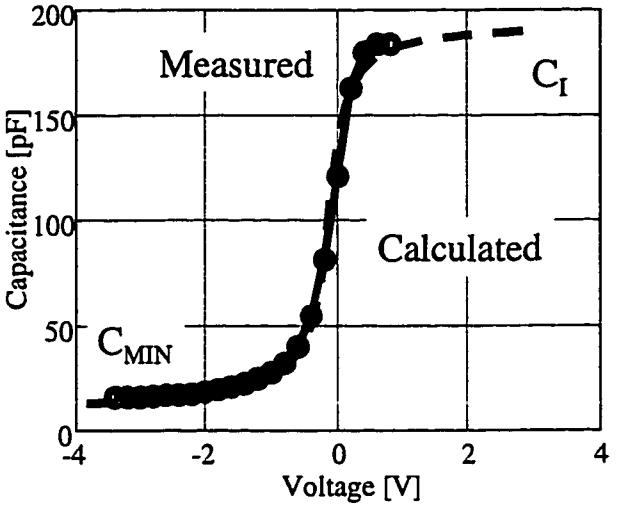


Figure 6.53. Measured (solid and markers) and calculated (dashed) C-V characteristics of AlN/GaN MISFET gate diodes.

The C-V characteristics of AlN/GaN MIS structures were also calculated using equations (6.16) through (6.19). For the purpose of calculation, an effective electron mass of $0.2m_0$, an effective hole mass of $0.8m_0$, a dielectric constant of *8.9*, an electron affinity of *4.1eV*, and an energy gap of *3.4eV* were used for GaN. The dielectric constant of AlN was considered to be *8* and a metal work function of *4.5eV* was assumed for *Pt*/Ti gates.

By matching experimental and theoretical C-V data, it was possible to obtain information about the AlN/GaN layers. Thus, based on the slope of $1/C^2$-V characteristics (see Figure 6.54), the doping of the GaN channel was found to be $N_D=1\times10^{17}cm^{-3}$.

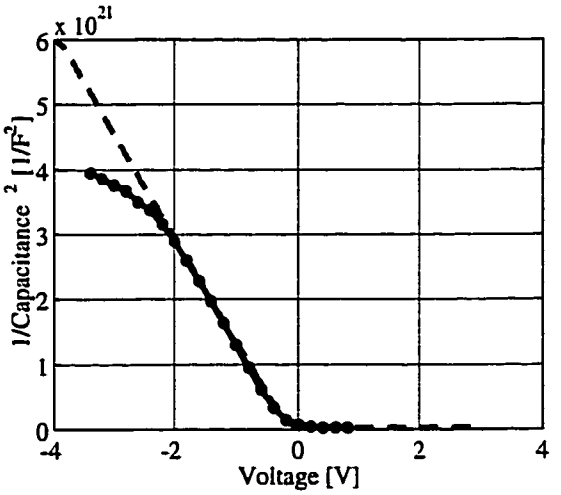


Figure 6.54. C-V characteristics of AlN/GaN MISFETs used to evaluate the properties of AlN/GaN interface.

The thickness (t_{AlN}) of the AlN barrier of *11nm* was estimated from the values of C_{MIN} and C_I. A voltage shift of *0.55V* was observed between the calculated and measured C-V characteristics. This difference was attributed to the presence of polarization charge at the AlN/GaN interface and corresponded to an electric field F_{PZ} of *500KV/cm*. Extracted value of the polarization field is lower than is predicted for a strained AlN/GaN system (*~3MV/cm*), indicating that partial strain relaxation may have taken place.

The density of interface states was evaluated by extracting a difference between the theoretical and experimental surface-charge capacitance:

$$D_{IT} = \frac{|C_{IT}|}{q} = \frac{|C_{SEXP} - C_{STH}|}{q} \tag{6.20}$$

The presence of interface states also affects the relationship between the biasing voltage V and the surface potential Ψ_S by providing additional screening which results in changes of the slope of the Ψ_S-V characteristic. Based on the relationship of equation (6.19), the slope of Ψ_S-V characteristic can be related to the C-V data:

$$\frac{dV}{d\Psi_S} = \frac{1}{C_I} \times \frac{dQ_S}{d\Psi_S} + 1 = \frac{C_S}{C_I} + 1 \tag{6.21}$$

Thus, D_{IT} can be calculated by combining equations (6.20) and (6.21):

$$D_{IT} = \frac{C_I}{q} \left| \left(\frac{dV}{d\Psi_S} \right)_{EXP} - \left(\frac{dV}{d\Psi_S} \right)_{TH} \right| \tag{6.22}$$

Such evaluation is based on the difference in the slopes of the theoretical and experimental Ψ_S-V curves. The experimental Ψ_S-V characteristic was found by matching bias V and surface potential Ψ_S, corresponding to the same MIS capacitance. This method is illustrated in Figure 6.55. Differences between the measured and theoretical C-V characteristics give rise to a decreased slope of the experimental Ψ_S-V characteristics, which indicate the presence of interface states.

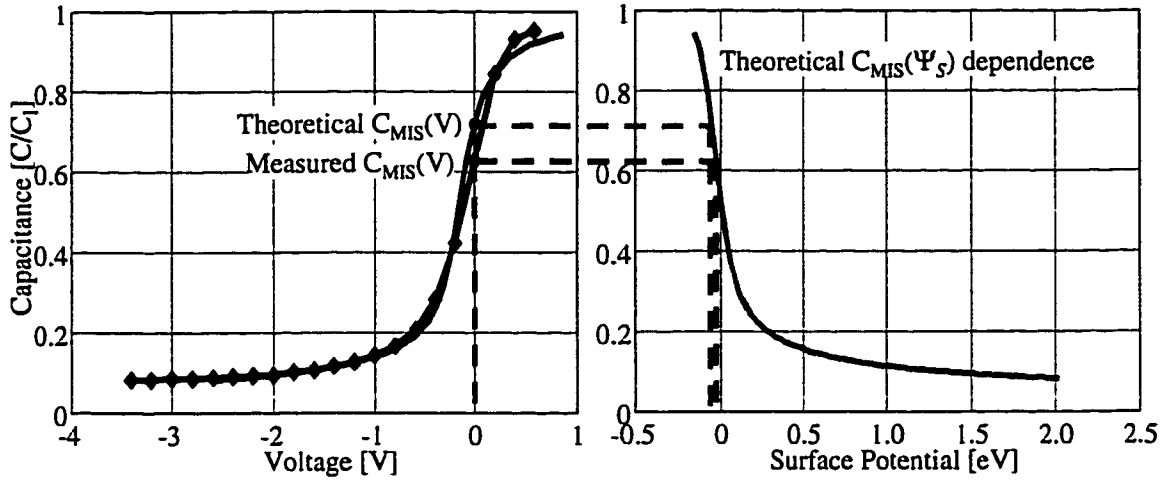


Figure 6.55. Determination of experimental and theoretical Ψ_S-V characteristics

The theoretical and experimental Ψ_S-V characteristics of AlN/GaN MIS diodes were extracted as shown in Figure 6.55 and the results are shown in Figure 6.56a. Equation (6.22) was used to evaluate the density of interface states for AlN/GaN interface as shown in Figure 6.56b. These results show that good interface properties are obtained from AlN/GaN heterostructures with a low interface-state density D_{IT} of $1\times10^{11}cm^{-2}eV^{-1}$. The interface state density was found to decrease when the surface potential varies from E_C to $1eV$ below the conduction band edge. The increase of the interface state density for energies below E_C-$1eV$ is attributed to measurement errors due to increased leakage current of the MIS diodes.

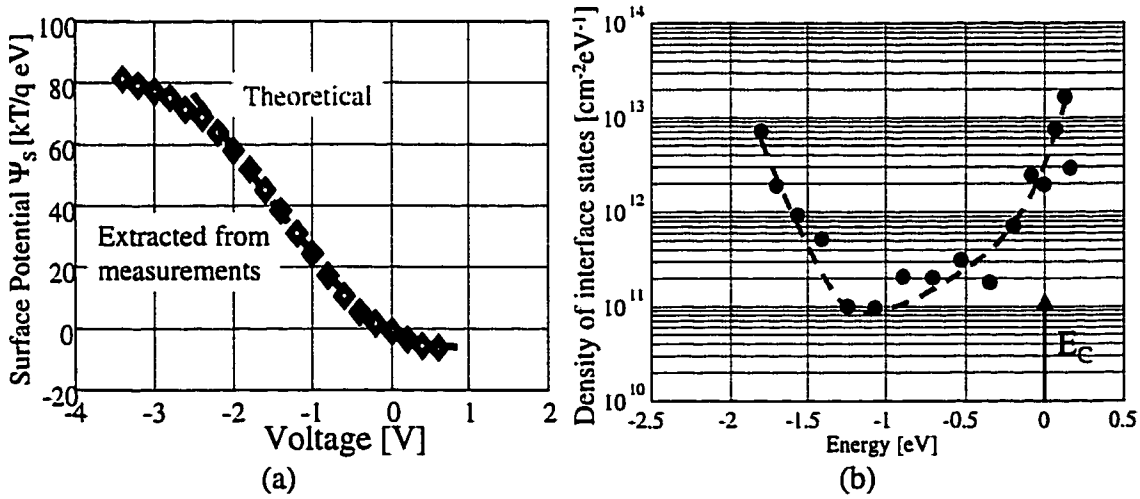


Figure 6.56. Theoretical and measured Ψ_S-V characteristics and extracted density of interface states D_{IT} in AlN/GaN MISFETs

6.4.3. Electrical Performance of AlN/GaN MISFETs

Typical DC I-V and transfer characteristics of AlN/GaN HFETs are shown in Figure 6.57. Devices with a gate length (L_G) of $2\mu m$ exhibited a peak transconductance of $\sim 135mS/mm$ at $V_{GS}=1V$, which exceeds previously reported results [107]. The threshold voltage of the devices was $-3.5V$ and the absence of full pinch-off at large drain bias was due to parasitic conductance in the NID GaN layer. The intrinsic transconductance $g_m^{int}=\sim 185mS/mm$ was found by taking into account contact resistance $R_C=2\Omega mm$ evaluated for these devices by TLM characterization.

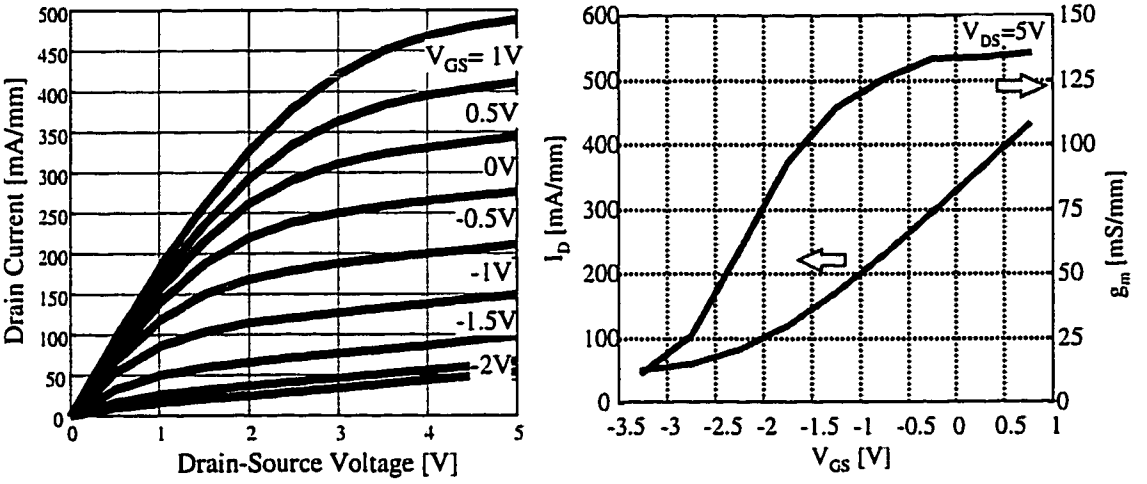


Figure 6.57. DC I-V and transfer characteristics of AlN/GaN MISFETs

The current capability I_{DSS} and transconductance g_m measured for AlN/GaN MISFETs with gate lengths varying between 2 and $100\mu m$ are shown in Figure 6.58.

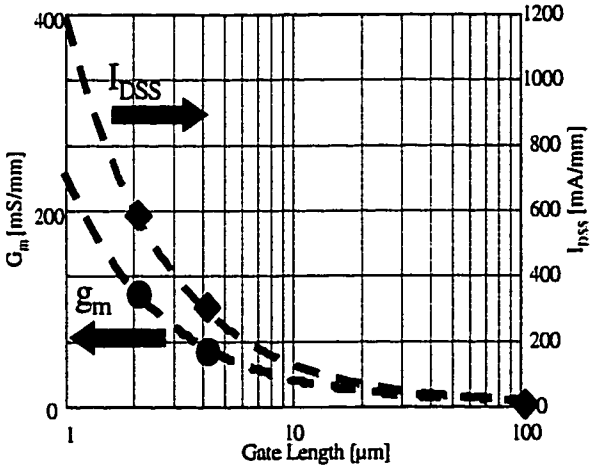


Figure 6.58. Scaling of I_{DSS} and g_m with gate length

The measured data show excellent agreement with a prediction based on a linear L_G dependence (shown by dashed lines) $g_m \sim 1/L_G$ and $I_{DSS} \sim 1/L_G$.

The I_D-V_{DS} and I_G-V_{GD} characteristics of the AlN/GaN MISFET shown in Figure 6.59 demonstrate its maximum current- and voltage-handling capability. An OFF-state drain-source breakdown at *31V* and an ON-state drain-source breakdown at *23V* were evidenced by "flashing" (thermal destruction) of the contact pads. The maximum drain current was greater than *700mA/mm*. Reverse I-V of characteristics of the gate-drain diode showed no evidence of tunneling or impact-ionization breakdown. Gate-drain breakdown occurred at *-42V* also by thermal destruction of the contact pads.

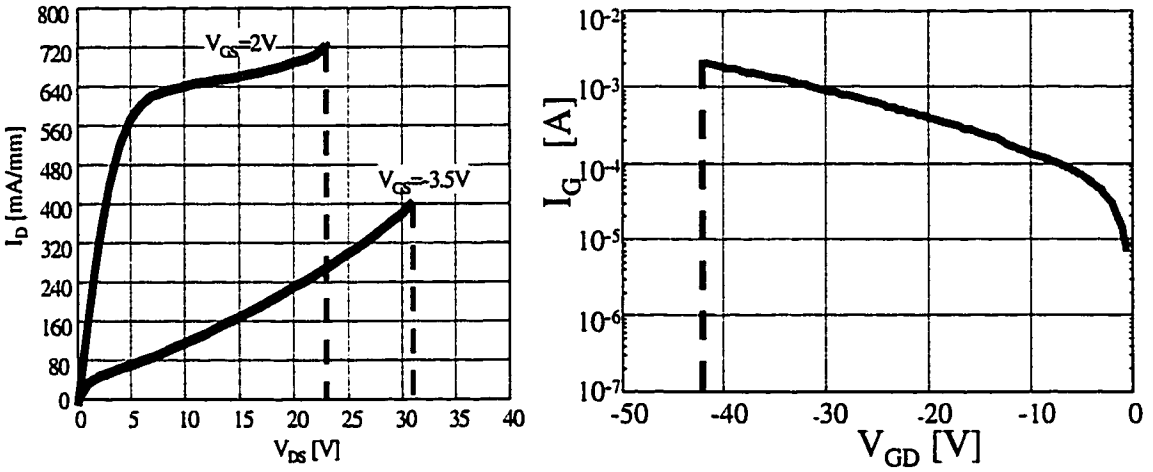


Figure 6.59. I_{DS}-V_{DS} characteristics showing the device breakdown features.

Overall, AlN/GaN MIS structures showed very low interface state density D_{it} values of $\sim 1 \times 10^{11} cm^{-2} eV^{-1}$ which was confirmed by a high value of transconductance (*185mS/mm*) for 2μm-long gate GaN-based MISFETs realized on these layers.

6.5. Summary

The advantages of using wide bandgap GaN-based materials for microwave switching applications were demonstrated by comparing theoretical figures-of-merit for GaN and GaAs as well as by considering basic characteristics and power-handling capabilities of FET switches made of these materials. GaN-based HFETs appear to be excellent candidates for design of high-power microwave switches and amplifiers.

The scalability of large-signal characteristics of AlGaN/GaN HFETs was investigated for the first time to confirm that the amount of power expected from a large-size component is not limited by parasitic effects. For this purpose, high-frequency large-signal characteristics of AlGaN/GaN HFETs with gate widths from *200μm* to *1mm* were measured at *8GHz* using automatic load-pull system.

The results demonstrated a notable scalability of AlGaN/GaN HFET power characteristics as desired for microwave switching applications. Thus, *1-dB* gain compression occurred at input power levels varying from *-1dBm* to *10dBm* as the gate width increased, while gain remained almost constant at *~17dB*. Output power density was *~1W/mm* for all devices and maximum output power (*29.9dBm*) occurred in devices with *1mm*-wide gates, while power-added-efficiency remained almost constant at *~30%*. The large-signal characteristics were compared with those obtained by DC and small-signal S-parameters measurements. Overall, these results indicated an excellent potential of GaN-based HFETs for high-power microwave applications.

The power capabilities and switching characteristics of GaN-based HFETs can be improved by using insulated-gate FET approach. AlN/GaN heterostructures using thin epitaxially grown AlN barrier layers have been investigated for purpose of developing III-N-based MISFETs. C-V characterization analysis was used to study the AlN/GaN MISFETs grown and fabricated at the University of Michigan and demonstrated low values of interface state density ($\sim 10^{11} cm^{-2} eV^{-1}$) of AlN/GaN interface. The high quality of the interface was confirmed by very high values of transconductance (*185mS/mm*) and drain current density (*>700mA/mm*) obtained from MISFETs fabricated on these layers.

Overall, good interface properties and electrical characteristics of AlN/GaN MISFETs were demonstrated for the first time. Promising results obtained by employing AlN/GaN MIS approach suggest its suitability for realization of GaN-based HFETs with increased electrical strength and frequency response as desired for their application in high-power MMICs.

CHAPTER 7

GaN-BASED NEGATIVE DIFFERENTIAL RESISTANCE DIODES FOR HIGH-POWER MILLIMETER SIGNAL GENERATION

So far, work described in this thesis was concerned with devices and circuits for signal control applications. Thus, InP-based PIN diodes for millimeter-wave switching applications were developed and employed for realization of high-performance W-band monolithic switches and phase-shifters for automotive and imaging applications. HFETs and MISFETs for control applications were studied and demonstrated a possibility to improve power-handling capabilities of FET-based switches by using wide bandgap GaN-based materials with increased electrical strength for their design. The investigated electronic components are used to provide amplitude- and phase-control functions as necessary for operation of high-power millimeter-wave transmitter-receiver modules introduced in Section 1.2.

However, signal-generation function is also very critical for operation of such systems. Signal generators at and beyond W-band frequencies can be implemented as HEMT- or HBT-based MMICs operating at the fundamental [108, 109] or at the sub-harmonic frequency [110, 111]. However, their output power is limited, especially at higher frequency range (*~50mW* at *80GHz* and *<1mW* at *130GHz*). At these frequencies, GaAs- and InP-based Gunn diodes remain primary semiconductor devices for signal generation and demonstrate larger output power (*~200mW* at W-band and *~80mW* at D-band [112]). Still, the power available from conventional GaAs- and InP-based Gunn diodes is shown to reduce sharply above *100GHz* [113] and the state-of-the-art result is only *~1mW* at *315GHz*.

The operation of Gunn diodes in conventional III-Vs is based on electron transfer between the high-mobility central and low-mobility satellite valley. The maximum output

power density is limited by the breakdown field (F_B), which, in the case of GaAs and InP, is *400* and *500KV/cm*, respectively. The use of wide-bandgap semiconductors, such as GaN, with increased electrical strength (F_B=*2MV/cm*), offers the possibility to increase the output power of the generated signals. Most of microwave device research on GaN so far has been concentrated on power field-effect transistors, and a record output power density for any FET of *7W/mm* was recently obtained with GaN-based MODFETs [114].

Studies of the fundamental properties of GaN indicate that this material also exhibits bulk NDR effect with a threshold field F_{TH} of the order of *80-200KV/cm*. Various possibilities are suggested for the nature of NDR in nitrides including electron intervalley transfer [115, 116] and special features of the band structure [117]. However, Gunn domain instability is expected to be possible independent of the nature of NDR, provided the appropriate I-V characteristics are present [118].

Although further confirmation is needed regarding the presence of bulk NDR in GaN, the use of GaN-based materials in NDR diodes appears to offer advantages over traditional GaAs devices. These include increased electrical strength, higher threshold field, and a possibility of faster operation due to reduced time constants of energy, momentum, and dielectric relaxation in GaN.

Theoretical studies were conducted to evaluate the power and frequency capability of GaN-based NDR diodes and to study power performance of GaN NDR oscillators as a function of bias, doping, frequency, and circuit design.

7.1. Mechanism of Negative Differential Resistance in GaN

Low-field electron transport in semiconductors is often described by an effective-mass approximation based on the curvature of the conductance band near its minimum energy. However, the effective mass approximation can not be used to accurately analyze high-field transport, when electron scattering rates are increased, electrons are scattered into satellite valleys, and the curvature of conduction band and, thus, the effective mass are altered.

A common method to describe high-field electron transport in semiconductors is to continue using a low-field value of the effective mass, and treat the drift velocity of

electrons as a nonlinear function of the accelerating electric field. Thus, high-field drift velocity in semiconductors converges to a finite saturation velocity $v_{SAT} \approx 10^7 cm/sec$. This velocity saturation is caused by increased interaction of high-energy electrons with the crystal lattice (generation of polar-optical phonons).

Most III-V compound semiconductors demonstrate velocity-field characteristics with a region of negative differential mobility. This effect is possible due to a special type of band structure alignment often observed in direct-band III-V compounds, such as GaAs and InP. A schematic of GaAs band structure is shown in see Figure 7.1a). The high-mobility Γ valley forms the bottom of the conduction band, while the low-mobility X valley is located ΔE above the bottom of the conduction band.

7.1.1. Transferred-Electron Effect NDR

Negative differential mobility is caused by field-induced transfer of high-mobility electrons from the Γ valley to the low-mobility X valley. For electric field above threshold field F_{TH}, electrons in the Γ valley acquire ΔE of kinetic energy and begin to transfer to the X valley. When enough high-mobility electrons are scattered into the low-mobility states, average electron drift velocity is reduced and v-F characteristics demonstrate NDR.

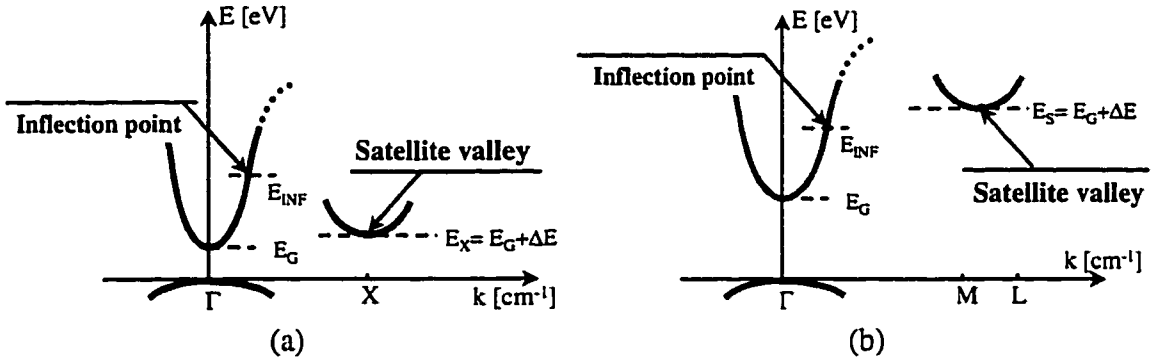


Figure 7.1. Schematic of (a) GaAs and (b) GaN band structure

The transferred-electron theory of NDR in GaAs and other III-V compound semiconductors had been successfully verified in experiments where ΔE was varied by applying pressure or altering material composition [119, 120]. The Monte Carlo simulation approach, which allows accurate modeling of scattering rates for a known band structure (including electron intervalley transfer), was applied to calculate the

velocity-field characteristics in GaAs and demonstrated an excellent agreement with measured *v-F* characteristics [121].

With development of GaN-based light-emitting diodes in the early 1990s, nitride-based electronic devices had emerged as excellent candidates for microwave power applications due to large electrical strength, high temperature, radiation, and environmental hardness of these materials [122]. Consequently, the GaN band structure was calculated and Monte Carlo simulation techniques were applied to investigate electronic transport in GaN [115, 123]. The GaN *v-F* characteristics, calculated in these studies, also demonstrated a bulk NDR effect in the high-field region due to the intervalley electron transfer. However, the threshold field for electron intervalley transfer and consequent appearance of NDR in GaN was much larger than in GaAs. An increase of the threshold field is caused by a larger separation between the satellite and central valleys in GaN $\Delta E \approx 2.1eV$ (for wurtzite (*Wz*) phase of GaN) compared to $\Delta E \approx 0.3eV$ for GaAs. A schematic of the GaN band structure is shown in Figure 7.1b to illustrate this difference in band alignment. The figure also illustrates another key difference between the GaAs and GaN bandstructures — the inflection point of the Γ valley E_{INF} in GaN is positioned below the bottom of the satellite valley E_S, according to studies reported in [117] and [124]. Such location of the inflection point can be exploited to increase frequency capabilities in GaN-based NDR devices as discussed in detail in Sections 7.1.2 and 7.2.

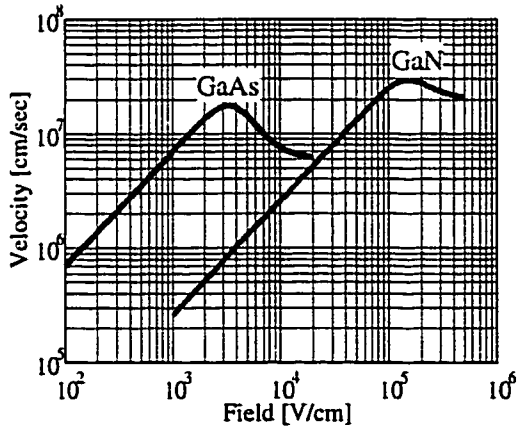


Figure 7.2. Comparison of *v-F* characteristics between GaAs and GaN

The *v-F* characteristic of *Wz* GaN were fitted to the results of [123] using a well known high-field *v-F* equation (see page *2-32* in *Volume I* of [125]):

$$v(F) = \mu F \frac{1 + \frac{v_{SAT}}{\mu F}\left(\frac{F}{F_{TH}}\right)^4}{1 + \left(\frac{F}{F_{TH}}\right)^4} \tag{7.1}$$

The results are shown in Figure 7.2. For purpose of comparison, this figure also includes *v-F* characteristics of GaAs calculated following reference [125]. GaN manifested a higher peak velocity v_{PEAK} (3×10^7 vs. $1.5\times10^7 cm/sec$), saturation velocity v_{SAT} (2×10^7 vs. $0.6\times10^7 cm/sec$) and much larger threshold field F_{TH} of *150KV/cm* compared with *3.5KV/cm* for GaAs. At the same time, the GaN low-field mobility of $\sim 280 cm^2/Vs$ is lower than the GaAs value of $\sim 8000 cm^2/Vs$.

7.1.2. Inflection-Point Effect NDR

Another important effect in high-field transport is dispersion of the effective mass. A constant value of the effective mass corresponds to a conduction band edge *E(k)* with an isotropic and parabolic dependence on the wave vector, as follows from the definition of the effective mass as the curvature of the conduction band edge:

$$\frac{1}{m_{eff}} \equiv \frac{1}{\hbar^2}\nabla_k^2 E(k)\Big|_{E_{MIN}} \tag{7.2}$$

However, Bloch theory predicts that the curvature of the conduction band edge has to change from concave-upward at the center of the band to concave-downward near the edge of the Brillouin zone. High-energy electrons experience a variable curvature of *E(k)*, which is reflected by the dispersion of the electron group velocity (v_{GR}) and the density of states dN/dE as shown in Figure 7.3 [126]. Thus, electrons accelerated by a high electric field will experience larger effective mass and slow down near the inflection point where the group velocity is maximal and the effective mass $m_{eff} \approx dN/dE$ approaches infinity [126]. Such electron behavior near the inflection point has also been suggested as a possible mechanism of NDR in semiconductors at high

fields (for example in InAs [127] and Ge [128]). However, the ordering of bands in most semiconductors is such that the inflection point energy ΔE_{INF} is comparable to the bandgap energy E_G or exceeds the energy of satellite valley ΔE (see Figure 7.1a). Thus, high-field *v-F* characteristics are dominated by impact ionization or intervalley transfer, which occur at a lower electric field than required for initiation of the inflection-related NDR [127]. Quantum-well superlattice structures were suggested by Esaki as means of forming a superlattice sub-band structure with reduced inflection point energy to overcome the impact-ionization problems [129]. The feasibility of QW inflection-based NDR to high-frequency applications had since been confirmed, as evidenced a recent report of GaAs/AlGaAs NDR diode oscillators operating up to *60GHz* [130].

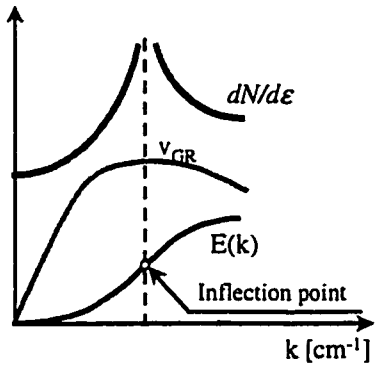


Figure 7.3. Electron group velocity (v_{GR}) and differential density of states ($dN/d\varepsilon$) in the vicinity of the inflection point of the conduction band *E(k)*.

According to recent studies, the *Γ*-valley inflection point in both *Zb* and *Wz* GaN is located below the lowest satellite valley and its threshold field is much smaller than the breakdown field [117, 131]. Therefore, NDR in bulk GaN may be caused by variations of drift electron velocity in the *Γ* valley, unlike in all other semiconductors, where intervalley-transfer-based NDR is initiated before the inflection-based NDR or the inflection-based NDR is overshadowed by avalanche breakdown effects. For example, the inflection point of the *Γ* valley and the *X* valley of the zinc blende (*Zb*) GaN are located *~1eV* and *~1.5eV* above the bandgap, respectively. The *v-F* characteristics calculated using Monte Carlo simulations based on a band structure including the inflection point [117] indicated that bulk NDR mechanism was indeed caused primarily by the variations of the electron drift velocity in the *Γ* valley. The inflection-based NDR had a threshold

field F_{TH} of *80KV/cm* and peak velocity v_P of 3.8×10^7*cm/sec* compared with F_{TH} of *110KV/cm* and V_{PEAK} of 2.7×10^7*cm/sec* for electron-transfer based NDR calculated in [115].

Monte Carlo simulations used to calculate *v-F* characteristics of GaN reported in [115] did not consider ordering of the band structure and, thus, overlooked the inflection-point mechanism of NDR formation, which resulted in a larger threshold field F_{TH}. However, by far a more important consequence of the inflection-based NDR mechanism is the reduction of the time constant required for formation of inflection-based NDR and, thus, a possibility of increased frequency capability for GaN-based NDR devices.

7.2. Fundamental Frequency Limitations of NDR Devices

While the previous section was concerned with electron transport in static electric field, the resulting velocity-field characteristic with NDR region has an underlying dynamic character due to its derivation from frequency-dependent processes, such as intervalley transfer, momentum, and energy relaxation. When the frequency of operation approaches the NDR relaxation frequency f_{NDR}, determined by these processes, the negative slope of the *v-F* characteristic diminishes and the efficiency of the NDR devices is reduced as shown in Chapter 3 of [132]. Moreover, the operation of NDR devices is based on the growth and change of electron domains and, thus, it can not be efficiently realized above the dielectric-relaxation frequency f_{DR}. Consequently, NDR devices made of materials with higher carrier mobility and designed using higher-doped active regions have higher frequency capabilities. Finally, the transit-time frequency of NDR devices f_T is determined by the domain velocity v_{DOM} and the active region thickness L_A.

This section compares frequency capabilities of GaN- and GaAs-based NDR devices in context of various frequency limitations imposed by the material properties and the device design as discussed above.

7.2.1. Dynamic High-Field Transport of a Single Electron

Frequency-independent velocity-field characteristics can be used to analyze the electron transport in the time-varying electric field as long as the frequency of operation is smaller than the slowest of all collision rates $1/\tau_0$ as given in (7.3):

$$f < f_{NDR} = \frac{1}{\tau_{MR} + \tau_{ER} + \tau_{ET}} < \frac{1}{\tau_A} \tag{7.3}$$

where τ_{MR} is the momentum-relaxation time corresponding to the rate of elastic collisions, τ_{ER} is the energy-relaxation time corresponding to the rate of inelastic collisions, and τ_{ET} is the intervalley relaxation time corresponding to the rate of intervalley electron transfer. The momentum-relaxation time τ_{MR} can be back-calculated from the measured electron mobility using expression (7.4). Such an experiment-based approach allows circumvention of time-consuming detailed calculations of individual scattering rates, unessential for purpose of this discussion. Given an electron mobility of *7000* and *280cm²/V/sec*, τ_{MR} is *0.26ps* and *0.03ps* for GaAs and GaN, respectively.

$$\tau_{MR} = \mu \frac{m_{eff}}{q} \tag{7.4}$$

An informative estimate for energy-relaxation time can be made using an acceleration-deceleration model for an electron, which neglects the small amount of energy lost in inelastic collisions following discussion in Chapter 3 of [132]. Then τ_{ER} can be found using expression (7.5), as the time it takes to accelerate an electron to the threshold energy where it experiences NDR:

$$\tau_{ER} = \frac{\sqrt{2 m_{eff} \Delta E}}{q F_{TH}} \tag{7.5}$$

where ΔE of *0.36* and *2eV* and F_{TH} of *3.5* and *150KV/cm* were used for GaAs and GaN, respectively. The energy-relaxation time of τ_{ER}=*0.15ps* calculated for GaN showed a *10*-times reduction compared with the GaAs value of *1.5ps*.

The time of intervalley electron transfer τ_{ET} was estimated from the results of Monte Carlo studies of ballistic transport in GaAs and GaN [133]. This work considered a step response of the electron velocity to the electric field. Initially the electron velocity

increased to the ballistic-overshoot peak value v_{PEAK}, and subsequently it decreases to its high-field steady-state saturation value v_{SAT} (due to electron intervalley transfer from the central to satellite valley). The results demonstrated that ballistic velocity overshoot was present over shorter distances in GaN than in GaAs. Thus, when a high electric field $F > 10 \times F_{TH}$ was applied to GaAs and GaN, ballistic transport was observed within *0.45* and *0.15μm*, respectively.

Electron intervalley transfer times in GaAs and GaN as a function of applied electric field were evaluated from the numbers of [133] using the following formula:

$$\tau_{ET} = \int_0^{L_B} \frac{dx}{v_e(x)} \approx \frac{L_B}{v_B / 2} \tag{7.6}$$

where L_B is the distance over which ballistic overshoot was taking place and v_B is the peak ballistic velocity. The results are shown in Figure 7.4. By extrapolating the obtained $\tau_{ET}(F)$ curves to point of threshold field $F=F_{TH}$, electron intervalley transfer times τ_{ET} of *7.7ps* and *1.2ps* were found for GaAs and GaN, respectively.

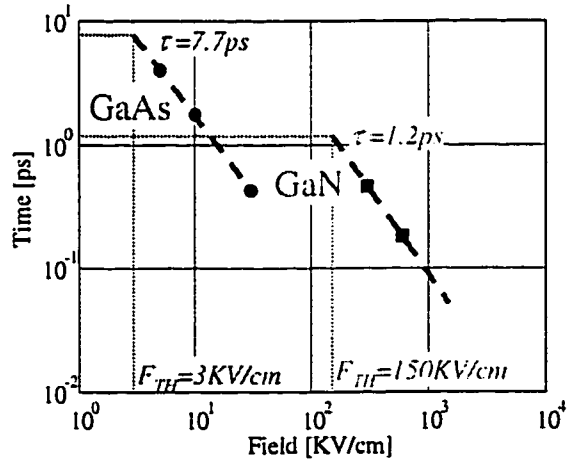


Figure 7.4. Evaluation of electron transfer time τ_{TE} in GaAs and GaN

The frequency capabilities of GaAs and GaN NDR devices can be evaluated using equation (7.3) and based on the values of energy, momentum, and intervalley relaxation times calculated in this section. The NDR relaxation frequency f_{NDR} of GaAs was found to be *~105GHz* in good agreement with the experimental and theoretical studies [134]. The frequency capabilities of GaN-based NDR devices was found superior to that of GaAs-based devices as indicated by the in GaN NDR relaxation frequency of *~700GHz*

for case of intervalley-transfer-based NDR and ~*4THz* for case of inflection-based NDR ($\tau_{ET}=0$).

Increased frequency response of high-energy electrons in GaN is attributed directly to higher electrical strength and higher saturation electron velocity of this material compared with GaAs. THz capability predicted for GaN NDR devices operating on the inflection-based mechanism is possible due to exceptionally high frequency response of electrons to the changes in the bandstructure as discussed in [130].

7.2.2. Dynamics of Electron Domains

So far, the discussion was concerned with the transport of a single electron. However, the operation of NDR devices is based on the propagation of multi-electron domains. According to Poisson's equation, a non-uniformity of electron concentration (domain) in a semiconductor at equilibrium conditions decays at a rate of $1/\tau_{DR}$, where τ_{DR} is known as the dielectric relaxation time, given by expression (7.7):

$$\tau_{DR} = \frac{\varepsilon}{q\mu N} \tag{7.7}$$

where N is the concentration of free carriers and ε is the dielectric constant. If a high electric field $F > F_{TH}$ is applied the electrons may possess a negative differential mobility μ_{NDR}. Under these conditions, an electron domain would grow at a rate $1/\tau_{DDR}$. τ_{DDR} is known as the differential dielectric relaxation time and is given by expression (7.8):

$$\tau_{DDR} = \frac{\varepsilon}{q\mu_{NDR} N} \tag{7.8}$$

where μ_{NDR} is the peak negative differential mobility $\mu_{NDR} \equiv \max(-dv/dF)$. The low-field mobility and the negative differential mobility in GaAs are larger than in GaN and, thus, growth and decay of electron domains occur faster in GaAs than in GaN for equally doped samples. It is recognized that domain formation and dissipation occur within at least $3\times\tau_{DDR}$ and $3\times\tau_{DR}$, respectively (where the latter is always much shorter) [135]. Thus, the frequency of operation of NDR devices is also limited by the time necessary for domain growth and change τ_{DOM} given by the following expression:

$$f < f_{DOM} = \frac{1}{\tau_{DOM}} \approx \frac{1}{\tau_A + 3\times\tau_{DR} + 3\times\tau_{DDR}} \tag{7.9}$$

The dependence of the frequency capabilities on the doping of the active layer N for GaAs and GaN was calculated using the v-F characteristics of references [117, 123, 125]. The peak negative differential mobility $\mu_{NDR} \equiv \max(-dv/dF)$ in *Wz* GaN, *Zb* GaN, and GaAs were *~50cm²/Vs*, *~220 cm²/Vs*, and *~2500cm²/Vs*, respectively. The results are shown Figure 7.5.

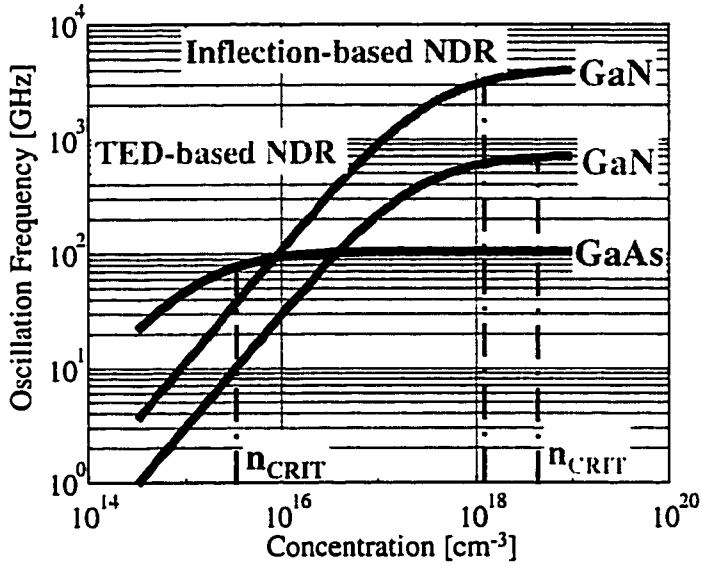


Figure 7.5. Frequency constraints of GaAs and GaN NDR devices

For low doping of the active layer, the GaN f_{DOM} is lower the GaAs f_{DOM} due to the higher negative electron mobility in GaAs. However, as the doping is increased, the dielectric relaxation times are reduced, and the GaN f_{DOM} exceeds that of GaAs for doping levels $N > 5\times10^{16}cm^{-3}$. Maximum f_{DOM} is limited by the NDR relaxation time discussed in the previous section. The maximum f_{DOM} in GaN is *~700GHz* and *~4THz* for a transferred-electron and an inflection-based mechanisms of NDR, respectively.

7.2.3. Transit-Time Frequency Limits

NDR devices are potentially unstable devices and tend to oscillate with a frequency, which is determined by the transit time of the active region. The transit-time frequency of NDR devices f_T is determined by the thickness of active region L_A and the

domain velocity v_{DOM}. Domain propagation, explained in detail in the following section, occurs with a velocity close to the peak velocity of the *v-F* characteristics v_{PEAK}. The peak electron velocity is estimated to be $\sim 2.5\times10^7$ *cm/sec*, $\sim 4\times10^7$ *cm/sec* and $\sim 1.5\times10^7$ *cm/sec* in wurtzite GaN, cubic GaN, and GaAs, respectively. Thus, the transit-time oscillation frequency would be higher for a GaN-based than a GaAs-based NDR device with the same thickness of the active layer. Transit-time frequency calculated for GaN and GaAs NDR devices with active layers thickness varying between $1\mu m$ and $8\mu m$ is shown in Figure 7.6.

The results of Figure 7.6 also indicate that NDR devices made of GaAs can not be designed with the thickness of the active regions shorter than $1\mu m$. This limitation is due to a long intervalley-transfer time in GaAs, which also limits the maximum oscillation frequency of GaAs devices to below *100GHz*. On the other hand, a properly designed GaN-based NDR device with $1\mu m$-thick active layer has transit time frequency of *~300GHz*. Moreover, GaN-based NDR devices with an active layer of $<0.5\mu m$ and doped at $\sim 10^{18} cm^{-3}$ appear to have up to *~700GHz* capabilities, provided that appropriate *v-F* characteristics are still present.

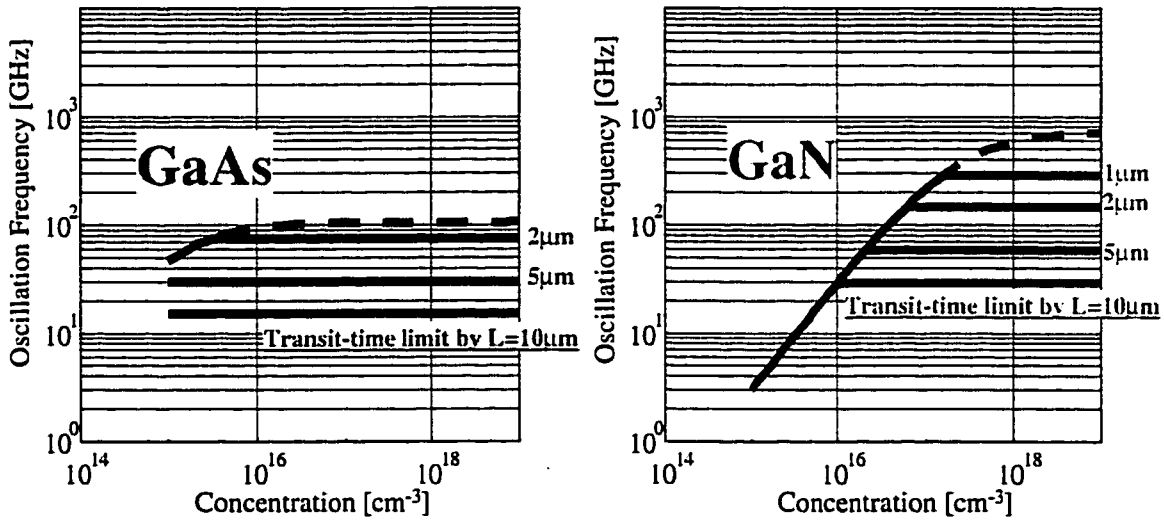


Figure 7.6. Transit-time frequency for GaAs and GaN NDR devices

7.3. GaN NDR Diodes Simulation Methodology

This section describes a numerical approach used to confirm that the postulated GaN *v-F* characteristics indeed lead to Gunn domain instability that can be exploited for design of GaN-based NDR oscillators.

7.3.1. Modeling of GaN Material Parameters

Studies of GaN-based NDR diodes were conducted by employing a commercial semiconductor-device simulator *Medici* [125]. While commercial software was used for conducting the simulations, such software did not posses any material parameters for GaN. Simulations of GaN-based devices were made possible by introducing a set of GaN material parameters evaluated, verified, and properly introduced into the simulator.

The predicted device characteristics depend strongly on the material properties used for analysis. Difficulties in GaN growth related to the lack of suitable substrates do not allow at this point the demonstration of the full potential promised by theoretically predicted material properties. The quality of available material limits, for example, the mobility and minimum background concentration that can be achieved in n-doped GaN. For this reason, the values for GaN parameters used in the analysis presented in this work were mostly selected to be consistent with the experimentally investigated material and device properties rather than based on theoretical predictions.

Thus, a low-field electron mobility of $\mu_n=280cm^2/Vsec$ and $60cm^2/Vsec$ were assumed for *Wz* GaN doped at $N=5\times10^{16}cm^{-3}$ and $1\times10^{19}cm^{-3}$, respectively [136]. Field dependence of carrier mobility (including NDR) was modeled by curve fitting of (7.1) to the *v-F* characteristics calculated by Monte-Carlo simulations [117, 123].

The value of electron lifetime $\tau_n=7ns$ and hole lifetime $\tau_p=0.1ns$ used in the simulations was based on the experimental data measured by electron beam induced current method [137]. Coefficients for calculating impact-ionization rates as a function of the electric field in GaN were first obtained by curve fitting to the theoretical predictions presented in [138]. Then, the GaN impact-ionization model employed in the analysis was verified by comparing the simulated and measured breakdown of GaN PIN diodes [139]. The I-layer of GaN PINs was linearly-doped and the doping gradient varied between

2×10^{22} and $2\times10^{23}cm^{-4}$. The simulated breakdown voltages for these values of doping gradient were *60* and *130V*, respectively, in good agreement with the experimental data, which varied between *40* and *150V*.

Table 7.1. Semiconductor material parameters of GaAs and GaN

Material	F_{TH}, [KV/cm]	F_B [MV/cm]	v_{SAT}, [cm/sec]	v_{PEAK}, [cm/sec]	μ [V/cm^2/s]	μ_{NDR} [V/cm^2/s]	τ_{NDR} [ps]
GaAs	3.5	0.4	0.6×10^7	1.5×10^7	8000	~2500	9.4
Wz GaN	150	2	2×10^7	2.9×10^7	280	~50	1.4
Zb GaN	80	1.2	1.7×10^7	3.5×10^7	730	~220	0.25

Important material parameters of wurtzite (*Wz*) and zinc-blende (*Zb*) phases of GaN as well as GaAs used in the simulations are listed in Table 7.1. GaN offers higher peak and saturation velocities than GaAs, which leads to a reduced transit time and an increased frequency of operation. The threshold and breakdown fields are also larger in GaN, which allows operation at a higher bias and leads to increased output power.

7.3.2. GaN NDR Diode Simulation Approach

Custom-developed *hydrodynamic* semiconductor device simulators have previously been used for investigations of high-frequency Gunn diode oscillators [140]. Commercial device simulator *Medici* also offers *hydrodynamic* or *energy-balance* simulation capabilities, and it had been successfully employed for a basic study of a possibility of Gunn oscillations in the collectors of GaAs-based HBTs [141]. In this work, hydrodynamic simulation capabilities of *Medici* were extended to allow small-signal stability analysis as well as large-signal harmonic power characterization. These novel techniques were applied to investigate the frequency and power potential of microwave signal generators using GaN NDR diodes and, for comparison purposes, GaAs Gunn diodes.

The equations used in the simulations of GaN NDR diodes include Poisson's equation (7.10), carrier-continuity equations (7.11), and an additional set of energy-balance equations (7.12), (7.13), and (7.14):

$$\vec{\nabla}\cdot\varepsilon\vec{\nabla}\Psi = -q(p - n + N_D - N_A) \tag{7.10}$$

where Ψ is the intrinsic Fermi level, n and p are the electron and hole concentrations, and N_D and N_A are the n-type and p-type doping concentrations, respectively. The Fermi level on the boundary between a semiconductor layer and an ohmic contacts was set equal to an externally-applied biasing voltage. Carrier-continuity equations are given by

$$\begin{aligned}\frac{dn}{dt} &= \frac{1}{q}\vec{\nabla}\cdot\vec{J}_n - U_n \\ \frac{dp}{dt} &= \frac{1}{q}\vec{\nabla}\cdot\vec{J}_p - U_p\end{aligned} \tag{7.11}$$

where J_n and J_p are the electron and hole current densities, and U_n and U_p are the electron and hole recombination rates, combined of Shockley-Read-Hall U_{SRH} and optical U_{DIR} recombination rates. A deep trap with energy E_{TRAP} close to E_{FI} was assumed for calculation of U_{SRH}. The Einstein coefficient for direct optical recombination B_N of $1.5\times10^{9}cm^{-3}$ was calculated for GaN-based semiconductor lasers in reference [142].

The hydrodynamic simulation approach introduces corrective terms to current density equations (7.12):

$$\begin{aligned}\vec{J}_n &= q\mu_n(u_n)\left[n\vec{E} + \vec{\nabla}(u_n n)\right] \\ \vec{J}_p &= q\mu_p(u_p)\left[p\vec{E} + \vec{\nabla}(u_p p)\right]\end{aligned} \tag{7.12}$$

where $u_n = k_B T_n/q$ and $u_p = k_B T_p/q$ are the thermal voltages of the electrons and holes, respectively. The energy-balance equations used in the simulations of GaN NDR diodes were developed for compound semiconductors in reference [143]. They were used to balance carrier heating by electric field with carrier cooling by energy relaxation, SRH recombination, and impact ionization mechanisms [125] as shown by (7.13) and (7.14):

$$\vec{S}_n = -\frac{5}{2}u_n\left(\frac{\vec{J}_n}{q} + \mu n\vec{\nabla}u_n\right) \tag{7.13}$$

$$\vec{\nabla}\cdot\vec{S}_n = \frac{1}{q}\vec{J}_n\cdot\vec{E} - \frac{3}{2}\left[n\frac{u_n - u_0}{\tau_{NDR}} + \frac{\partial(nu_n)}{\partial t}\right] - \frac{1}{q}\frac{E_g G''_n}{q} + \frac{3}{2}U_{SHR}u_n \tag{7.14}$$

where $\bar{S}_n$ is the electron energy flow density, τ_{NDR} is the total energy relaxation time, and G^{II}_n is the impact ionization rate. By including energy-balance equations and adding NDR relaxation times to the energy relaxation time, it was possible to ensure that the frequency of operation of the investigated NDR devices can not exceed the NDR relaxation frequency f_{NDR}.

A fully-coupled solution of Poisson, current continuity, and energy-balance equations was obtained by applying Newton's numerical differentiation and integration method to spatial distributions of GaN NDR diode variables (Ψ, n, p, *etc*) as described in *Volume I* of *Medici* manuals [125].

7.4. Design of GaN NDR Diodes

Criteria for possibility of sustained oscillations in a Gunn diode are based on the fact that the Gunn domain growth rate $1/\tau_{DDR}$ (see equation (7.8)) should be faster than the transit frequency $f_T = v_{PEAK}/L_A$. These considerations lead to ($N \times L$) criteria [132] for possibility of formation of Gunn domains, which can be expressed as:

$$(N_A \times L_A) > (N \times L)_0 \equiv \frac{3 \times \varepsilon \times v_{PEAK}}{q \times \mu_{NDR}} \tag{7.15}$$

where N_A is the doping and L_A is the thickness of the active layer, $\mu_{NDR} \equiv \max(-dv/dF)$, and v_{PEAK} is the peak electron velocity. The critical values of ($N \times L$) product for GaN and GaAs calculated using (7.15) and the material parameters of Table 7.1 are summarized in Table 7.2. The results show that, due to a higher peak velocity and a smaller negative mobility, $(N \times L)_0$ for GaN is *10* to *100* times larger than the GaAs $(N \times L)_0$. The latter is a very important result in terms of feasibility of GaN-based NDR diodes since the availability of low-doped GaN material ($N_A < 5 \times 10^{16} cm^{-3}$) is still limited.

Table 7.2. $(N \times L)_0$ Products and Critical Doping Levels for GaN and GaAs

Material	GaAs	*Zb* GaN	*Wz* GaN
$(N \times L)_0$, $[cm^{-2}]$	0.1×10^{11}	2.5×10^{12}	8.2×10^{12}
N_{CRIT} $[cm^{-3}]$	3.4×10^{15}	1.2×10^{18}	4.3×10^{18}

However, if N_A exceeds the critical doping concentration N_{CRIT} then the equilibrium charge density continuously remains larger than the domain charge density. Under such conditions, stable static domains can be formed inside the active layer [135]. Formation of parasitic static domains results in a decrease of output power and may lead to an early breakdown of Gunn diodes. Values of critical doping concentration N_{CRIT} for cases of GaN and GaAs were calculated using (7.16) and the results are listed in Table 7.2.

$$N_{CRIT} = \frac{\varepsilon \times F_{TH}^{\ 2}}{q} \tag{7.16}$$

Due to the large difference in threshold electric fields, the critical doping concentration in GaN is much higher than in GaAs and, thus, the active region in GaN diodes can be doped significantly higher ($\sim 10^{17} cm^{-3}$) than in GaAs designs ($\sim 10^{15} cm^{-3}$). Higher doping of active layers in GaN NDR diodes also allows to overcome large values of differential relaxation time τ_{DDR} in this material (see (7.8)), and helps to increase frequency capability up to *200GHz* for $N_A = 1 \times 10^{17} cm^{-3}$.

A typical GaN NDR diode designed to operate at *~100GHz* had a n-type active layer with thickness L_A of $3\mu m$ and doping N_A of $1 \times 10^{17} \text{cm}^{-3}$. The active layer was sandwiched between anode and cathode layers and their corresponding ohmic contacts as shown in Figure 7.7. Both contact layers were $0.1\mu m$-thick and doped at $1 \times 10^{19} cm^{-3}$.

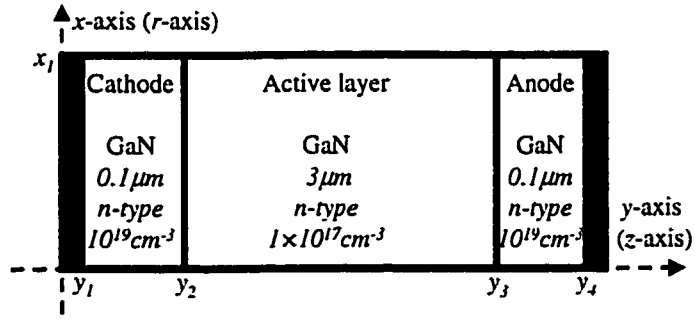


Figure 7.7. Two-dimensional cross-section of considered GaN NDR diodes

For simulation purposes, the rectangular cross-section of Figure 7.7 was divided into a fine triangular mesh of spatial nodes. The meshing was completed by transforming the two-dimensional *x-y* coordinates into the cylindrical *r-z* coordinates (devices are assumed to be symmetrical about the azimuthal angle θ). During the transformation to

cylindrical coordinates, the two-dimensional mesh was rotated 2π around the y-axis (which becomes the z-axis). Thus, the diameter of a typical GaN NDR diode D was twice the width of the original cross-section and was selected to be $50\mu m$. A final three-dimensional model of GaN NDR diode is shown in Figure 7.8 together with the bias supply and small-signal equivalent elements of the active layer: conductance G and susceptance B.

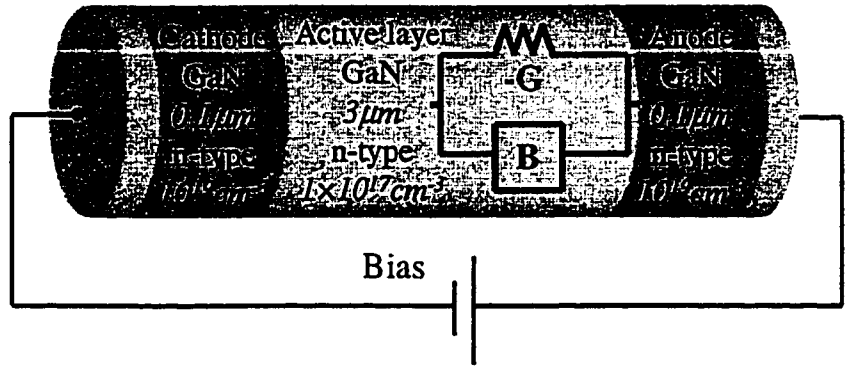


Figure 7.8. *3-D* model of GaN NDR diode used in computer simulations

Operating conditions of the proposed GaN NDR diode oscillators, their stability to small-signal perturbations, and the their frequency capabilities were evaluated using DC and small-signal high-frequency simulation techniques as described in the following sections. Since availability of the *Zb* phase of GaN is limited, material parameters corresponding to *Wz* GaN were used for all following studies unless otherwise specified.

7.5. Small-Signal Analysis of GaN NDR Diode Oscillators

During the operation of a GaN NDR diode, bias V_D is applied to the anode contact. If the bias is smaller than the critical value $V_{CR}=F_{TH}\times L_A$, the DC I-V characteristics of the device appear to be that of a small resistor. An application of V_D exceeding V_{CR} leads to an outside electric field $F > F_{TH}$ leading to device operation in a region of NDR according to the v-F characteristics. Under such operating conditions, the device may become unstable, and its stability and the shape of DC I-V characteristics depend on termination impedance Z_L. When a GaN NDR diode is biased using a voltage source as shown in Figure 7.8, it is terminated with a short circuit ($Z_L=0\Omega$). Most of the investigated GaN NDR diodes and GaAs Gunn diodes are stable when terminated with

$Z_L=0\Omega$ and, thus, it was possible to investigate their DC and small-signal high-frequency characteristics using steady-state hydrodynamic simulations described earlier.

7.5.1. Operating Conditions of GaN NDR Diodes

Simulated DC I-V characteristic of a GaN NDR diode with $L_A=3\mu m$, $N_A=5\times10^{16}cm^{-3}$, and $D=50\mu m$ are shown in Figure 7.9. For comparison purposes, the figure also includes I-V characteristics of a sample GaAs Gunn diode obtained using the same simulation approach. The sample GaAs Gunn diode had the same-size active layer: $L_A=3\mu m$ and $D=50\mu m$, but the doping of the active layer N_A was reduced to $3\times10^{15}cm^{-3}$ in order to satisfy the design condition $N_A < N_{CRIT}$. This design was analogous to published descriptions of Ka-band Gunn diodes [134].

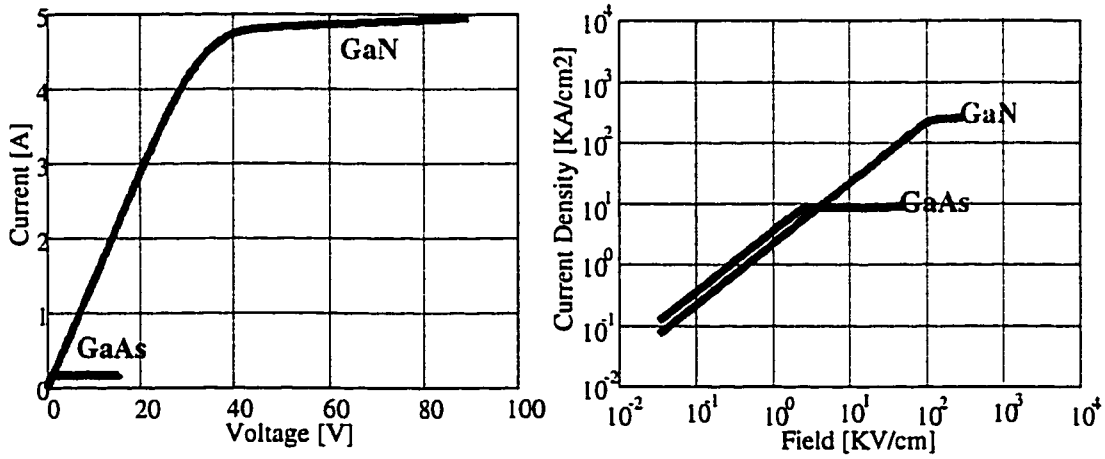


Figure 7.9. DC *I-V* and *J-F* characteristics simulated for a GaN NDR diode and a GaAs Gunn diode

The results of Figure 7.9 indicate that GaN NDR diodes have significantly higher voltage and current handling capabilities. Thus, operational current density of GaN NDR diodes and GaAs Gunn diodes was $250KA/cm^2$ and $10KA/cm^2$, respectively. Gunn diodes are typically biased with V_D of $\sim2\times V_{CR}$ corresponding to an outside electric field of $2\times F_{TH}$ and these biasing conditions were used for further studies. The biasing voltages for the GaN and GaAs diodes with $3\mu m$-thick active layers were $90V$ and $2.1V$, respectively.

7.5.2. Small-Signal Characteristics of GaN NDR Diodes

The small-signal equivalent circuit of a GaN NDR diode is shown in Figure 7.8 and consists of admittance $Y_D=G_D+jB_D$. Frequency and bias dependence of high-frequency conductance G_D and shunt capacitance $C_D=B_D/\omega$ were evaluated using small-signal *AC* simulation capability of *Medici*. The small-signal extraction of G_D and C_D is performed by analyzing solutions of previously obtained steady-state analysis. During the *AC* analysis a sinusoidal input of given frequency was applied to the contact terminals and the corresponding sinusoidal currents and voltages were calculated following procedure described in [125]. The complex small-signal current and voltage amplitudes were used to calculate small-signal conductance G_D and capacitance C_D using (7.17):

$$Y_D = G_D + j\times\omega\times C_D = \frac{\tilde{I}_D}{\tilde{V}_D} \tag{7.17}$$

The bias dependence of G_D and C_D was evaluated for a GaN NDR design with $L_A=3\mu m$, $N_A=1\times10^{17}cm^{-3}$, and $D=50\mu m$. The small-signal elements were extracted at the transit frequency $f_T=v_{PEAK}/L_A=100GHz$ and the results are shown in Figure 7.10.

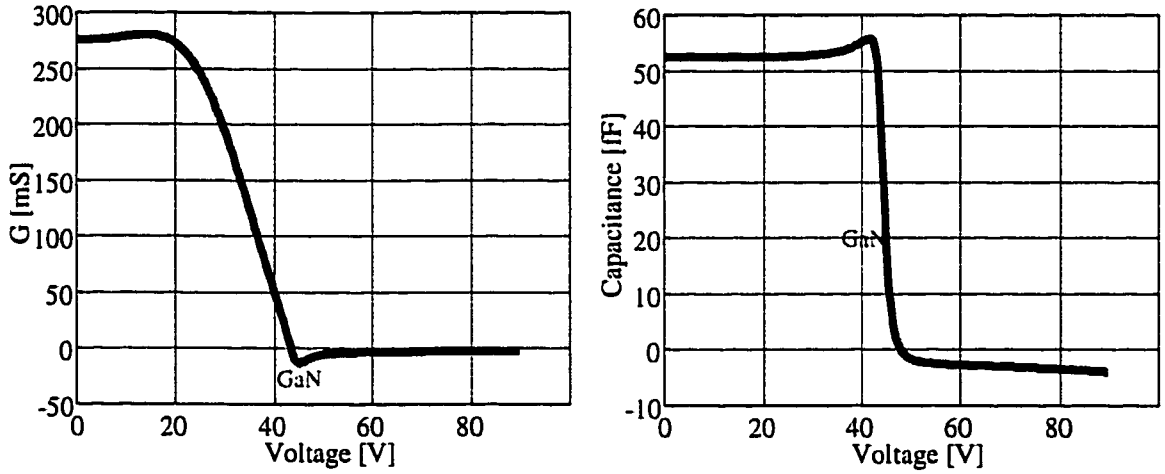


Figure 7.10. Bias dependence of G_D and C_D for a GaN NDR diode

For low values of bias, the small-signal conductance G_D is constant at about *270mS* (R_D of *3.7Ω*), as the bias is increased, G_D increases slightly to *280mS* and then sharply decreases. G_D turns negative near the critical bias V_{CR} and has a peak value of *–15mS* at the critical bias ($V_{CR}=45V$). For higher bias, G_D saturates at *–2.5mS*. At low bias, the shunt capacitance C_D is constant at about *53fF*. When bias is increased pass the

critical value, C_D sharply drops. Negative values of C_D (*-2fF* to *-4fF*) observed for $V > V_{CR}$ should be interpreted as an inductance of the slow-moving Gunn domains. Similar trends were observed for GaAs Gunn diodes.

It should be noted that Gunn domains manifest inductive behavior only within the framework of small-signal stability analysis. Experimental observation and large-signal simulations, discussed further, show that full-grown Gunn domains are capacitive due to large charge density inside the fully-grown domains. The small-signal conductance of the GaN is also transformed under large-signal conditions. As the amplitude of oscillations increases, G_D decreases until conditions for sustained oscillations are achieved.

Frequency dependence of the small-signal conductance G_D was evaluated for the GaN NDR diode under the biasing conditions $V_D = 2 \times V_{CR}$. The results are shown in Figure 7.11. At low frequencies, G_D had a small positive value corresponding to *1KΩ* of DC resistance. The value of G_D oscillated with frequency and was negative in the range between *40* and *110GHz*, which corresponding to the self-resonant transit-time frequency of *100GHz* of this design. The regions of negative conductance were repeated around second (*200GHz*) and third (*300GHz*) harmonics of the transit-time frequency.

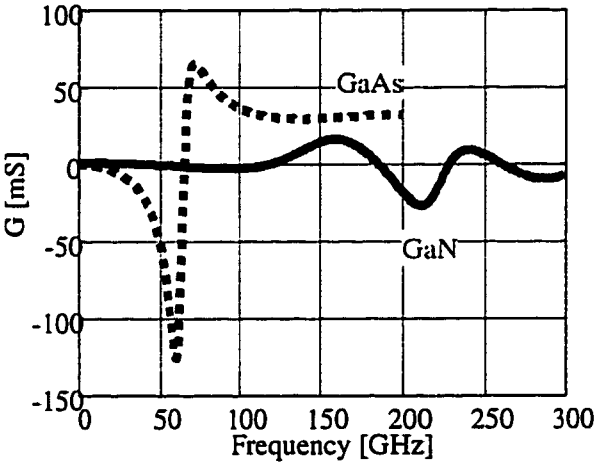


Figure 7.11. Frequency dependence of G_D for a GaN and GaAs NDR diodes

For comparison purposes, frequency dependence of the small-signal conductance was also investigated for case of the GaAs Gunn diode with *3μm*-thick active layer doped at $3 \times 10^{15} cm^{-3}$. The GaAs small-signal conductance also was negative for frequency range around its transit-time frequency of *50GHz* (between *2.5* and *60GHz*), but unlike the GaN

case, the GaAs conductance remained positive at higher harmonics of the transit-time frequency. This difference in high-frequency characteristics is attributed to the low value of NDR relaxation frequency f_{NDR} in GaAs, which limits frequency-capability of GaAs-based NDR devices to frequency below *100GHz*. On the other hand, frequency-capability of a GaN NDR diode with $3\mu m$-thick active layer doped at $1\times10^{17}cm^{-3}$ approached *300GHz* due to higher electron velocities and shorter NDR relaxation times in this material.

7.5.3. Stability Analysis of GaN NDR Diode Oscillators

($N\times L$) criteria explained in Section 7.4 provided only an initial assessment for possibility of Gunn instabilities in an NDR device. An exact analysis of NDR device stability to high-frequency small-signal perturbations is carried out by applying Nyquist criteria to the impedance function Z_D following discussions in [132] and [144]:

$$Z_D = R_D + jX_D = \frac{G_D}{G_D^2 + B_D^2} + j\frac{-B_D}{G_D^2 + B_D^2} \tag{7.18}$$

Figure 7.12 shows the Nyquist diagram of R_D and Z_D obtained for the GaN NDR diode of the previous section. The stability of the frequency-dependent impedance $Z_D=R_D+j\times X_D$ is determined by tracing its position on the Nyquist diagram as the frequency is varied between $-\infty$ and $+\infty$ (impedance values at negative frequencies are obtained by reversing the sign of X_D). Completing the motion from DC to infinite positive frequency along the curve in Figure 7.12 moves Z_D from *Quarter II* to *III*, from *III* to *IV*, from *IV* to *I*, from *I* back to *II*, from *II* again to *III*, and finally from *III* to *II*, from where it converges to origin at $+\infty$. The origin is encircled twice, and, thus, this device is unstable when operated with a zero impedance source. An oscillator using the GaN NDR diode of Figure 7.12 will still oscillate if terminated with a different load, as long as the total impedance Z_{OSC} still encircles the origin.

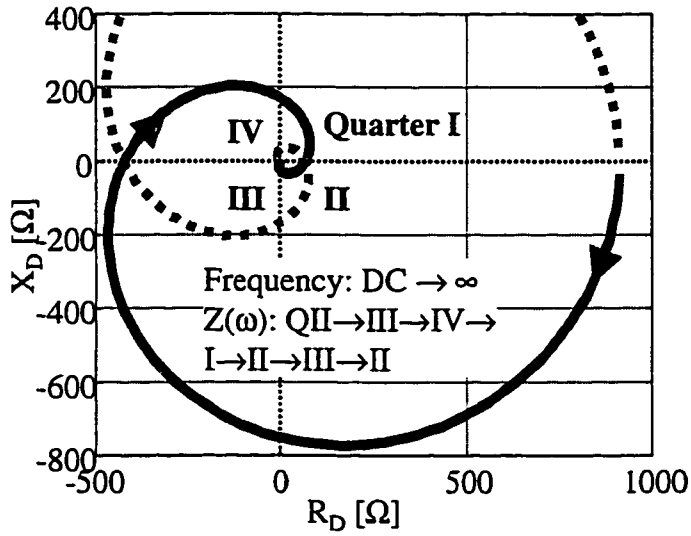


Figure 7.12. Nyquist diagram of resistance and reactance as a function of frequency for a GaN NDR diode.

Stability of a semiconductor device in a circuit environment is better analyzed by applying Nyquist criteria to the closed-loop transfer function and examining its position around the point of positive feedback, which is represented by *–1,0* on the complex plane. The closed-loop transfer function of the GaN NDR diode oscillator is given by its small-signal gain, which is characterized by the scattering parameter S_{11}:

$$S_{11} = \frac{Z_D - Z_L}{Z_D + Z_L} \tag{7.19}$$

where Z_L is the load impedance. The possibility of oscillations, as well as the oscillation frequency and the small-signal gain of the circuit are affected by the selection of the load impedance Z_L. The Nyquist diagrams of the GaN NDR oscillator obtained for cases $Z_L=50\Omega$ and $Z_L=50\Omega-204j\Omega$ are shown Figure 7.13. No oscillations are expected for a $Z_L=50\Omega$ termination since S_{11} does not encircle *–1,0* point. On the other hand, when the GaN NDR diode is terminated with $Z_L=50\Omega-204j\Omega$, S_{11} encircles the positive feedback point twice.

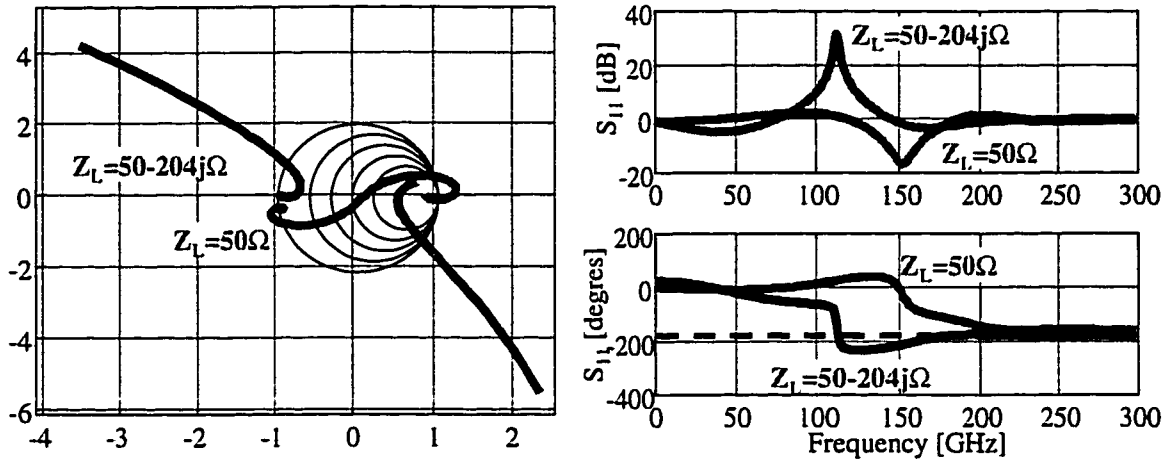


Figure 7.13. Nyquist diagram and Bode plot of the GaN NDR diode oscillator obtained for Z_L=*50Ω* and Z_L=*50-204jΩ*.

The frequency and the small-signal gain of the GaN NDR diode oscillator are determined from Bode plot. The Bode plot for the GaN NDR diode oscillators with Z_L=*50Ω* and Z_L=*50-204jΩ* is shown in Figure 7.13. When the load was *50Ω*, the phase of S_{11} is shown to never reach the oscillation margin of *–180 degrees* making oscillations impossible, although a positive gain was also present in this case. On the other hand, the phase of S_{11} for Z_L=*50-204jΩ* crosses a *–180-degrees* line at the oscillation frequency of *110GHz*, at which point the small-signal gain has a maximum value of *~32dB*.

Overall, DC and small-signal hydrodynamic numerical simulations allowed determination of operating conditions and evaluation frequency capabilities of GaN NDR diode oscillators. Nyquist criteria were applied to design a GaN NDR diode oscillator which was biased at *90V* and had small-signal oscillation frequency of *110GHz*.

7.6. Large-Signal Analysis of GaN-based NDR Diodes

Since in practice GaN NDR diode oscillators operate under large-signal conditions, the small-signal analysis techniques developed in the previous section could not be used to obtain accurate predictions of their power and frequency capabilities. This section introduces transient hydrodynamic simulations used to evaluate large-signal characteristics of GaN NDR diode oscillators and describes results obtained by analysis and optimization of these oscillators.

7.6.1. Transient Large-Signal Simulations of GaN NDR Diode Oscillators

Time-dependent coupled solutions of the hydrodynamic equations were obtained by applying Newton's numerical differentiation and integration method to spatial distributions of electron concentration, potential, electric field, and electron velocity [125]. During simulations of GaN NDR diode oscillators, additional boundary conditions for terminal voltages and currents were used to represent loading impedance Z_L (shown in Figure 7.14) as necessary for oscillator operation.

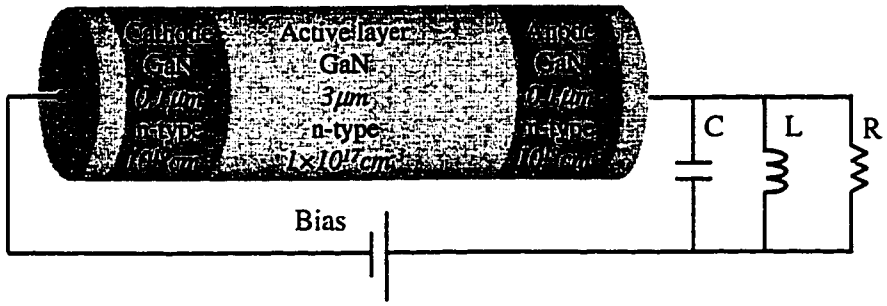


Figure 7.14. Schematics of GaN-based NDR diode oscillator

The boundary conditions were based on Kirchhoff equations for a parallel *LCR* circuit inserted between the bias supply and the anode contact of the NDR diode:

$$\frac{V_A-\phi}{R}+C\frac{d(V_A-\phi)}{dt}+I_L-I=0$$
$$V_A-\phi-L\frac{dI_L}{dt}=0 \qquad (7.20)$$

where V_A is the anode bias, Φ is the Fermi potential at the anode, I is the anode current, and I_L is the current in the inductor L.

Transient large-signal simulations were used to extract profiles of electron concentration and electric field as a function of time and demonstrated formation and propagation of Gunn domains in GaN devices as is described in the next section.

7.6.2. Formation and Propagation of Gunn Domains in GaN NDR Diodes

A nominal $3\mu m$-thick $1\times10^{17}cm^{-3}$-doped GaN NDR diode was connected to a parallel *LCR* circuit with $L=17.5pH$, $C=0.1pF$, and $R=50\Omega$. Starting at time zero, V_D was increased from 0 to $90V$ with a large rise time of $>1ns$ in order to minimize voltage

overshoot. Transient hydrodynamic simulations were used to extract profiles of electric field and electron concentration along the active region from cathode to anode a function of time at *1ps* intervals starting at *1.4ns*.

Initial bias application resulted in an outside electric field F of *300KV/cm*. Carrier diffusion from the contacts lowers the electric field near the cathode as shown in Figure 7.17. Electrons within this region move at an increasingly higher velocity as dictated by the v-F characteristics.

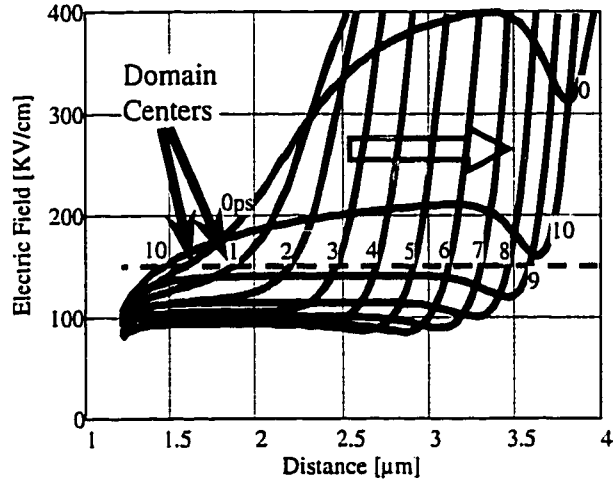


Figure 7.15. Formation and propagation of Gunn domains: electric field.

Leaving this region, electrons exhibit velocity overshoot (as shown in Figure 7.16) and then slow down to $v_{SAT}(F)$ corresponding to the local electric field. The resulting field configuration leads to carrier acceleration in one part of the device where $F < F_{TH}$ and carrier slowdown in the region where $F > F_{TH}$. A pileup of carriers is consequently created resulting in the formation of an accumulation-layer domain as shown by the corresponding electron concentration profile in Figure 7.17. The center of the domain corresponds to the region of maximum electron concentration, which is also the location where the local electric field is equal to the threshold field F_{TH}.

At the following intervals, the domain screens and lowers the electric field to its left while the electric field on the right is increased (see Figure 7.15). Because of this change, the region with peak electron velocity moves to the right (as shown in Figure 7.16). This corresponds to an effective move of the accumulated domain towards the anode at a domain velocity v_{DOM} of $\sim 2.9\times10^{7} cm/sec$.

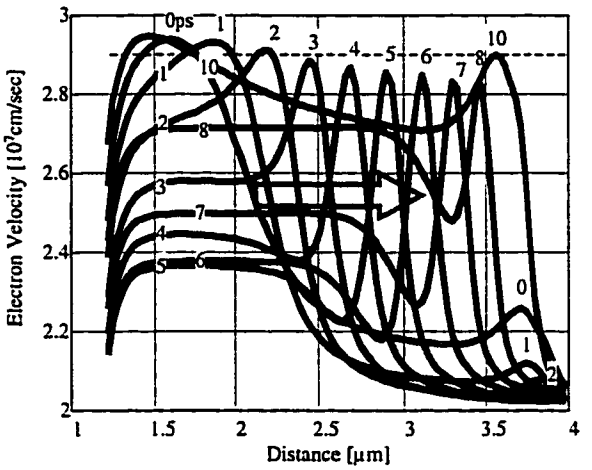


Figure 7.16. Formation and propagation of Gunn domains: electron velocity.

The domain grows as it propagates (see Figure 7.17) because the foremost electrons are slowed down even further by the presence of a higher field. Carrier accumulation continues until the domain reaches the anode and is absorbed by it after which the cycle is repeated.

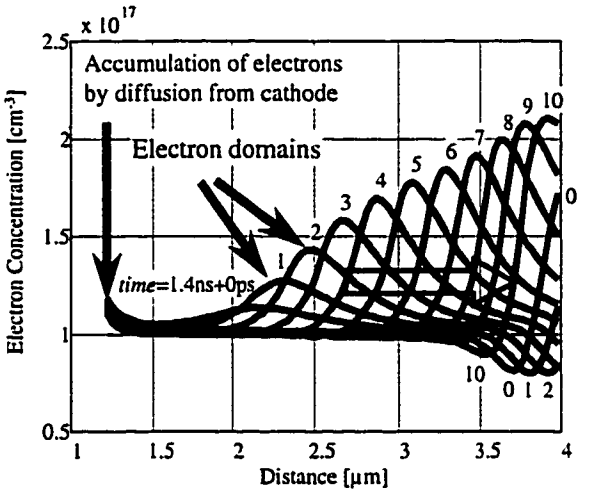


Figure 7.17. Formation and propagation of Gunn domains: electric concentration.

Operation of the GaN NDR diode corresponds in this case to the transient accumulation-layer mode. The analysis presented above confirms that GaN diodes can operate under conditions that lead to signal generation. The period of observed oscillations was *~11ps* corresponding to an oscillation frequency of *~90GHz*.

7.6.3. Large-Signal Harmonic Analysis of GaN NDR Diodes

Transient large-signal simulations of the previous section were further used to obtain current and voltage time waveforms corresponding to the described oscillations. The voltage and current time waveform recorded for time interval between *0* and *1.8ns* are shown in Figure 7.19. The figure shows emergence of oscillations in voltage and current when the bias exceeds the critical voltage V_{CR}=*45V*. Gradual build-up of the amplitude of current oscillations is shown in Figure 7.18 (see inset). The growth of oscillations takes place over *0.5ns* and is followed by sustained oscillations as shown in the figure.

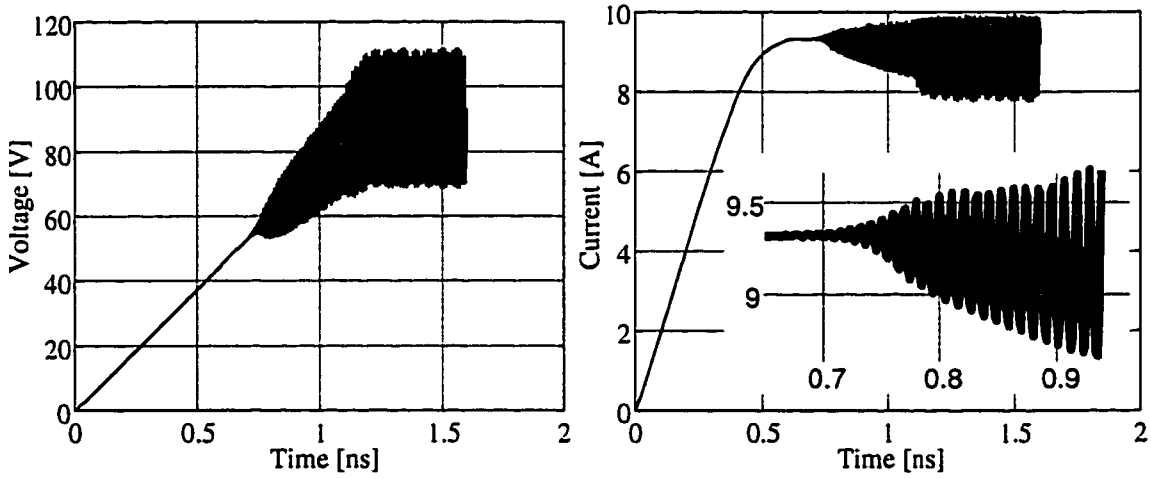


Figure 7.18. Voltage and current waveforms of GaN NDR diode oscillator

The dynamic load line corresponding to sustained oscillations of Figure 7.18 is shown in Figure 7.19 together with a DC I-V curve simulated for case when the GaN diode was connected directly to a voltage source. The reduced value of the quiescent current in this figure is caused by the presence of sustained oscillations. Experimentally observed NDR in the I-V characteristics of Gunn-diode oscillators confirms this trend.

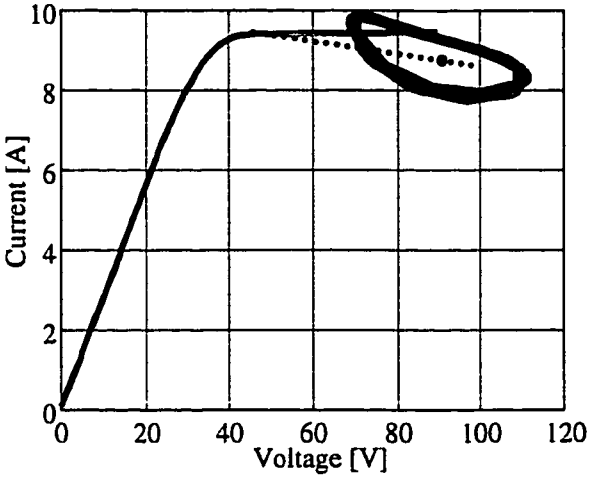


Figure 7.19. Dynamic load-line and I-V characteristic of GaN NDR oscillator

The regions of voltage *V(t)* and current *I(t)* waveforms corresponding to sustained oscillations were subjected to harmonic power analysis. First, the frequency of oscillations was determined using standard *IEEE* algorithms [145] and then the output power spectrum of the instantaneous power wave was calculated used fast Fourier transforms. The obtained spectrum of the output power is shown in Figure 7.20. It should be noted that fine frequency resolution of the calculated spectrum was achieved by simulating long time-trains (*>20 cycles*) of in the region of sustained oscillations. High resolution in spectral power components was achieved by ensuring that at least 16 points per cycle were recorded during the simulations.

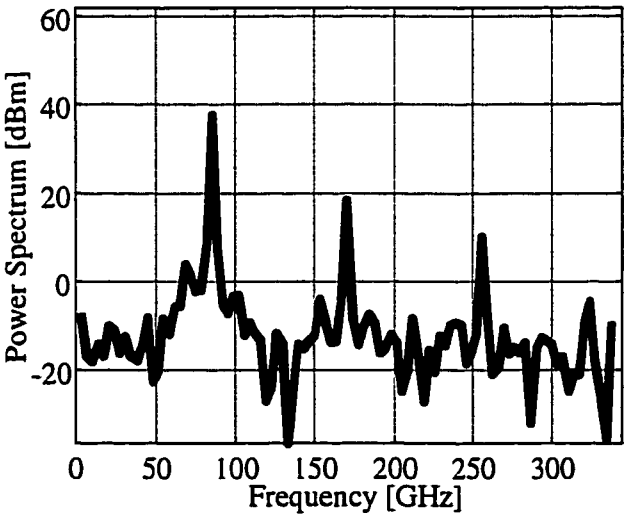


Figure 7.20. Output power spectrum of GaN NDR diode oscillator

The oscillation frequency of the GaN NDR diode oscillator employing *3μm*-thick *50μm*-diameter GaN NDR diode was *87GHz*. Considering the employed *LCR* circuit parameters (*L=17.5pH*, *C=0.1pF*, and *R=50Ω*.) and the oscillation frequency, the large-signal capacitance of the GaN NDR diode was *~100fF*. The fundamental output power was *37.6dBm* corresponding to the power density of $2\times10^5 W/cm^2$, while conversion efficiency was *0.73%*.

This modest value of conversion efficiency compared with the Gunn diode theoretical limit of $\eta=8/\pi^2\times(v_{PEAK}-v_{SAT})/(v_{PEAK}-v_{SAT})$ of *15%* is attributed to a low value of the quality factor ($R/\omega L=\sim5.4$) of the *LCR* circuit used to represent the resonant cavity.

7.6.4. Optimization of Operating Conditions for GaN NDR Oscillators

The impact of the biasing voltage V_D and the terminating impedance $Z_L(LCR)$ on the frequency, output power, and efficiency of the GaN NDR oscillators was investigated in order to optimize its operating conditions.

The results of the study are shown in Figure 7.21. The frequency of oscillations decreased steadily from *98* to *83GHz* as the bias was increased from *55* to *125V* in agreement with the experimental trends observed for GaAs Gunn diodes [146].

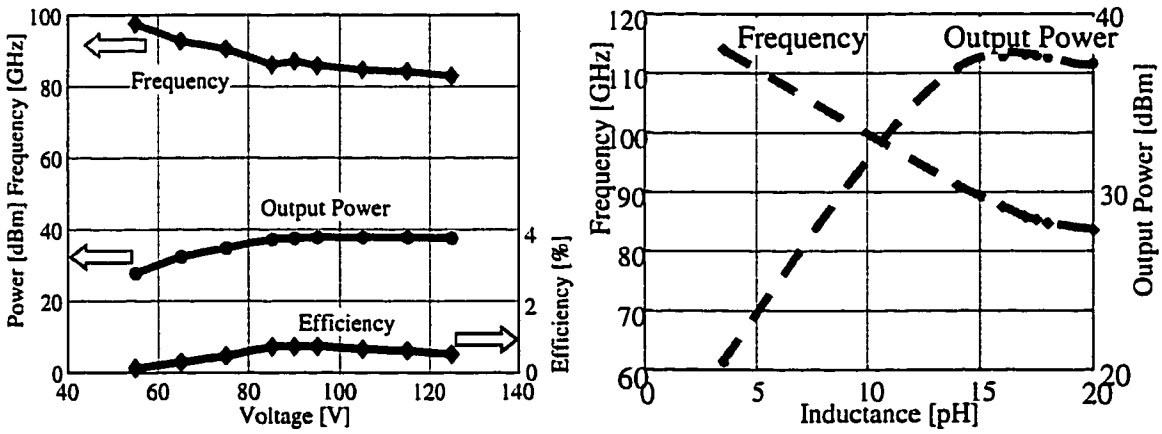


Figure 7.21. Variation of the output power, frequency, and efficiency of GaN NDR diode oscillator with bias and terminating load

The output power increased steeply once the applied bias exceeded V_{CR}, and saturated for $V_D>2\times V_{CR}$. A slight decrease observed for $V_D>3\times V_{CR}$ is attributed to an ensuing mismatch between the large-signal impedance of the GaN NDR diode and the

terminating impedance Z_L, which was determined by the *LCR* circuit. The conversion efficiency was maximal for $V_D=2\times V_{CR}$ and this bias was employed for performing comparative studies of various GaN NDR diode oscillators.

The terminating impedance Z_L was optimized by varying its parameters: inductance L, capacitance C, and resistance R. The results obtained when L was varied between *3* and *20pH* are shown in Figure 7.21. As expected, the oscillation frequency was reduced from *115GHz* to *85GHz* and the output power was maximal when L had an optimal value of *17pF*. Similar trends were observed during optimization of the terminating capacitance around its optimal value of *0.1pF*. The output power and frequency remained practically constant when the terminating resistance R was varied between *50* and *450Ω*, and thus a more practical value of *50Ω* was selected. This cavity design was used for performing further simulations.

7.7. Evaluation of Frequency and Power Capabilities of GaN NDR Sources

The power and frequency capabilities of GaN NDR diodes were compared with that of GaAs Gunn diodes by simulating the performance of the corresponding oscillators while modifying the thickness L_A and the doping N_A of the active layer in these devices.

The nominal GaAs Gunn diode had the same dimensions as the nominal GaN NDR diode: $L_A=3\mu m$ and $D=50\mu m$, but the doping was reduced to $3\times10^{15}\text{cm}^{-3}$ in order to satisfy the design condition $N_A < N_{CRIT}$ (see Table 7.2). This design of GaAs Gunn diode was analogous to published descriptions of Ka-band Gunn diodes in reference [147]. The bias V_D for both GaN- and GaAs-based devices was selected to be twice the critical bias V_{CR} and, for nominal designs, was *90V* and *2.1V*, respectively. Designs of *LCR* circuits for GaN (*L=17.5pH*, *C=0.1pF*, *R=50Ω*) and GaAs (*L=25pH*, *C=0.45pF*, *R=50Ω*) were optimized to provide maximum output power when used with devices of nominal designs.

The results of the study conducted by varying the thickness of the active layer are shown in Figure 7.22. All devices demonstrated expected trends of increasing the oscillation frequency and decreasing the output power when the thickness of the active layers was reduced. Reduction of output power for GaN NDR diodes with thicker than

3μm active layers was due to an increasing mismatch with the resonant cavity. An even more significant degradation was observed for GaAs Gunn diodes and special care was taken in that case to re-optimize Z_L for devices with thicker active layers. The frequency-power tradeoff of GaAs Gunn diodes was restored by proper choice of Z_L and only the re-optimized results are shown in Figure 7.22.

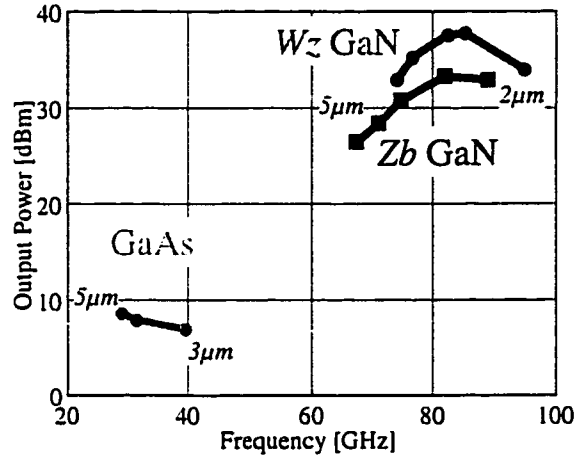


Figure 7.22. Power-frequency diagram for GaN NDR diode and GaAs Gunn diode oscillator for devices with active layer width between *2* and *5um*

In this study GaN NDR diodes made of both *Wz* and *Zb* phases of GaN were simulated in order to account for uncertainty in published *v-F* characteristics. The simulations showed that the overall characteristics of GaN-based NDR diodes outperform those of GaAs Gunn diodes in terms of output power and frequency of oscillations independent of the specific *v-F* characteristics used to model material properties of GaN. Thus, given the same thickness of the active layer, the operation frequency of GaN NDR diodes (*65-95GHz*) was approximately twice that of GaAs Gunn diodes (*27-40GHz*), while given the same device area, the maximum output power of GaN NDR diodes was *~35dBm* compared with *~10dBm* for GaAs Gunn diodes.

The power-frequency capability of GaN *Wz* and *Zb* NDR diodes was also compared as a function of the doping of the active layer and the results are shown in Figure 7.23. When N_A was increased from $5\times10^{16}cm^{-3}$ to $5\times10^{17}cm^{-3}$ the oscillation frequency increased from *85* to *120GHz* due to reduced differential dielectric relaxation time in higher-doped devices.

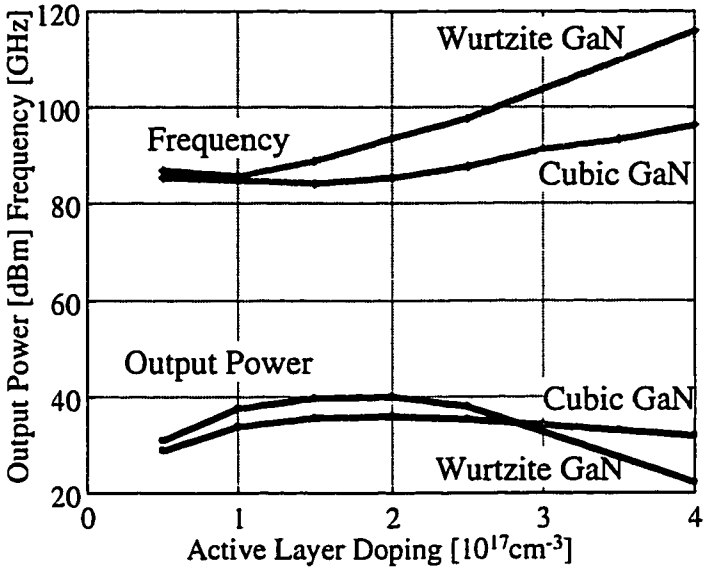


Figure 7.23. Power and frequency of *Wz* and *Zb* GaN NDR diode oscillators as a function of the doping of the active layer

Overall, when compared with GaAs Gunn diodes, GaN NDR diodes showed a significant improvement in terms of output power density and frequency. These results are supported by similar conclusions drawn with the help of the microwave signal generator figure-of-merit $Pf^2Z=F_B^2v_{PEAK}^2/4$, which measures the maximum output power (P) delivered from an oscillator to a matched impedance (Z) at a frequency (f) [132]. Based on the considered material properties, Pf^2Z for GaN is *50* to *100* times that of GaAs, indicating a strong potential of GaN for microwave signal generation.

7.8. Conclusions

In this chapter, a theoretical study is conducted to evaluate the microwave potential of wide bandgap GaN semiconductor for high-power signal generation as necessary for next-generation automotive and imaging radars operating at frequencies beyond W-band. Diverse numerical simulations were conducted to confirm that the postulated GaN *v-F* characteristics indeed lead to Gunn domain instability that can be exploited for design of GaN-based NDR oscillators. The Gunn diode ($N\times L$) criteria were used in defining device structures for GaN NDR diodes. Computer simulations allowed evaluation of DC I-V characteristics of GaN NDR diodes, their small-signal high-

frequency admittance characteristics, and corresponding equivalent-circuit elements. Design of the GaN-based NDR diode oscillators was analyzed using Nyquist criteria.

Transient large-signal hydrodynamic simulations were used to evaluate power and frequency capabilities of GaN NDR oscillators. Microwave characteristics of GaN NDR diodes were evaluated and compared with those of GaAs Gunn diodes. The results obtained on GaAs devices showed good agreement with experimentally reported data. It was found that due to reduced time constants, GaN NDR diodes offer higher frequency operation capability (up to *120GHz* for *3μm*-thick diode), while the output power density exceeds $10^5 W/cm^2$, and is therefore at least *100* times higher than that of GaAs devices. The improvements offered by the wide-gap semiconductor are due to a significantly higher electrical strength which allows operation with higher doping levels and at a higher bias, than in conventional narrow-gap III-V semiconductors.

CHAPTER 8
CONCUSIONS AND SUGGESTIONS FOR FUTURE STUDIES

In this work, InP- and GaN-based devices and their applications to millimeter-wave signal control and generation applications were designed, fabricated, and characterized. The following sections summarize developments and contributions made during these studies and offers suggestions for future research. Thus, the first part of the thesis describes switching InP-based PIN diodes and their applications to W-band monolithic switches and phase-shifters for emerging automotive and imaging applications. The second part of the thesis addresses an application of wide-bandgap GaN-based semiconductors to high-power microwave signal control and generation.

8.1. Summary and Conclusions

A set of analytical equations was used to model InGaAs PIN diodes and allowed evaluation of such fundamental properties of InGaAs as breakdown field (*~180KV/cm*) and low-level recombination lifetime (*~1.4ns*). Based on theoretical considerations, a practical small-signal equivalent-circuit model for switching InGaAs PIN diodes was introduced. A numerical simulator for InGaAs PIN diodes was developed based on quasi-3D drift-diffusion approach. Results of these numerical simulations allowed a more precise evaluation of the high-frequency characteristics and consequent optimization of InGaAs PIN diodes for millimeter-wave switching applications. Thus, an optimal design for W-band employed a *1-1.5μm*-thick I-layer and had a diameter of *8-10μm*.

Millimeter-wave MMIC process technology for InP-based InGaAs PIN diodes was developed. The diodes were fabricated using wet etching and lift-off metalization techniques. Electroplated Au airbridges were used for connecting the diodes with the rest of the circuit.

The switching InGaAs PIN diodes were characterized at low frequency by I-V and C-V measurements and at high frequency by small-signal S-parameter and large-signal power measurements. A typical InGaAs PIN diode had a low turn-on voltage of *0.4V* and a high breakdown voltage of *20V*. Temperature-dependent DC characterization of InGaAs PIN diodes was used to establish that reverse breakdown in InGaAs PIN diodes under study occurred via impact ionization. Thermal nature of the S-shaped NDR in the ON-state I-V characteristics of PIN diodes was determined by pulsed I-V characterization. The minimum electron concentration of $\sim 2\text{-}3\times10^{15}cm^{-3}$ for non-intentionally-doped (nid) InGaAs was determined by low-frequency C-V characterization.

Coplanar single-pole single-throw (SPST) InGaAs PIN diode switches were formed by inserting the diodes in series with coplanar-waveguide transmission lines. Small-signal S-parameters of the switches were measured and demonstrated good switching characteristics with insertion loss of *0.5dB* and isolation of *19dB* for frequencies up to *40GHz*. S-parameters of discrete InGaAs PIN diodes were extracted from the switches' characteristics and were used to evaluate small-signal equivalent-circuit models of the diodes. Next, the extracted PIN models were used for designing W-band InP-based MMICs, which used InGaAs PINs as switching elements.

Microstrip W-band InGaAs PIN monolithic switches and phase shifters were designed with the help of *HP EEsof Libra* and *Momentum* simulators. After the circuits were optimized, their layouts were generated using custom-made layout scripts, which allowed immediate placement of the generated designs on lithographic fabrication masks.

W-band InP-based microstrip MMICs relied on backside via holes for high-frequency grounding. A low-inductance InP backside-via technology was developed for this purpose and allowed realization of high-performance InP-based microstrip circuits.

W-band InP-based InGaAs PIN diode microstrip SPST switches were fabricated and demonstrated state-of-the-art performance at W-band frequencies. W-band SPST switches with a single InGaAs PIN diode had low insertion loss of *1.2-1.3dB* and high-isolation of *23-25dB*. A high-isolation *94GHz* SPST switch with two InGaAs PIN diodes showed a record-high isolation in excess of *35dB*. This state-of-the-art performance of InGaAs PIN diode switches was accompanied by reduced DC power consumption

(*<1mW*) of InP-based technology vs. conventional GaAs-based solutions. Loaded-line InGaAs PIN phase shifters were also fabricated using InP-based microstrip technology and demonstrated a *90-degree* phase shift at *93GHz*.

Coplanar InGaAs PIN diode technology was developed and applied to design and fabrication of *77* and *94GHz* InGaAs PIN SPDT transceiver switches. The switches employed a specially designed transition between a switching PIN diode and a coplanar-waveguide, which allowed low-inductance shunt mounting of the diodes. Coplanar W-band SPDT switches employing low-parasitics InGaAs PIN-CPW transitions demonstrated low insertion loss of *1.6dB*, small crosstalk of *-30dB*, and record isolation of *43dB*. Low-parasitics coplanar technology was also used to realize W-band reflection-type InGaAs PIN diode phase shifters with constant time-delay and constant phase-shift properties. Reflection-type phase shifters demonstrated low insertion loss (*<2dB*) and wide bandwidth in excess of *10GHz*.

An automated on-wafer large-signal characterization system has been developed for W-band frequency applications. The system employed was intended for measuring load-pull and power-saturation characteristics of submillimeter-wave devices directly at their design frequency of operation. Its capabilities were demonstrated by evaluating constant-loss contours and large-signal characteristics of W-band InGaAs PIN MMIC switches at *77* and *102GHz*. The InGaAs PIN diode switches did not demonstrate any degradation of switching characteristics for input power levels up to the maximum available from a W-band source power of *12dBm* at *102GHz*.

The power-handling capabilities of InGaAs PIN diode switches were evaluated by large-signal power measurements at a lower frequency where higher-power sources were available. Power-handling capability of W-band InGaAs switches was comparable to that of GaAs and exceeded *20dBm* when the InGaAs switch was biased with a practical OFF-state bias of *–2V*. A discrete InGaAs PIN diode measured at *10GHz* demonstrated a high isolation of *20dB* and a low insertion loss of *0.5dB* under a high input power of *26dBm* for V_{ON} and V_{OFF} of *0.5V* and *–12V*, respectively.

The switching time characteristics of InGaAs PIN diodes were studied in order to determine their modulation-rate capabilities. Very short switching times (*130ps* and

250ps) were demonstrated by InGaAs PIN diode switches, which allowed operation with a very high switching rate of *5Gbps*. The switching mechanisms were identified and related to material properties by analyzing the amplitude and size dependence of the PIN switching times. The bulk recombination lifetime in the nid-InGaAs was estimated to be *1.4ns* and was reduced to *1ns* in small-size diodes due to surface effects.

Overall, InGaAs PIN MMICs for switching and phase-shifting applications were realized and demonstrated state-of-the-art performance at W-band frequencies. The developed InP-based PIN-diode monolithic-circuit technology offers multiple advantages compared with the conventional GaAs-based MMICs, namely: increased isolation, reduced DC power consumption, comparable RF-power handling, fast switching, and compatibility with high-frequency low-power InP-based electronics. It is expected that monolithic integration of switching InGaAs PIN diodes with InAlAs/InGaAs/InP HEMTs will enable demonstration of a monolithic InP-based millimeter-wave transceiver for automotive and imaging applications at W-band frequencies.

Scalability of large-signal characteristics of AlGaN/GaN HFETs as desired for power MMIC devices was evaluated by performing on-wafer load-pull characterization. AlGaN/GaN power HFETs with gate widths up to *1mm* showed excellent scalability of output power density (*~1W/mm*) and power-added efficiency (*30%*). *1-dB* gain compression occurred at input power levels varying from *-1dBm* to *10dBm* as the gate width was increased from *0.2* to *1mm*, while the associated gain remained almost constant at *~16dB*.

AlN/GaN MIS heterostructures grown by MOCVD at the University of Michigan were investigated for purpose of developing GaN-based MISFETs. C-V characterization analysis demonstrated low values of interface state density (*$\sim 10^{11} cm^{-2} eV^{-1}$*) which was confirmed by very high values of transconductance (*185mS/mm*) and drain current density (*>700mA/mm*) obtained from MISFETs fabricated on these layers. Overall, these results indicated an excellent potential of GaN-based HFETs for power microwave switching applications.

In the last part of the thesis, the possibility of using wide bandgap GaN-based semiconductors for microwave signal generation based on the active-device properties of

GaN NDR diodes were evaluated for the first time. For this purpose, physical-based hydrodynamic simulations were developed and utilized to confirm that the postulated GaN *v-F* characteristics indeed lead to Gunn domain instability that can be exploited for design of GaN-based NDR oscillators. These simulations were used to study DC I-V characteristics of GaN NDR diodes, their small-signal high-frequency admittance characteristics, and corresponding equivalent-circuit elements, as well to analyze their small-signal stability using Nyquist criteria and Bode plots.

Power and frequency capabilities of GaN NDR diodes and GaAs Gunn diodes were evaluated by large-signal harmonic analysis of the corresponding diode oscillators. For this purpose, transient large-signal hydrodynamic simulations were used to obtain time-domain current and voltage time waveforms corresponding to sustained oscillations. The frequency and power of sustained oscillations were evaluated by specially developed *Matlab* scripts based on Fourier-transform techniques.

Results of the performed studies showed that GaN offers higher frequency operation capability (possibly up to *THz* region), while its power capabilities are at least *100* times higher than that of GaAs devices. The improvements offered by the wide-gap semiconductor are due to a significantly higher electrical strength which allows operation with higher doping levels, reduced time constants, and at a higher bias, than in conventional narrow-gap III-V semiconductors.

8.2. Suggestions for Future Work

Research following the work described in this thesis will focus on the following: (i) design and implementation of a W-band integrated HEMT/PIN transceiver, (ii) design and fabrication of GaN-based HFET MMICs for power switching applications; and (iii) design and fabrication of GaN NDR diode oscillators for microwave signal generation. Suggestions for the future work are presented in the following sections.

8.2.1. Monolithic Integration of InP-based PIN diodes with HEMTs

While the W-band InP-based InGaAs PIN diode MMICs developed in this work demonstrated excellent performance, the area of their applications can be extended

further by monolithic integration with active InP-based devices, such as HEMTs and HBTs. Thus, the realization of the amplifying HEMT MMICs and control PIN MMICs on a single InP chip would be an important advance in the development of monolithic W-band automotive radars, which are intended for high-volume commercial production.

There are several options for implementing integrated PIN/HEMT circuits. In the selective-growth technique, PINs and HEMTs are located in different areas of the wafer. When the PIN layers are grown, when the HEMT area is masked, and the HEMT layers are grown when the PIN area is masked. While the selective-growth technique allows optimizing both layers individually, it requires that the devices are located far from each other because of the poor material quality on the boundaries between PIN and HEMT areas. Moreover, selective-area growth also requires multiple epitaxial growth sequences, which is undesirable in cost-driven commercial applications.

Vertical integration of the layers, when PIN and HEMT layers are stacked on top of each other, has been successfully applied to optical photoreceivers. The HEMT layers are grown first, so the modulation of the channel is not affected by the thick high-doped layers of the PIN diode. Special caution should be taken to preserve the high quality of the HEMT layers during the consequent growth of the thick PIN diode layers. First integration efforts on stacked HEMT/PIN layers resulted in a successful fabrication of test devices. Preliminary characterization demonstrated no degradation of the characteristics due to the influence of the stacked layers. Future work will be concentrated on the development of an integrated InP-based PIN/HEMT high-performance millimeter-wave MMIC technology. An integrated transceiver would integrate a SPDT InGaAs PIN diode switch with transmit and receiver HEMT MMICs, as was discussed in the introduction to this thesis.

A further improvement to the performance of InGaAs PIN diode switches can be possible by employing micromachining technology for transmission-line fabrication. This novel technology would allow reduction of the transmission-line losses and realization of high-impedance transmission lines ($>100\Omega$), which is expected to increase isolation and reduce insertion loss at millimeter-wave frequencies.

8.2.2. Design and Fabrication of GaN-Based HFET Control MMICs and NDR Diode Generators

While AlN/GaN MISFETs and GaN-based NDR diodes studied in this work demonstrated promising electrical characteristics and expected to have very high frequency and power capabilities, these predictions need to be followed up by experimental verification. Due to the novelty of GaN device research, all areas of basic device and circuit research need to be addressed: layer growth, fabrication technology, and characterization techniques.

For example, successful realization of GaN devices depends on the availability of high-quality thick epitaxial layers of GaN with low background concentration and high electron mobility. While recent years has shown tremendous progress in the quality of GaN growth, vast majority of GaN epitaxial layers is still grown either on the lattice-mismatched hetero-substrates, which limits the availability of high-quality epitaxial material. The lateral-epitaxial overgrowth (*LEO*) and compliant-substrate techniques need to be investigated as possible means of improving the quality of epitaxial material.

Due to high chemical inertness of GaN, development of wet etching techniques for GaN-based fabrication technology is challenging. Low-damage wet etching instead of high-energy plasma etching is desired for fabrication of ohmic contacts with small contact resistance and gates with high Schottky barriers. A high-temperature ($>100°C$) or photo-assisted (deep UV) KOH- or NaOH-based etching processes needs to be developed and refined for this purpose.

Currently, the GaN ohmic contacts are based on Ti/Al metallization and have to be annealed at very high temperature of $800°C$, which causes problems with morphology and chemical stability of the contacts. The ohmic-contacts technology for GaN-based materials need to be optimized to provide better chemical and structural stability at high-temperature operating and processing conditions.

In order to realize high-frequency high-power potential of GaN-based HFETs submicron gate lithography needs to be optimized for use on high-resistivity sapphire substrates. At the same time more detailed theoretical and experimental studies of AlGaN/GaN and AlN/GaN interface and electron transport are necessary to improve

understanding of the piezoelectric effects in GaN-based materials, which would help in optimization of device layers.

The area of GaN NDR-diode oscillators also needs work in the area of basic device research. Thus, the performance of GaN NDR diodes could be enhanced by using heterojunction-injector or Schottky-cathode designs, which results in high electric field near the cathode. Thus, the width of parasitic "dead" zone would be reduced and the power and efficiency of the GaN NDR diodes would be increased.

The thermal limitations on power performances of GaN-based NDR diode oscillators and possibility of fabrication with substrate-removal should also be investigated. Thus, laser-ablation substrate-removal technique needs to be optimized in order to allow fabrication of discrete GaN NDR diodes with low thermal resistance as desired for these high-power devices.

High-power operating conditions and high-frequency response predicted for GaN-based devices would also require development of novel characterization techniques, such as high-power millimeter-wave probes with resonant cavities integrated on the probe.

Finally, design of GaN HFET control MMICs and GaN NDR oscillators requires more investigation and optimization. Thus, the resonant cavities should be designed to better match the GaN NDR diodes, which would increase the power and efficiency of the oscillators and improve their frequency stability. Other high-frequency circuits can also be designed to take advantage of GaN-based NDR effects. For example, using GaN NDR diodes as amplifiers can allow increased output power and frequency response compared with the conventional three-terminal device technology. Overall, microwave-capable GaN-based devices and circuits need to be fabricated and characterized as they have much to offer in the power and frequency performance as desired for high-power microwave signal switches, amplifiers, and generators.

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