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HIGH-Q INTEGRATED MICROMACHINED COMPONENTS FOR A 28 GHz FRONT-END TRANSCEIVER

by

Andrew R. Brown

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
(Electrical Engineering)
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To my family.

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CHAPTER 1

INTRODUCTION

The past two decades have shown a large growth in consumer based, wireless communication systems, including cellular phones (GSM, PCS), direct satellite communication (DBS, GPS), and high data-rate secure digital networking (WLAN). With the exception of DBS satellite television systems, the standard frequency ranges are from 900 MHz - 6 GHz allowing for low cost, portable system implementations. However, with the increase in demand for bandwidth in the wireless spectrum, there is an increased interest in the use of the higher microwave region through millimeter-wave frequencies (10-100 GHz) for consumer applications.

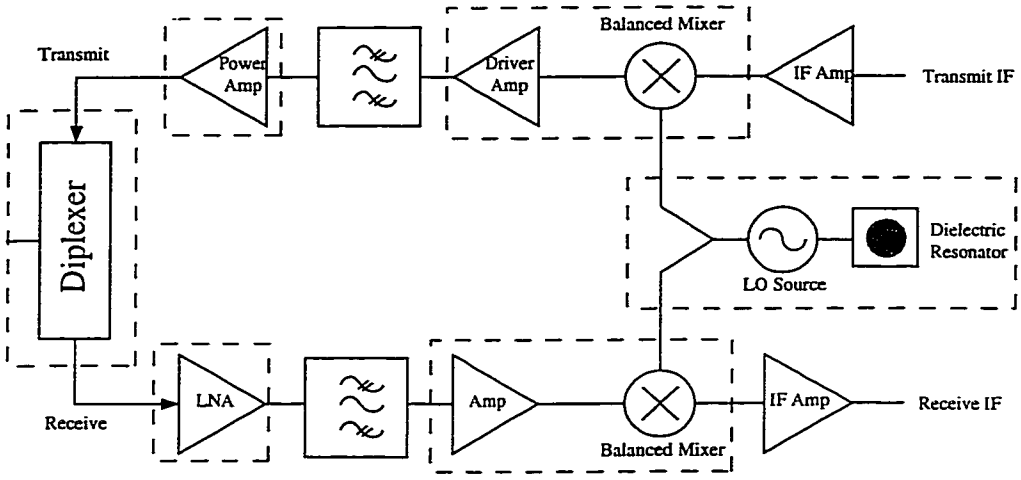
Microwave and millimeter-wave communication systems are a strong candidate for certain applications as they offer many advantages over conventional wireless links. For a given antenna aperture size, the gain of the antenna will increase with frequency allowing for a narrower beamwidth. This is important for the increased number of point-to-point communication systems that share the same bandwidth. Conversely, for a given gain, a smaller antenna could be used. This results in a smaller, more compact system which is often one of the major driving forces in portable consumer electronics. However, path loss is increased greatly with frequency ($\approx f^2$), and can be compensated with the used of high gain antennas for medium and large distance links. This makes millimeter-wave systems as very good candidates for point-to-point

and point-to-multipoint commercial systems.

Higher microwave frequency and millimeter-wave systems also allow for a wider bandwidth compared to conventional wireless links. The wider bandwidths allow for a larger number of channels and increased data rates. Commercially available systems are under development at 28 GHz for the Local Multipoint Distribution System (LMDS) [1], the PCN networks at 38 GHz [2], [3], and for a new indoor short-range telecommunication band at 60 GHz.

While military systems have used the higher end of the microwave spectrum and millimeter-wave frequencies for many years, mainstream commercial systems are fairly new at these frequencies. Some of the requirements for commercial systems include the overall system size and weight, fabrication and assembly costs, and the ability to produce large quantities quickly. Current millimeter-wave wireless front-end transceivers use a hybrid approach with a combination of waveguide components, solid state devices, and dielectric resonators (Fig. 1.1). All of the active components (LNA, power amplifier, mixer) are based on GaAs, InP, or SiGe solid state technology and are implemented using planar MMICs. The filters are typically implemented using waveguide resonators in order to obtain low insertion loss, narrow bandwidth, and high out-of-band rejection. The local oscillator is conventionally made with a dielectric resonator for good frequency stabilization. For transceiver systems, separate substrates are mounted on separate metal carriers with machined walls between them to result in a high level of isolation between transmit and receive channels. While this architecture may be acceptable for military communication and radar systems, it is not compatible with the requirements for low-cost mass production.

Another application of low-loss micromachined filters is in the phased-array antenna for the new mobile satellite communication systems. These systems consists of a satellite constellation at low earth orbits, and use L-band frequencies (1.5-2.0 GHz) for communication between the satellites and the users on the ground, and



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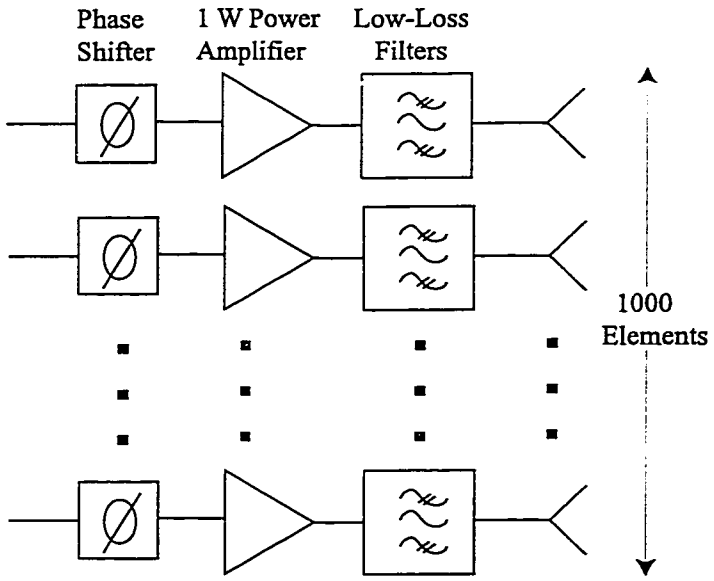


(b)

Figure 1.1: Typical millimeter-wave (a) transceiver front-end block diagram and (b) new generation K-band phased array for satellite communications.

K/Ka-band frequencies for inter-satellite data transfer. The K/Ka-band antennas are phased-arrays with multiple beam capabilities, and are composed of several hundred elements, each with a 0.5-2 W power amplifier, a low-loss filter and a high efficiency antenna. The low-loss filter is needed to filter the power amplifier harmonics since it is driven in saturation for high power added efficiency operation. It is therefore imperative to have a low-cost, low weight, small volume filter, which still results in excellent K/Ka-band performance, which is a perfect match for the micromachined filters developed in this thesis.

The objective of this thesis is to demonstrate alternative methods for designing and implementing the "non-planar" components used in microwave and millimeter-wave communication systems. Specifically, the high-Q resonator components are examined, namely full diplexers, high-rejection filters, low-phase noise oscillators, and tunable bandpass filters. A micromachining process is used to implement these structures in a planar fashion on low-cost materials. This new technique is compatible with most MMIC processing and can be mass produced to result in low-cost systems.

1.1 Millimeter-wave Filters and Diplexers

In typical full-duplex millimeter-wave communication systems, the frequency selective diplexer immediately follows the antenna at the common port and directs the signal from the power amplifier (transmit channel) to the antenna, and from the antenna to the low noise amplifier (receive channel). The key requirements for such a component are low insertion loss, high isolation, and narrow bandwidth. For the transmit side, the insertion loss needs to be minimized for power conservation. Also, the insertion loss adds directly to the noise figure of the system for the receive chain. A low-loss diplexer is therefore essential for maintaining a reasonable signal to noise ratio. Isolation also has a strong impact on overall system noise figure. The output

wideband white noise of the power amplifier is much greater than that of the LNA. If any of the power amplifier noise leaks into the LNA, the system noise figure is greatly increased. Also, the output power of the power amplifier is much higher than the received signal ($10^6 - 10^{10}$ times). Therefore, power leakage from the PA to the LNA chain may cause the LNA chain to saturate. This has the effect of decreasing the LNA gain, increasing the noise figure, generating intermodulation distortion in the LNA chain, and desensitizing the receiver. This may also lead to a feedback loop that could result in system-wide oscillation. Also, with increasing numbers of competing wireless technologies, there is a strong emphasis on increasing the number of total channels available in a given bandwidth, thereby resulting in closely-spaced channels with narrow or even no guard-band. This puts tight system constraints on the input diplexer, the LNA filtering, and the IF filtering stage.

High quality factor resonators are needed in order to have a low insertion loss, high out-of-band rejection, and high channel-to-channel isolation. The theoretical insertion loss of a filter is given by [4]:

$$\Delta L_A(dB) \approx 8.686 \frac{c_n}{\bar{\omega} Q_u} \tag{1.1}$$

where $\Delta L_A(dB)$ is the inband insertion loss, c_n is the filter prototype coefficient and is a function of the number of poles and passband ripple of the filter, $\bar{\omega}$ is the filter fractional bandwidth, and Q_u is the unloaded quality factor of the resonator. Figure 1.2 shows the impact of a the quality factor on the insertion loss of a 3% and an 8% filter. For narrow bandwidths filters (less than 3%), the impact of the quality factor on the insertion loss is very strong for quality factors less than 500. It is difficult to obtain resonators with quality factors above 100 at millimeter-wave frequencies unless they are built on low dielectric constant substrates such as quartz and teflon in a stripline configuration. Even so, this configuration is limited in the resonator quality factor to about 250-300 at 30 GHz. Therefore, the diplexer and other filters are typically implemented using high-Q structures such as resonant waveguide

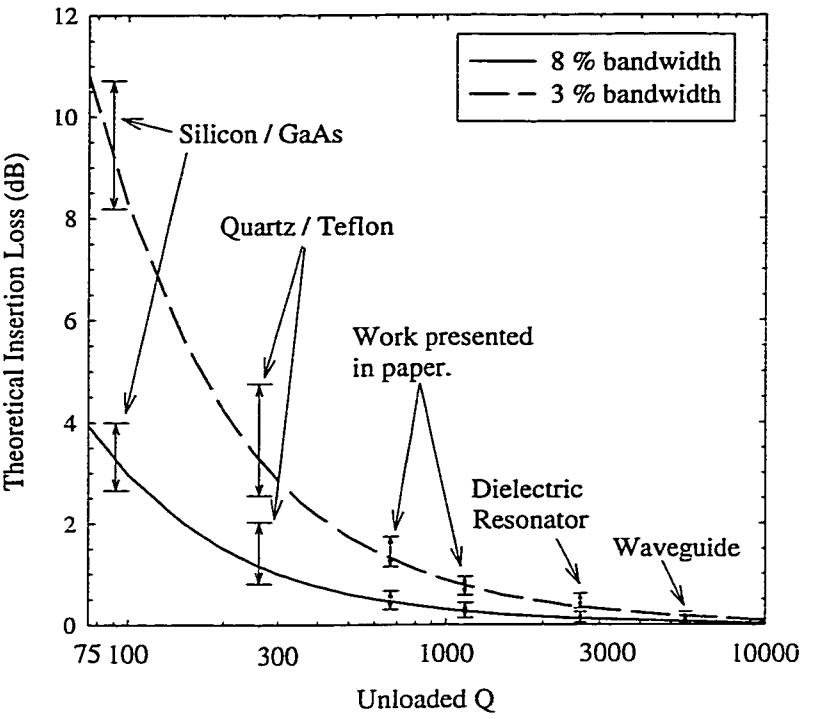


Figure 1.2: Theoretical insertion loss for 3% and 8% filters. The estimated type of resonator is based on data from 30-60 GHz.

cavity filters or dielectric resonator filters.

Waveguide filters are constructed by precise milling of a metallic block to form the resonators. The coupling between the resonators is formed by an iris in the cavity walls. Even with high precision machine tools, it is difficult to obtain high levels of accuracy for both the resonators and the irises [5], [6], [7]. Therefore, tuning screws are used to control the resonant frequencies of the cavities and to set the correct coupling through the irises. The large, metallic structure results in a heavy and bulky system. The requirement for precise machining and tuning makes this expensive to produce and difficult to fabricate in large quantities. Further, for the waveguide filter/diplexer to interface with a planar amplifier, a transition from waveguide to either coaxial or planar transmission line is necessary. Such a transition adds insertion loss and is expensive for millimeter-wave applications.

Dielectric resonator filters with high-Q resonators have advanced considerably over the last several years as dual-mode filters with compact size [8], [9], [10]. The resonators are formed by dielectric pucks suspended in the center of a below-cutoff waveguide by teflon positioning screws. The coupling between the resonators is controlled either by iris or coupling screws depending on the necessary amount of coupling. As with the waveguide filters, dielectric resonators require precise machining. Also, the coupling of the resonators is very sensitive to resonator position and iris/tuning screw dimensions. This type of filter also requires transitions to interface with planar structures. While the size is reduced compared to a waveguide cavity filter, the dielectric resonator is still a large structure and requires precise machining and tuning making it difficult to be used in mass commercial applications.

Planar filters have been investigated in the past to address these problems by using bulk micromachining techniques [11], [12], [13], [14]. These filters produced high quality filters compared with existing planar technologies and could be reproduced in large quantities with better tolerances than waveguide or dielectric resonators due to the use of photolithography. This work (Chapters 2,3, and 4) explores further optimization of the filters done in the past. In Chapter 2, the resonators are examined and optimized to result in a much higher quality factor than previously demonstrated. The micromachined planar resonators do not conform to existing transmission line models that have been used in the past. To advance filter design using these elements, a filter synthesis method is derived in Chapter 3 that allows for rapid filter synthesis while minimizing time spent on full-wave simulating. Also, the parasitic effects of the transition from CPW-on-silicon to membrane suspended microstrip are investigated and included in the filter design. Chapter 4 presents narrowband 3 and 4-pole filters which are fabricated individually, and together to form a low-loss, high-isolation, planar diplexer at 28 and 30 GHz.

1.2 Millimeter-wave Local Oscillator Sources

The error rate of a communication system and the system noise figure for low IF systems is strongly dependent on the spectral purity of the local oscillator. The local oscillator should therefore exhibit a very low-phase noise performance which is strongly dependent on the quality factor. The oscillator phase noise, using a linear approximation, is given by [15]:

$$N_{pn}(f_m) = \frac{FkT}{2P_{avs}}\left[1 + \left(\frac{1}{2Q_L}\right)^2\left(\frac{f_0}{f_m}\right)^2\right] \tag{1.2}$$

where F is the noise figure of the active circuit with the positive feedback removed, k is the Boltzman constant, T is the temperature, P_{avs} is the available signal power, Q_L is the resonator loaded Q, f_0 is the oscillation frequency, and f_m is the frequency offset from the carrier where the noise spectral power is measured. For frequencies near the carrier, the phase noise is a function of $1/Q^2$. Millimeter-wave oscillators are typically fabricated with either a waveguide cavity such as the case of Gunn or IMPATT diodes [16] or using a dielectric resonator as in the case of HEMT or HBT devices [17], [18], [19]. These resonators exhibit a Q of 1000-3000 at 30-60 GHz and result in excellent phase noise performance. As with filters and diplexers, the use of waveguide cavity resonators result in large and bulky systems. Waveguide structures also require transitions to planar structures and tuning to achieve proper coupling. Dielectric resonators are much smaller than waveguides and can be mounted next to a microstrip line to control the coupling. This eliminates the need of a waveguide transition. However, the coupling is extremely sensitive to the position of the dielectric puck. Since the mounting of the puck is essentially a mechanical process, this often requires tuning.

While oscillators with a Q of 1000-3000 do result in good phase noise performance, reasonable performance can still be achieved with a Q of 500 if there are other advantages such as the elimination of tuning and transitions. In Chapter 5, free-running

oscillator is explored using a micromachined planar resonator. Since the resonator is determined by photolithography, the length of the resonator and the coupling to the transistor are carefully controlled. The resulting oscillators do not require any manual tuning, and can be produced in large quantities. In addition, the fabrication process for the local oscillator is identical to that of the filters and diplexers and is compatible with a CPW process on high-resistivity silicon or GaAs substrates.

1.3 Filter Banks and Tunable Bandpass Filters

Switched filter banks are commonly used for multiband communication systems and frequency hopping radar systems where high isolation between the filter elements is a requirement. Also, compact size, reduced weight, and low material and fabrication costs are essential. The conventional design for a switched filter bank is to machine a series of channels in a metal carrier and to place individual filters inside these channels. Chapter 6 discusses how micromachining techniques can be applied to an X-Band filter bank.

Some communication systems use tunable frequency filters for switching frequency bands in multiband systems. At low microwave frequencies (<4 GHz), active tuned filters are sometimes used. However, active filters typically have a high noise figure. Mechanically tunable filters offer very low loss, but are large and difficult to implement in low-cost commercial systems. Filters based on ferromagnetic elements such as yttrium-iron-garnet (YIG) offer a wide tuning range, electrical tuning, and moderately low insertion loss, but require intricate assembly and tuning [4]. An electrically tunable filter is presented in Chapter 7 as an alternative to the above mentioned methods. This filter is implemented using a suspended-substrate design at 0.8-1.3 GHz, and by using micromachining techniques at 5.5-10.5 GHz. As with the other micromachined structures, this offers a planar topology using conventional

processing techniques.

CHAPTER 2

HIGH-Q MICROMACHINED RESONATORS

2.1 Introduction

Microwave and millimeter-wave resonators play an important part in modern communication systems in areas of filter design, oscillator stabilization, and low loss impedance matching circuits. A figure of merit for a resonator is the quality factor. The in-band insertion loss and out-of-band rejection of a filter and phase noise performance of an oscillator are strongly dependent on the quality factor of a resonator. In this chapter, a detailed method of measuring the quality factor of resonators is discussed including practical limitations such as resonator coupling.

As discussed in the thesis introduction, current millimeter-wave wireless front-end transceivers use a hybrid approach with a combination of waveguide components, solid state devices, and dielectric resonators. This results in large and bulky systems. This chapter discusses alternative methods for obtaining *planar* high-Q elements by using micromachining techniques to alter the geometry of a silicon substrate to allow for integration of the high-Q elements formerly done with waveguides and dielectric resonators with planar structures such as solid state devices. The chapter presents two methods: the first technique is based on thin dielectric (membrane) technology and the second technique is based on three-dimensional etching in a cavity formation of a

silicon wafer. The micromachined resonators are fully compatible with MMIC technology and most importantly, do not require low-loss millimeter-wave transitions to waveguides. Also, micromachined resonators are lithographically defined and therefore do not require exact placement and manual tuning such as in dielectric resonator designs.

2.2 The Q-factor and Equivalent Resonator Circuits

The quality factor, or Q factor, is a figure of merit for a resonator. The general definition for the Q factor is given by:

$$Q = \omega \frac{\text{energy stored in resonator}}{\text{energy dissipated}} \tag{2.1}$$

At resonance, the quality factor is:

$$Q = \omega_0 \frac{W_m + W_e}{P_{loss}} = \omega_0 \frac{2W_m}{P_{loss}} \tag{2.2}$$

where ω_0 is the resonant frequency, W_m and W_e are the average magnetic and electric energies stored in the resonant structure, and P_{loss} is the power loss. At resonance, the electric and magnetic energies are equal.

Since the behavior of microwave and millimeter-wave resonators are based on distributed effects and difficult to analyze, it is often much easier to model them with equivalent lumped element models. The basic model taken is either a series RLC structure or a parallel RLC (fig. 2.1) depending on the configuration of the structure to be analyzed. The structures presented throughout this section are all analyzed with the parallel RLC resonator.

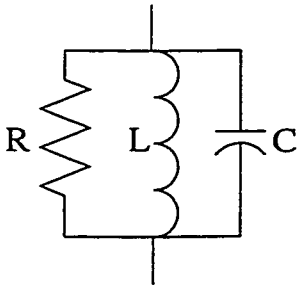


Figure 2.1: Parallel RLC resonator

2.2.1 The Unloaded Q

If the resonator is unloaded and driven by an ideal voltage source, the Q is given by:

$$Q = \frac{R}{\omega_0 L} = \omega_0 RC \tag{2.3}$$

where ω_0 is the resonance frequency and is given by:

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{2.4}$$

The Q factor of an unloaded resonator as described above is a special case and will be referred to as the unloaded Q, or Q_u, for the remainder of this thesis. This is the theoretical maximum Q and is dependent only on the physical constraints of the structure, such as by geometry, conductivity, etc. Since Q_u can only occur by not loading the resonator with any other circuitry, it is not directly of any use, but is merely a theoretical figure of merit.

The impedance seen looking into the lumped element resonator model is

$$Z_{in} = \left(\frac{1}{R} + \frac{1}{j\omega L} + j\omega C\right)^{-1} \tag{2.5}$$

By taking a Taylor expansion for Z_{in} at a frequency of $\omega_0 + \Delta\omega$ where $\Delta\omega$ is small

in comparison to ω_0, equation 2.5 can be approximated [20] by:

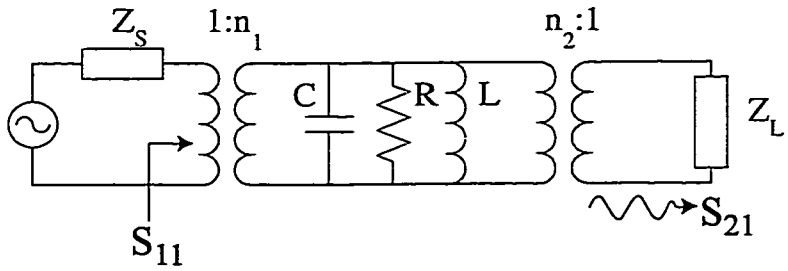
$$\begin{aligned} Z_{in} &\approx \left(\frac{1}{R} + \frac{1-\Delta\omega/\omega_0}{j\omega_0 L} + j\omega_0 C + j\Delta\omega C\right)^{-1} \\ &\approx \left(\frac{1}{R} + j\frac{\Delta\omega}{j\omega_0^2 L} + j\Delta\omega C\right)^{-1} \\ &\approx \left(\frac{1}{R} + 2j\Delta\omega C\right)^{-1} \\ &\approx \frac{R}{1+2j\Delta\omega RC} \\ &\approx \frac{R}{1+2jQ\Delta\omega/\omega_0} \end{aligned} \tag{2.6}$$

The half-power bandwidth of this structure occurs when the $|Z_{in}(\omega)|^2 = |Z_{in}(\omega_0)|^2/2$. By using expression 2.6, the half-power bandwidth is

$$\mathrm{BW} = \frac{1}{Q} \tag{2.7}$$

2.2.2 The Q factor for a loaded resonator

As discussed above, the unloaded Q is merely a figure of merit. For the resonator to be used in a system, it will have to be loaded by external circuitry. This consists of coupling power into the resonator from a power source of characteristic impedance Z_0. The coupling can be done at an arbitrary amount and for generalization, it is modeled by a transformer with a voltage coupling of n. A common configuration is a two port coupling in bandpass mode as in figure 2.2a. The source impedance is Z_S and the load impedance is Z_L. The transformers are considered ideal and have voltage couplings of n. In this configuration, the resonator acts as a filtering element by presenting a high shunt impedance and allows more power to pass through the resonator at the resonant frequency. Another configuration used is the resonator in bandstop mode (fig. 2.2b) where power is transmitted off resonance and the resonator presents a higher impedance at resonance reflecting at a narrow band.



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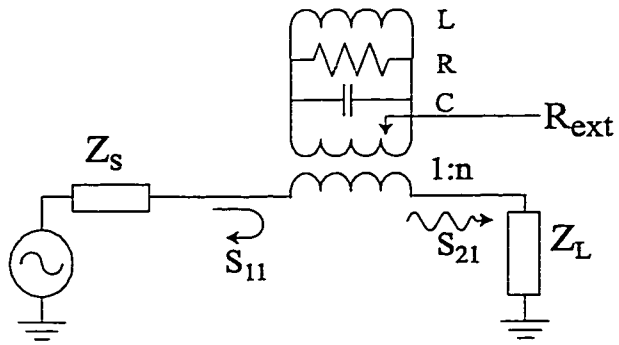


(b)

Figure 2.2: Two port loading of a parallel RLC resonator for (a) bandpass configuration and (b) bandstop configuration

The loading of the resonator degrades the quality factor and can shift the resonant frequency. It is necessary to introduce two different quality factors, namely, the external quality factor, Q_{ext}, and the loaded quality factor, Q_L. The external Q is defined as the effective Q due to the impedance of any loading only. This does not take into account the internal resistance, R, of the resonator. The loaded Q is the effective Q due to both the loading plus internal resistance of the resonator.

For the remainder of this section, Z_S and Z_L are taken to be real values. This is a good assumption if the resonator is loaded by a matched termination or transmission line. However, this is not accurate for filter applications except for the input and output resonators. This is also not an accurate assumption for applications such as oscillators, since the impedance seen looking into an unstable transistor is a negative resistance and not necessarily a purely real value. By taking the assumption of loading the resonator with a purely real load, then

$$Z_S = R_S \tag{2.8}$$

$$Z_L = R_L \tag{2.9}$$

Therefore, the effective loading resistance, R_{ext}, is the parallel combination of the transformed impedance at the ports of the resonator as

$$R_{ext} = \frac{n^2 R_L R_S}{R_L + R_S} \tag{2.10}$$

The external Q is then simply:

$$Q_{ext} = \frac{R_{ext}}{\omega_0 L} \tag{2.11}$$

The loaded Q given by the lossless resonator loaded by the parallel combination of the resonator resistance and the total external resistance, and is:

$$Q_L = \frac{R R_{ext}}{(R + R_{ext}) L \omega_0} \tag{2.12}$$

As shown in equation 2.12, if R_{ext} is very large, then Q_L approaches the value of Q_u. However, if R_{ext} is reduced to increase matching and coupling to the resonator, then

Q_L degrades quickly. The three values of Q are related by the expression

$$\frac{1}{Q_L} = \frac{1}{Q_{ext}} + \frac{1}{Q_u} \tag{2.13}$$

2.2.3 Relation of Q and Coupling to the Scattering Matrix

The unloaded Q and the resonant frequency of a resonator are constants defined by the physical structure of the unloaded resonator. However, only the loaded Q can be measured since the resonator must be loaded to be observed. The loaded Q of a resonator can be found by measuring the half-power bandwidth of the resonator under loaded conditions as discussed above. The unloaded Q and the resonator coupling must then be extracted from the measured loaded Q and the resonator impedance at resonance in order to develop lumped element models for arbitrary loading. At resonance, the inductance and capacitance cancel each other and the impedance is defined by the transformed resistance of the resonator and the loading.

Resonator in Bandpass Configuration

Based on the circuit in figure 2.2a, at the resonant frequency, ω_0, S_{21} and S_{11} are:

$$S_{21} = \sqrt{\frac{Z_S}{Z_L}} \frac{2n^2 R Z_L}{n^2 R Z_L + Z_S Z_L + n^2 R Z_S} \tag{2.14}$$

$$S_{11} = \frac{n^2 R Z_L - Z_S n^2 R - Z_S Z_L}{n^2 R Z_L + n^2 R Z_S + Z_S Z_L} \tag{2.15}$$

By solving for the $n^2 R$ term and then using the equation for Q_L, equation 2.12, the loaded Q can be solved in terms of S_{21}, S_{11}, Q_u, Z_S, and Z_L at resonance.

$$Q_L = Q_u \left(1 - \frac{S_{21}}{2} \sqrt{\frac{Z_S}{Z_L}} (1 + \frac{Z_S}{Z_L}) \right) \tag{2.16}$$

$$Q_L = \frac{Q_u}{2} \left((1 - S_{11}) - \frac{Z_S}{Z_L} (1 + S_{11}) \right) \tag{2.17}$$

For the special case where $Z_S = Z_L$, these expressions simplify to:

$$Q_L = Q_u (1 - S_{21}) \tag{2.18}$$

$$Q_L = Q_u S_{11} \tag{2.19}$$

Resonator in Bandstop Configuration

Based on the circuit in figure 2.2b, at the resonant frequency, ω_0, S_{21} and S_{11} are:

$$S_{21} = 2\sqrt{\frac{Z_S}{Z_L}}\frac{Z_L}{n^2R + Z_S + Z_L} \tag{2.20}$$

$$S_{11} = \frac{n^2R + Z_L - Z_S}{n^2R + Z_L + Z_S} \tag{2.21}$$

By solving for the n^2R term and then using the equation for Q_L, equation 2.12, the loaded Q can be solved in terms of S_{21}, S_{11}, Q_u, Z_S, and Z_L at resonance.

$$Q_L = Q_u\frac{(1 - S_{11})(Z_S + Z_L)}{2Z_S} \tag{2.22}$$

$$Q_L = Q_u\frac{S_{21}(Z_S + Z_L)}{2\sqrt{Z_S Z_L}} \tag{2.23}$$

For the special case where $Z_S = Z_L$, these expressions simplify to:

$$Q_L = Q_u(1 - S_{11}) \tag{2.24}$$

$$Q_L = Q_u S_{21} \tag{2.25}$$

2.2.4 Influence of Coupling on the Accuracy of the Extraction of Q_u

A simple method for measuring the quality factor of distributed resonators at microwave and millimeter-wave frequencies is by using a network analyzer. The loaded Q can be found from measuring the 3 dB fractional bandwidth of either the transmission of a resonator in the bandpass configuration or the bandwidth of the reflection for a resonator in bandstop configuration. From the measured loaded Q, a calibrated measurement can determine the loading of the resonator and the unloaded Q is then extracted. This is a straightforward procedure, but care must be taken for determining the resonator coupling in order to obtain an accurate value for the unloaded Q. Defining the sensitivity of a function y as a variable of x as:

$$S_x^y = \frac{x}{y}\frac{\partial y}{\partial x} \tag{2.26}$$

The sensitivity for the extraction of the unloaded quality factor from the loaded quality factor for the bandpass resonator configuration is:

$$S_{S_{21}}^{Q_u} = \frac{S_{21}}{1 - S_{21}} \tag{2.27}$$

To minimize the sensitivity, the coupling should be as weak as possible. Since the resonator under test is connected to feedlines with possible loss and mismatch and is measured with a calibration that has a non-zero amount of error with a network analyzer that has limited resolution, the sensitivity should be a strong factor when designing a resonator test structure if an accurate unloaded Q is desired. Since most network analyzer measurements are taken in a dB scale, the sensitivity in unloaded Q to S_{21} in terms of dB is:

$$S_{S_{21}(dB)}^{Q_u} = \frac{S_{21}(dB)}{20} \frac{10^{S_{21}(dB)/20} \ln 10}{1 - 10^{S_{21}(dB)/20}} \tag{2.28}$$

This is plotted in Fig. 2.3. Note that for values of S_{21} approaching 0 dB, the sensitivity greatly increases. Therefore, care must be taken in designing a weak coupling scheme if an accurate value of the unloaded Q is desired. The sensitivity for a resonator in a bandstop configuration is identical to that in the bandpass case (replace S_{21} with S_{11}).

2.3 Measurement Configuration of Distributed Resonators

The resonators presented in this chapter consist of distributed resonators in the form of suspended microstrip lines in both the bandpass and bandstop configuration. The coupling of a microstrip resonator placed in close proximity to a microstrip line is achieved primarily by fringe electric and magnetic fields and determine the strength of the coupling. For a $\lambda/2$ open circuit resonator, there is a maximum of electric field at the open ends with a minimum at the center of the resonator. Similarly, there is a magnetic field minimum at the ends and a maximum at the center of the resonator.

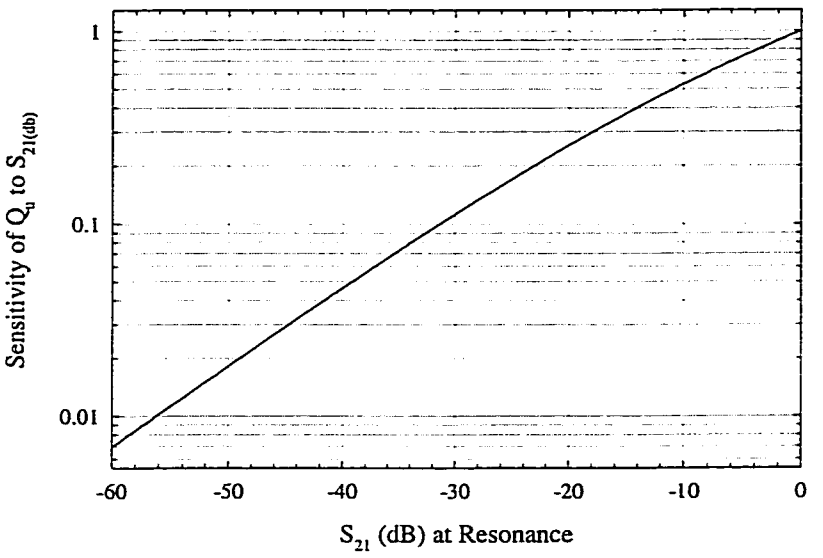
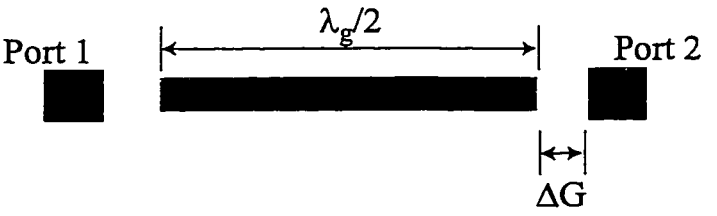


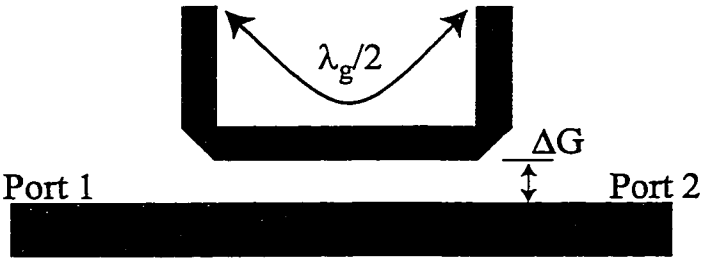
Figure 2.3: Sensitivity of the extracted unloaded Q to S_{21} (dB) at resonance.

The microstrip bandpass resonator can be measured by coupling two microstrip feedlines to the resonator at the open end by a small coupling gap (Fig. 2.4a). Since there is an electric field maximum at the ends of the resonator and a magnetic field minimum, this is a capacitive coupling. The gap acts as a capacitive transformer coupling energy into and out of the resonator. The gap distance determines the amount of coupling to the resonator setting the external Q of the structure.

The bandstop configuration can be measured by coupling a microstrip through-line to the center region of the resonator with a parallel coupled line (Fig. 2.4b). Since there is a magnetic field maximum and an electric field minimum in the center region of the resonator, this is primarily inductive coupling. The gap distance sets the coupling to the resonator (external Q) and acts as an inductive transformer.



(a)



(b)

Figure 2.4: Microstrip line coupling schemes for measuring the Q of resonators.

2.4 Membrane Supported Suspended Microstrip Resonators

2.4.1 Quality Factor of a Microstrip Line

As shown previously, the unloaded quality factor of a shunt resonator is:

$$Q_u = \omega_0 \frac{2W_{m/e}}{P_{loss}} \tag{2.29}$$

For a distributed transmission line resonator, the P_{loss} includes ohmic loss, dielectric loss, radiation loss to free space and into undesired modes. As shown in [20], the unloaded quality factor of a generalized transmission line resonator is:

$$Q = \frac{\pi}{\lambda_g \alpha} \tag{2.30}$$

where λ_g is the guided wavelength (m) of the transmission line and α is the total attenuation constant (Np/m). For a high quality factor, the guided wavelength and the attenuation coefficient should be as small as possible. However, for a smaller guided wavelength, a higher dielectric constant is needed. The higher dielectric constant leads to many design constraints to limit substrate mode loss, including thin substrates and relatively narrow transmission lines. This greatly increases the ohmic loss of the transmission line. There is a trade-off between the attenuation coefficient and the guided wavelength (and dielectric constant) in order to maximize the unloaded quality factor.

Micromachined structure have been used in the past to reduce the attenuation in a transmission line and hence, increase the unloaded quality factor. In the past, micromachining techniques have been successfully applied from K-band through submillimeter-wave frequencies [11], [14], [21]. However, the emphasis of this work is limited to the region of K-band due to the strong demand for high performance integrated applications. The method implemented is that of membrane suspended microstrip transmission lines.

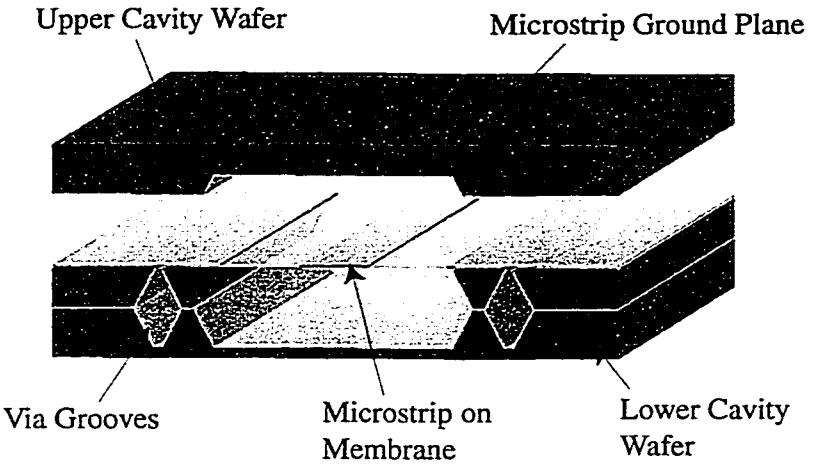


Figure 2.5: Transverse section of the microstrip structure

Membrane supported microstrip structures are formed by removing the silicon substrate and suspending a microstrip line on a thin (1.4 μm) dielectric membrane. A ground plane is formed by another micromachined substrate and attached to the top of the circuit. The bottom is also shielded with a third substrate (Fig. 2.5). For this structure, dielectric loss is eliminated with the air dielectric, the radiation loss is minimized by shielding the structure on all sides using thick via grooves to limit substrate modes, and ohmic loss is greatly reduced by allowing for very wide transverse microstrip geometries. Silicon has been used for its low cost anisotropic etching properties. Other materials can also be used such as InP and GaAs.

2.4.2 Fabrication of Membrane Suspended Microstrip Lines

The micromachined suspended microstrip transmission line is based a three wafer process (Fig. 2.5). The top wafer will be referred to as the ground plane wafer, the middle wafer as the circuit wafer, and the bottom wafer as the shielding wafer. For the circuit wafer, a stress compensated 1.4 μm membrane layer consisting of $SiO_2/Si_3N_4/SiO_2$ (7000Å/4000Å/3000Å) is deposited on a high resistivity 525 μm thick silicon substrate using thermal oxidation and low pressure chemical vapor de-

position. This process deposits the thin film on both sides of the silicon wafer allowing for a membrane on the top side of the wafer and a good etch mask for the silicon removal on the back side. The thicknesses of the SiO_2/Si_3N_4 layers are optimized to balance the net stress leaving the membrane in slight tension to result in flat and rigid membranes. After the membrane is deposited, the circuit is patterned on the top side of the wafer using either standard 2 μm gold electroplating technique or 1 μm evaporated gold and lift-off procedure depending on the operating frequency of the resonator. Other circuit components such as thin film capacitors, resistors, or air bridges can also be included at this time. Next, an opening is defined on the back side of the wafer under the resonators and areas where via holes are to be formed by etching the backside membrane with an RIE machine. The silicon is then completely etched under the circuit to the dielectric membrane which acts as an excellent etch stop. The etchant used in this work was a solution of 12.5% tetramethyl ammonium hydroxide (TMAH) and water [22]. This solution has a 1.1 μm/min etch rate for the $\langle 100 \rangle$ crystal plane with a $\langle 100 \rangle : \langle 111 \rangle$ selectivity of 25:1.

The bottom shielding wafer and the top ground plane wafer are 525 μm thick low resistivity wafers with a 1.2 μm layer of thermal oxide that acts as an etch mask. The bottom wafer is etched down 400 μm and metalized with gold to prevent radiation.

The ground plane wafer requires a two step etch from both the top and bottom side of the wafer for the formation of the ground plane plus access windows for on-wafer probing. The process flow is shown in fig. 2.6. Alignment marks are deposited on the front side of the wafer to allow for alignment from front to back sides. Photoresist is spun on the front side of the wafer and hardbaked to prevent etching of the silicon dioxide layer on the front of the wafer. Photoresist is then spun on the back side of the wafer and patterned with the probe window openings. The silicon dioxide is completely removed from the openings exposing the bare silicon. Similarly, the back side of the wafer is protected with photoresist and the front side is patterned with

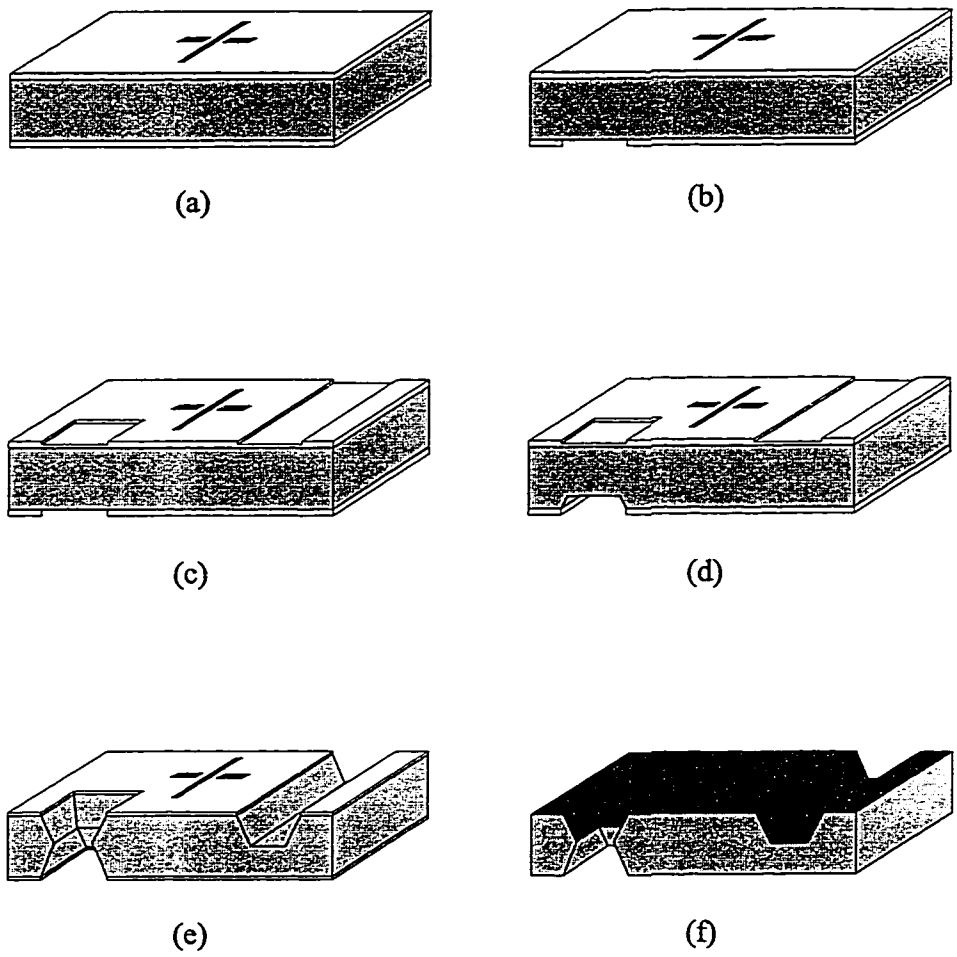


Figure 2.6: Fabrication of the ground plane wafer. (a) Alignment marks are deposited on a low-resistivity oxide wafer (oxide thickness = 1.2 μm). (b) The backside is patterned and the oxide is etched in the pattern openings. (c) The front side of the wafer is patterned and 9000 Å of oxide is etched. (d) The silicon is etched from the back of the wafer using the oxide as an etch mask. (e) 3000 Å of oxide is etched from the entire sample exposing the silicon on the front side. The sample is then etched until the ground plane is at the specified depth. (f) The oxide is stripped off of the sample and the sample is metalized.

the ground plane pattern plus the probe window openings. Only 9000 Å of silicon dioxide is etched from the pattern openings leaving 3000 Å of oxide to mask the etch. The sample is then placed in a solution of 12.5% TMAH and water to begin the etch of the probe window openings. The wafers used for the ground plane wafer are only polished on one side resulting in a rough surface on the back side of the wafer. The rough surface has a much slower etch rate due to the formation of small hillocks in the crystal plane [23]. The etch rate for the rough, unpolished surface is approximately 0.7 times the etch rate for polished surfaces. The backside of the substrate is etched to a depth given by:

$$t_{back} = t_{sub} - 1.7t_{ground} \tag{2.31}$$

where t_{back} is the etch depth of the initial etching of the probe window openings, t_{sub} is the thickness of the substrate, and t_{ground} is the total depth of the ground plane. For the case of a 525 μm wafer with a 250 μm ground plane, the initial etch depth is 100 μm. The oxide layer is then etched uniformly by 3000 Å completely exposing the silicon patterns on the front side of the sample. The oxide layer is thick enough that reducing it by 3000 Å in the unpatterned areas still acts as a good etch mask. The sample is placed back in the silicon etchant where the silicon is etched from both sides of the sample. When the ground plane has been etched to the specified depth, the sample is removed from the etchant and all of the oxide masking layer is stripped off to provide a smoother surface for bonding. The ground plane is then metalized with a 500 Å/ 2 μm layer of titanium/gold using a static deposition with a sputtering tool. The three wafers are finally assembled together under a microscope using EPO-TEK H20E conductive silver epoxy[1] to form the complete resonator.

[1]EPO-TEK H20E is a product of Epoxy Technology, Inc., Billerica, MA

2.4.3 CPW-on-Silicon to Membrane Suspended Microstrip Transitions

Membrane suspended microstrip transmission lines has the advantage of low loss as compared with conventional transmission line structures. However, there are many disadvantages:

1. The membrane lines are fragile and difficult to interface to the outside world for connections to other circuits, probe measurements, etc.

2. It is not a uniplanar transmission line structure. Shunt connections must be done using ground vias.

3. The dielectric constant is low (ϵ_{eff}=1.05). The membrane suspended microstrip lines are much longer than lines on high dielectric substrate. Also, for a given substrate geometry, the microstrip lines are very wide to yield the same characteristic impedance as lines on higher dielectric substrate.

4. The thermal properties of the membrane circuits are poor. The thermal conductivity is almost that of air whereas other transmission line structures use the substrate for heat sinking.

For these reasons, it is necessary to use the membrane suspended microstrip lines for the high Q components only and transition to the high resistivity silicon for other functions. Transitioning to silicon aids in the taking of measurements by allowing for conventional probe pads with standard pitch probes. Active devices can be mounted easily without worrying about shattering the membrane in the process of mounting the devices. Also, the active devices use the high thermal conductivity for better heat dissipation. By using CPW, a uniplanar design can be implemented. If standard thickness wafers (400-500 μm thick) are used, transmission lines on the high dielectric substrate should not be microstrip lines to avoid triggering substrate modes [24]. By

using correctly designed CPW lines [25], substrate modes are avoided and a uniplanar design can be implemented.

Transitions from silicon substrates to membrane supported transmission lines have been measured for CPW-on-silicon to microshield lines [14] and microstrip-on-silicon to microstrip-on-membrane [26]. However, design models were not performed. The abrupt discontinuity from CPW-on-silicon to microstrip-on-membrane has typically been calibrated out of most early measurements by using a TRL calibration method [27] in order to focus on the membrane circuit itself [28]. However, most of the applications in this thesis utilize both the high-Q membrane structure as well as the CPW-on-silicon for all of the non-resonator portions of the circuits including feedlines, active devices, and matching networks and an analysis of the transition is necessary. Also, if accurately modeled, the effects of the transition can be included in the circuit itself, thereby resulting in more accurate and compact designs.

The transition occurs by taking the ground plane of the CPW lines up the sides of the ground plane wafer along the etched shielding channels ("mouseholes"). The mousehole sidewalls act as ground plane via holes changing the ground from the uniplanar CPW to the microstrip ground plane. As the ground is transitioned, there is an abrupt change from the high dielectric silicon the low dielectric air cavity. This requires the CPW signal line conductor to flair out to form the wide microstrip-on-membrane line (Fig. 2.7).

A 50 Ω membrane supported microstrip through-line was designed and measured with emphasis on the transition. The calibration planes are located 750 μm from any discontinuity to ensure an accurate calibration. After the calibrated reference plane, the feedlines are grounded CPW with a gap/center/gap spacing of 65/100/65 μm. The CPW line flairs out gradually over a 350 μm long distance. The CPW gap width increases as well. The microstrip is 1025 μm wide with a ground plane height set at 250 μm for 3.9 mm and then transitions back to the silicon in the same manner.

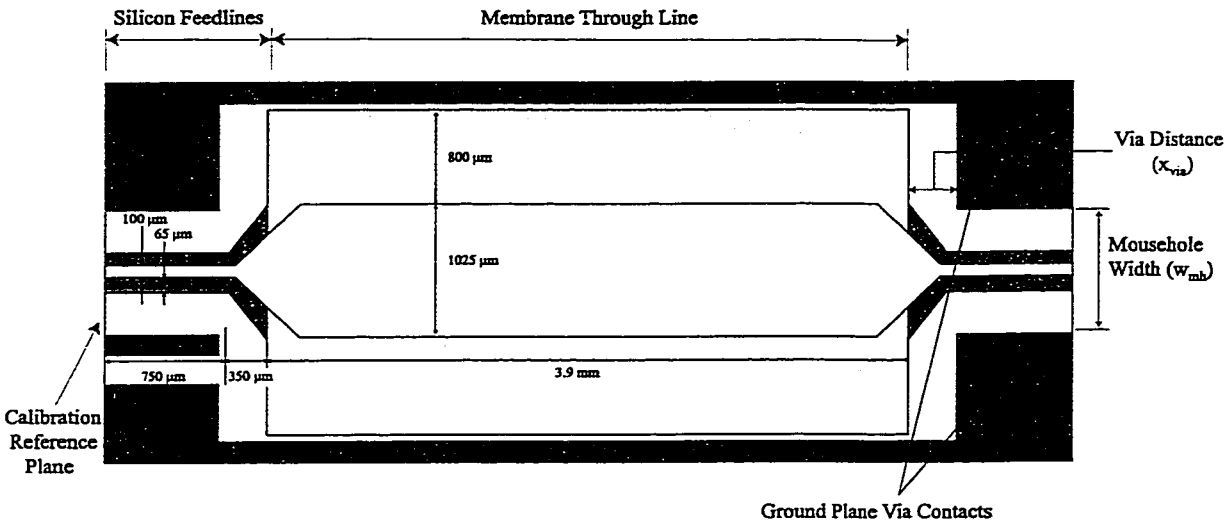
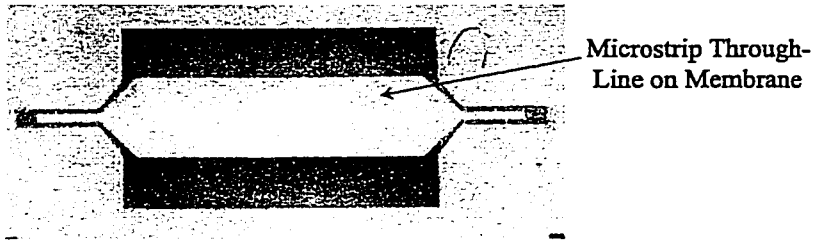


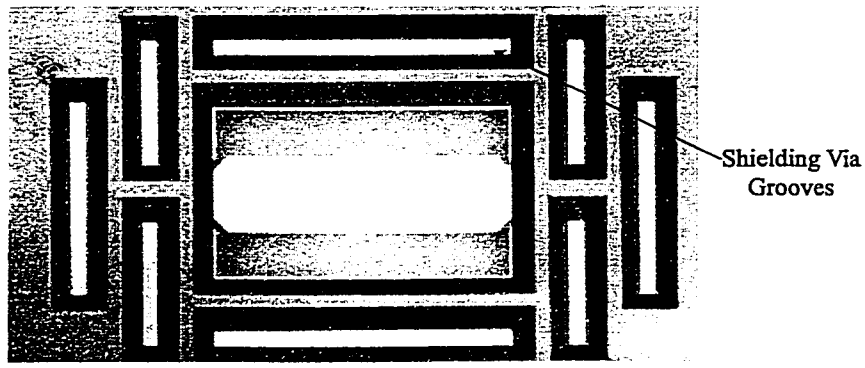
Figure 2.7: Design of the transition test line.

The membrane width continues for 800 μm past the edge of the microstrip line edge (Fig. 2.7). There are also via grooves completely surrounding the membrane area beginning at 200 μm from the membrane etch edge (Fig. 2.8b).

The top ground plane wafer was designed so that the via walls at the sides of the mouseholes and beginning of the membrane area are square as shown in Fig. 2.7. The designed values for the via distance, x_{via}, and the mousehole width, w_{mh}, are 200 μm and 500 μm, respectively. However, these are convex corners and expose a set of crystal planes that are etched rapidly by the anisotropic etchant used (TMAH) [29]. The planes that are exposed include the $\langle 110 \rangle$, $\langle 210 \rangle$, $\langle 211 \rangle$, $\langle 310 \rangle$, $\langle 311 \rangle$, and $\langle 320 \rangle$ crystal planes. According to [30], these crystal planes have etch rate in excess of 2 times that of the $\langle 100 \rangle$ crystal plane. There are several methods of corner compensation that involve leaving sacrificial amounts of silicon around the convex corner [31]. However, these methods require an area of at least 3 times the etch depth for the sacrificial silicon. In order to get the via distance as close as possible to the CPW line, there was not room for the etch compensation. As a result, the vias are located much further than the designed distance. The actual fabricated dimensions



(a)



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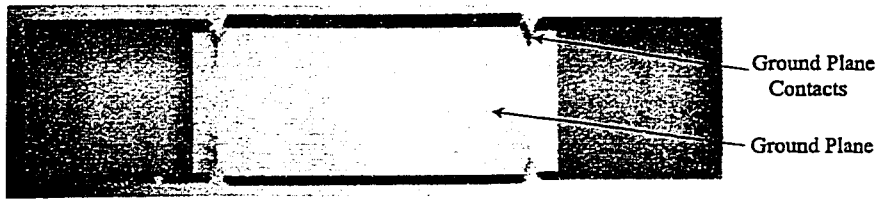

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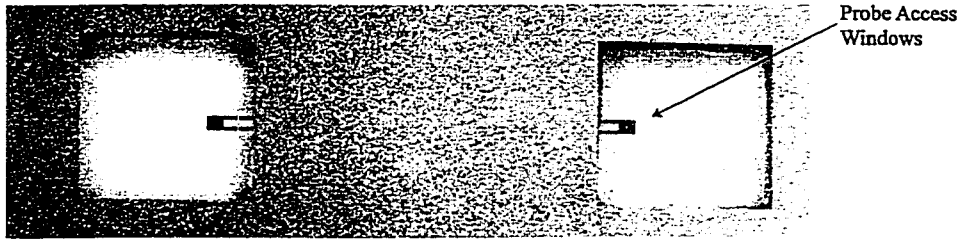


(d)

Figure 2.8: Fabricated membrane suspended microstrip through line (a) top view of circuit wafer, (b) bottom view of circuit wafer, (c) bottom view of ground plane wafer, and (d) packaged structure.

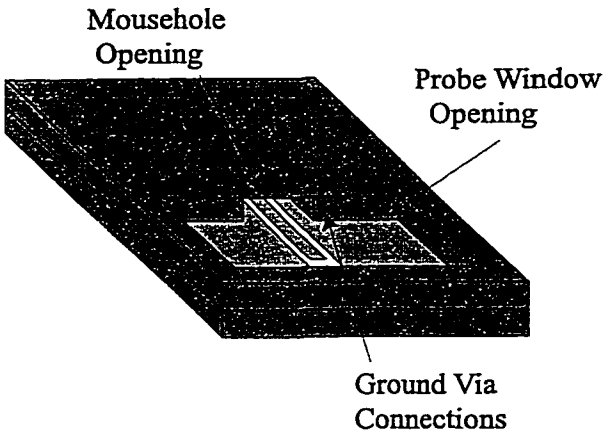
of x_{via} and w_{mh} are 600 μm and 1500 μm, respectively.

The through line test structure was fabricated with a 250 μm ground plane height and 2 μm thick electroplated gold conductors. The through line was measured using an HP8510C network analyzer calibrated using a TRL calibration method [27], [32] with 150 μm pitch coplanar Picoprobes[2]. On all measurements, the system was calibrated with a reference plane located 750 μm from the point where the CPW line begins to flair out for the transition. The measured results show a standing wave pattern with a null at 29 GHz. The maximum return loss is less than -10 dB before the null and then rises to -7 dB for frequencies above 30 GHz.

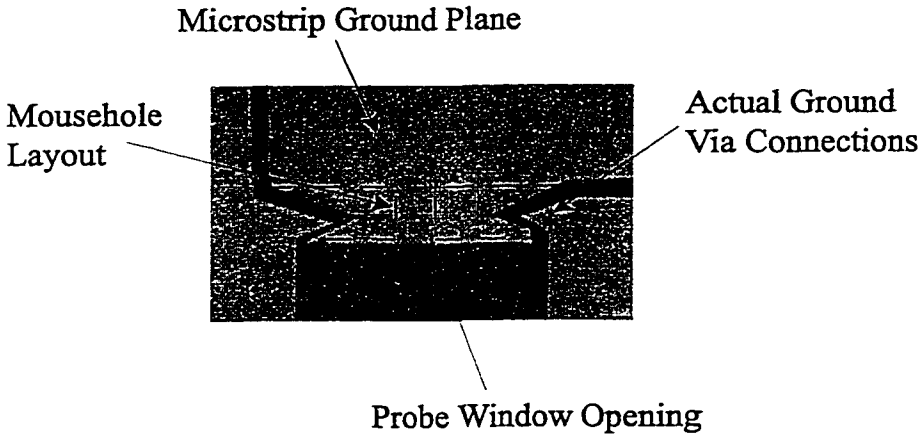
The transition with a through line was then simulated using the finite element method (FEM) full-wave analysis tool HP HFSS [33]. The full-wave analysis assumes perfectly conducting metallic surfaces and a perfect dielectric for the silicon substrate. The sloped crystal plane etch walls are assumed to be vertical. Using a values of x_{via} and w_{mh} that were actually fabricated (600 μm and 1500 μm, respectively), there is a very close agreement in S_{11} to the measured results (Fig. 2.10). However, since the full-wave analysis does not model the dielectric or ohmic loss of the 1.5 mm of CPW feedline, there is a substantial difference in the measured and simulated results for S_{21}.

By changing the values of x_{via} and w_{mh} in the FEM simulation, the standing wave pattern changes. Several values of x_{via} and w_{mh} were modeled ranging from 400-600 μm and 600-1600 μm, respectively, to study the their effects. The parameters were then fitted to a circuit model consisting of 750 μm of 50 Ω CPW feedlines, a 350 μm long section of 34 Ω line followed by a series inductor which is a function of x_{via} and w_{mh}, and the 50 Ω microstrip line on the membrane, followed by an identical structure for the transition at the output (Fig. 2.11). The 350 μm long section of 34 Ω represents the average impedance of the section of CPW line where the width of

[2]Picoprobe is a product of GGB Industries, Inc., Naples, FL.



(a)



(b)

Figure 2.9: Mousehole feed structure (a) isometric view of mousehole with probe access window, and (b) fabricated mousehole structure in top ground plane wafer (bottom view). The dotted line indicates the designed mousehole dimension (layout). Note the large amount of undercut for the convex corner increasing the width of the mousehole (increases distance of via walls from transition.

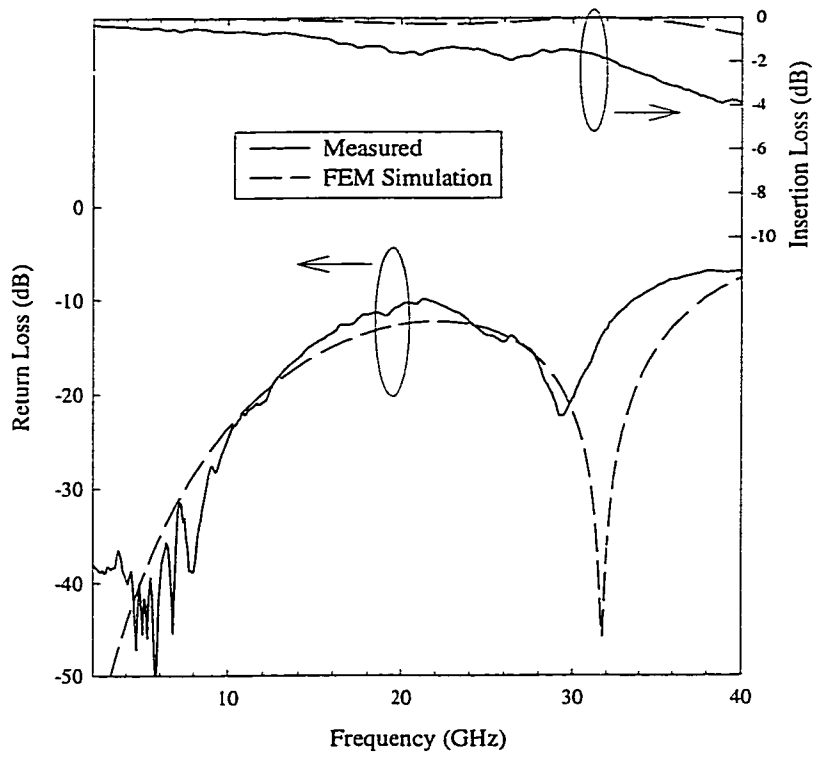


Figure 2.10: Comparison of measured S parameters to FEM modeling of transition and through line. FEM does not include any dielectric or ohmic loss.

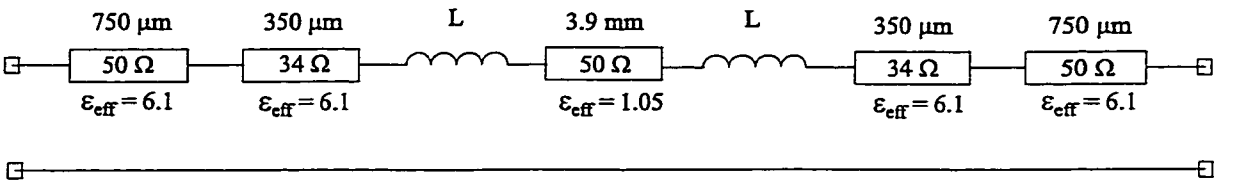


Figure 2.11: Circuit model for transition and through line structure.

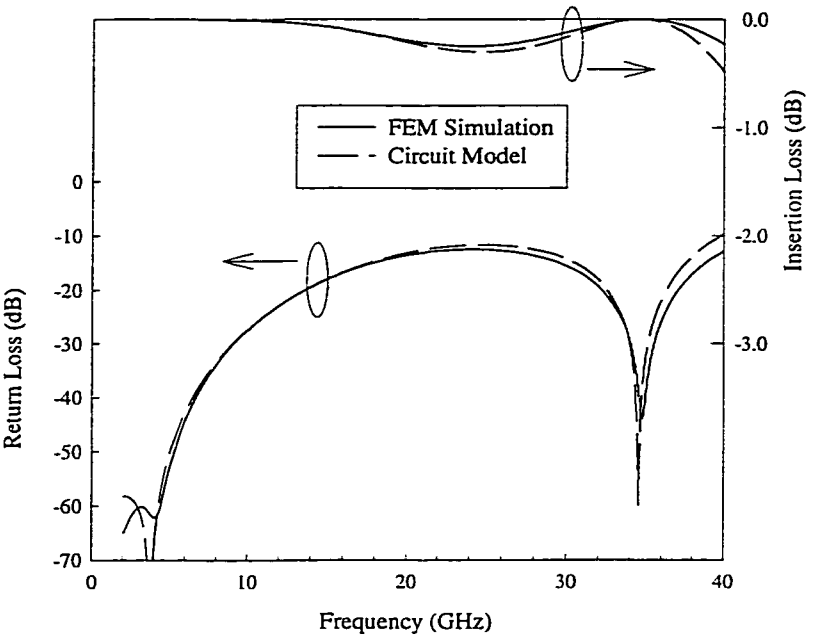
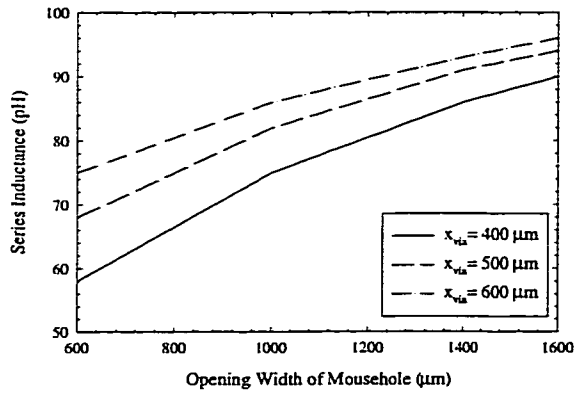
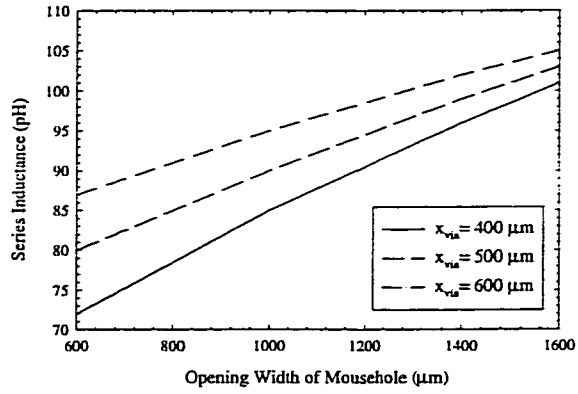


Figure 2.12: Comparison FEM analysis of a transition and the circuit model for $x_{via} = 400$ μm and $w_{mh} = 600$ μm.

the center conductor flairs out to match the 50 Ω microstrip line. Using this model, a good agreement is achieved with the FEM simulation by only changing the value of the inductance for the range of vias conditions simulated (Fig. 2.12). The series inductance is on the order of 60-90 pH for the range simulated (Fig. 2.13b). Note that the inductance increases with both x_{via} and w_{mh} which implies that the inductance is due to the added path length for the ground vias. Different ground plane heights (200 and 300 μm) were also investigated using HFSS to see the effect on the inductance (Fig. 2.13a and b). As expected, the inductance is less for the 200 μm ground plane height and more for the 300 μm ground plane.



(a)



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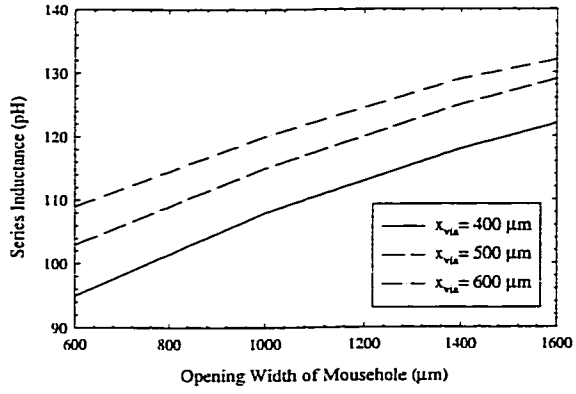


(c)

Figure 2.13: Simulated series inductance at the CPW-on-silicon to membrane suspended microstrip transition for (a) 200 μm, (b) 250 μm, and (c) 300 μm ground plane heights

2.4.4 Resonator Simulation and Measurement

Several resonators were constructed using both the bandpass and the bandstop configurations. In all cases, the resonators are $\lambda_0/2$ microstrip lines that are weakly coupled by capacitive coupling gaps or magnetically coupled by parallel coupled lines.

A single resonator was fabricated at 29 GHz in a bandstop configuration (Fig. 2.14). The ground plane height is 250 μm with an 800 μm wide conductor. The metal thickness of the conductor is 2 μm of electroplated gold (4 skin depths at 29 GHz). The shielding cavity is 800 μm away from the resonator. In order to conserve membrane space, the resonator was bent in a U shape using optimal miters. The length of the resonator was adjusted for the correct resonant frequency to 29.0 GHz by using a $2\frac{1}{2}$D moment method package IE3D [34]. The measured resonance was at 28.7 GHz showing a 1% shift in the resonant frequency. This is due to the fringing capacitance to the sidewalls of the cavity that was not modeled with the full wave analysis technique.

The microstrip through line used for is 1025 μm wide resulting in an impedance of 50 Ω over a 250 μm ground plane. As shown in the previous section, the via inductance from the transition causes a standing wave pattern. For the bandstop resonator, a good impedance match is necessary around resonance. For this reason, the resonator was made to correspond with the null of the standing wave pattern of the through line. The bandstop resonator was measured using an HP8510C network analyzer calibrated using a TRL calibration method [27], [32] with 150 μm pitch coplanar Picoprobes[3]. On all measurements, the system was calibrated with a reference plane located 500 μm from the point where the CPW line begins to flair out for the transition. Figure 2.15 shows the measured S_{11} of the through line alone as well as the through line with the resonator present. As shown, the microstrip line length is chosen to result in a good match at 27-32 GHz with the effects of the transition discontinuity. The measured loaded Q was 190 with a coupling -4.6 dB giving an extracted unloaded Q of 460 at

[3]Picoprobe is a product of GGB Industries, Inc., Naples, FL.

28.7 GHz.

Three different resonators were fabricated in bandpass configurations at 37 and 60 GHz. For the weakly coupled bandpass configuration, the effects of the transition are not nearly as important as with the broadband match of the through line in the bandstop configuration. At 37 GHz, the resonator has a ground plane height of 200 μm and a line width and thickness of 700 μm and 2 μm, respectively. The extracted unloaded Q based on measurements is 412 at 37 GHz. Two different resonators were also fabricated at 60 GHz. Both resonators have a ground plane height of 250 μm with widths of 500 and 700 μm. The resonator thickness is 1 μm of evaporated gold (3 skin depths at 60 GHz). The 500 μm wide resonators had an extracted unloaded Q of 454 and the 700 μm wide resonators had an extracted unloaded Q of 503.

The four structures described above were simulated using method of moments based HP-Momentum [35], a finite element tool developed at the University of Limoges [36], an empirical model from Linecalc [37], and a code based on the surface impedance ribbon method [38] called Simian [39]. For the simulations, the conductivity of the gold lines was assumed to be $3.9 \times 10^7\ \Omega^{-1}m^{-1}$. For the moment method, FEM, and Linecalc empirical analysis method, the attenuation constant of the line was found at the design frequency. The frequency dependent attenuation constant was then converted into the unloaded quality factor by equation 2.30.

The surface impedance ribbon method calculates the frequency dependent resistance and inductance matrix per unit length of an arbitrary metallic cross section. This method does not support the use of dielectric layers. Since this is in air dielectric, this is not an issue. The ribbon method is very accurate for modeling conductor loss since it solves for the true current on the conductors and does not make skin depth approximations for the sheet resistance of the metal structures. The resistance and inductance matrices obtained are converted to transmission line resistance and

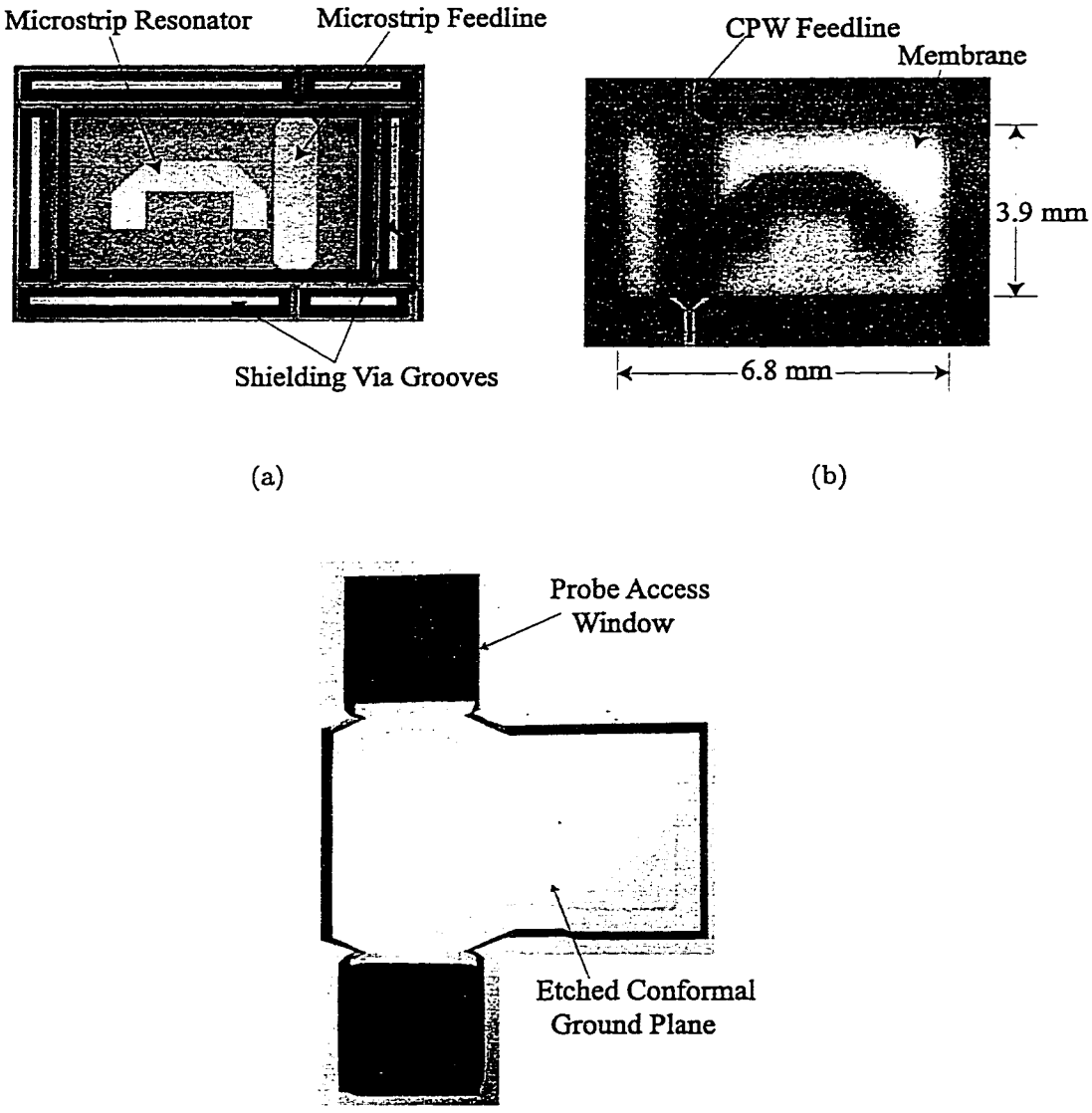


Figure 2.14: Circuit wafer of a 29 GHz microstrip resonator in bandstop configuration (a) bottom view, (b) top view, (c) and bottom view of the ground plane wafer.

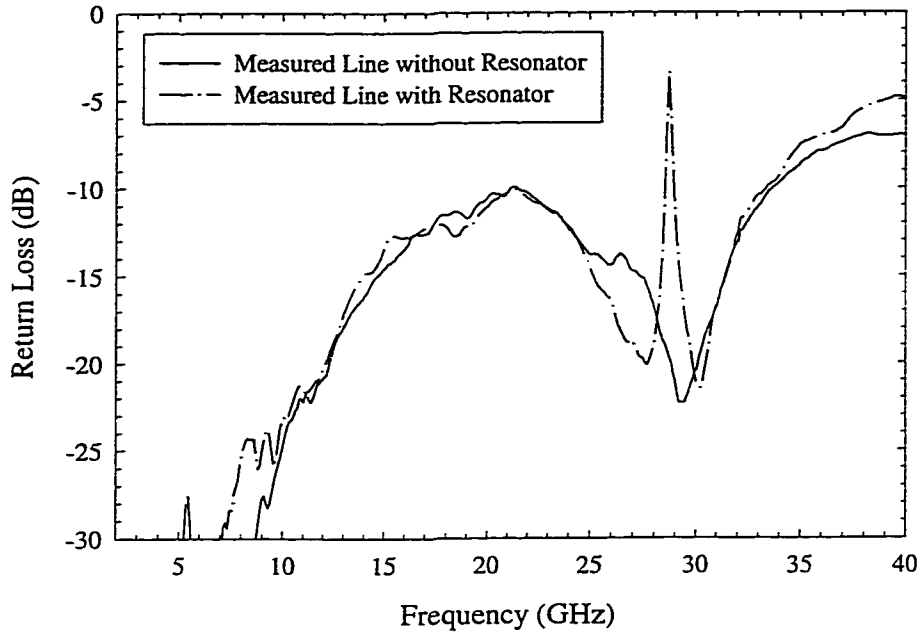


Figure 2.15: Measured S_{11} of bandstop resonator including effects of transition.

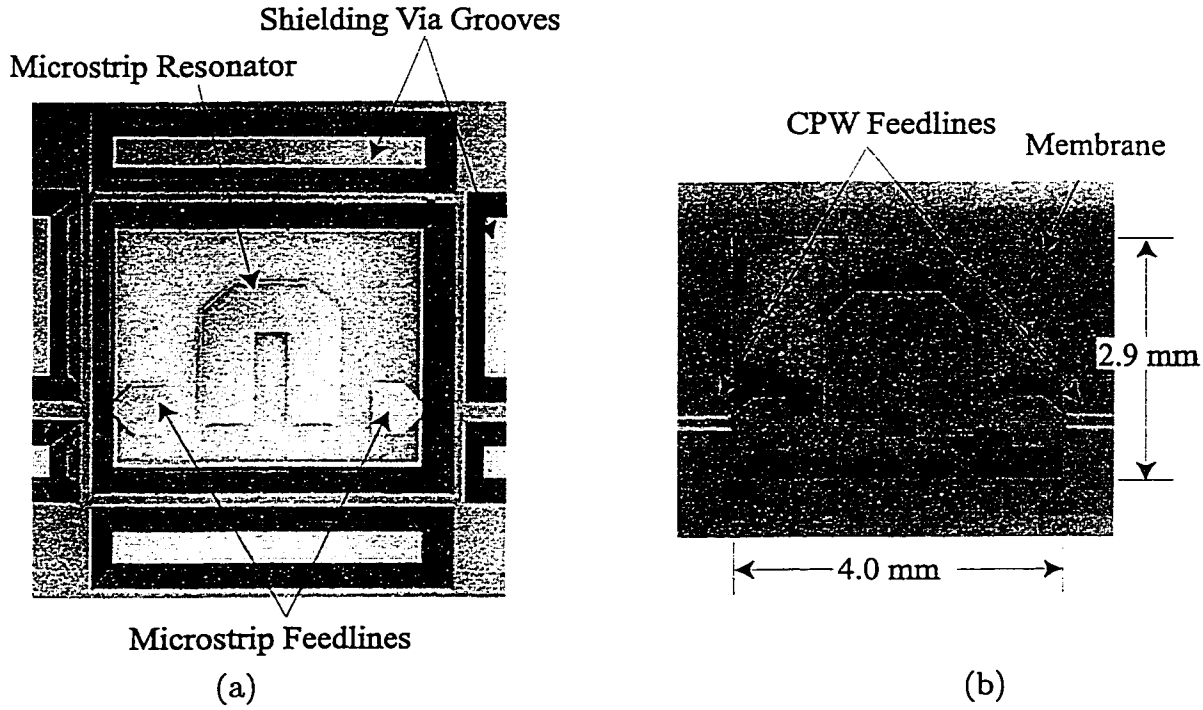
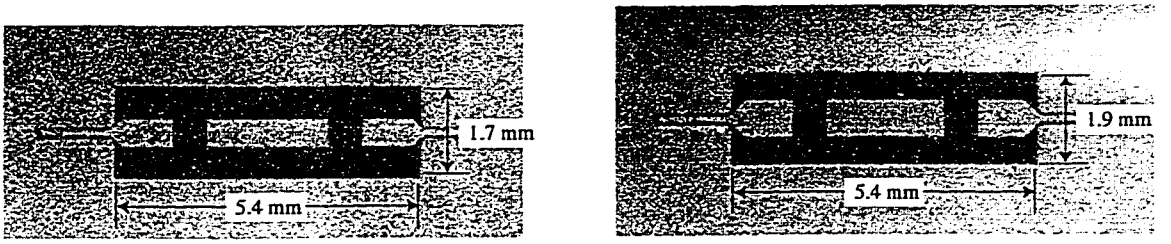
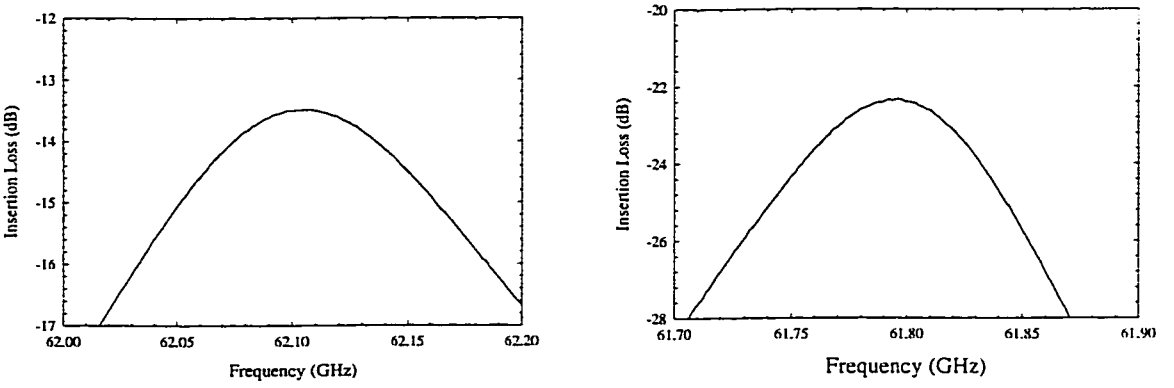


Figure 2.16: Bandpass configuration of 37 GHz micromachined microstrip resonator (a) bottom view and (b) top view.



(a) (b)

Figure 2.17: Fabricated 60 GHz (a) 500 μm wide microstrip resonator and (b) 700 μm wide microstrip resonator.



(a) (b)

Figure 2.18: Measured response for 60 GHz (a) 500 μm wide microstrip resonator and (b) 700 μm wide microstrip resonator.

inductance per unit length. For the two conductor case, this is simply:

$$R_{T-line} = R_{11} + R_{22} - 2R_{21} \tag{2.32}$$

$$L_{T-line} = L_{11} + L_{22} - 2L_{21} \tag{2.33}$$

where R_{11}, R_{22}, L_{11} and L_{22} are the self resistance and inductance per unit length for each conductor (microstrip and ground plane) and R_{21} and L_{21} are the mutual resistance and inductance per unit length. The transmission line attenuation and propagation coefficients are related to the lumped element equivalent model of a transmission line as a function of series resistance and inductance, and shunt capacitance and conductance, per unit length by:

$$\alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{2.34}$$

Setting the dielectric loss to zero (ideal dielectric) and assuming a low loss transmission line where $\beta = \omega\sqrt{LC}$, the attenuation coefficient is:

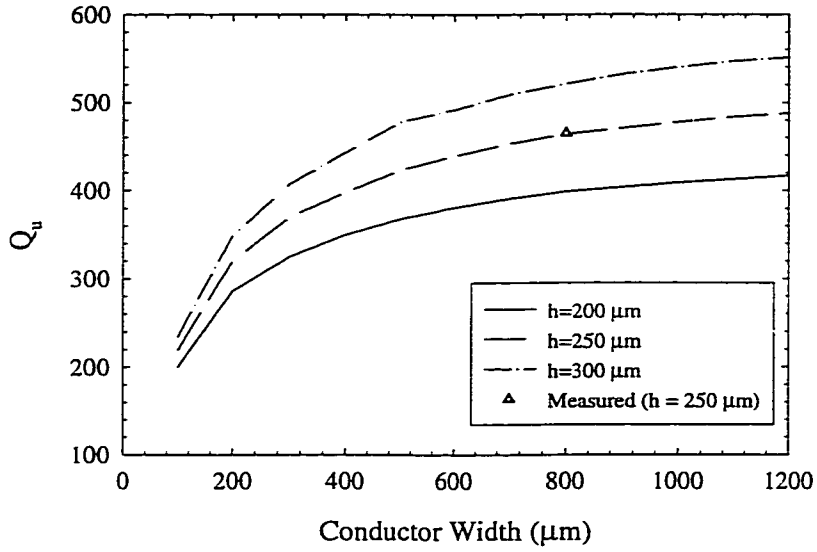
$$\alpha = \frac{RC}{2\sqrt{LC}} \tag{2.35}$$

The unloaded quality factor as a function of the transmission line impedances per unit length can then be found by:

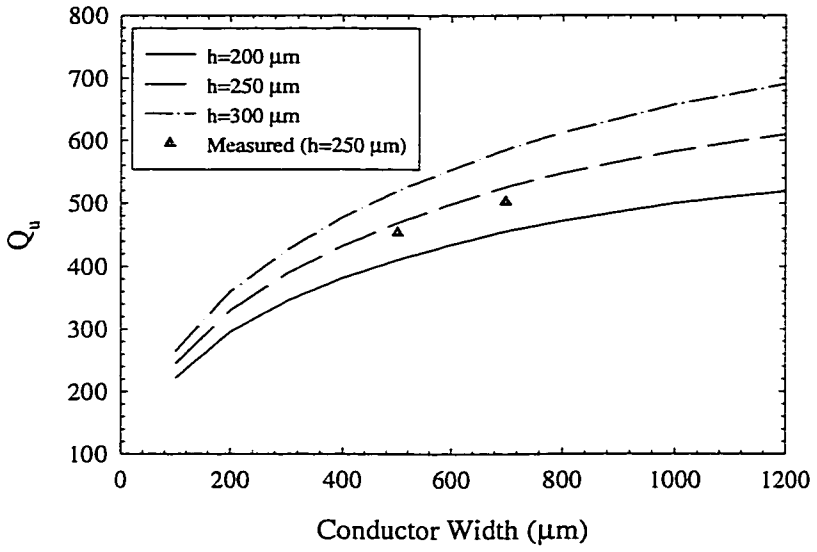
$$Q = \frac{\pi}{\lambda_g \alpha} = \frac{\beta}{2\alpha} = \frac{\omega L}{R} \tag{2.36}$$

where L and R are the transmission line impedances per unit length. Note that as long as a transmission line is resonant, and the transmission line parameters per unit length model all losses, the value of the unloaded Q for an arbitrary transmission line resonator is equivalent to the lumped element model, and the resistance and inductance matrices from the surface ribbon method can be easily converted in unloaded quality factors.

The results for the simulations and measurements are summarized in Table I. The values based on Linecalc, MoM, and FEM all overestimate the value for the unloaded



(a)



(b)

Figure 2.19: Simulated (Simian) microstrip resonator Q as a function of height and strip width at (a) 30 GHz with 2 μm thick lines and (b) 60 GHz 1 μm thick lines.

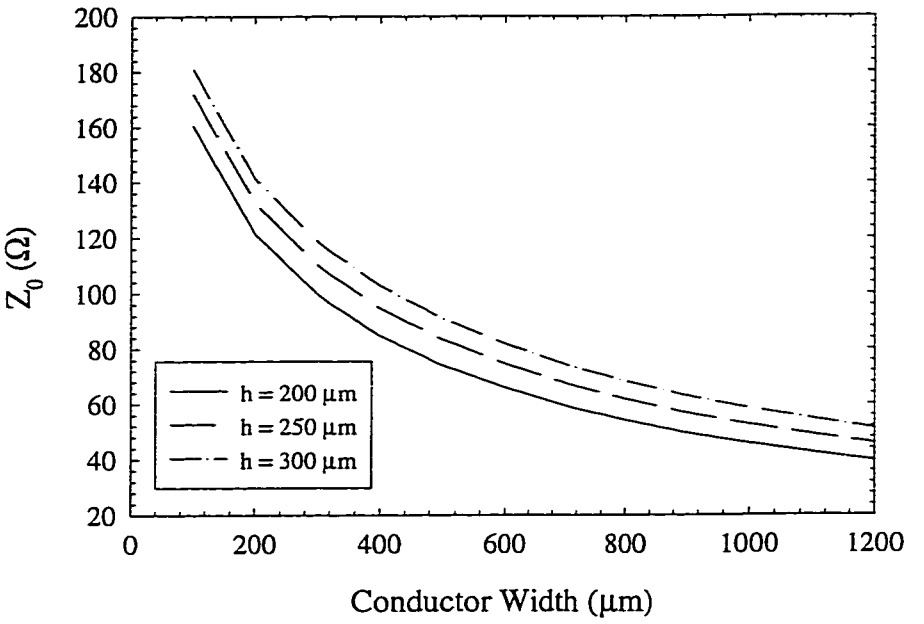


Figure 2.20: Simulated impedance value for suspended microstrip resonator as a function of height and strip width.

Q considerably. However, Simian models the loss very accurately and is within 5% of the measured values.

Table 2.1: Comparison between Measured and Simulated values of Unloaded Q.

Q_u	w=800 μm h=250 μm fo=29 GHz	w=700 μm h=200 μm fo=37 GHz	w=700 μm h=250 μm fo=62 GHz	w=500 μm h=250 μm fo=62 GHz
linecalc [37]	528	474	665	606
FEM [36]		442	661	610
MoM [35]	550	470	613	536
Simian [39]	450	403	525	474
Measured	460	412	503	454
α (dB/cm)	0.057	0.082	0.112	0.119

Design curves for the Q factor were generated using Simian (Fig. 2.19) for both the 30 GHz (t=2 μm gold) and 60 GHz (t=1 μm gold) resonators. For the 60 GHz calculations, increasing the metal thickness to 2 μm will result in a 2-3% improvement in Q. The value of the resonator Q is very sensitive to the ground plane height.

However, with increasing height (h> 250 μm), the CPW-to-membrane transition becomes more difficult with added transition inductance from the CPW ground to the microstrip ground plane. Also, increasing the width of the lines past 800-900 μm resulting in very wide transmission lines and makes circuit modeling and design more difficult. Therefore, practical considerations will limit the Q of such resonators to 450-550 for most K and V-band applications.

2.4.5 Effects of Thermal Expansion on the Resonant Frequency

Changes in temperature have the effect of thermal expansion and contraction of the metallic transmission line, the membrane, and the silicon substrate resulting in a change in resonant frequency. Since the membrane is large, relatively elastic, and has low net stress, small changes in the geometry of the silicon carrier has little effect on the geometry of the microstrip line. The temperature coefficient of linear expansion, α, is defined as:

$$\alpha = \frac{\Delta l}{l_0 T} \tag{2.37}$$

where l_0 is the length of the structure at 0° C, Δl is the change in length, and T is the temperature in Celsius. The temperature coefficients for linear expansion for gold, silicon dioxide, and silicon nitride are [40]:

$$\alpha_{Au} = 14.2 \times 10^{-6} C^{-1} \tag{2.38}$$

$$\alpha_{SiO_2} = 0.5 \times 10^{-6} C^{-1} \tag{2.39}$$

$$\alpha_{Si_3N_4} = 4.0 \times 10^{-6} C^{-1} \tag{2.40}$$

The coefficient of expansion for gold is much greater than that of the silicon dioxide and the silicon nitride and will dominate the expansion of the microstrip line length. The resonant frequency is directly proportional to the physical length of the transmission line. Due to the layered structure, this is a complicated problem to solve;

however, as a worst case, the percent change in resonant frequency as a function of temperature of the microstrip line due to the thermal expansion of gold alone is given by:

$$f_0' = \frac{f_0}{1 + (14.2 \times 10^{-6} C^{-1})T} \tag{2.41}$$

were f_0' is the resonant frequency including temperature fluctuations. The fractional temperature coefficient is then given by:

$$TC_F = \frac{1}{f_0'} \frac{\partial f_0'}{\partial T} = \frac{-14.2 \times 10^{-6}}{1 + 14.2 \times 10^{-6} T} \tag{2.42}$$

This results in a worst-case fractional temperature coefficient for the resonant frequency of -14.2 ppm/° C. Temperature compensated dielectric resonators are of the order of -6 ppm/° C and since the above result is a worst-case calculation, one can safely say that the micromachined resonators offer a similar thermal performance as state-of-the-art dielectric resonators at 30 GHz.

2.4.6 Comparison of Microstrip Transmission Lines on Higher Dielectric Substrates

While the membrane suspended microstrip lines do have very low attenuation coefficients, they also have a very large wavelength. The microstrip transmission lines are compared for a given characteristic impedance on different substrates at 29 GHz with a 2 μm metal thickness. The impedance chosen is 62 Ω to correspond to the 800 μm line on a 250 μm air dielectric substrate as presented above. To allow for a fair comparison with other microstrip lines, the thickness of the dielectric is set to $\lambda_d/20$ for all the cases except the membrane suspended microstrip[4] to limit the formation of substrate modes. This analysis is done using Simian [39] to model the frequency dependence resistance and inductance. The capacitance per unit length of

[4]The membrane suspended microstrip is actually $\lambda/40$. However, the limiting factor of the membrane suspended microstrip is the series inductance of the transition and not the formation of substrate modes.

the microstrip line is found by an analytical formula [20]:

$$C = \frac{1}{\sum_{\substack{n=1 \\ \text{odd}}}^{\infty} \frac{4a \sin(n\pi W/(2a)) \sinh(n\pi d/a)}{(n\pi)^2 W \epsilon_0 [\sinh(n\pi d/a) + \epsilon_r \cosh(n\pi d/a)]}} \tag{2.43}$$

where a is the lateral extent of the substrate (taken as 10 cm), W is the width of the line, d is the substrate height, and ϵ_r is the relative permittivity of the substrate. The simulations assume that there is no substrate loss. To prevent radiation, a shielding cover is added to each structure 800 μm from the top of the substrate. The total attenuation coefficient is found from

$$\alpha = Re\{\sqrt{(R + j\omega L)(j\omega C)}\} \quad \text{Np/m} \tag{2.44}$$

Table 2.2 shows the unloaded quality factors for several commonly used substrates. This table includes the dielectric thickness, d (set to $\lambda_d/20$ for all cases except the air dielectric), the conductor width, w (set to the required width for a 62 Ω microstrip line impedance), the simulated frequency dependent transmission line series resistance and inductance per unit length, and the simulated unloaded quality factor. The air dielectric (membrane supported microstrip line) has the highest unloaded quality factor and the higher dielectrics have a decreasing quality factor with increasing dielectric constant. For a substrate with a fixed electrical thickness ($\lambda_d/20$), and a fixed characteristic impedance, the width of the microstrip line decreases considerably with increasing dielectric constant. This causes an increase in attenuation due to ohmic loss that is greater than the decrease in guided wavelength as a function of dielectric constant, resulting in a decreasing quality factor.

2.5 Integrated Micromachined Cavity Resonators

The quality factor of the suspended microstrip line shows a large improvement over conventional microstrip lines, but in many cases, an unloaded quality factor of

Table 2.2: Comparison of Simulated Unloaded Quality Factors for Different Substrates at 29 GHz. All lines are 62 Ω lines with a 2 μm metal thickness. Dielectric loss is neglected. Dielectric thickness is $\lambda_d/20$ except for the case of air dielectric ($\lambda/40$)

Substrate	ϵ_r	d (μm)	w (μm)	R (Ω/cm)	L (μH/cm)	Q_u
Air	1	250	800	0.92	2.28	450
Quartz	4	260	350	1.97	3.88	380
Alumina	9.5	170	100	6.00	6.02	185
GaAs	13	140	56	10.05	7.22	143

500 is still not enough. One way to increase the resonator Q is to integrate miniature 3-dimensional cavities in the silicon substrate.

The integrated micromachined waveguide resonator was first demonstrated at 10 GHz for the case of very strong transmission coupling using a two wafer process with a slot-aperture coupling [41]. The slot was excited by a microstrip line above it. This method requires two wafers: one for the microstrip to slot transition, and the second for the actual cavity (Fig. 2.21a). However, the Q of the resonator is strongly related to the thickness of the cavity, which, in this case, is limited to a standard thickness wafer. Also, at millimeter-wave frequencies, the microstrip line must be integrated on a thin substrate (250 μm at 30 GHz, 150 μm at 60 GHz, etc.) with the expected additional circuit losses.

A new approach is presented for feeding the cavity that increases the quality factor and simplifies the fabrication. The cavity is constructed from two standard thickness (525 μm) silicon wafers etched 450 μm down. A CPW line is defined on the bottom wafer to the edge of the cavity, and a wire bond is placed from the end of the CPW line to the base of the cavity. This acts as an electric loop triggering the dominant TE_{011} mode at resonance. The amount of coupling is controlled by the length of the wire bond and the number of bonds placed. The top cavity is identical to the bottom cavity except a groove (mousehole) is etched above the CPW line on

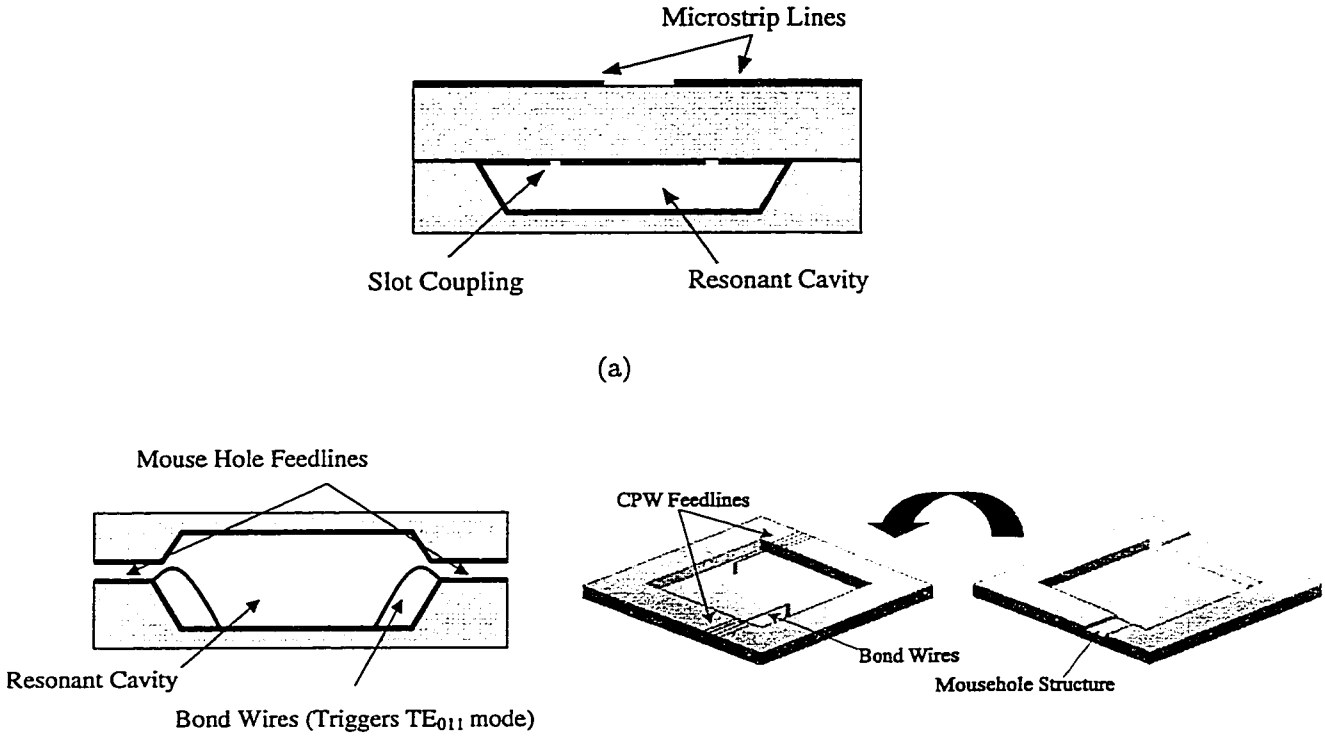


Figure 2.21: Side view of micromachined cavity resonator (a) method used by Papapolymerou, et al. and (b) method used in this work.

the bottom cavity. The groove is to prevent shorting the CPW line when the two wafers are bonded together (Fig. 2.21b). The two wafers are bonded together with conductive epoxy. For minimal cavity disturbance, the feedlines and wire bonds are placed where the current on the side walls of the cavity are at a minimum. For the case of a rectangular cavity, the corners have a current null. Using this method, the maximum operating frequency is set by the dimensions of the CPW feedlines and not the substrate thickness, and the Q is increased by increasing the cavity height by a factor of two using standard thickness substrates.

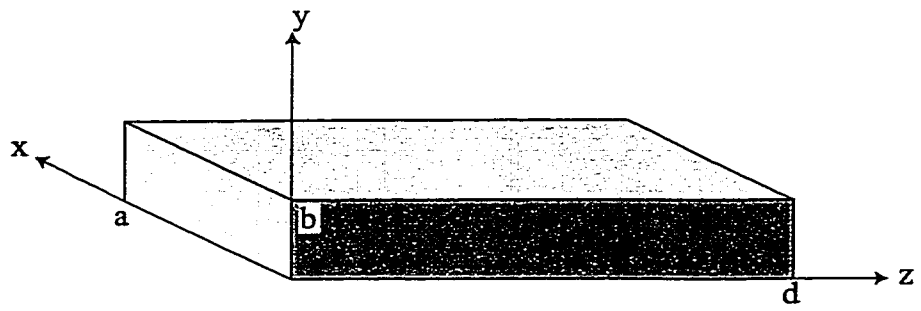


Figure 2.22: Rectangular Cavity

2.5.1 Simulation

The first two dominant modes are both modes with the electric field transverse to the z-axis where the coordinate system is described in Fig. 2.22 [42]. The wave number for the TE_{nml} mode is given by:

$$k_{nml} = \left[\left(\frac{l\pi}{d}\right)^2 + \left(\frac{m\pi}{b}\right)^2 + \left(\frac{n\pi}{a}\right)^2\right]^{1/2} \tag{2.45}$$

giving resonant frequencies at

$$f_{nml} = \frac{ck_{nml}}{2\pi} = c\left[\left(\frac{l\pi}{2d}\right)^2 + \left(\frac{m\pi}{2b}\right)^2 + \left(\frac{n\pi}{2a}\right)^2\right]^{1/2} \tag{2.46}$$

where a, b, and l are the dimensions of the cavity, and c is the speed of light.

The unloaded quality factor of a resonant cavity is found from:

$$Q_u = \omega\frac{W_m + W_e}{P_l} \tag{2.47}$$

where W_m and W_e are the energies stored in the magnetic and electric fields respectively, and P_l is the net power dissipated. In the case of the air filled cavity, the net power dissipated is purely the ohmic loss from the currents on the sides of the resonator. By neglecting the effects of the non-vertical sidewalls, the effects of the mousehole, any imperfections in bonding, and the by assuming all the current is concentrated in one skin depth, the quality factors for different resonances can be easily calculated using the known current and field distribution for a given cavity mode.

The wave number can be broken down into its components as:

$$k_x = \frac{m\pi}{a} \tag{2.48}$$

$$k_y = \frac{n\pi}{b} \tag{2.49}$$

$$k_z = \frac{l\pi}{d} \tag{2.50}$$

The fields within the cavity for the TE modes are solved by using the magnetic Hertz potential, $\bar{\pi}_m$. The magnetic Hertz potential satisfying boundary conditions for a cavity excited by a TE wave is:

$$\bar{\pi}_m = \hat{z}\cos(k_x x)\cos(k_y y)\sin(k_z z) \tag{2.51}$$

The electric and magnetic field can then be found from:

$$\bar{E} = -j\omega\mu\nabla \times \bar{\pi}_m \tag{2.52}$$

$$\bar{H} = \nabla\nabla \cdot \bar{\pi}_m + k^2\bar{\pi}_m \tag{2.53}$$

Substituting for equation 2.51 for $\bar{\pi}_m$ and simplifying, the field expression are:

$$E_x = j\omega\mu k_y \cos(k_x x)\sin(k_y y)\sin(k_z z) \tag{2.54}$$

$$E_y = j\omega\mu k_x \sin(k_x x)\cos(k_y y)\sin(k_z z) \tag{2.55}$$

$$H_x = -k_x k_z \sin(k_x x)\cos(k_y y)\cos(k_z z) \tag{2.56}$$

$$H_y = -k_y k_z \cos(k_x x)\sin(k_y y)\cos(k_z z) \tag{2.57}$$

$$H_z = (k^2 - k_z^2)\cos(k_x x)\cos(k_y y)\sin(k_z z) \tag{2.58}$$

The time average electric energy, W_e, is found from

$$\begin{aligned} W_e =& \frac{\epsilon}{4}\int_0^a\int_0^b\int_0^d \bar{E}\cdot\bar{E}^* dxdydz \\ =& \frac{\omega^2\mu^2\epsilon}{4}\left[k_y^2\left(\frac{a}{2}+\frac{\sin(2ak_x)}{4k_x}\right)\left(\frac{b}{2}-\frac{\sin(2bk_y)}{4k_y}\right)\right. \\ &\left. + k_x^2\left(\frac{a}{2}-\frac{\sin(2ak_x)}{4k_x}\right)\left(\frac{b}{2}+\frac{\sin(2bk_y)}{4k_y}\right)\right] \times \left(\frac{d}{2}-\frac{\sin(2dk_z)}{4k_z}\right) \end{aligned} \tag{2.59}$$

The time average electric energy, W_e, is found from

$$W_m = \frac{\mu}{4}\int_0^a\int_0^b\int_0^d \bar{H}\cdot\bar{H}^* dxdydz = W_e \tag{2.60}$$

The power loss, P_l, is the total power lost in the sidewalls of the cavity. P_l is found by

$$P_l = \frac{R_m}{2} \int_{walls} \bar{J}_s \cdot \bar{J}_s^* dS \tag{2.61}$$

where R_m is the surface resistance of the metalized sidewall. Since the current distribution within the sidewall is not constant, it is approximated that all the current is within the first skin depth. Therefore, $R_m = 1/(\sigma\delta_s)$ where σ is the conductivity of the metal and the skin depth is $\delta_s = \sqrt{2/(\omega\mu\sigma)}$. The surface current distribution can be found by:

$$\bar{J}_s = \hat{n} \times \bar{H} \tag{2.62}$$

The total power loss is given by:

$$\begin{aligned} P_l = & R_m \left[k_x^2 k_z^2 \left(\frac{a}{2} - \frac{\sin(2ak_x)}{4k_x} \right) \left(\frac{d}{2} + \frac{\sin(2dk_z)}{4k_z} \right) + \right. \\ & (k_x^2 + k_y^2)^2 \left(\frac{a}{2} + \frac{\sin(2ak_x)}{4k_x} \right) \left(\frac{d}{2} - \frac{\sin(2dk_z)}{4k_z} \right) + \\ & k_x^2 k_z^2 \left(\frac{a}{2} - \frac{\sin(2ak_x)}{4k_x} \right) \left(\frac{b}{2} + \frac{\sin(2bk_y)}{4k_y} \right) + \\ & k_y^2 k_z^2 \left(\frac{a}{2} + \frac{\sin(2ak_x)}{4k_x} \right) \left(\frac{b}{2} - \frac{\sin(2bk_y)}{4k_y} \right) + \\ & k_y^2 k_z^2 \left(\frac{b}{2} - \frac{\sin(2bk_y)}{4k_y} \right) \left(\frac{d}{2} + \frac{\sin(2dk_z)}{4k_z} \right) + \\ & \left. (k_x^2 + k_y^2)^2 \left(\frac{b}{2} + \frac{\sin(2bk_y)}{4k_y} \right) \left(\frac{d}{2} - \frac{\sin(2dk_z)}{4k_z} \right) \right] \end{aligned} \tag{2.63}$$

Substituting P_l and W_e into equation 2.47, the unloaded quality factor of the cavity for the TE_{101} mode is:

$$Q_{101} = \frac{(kad)^3 b Z_0}{2\pi^2 R_s (2a^3 b + 2d^3 b + a^3 d + d^3 a)} \tag{2.64}$$

where

$$Z_0 = \sqrt{\frac{\mu}{\epsilon}} \tag{2.65}$$

Similarly, the unloaded quality factor for the TE_{102} mode is:

$$Q_{102} = \frac{(kad)^3 b Z_0}{2\pi^2 R_s (8a^3 b + 2d^3 b + 4a^3 d + d^3 a)} \tag{2.66}$$

Given that $b < a, d$ for the micromachined cavity, the maximum quality factor for the TE_{101} mode is achieved by making $a = d = \lambda_0/\sqrt{2}$ and making b as large as possible. For a resonant mode of 24 GHz for the TE_{101} mode, both the width and length (a and b) of the cavity is set to 8.84 mm. The cavity is constructed from two standard thickness wafers (525 μm) and requires approximately 100 μm for the top and bottom of the cavity for structural rigidity. Therefore, the height of the cavity is set at 850 μm. The unloaded quality factor for the first two modes are 1240 for the TE_{101} at 24 GHz and 1560 for the TE_{102} mode at 38 GHz using the conductivity of gold as $3.9 \times 10^7\ \Omega^{-1}m^{-1}$. However, these values can be increased to 1620 and 2040 for the TE_{101} and TE_{102}, respectively, by using a silver as the metallic wall ($\sigma = 6 \times 10^7\ \Omega^{-1}m^{-1}$).

2.5.2 Fabrication

A thermal oxide is grown on two standard thickness silicon wafers to act as an etch mask for the micromachining process. The bottom wafer that contains the feedlines is a high resistivity substrate (2000 Ω-cm) and the top wafer is a low resistivity substrate (5-7 Ω-cm). The CPW feedlines are deposited on the bottom wafer using a gold electroplating process. Next, the oxide where the cavity is to be etched is removed with a wet chemical etch. The cavity resonator is defined 500 μm away from the end of the CPW feedline. The designed cavity dimensions are 8.84 mm $\times$ 8.84 mm for a TE_{011} resonant frequency of 24 GHz. The cavity is then etched 450 μm in an anisotropic silicon etchant (TMAH). The etchant has a selectivity to the $\langle 100 \rangle : \langle 111 \rangle$ crystal plane of approximately 25:1. This gives an undercut of roughly 15 μm leaving a small SiO_2 lip. It is essential to remove this lip in BHF to eliminate any gold

shadowing due to the lip that would produce a break in the gold between the upper and lower portions of the cavity and resulting in a very low quality factor. The CPW feedlines are then masked with photoresist and the entire cavity is metalized with a 3 μm layer of sputtered and electroplated gold. Four 18 μm thick gold wirebonds in parallel are used to excite the cavity. The wirebonds were approximately 1.2 mm long placed from the feedline in the corner of the cavity diagonally toward the center of the cavity with a calculated series inductance of 0.5 nH.

The top wafer is fabricated using a two step etch to allow for the mouseholes above the CPW feedlines. First, the cavity and the feedline mouse holes are patterned and the oxide is etched half way through. Next, the cavity alone is patterned and the remaining oxide covering the cavity is etched exposing the bare silicon. The substrate is then placed in the anisotropic etchant and the cavity is etched 350 μm down. The remaining oxide covering the feedline mouseholes is carefully etched away making sure not to completely etch the oxide protecting the surrounding areas. Again, the substrate is placed in the silicon etchant for another 100 μm of etching yielding a cavity depth of 450 μm and the mousehole depth of 100 μm. The thermal oxide is completely stripped off eliminating the lip formed from the undercut of the silicon etching. The top wafer is then metalized with a 3 μm layer of sputtered and electroplated gold. The two substrates are bonded using conductive epoxy.

2.5.3 Measurements

The cavity resonator was measured with an HP8510C using an SOLT calibration with the probe tips as the calibrated reference plane. The measured TE_{101} resonant mode was 23.97 GHz which is in excellent agreement with the designed value of 24 GHz. At resonance, the measured S_{21} is -15.2 dB with a loaded quality factor (Q_l) of 909, resulting in an Q_u of 1100, which is in good agreement with the calculated value of 1237. The calculated value does not include the increase resistance from the

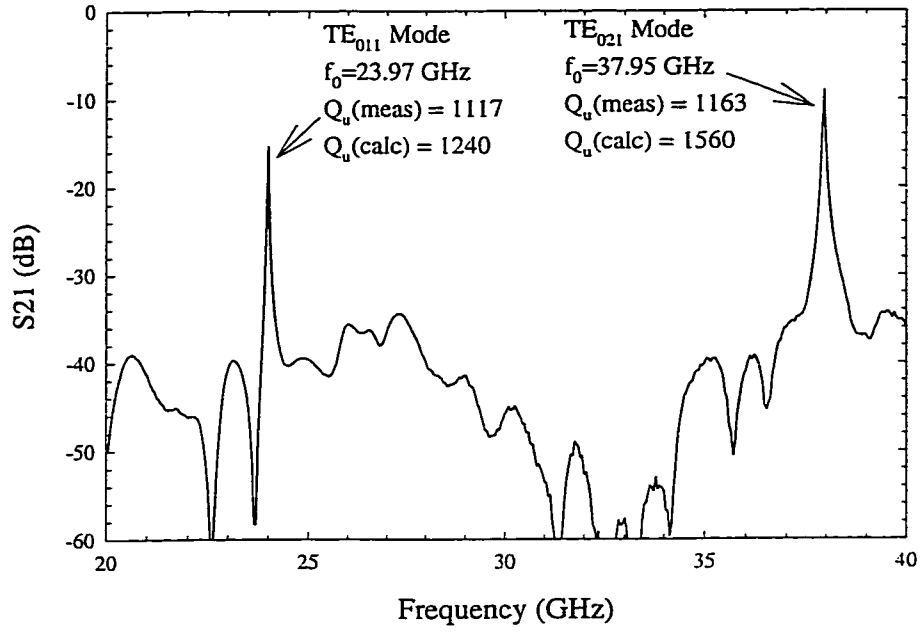


Figure 2.23: Two wafer micromachined cavity resonator.

silver epoxy bonding, the effects of the mouse holes altering the current distribution on the resonator, or the loss in the 2 mm CPW feedlines. The combined loss of both feedlines is 0.6 dB. Subtracting this from the measured S_{21} gives a Q_u of 1117. The TE_{021} occurs at 37.95 GHz with a measured value of Q_l of 690 with an S_{21} of -7.9 dB. When the loss of the CPW feedlines (0.75 dB at 38 GHz) is removed, the Q_u is 1163. To the author's knowledge, this is the highest Q integrated resonator to date at K-band, and could be used in low-phase noise millimeter-wave oscillator designs.

2.6 Conclusions

In this chapter, a detailed procedure for measuring the quality factor of a microstrip resonator is discussed. Micromachining techniques have then been applied to fabricate high-Q integrated microstrip resonators. The fabrication is compatible

with most CMOS and MMIC processes. Finite element modeling was performed with good agreement with measured data on a transition from CPW-on-silicon to microstrip-on-membrane. Micromachined suspended microstrip lines exhibit quality factors in the range of 450-500 at 29, 37, and 62 GHz in both bandpass and bandstop configurations with conductor loss limited performance. Furthermore, calculations using Simian show that practical considerations limit the Q of suspended microstrip resonators to 550. These resonators can be easily used in complex filter designs [43].

Integrated miniature waveguide cavity resonators have also been fabricated at 24 GHz (dominant mode) with a quality factor of 1100-1200. The micromachined waveguide cavities can be readily scaled to 60 GHz (3.5 mm $\times$ 3.5 mm $\times$ 800 μm with a calculated $Q_u = 1600$) and to 77 GHz (2.8 mm $\times$ 2.8 mm $\times$ 800 μm with a calculated $Q_u = 1670$) using standard thickness wafers for communication systems and automotive radars.

CHAPTER 3

SUSPENDED MICROSTRIP FILTER SYNTHESIS

3.1 Introduction

Modern microwave and millimeter-wave communications have strict requirements for filter performance. Narrow bandwidths with high rejection to prevent adjacent channel interference are necessary with an increasing number of competing communication, radar, and radiometry systems. Also, there is a strong demand for low-power, low-noise systems putting an emphasis on reduced filter insertion loss.

Membrane suspended microstrip resonators have been demonstrated to have a high quality factor for a compact, planar structure (Chapter 2). This allows for a higher level of integration of resonant elements with reduced cost, volume, and weight compared to competitive technologies such as dielectric and waveguide resonators. However, a high-Q resonator does not produce a good filter without a proper method of filter synthesis. Empirical models for microstrip transmission line coupling schemes do exist [44], [45], [46], but are not accurate for exact synthesis of discontinuities of transmission lines for narrow-band resonant structures [47]. Full-wave 3-dimensional field solvers have been developed which simulate filter structures accurately. However,

they provide more of an analysis tool than a synthesis tool. For filter synthesis, the full-wave solvers must be used in conjunction with an analytical method for a filter complete design.

This chapter presents a method used for accurate filter synthesis by mapping a pair of coupled resonators to a lumped-element equivalent model for the resonators and the coupling scheme. This results in a minimum of time-intensive simulation for large, multi-resonator filter structures. Specifically, this method is applied to a membrane suspended microstrip bandpass filter. The full-wave design is compared to measured results and also with simulations based on accepted empirical models.

3.2 Direct-Coupled Resonator Filter Synthesis from Two Element Pole Splitting

The method of direct-coupled resonator filter synthesis from pole splitting involves analyzing the effects of two coupled resonators and maps the change in resonant response to an impedance inverter that describes the coupling scheme. The impedance inverter that represents the coupling is then mapped to a lumped element equivalent circuit. Once the structure is mapped, for several geometries, the filter can be designed by interpolation. The synthesis of the lumped element equivalent circuit is well published [4], [20] and will not be derived in this chapter. The individual resonators used should be resonant at the same frequency. This method can be modified to allow for resonators with different resonant frequencies, but is not included in this chapter as all the filters developed in this work are based on resonators with the same resonant frequencies.

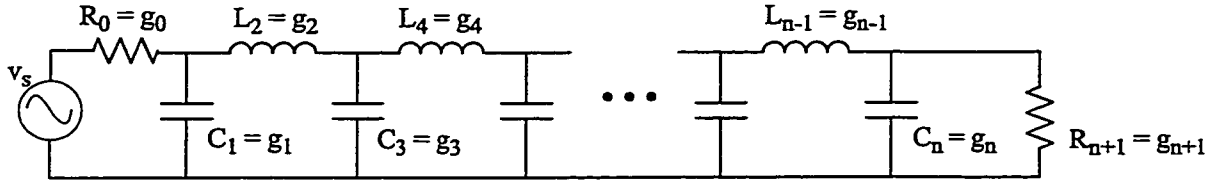
The derivation of this method is in the opposite order. First, the low-pass prototype filter is mapped to a bandpass lumped-element filter. This filter is then described in terms of shunt resonators that are coupled together with admittance inverters. The admittance inverter is related to the resonance points of two coupled resonators by

the method of pole splitting. This admittance inverter controls the coupling between the resonators and determines the filter response. The geometry of the filter is synthesized using interpolation (if needed) and the filter design is complete.

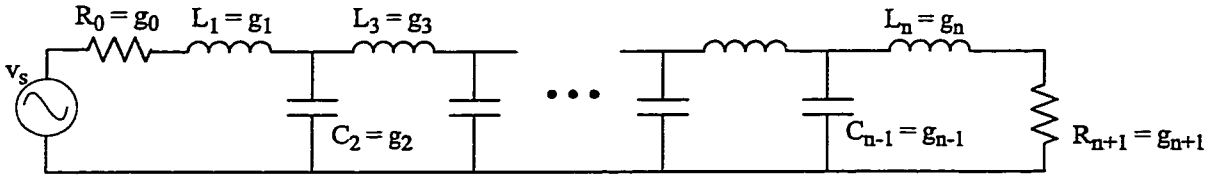
3.2.1 Lumped Element Prototype

The majority of filter design is based on generalized low-pass filter prototypes with a source impedance of 1 Ω and an upper frequency cut-off of ω_c=1. The generalized filter prototype is then transformed to either a low-pass filter with different cut-off and source impedance, a high-pass, a bandpass, or a bandstop filter. The work presented will focus only on bandpass filter transformations and design. A typical lumped element low-pass prototype is shown in Fig. 3.1a and b. The elements g_i are the low-pass prototype filter element values and are extracted from the type of low-pass prototype used. For conventional Maximally flat and Chebyshev designs, these values are tabulated in [4]. Two low-pass filter prototypes are shown in Fig. 3.1. The first begins with a shunt element and the out of band rejection is that of a large shunt capacitance tending toward a short circuit. The second prototype begins with a series inductor that rejects as an inductance tending toward an open circuit.

The low-pass prototype filters can be changed to lumped element bandpass filters by using a transformation (Fig. 3.1c and d). For the transformation, each of the shunt capacitors, C_j in Fig. 3.1a and b are replaced by a parallel LC resonator with $C_j = g_j \omega_1'/(\omega_0 \bar{\omega})$ and $L_j = \bar{\omega}/(g_j \omega_0 \omega_1')$ in Fig. 3.1c and d. Similarly, each series inductor, L_j, in the low-pass prototype is replaced by a series LC resonator with $C_j = \bar{\omega}/(g_j \omega_0 \omega_1')$ and $L_j = g_j \omega_1'/(\omega_0 \bar{\omega})$ where ω_0 is the center frequency of the filter defined as $\omega_0 = \sqrt{\omega_1 \omega_2}$ with ω_1 and ω_2 being the lower and upper cut-off frequencies of the bandpass filter, $\bar{\omega}$ is the fractional bandwidth of the bandpass filter defined as $\bar{\omega} = (\omega_2 - \omega_1)/\omega_0$, and ω_1' is the cut-off frequency of the low-pass prototype filter used (typically $\omega_1' = \pi/2$).



(a)



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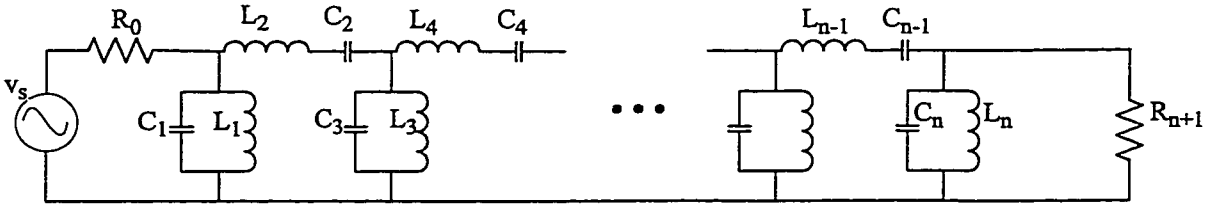

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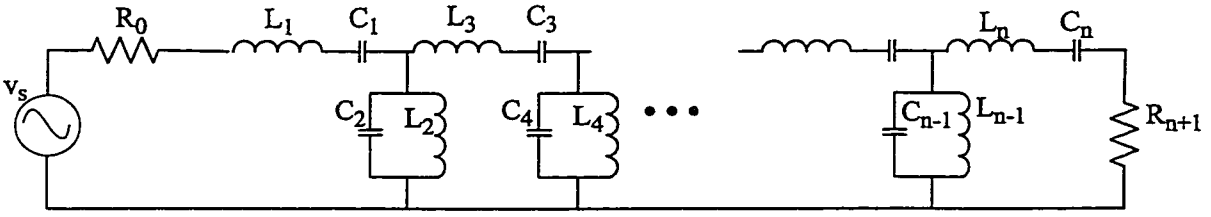
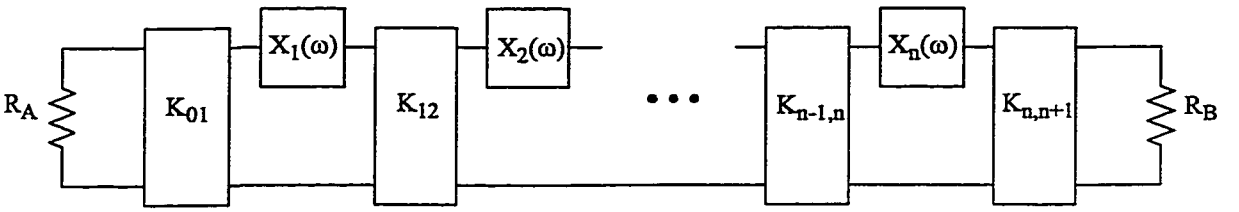
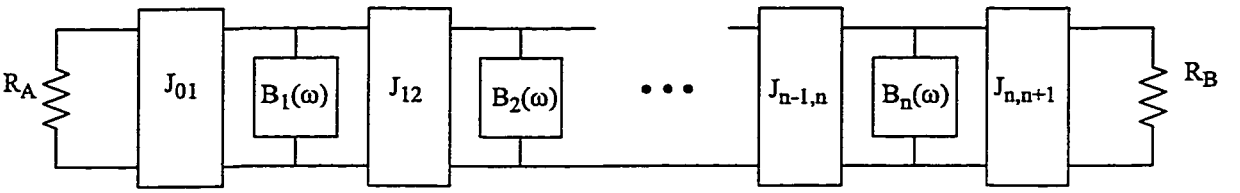


(d)

Figure 3.1: Lumped element filter prototypes in (a) shunt first low-pass prototype, (b) series first low-pass prototype, (c) bandpass transformed shunt first prototype, and (d) bandpass transformed series first prototype filter.



(a)



(b)

Figure 3.2: Equivalent circuit model of a bandpass filter using (a) series resonators with K-inverters and (b) shunt resonators with J-inverters.

3.2.2 Ideal Impedance Inverters

In practical microwave and millimeter-wave circuits, it is difficult to realize both shunt and series resonators simultaneously. Also, each resonator has a reactance slope due to the different values of L and C within the filter. This requires the design of each resonator in the filter to be slightly different. By using an impedance/admittance inverter, the shunt resonator can be transformed into a series resonator (or the series resonator to a shunt resonator) allowing for a single type of resonator to be used. This results in a filter with only series resonators or only shunt resonators with impedance/admittance inverters in between each resonator. The equivalent circuit for a bandpass filter with impedance/admittance inverters is shown in Fig. 3.2. In Fig. 3.2a, the shunt resonators are transformed into series resonators by means of an impedance inverter. The series resonators are denoted as $X_n(\omega)$ and the impedance

inverters are $K_{n,m}$ where n and m are the element values. Similarly, in Fig. 3.2b, the series resonators are transformed into shunt resonators by means of an admittance inverter. The shunt resonators are denoted as $B_n(\omega)$ and the impedance inverters are $J_{n,m}$. The J and K inverters are used to control the coupling between resonators which determines the filter response. The only aspect that the resonators control is the center frequency and the amount of filter degradation associated with the dissipation of energy due to the resonator. Ideally, the impedance/admittance inverters are not a function of frequency and the filter response is governed only by the resonators and the value of the inter-resonator coupling (impedance inverter). However, practical implementation of inverters are frequency dependent limiting the total realizable filter bandwidth.

The majority of the work presented in this thesis uses shunt type resonators. Therefore, the discussion on the inverters will be limited to dealing with admittance, J-type inverters. An ideal admittance inverter has the transforming property of:

$$Y_a = \frac{J^2}{Y_b} \tag{3.1}$$

where Y_b is the original admittance of the load, J is the size of the inverter, and Y_a is the transformed admittance (Fig. 3.3). This ideal transformer has a $\pm 90°$ phase shift. This allows for a straightforward method of calculating and measuring the resonator coupling coefficient between elements. If $B_j(\omega)$ is the susceptance of the j^{th} resonator in the filter, then let b_j be the susceptance slope parameter of the j^{th} resonator as defined by:

$$b_j = \frac{\omega_0}{2} \frac{dB_j(\omega)}{d\omega}|_{\omega=\omega_0} \tag{3.2}$$

For an ideal lumped element LC shunt resonator, this reduces simply to $b_j = \omega_0 C_j = 1/(\omega_0 L_j)$. By applying impedance scaling and solving for the J terms from the ideal

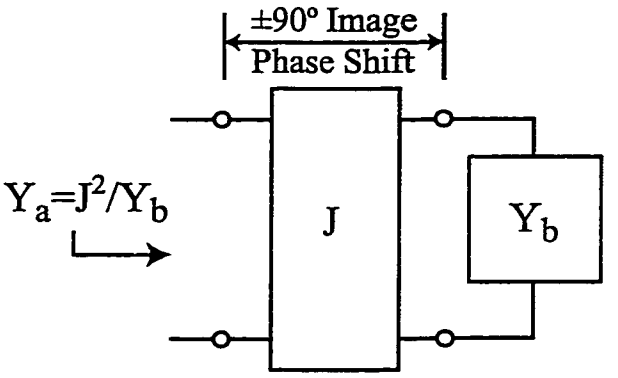


Figure 3.3: Ideal admittance inverter.

bandpass lumped element model shown in Fig. 3.1b, the J terms are [4]:

$$J_{01} = \sqrt{\frac{G_A b_1 \bar{\omega}}{g_0 g_1 \omega_1'}} \tag{3.3}$$

$$J_{j,j+1}|_{j=1\,to\,n-1} = \frac{\bar{\omega}}{\omega_1'}\sqrt{\frac{b_j b_{j+1}}{g_j g_{j+1}}} \tag{3.4}$$

$$J_{n,n+1} = \sqrt{\frac{G_B b_n \bar{\omega}}{g_n g_{n+1} \omega_1'}} \tag{3.5}$$

where G_A and G_B are the source and load conductance, respectively ($G_A = 1/R_A$ and $G_B = 1/R_B$ from Fig. 3.1).

The change in the magnitude of the transformed loads allows for arbitrary matching of resonators. In conventional lumped-element filter design, the resonator elements must have exact values for the L's and C's in order to determine the proper coupling to each resonator. However, with the use of transformers, there is no unique solution. Any arbitrary resonator can be used by finding the susceptance slope parameter of the resonator and calculating the correct J inverter. For instance, a single high-Q resonator can be developed, optimized, and characterized. This one resonator can then be used for each resonator in the filter just by changing the value of the J inverter as opposed to designing different resonators for the values of the L's and C's in the prototype [20]. By using identical resonators, the filter design is greatly simplified

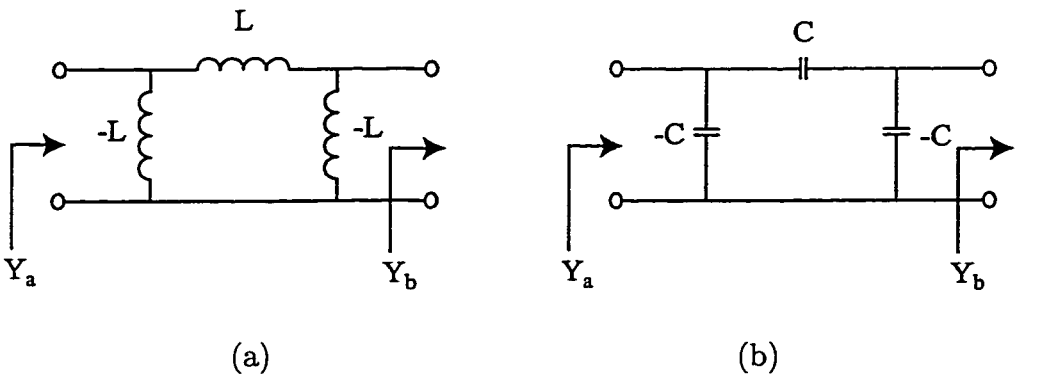


Figure 3.4: Ideal lumped element admittance inverter.

by eliminating the need to tune the center frequency of each resonator. Also, the insertion loss of the filter is improved by using a resonator that has been optimized for a high Q. This allows for an overall higher performance filter.

Such an inverter can be realized over a narrowband frequency range by a quarter-wave line of characteristic admittance of J. The J-type resonator can also be realized using ideal dissipationless lumped elements such as inductors or capacitors as shown in Fig. 3.4. Such structures have a much wider bandwidth than the quarter-wave transmission line. The J-inverter is $J = 1/(\omega L)$ for the inductive model, and $J = \omega C$ for the capacitive model. The coupling scheme of the resonator determines which inverter is to be used.

3.2.3 Practical Design and Measurement of Impedance Inverters

In many distributed circuits, a lumped element equivalent circuit for a resonator is not available. Also, the susceptance slope is not an easily measured quantity at microwave and millimeter wave frequencies. Therefore, it is desirable to use an alternate method of finding the coupling between two resonators.

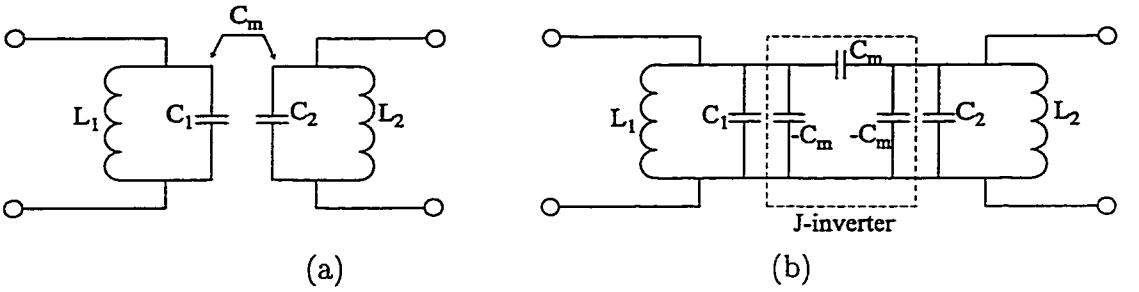


Figure 3.5: Two element capacitively coupled resonator in (a) standard form and (b) π-network equivalent form.

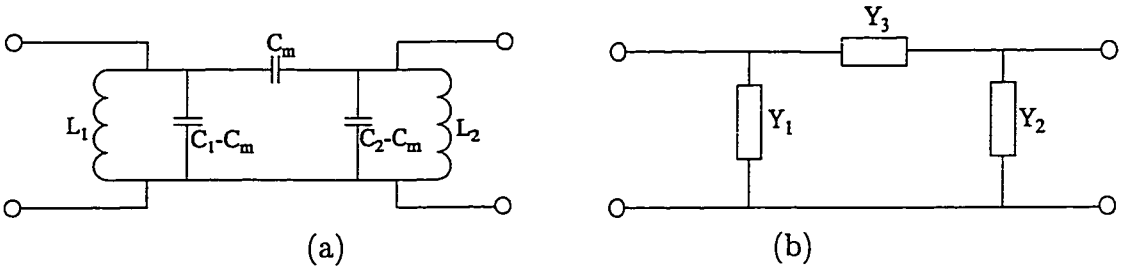


Figure 3.6: (a) Two element capacitively coupled resonator with mutual capacitance absorbed into resonator capacitance and (b) hybrid π-network structure.

Inter-Resonator Coupling

Consider two coupled resonators that are capacitively coupled by a mutual capacitance C_m as shown in Fig. 3.5a. Both resonators are resonant at the same frequency ($1/\sqrt{L_1C_1} = 1/\sqrt{L_2C_2} = \omega_0$). The mutual capacitive coupling can be represented in alternate form by use of an ideal capacitive π-network as shown in Fig. 3.5b. By absorbing the negative capacitance into the the resonator, a new π-network is formed as in Fig. 3.6a. By letting the resonators correspond to elements Y_1 and Y_2 and the series capacitance be Y_3, the equivalent network is shown in Fig. 3.6b where:

$$Y_1 = \frac{1 - \omega^2 L_1(C_1 - C_m)}{j\omega L_1} \tag{3.6}$$

$$Y_2 = \frac{1 - \omega^2 L_2(C_2 - C_m)}{j\omega L_2} \tag{3.7}$$

$$Y_3 = j\omega C_m \tag{3.8}$$

The network response of a π-network can easily be solved using $ABCD$ matrix representation where:

$$A = 1 + \frac{Y_2}{Y_3} \qquad B = \frac{1}{Y_3} \tag{3.9}$$

$$C = Y_1 + Y_2 + \frac{Y_1 Y_2}{Y_3} \qquad D = 1 + \frac{Y_1}{Y_3} \tag{3.10}$$

By substituting the correct values for $Y_{1,2,3}$, the $ABCD$ matrix becomes:

$$A = \frac{\omega^2 L_2 C_2 - 1}{\omega^2 L_2 C_m} \qquad B = \frac{1}{j\omega C_m} \tag{3.11}$$

$$C = \frac{1 - \omega^2(C_1 L_1 + C_2 L_2) + \omega^4(C_1 L_1 C_2 L_2 - C_m^2 L_1 L_2)}{-j\omega^3 L_1 L_2 C_m} \qquad D = \frac{\omega^2 L_1 C_1 - 1}{\omega^2 L_1 C_m} \tag{3.12}$$

Since the each resonators have the same resonant frequency, the C term can be simplified to

$$C = \frac{\left[1 - \omega^2\sqrt{L_1 L_2}\left(\sqrt{C_1 C_2} - C_m\right)\right]\left[1 - \omega^2\sqrt{L_1 L_2}\left(\sqrt{C_1 C_2} + C_m\right)\right]}{-j\omega^3 L_1 L_2 C_m} \tag{3.13}$$

The Z-parameters can then be found from the $ABCD$ matrix by

$$Z_{11} = \frac{A}{C} \tag{3.14}$$

$$= \frac{j\omega L_1(1 - \omega^2 L_2 C_2)}{\left[1 - \omega^2\sqrt{L_1 L_2}\left(\sqrt{C_1 C_2} - C_m\right)\right]\left[1 - \omega^2\sqrt{L_1 L_2}\left(\sqrt{C_1 C_2} + C_m\right)\right]} \tag{3.15}$$

$$Z_{21} = \frac{AD - BC}{C} \tag{3.16}$$

$$= \frac{-j\omega^3 L_1 L_2 C_m}{\left[1 - \omega^2\sqrt{L_1 L_2}\left(\sqrt{C_1 C_2} - C_m\right)\right]\left[1 - \omega^2\sqrt{L_1 L_2}\left(\sqrt{C_1 C_2} + C_m\right)\right]} \tag{3.17}$$

This shows that there are a natural resonances at:

$$\omega_e = \frac{1}{\sqrt{\sqrt{L_1 L_2}(\sqrt{C_1 C_2} - C_m)}} \tag{3.18}$$

$$\omega_o = \frac{1}{\sqrt{\sqrt{L_1 L_2}(\sqrt{C_1 C_2} + C_m)}} \tag{3.19}$$

where ω_e and ω_o are the even and odd mode resonances of the structure. Eliminating L from the above equations:

$$\frac{C_m}{\sqrt{C_1 C_2}} = \frac{\omega_e^2 - \omega_o^2}{\omega_e^2 + \omega_o^2} = \frac{f_e^2 - f_o^2}{f_e^2 + f_o^2} \tag{3.20}$$

Equation 3.20 relates the pole splitting effect of coupled resonators to the mutual capacitance between the resonators and the capacitances of the resonators. For distributed circuits, it is more convenient to work in terms of the susceptance slope parameter, b_j, from equation 3.2. For the lumped element case presented, $b_j = \omega_0 C_j$. Therefore, the pole splitting results in:

$$\frac{\omega_0 C_m}{\sqrt{b_1 b_2}} = \frac{f_e^2 - f_o^2}{f_e^2 + f_o^2} \tag{3.21}$$

By the definition of the J parameter, $J_{12} = \omega C_m$, the pole separation is related to the J inverter and the slope susceptance parameter at resonance by:

$$\frac{J_{1,2}}{\sqrt{b_1 b_2}} = \frac{f_e^2 - f_o^2}{f_e^2 + f_o^2} \tag{3.22}$$

The distance between two poles of two distributed coupled resonators can accurately be simulated and measured and is insensitive to line loss and calibration error. The term $C_m/\sqrt{C_i C_j}$ is referred to as the coupling coefficient, k_{ij}, between resonators i and j. The coupling coefficient is related to the J inverter parameter by:

$$k_{ij} = \frac{C_m}{\sqrt{C_i C_j}} = \frac{J_{ij}}{\sqrt{b_i b_j}} \tag{3.23}$$

The ideal filter parameters are related to the admittance inverter by equation 3.4. Substituting equation 3.4 into equation 3.23, the value of k_{ij} to result in the designed filter parameters is given by:

$$k_{j,j+1}|_{j=1 \text{ to } n-1} = \frac{\bar{\omega}}{\omega_1'} \sqrt{\frac{1}{g_j g_{j+1}}} \tag{3.24}$$

Resonator to Load Coupling

The input/output resonator-to-load couplings can be calculated by observing how the Q_{ext} of the first/last resonator change with coupling values. For a frequency independent J-inverter, the transformed impedance is $Y_a = J^2/Y_b$. If G_A and G_B are the input and output admittances of a filter, then the transformed admittances

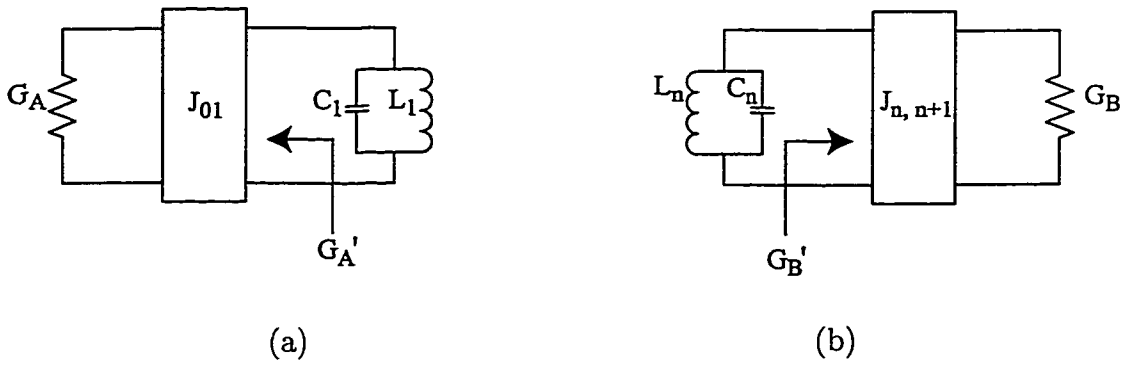


Figure 3.7: Lumped element resonator to load coupling for (a) input and (b) output.

present at the input/output resonators, $G'_{A/B}$ are:

$$G'_A = \frac{J_{01}^2}{G_A} \tag{3.25}$$

$$G'_B = \frac{J_{n,n+1}}{G_B} \tag{3.26}$$

Once the loading is known, the external Q of the resonator can be found by:

$$Q_{ext} = \frac{R_{ext}}{\omega_0 L} = \frac{b}{G_{ext}} \tag{3.27}$$

where b is the susceptance slope parameter of the first/last resonator. Solving for the external Q for the input and output,

$$(Q_{ext})_A = \frac{b_1}{J_{01}^2/G_A} \tag{3.28}$$

$$(Q_{ext})_B = \frac{b_n}{J_{n,n+1}^2/G_B} \tag{3.29}$$

By substituting in the values of J from equation 3.3 and equation 3.5, the ideal values for the external Q are:

$$(Q_{ext})_A = \frac{g_0 g_1 \omega'_1}{\bar{\omega}} \tag{3.30}$$

$$(Q_{ext})_B = \frac{g_n g_{n+1} \omega'_1}{\bar{\omega}} \tag{3.31}$$

Typical values of external Q's are on the order of 20-40 for low to moderate bandwidths. The external Q of a resonator cannot be directly measured, but the loaded

Q (Q_L) can be measured or simulated. If the unloaded Q (Q_U) of the resonator is known, the external Q (Q_{ext}) can be found by:

$$\frac{1}{Q_{ext}} = \frac{1}{Q_L} - \frac{1}{Q_U} \tag{3.32}$$

Therefore, the loaded Q of the first and last resonator should be set to:

$$\frac{1}{(Q_L)_A} = \frac{\bar{\omega} Q_U}{g_0 g_1 \omega_1' Q_U + \bar{\omega}} \tag{3.33}$$

$$(Q_L)_B = \frac{\bar{\omega} Q_U}{g_n g_{n+1} \omega_1' Q_U + \bar{\omega}} \tag{3.34}$$

3.3 Synthesis of Bandpass Filters from Simulated Pole Splitting

This section discusses the synthesis of a bandpass filter and shows the simulated and measured results. The filter design parameters are for a 4-pole Chebyshev filter with a 5.5% relative bandwidth, 0.1 dB of pass band ripple, and a center frequency of 28.0 GHz. The resonators are based on 800 μm wide microstrip lines suspended on a 250 μm high ground plane with a dielectric membrane. There is a shielding cover that is 800 μm from the line. The sidewalls of the structure are 800 μm from the line adding considerable parasitic capacitance. The resonators are 5 mm long ($\lambda/2$ at 28 GHz including fringing capacitance). This is similar to the resonator discussed in Chapter 2 with a Q of 460 and an intrinsic impedance of 62 Ω.

The topology for the bandpass filter capacitively coupled bandpass filter demonstrated by Blondy, Brown, et al. [43] is shown in Figure 3.8. The resonators are $\lambda/2$ lengths of capacitively end-coupled microstrip transmission lines. The equivalent model for the $\lambda/2$ lines is a shunt resonator. The end-coupling of the microstrip lines act as a capacitive J-inverter as in Fig. 3.4b where the series capacitance is the capacitance between the lines and the shunt capacitance models the phase delay across the gap between the lines. The feedlines are coplanar waveguide lines on silicon with an abrupt transition to microstrip at the edge of the membrane. The ground plane wafer

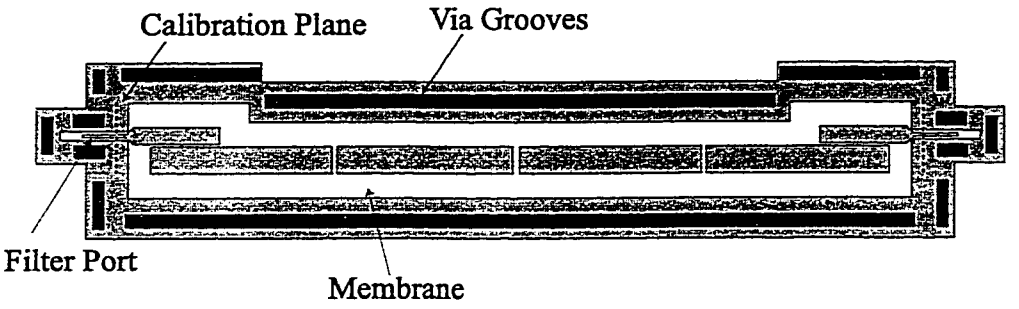


Figure 3.8: Topology for 4-Pole filter design

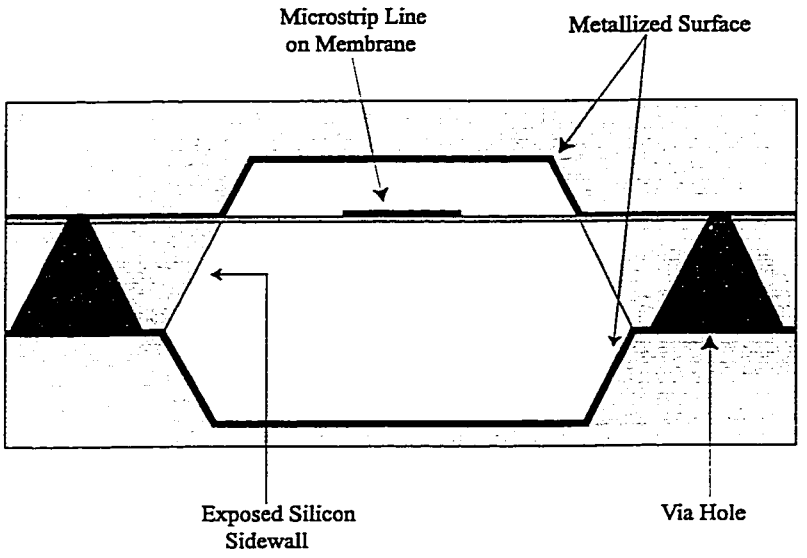
is etched to conform to the membrane area and has small "mouseholes" over the CPW lines. The edge of the mouseholes contact the CPW ground planes, and act as a via from the CPW ground plane to the microstrip ground plane at the silicon/membrane interface. Due to the anisotropic etching properties of the etchant used for fabrication, these ground vias are 1 mm from the signal conductor and add inductance (0.05-0.06 nH) in the CPW-to-microstrip ground plane transition. Immediately following this transition, an edge coupled $\lambda/4$ section of microstrip transmission line is used. The $\lambda/4$ section reduces the effects of the series inductance and the abrupt change in permittivity in the silicon-to-air interface. It also acts as a transformer coupling to the filter and sets the external Q. This filter has the same equivalent model of Fig. 3.2c.

3.3.1 Inter-Resonator Couplings

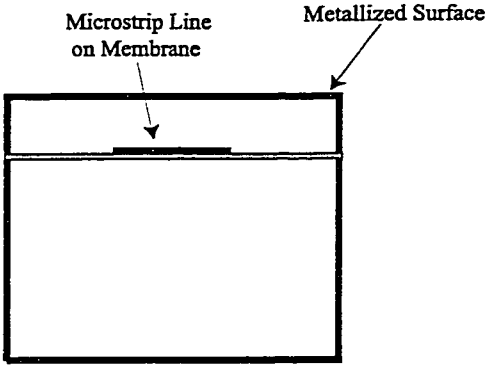
The first step in the synthesis of bandpass filters is to relate the geometry of the filter structure to the J inverter coupling coefficients (k_{ij}). This is done by simulating two resonant lines with varying gap dimensions (Fig. 3.10) with weak external coupling. The choice of a full-wave simulation tool is a critical decision for obtaining

accurate enough results for a filter design. The most important design criteria for calculating the inter-resonator couplings are the resonant frequencies of the individual resonators, the susceptance slope parameter, and the J-inverter value. Since the susceptance slope parameter and the J-inverter value are related to each other by the resonator pole splitting, a high degree of frequency resolution is necessary. It is also not necessary for a full frequency spectrum to be generated, but rather just near the resonances to save in computational time. This leads to using a frequency domain method such as FEM and MoM. Also, it is necessary to include the dielectric membrane in the simulations (t = 1.4 μm with ϵ_r=5). The presence of the dielectric membrane increases the overall effective dielectric constant of the microstrip from an air dielectric of 1 to 1.05 [48], thereby shifting the resonance down in frequency. Also, the coupling is predominately capacitive between the ends of the lines. When the coupling gap becomes small (less than 200 μm), the electric fringing fields are more affected by the dielectric membrane. This creates a higher capacitance and coupling coefficient. The presence of the dielectric membrane would greatly increase the complexity of a FEM mesh, while the MoM has little difficulty in dealing with this.

The simulations were done using Sonnet EM [49], a commercially available method of moments package. This simulation includes the effects of the thin dielectric membrane. In the actual circuit, the sidewalls between the microstrip and the ground plane are coated with gold. However, in the region between the membrane and the shielding cover, there is a region of silicon on the sidewalls before the via grooves that is not shielded (Fig. 3.9a). At the present time, there is not a method of moments tool that can analyze the effects of the dielectric wall on the coupling between resonators. The Sonnet EM is a "closed box" 2 1/2-D simulator. The sides of the box are lined with a perfect electric conductor (PEC) that models the micromachined channel sidewalls and shielding cover as PEC's (Fig. 3.9b).



(a)



(b)

Figure 3.9: Cross section of (a) actual filter structure and (b) simulated filter structure.

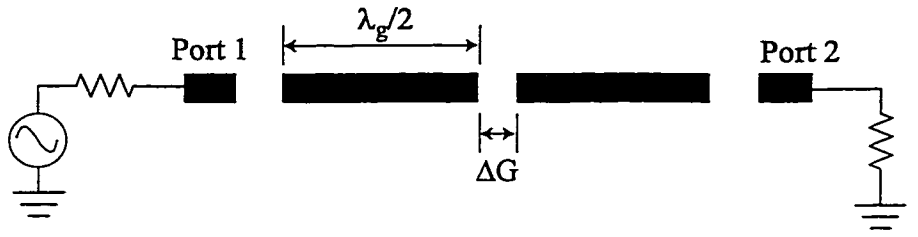


Figure 3.10: Insertion Loss of two weakly coupled resonators for varying gap sizes.

The transmission for the resonators for various gap widths is given in Fig. 3.11. This shows the two resonances from the pole splitting of the resonators. The coupling coefficient, k, can then be extracted and plotted (Fig. 3.12). The coupling for an arbitrary gap size is then found by a curve fit using the equation:

$$k(G) = 0.134654 + \frac{1.17939}{G} - 0.0205604 \ln(G) \tag{3.35}$$

The same structure was simulated with HP Libra, Series IV [50] using the MLIN model for the microstrip lines and the MGAP model for the gaps between resonators. This model neglects the effects of the dielectric membrane and metallic sidewalls, but does model the shielding cover. There is a strong disagreement between the moment method and the empirical MGAP model (Fig. 3.13). By neglecting the dielectric membrane and the metallic sidewalls, the capacitance should have been decreased resulting in a decrease in coupling coefficient. For small gap widths, the Libra model greatly overestimates the coupling coefficient while underestimating it for large gap widths.

The coupling coefficients needed for the inter-resonator coupling are calculated using equation 3.24 for the filter design (4-pole, Chebyshev filter with 5.5% bandwidth and 0.1 dB ripple) and are given in Table 3.1.

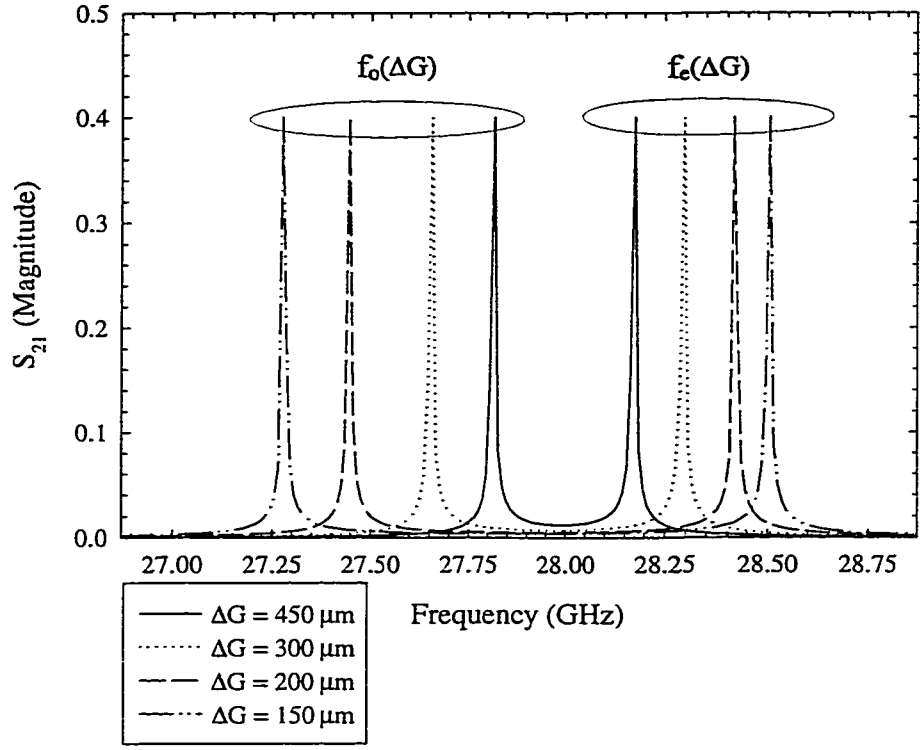


Figure 3.11: Simulated insertion loss of two coupled resonators for varying gap widths. Note that the distance between the two resonances increase with decreasing gap width (increasing coupling capacitance, C_m).

Table 3.1: Summary of Inter-Resonator Couplings

i	Coupling $k_{i,i+1}$	Gap Width $g_{i,i+1}$
1	0.042	140 μm
2	0.033	190 μm
3	0.042	140 μm

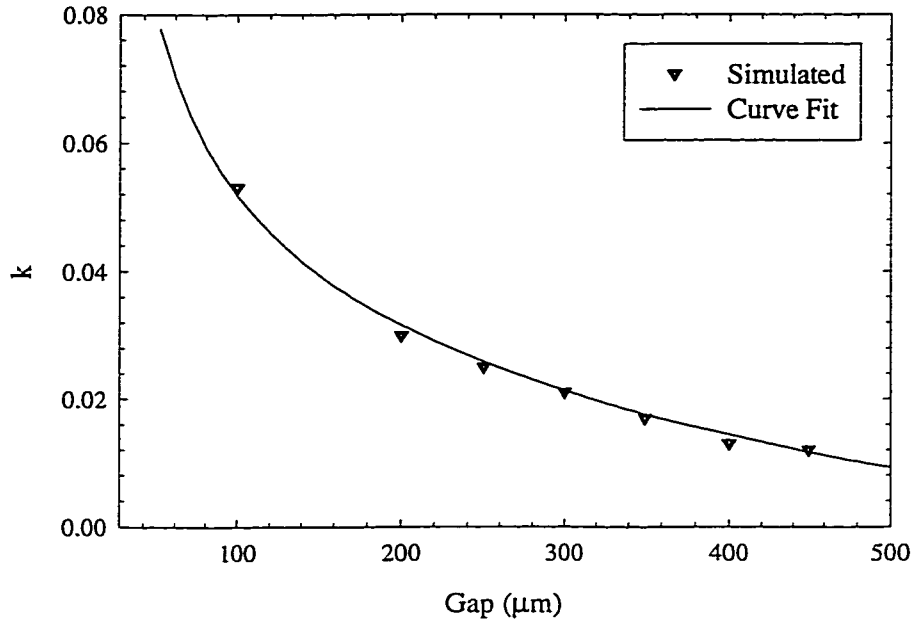


Figure 3.12: Coupling coefficient of two coupled micromachined resonators as a function of gap size.

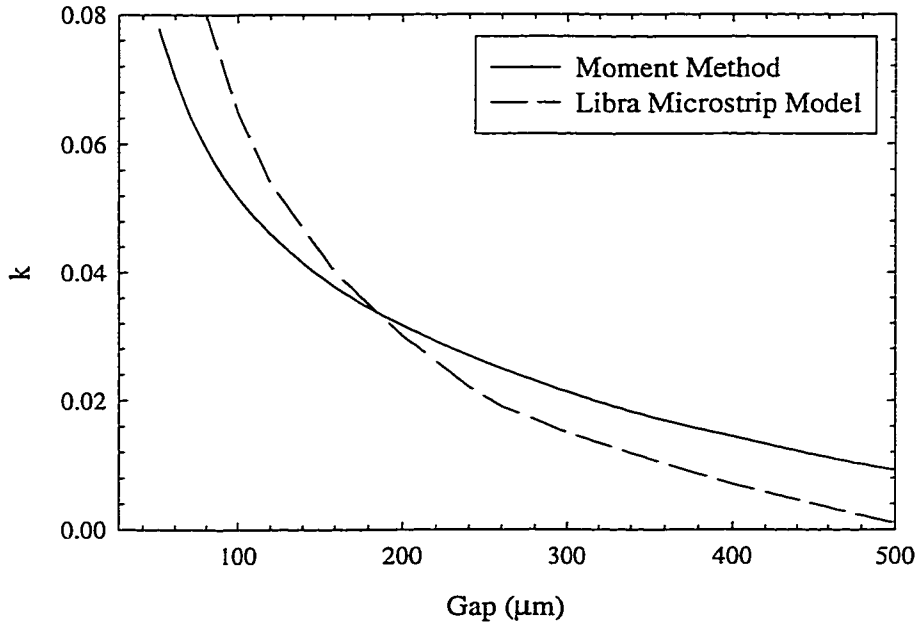


Figure 3.13: Comparison of Libra models for microstrip gaps (MGAP) with full wave analysis.

3.3.2 External Coupling

The external coupling is set by the external Q of the first/last resonator. If the unloaded quality factor of the resonator is known, the external Q can be extracted by looking at the reflection coefficient for a one port coupling to an open ended resonator (Fig. 3.14). The loaded Q can be found by taking the inverse of the fractional bandwidth over which the phase of the reflection coefficient changes by 180° centered at resonance, $Q_L = 1/\delta f$ (Fig. 3.15). The length of the feedline, L_1, must be deembedded from the reflection coefficient for accurate phase response. The deembedding of the phase was done graphically by changing the slope of the phase response to compensate for the phase of the feedline. The reflection coefficient for several geometries was found using Sonnet EM for the structure from beginning of the microstrip on membrane section. The effect of the silicon-to-membrane transition is then included by adding the appropriate inductance[1] (100 pH) and using a linear circuit simulator [50] to solve for the total reflection coefficient (Fig. 3.16). As the gap distance increases, the effects of the loading are decreased as shown by an increasing slope in the phase of the reflection coefficient (Q_L increases). Since the unloaded quality factor of this resonator is known, the external quality factor can then be plotted using equation 3.32 as a function of gap dimension, and is used for synthesis (Fig. 3.17). For the filter demonstrated in this section, the ideal Q_{ext} from equation 3.30 is 31.7. This corresponds to a coupling gap of approximately 70 μm from the plot in Fig. 3.17. This completes the entire filter design without ever running a full-wave simulation of the entire filter structure.

[1]The series inductance due to the transition was analyzed in Chapter 2 as a function of ground plane height and mousehole width. Values of inductance are taken from Fig. 2.13.

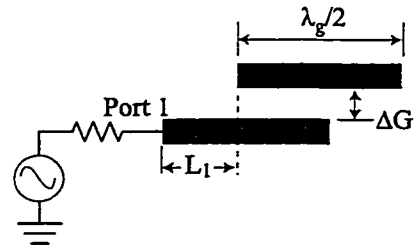


Figure 3.14: Method of simulating a one port coupling to a resonator for the extraction of the external Q.

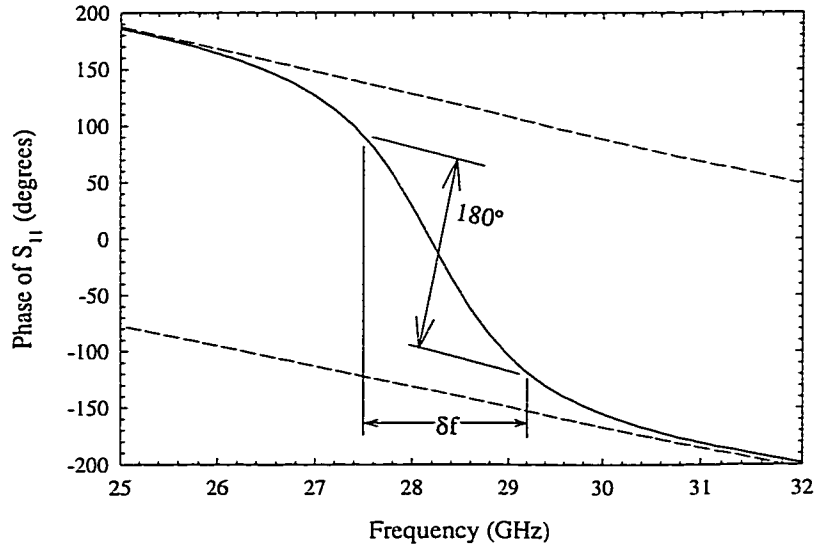


Figure 3.15: Reflection coefficient for a 28 GHz resonator. The loaded Q is given by the reciprocal of the fractional bandwidth over which a 180° phase shift occurs.

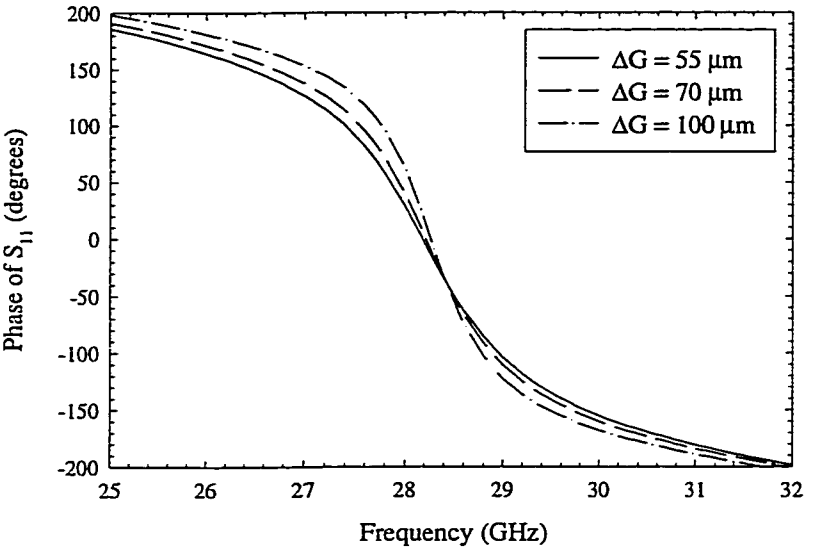


Figure 3.16: Simulated reflection coefficients for various gap widths.

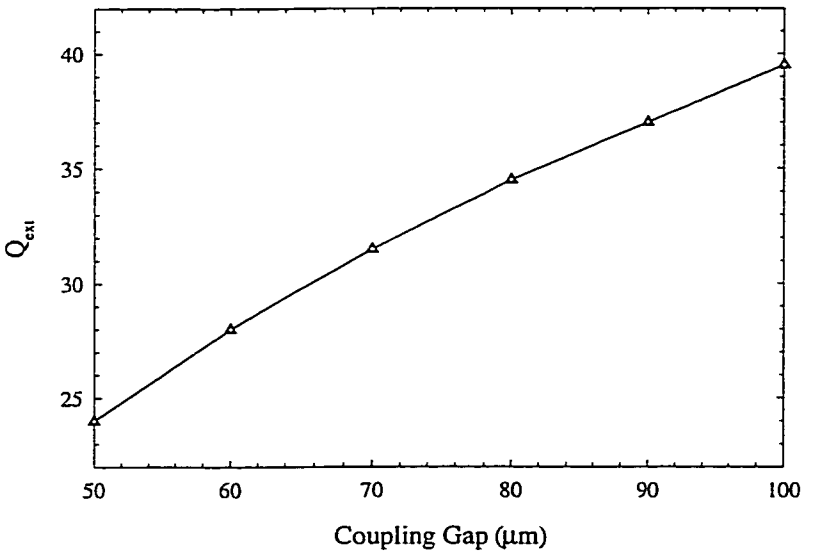


Figure 3.17: Extracted values of external Q's for a range of gap widths.

3.3.3 4-Pole Filter Measurements

The filter was fabricated in the same manner as the planar resonators in Chapter 2. The gold thickness was 2 μm of electroplated gold. An air-bridge was added at the edge of the CPW feed structure just before the transition to microstrip on membrane. The filter response was measured with an HP8510C network analyzer calibrated using a a TRL calibration method [27], [32] with 150 μm pitch coplanar Picoprobes[2]. On all measurements, the system was calibrated with a reference plane located 500 μm from the silicon-to-membrane transition in order to take into account the discontinuity of the transition. The measured results are compared with the simulated results in Fig. 3.18. The simulated results were done using IE3D [34], a commercially available moment method analysis tool. The simulation was done by simulating the full filter structure including the dielectric membrane. Both the simulated and measured results are in very good agreement until the -30 dB level for the insertion loss. At this point parasitic coupling along the membrane cavity walls occurs, limiting the filter performance. This will be addressed in the following chapter. The measured center frequency is 27.92 GHz and is within 0.3% of the designed value of 28.00 GHz. The simulated and measured results are also in very good agreement with initial design parameters of a 4-pole, 5.5% filter with a theoretical insertion loss of 0.75 dB. The actual measured passband is 6% with an insertion loss of 0.85 dB. The designed ripple should have produced a filter with a maximum return loss of -16.4 dB in the passband. The simulated return loss has a maximum of -13 dB in between the highest pole of the filter. This is due to a slight shifting of one of the poles from its designed value, and is apparent from the return loss which only shows a 3-pole response. This means that one of the poles shifted into the location of an adjacent pole creating a double pole. This same effect is also present in the measured results, but at the lower end of the passband. This discrepancy may be due to a small

[2]Picoprobe is a product of GGB Industries, Inc., Naples, FL.

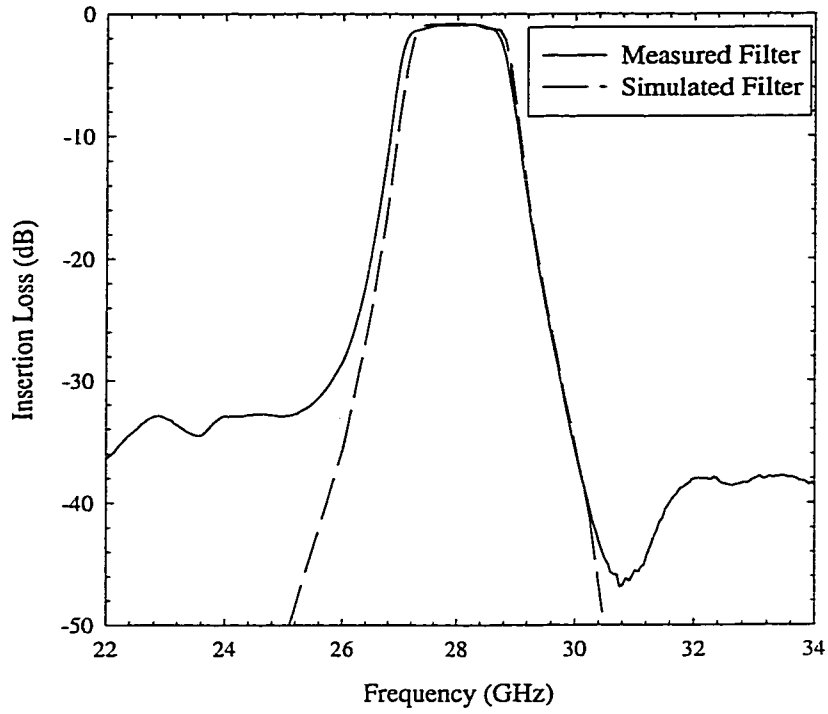
change in the inductance of the transition network.

The filter was also measured under high power. A 28 GHz signal was generated with an HP83554A millimeter-wave source module. This signal was then amplified with a Hughes 8001H traveling wave tube amplifier (TWTA) and used as the input to the filter. The incident total power on the filter was approximately 0.7 W with no apparent increase in insertion loss or filter failure. One can safely say that such filters can handle 1-2 W of power levels, but more testing is needed to determine the maximum allowable values. It is evident that the maximum power will depend on the gold thickness, resonator width, ground-plane height, and the filter insertion loss.

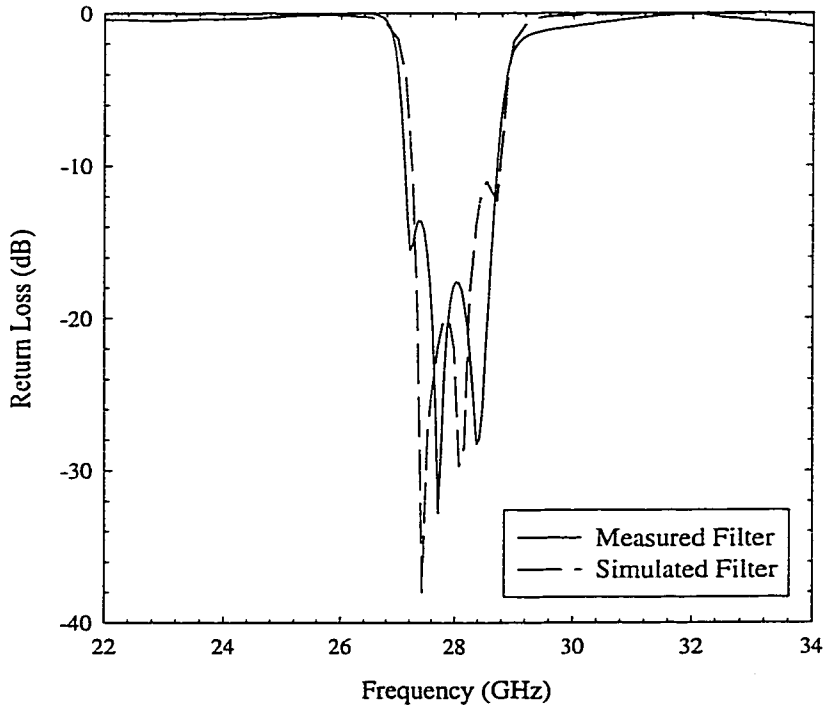
As a comparison, the same structure was simulated in HP EESOF Libra [50] using the empirically based models MLIN (based on [51]) for the microstrip lines and MGAP (based on [52]) for capacitive gaps. Included in the simulation was a shielding cover and sidewalls. The Libra simulation greatly disagrees with the full-wave simulation and the measured results (Fig. 3.19). It is evident that the Libra models cannot be used for this type of narrowband filter.

3.4 Conclusions

A filter design techniques has been demonstrated that allows for a direct conversion from the low-pass filter prototype to a coupled resonator filter with arbitrary resonators and input/output load impedances. This allows for an optimization of the resonator independent of the filter design. The coupling scheme of the resonators is then examined and mapped directly to the low-pass prototype. This breaks the filter design down into small steps allowing for a fast design by minimizing the total amount of full-wave analysis. To demonstrate this technique, a 4-pole filter was designed and fabricated. The measured and simulated results are in very good agreement with the low-pass prototype filter.



(a)



(b)

Figure 3.18: Measured results of 4-pole filter.

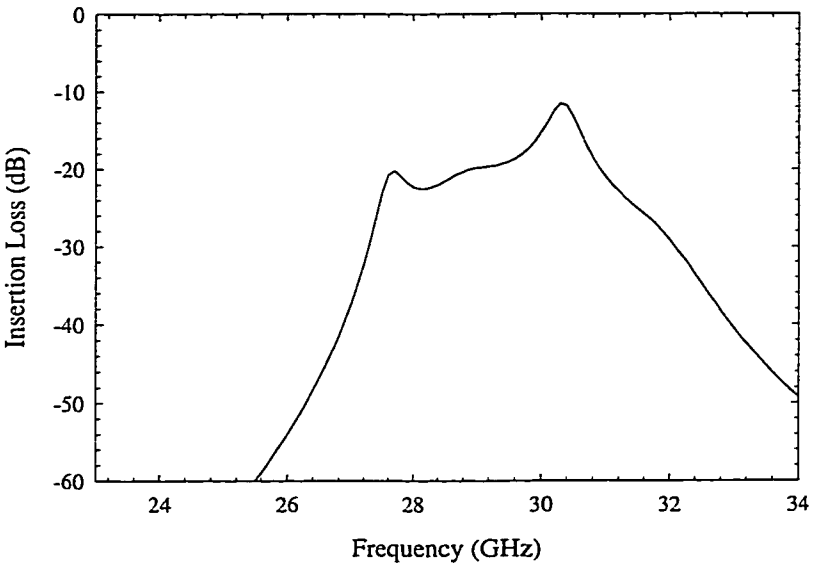


Figure 3.19: Simulation of the 4-pole filter in Libra using MLIN and MGAP microstrip models.

CHAPTER 4

LOW-LOSS, HIGH-ISOLATION PLANAR DIPLEXER

4.1 Introduction

The purpose of the work presented in this chapter is to develop a diplexer that not only has very low insertion loss, but to have a very high level of isolation between transmit and receive channels. Conventional diplexers consist of machined waveguide cavities having a very high quality factor allowing for low insertion loss for a many pole filter. Planar resonators traditionally do not have a high enough quality factor resulting in poor insertion loss. Further, planar resonators tend to couple energy into the substrate in the form of substrate modes limiting the amount of filter rejection to 30-40 dB depending on the substrate dielectric constant and thickness. By applying micromachining techniques, the dielectric constant of the substrate is reduced eliminating the formation of substrate modes. However, micromachining a cavity under a circuit produces another effect in that cavity modes can form greatly limiting the filter performance. Even if the cavity mode cutoff frequency is well above the frequency of interest, coupling due to evanescent modes can limit the isolation [47].

This chapter describes the design and measurements of a micromachined, planar

K-band diplexer. The diplexer is based on the membrane supported, capacitively coupled bandpass filter presented in the previous chapter. One drawback of the 4-pole filter discussed in Chapter 3 was the out-of-band rejection. By altering the geometry of the filter channel, this is greatly improved to proved much higher isolation. The filter design technique from the previous chapter is then applied to the diplexer. The common port (antenna port for a full-duplex wireless system) is then examined for the case of coupling to two resonators. The measured response of the diplexer is then compared with the simulated data.

4.2 Design

The diplexer topology is based on a membrane supported, capacitively coupled bandpass filter demonstrated by Blondy et al. [43] as shown in Figure 4.1a. The resonators are $\lambda/2$ lengths of capacitively end-coupled microstrip transmission lines. The feedlines are coplanar waveguide lines on silicon with an abrupt transition to microstrip at the edge of the membrane. The ground plane wafer is etched to conform to the membrane area and has small "mouseholes" over the CPW lines. The edge of the mouseholes contact the CPW ground planes, and act as a via from the CPW ground plane to the microstrip ground plane at the silicon/membrane interface. Due to the anisotropic etching properties of the etchant used for fabrication, these ground vias are 1 mm from the signal conductor and add inductance (0.1 nH) in the CPW-to-microstrip ground plane transition. Immediately following this transition, an edge coupled $\lambda/4$ section of microstrip transmission line is used. The $\lambda/4$ section reduces the effects of the series inductance and the abrupt change in permittivity in the silicon to air interface. It also acts as a transformer coupling to the filter and sets the external Q.

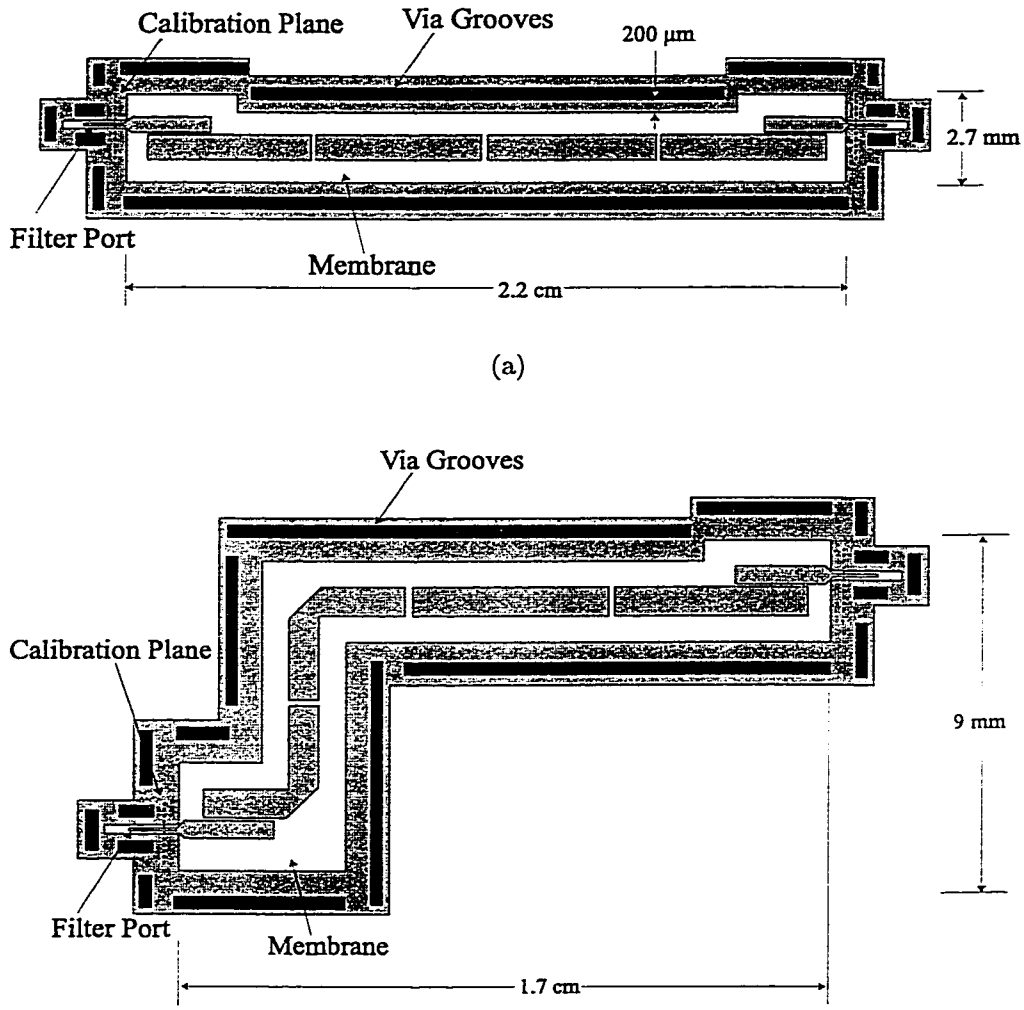
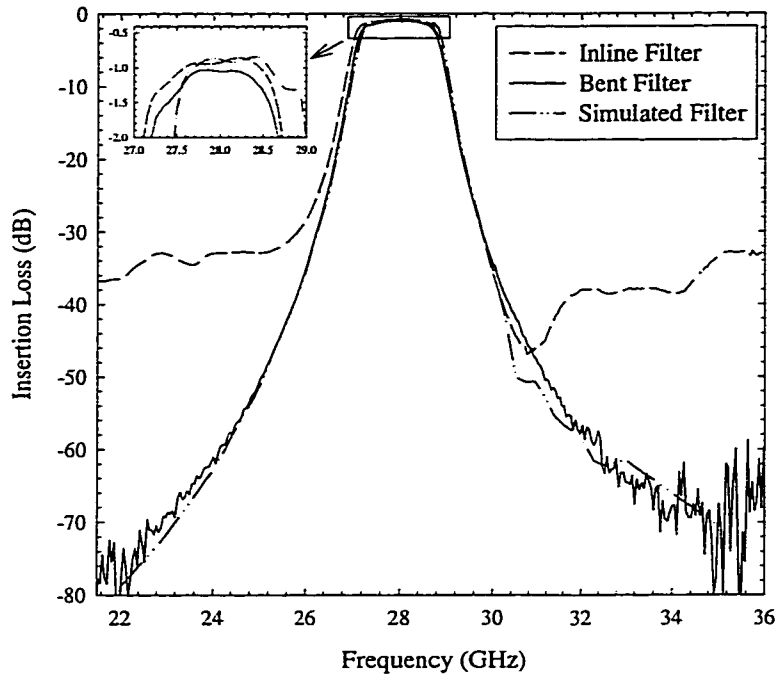


Figure 4.1: Capacitively coupled membrane filter (a) inline and bent (b) bent filter method.

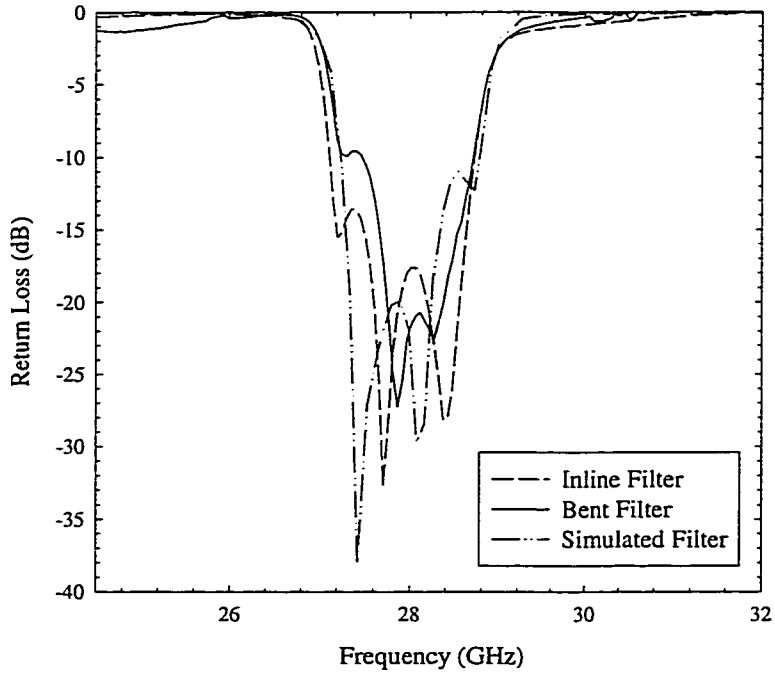
4.2.1 Improvement in Filter Out-of-Band Rejection

A disadvantage of the filter shown in figure 4.1a is that the out-of-band rejection is very susceptible to degradation by parasitic modes in the micromachined structure. These result in an increase in coupling due to the evanescent modes in the cavity structure and also in propagating modes in the silicon wafer surrounding the cavity. This is greatly improved by bending the filter structure and altering the arrangement of the via grooves to disturb any possible modes that are formed (Fig. 4.1b). The 4-pole filter depicted in Fig. 4.1a is identical to the filter presented in the previous chapter. The design of the bent filter in Fig. 4.1b is identical to the inline filter except that the first and second resonator are bent as well as the micromachined channel. Both filters use 800μm wide resonators with a gold thickness of 2 μm on a 250 μm high ground plane. The details of the design of the coupling gaps is given in section 3.3. The lengths of the bent resonators are adjusted to compensate for the bends using IE3D [34], a $2\frac{1}{2}$D commercially available software package based on the method of moments. The length of the 28 GHz straight resonator is found to be 5 mm, while the bent resonator consists of two 2.2 mm lines connected to an optimally mitered corner.

Figure 4.2 shows a comparison of measured results for the inline filter from fig. 4.1a, the bent filter from fig. 4.1b, and a full-wave simulation for a 4-pole capacitively coupled filter with 5.5% bandwidth a center frequency of 28.0 GHz. The measured results are calibrated to the reference plane 500 μm from the membrane (Fig. 4.1) using a TRL calibration method [32] and include the CPW-to-microstrip transition. The simulated results were done using IE3D. The simulation conditions neglect the effects of the CPW to microstrip transition and assume a 1.4 μm thick dielectric membrane (ϵ_R=5) on a 250 μm air layer with an 800 μm high shielding cover which is infinite in extent. The resonators are 800 μm wide with a measured Q of 460 which agrees very well with a simulated value of 450 using SIMIAN [39], a



(a)



(b)

Figure 4.2: Comparison of the measured inline and bent 4-pole filters, and the simulated inline 4-pole filter (a) insertion loss and (b) return loss.

surface ribbon method program [38]. The simulation is done for an inline filter. The simulation for the bent filter is not shown, but has an identical response to the bent filter simulation. The measured insertion loss is 0.85 dB and 1.00 dB for the inline, and bent filters, respectively, which is close to the simulated loss of 0.75 dB. Note that the bent topology has a large improvement in out-of-band rejection compared to the inline filter (better than -75 dB for the bent as compared to -35 dB for the inline filter) with only a 0.15 dB increase in insertion loss due to the mitered resonator bends. The -80 to -75 dB filter rejection is competitive with "stand-alone" filters used in multi-substrate packages.

Similarly, a 3-pole filter was designed and fabricated to observe if the improvement in the out-of-band rejection will be maintained for "shorter" filters. The 3-pole filter is based on the same topology as the 4-pole design, but with a center frequency of 31.75 GHz. The designed relative bandwidth is 5.5% with a ripple of 0.1 dB. The design method is identical to that of the 4-pole filter. The 3-pole filter was fabricated on the same wafer as the 4-pole filter using the same fabrication steps. The measured passband response of the 3-pole filter showed an increase in passband ripple to 0.5 dB (Fig. 4.4). This is characteristic of a mismatch in the input/output coupling that may be due to inaccuracy of modeling or fabricating the transition. The bandwidth and filter roll-off of the bent filter agreed very well with the simulated filter response. However, the inline 3-pole filter bandwidth increased slightly, and the out-of-band rejection was substantially worse. Also note, there appears to be a transmission zero on the low side of the passband at 28.5 GHz. This is characteristic of a filter with negative feedback due to non-adjacent resonator coupling.

4.2.2 Microwave Modeling

A microwave model (12×) of the 4-pole, inline filter was constructed to analyze the coupling mechanism for the leakage in the out-of-band rejection. The channel of

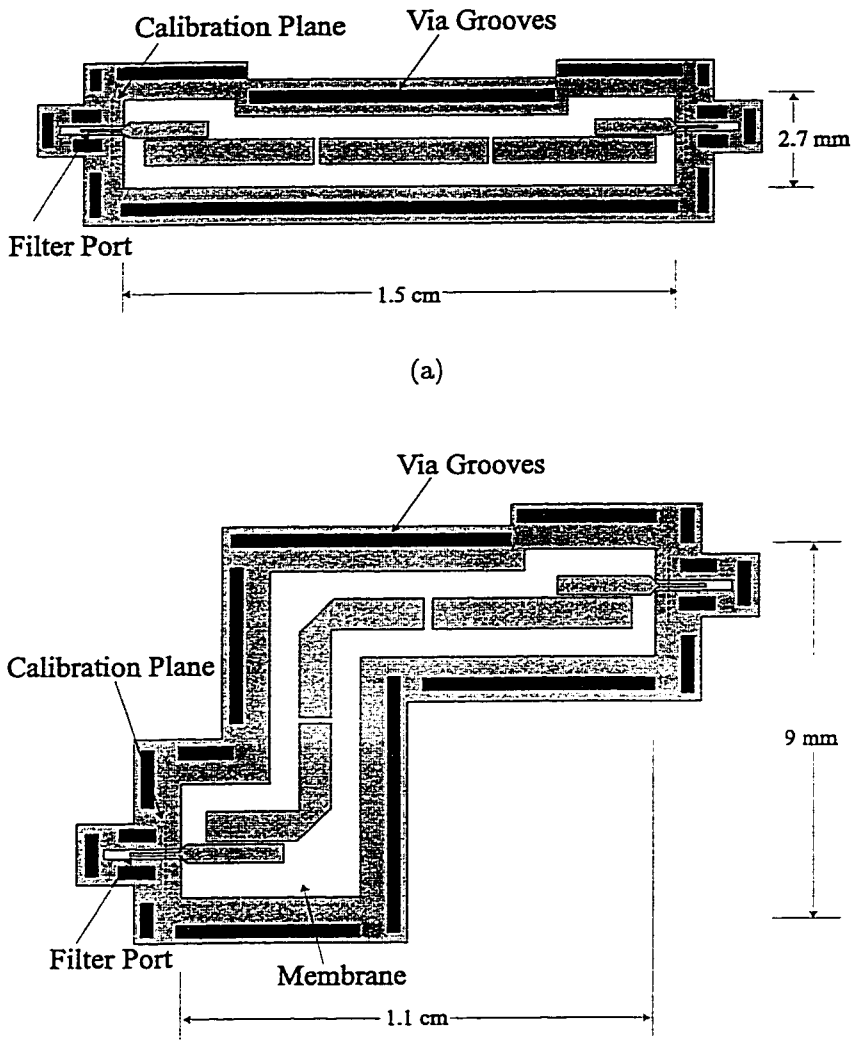
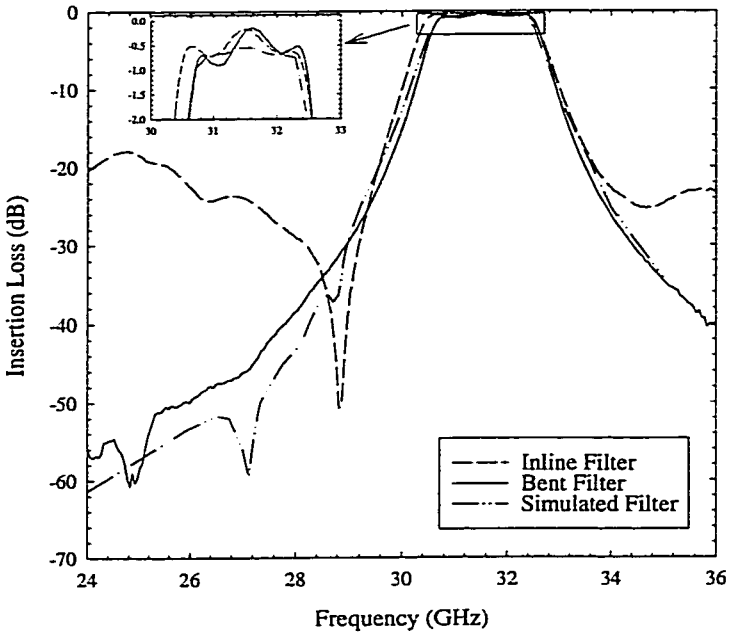
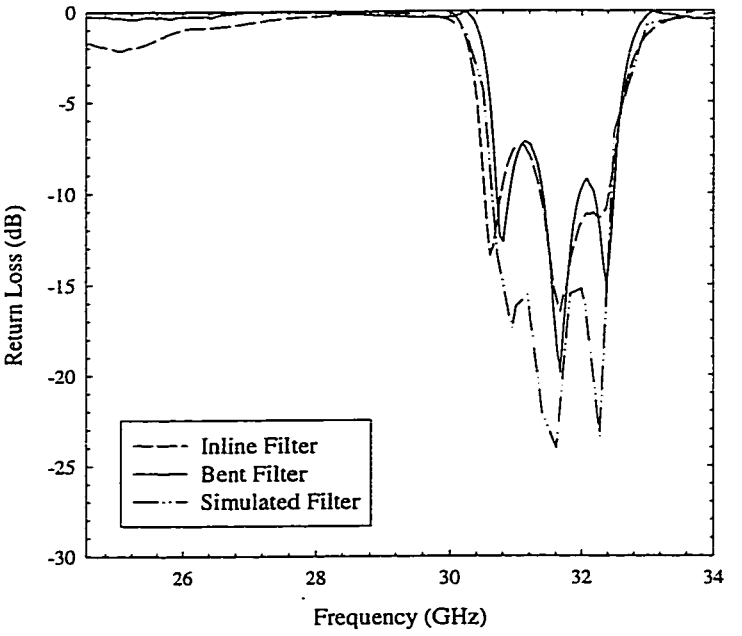


Figure 4.3: Capacitively coupled membrane filter (a) inline and (b) bent filter method.



(a)



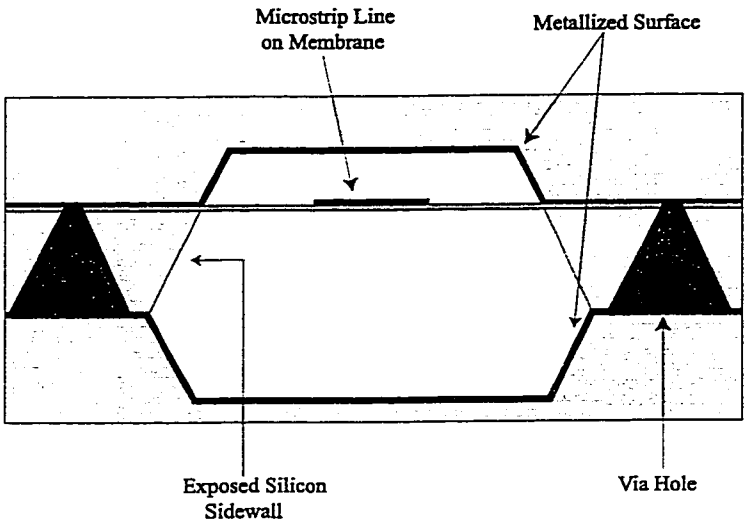
(b)

Figure 4.4: Comparison of the measured inline and bent 3-pole filter, and simulated inline 3-pole filter (a) insertion loss and (b) return loss.

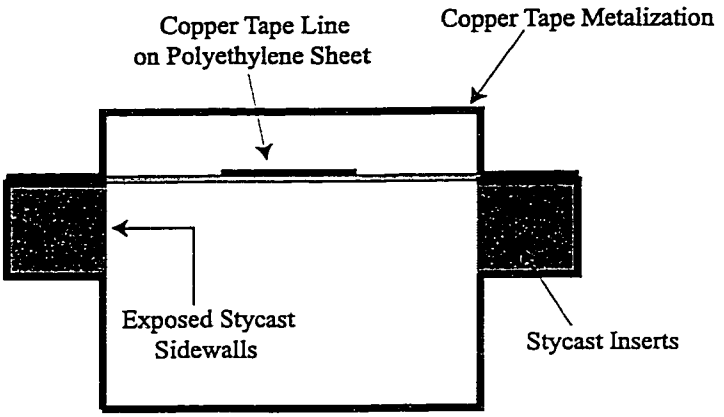
the filter was milled out of a block of plastic that was covered with copper tape to simulated the gold shielding cavity and via holes. Stycast[1] (ϵ_r=12) was then inserted to simulate the thin ring of silicon in the middle wafer between the filter channel and the via grooves. The slanted silicon sidewalls are approximated as vertical walls in the microwave model (Fig. 4.5). The filter conductor pattern was constructed from copper tape suspended on a 152 μm thick polyethylene sheet to simulate the resonators on membrane. The microwave model of the filter was then measured using an HP8720B with a coaxial SOLT calibration. The out-of-band rejection for the microwave model filter was limited to about approximately -40 dB. To investigate the effects of the Stycast inserts on the out-of-band rejection, portions of the exposed Stycast sidewalls were covered with copper tape. If an entire side of the filter with the bends (top edge of the filter in Fig. 4.6) is covered in copper tape, there was no improvement in the out-of-band rejection. However, if the straight side of the filter (bottom edge of the filter in Fig. 4.6) is coated, there is substantial improvement depending on how much copper tape is used. For increasing amounts of copper tape centered on the straight edge of the filter, the out-of-band rejection increases. Fig. 4.7 shows the improvement in the filter response for increasing amounts of copper tape covering the Stycast. The tape is centered and the maximum amount plotted (10 inches), spans the length of the filter.

The results from the microwave model suggest that the straight dielectric wall allows some power to leak from the input to output bypassing the filter in out-of-band region. Copper tape was effective at suppressing this leakage. However, the leakage was not reduced when copper tape was added to the side of the filter that had the two bends in it, suggesting that the bends alone suppress the leakage. This is consistent with the millimeter-wave measurements made on both the 3 and 4-pole filters presented above. In conclusion, the out-of-band rejection is greatly improved

[1]Stycast HiK is a product of Emerson and Cumings, Inc., Canton, MA.



(a)



(b)

Figure 4.5: (a) Actual cross section of millimeter-wave filter and (b) cross section of the 12× microwave model. Note that the exposed Stycast was not metalized to simulate the actual micromachined circuit.

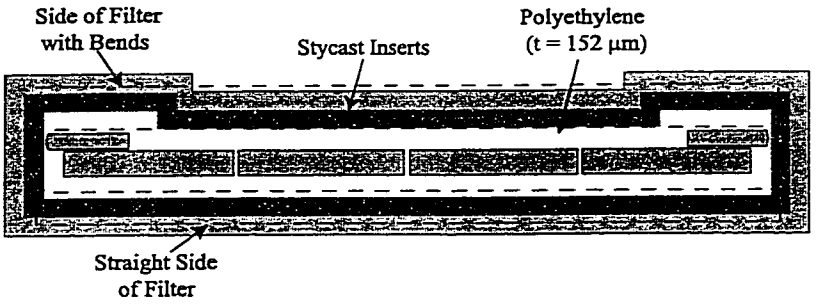


Figure 4.6: Top view of the 2.3 GHz microwave model filter structure.

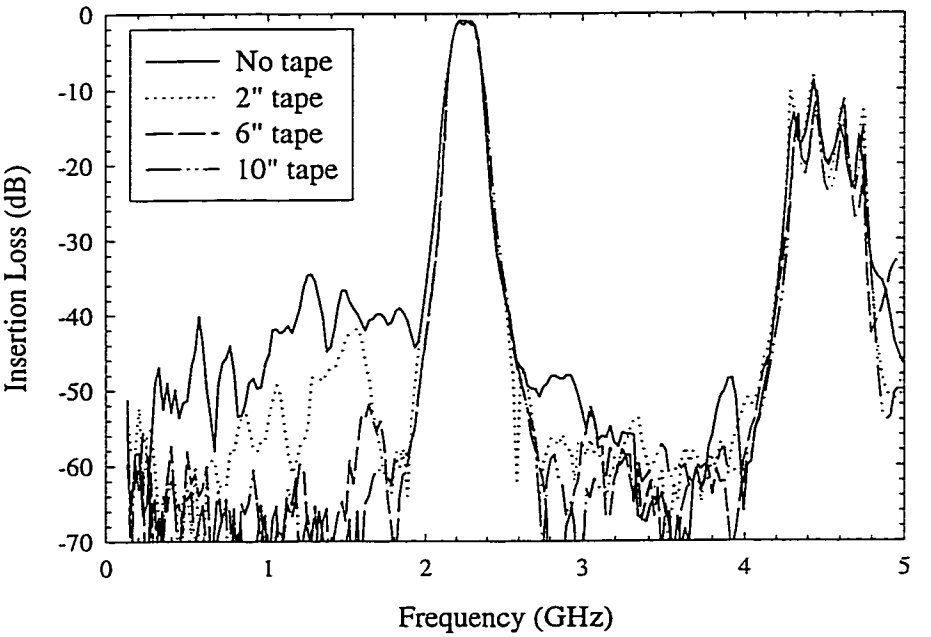


Figure 4.7: Measured response of the microwave model filter with varying amounts of copper tape on the straight portion of the filter. The 2", 6", and 10" values are referenced to copper tape coverage centered at the filter midpoint.

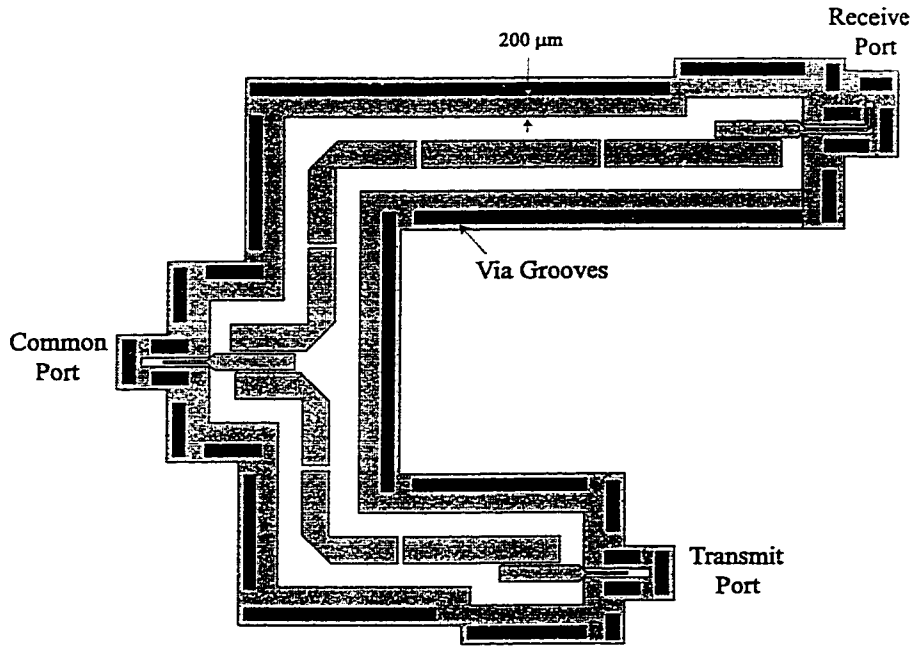


Figure 4.8: Integrated k-band diplexer topology.

by either bending the structure, or applying a metal coat to the silicon sidewall within the filter channel (this requires a shadow mask and additional fabrication steps).

4.2.3 Diplexer Design Details

The diplexer consists of two bent capacitively coupled bandpass filters with one port shared between the filters (Fig. 4.8). The two channels for the diplexer were chosen to correspond roughly to the commercial Local Multipoint Distribution System (LMDS). The receive band filter is designed using a 4-pole Chebyshev prototype with a center frequency of 28.2 GHz, relative bandwidth of 5.5%, and a ripple of 0.1 dB. The transmit band filter is a 3-pole Chebyshev filter with a center frequency of 31.75 GHz, relative bandwidth of 5.5%, and a ripple of 0.1 dB.

The resonators used in this paper consist of 800 μm wide lines with a ground plane height of 250 μm (etch depth of the top wafer) and a shielding cavity height of 800 μm (400 μm for the thickness of the middle wafer and 400 μm for the etch depth

of the bottom shielding wafer). The distance from the edge of the conductor to the sidewall of the micromachined channel is 700 μm. The conductors are 2 μm thick electroplated gold. This results in a microstrip line with a characteristic impedance of 62 Ω. A half-wavelength resonator constructed from this geometry has a measured unloaded quality factor of 460 at 29 GHz with a corresponding attenuation coefficient of 0.057 dB/cm [53].

The design of the inter-resonator couplings follows the standard procedure as presented in Chapter 3. The inter-resonator couplings are calculated using Sonnet EM [49], a commercially available method of moments package. The effects of the micromachined sidewalls are modeled using a perfect conducting vertical wall. The coupling coefficients and associated end gaps are given in Table 4.1.

Table 4.1: Summary of Inter-Resonator Couplings

	Receive Band		Transmit Band	
i	$k_{i,i+1}$	$g_{i,i+1}$	$k_{i,i+1}$	$g_{i,i+1}$
1	0.042	140 μm	0.034	160 μm
2	0.033	190 μm	0.034	160 μm
3	0.042	140 μm		

The output coupling (non-common port of the two filters) was set by the required external Q as determined by the low frequency prototype. The receive and transmit band filters have an external Q of 22 and 34, respectively. This is implemented by a section of asymmetric coupled microstrip line, followed by a short section of line and the transition from microstrip-on-membrane to CPW-on-silicon. The microstrip section of the structure was simulated with Sonnet EM [49] and the S-parameters were then ported to HP EESOF Libra [50] where an added series inductance (100 pH) and a 350 μm section of 34 Ω CPW transmission line on silicon are used to model the effects of the transition. The length of the 500 μm wide feedline on membrane, and the length and gap of coupled section, were then optimized using combination of Sonnet EM and Libra. For the receive (transmit) band filter, the length of the feed

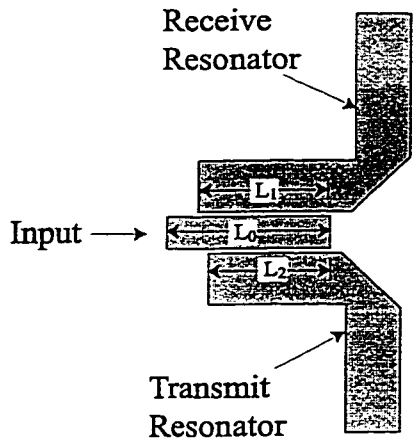


Figure 4.9: Coupling structure of the common port of the diplexer.

line is 2500 μm (2350 μm) with a coupled section of 1900 μm (1700 μm) long coupling gap of 60 μm (70 μm). These dimensions set the external Q of the filter *including* the effects of the transition.

The coupling structure of the common port of the diplexer is a three-line coupled microstrip geometry (Fig. 4.9). As with the other ports, the feed line is 500 μm wide. However, since there are two resonators present that are resonant at different frequencies, there is an added reactance term from the off-resonant resonator. The amount of added reactance is determined by the separation of the center frequencies and the external Q of each resonator. If the external Q is high enough and the resonances are far apart, then each resonator presents a very high shunt reactance at the resonance of the other resonator having little effect on the other resonator. However, for low values of external Q's (22 and 34) and close center frequencies (28.2 GHz and 31.75 GHz) as with this diplexer, the reactance of the off-resonant resonator has a strong effect on the performance of the other resonator. The shunt reactance of the off-resonant resonator adds to the shunt reactance of the other resonator, shifting the resonator center frequency. For a filter application, this can move a pole out of location increasing the bandwidth and mismatch, and degrading the out-of-band

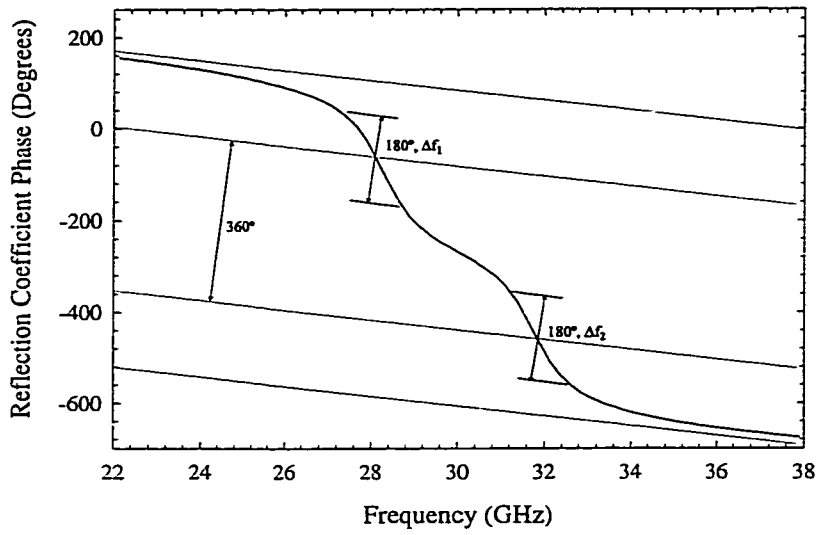


Figure 4.10: Coupling structure of the common port of the diplexer.

rejection.

In order to set the external Q correctly for each filter, the reactance from the rejection of one filter is compensated by subtracting an equal reactance from the other filter in the passband. The external Q is initially set for each resonator without the other resonator present as in the case of the individual ports discussed above. This takes into account the effect of the transition inductance and a short section of CPW line on silicon. The phases for each port were then compensated by extending the length of the feed line (L_0 in Fig. 4.9) to 2375 μm, increasing the length of the coupling section of the receive filter, L_1, to 1950 μm, and decreasing the length of the coupled section for the transmit filter, L_2, to 1650 μm. The coupling gap remained at 60 μm and 70 μm for the receive and transmit filters, respectively. This results in a net phase of 0° at each resonance. The phase of the simulated reflection coefficient (microstrip simulation in Sonnet EM plus the circuit model for the transition using HP EESOF Libra) is shown in Fig. 4.10. With the phase of the feedlines deembedded out, the resonances are at 0° and 360° at the correct frequencies showing that the off-resonance shunt reactance is canceled out.

4.3 Integrated Diplexer Measurements

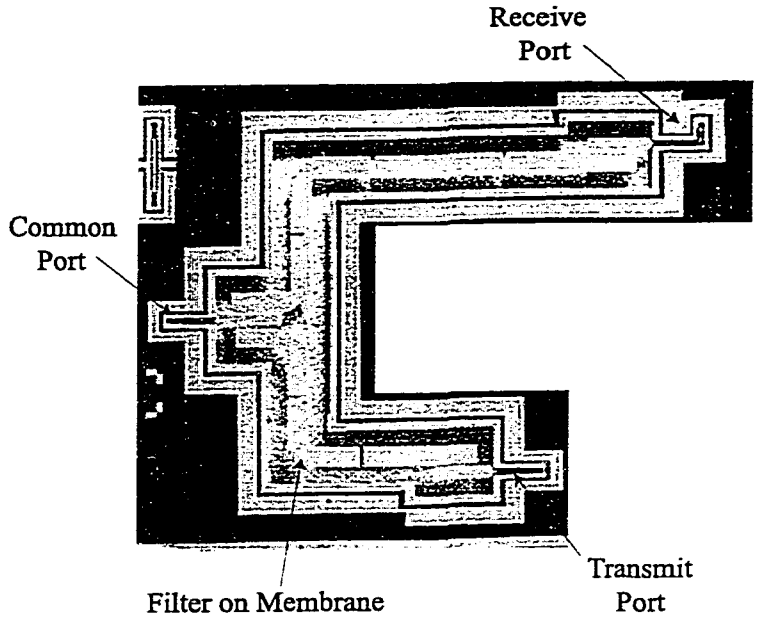
The micromachined diplexer was fabricated in silicon using a MMIC compatible process (Fig. 4.11). The diplexer outer dimensions are 1.5 cm × 1.6 cm and is only 1.4 mm thick. A considerable amount of the space in the outer dimension is not used for the actual diplexer and can fit other micromachined or planar circuitry (LNA, PA, biasing circuits, etc).

The diplexer response was measured with an HP8510C network analyzer calibrated using a a TRL calibration method [27] [32] with 150 μm pitch coplanar Picoprobes[2]. Since this is a two port measurement system, the third port was always terminated by another probe with an HP901C 2.4 mm Broadband Load. On all measurements, the system was calibrated with a reference plane located 500 μm from the silicon-to-membrane transition in order to take into account the discontinuity of the transition (see Fig. 4.1).

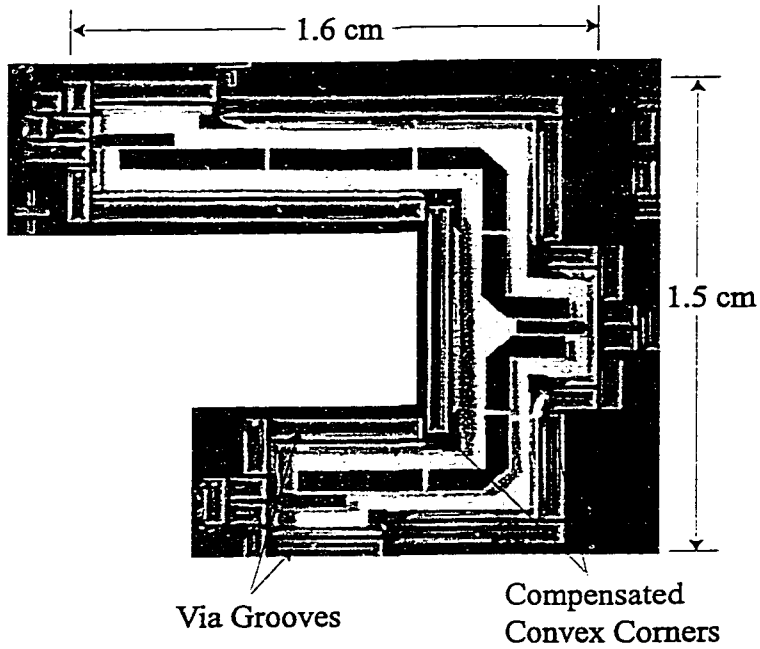
Fig. 4.13 shows the measured and simulated response of the receive band 4-pole filter. The simulated data was done using IE3D [34] for the entire diplexer assuming a substrate that is infinite in extent and does not model the CPW to microstrip transition. The transition effects were then added using HP EESOF Libra as discussed previously. The measured results are very close to the simulated data with a 1.2% shift in center frequency. The relative bandwidth increased from the designed value of 5.5% to 6.3%. The return loss increased from -15 dB to -10 dB. The increase in return loss is due to inaccuracy in setting the external Q of the filter. The measured insertion loss is 1.4 dB including all transition effects, the effects of the loss in the rejection of the transmit filter, the high return loss, and the 500 μm long CPW feedlines on silicon at both ports. This is in very good agreement the the simulated value of 0.9 dB which neglects these losses.

Fig. 4.14 shows the measured and simulated response of the transmit band 3-pole

[2]Picoprobe is a product of GGB Industries, Inc., Naples, FL.



(a)



(b)

Figure 4.11: Fabricated k-band diplexer (a) top view and (b) bottom view without the ground plane or shielding cavity.

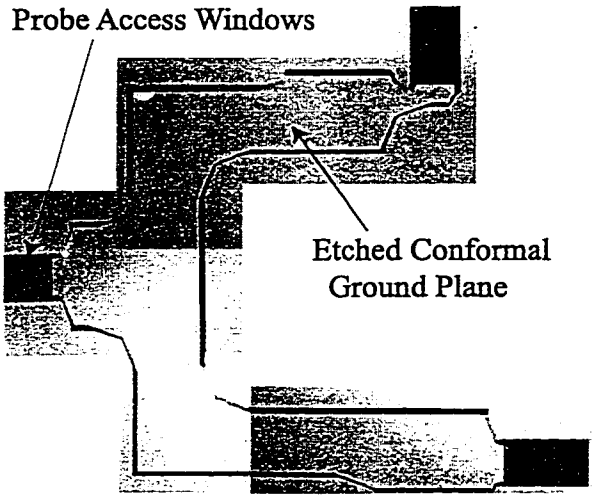


Figure 4.12: Fabricated diplexer conformal ground plane (bottom view).

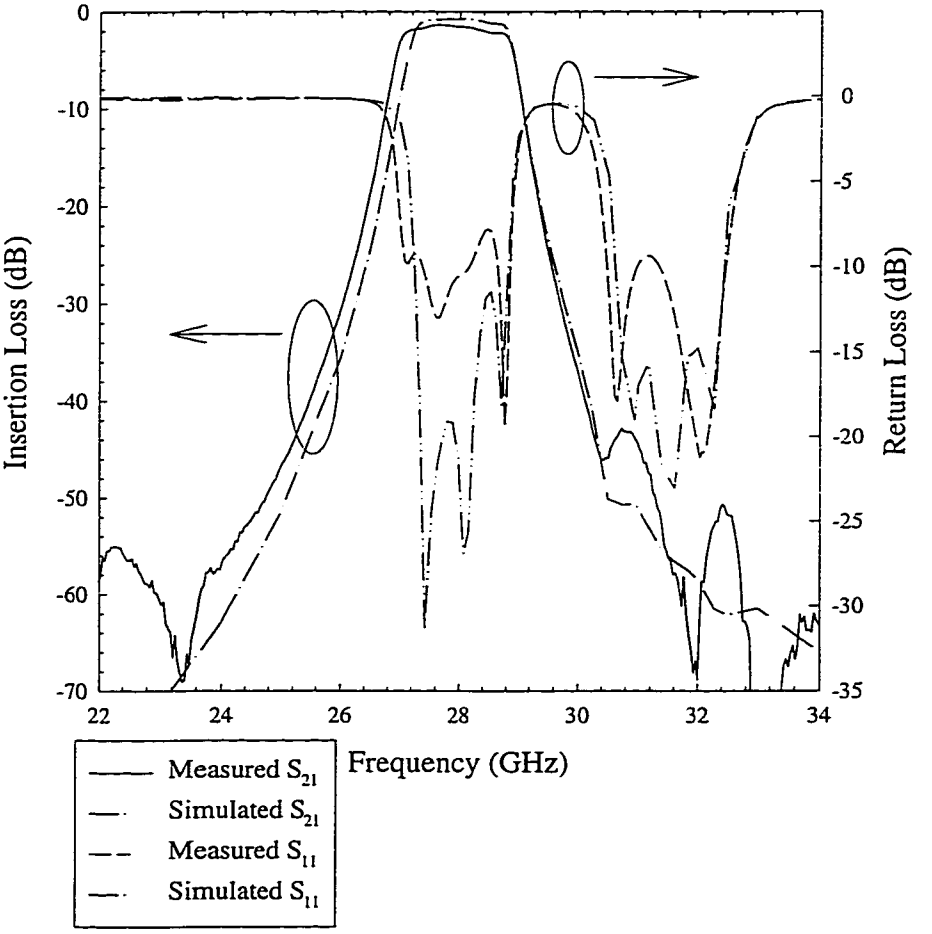


Figure 4.13: Measured and simulated receive channel response.

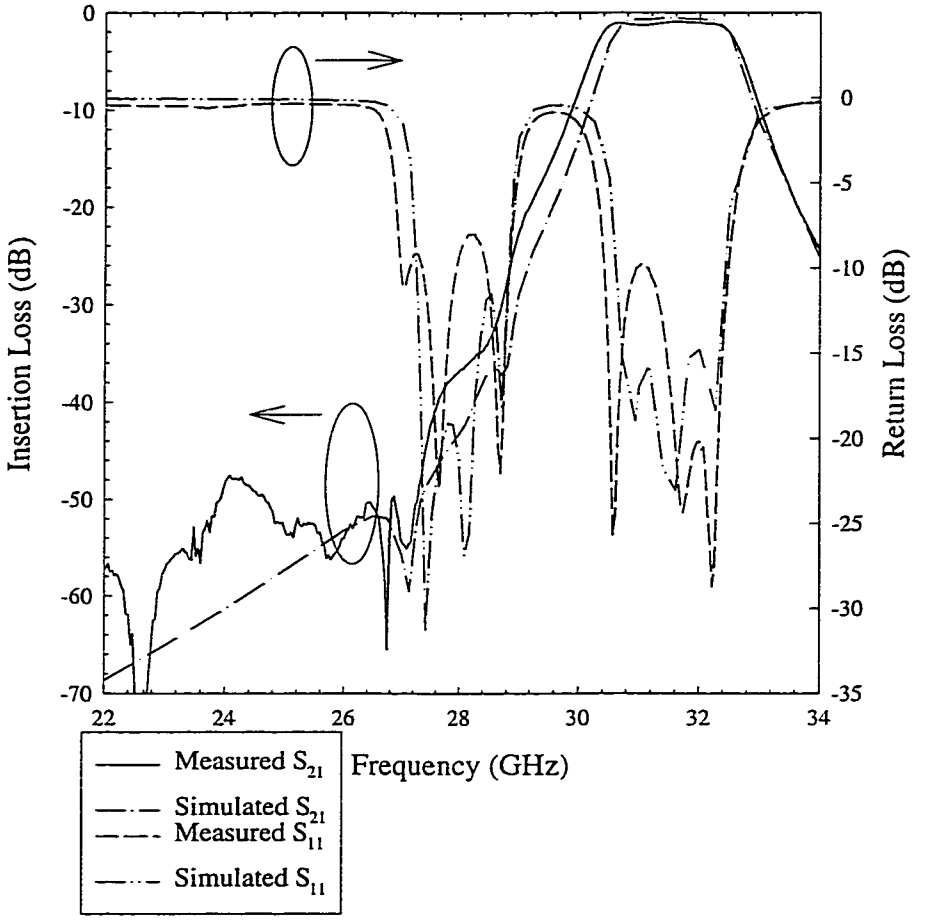


Figure 4.14: Transmit channel measured and simulated diplexer response.

filter. The simulated results are under the same conditions as those for the receive band filter. The measured and simulated results show a close agreement with a 1.6% shift in center frequency. However, the bandwidth increased to 7%. As with the receive band filter, the return loss increased to -10 dB. The measured insertion loss is only 0.9 dB compared to a simulated value of 0.65 dB. Again, this includes the added loss from the rejection of the receive filter, an increase in return loss, and the loss of the 500 μm long CPW feedlines on silicon at both ports.

The filter-to-filter isolation was measured by loading the common port with the broadband load (Fig 4.15). Again, the simulated results do not take into account the transition or finite width dielectric effects. The measured isolation is better than

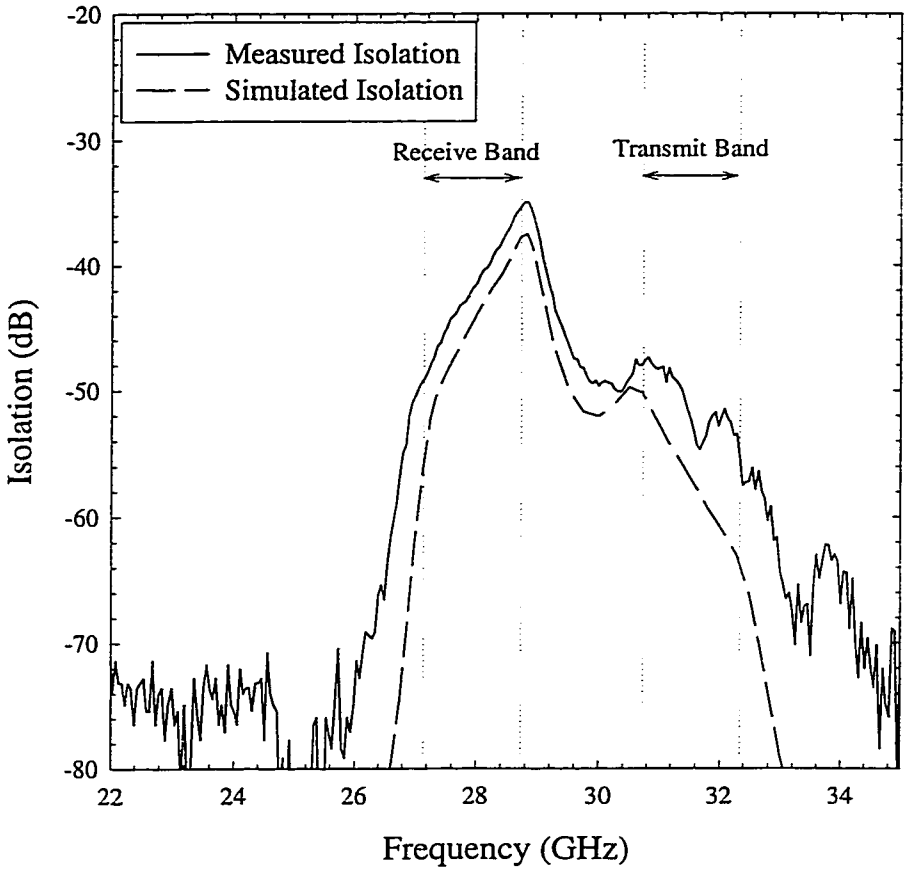


Figure 4.15: Measured and simulated transmit port to receive port isolation.

-35 dB across the receive band (-40 dB in the center of the band) and better than -50 dB in the transmit band. The measured agree very well with the simulated results with a slight degradation in isolation. The decrease in isolation is due to the increase of bandwidth of each of the individual filters. Notice that the leakage into the substrate is below -70 dB which is competitive with hybrid-cavity packaging techniques. All of the measured results are summarized in Fig. 4.16. Note that the filter-to-filter isolation closely follows the rejection of the individual filters.

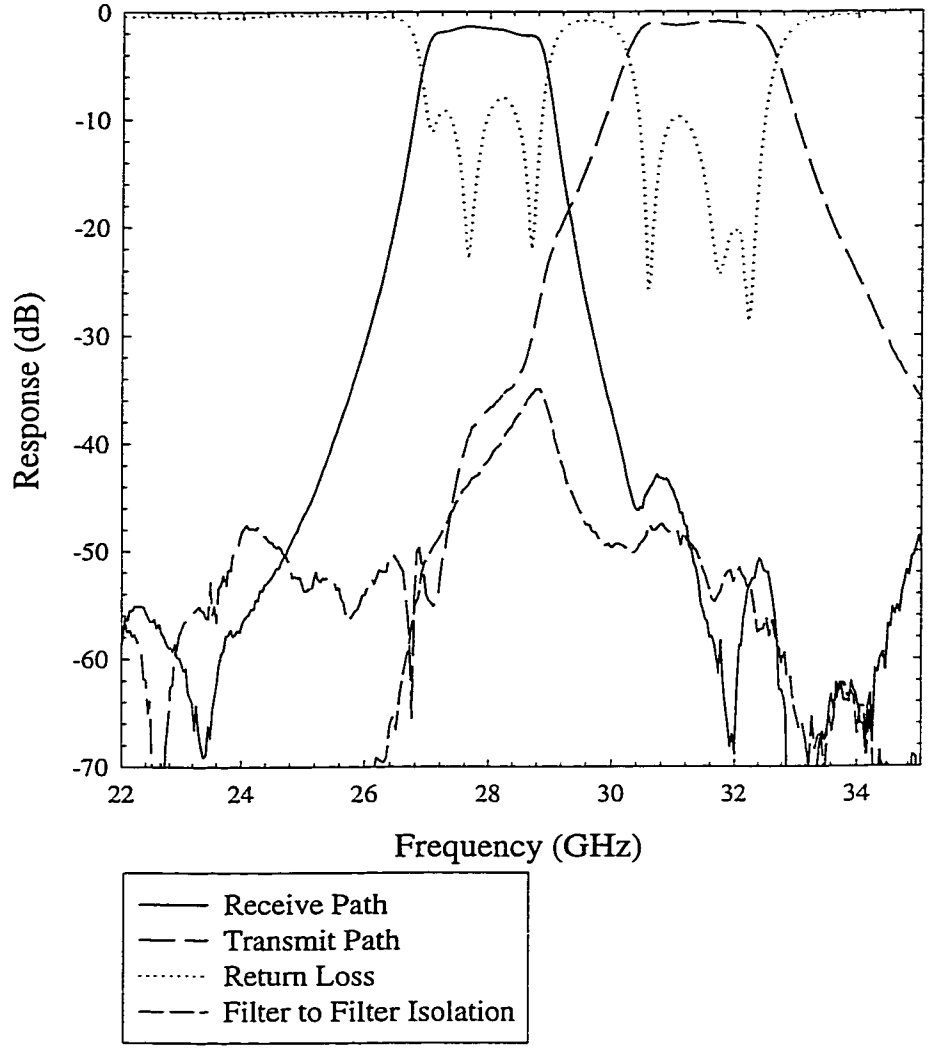


Figure 4.16: Summary of the measured K-band diplexer.

4.4 Conclusions

A planar Ka-band diplexer was designed and fabricated on a single substrate using micromachining techniques. The diplexer showed very low port-to-port insertion loss (1.4 dB and 0.9 dB for the 28 and 31 GHz bands, respectively) while still providing high isolation and agrees very well with the simulated results. The integrated diplexer is competitive with similar waveguide structures at a much smaller volume and production cost. Further, this topology allows for straightforward integration of other planar elements, such as LNA's and PA's on the same substrate, thereby eliminating the need for transitions.

CHAPTER 5

LOW-PHASE NOISE PLANAR OSCILLATORS

5.1 Introduction

High quality, low-phase noise oscillators are an integral part of microwave and millimeter-wave communication systems as a local oscillators. The stability and phase noise performance of an oscillator is strongly dependent on the quality factor of the loading circuit. The oscillator phase noise, using a linear approximation, is given by [15]:

$$N_{pn}(f_m) = \frac{FkT}{2P_{avs}}\left[1 + \left(\frac{1}{2Q_L}\right)^2\left(\frac{f_0}{f_m}\right)^2\right] \tag{5.1}$$

where F is the noise figure of the active circuit with the positive feedback removed, k is the Boltzman constant, T is the temperature, P_{avs} is the available signal power, Q_L is the resonator loaded Q_L, f_0 is the oscillation frequency, and f_m is the frequency offset from the carrier where the noise spectral power is measured. For frequencies near the carrier, the phase noise is a function of $1/Q_L^2$.

A popular design for dielectric resonator low-phase noise oscillators is the series feedback (Fig. 5.1a) [54]. This topology allows for a relatively straightforward design without a lot of nonlinear modeling and has demonstrated state-of-the-art oscillators at Ka-Band and U-Band [17], [18], [19]. However, dielectric resonators (DR) require

precise machining for fabrication and very careful placement of the dielectric puck for optimal resonator coupling. This often requires manual tuning of the DR for proper oscillator performance. The coupling structure is also implemented in microstrip form requiring thin substrates at millimeter-wave frequencies.

This chapter discusses one alternative method for building low-phase noise oscillators in an integrated, planar structure while maintaining the basic oscillator design of a DRO. Rather than using an external high-Q resonator, micromachining techniques are used to produce a micropackaged, air dielectric line with wide transverse dimensions resulting in high-Q resonators at millimeter-wave frequencies. Also, for comparison purposes, a non-micromachined oscillator is designed and fabricated in parallel with the micromachined case. The non-micromachined oscillator is designed in a similar method as the micromachined one, but the resonator is replaced with a CPW resonator designed to present a similar resonant impedance, but with a much lower quality factor.

The micromachining techniques used are based on the membrane supported suspended microstrip line presented in Chapter 2. While the unloaded quality factor of this type of resonator is less than that of a dielectric resonator (500-1500 at K-Band [42]), there are other advantages to using the micromachining technology. The resonator coupling is determined by the tolerances of optical lithography (1-2 μm maximum). Since this is a very repeatable process, there is no need for manual placement and tuning. Also, while the resonator is on suspended microstrip, the remaining part of the oscillator is based on coplanar waveguide technology eliminating the need for wafer thinning. It is the author's belief that the accuracy and repeatability of the coupling and resonant frequency for the micromachined case will allow for comparable values of loaded Q's at a lower material and fabrication cost.

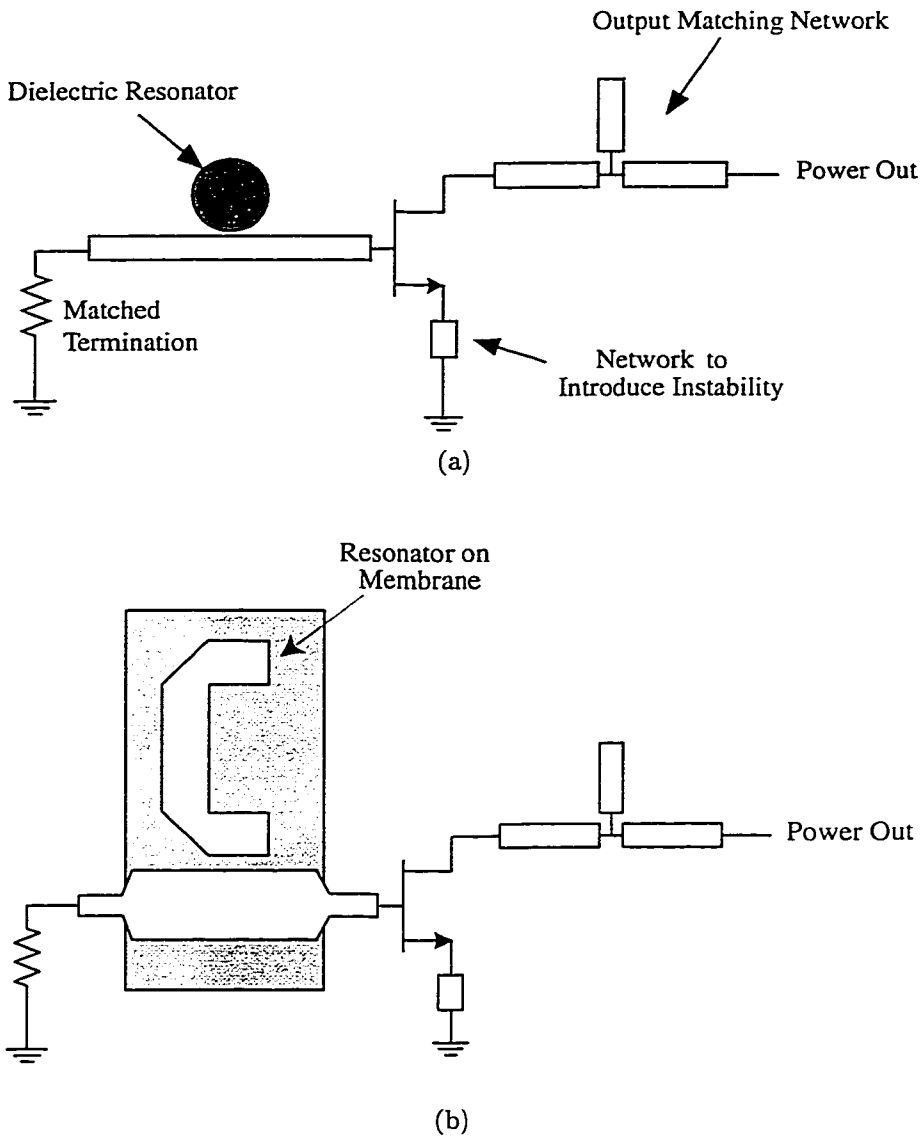


Figure 5.1: Series feedback (a) dielectric resonator oscillator, and (b) membrane supported microstrip topology.

5.2 Basic Oscillator Design Method

The design technique used for the oscillator is based on the reflection amplifier method [55], [56]. This method takes a 3-port transistor and loads two of the ports in a way that creates high instability at the point where oscillations are to occur. This loading reduces the problem to a one port network with negative resistance. The negative resistance is then matched for oscillation conditions. For the series feedback topology used in this chapter (Fig. 5.1), the problem is broken down into three main sections: (1) design of source feedback network, (2) design of the resonant feedback circuit, and (3) design of the matching network for oscillation conditions.

The transistor used is a commercially available GaAs HEMT (FHR20X)[1]. The device has a minimum noise figure of 1.5 dB at 28 GHz with an associated gain of 8 dB. A nonlinear model for this device was not available, so the design was based solely on the manufacturer supplied small signal S-parameter file. The S-parameter file was a two-port network that included the effects of the wirebonding of the chip HEMT to the carrier substrate. The two-port S-parameter matrix assumes the device is in a common source configuration. The naming conventions for the transistor ports follow the same conventions for an amplifier design [57] for a common source configuration. The input (or source) is treated as the gate of the device and the output (or load) is the drain of the HEMT. Since this is an oscillator and there is no input signal, the "input" will be terminated in a way that that reflects noise generated in the device to produce oscillations at the load.

5.2.1 Source Loading

The FHR20X is an unconditionally stable transistor at 28.7 GHz for any passive load. Therefore, the source of the device needs to be loaded in a way to make it

[1]The FHR20X GaAs HEMT is a product of Fujitsu Compound Semiconductor, Inc., San Jose, CA.

possible for instability at the output of the device (drain) under the passive loading of a resonator at the input. The first step is to change the two-port S-parameter matrix into an indefinite scattering matrix, and this can be done using HP EESOF Libra [50]. The indefinite scattering matrix allows for the ground port (device source terminal) to be undefined. This undefined port can then be loaded with stubs to increase instability.

The FHR20X is a dual source device. For the device to be balanced, both source terminals need to be loaded the same. To allow for a DC path for the bias current, shorted stubs are used. The stubs are 50 Ω CPW lines that are electrically short and act inductive at 28.7 GHz. All the 50 Ω CPW lines used have a center conductor width of 100 μm and a gap width of 65 μm on high-resistivity silicon. The input plane stability circles for the transistor are given for varying values of L_{stub} in Fig. 5.3. While the electrical length of the stubs increases linearly with frequency, the stability circles are not sensitive to frequency and shift very slightly over a 5 GHz bandwidth around 28.7 GHz due to a decreasing transistor gain as frequency increases.

When the edge-coupled resonator is away from resonance, it behaves close to a through line, and connects the gate of the transistor to the 50 Ω load. Therefore, at frequencies away from resonance, the center of the Smith chart must represent a stable impedance. When the resonator is resonating, the impedance seen at the beginning of the coupling scheme is the terminating impedance plus n^2R_{res} where n is the voltage coupling coefficient and R_{res} is the effective resistance of the resonator (Fig 5.4). This causes the reflection coefficient to swing from the center of the Smith chart (off resonance) to a higher impedance at resonance, and then back to the center. The amount of increase in impedance is determined by the amount of coupling. For very weak coupling ($n^2R < 50$), the reflection coefficient barely moves from the center of the Smith chart. For the over-coupled case ($n^2R > 225$), the reflection coefficient moves very far towards the edge of the Smith chart and the loaded quality factor

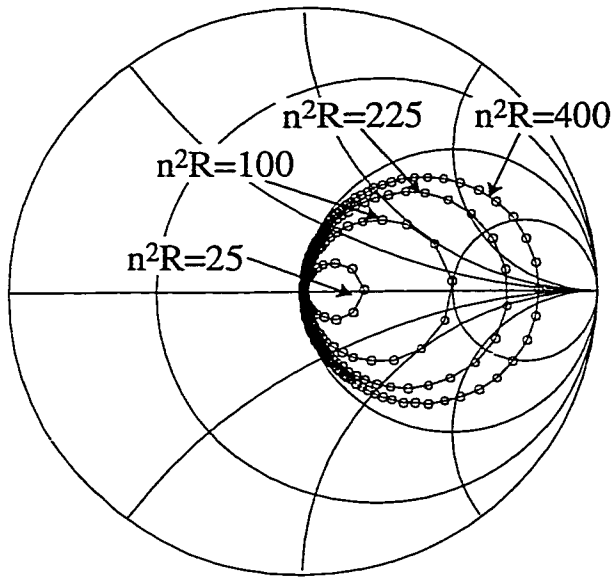


Figure 5.2: Simulated response for ideal resonator model with varying levels of coupling. The coupling is defined as the transformed resistance of the equivalent model for the resonator.

is greatly decreased (Fig. 5.2. Therefore, the loading at the source of the transistor needs to be such that the center (and small radius for a margin of error) of the Smith chart is stable and a region towards the outside of the Smith chart is unstable. The length is set at 650 μm allowing for some room for mismatch in the 50 Ω termination (including the CPW-on-silicon to membrane supported microstrip transition) while still maintaining a high loaded resonator quality factor.

5.2.2 Design of Resonant Feedback Circuit

Micromachined Resonator Case

The equivalent circuit model for the dielectric resonator is shown in Fig. 5.4. This is the same model as a microstrip through line with an edge-coupled $\lambda/2$ resonator adjacent to it. The suspended microstrip version of this is shown in Fig. 5.5a. This is identical to the resonator described in Chapter 2 in the bandstop resonator configuration. The input to the suspended microstrip section is coplanar waveguide (CPW)

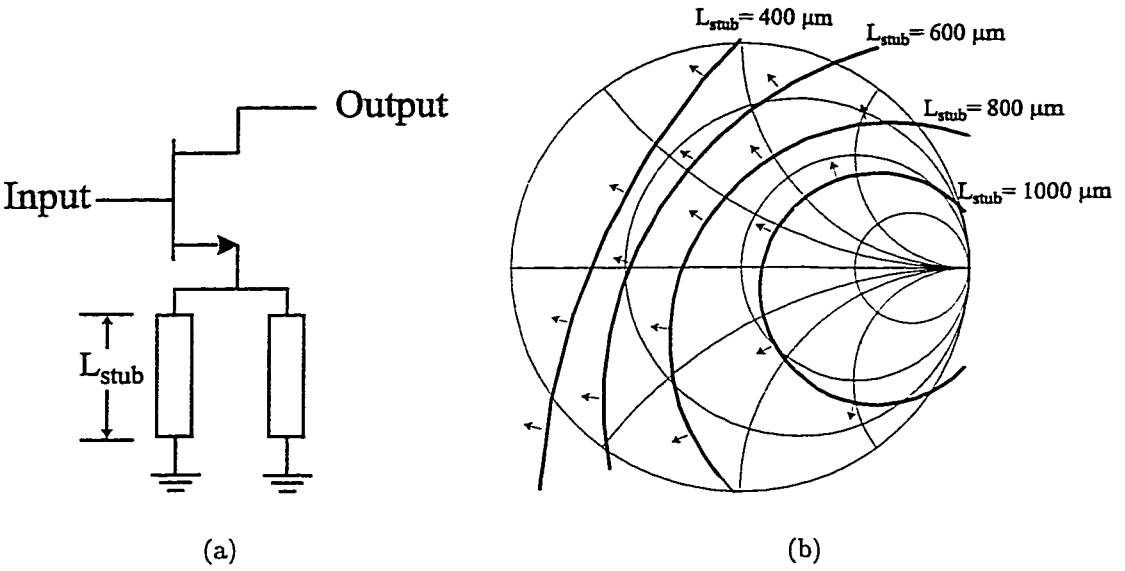


Figure 5.3: Input plane stability circles at 28.7 GHz for the FHR20X HEMT loaded at the source with 50 Ω CPW transmission lines on silicon of length L_{stub}. The arrows indicate the unstable regions for loading on the gate of the transistor.

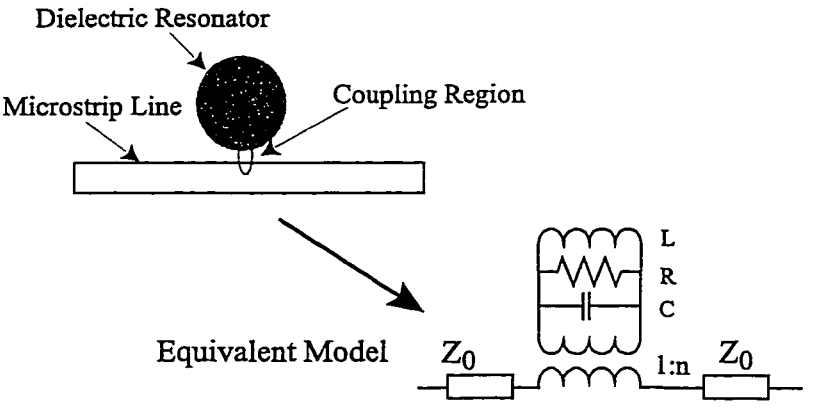
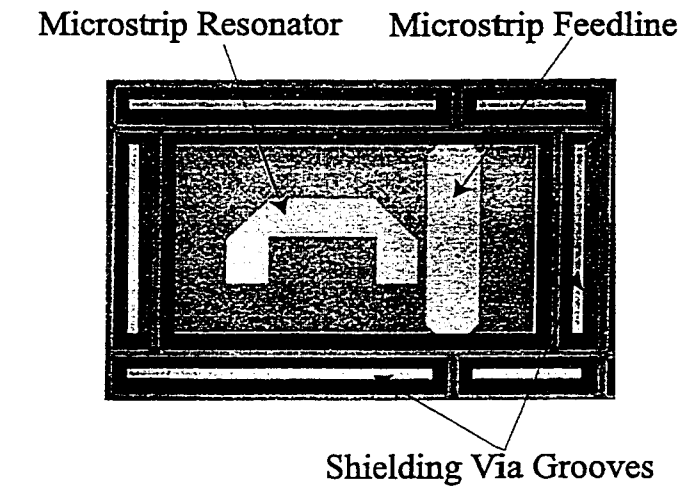
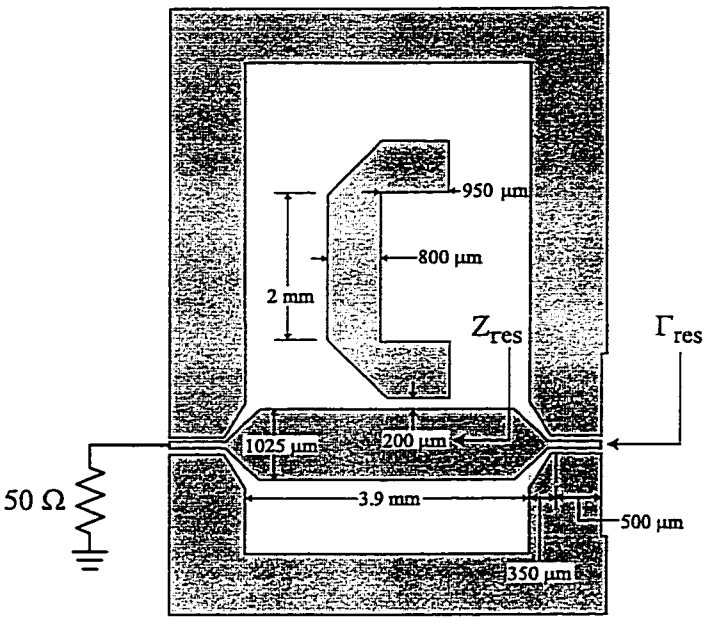


Figure 5.4: Dielectric resonator and its equivalent model.



(a)



(b)

Figure 5.5: Micromachined resonant input circuit of the oscillator (a) bottom view and (b) top view with dimensions.

on 400 μm thick, high-resistivity silicon (ρ=1000 Ω-cm). There is an abrupt change from the CPW on silicon to the membrane suspended microstrip. The microstrip ground plane (top wafer) is etched 250 μm and the distance from the microstrip to the shielding cover (middle and bottom wafers) is 800 μm. The microstrip through line is 1025 μm wide constructed from 2 μm thick electroplated gold forming a 50 Ω line. The CPW-to-microstrip transition has approximately 0.1 nH of series inductance from the CPW ground to microstrip ground plane connection. This causes some reflection and a standing wave on the through line. To reduce the effects of the inductance, the length of the line is adjusted to create a null at 29 GHz due to the interactions of the inductances. The line length used is 3.9 mm.

The resonator is an 800 μm wide microstrip line that has been bent in a U shape using optimal miters to conserve membrane space. The length of the resonator was adjusted to give a resonance at 28.7 GHz using a commercially available method of moments software package [34]. The coupling gap is 200 μm wide and 900 μm long (Fig. 5.5b). The measured loaded Q was 190 with a coupling of -4.6 dB ($n^2R = 144\,\Omega$), giving an extracted unloaded Q of 460 at 28.70 GHz. If the line lengths of the resonator are deembedded to the coupling gap, the resonator presents an impedance of Z_{res}=144 Ω at resonance. By adding the correct line length, the phase of the reflection coefficient is rotated around the Smith chart so that it crosses the stability circle at resonance. The equivalent added line length is the original line length of the resonator structure including the transition plus 500 μm of 50 Ω CPW line on silicon. Fig. 5.6 shows the measured response for the micromachined resonator with added line length (feedline) to achieve the correct phase. Note that the reflection coefficient crosses the input plane stability only around the resonance peak.

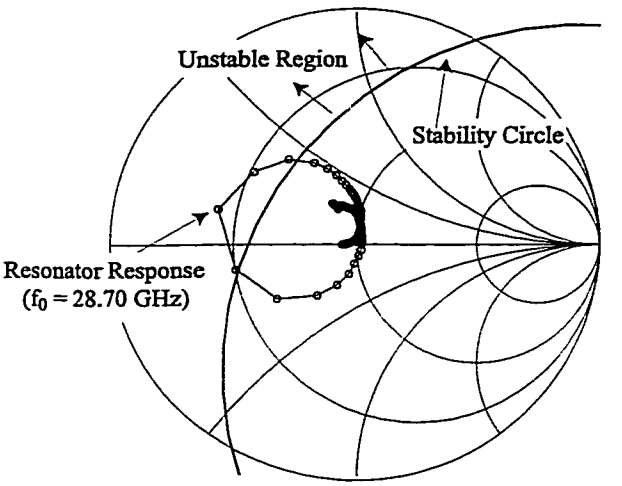


Figure 5.6: Input plane stability circle and measured micromachined resonator reflection coefficient, Γ_{res}. The points are plotted at 50 MHz intervals from 20-35 GHz.

Conventional CPW Matching Case

A second oscillator input network was designed by changing the resonator network at the gate of the transistor. Rather than using a micromachined resonator, a matching network of open circuited CPW stubs with a relatively low Q is used. This allows for a comparison of the high-Q, micromachined design with a low-Q, planar design. The rest of the oscillator circuit is unchanged. The resonator network at the gate of the transistor was designed to present the same impedance to the transistor as the micromachined resonator at 28.7 GHz (resonance). This was done using a 450 μm section of feed line with two 550 μm open circuit stubs connected at a CPW cross junction (Fig. 5.7). The cross junction has air bridges to suppress the slotline mode. Tuning pads are included in the open circuit stubs, but were not used in the actual circuit. The CPW lines are 50 Ω with a 100 μm center conductor and 65 μm gaps. The CPW lines on 1000 Ω-cm silicon have an attenuation constant of 0.049 dB/mm with an associated Q of 55 based on a method of moments simulation [34]. The input network was simulated with IE3D and measured with good agreement (Fig. 5.8). The measured input reflection coefficient has a slightly higher value

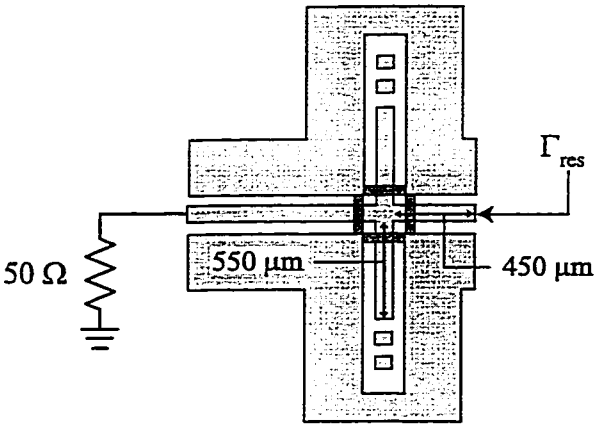


Figure 5.7: Non-micromachined input circuit. This is designed to present the same impedance at 28.7 GHz as the micromachined resonator. Tuning pads were included in the stub design, but were not used.

than the micromachined resonator. The effects of this will be discussed later in this chapter.

5.2.3 Output Matching Network

By loading the gate and source to create instability, a negative impedance is presented at the drain of the transistor. The simulated impedance at the drain is $Z_{out} = -12+j50\ \Omega$ for small signal conditions at 28.7 GHz for both the micromachined (measured data) and the non-micromachined (simulated data) input networks. For steady-state oscillations to occur, the small signal parameters must satisfy:

$$R_L < -R_{in} \tag{5.2}$$

$$X_L = -X_{in} \tag{5.3}$$

where R_L and X_L is the effective resistance and reactance looking into the output matching network and R_{in} (negative) and X_{in} is the resistance and reactance looking into the drain of the transistor at 28.7 GHz.

An output matching circuit was designed to satisfy the above conditions for oscillations at 28.7 GHz by using a single stub matching network. All lines in the

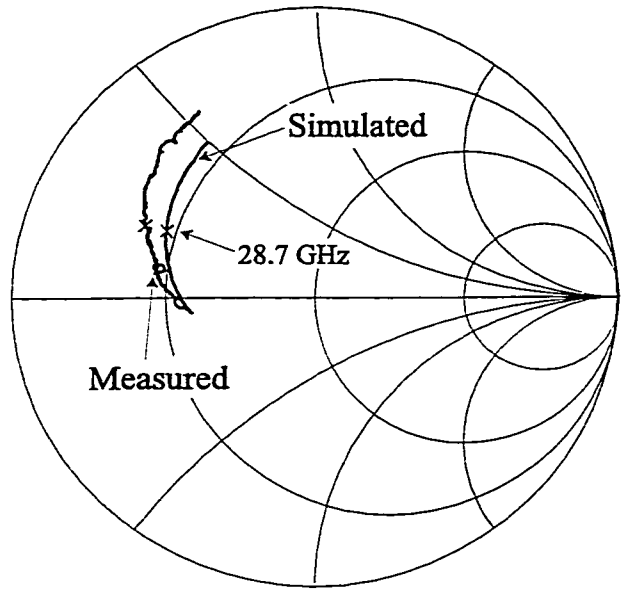
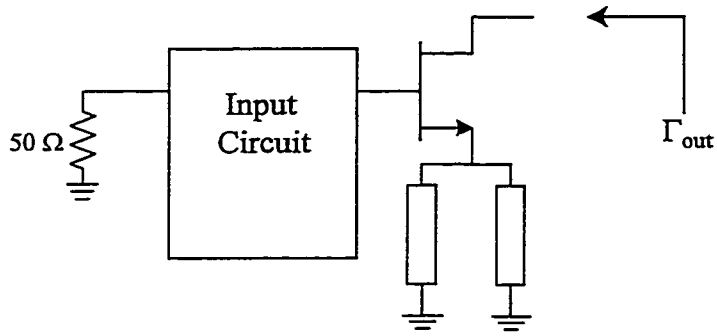


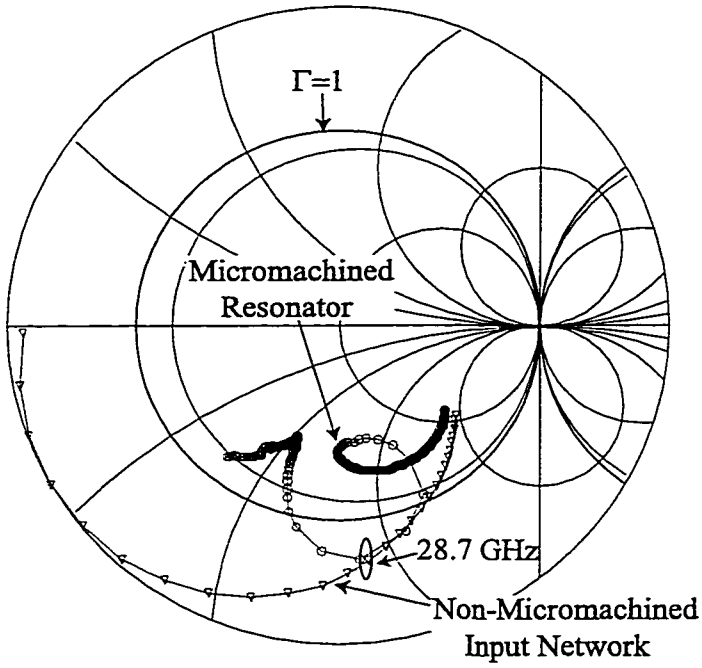
Figure 5.8: Simulated and measured input circuit response for the non-micromachined oscillator from 20-35 GHz.

matching network are 50 Ω lines with a center conductor of 100 μm and a gap width of 65 μm. The matching network was implemented by a 725 μm long line to a CPW cross loaded with pair of 800 μm long open circuited stubs. Air bridges were placed at the cross to reduce the effects of the discontinuity. Tuning pads were also included at the ends of the open circuit stubs for increasing the length if needed (tuning was not needed). The network was designed using HP EESOF Libra [50] and optimized using a moment method tool, IE3D [34] to include the effects of the CPW cross and air bridges. The matching network presents a simulated impedance of $4 + j50$ Ω, and a measured impedance of $8.1 + j55.3$ Ω at the drain of the transistor at 28.7 GHz.

The difference between the simulated and measured results has two main effects on the oscillator performance. While the resistance is still less than the absolute value of the output negative resistance, it is not much less. The common design rule for small signal microwave oscillator design is to use $R_L = |R_{in}|/3$ [18], [20], [42], [57]. As the oscillations increase, the nonlinearities of the transistor force the negative resistance to decrease until $|R_{in}| = R_L$ for steady state oscillations. If resistance of the transistor



(a)



(b)

Figure 5.9: Reflection coefficient at the output of the transistor (a) test configuration and (b) simulated response using the measured micromachined resonator data (50 MHz between points) and the simulated non-micromachined resonator data (500 MHz between points) from 20-35 GHz.

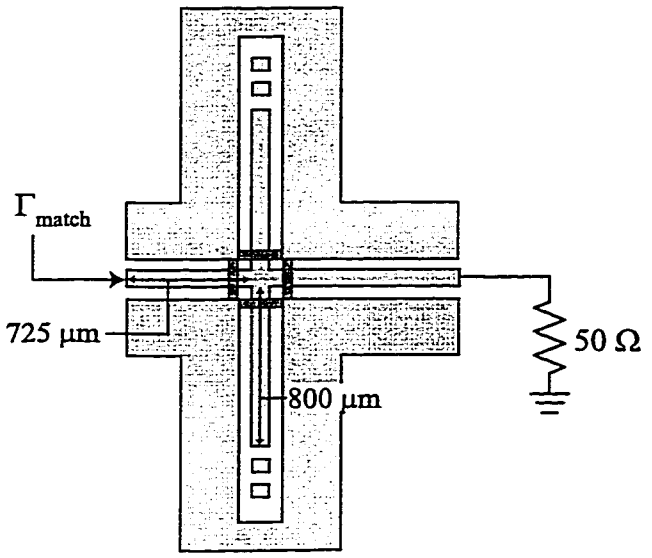


Figure 5.10: Output matching network to satisfy the small signal oscillation conditions.

oscillator reaches the steady state value too early, the output power is relatively low. The second main effect from the difference in the simulated and measured data is the oscillation frequency. Since the reactance is different for the measured and simulated data ($Z_{match} = 8.1 + j55.3\ \Omega$ instead of $4 + j50\ \Omega$, the phase matching condition may be met at a different frequency. Since the slope of the reactance is very high for a high-Q structure, this not a large concern. However, for the case of the oscillator that uses the low-Q CPW matching circuit, this has a larger effect.

5.3 Measured Results

The fabricated micromachined oscillator is shown in Fig. 5.12. The total dimensions of the assembled circuit is 6.8 mm × 8 mm and 1.4 mm thick. The oscillator was measured using 150 μm pitch Picoprobes[2]. connected to HP11612B Bias Networks and the output signal was measured with an HP8564E Spectrum Analyzer. The transistor oscillated at a bias condition of V_{GS}=-0.3 V, V_{DS}=2 V and was drawing an

[2]Picoprobe is a product of GGB Industries, Inc., Naples, FL.

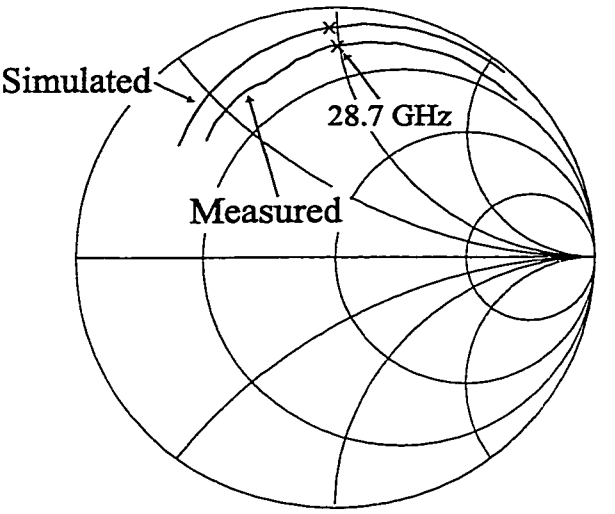
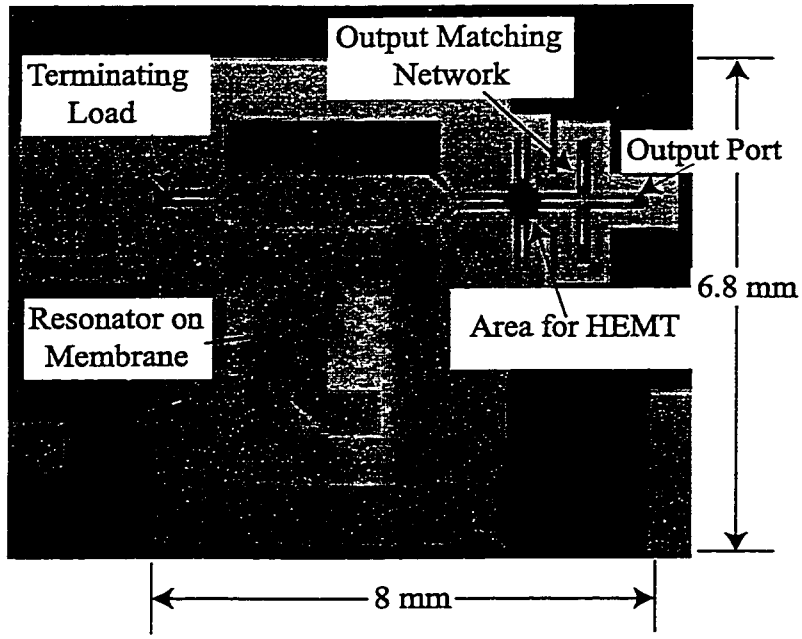


Figure 5.11: Simulated and measured output matching circuit (20-35 GHz).

I_{DS}=10 mA. The oscillation frequency was 28.6536 GHz in close agreement with the design value of 28.7 GHz. The output power was -3.5 dBm at the spectrum analyzer (Fig. 5.16). By subtracting the probe loss of 0.6 dB, and the cable and bias tee loss of 3.5 dB, the net output power is 0.6 dBm. This gives a 5.7% DC-RF efficiency.

The phase noise of the circuit was initially measured using the HP85671A Phase Noise Utility on the spectrum analyzer. The measured phase noise using this method is shown in Fig 5.14. However, this phase noise measurement tool has severe limitations when measuring free-running oscillators. The phase noise utility is essentially a software macro for the spectrum analyzer that performs several direct-spectrum noise measurements at different offset frequencies. The phase noise is calculated by measuring the peak signal level, offsetting the marker by a given amount, measuring the sideband noise power, then dividing the peak signal level by the power at the offset and the resolution bandwidth. This measurement is taken over 5 decades of offset frequencies. In the process of sweeping in between decades, the free-running oscillator may drift slightly. In addition, the spectrum analyzer resets IF filters several times during the sweep. This has the effect of frequency pulling the oscillator by a small amount [58]. All of this results in a large error in the phase noise measurement for



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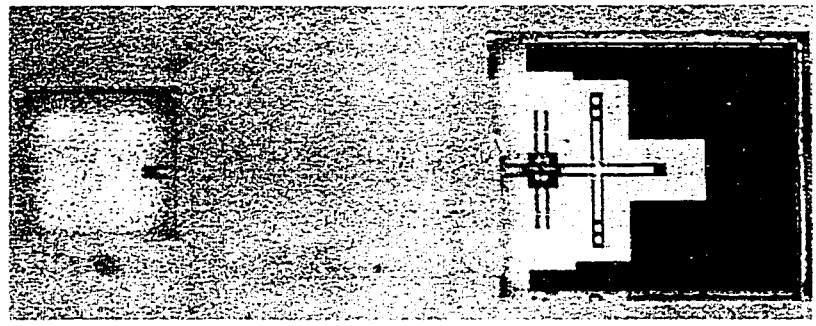


(b)

Figure 5.12: Fabricated micromachined oscillator (a) with the cover removed (photo taken before the HEMT was mounted) and (b) packaged with device mounted and ground plane cover assembled.

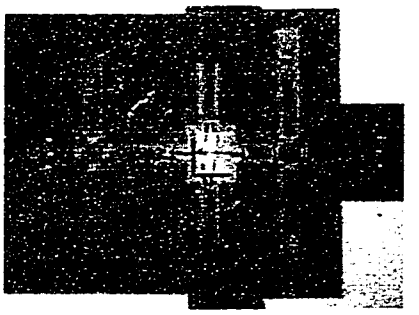


Figure 5.13: Fabricated non-micromachined oscillator.

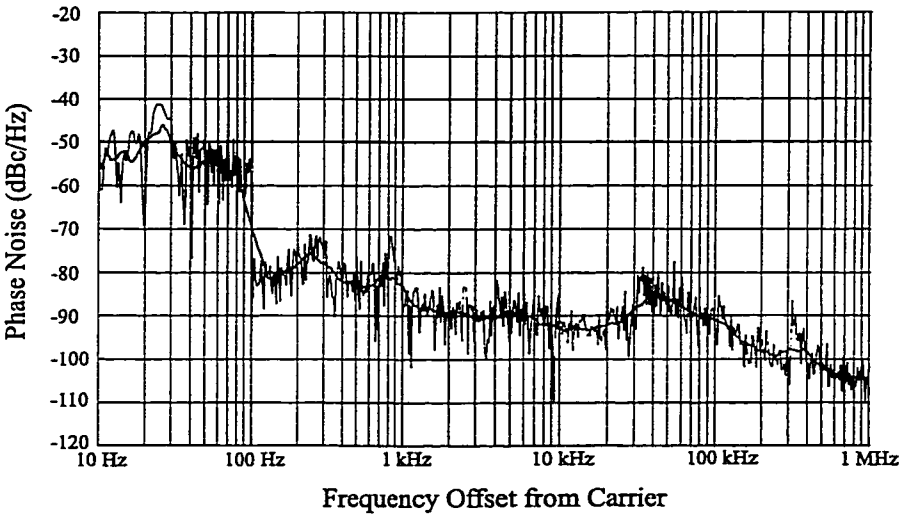


Figure 5.14: Phase noise measurement of micromachined oscillator using HP85671A Phase Noise Utility.

frequencies close to the carrier ($f_m < 100$ kHz).

The phase noise was re-measured manually by performing several sweeps over a 5 MHz bandwidth with a 3 kHz resolution bandwidth and averaging the sweeps. The data was then averaged and converted to noise spectral density in a 1 Hz bandwidth by taking into account the peak signal power and the resolution bandwidth (Fig. 5.15). This results in a very different value of phase noise than the measurements taken using the HP85671A for offset frequencies less than 100 kHz. The measured phase noise is -92 dBc/Hz at 100 kHz and -122 dBc/Hz at 1 MHz offset. The slope of the phase noise below 1 MHz shows that the phase noise is rolling off as $1/f_m^3$ where f_m is the frequency offset from the carrier. This is characteristic of up-converted FM flicker noise [15]. After an offset frequency of 1 MHz, the sideband noise reaches the noise floor of the spectrum analyzer[3]. The manufacturer of the HEMT does not specify any data for flicker noise of the FHR20X. However, HEMT devices are known for having poor flicker noise performance with high values for flicker noise cutoff frequencies [60]. HEMT devices are based on current conduction along a surface channel leading to large amounts of flicker noise from surface traps and recombination. The effects of flicker noise can be reduced by using HBT devices where the current conduction is through the bulk material [61]. This is compared with the linear model for phase noise based on equation 5.1 from the beginning of this chapter. Assuming a noise figure of 5 dB for the device without feedback (extrapolated from manufacturer data), a loaded Q of 190, and room temperature operation, the linear model for phase noise is plotted on Fig. 5.15. This approximation models random white FM noise and neglects flicker noise resulting in a roll-off of 20 dB/decade [62]. If the measured phase did not hit the noise floor of the spectrum analyzer, it should eventually converge with the linear model for phase noise. This implies that the oscillator is predominately limited by

[3]The specification for the noise floor on the spectrum analyzer is less than -95 dBm for a 1 kHz resolution bandwidth [59]. The noise floor specification is not given for a 3 kHz resolution bandwidth. Based on the value of -95 dBm in a 1 kHz bandwidth, the average power in a 1 Hz bandwidth is -125 dBm. With a -3.5 dBm input signal, the noise floor the phase noise is roughly -121.5 dBc/Hz.

1/f noise.

The fabricated non-micromachined oscillator is shown in Fig. 5.13. The oscillator that was not micromachined oscillated under the same bias conditions at 27.3751 GHz with an output power of 1.3 dBm (-2.8 dBm measured at the spectrum analyzer with the total of 4.1 dB of loss from the probe, cable, and bias-T) resulting in a DC-RF efficiency of 6.7%. The output spectrum is shown in Fig. 5.17. The increase in power compared to the micromachined case is due to the higher mismatch in the input circuit of the non-micromachined oscillator as well as a higher transistor gain at 27.4 GHz versus 28.6 GHz. This non-micromachined resonator circuit was designed to present the same impedance as the micromachined resonator. However, the actual measured performance shows that the impedance is actually lower resulting in a larger reflection coefficient (Fig. 5.8). The change in impedance combined with a higher gain creates a larger negative resistance at the output resulting in a higher output power. The frequency shift is due to the low quality factor of the feedback circuit. The phase noise was measured in a similar manner as with the micromachined oscillator and is shown in Fig. 5.15. The phase noise performance was -84 dBc/Hz at 100 kHz and -112 dBc/Hz at 1 MHz offset. On an average, the phase noise performance of the non-micromachined oscillator was 10 dB worse than the micromachined oscillator.

As a comparison, the spectrum for both oscillators are plotted together in Fig. 5.18. The calculated Q of the CPW lines is 55. Since the impedance and coupling of the resonant structure are approximately the same, the external loading is the same for the two oscillators resulting in the same external Q for both cases. The external Q is approximately 300 based for the weak coupling of the resonator based on the measurements from the micromachined resonator. From [42], the loaded, unloaded, and external Q's of a resonant structure are given by:

$$\frac{1}{Q_L} = \frac{1}{Q_U} + \frac{1}{Q_{ext}} \tag{5.4}$$

where Q_L, Q_U, and Q_{ext} are the loaded, unloaded, and external Q's of a resonant

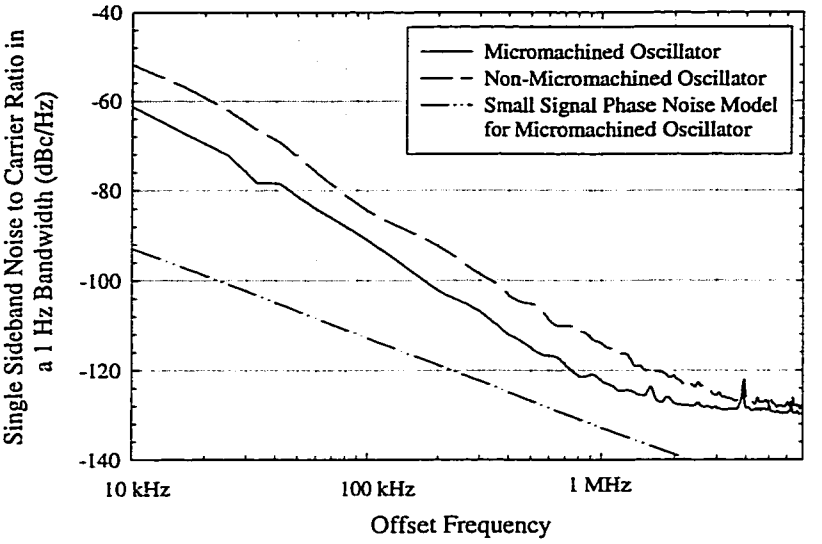


Figure 5.15: Measured and simulated phase noise performance. Simulated curve is based on linear approximation for phase and neglects flicker noise.

system. For two resonators with unloaded Q's of Q_{U_1} and Q_{U_2}, and the same external Q of Q_{ext}, the ratio of the loaded Q's is:

$$\frac{Q_{L_1}}{Q_{L_2}} = \frac{Q_{U_1}}{Q_{U_2}}\left(\frac{Q_{U_2}+Q_{ext}}{Q_{U_1}+Q_{ext}}\right) \tag{5.5}$$

Doing the calculation for $Q_{U_1} = 460$ and $Q_{U_2} = 55$, for the micromachined case and the non-micromachined case, respectively, the ratio of the loaded Q's, $Q_{L_1}/Q_{L_2} = 3.9$. By using the linear approximation for phase noise in oscillators, the phase noise is approximately proportional to $1/Q^2$, and the micromachined oscillator should show an 11.8 dB improvement in phase noise performance. This is in good agreement with the measured phase noise results showing an average of 10 dB improvement in phase noise.

5.4 Conclusion

A 28.6 GHz oscillator with low phase noise has been demonstrated using a planar micromachined resonator. The oscillator has an output power of 0.6 dBm with a

5.7% DC-RF efficiency and a measured phase noise of -92 dBc/Hz at a 100 kHz offset frequency. A non-micromachined oscillator was also fabricated for comparison showing that the high-Q, micromachined resonator gave an 10 dB improvement in phase noise. A comparison of the micromachined oscillator with published work in the area of DRO's is difficult in that phase noise is rarely given over a range of offset frequencies. Also, since 1/f noise is such a dominant factor in phase noise, the phase noise of an oscillator is a strong function of they type of device (either MESFET, HEMT, or HBT).

HEMT devices have been implemented in DRO's that have resulted in phase noise of -102 dBc/Hz at 100 kHz offset for a DRO at 23 GHz [54], -75 dBc/Hz at 10 kHz offset for a DRO at 27.6 GHz [55], -102 dBc/Hz at 100 kHz and -117 dBc/Hz at 1 MHz offset at 30 GHz [17], and -68 dBc/Hz at a 100 kHz offset for a DRO at 38 GHz in [63]. The noise figure of device increases with frequency resulting and the quality factor of the dielectric resonator changes resulting in an inaccurate comparison. Therefore, the only real comparison would be with [17] (-102 dBc/Hz at 100 kHz and -117 dBc/Hz at 1 MHz offset at 30 GHz). The micromachined oscillator showed a phase noise that was 10 dB worse than that of [17] at 100 kHz offset frequency and 5 dB better at 1 MHz. Note that the reported phase noise does not follow either the 1/f phase noise profile of -30 dB/decade or the pure white FM phase noise profile of -20 dB/decade and no measurement details were provided in the published work.

Published work with HBT DRO's have shown excellent phase noise performance due to the reduced device 1/f noise. State of the art HBT based DRO's have published phase noise values of -124 dBc/Hz at 100 kHz offset at 11.02 GHz [64] and -82 dBc/Hz at 100 kHz offset at 37.7 GHz [65]. In both HBT cases, 1/f noise was greatly reduced at offset frequencies above 100 Hz.

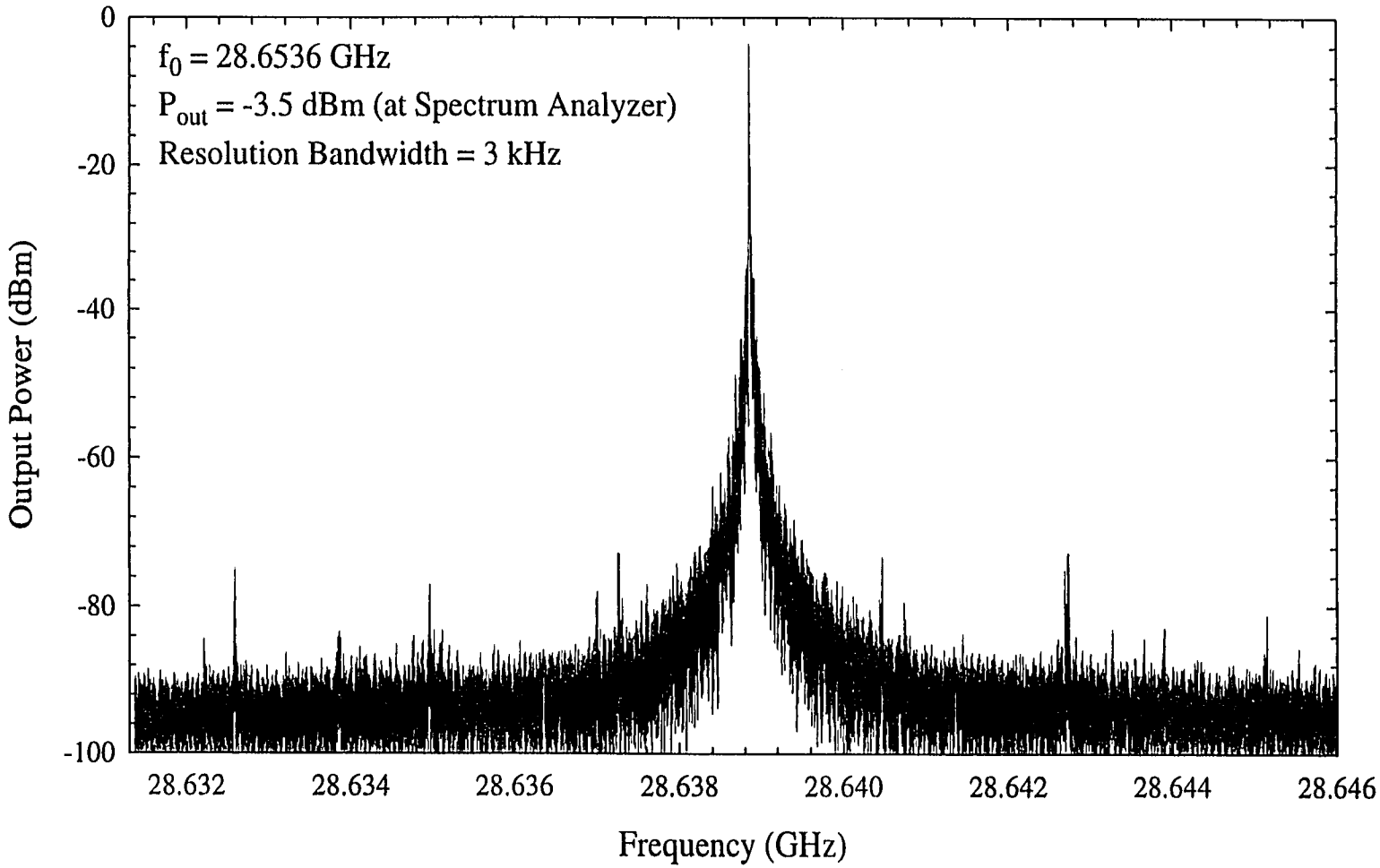


Figure 5.16: Measured micromachined oscillator spectrum. The power is defined at the spectrum analyzer port.

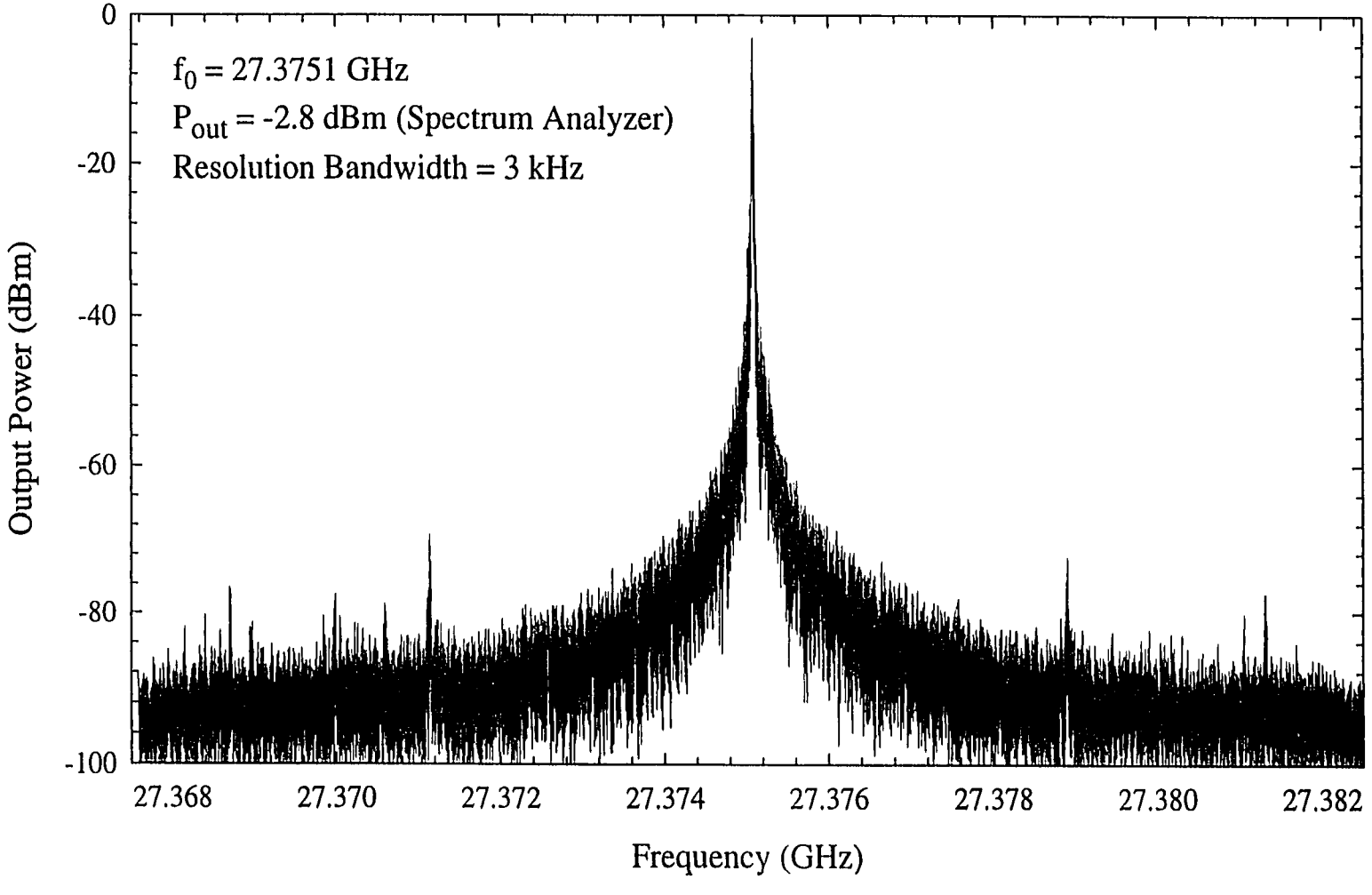


Figure 5.17: Measured non-micromachined oscillator spectrum. The power is defined at the spectrum analyzer port.

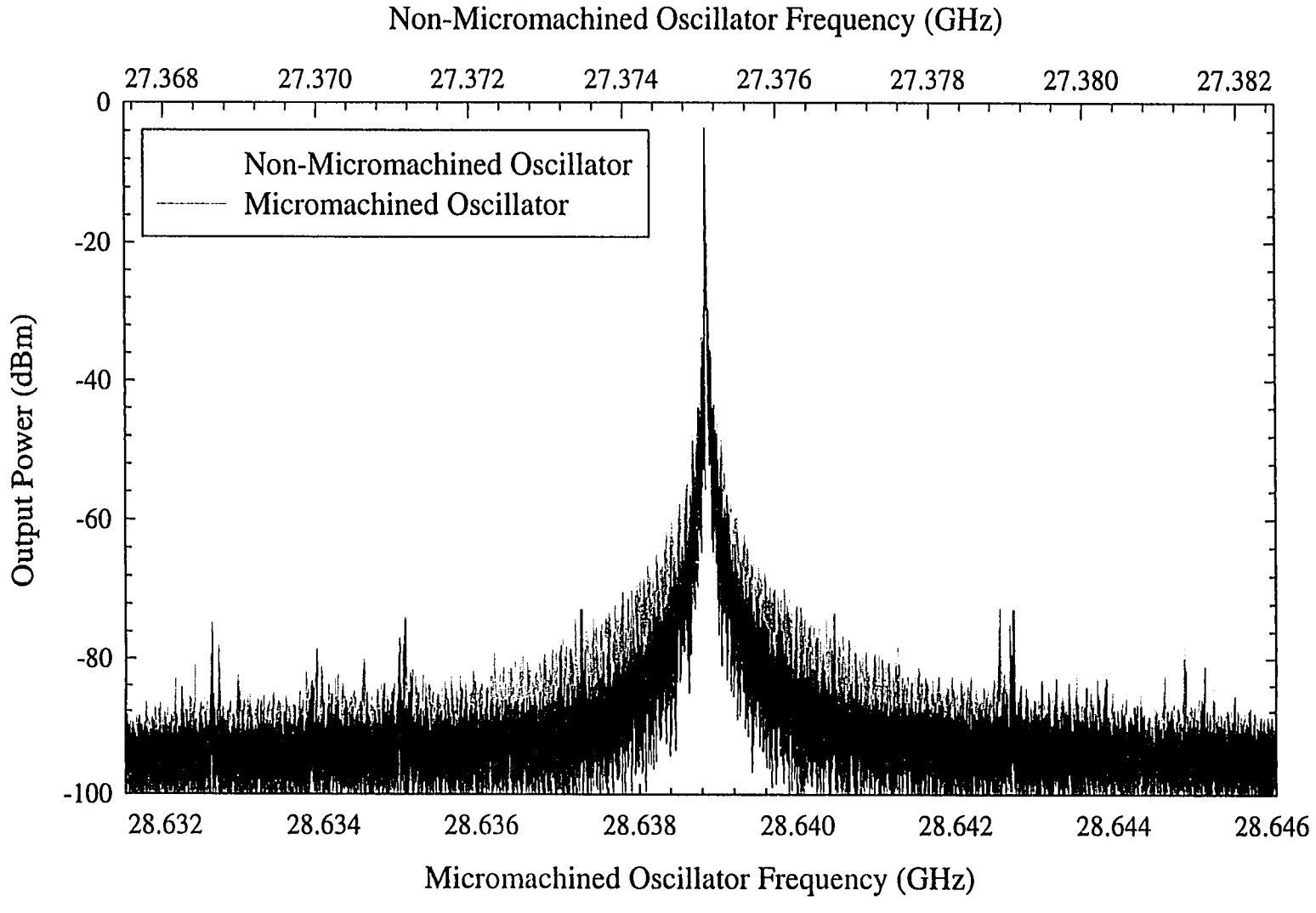


Figure 5.18: Comparison of micromachined to non-micromachined oscillator spectrum. The x-axis is adjusted to match the oscillation frequency of the non-micromachined oscillator to the micromachined case. The frequency span and scale are identical for both cases. Displayed data was taken with a 3 kHz resolution bandwidth.

CHAPTER 6

A MICROMACHINED INTERDIGITAL FILTER BANK

6.1 Introduction

Switched filter banks are commonly used for multiband communication systems and frequency hopping radar systems where high isolation between the filter elements is a requirement. Also, compact size, reduced weight, and low material and fabrication costs are essential. The conventional design for a switched filter bank is to machine a series of channels in a metal carrier and to place individual filters inside these channels. An input and output switching network of PIN diodes selects the filter response (Fig. 6.1). The conventional design technique suffers from many drawbacks. The machined metal carrier and packaging is custom made and therefore is very expensive to produce. Furthermore, the use of separate low-loss substrates for filters combined with active semiconductor substrates for PIN diodes is expensive in assembly cost. Silicon micromachining, combined with micropackaging, is a possible solution to the cost problem.

The purpose of this work is to demonstrate the capability of combining the low-loss characteristic obtained using membrane technology with the high isolation and

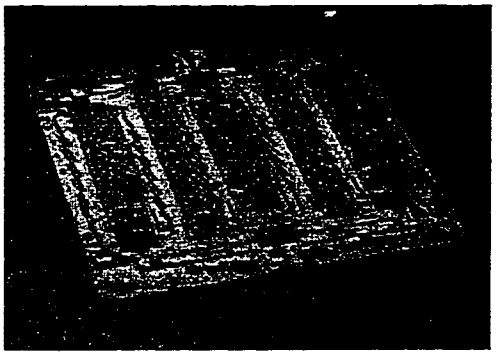


Figure 6.1: Switched filter bank (*Courtesy of Texas Instruments*).

compact size obtained using micropackaging. The goal is to construct a high performance X/Ku-band filter bank with high isolation between the filters constructed on the *same substrate.*

6.2 Design of Micromachined Filter Banks

The micromachined filters are based on an interdigital design shown by Matthaei et al. [4]. Interdigital filters have been used extensively at frequencies in the low microwave region where they have been constructed from milled aluminum bars and mounted in thick cavities [66]. Recently, this filter topology has been demonstrated at Ku-Band by applying micromachining techniques [11]. The filter topology consists of an array of interdigital fingers that are approximately $\lambda/4$ in length. The fingers are shorted on one end and and open circuited on the other end in an alternated fashion to form quarter-wave resonators (Fig. 6.2). The first and the last finger act as impedance transformers that match the loading impedance to the filter impedance. Each resonator then has a self capacitance to ground and a mutual capacitance between each resonator. An assumption is made in this chapter that the mutual capacitance between non-adjacent resonators is much smaller as compared to the capacitance of adjacent resonators and will be neglected. This leads to a ca-

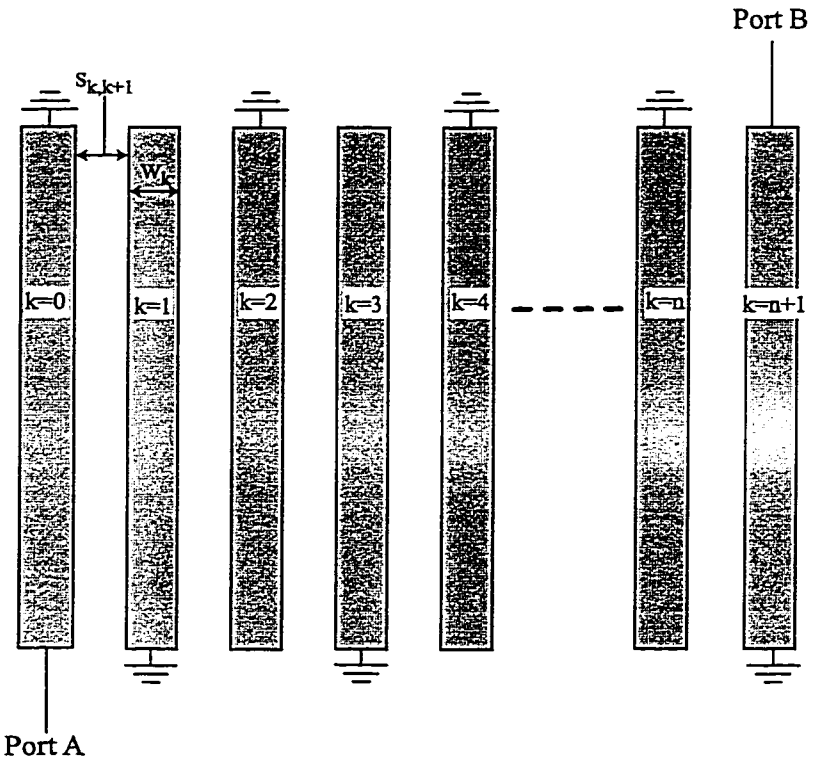


Figure 6.2: Topology of interdigital coupled line filter

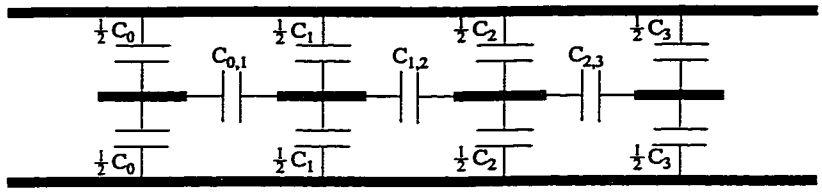


Figure 6.3: Cross section of an array of coupled lines

pacitive coupling structure of an array of lines (Fig. 6.2). The self capacitance is labeled as C_k and the mutual capacitance is $C_{k,k+1}$. This is a structure with an array of quarter-wave resonators acting as shunt resonators with shunt capacitances to ground and mutual capacitances between elements. As shown in Fig. 3.5 this is a J inverter [67]. Therefore, the filter is of the form of Fig. 3.2 and is a bandpass filter.

The basic design consists of determining the low-pass prototype function, calculating the admittance inverters for the structure which sets the self and mutual capacitances of the lines, and then finally converting that into a geometry (resonator widths and lengths) for the filter.

The impedance inverters are found from eqn. 3.4. The design equations for the interdigital require a phase term that includes the effects of a non-zero bandwidth. The phase term is:

$$\theta_1 = \frac{\pi}{2}\left(1 - \frac{\bar{\omega}}{2}\right) \tag{6.1}$$

where $\bar{\omega}$ is the percent bandwidth of the filter. The self capacitance per unit length of each filter finger, C_k, is:

$$\frac{C_0}{\epsilon} = \frac{\eta_0 Y_a}{\sqrt{\epsilon_r}}\left(1 - \frac{J_{0,1}}{Y_a}\sqrt{h}\right) \tag{6.2}$$

$$\begin{aligned}\frac{C_1}{\epsilon} =& \frac{\eta_0 Y_a}{\sqrt{\epsilon_r}}\left(-\frac{J_{0,1}}{Y_a}\sqrt{h} + h\left[\frac{\tan\theta_1}{2} + \left(\frac{J_{0,1}}{Y_a}\right)^2 + \right.\right. \\ & \left.\left.\sqrt{\left(\frac{J_{1,2}}{Y_a}\right)^2 + \frac{\tan^2\theta_1}{4}} - \frac{J_{1,2}}{Y_a}\right]\right)\end{aligned} \tag{6.3}$$

$$\left.\frac{C_k}{\epsilon}\right|_{k=2 \text{ to n-1}} = \frac{\eta_0 Y_a}{\sqrt{\epsilon_r}}\left(\sqrt{\left(\frac{J_{k-1,k}}{Y_a}\right)^2 + \frac{\tan^2\theta_1}{4}} + \sqrt{\left(\frac{J_{k,k+1}}{Y_a}\right)^2 + \frac{\tan^2\theta_1}{4}} - \frac{J_{k-1,k}}{Y_a} - \frac{J_{k,k+1}}{Y_a}\right) \tag{6.4}$$

$$\frac{C_n}{\epsilon} = \frac{\eta_0 Y_a}{\sqrt{\epsilon_r}}\left(-\frac{J_{n,n+1}}{Y_a}\sqrt{h} + h\left[\frac{\tan\theta_1}{2} + \left(\frac{J_{n,n+1}}{Y_a}\right)^2 + \sqrt{\left(\frac{J_{n-1,n}}{Y_a}\right)^2 + \frac{\tan^2\theta_1}{4}} - \frac{J_{n-1,n}}{Y_a}\right]\right) \tag{6.5}$$

$$\frac{C_{n+1}}{\epsilon} = \frac{\eta_0 Y_a}{\sqrt{\epsilon_r}}\left(1 - \frac{J_{n,n+1}}{Y_a}\sqrt{h}\right) \tag{6.6}$$

where Y_a is the loading impedance and h is an admittance scaling factor equal to Y_{int}/Y_a where Y_{int} is the internal admittance of the filter. The mutual capacitance per unit length, $C_{k,k+1}$ is:

$$\frac{C_{0,1}}{\epsilon} = \frac{\eta_0 Y_a}{\sqrt{\epsilon_r}}\frac{J_{0,1}}{Y_a}\sqrt{h} \tag{6.7}$$

$$\left.\frac{C_{k,k+1}}{\epsilon}\right|_{k=1 \text{ to n-1}} = \frac{\eta_0 Y_a h}{\sqrt{\epsilon_r}}\left(\frac{J_{k,k+1}}{Y_a}\right) \tag{6.8}$$

$$\frac{C_{n,n+1}}{\epsilon} = \frac{\eta_0 Y_a}{\sqrt{\epsilon_r}}\frac{J_{n,n+1}}{Y_a}\sqrt{h} \tag{6.9}$$

The process of finding the physical dimensions of the interdigital fingers coupling gaps is derived from analyzing the even and odd-modes of the fringing capacitance of the fingers. The total mutual capacitance, $C_{k,k+1}$, is difference of the even and odd-mode fringing capacitance:

$$C_{k,k+1} = C_{fo_{k,k+1}} - C_{fe_{k,k+1}} \tag{6.10}$$

The even mode fringing capacitance, $C_{fe_{k,k+1}}$, and odd mode fringing capacitance, $C_{fo_{k,k+1}}$, of suspended coupled lines are given by Cohn [44]:

$$\frac{C_{fe_{k,k+1}}\left(\frac{s_{k,k+1}}{b}\right)}{\epsilon} = \left(\frac{s_{k,k+1}}{b}\right) - \frac{2}{\pi}\ln\left(\cosh\frac{\pi s_{k,k+1}}{2b}\right) \tag{6.11}$$

$$\frac{C_{fo_{k,k+1}}\left(\frac{s_{k,k+1}}{b}\right)}{\epsilon} = \left(\frac{s_{k,k+1}}{b}\right) - \frac{2}{\pi}\ln\left(\sinh\frac{\pi s_{k,k+1}}{2b}\right) \tag{6.12}$$

where b is the distance between the two ground planes and $s_{k,k+1}$ is the spacing between two fingers k and k+1. The spacing between the adjacent fingers of the filter can then be found by solving equation 6.11 and 6.12 by substituting from 6.10 to get:

$$s_{k,k+1} = \frac{2b}{\pi} \tanh^{-1}\left[\exp\left(\frac{-\pi C_{k,k+1}}{2\epsilon}\right)\right] \tag{6.13}$$

The line widths, w_k, are calculated by taking the static capacitance per unit length of the line between the two ground planes and subtracting the even-mode fringing capacitance per unit length of the two adjacent lines [45]. Once the separation between the two lines is known, the even mode capacitance is calculated by equation 6.11 and the line width is:

$$w_k = \frac{b}{2}\left(\frac{1}{2}\frac{C_k}{\epsilon} - \frac{C_{fe_{k-1,k}}}{\epsilon} - \frac{C_{fe_{k,k+1}}}{\epsilon}\right) \tag{6.14}$$

The two filters for the filter bank were designed to be 4-pole, 18% bandwidth filters with 0.2 dB ripple centered at 11 GHz and 13.75 GHz. The finger lengths are 6100 μm and 4960 μm for the 11 and 13.75 GHz filters, respectively. Since the number of poles, bandwidth, and the pass band ripple are identical for the two filters, the line widths and gaps are the same. The filters are stripline with the top wafer etched completely through as opposed to the timed etched of the suspended microstrip. This gives a total height between ground planes of 2 $\times$ 525 μm increasing the quality factor of the resonators compared to the case of suspended microstrip. Table 6.1 list the line widths and gaps for the fingers of both filters.

To increase the isolation between the two filters, a micropackaging technique was developed isolating each cavity containing separate filters. The micropackage is a two layer structure placed on a bottom carrier substrate. The two layers consist of a micromachined filter substrate and a top cavity substrate (Fig. 6.4). Surrounding the filters are etched via grooves which prevent substrate modes from forming and most importantly, isolate the two filters. The top cavity substrate is a micromachined wafer that surrounds the filters except for small mouse-holes for feedlines to the filters. The

Table 6.1: Micromachined Filter Bank Finger Dimensions

Finger, k	w_k	$s_{k,k+1}$
0	620 μm	
1	720 μm	25 μm
2	590 μm	300 μm
3	590 μm	410 μm
4	720 μm	300 μm
5	620 μm	25 μm

layers are secured to each other with a silver conductive epoxy [1]. The package forms a rugged, compact, and light weight structure.

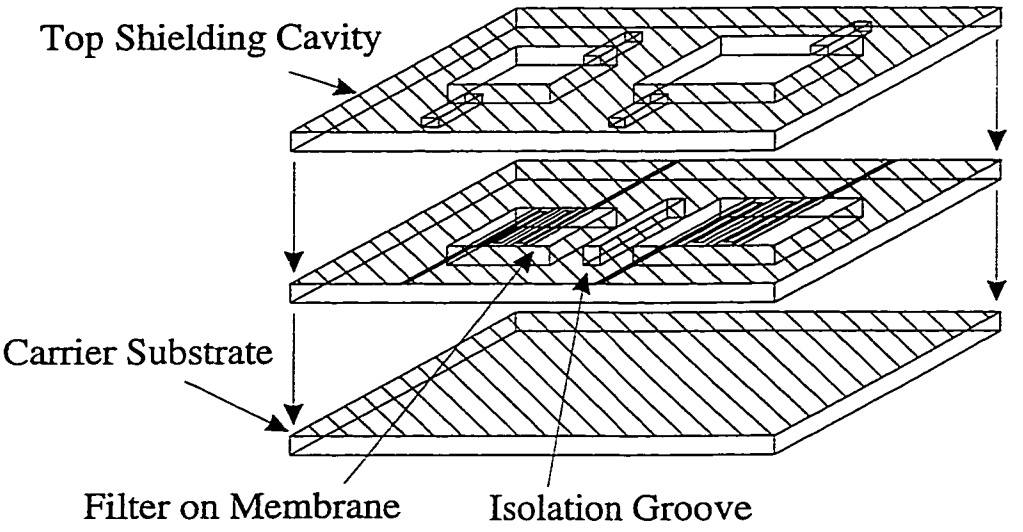
The feedlines for the filters are 2.4 mm long shielded grounded coplanar waveguide lines on high resistivity silicon (ρ=1200 Ω-cm). The lines extend beyond the via holes of the filter and are not isolated from each other in any other way (Fig. 6.5a). An airbridge was fabricated at the input of each filter to suppress undesired modes resulting from the strong coupling of the first finger of the filter.

The total surface area of the filter bank is 22.5 mm $\times$ 10.3 mm (Fig. 6.5). The entire structure is only 1 mm thick which is about 5$\times$ smaller than conventional switched filter banks.

6.3 Filter Bank Measurements

The total surface area of the filter bank is 22.5 mm $\times$ 10.3 mm (Fig. 6.5). The entire structure is only 1 mm thick which is about 5$\times$ smaller than conventional switched filter banks. The filter response and isolation were measured from 2-16 GHz using an

[1]EPO-TEK H20E is a product of Epoxy Technology, Inc., Billerica, MA



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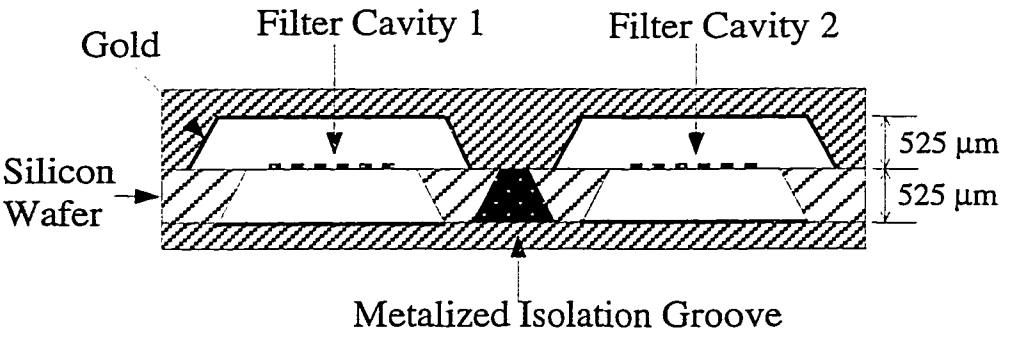
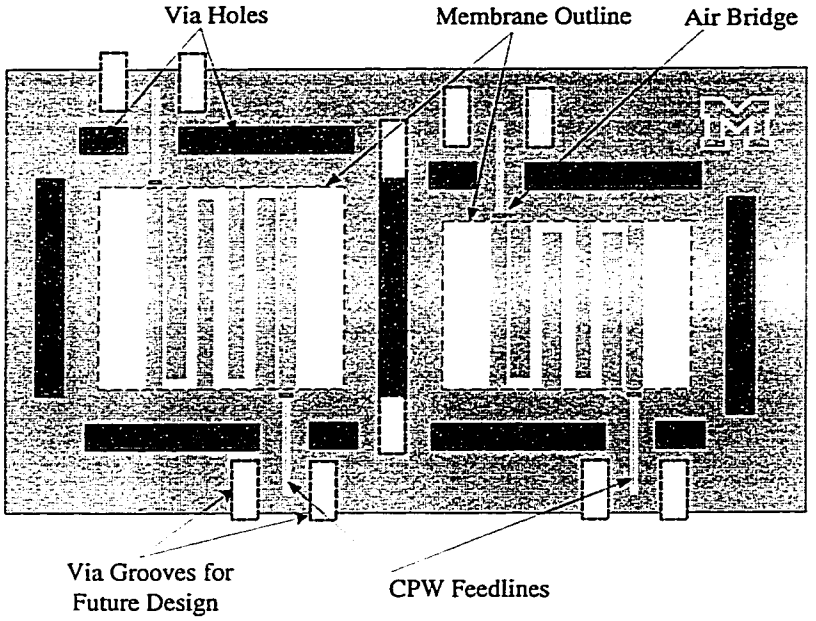


(b)

Figure 6.4: Micropackaging of micromachined filter bank, (a) isometric view, (b) cross section view.



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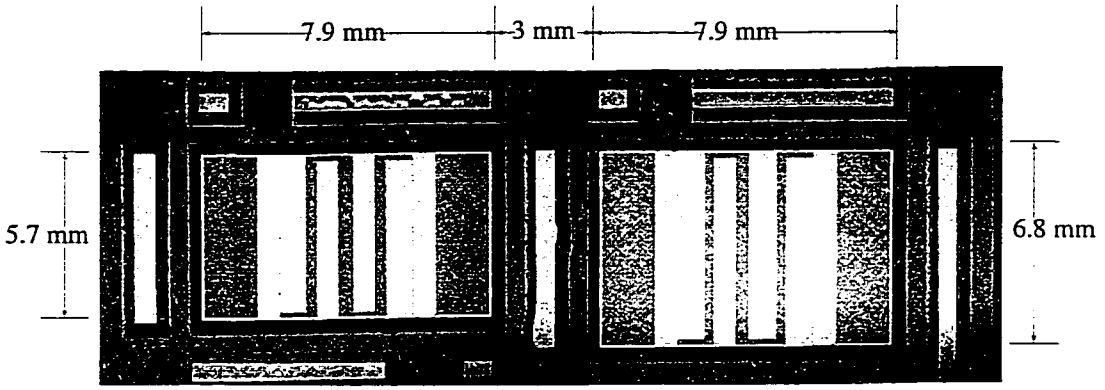


(b)

Figure 6.5: Micromachined micropackaged filter bank with top cavity and carrier substrate removed, (a) top view of filter substrate, (b) bottom view of fabricated filters.

HP 8510C Network analyzer. A Short-Open-Load-Through calibration method was used with 150 μm pitch Picoprobes and CS-5 calibration substrate [2].

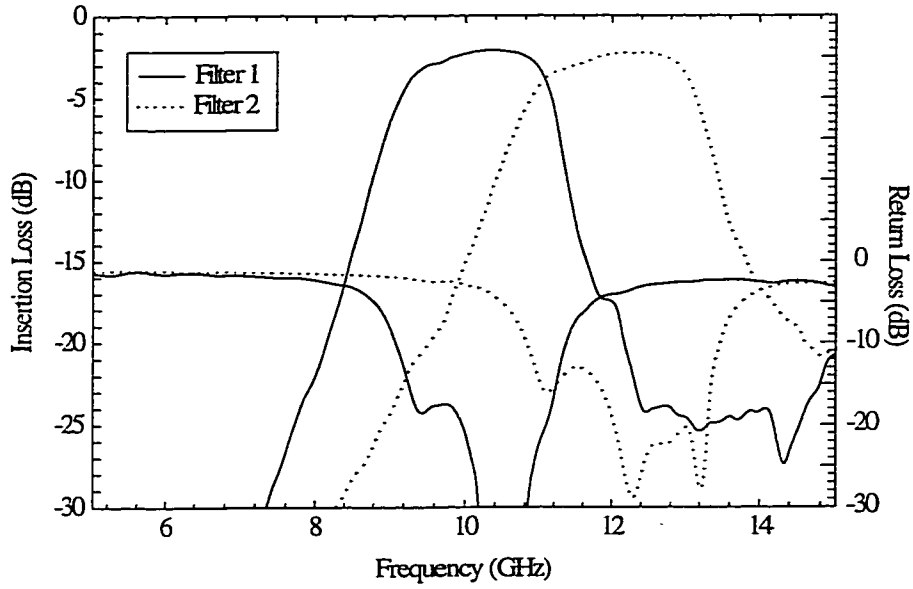
The measured port-to-port insertion loss is 2 dB for each filter (Fig. 6.6a). The port-to-port loss includes the feedline loss, the transition loss between the silicon and the membrane, and the loss within the filter. The loss of each of the 0.4 mm GCPW feed lines is 0.4 dB each making a total feedline loss of 0.8 dB. The filter mismatch loss $(1 - |S_{11}|^2)$ is 0.4 dB. The theoretical Q of the quarter-wave resonators was found to be 310 using a commercial method of moments analysis package [34]. This results in a calculated loss from the resonator fingers of 0.8 dB [4], and a port-to-port calculated loss of 2 dB, which is in very close agreement with the measurements.

The isolation between the filters was measured by loading one filter with a broadband matched load at one port, applying a signal to the other port, and measuring the transmission at the closest port to the other filter. This is the case of the strongest coupling between the two filters. The measured isolation was below -40 dB across the passbands of the filters (Fig. 6.6b). This is limited by feedline radiation into the 525 μm silicon substrate [68]. While the filters themselves are isolated from each other, the feedlines are not. In future designs, via grooves should be added along the feedlines to improve isolation. It is important to note that micropackaging technologies will never achieve the isolation level obtained using two physically isolated substrates, but it does offer excellent performance for filters integrated close together on the *same* substrate.

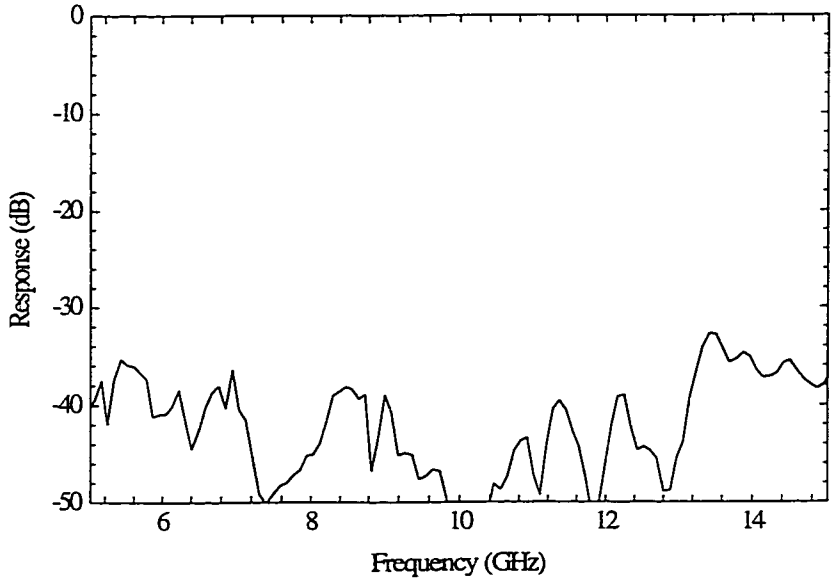
6.4 Conclusion

This demonstrates the capability of combining micromachining and micropackaging techniques to fabricate completely integrated, high performance filter banks with

[2]Picoprobe and CS-5 are products of GGB Industries, Inc., Naples, FL.



(a)



(b)

Figure 6.6: Measured response (a) and isolation (b) of the micropackaged filter bank.

high isolation between elements. To increase isolation, the more via grooves should be added to shield the feedlines from radiating. The processing used is compatible with via-hole fabrication in Silicon, SiGe, GaAs, and InP. This can result in low cost integration of high performance filter banks for communication systems.

CHAPTER 7

A WIDEBAND VARACTOR TUNED FILTER

7.1 Introduction

Low-loss, tunable frequency filters are often used as tracking filters for multiband telecommunication systems, radiometers, and wideband radar systems. Typically, tracking filters are mechanically tuned by adjusting the cavity dimensions of the resonators or magnetically altering the resonant frequency of a ferromagnetic yttrium-iron-garnet element [4], [69]. Neither of these approaches can easily by miniaturized or produced in large volumes for wireless communication products. The filters must be custom machined, carefully assembled, tuned, and calibrated.

An electrically tunable, capacitively-loaded interdigital filter is presented in this chapter. The tuning element is a reverse-biased varactor diode. The resonators of the tunable filter are shortened interdigital fingers with varactor diodes at the ends. The coupling is carefully controlled by the geometry of the fingers and the tuning is performed by changing the bias on the varactor diodes. Since both the interdigital fingers and the diodes are carefully controlled and fabricated in batch, this filter can easily be produced in large quantities. The filter is fabricated using suspended stripline in an aluminum cavity for the RF band filter (0.7-1.3 GHz) and micromachined in silicon for the X-band filter (5.5-10.5 GHz).

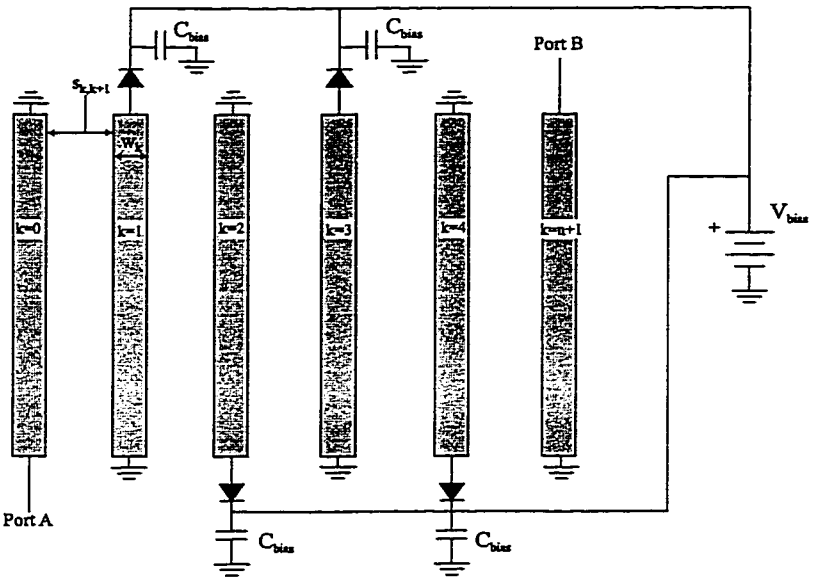


Figure 7.1: Topology of the varactor loaded interdigital bandpass filter

7.2 Design of Varactor Loaded Micromachined Interdigital Filters

The design of a varactor-loaded interdigital filter is similar to the capacitively loaded comb-line filter presented in Matthaei [4], but is adapted for the interdigital topology. The interdigital filter is a symmetric filter of coupled resonators. The first finger at the input and output port is a shorted line that acts as an impedance transformer for the filter. This is the only line with a fixed termination. The interior coupled lines are shorted at one end and loaded with varactor diodes at the other end (Fig. 7.2). To allow for biasing, large capacitors are added (C_{bias}). When the bias voltage is changed, the thickness of the depletion region of the varactor diodes changes. This alters the capacitance of the varactor tuning the resonant length of fingers. The width and separation of the interior lines are determined only by the bandwidth of the normalized filter response function, and is independent of the center frequency. The center frequency of the filter is determined by the resonant lengths of the lines which is tuned by the varactors. The limiting factor for the filter tuneability is the fixed lengths of the input and output finger lengths, the internal impedance of

the filter, the range of capacitance of the varactor diodes, and the electrical length of the fingers.

The electrical length of a single finger, θ, without the capacitive loading is given by:

$$\theta(V_{bias}) = 2\pi f l \sqrt{\epsilon_{eff}}/c \tag{7.1}$$

where f is the frequency, l is the length of the fingers, ϵ_{eff} is the effective relative dielectric constant (approximately 1.05 for membrane supported microstrip) and c is the speed of light. If the finger is loaded by a shunt capacitance, the effective length of the transmission line increases. If the amount of capacitance added increases the overall effective length to $\pi/2$, and the transmission line is shorted at one end as in the case of the interdigital filter, then the capacitively loaded transmission line behaves as a quarter-wave resonator. In order to achieve resonance, the reactance of the transmission line and the varactor must cancel ($X_{Varactor} + X_{T-Line}$=0). By using a lossless transmission line approximation ($X_{T-Line} = Z_{ak} \tan\theta$ where Z_{ak} is the intrinsic impedance of the k^{th} finger), the necessary capacitance is given by:

$$C_{var} = \frac{1}{Z_{ak} 2\pi f_0 \tan\theta_0} \tag{7.2}$$

where f_0 and θ_0 are the frequency and electrical length of the finger at resonance. Conversely, the resonant frequency of the varactor loaded finger for a given capacitance is:

$$f_0(V_{bias}) \approx \frac{1}{Z_{ak} 2\pi C_{var}(V_{bias}) \tan\left(\theta_0(V_{bias})\right)} \tag{7.3}$$

where f_0, C_{var}, and θ_0 are now functions of the bias voltage. Note that this is a transcendental function since the value of $\tan\theta_0$ is also a function of f_0.

The first step is to choose a characteristic impedance that gives a reasonable quality factor for the resonator and allows for a wide tuning range. From equation 7.3, a larger tuning range is obtained by making Z_{ak} small. A lower internal impedance

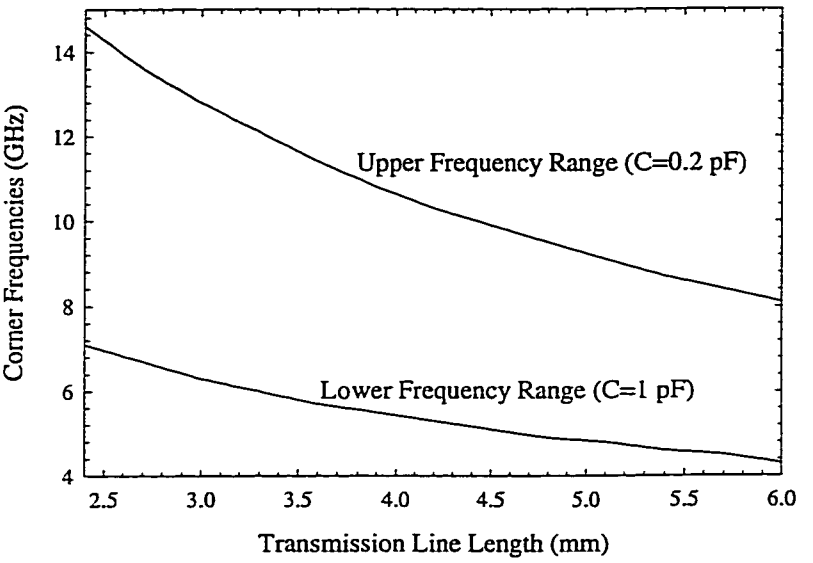


Figure 7.2: Theoretical resonant frequency tuning range for a varactor with a capacitance range of 0.2-1.0 pF as a function of transmission line physical length.

will also increase the overall resonator quality factor. An internal impedance of 60 Ω was chosen. This is a relatively low impedance line while still maintaining a reasonable conductor width.

The resonant frequency (equation 7.3) was solved graphically for the upper and lower tuned center frequencies as a function of physical length of the transmission lines assuming a varactor with a capacitance range of 0.2-1.0 pF (Fig. 7.2). This is a typical varactor value for an X-Band tunable filter. This can be scaled in frequency by the transmission line physical length and the capacitance value. According to Fig. 7.2, the length of the transmission line segment should be as short as possible for the widest tuning range. However, the series resistance of the varactor has a stronger influence on the quality factor of the resonators as the transmission line section decreases.

The quality factor of the resonant fingers is a function of the intrinsic impedance, the line length, the attenuation of the line, and the series resistance of the varactor.

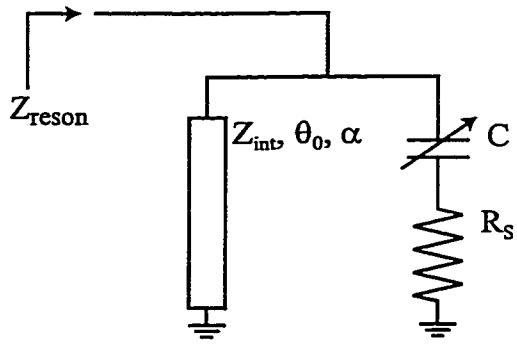


Figure 7.3: Model of a varactor loaded transmission line resonator.

The resonator can be viewed as a short transmission line in parallel with a varactor to ground as in Fig. 7.2 where R_s is the series resistance of the varactor and α is the loss of the transmission line. The input impedance of the shorted transmission line alone is:

$$Z_{line} = Z_{int}\frac{\tanh(\alpha l) + j\tan(\beta l)}{1 + j\tan(\beta l)\tanh(\alpha l)} \tag{7.4}$$

The input impedance of the varactor alone including the series resistance is:

$$Z_{cap} = \frac{1}{j\omega C} + R_s \tag{7.5}$$

$$= -j\frac{\omega_0}{\omega}Z_{int}\tan\theta + R_s \tag{7.6}$$

The total impedance can be found by taking the parallel combination. The 3 dB bandwidth can be determined by finding the bandwidth where the magnitude of the impedance falls by a factor of $\sqrt{2}$ giving the reciprocal of the overall resonator unloaded quality factor[1]. As the filter tunes, the electrical length of the transmission line changes altering the quality factor of the resonator. Fig. 7.2 shows the resulting quality factor of the resonator as a function of resonator electrical length for different values of transmission line quality factor and different values of varactor series

[1]The overall resonator unloaded quality factor is defined as the unloaded quality factor of the transmission line loaded with the varactor. The "unloaded" term is to refer to zero "external" loading where the varactor is clearly part of the overall resonator.

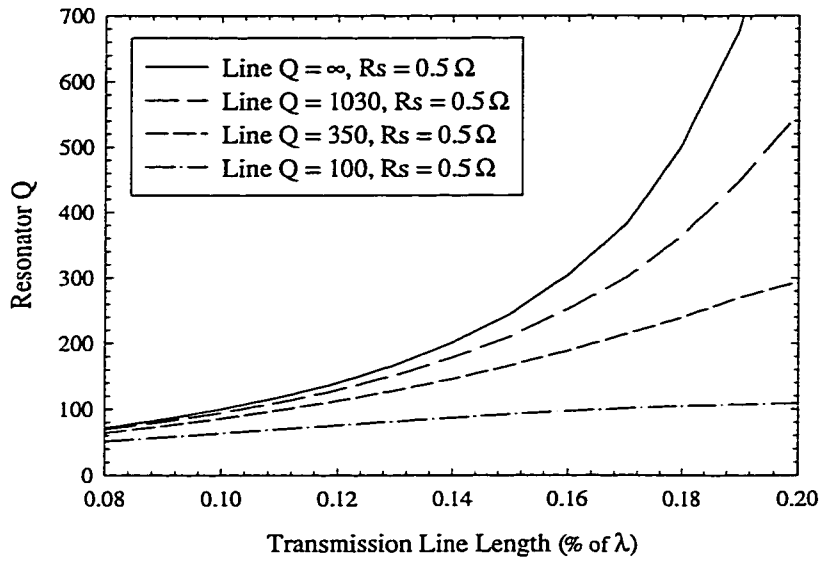
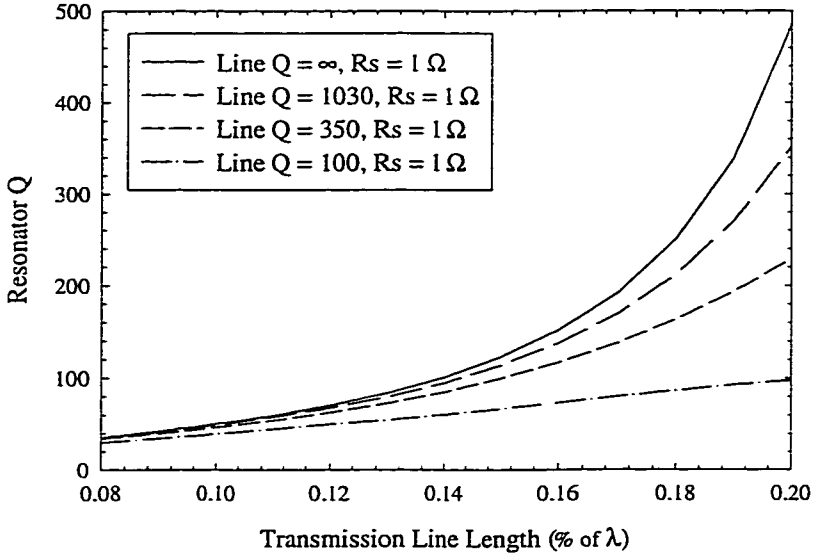
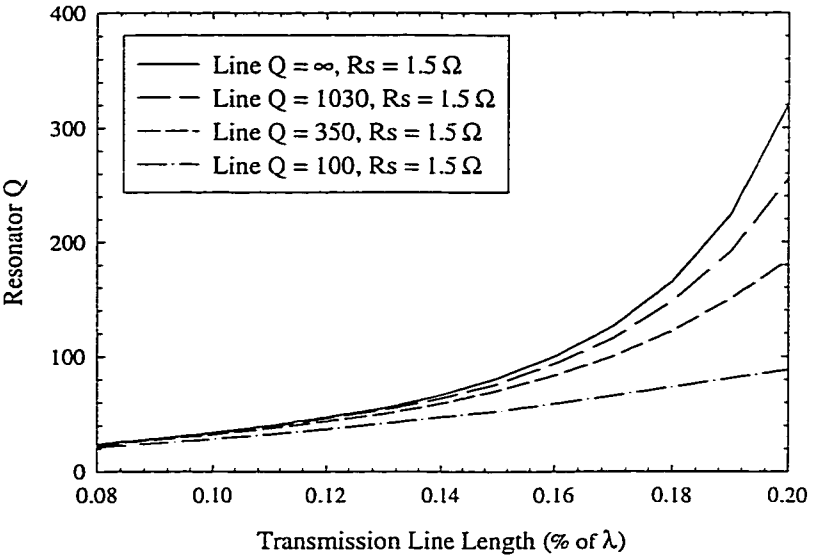


Figure 7.4: Overall resonator unloaded quality factor as a function of transmission line length in terms of λ for varying transmission line quality factors for Rs=0.5 Ω.

resistance. As the transmission line becomes electrically small, the Q of the transmission line has a decreasing effect. For wavelengths where the line is less than 0.1λ, the unloaded quality factor of the transmission line is not significant, and the varactor series resistance controls the resonator quality factor. As the transmission line portion becomes electrically longer, the overall resonator quality factor is strongly dependent on the transmission line unloaded quality factor, showing the advantages of the micromachined transmission lines. However, this comes at the expense of the tuning range. Based on equations 7.3, the tuning range for a given capacitance ratio decreases considerably with increasing electrical length.

The calculation of the inter-resonator couplings and the impedance transformers are frequency specific. For the coupling analysis, it is necessary to define a center tuning frequency, f_0. The transmission line segments will be referred to in terms of a percentage of λ_0 with electrical length of θ_0 at f_0. The electrical length of the resonators was chosen to be $0.13\lambda_0$ ($\theta_0 = 46.8°$) at the design frequency. This is a balance on very wide tuning range and resonator quality factor at f_0. The values of





(b)

Figure 7.5: Overall resonator unloaded quality factor as a function of transmission line length in terms of λ for varying transmission line quality factors for (a) Rs=1 Ω, and (b) Rs=1.5 Ω.

the overall resonator unloaded quality factor at f_0 as a function of series resistance and the quality factor of the transmission line is shown in Fig. 7.2.

For a transmission line of electrical length θ_0, loaded by a diode of capacitance C_{var} as defined in equation 7.2, with intrinsic admittance of Y_{ak}, the admittance of the transmission at the open end is:

$$Y_{line} = -jY_{ak}\cot(\theta_0\omega/\omega_0) \tag{7.7}$$

The admittance of the varactor capacitance is:

$$Y_{var} = j\omega C_{var} \tag{7.8}$$

$$= jY_{aj}\frac{\omega}{\omega_0}\cot\theta_0 \tag{7.9}$$

This is a shunt reactance that is purely imaginary. Therefore, the susceptance of the k^{th}, B_k, element is:

$$B_k(\omega) = Y_{ak}\left[\frac{\omega}{\omega_0}\cot\theta_0 - \cot(\theta_0\omega/\omega_0)\right] \tag{7.10}$$

The normalized susceptance slope of the resonator at resonance, b_k/Y_a, is:

$$\frac{b_k}{Y_a}|_{k=\text{ 1 to n}} = \frac{1}{Y_a}\frac{\omega_0}{2}\frac{dB_j(\omega)}{d\omega}|_{\omega=\omega_0} \tag{7.11}$$

$$= \frac{Y_{ak}}{Y_a}\left(\frac{\cot\theta_0 + \theta_0\csc^2\theta_0}{2}\right) \tag{7.12}$$

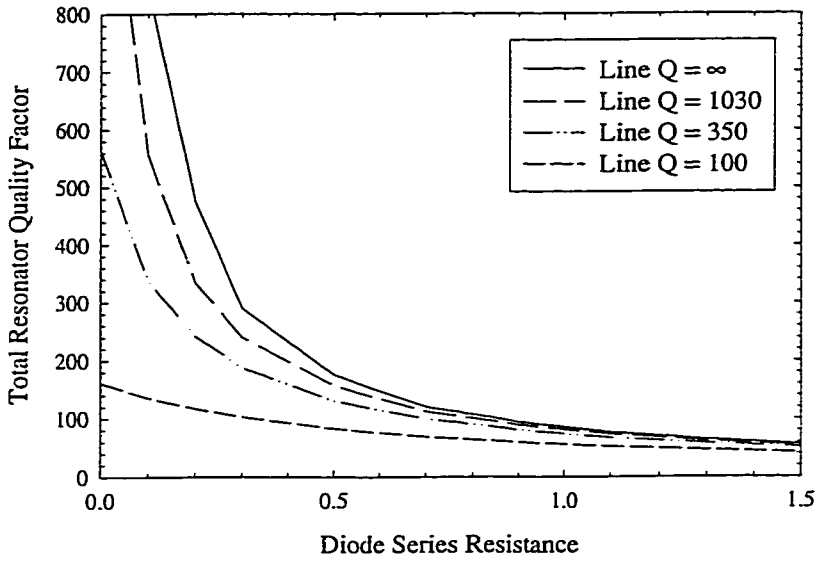
From the susceptance slope, the normalized admittance inverters are:

$$\frac{J_{0,1}}{Y_a} = \frac{\bar{\omega}\frac{b_1}{Y_a}}{g_0 g_1 \omega_1'} \tag{7.13}$$

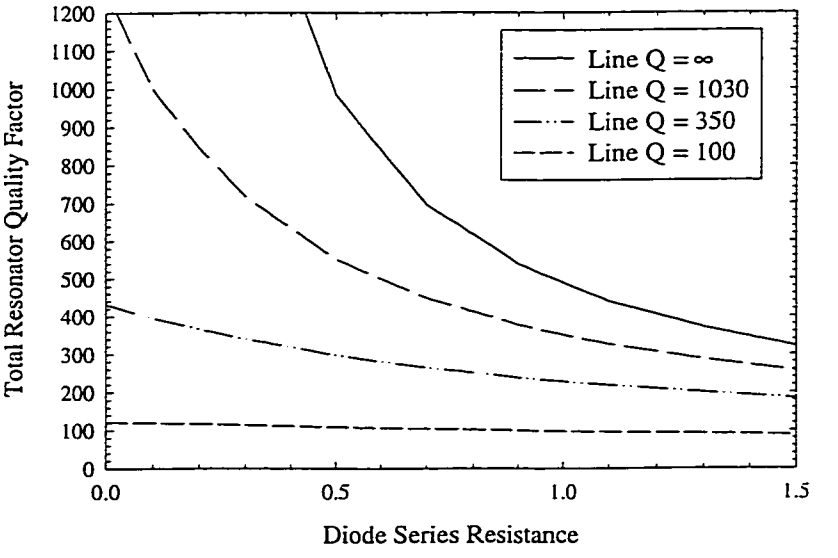
$$\frac{J_{k,k+1}}{Y_a}|_{j=\text{ 1 to n-1}} = \frac{\bar{\omega}}{\omega_1'}\sqrt{\frac{(b_k/Y_a)(b_{k+1}/Y_a)}{g_k g_{k+1}}} \tag{7.14}$$

$$\frac{J_{n,n+1}}{Y_a} = \frac{\bar{\omega}\frac{b_n}{Y_a}}{g_n g_{n+1}\omega_1'} \tag{7.15}$$

The J-inverters are then converted to capacitance from each resonator to ground, C_k, and capacitance and mutual capacitance between adjacent lines, $C_{k,k+1}$. The design process used for the tunable interdigital filter did not take into account the coupling



(a)



(b)

Figure 7.6: Overall resonator unloaded quality factor as a function of the Q of the transmission line and series resistance of the varactor for $Z_{int} = 60\ \Omega$ and the electrical length is (a) 0.13 λ_0 and (b) 0.20 λ_0.

between non-adjacent elements. The self capacitance from the resonators to ground are:

$$\frac{C_0}{\epsilon} = \frac{\eta_0 Y_a}{\sqrt{\epsilon_r}}\left(1 - \sqrt{\frac{J_{0,1}}{Y_a}}\right) \tag{7.16}$$

$$\frac{C_1}{\epsilon} = \frac{\eta_0 Y_a}{\sqrt{\epsilon_r}}\left(\frac{Y_{a1}}{Y_a} - 1 + \frac{J_{0,1}}{Y_a} - \frac{J_{1,2}}{Y_a}\tan\theta_0\right) + \frac{C_0}{\epsilon} \tag{7.17}$$

$$\frac{C_k}{\epsilon}|_{k=2 \text{ to n-1}} = \frac{\eta_0 Y_a}{\sqrt{\epsilon_r}}\left(\frac{Y_{ak}}{Y_a} - 1 + \frac{J_{k-1,k}}{Y_a} - \frac{J_{k,k+1}}{Y_a}\tan\theta_0\right) \tag{7.18}$$

$$\frac{C_n}{\epsilon} = \frac{\eta_0 Y_a}{\sqrt{\epsilon_r}}\left(\frac{Y_{an}}{Y_a} - 1 + \frac{J_{n,n+1}}{Y_a} - \frac{J_{n-1,n}}{Y_a}\tan\theta_0\right) + \frac{C_n + 1}{\epsilon} \tag{7.19}$$

$$\frac{C_{n+1}}{\epsilon} = \frac{\eta_0 Y_a}{\sqrt{\epsilon_r}}\left(1 - \sqrt{\frac{J_{n,n+1}}{Y_a}}\right) \tag{7.20}$$

where η_0 is the intrinsic impedance of air and ϵ_r is the relative dielectric constant of the medium. The normalized mutual capacitances are:

$$\frac{C_{0,1}}{\epsilon} = \frac{\eta_0 Y_a}{\sqrt{\epsilon_r}} - \frac{C_0}{\epsilon} \tag{7.21}$$

$$\frac{C_{k,k+1}}{\epsilon}|_{k=1 \text{ to n-1}} = \frac{\eta_0 Y_a}{\sqrt{\epsilon_r}}\left(\frac{J_{k,k+1}}{Y_a}\tan\theta_0\right) \tag{7.22}$$

$$\frac{C_{n,n+1}}{\epsilon} = \frac{\eta_0 Y_a}{\sqrt{\epsilon_r}} - \frac{C_{n+1}}{\epsilon} \tag{7.23}$$

From the ideal self and mutual capacitance per unit length, the separation between fingers can be calculated in a similar way as the interdigital filters presented in the preceding chapter.

7.3 RF Tunable Filter

The RF tunable filter was fabricated on 127 μm RT/Duroid [2] with a dielectric constant of 2.2 to suspend the circuit. The circuit was suspended over an aluminum cavity that is the same dimension of the filter to simulated the effect of a micromachined cavity. The depth of the cavity was 4 mm with an attached 4 mm top shielding cover. The finger length is 0.13λ at 1.25 GHz (3.1 cm) with an internal impedance of

[2]RT/Duroid is a product of Rogers Corporation, Rogers, CT.

60 Ω and a filter bandwidth of 16% with a ripple of 0.2 dB. The line widths and gaps were calculated from the equations above and are summarized in the Table 7.1 where w_k is the width of the k^{th} filter finger and $g_{k-1,k}$ is the gap between fingers $k-1$ and k. The quality factor of stripline transmission lines is 1030 at 1.25 GHz.

Table 7.1: RF Tunable Filter Finger Dimensions

Finger, k	w_k	$g_{k-1,k}$
0	9.63 mm	
1	5.97 mm	0.25 mm
2	7.11 mm	2.87 mm
3	7.11 mm	3.51 mm
4	5.97 mm	2.87 mm
5	9.63 mm	0.25 mm

The varactors are BB811 RF Variable Capacitance Diodes [3] with a series resistance of about 1 Ω and a junction capacitance from 1 pF to 8.8 pF over a 30 V bias range[4]. The varactors are biased equally with a 75 pF capacitor from the bias line to ground to provide an RF short for the varactor and an open circuit for the bias (see Fig. 7.2). The predicted tuning range is from 660 MHz to 1.6 GHz (83% tuning range) with all varactors biased equally in parallel (Fig. 7.7).

The measured response of the filter showed a 60% tuning bandwidth from 700 MHz to 1.33 GHz (Fig. 7.8). The filter input matching is good with a return loss of better than -10 dB over the tuning range up to 1.3 GHz. At center frequencies below 1 GHz, the bandwidth is reduced and the insertion loss increases. The reduced bandwidth is due to the bandwidth of the impedance inverter network of coupled lines. The

[3]BB811 RF Variable Capacitance Diodes are a product of Phillips Semiconductor, Sunnyville, CA.

[4]Device parameters based on manufacturer supplied data.

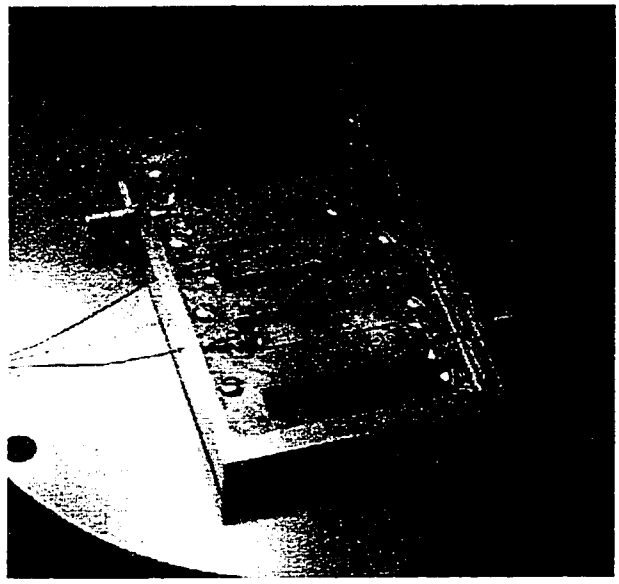


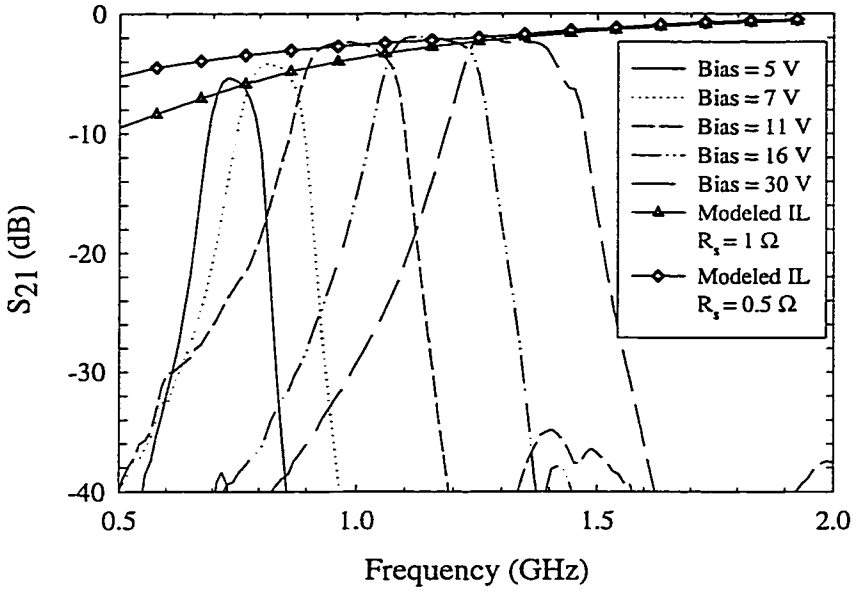
Figure 7.7: The RF varactor tuned bandpass filter.

increase in insertion loss at the low end of the tuning range is due to the decrease in overall resonator quality factor as the electrical length of the transmission line portion becomes shorter.

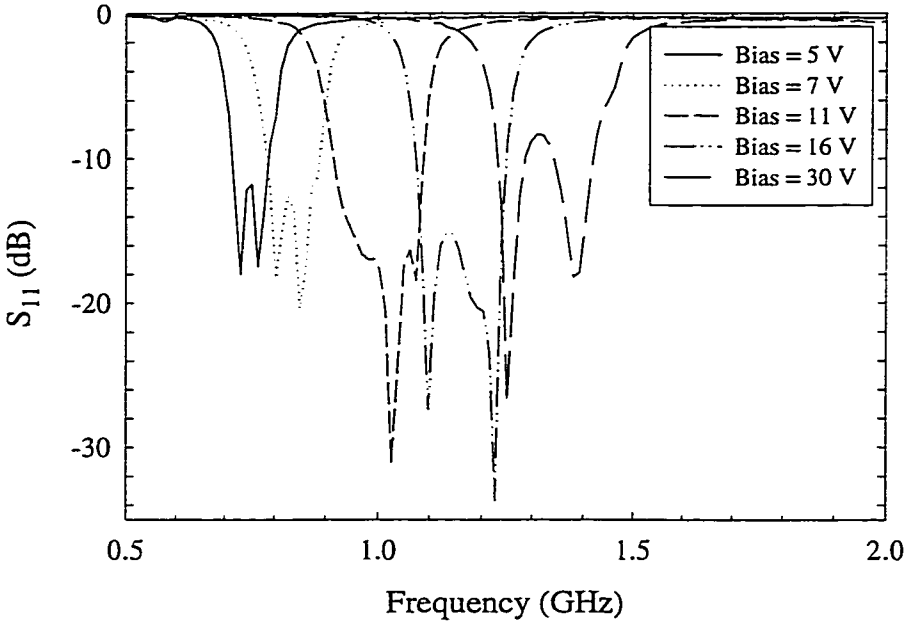
The theoretical insertion loss assuming a 16% bandwidth, 0.2 dB ripple Chebyshev 4-pole filter was calculated based on the modeled resonator quality factor with a varactor series resistance of 0.5 Ω and 1 Ω from Fig. 7.2 and is plotted on Fig. 7.8a. There is a good agreement with measured and calculated insertion loss. For center frequencies above 1 GHz, the insertion loss is less than 3 dB in the passband. The series resistance of the varactor diode is the major limiting factor in filter the insertion loss. Still, the tuned RF filter performance is comparable to state-of-the-art YIG and mechanically tuned filters at only a fraction of the material and assembly cost.

7.4 X-Band Tunable Filter

A micromachined tunable filter was fabricated on silicon using standard membrane technology [12]. The filter is based on an 8× scaling of the RF tunable filter presented



(a)



(b)

Figure 7.8: RF tunable filter measured (a) insertion loss and (b) return loss for various bias levels.

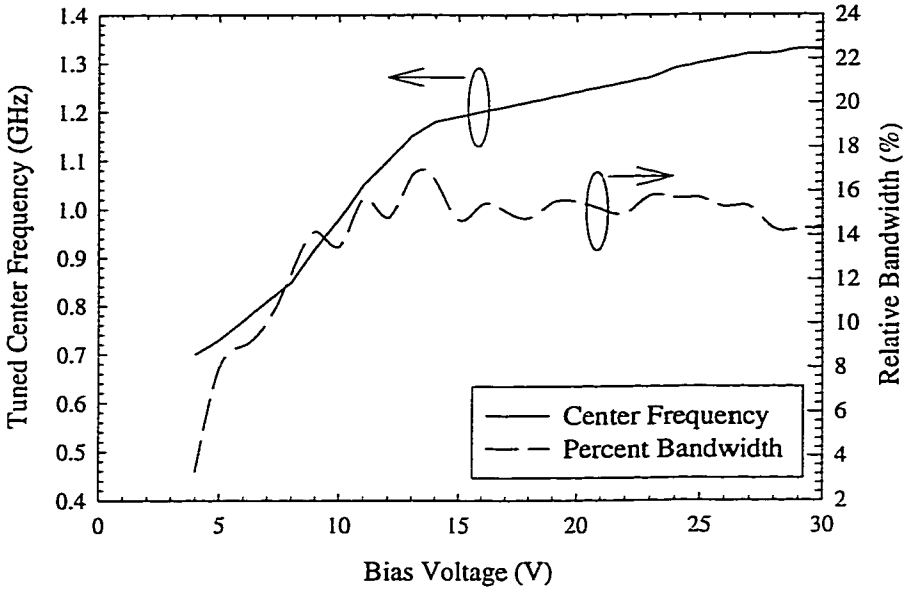


Figure 7.9: Measured center frequency and relative bandwidth as a function of bias voltage.

in the previous section. The finger lengths are 0.13λ at 10 GHz (3.9 mm) with an internal impedance of 60 Ω and a designed filter bandwidth of 10% with 0.2 dB ripple. The line widths and gaps are given in Table 7.2 where w_k is the width of the k^{th} filter finger and $g_{k-1,k}$ is the gap between fingers $k-1$ and k. The quality factor of the micromachined transmission line is 350 at 10 GHz.

The varactors were biased by breaking the ground plane with a thin slit and applying the DC bias through an external bias-T (Fig. 7.10). This raised the DC potential on one half of the circuit to the bias voltage while the other half of the circuit was DC grounded. The ground plane was broken again around the port where the bias was not applied. This prevented the bias from shorting out from the ground loop through the probes to the network analyzer. A polyimide film (Pyralin PI-2545[5]) was used to coat the circuit to prevent the top cavity from shorting out the bias and providing a higher capacitance across the break in the ground plane. The polyimide was 2.4 μm thick with a relative dielectric constant of 3.5. The polyimide film was

[5]PI-2545 is a product of DuPont Company, Semiconductor Materials, Wilmington, DE.

Table 7.2: X-Band Tunable Filter Finger Dimensions

Finger, k	w_k	$g_{k-1,k}$
0	1205 μm	
1	745 μm	31 μm
2	890 μm	360 μm
3	890 μm	440 μm
4	745 μm	360 μm
5	1205 μm	31 μm

deposited after the bulk micromachining since it dissolves in the etchant (TMAH). Capacitors (100 pF MCC50-100H[6] silicon MIM chip capacitors) were used to short the slit at 10 GHz and to prevent any slotline mode propagation. The X-band varactors are MA46580[7] beam lead varactors with capacitance values of 0.1 pF to 1.1 pF for an 18 V tuning range and a series resistance of about 1.5 Ω. The predicted tuning range is from 5.3 GHz to 12.8 GHz. The total area of the filter is 12.1 mm $\times$ 7.5 mm $\times$ 1 mm which is considerably smaller than a YIG-filter of similar specifications.

The X-band tunable filters were measured from 2-16 GHz using an HP 8510C Network analyzer. A Short-Open-Load-Through calibration method was used with 150 μm pitch Picoprobes and a CS-5 calibration substrate [8]. The varactors were measured to have a capacitance variation of 1.8 pF to 0.18 pF. The measured tuning range was approximately from 5.5 GHz to 10.5 GHz with an insertion loss of about 5 dB (Fig. 7.12). The tuning range was limited by varactor capacitance not tuning below 0.18 pF.

The insertion loss is higher than the 1.25 GHz filter due to the increase in series resistance of the varactors and a decrease in the transmission line Q. The theoretical insertion loss assuming a 10% bandwidth, 0.2 dB ripple Chebyshev 4-pole filter was calculated based on the modeled resonator quality factor from Fig. 7.2 and is plotted

[6]The MCC50-100H capacitor is a product of Metelics, Sunnyvale, CA
[7]MA46580 Varactors are a product of M/A-Com, Inc., Burlington, MA.
[8]Picoprobe and CS-5 are products of GGB Industries, Inc., Naples, FL.

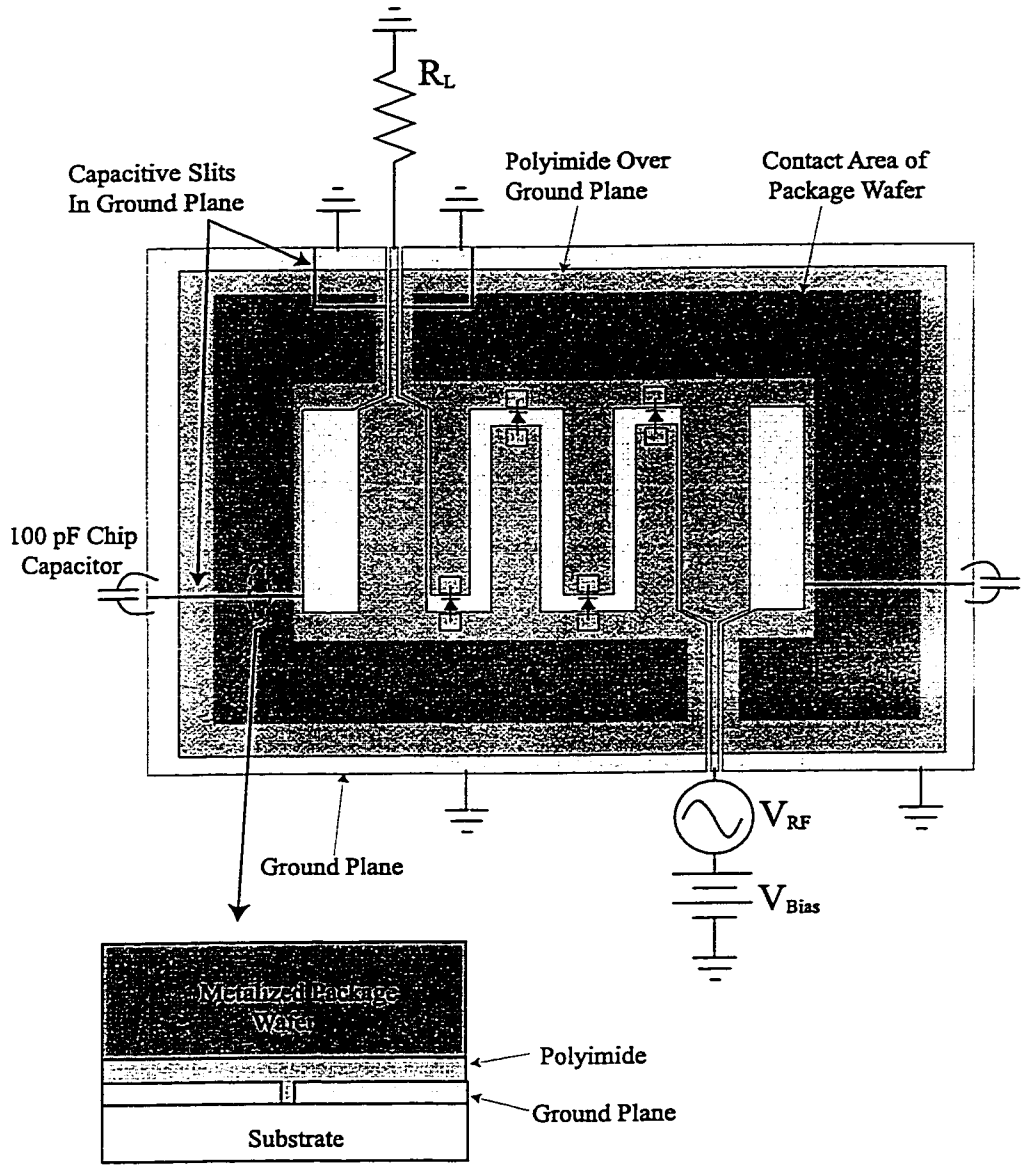


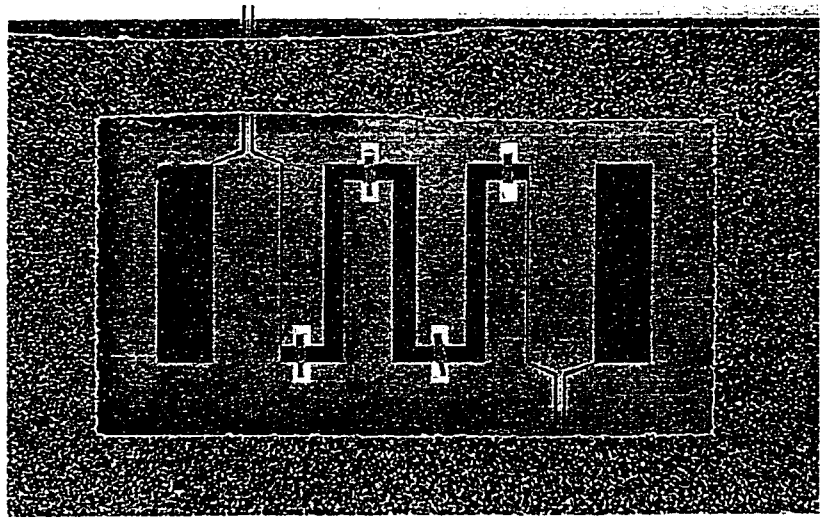
Figure 7.10: Schematic of microwave tunable filter with bias breaks.

on Fig. 7.12. There is a good agreement with measured and calculated insertion loss. This also includes 0.4 dB of loss in each feed line giving an additional 0.8 dB of attenuation. The port-to-port total attenuation is 4.7 dB and agrees well with measurements at 10-11 GHz. The degradation of the out of band rejection is due to the lower Q and also from the upper cavity not having a direct contact with the ground. This also changes the filter from the designed filter prototype performance and the calculated insertion loss deviates considerably at the lower frequency end. In future designs, MMIC capacitors should be used for biasing the varactors allowing for better grounding of the top and bottom ground planes of the stripline structure.

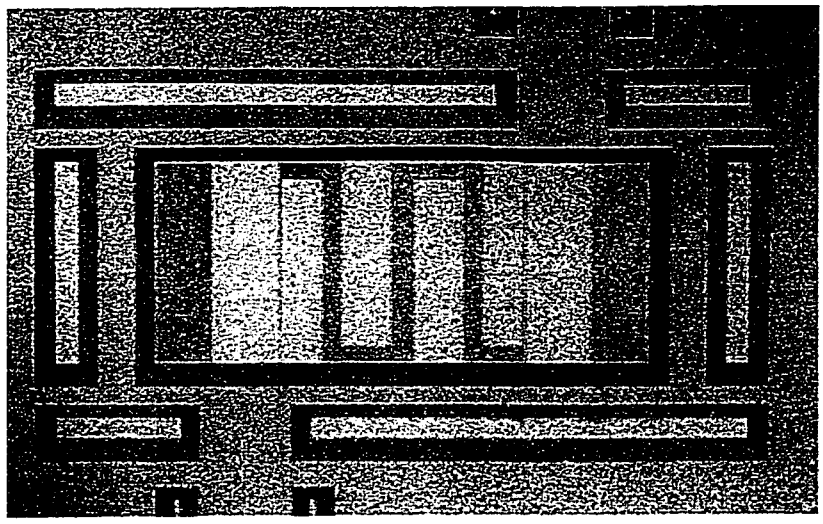
7.5 Conclusion

A wideband tunable filter was designed and fabricated. The RF tunable filter has over a 60% measured tuning range range from 700 MHz to 1.33 GHz. Over the range of 900 MHz to 1.33 GHz, the insertion loss is better than 3 dB. At a lower tuning range, the insertion loss increases due to the series resistance of the varactor diode. This is competitive in performance with YIG components with a much simpler design and fabrication and requires no tuning.

The tunable filter was scaled to X-band and fabricated using membrane suspended microstrip lines. However, the series resistance of the varactor diodes was higher for this filter, thereby limiting its performance. The measured tuning range is 5.5-10.5 GHz (62.5%) with an insertion loss ranging from 7 to 5 dB depending on the tuning frequency. This can be greatly improved by using varactor diodes with a lower series resistance.

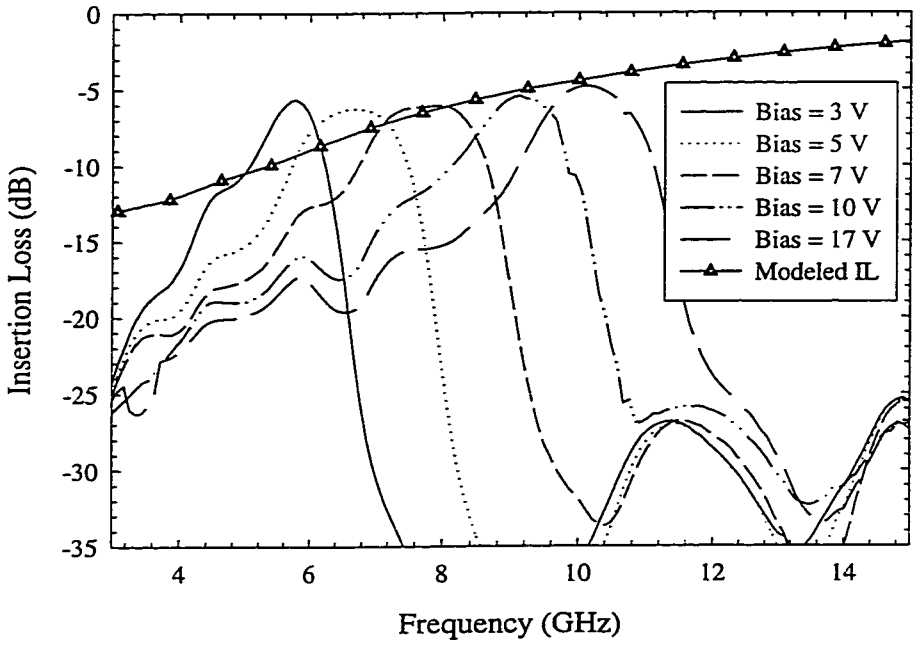


(a)

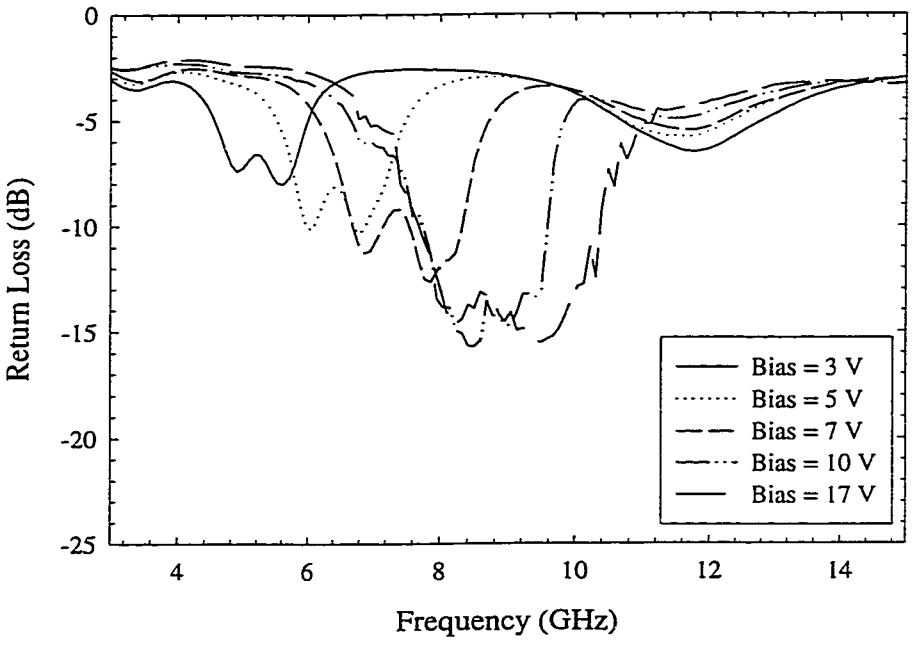


(b)

Figure 7.11: (a) Partially assembled tunable microwave filter, (b) backside of tunable filter.



(a)



(b)

Figure 7.12: Measured X-band tunable filter (a) insertion loss and (b) return loss.

CHAPTER 8

CONCLUSIONS AND FUTURE WORK

This thesis presented alternative methods of implementing high-Q components in a compact, planar fashion by using micromachining techniques have been presented. While this method does not achieve the high levels of performance of full height waveguides or dielectric resonators, it does offer very good performance with advantages in that it is planar and compact, it is compatible with standard processing techniques, offers very high alignment, and can be fabricated in large quantities without the need for manual tuning and difficult assembly.

8.1 Receiver on a Chip

The so-called "receiver on a chip" was dubbed the "Holy Grail" in the Advanced Program for the 1999 International Symposium on Microwave Theory and Techniques. Integrating a single substrate receiver on a chip poses many challenges in circuit design, process compatibility, packaging, and architecture. Each subsystem typically requires its own optimized process. For millimeter-wave applications, this idea may not be economically feasible for full system integration. Since GaAs devices are necessary for much of the system electronics (LNA, PA, mixers, etc.), it is not practical to attempt to integrate all of the large passive structures on a single GaAs substrate.

However, full front-end integration on a micromachined, micropackaged module is possible.

State-of-the-art mixer and amplifiers have been demonstrated using flip-chip active devices mounted on silicon and ceramic substrates [70], [71], [72]. The flip-chip active components can be integrated with the high-Q micromachined components presented in this thesis. In addition, much work has been done in using micromachining for high-efficiency antennas. Micromachined high-efficiency integrated antennas have been demonstrated by Gauthier, et al. [73] and Ellis, et al. [74] with planar antennas integrated on silicon with efficiencies of 85%. The method used by [73] is a volumetric reduction of the effective dielectric constant of the substrate by etching away selected portions under a microstrip patch antenna. By reducing the effective dielectric constant from that of silicon down to 2.9, the radiation efficiency was increased from 58% to 85%. Another approach was used by [74] where there was a volumetric effect of reducing the dielectric constant, but by placing holes in a specific orientation and lattice dimension, there was a further reduction of substrate modes. For the case of a tapered slot antenna, the measured improvement in efficiency is from 30% to 85% at 10 GHz.

The entire transmit/receive module could be packaged together on the same substrate in order to ensure low cost production. This is the most critical aspect of the front-end, and it is expected that the front-end layout must ensure a minimum of -70 dB coupling between the transmit and receive channels for proper operation of the low noise receiver. This cannot be done in normal microstrip or CPW lines integrated on teflon substrates and placed in a large cavity. However, with silicon micromachining, it is possible to integrate a micro-shield around each component to ensure no radiation and cross coupling. Rejection of -70 to -80 dB has been demonstrated on a single substrate at 30 GHz (See Section 4.2.1) by using micropackaging techniques.

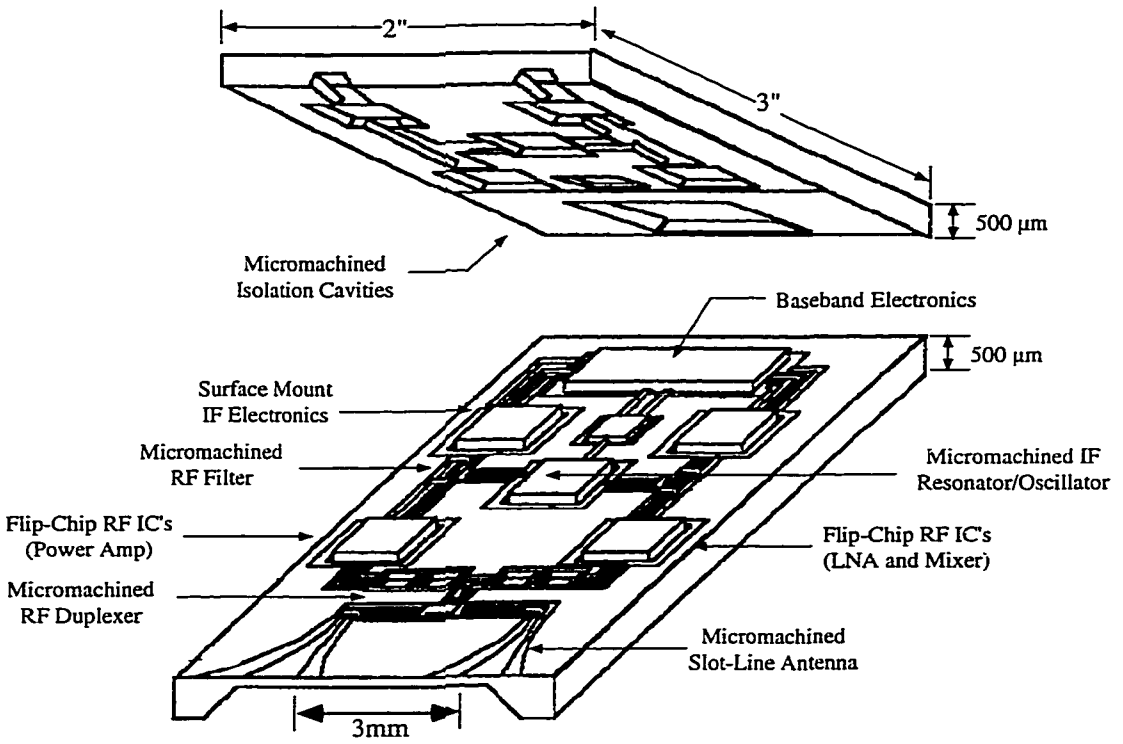


Figure 8.1: Conceptual design of 28 GHz integrated transmit/receive module.

By combining the previously done work in flip-chip circuit design, high-Q micromachined components, micromachined high-efficiency antennas, and micropackaging, a "receiver on a substrate" is possible. Fig. 8.1 depicts a conceptual design the micromachined/micropackaged integrated receiver.

8.2 MEMS Varactors for Frequency Tuning

Microelectromechanical system (MEMS) have recently been developed for low-loss microwave and millimeter-wave switches and phase shifters [75], [76]. The switches and phase shifters consist of a metal bridge suspended above a transmission line. When a bias is applied between the signal line and the bridge, electrostatic forces pulls the bridge closer to the transmission line increasing the capacitance. The bridge can be implemented as a fixed-fixed bridge (similar to an air-bridged) or as a cantilever

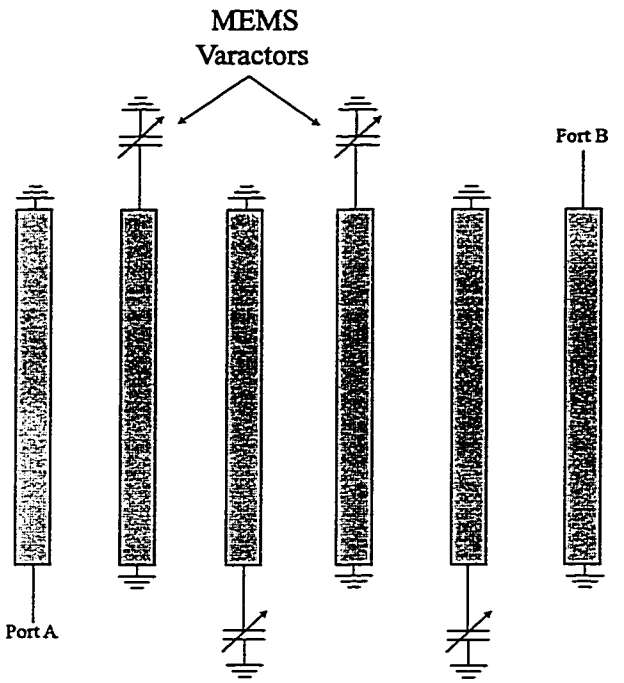


Figure 8.2: Tunable bandpass filter with MEMS varactors

beam. For applied bias below the pull-down voltage of the beam, the bridge acts as a voltage controlled variable capacitance. The advantage that a MEMS varactor has over a solid state varactor diode is that the series resistance is the resistance of the beam itself, and is much less than a varactor diode.

The MEMS varactor could be applied to the micromachined tunable filter (Fig. 8.2). As with the tunable interdigital filter in Chapter 7, varactors load the resonators to tune their resonant frequency. In order to obtain the large values of capacitance needed for this filter (0.1-2 pF), a wide cantilever beam could be used. This would result in wide beams with very low Ohmic loss. As shown in Chapter 6, the insertion loss of the tunable filter is a strong function of the series resistance of the varactor. Using a MEMS varactor, this series resistance is greatly reduced and would result in a very low-loss tunable filter.

The oscillator presented in Chapter 5 was a fixed frequency oscillator. This oscillator could be altered to be a voltage controlled oscillator (VCO) by using MEMS var-

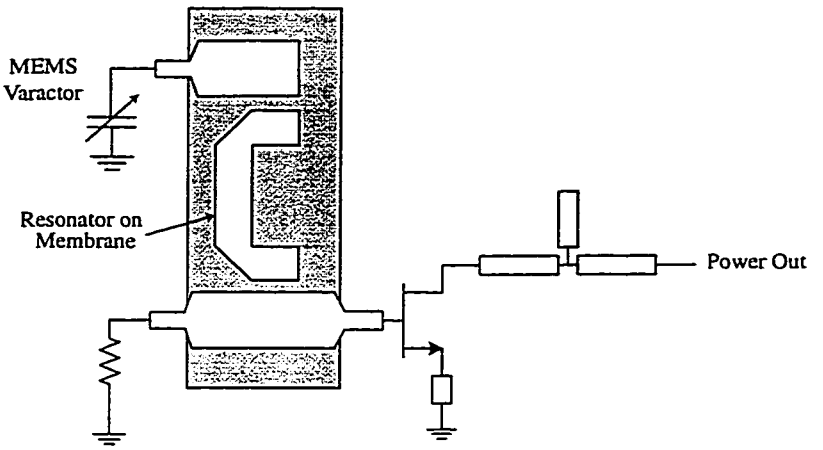


Figure 8.3: Voltage controlled oscillator using MEMS varactors

actors to tune the resonant frequency of the suspended microstrip resonator (Fig. 8.3). Conventional VCO's use varactor diodes for frequency tuning. Coupling a varactor diode to a resonator degrades the loaded quality factor of the resonator due to the series resistance of the varactor. However, with a MEMS varactor, the series resistance is considerably less, resulting in a large improvement in phase noise performance.

8.3 Push-Push Micromachined Oscillator/Doubler

The coupling structure of the micromachined oscillator presented in this thesis could easily lead into a push-push oscillator. A push-push oscillator has the effect of doubling the oscillation frequency. The transistors are coupled to a single resonator so that the phase of the voltages are 180° apart at the fundamental frequency. The outputs of the transistors are then attached in parallel in a T-junction. With a 180° phase difference between the outputs, the fundamental frequency is essentially shorted out allowing only even numbered harmonics. The most dominant even harmonic is the second harmonic [77]. A push-push oscillator has been demonstrated using a dielectric resonator [78] and could be adapted to a membrane suspended microstrip design. Such circuit could be implemented as in Fig. 8.4. The advantages of a push-

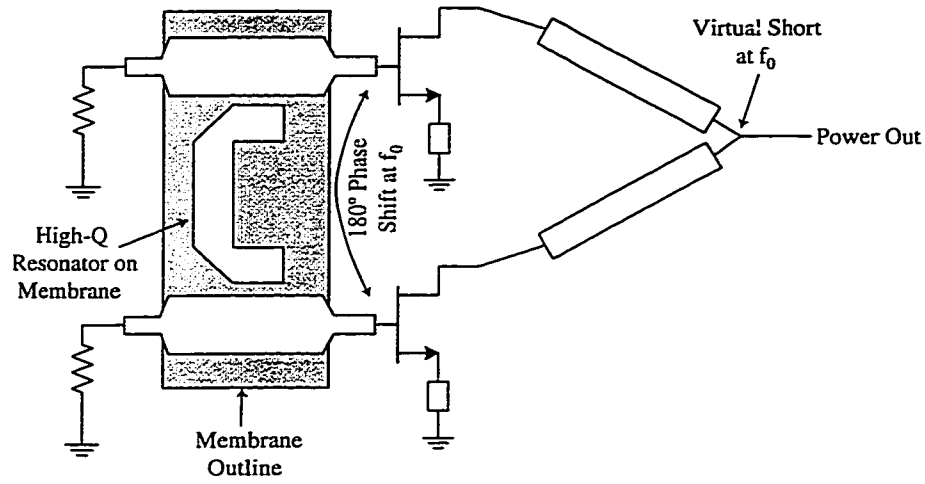
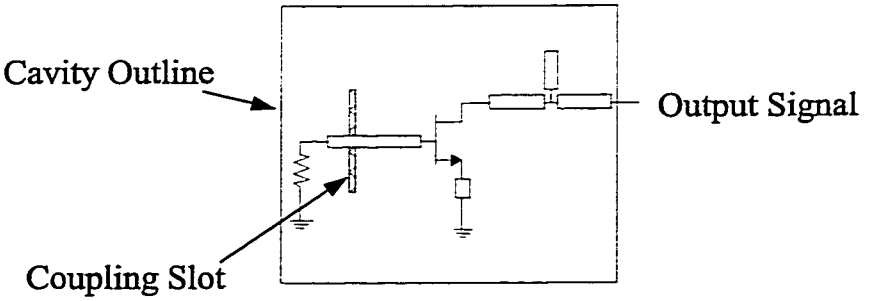


Figure 8.4: Membrane supported microstrip resonator push-push oscillator.

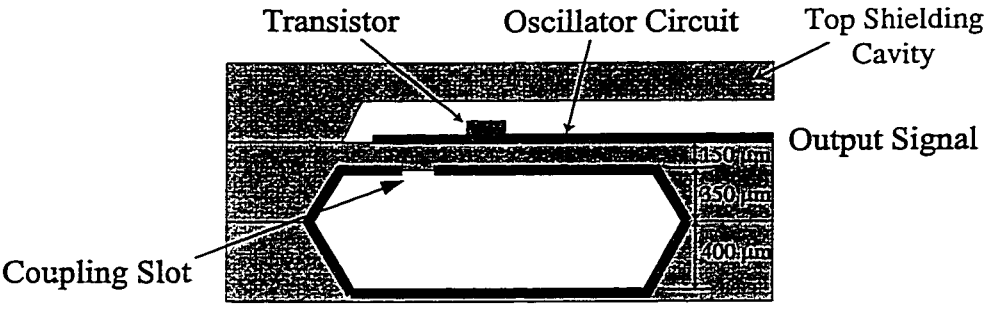
push oscillator are that a lower frequency resonator can be used with reduced effects of the silicon-to-membrane transition, and a transistor with a lower cutoff frequency can be used.

8.4 Integrated Cavity Resonator Oscillator

A similar topology used for the DRO and membrane supported microstrip resonator oscillated can be applied to the integrated cavity resonator presented in Chapter 2. This would result in a higher quality factor than the membrane supported microstrip resonator oscillator presented in Chapter 5. Rather than using wirebonds to couple to the cavity as in Section 2.5, coupling slots could be used to couple to the resonator in a bandstop configuration. This would allow the oscillator circuit to be fabricated on the top of the resonator in a microstrip configuration and couple to the cavity via a microstrip-to-slot transition (Fig. 8.4). The substrate could be locally thinned in the cavity region to increase the Q of the cavity resonator and decrease the height of the dielectric for the microstrip lines (decreasing the effects of substrate modes).



(a)



(b)

Figure 8.5: Micromachined cavity resonator oscillator (a) top view and (b) side view.

8.5 Network Analyzer Test Set on a Probe

The test set of a network analyzer determines the frequency range of the measurement setup and is the main contributor to system specifications. The purpose of the test set is to generate the RF test signal when a higher frequency is required than that supplied by the system synthesizer, switch between ports being measured, sample the input power (a-terms), sample the reflected and through power (b-terms), and mix the signals down to an IF that can be picked up by an A/D-converter (Fig. 8.5). There are many trade-offs in the performance of a test set. The true dynamic range of the network analyzer is determined by the loss of the test set, the directivity of the coupler, the loss between the test set and the calibrated reference, and the sensitivity of the A/D-converter. However, it is difficult to manufacture wideband components that are optimized in all of the above factors. For this reason, high-performance network analyzers have a different test set module for specific frequency bands. Each test set utilizes the lowest loss transmission medium that is practical to use at these frequencies (e.g., different waveguides for ranges in U, V, and W-bands as well as different coaxial lines for k-band). The test set also utilizes different couplers for each band that are optimized for high directivity.

By using micromachining techniques, it is possible to integrate a low-cost network analyzer test set module on a single substrate. Further, the CPW probe tip itself can be integrated on the same substrate. This allows for close proximity of the test set to the device under test resulting in a decrease in transmission loss and an increase in measurement dynamic range. The micromachined test set would utilize a membrane supported microstrip coupler to result in good directivity [79], and MEMS absorptive switches for high isolation, thereby providing a low-cost, high-performance solution for probe based network analyzer measurements.

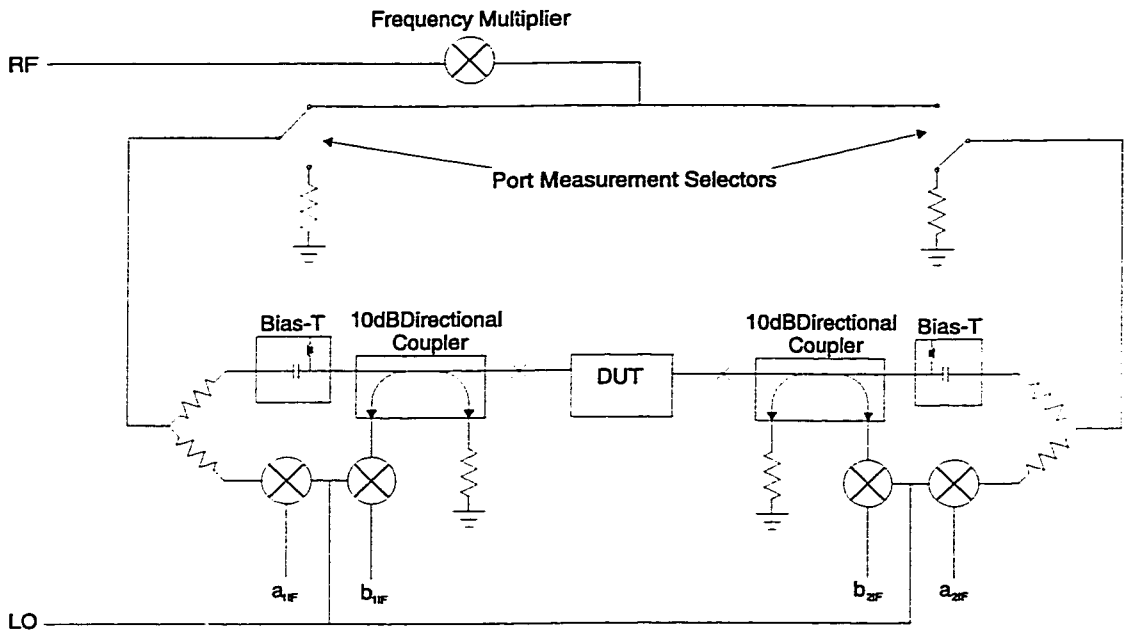


Figure 8.6: Network analyzer test set architecture.

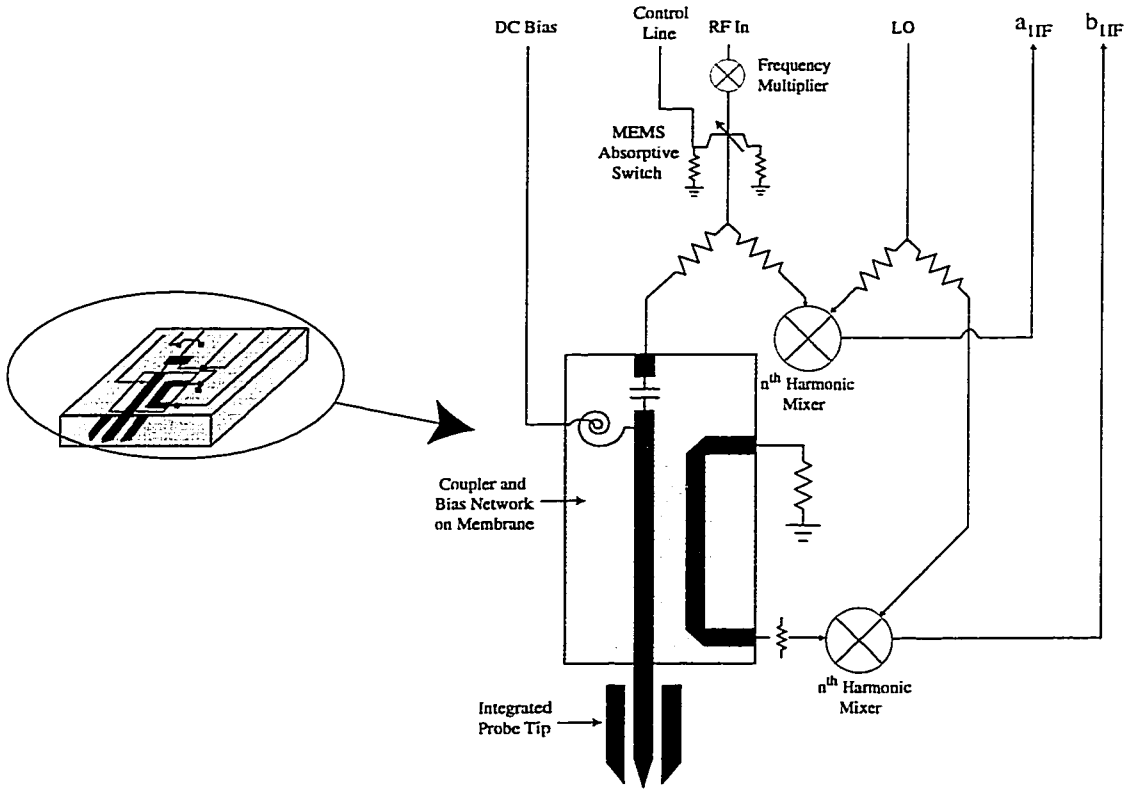


Figure 8.7: Micromachined network analyzer test set integrated on a probe.

APPENDICES

APPENDIX A

ANALYSIS OF MEMBRANE NONUNIFORM DIRECTIONAL COUPLERS

A.1 Introduction

A wideband (10-120 GHz) membrane supported microstrip coupler was demonstrated by Robertson [48] (Fig. A.1). This was based on a 20 dB nominal coupling with a Klopfenstein impedance taper [80] with a maximum ripple reflection of -30 dB. The taper is a gradual change from a very low coupling value (wide separation) to a very high coupling value (narrow separation) to give a very wideband response. Ideally, the Klopfenstein function gives a high pass response. The length of the coupler is given by the electrical length of the coupler at the lowest frequency of operation, the maximum acceptable return loss, and the value of coupling. The length of this coupler is 4.5 mm ($0.6\lambda_0$ at 10 GHz) with a port impedance of 90 Ω. The synthesis of the coupler assumes ideal coupled transmission lines since, at the time of the development of this project, there was no equivalent model for membrane suspended microstrip lines.

It has been previously observed that the effects of the dielectric membrane can be included in the design by using the already established MLIN transmission line

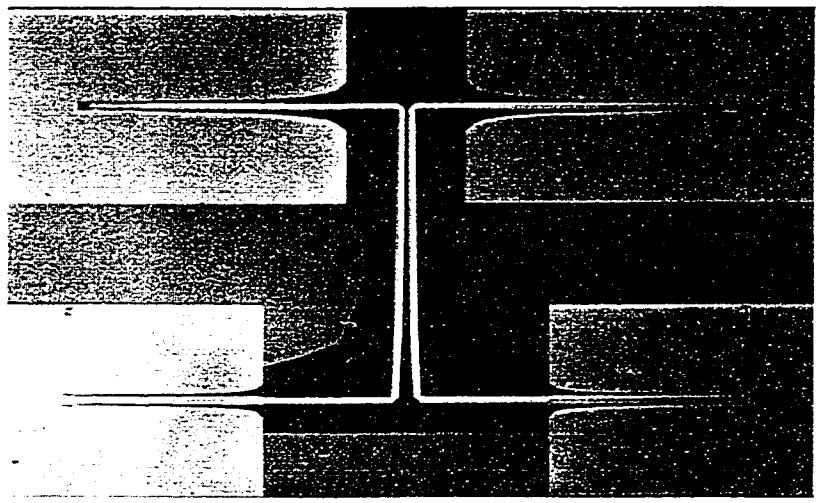


Figure A.1: Photograph of the micromachined directional coupler demonstrated by Robertson. The membrane supported region appears darker than the surrounding silicon support rim. Ports 2 and 4 are terminated with matching loads to permit coupled response measurements (Photograph courtesy of Stephen V. Robertson).

model with an assumed uniform dielectric substrate with a relative dielectric constant of 1.05. This assumption was applied to the analysis of a bandpass filter constructed of weakly coupled microstrip lines with good agreement with measurements [28]. However, the bandpass filter is not as sensitive to differences in even and odd mode phase velocities as a wideband coupler. When this method was applied to the wideband coupler, there was a large discrepancy between the measured and simulated data for the isolation term (Fig. A.2). The measured results were performed by deembedding the transition from CPW-on-silicon to microstrip-on-membrane transition, and the wideband impedance transformer from 50 to 90 Ω [48]. The large discrepancy between measured and simulated performance in the isolated port brought about a need to investigate the cause of the degradation in performance, and also a new method for accurately analyzing coupled lines on membrane for future designs. This appendix begins with analyzing a uniform coupled line with non-ideal parameters. The technique is then applied to the membrane supported microstrip lines and the nonuniform coupler. There are also recommendations for improvements for future designs.

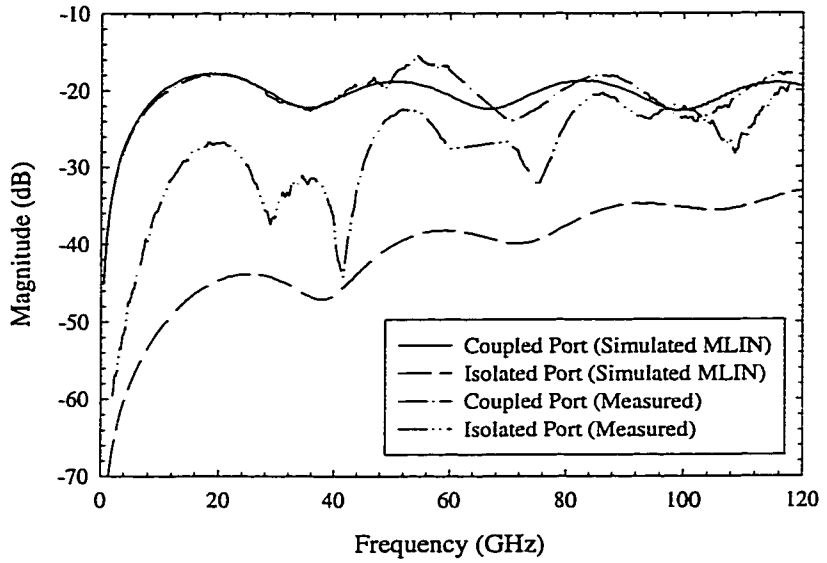
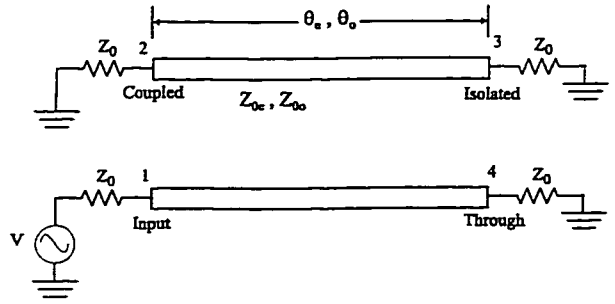


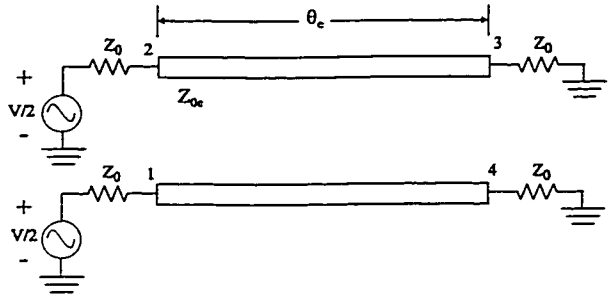
Figure A.2: Membrane supported microstrip wideband directional coupler measured and simulated (MLIN model) results.

A.2 Analysis of Edge-Coupled Membrane Suspended Microstrip Lines

For a uniform cross section of coupled lines, the non-ideal coupled transmission line parameters can be extracted by applying even/odd mode analysis (Fig. A.3). The field components for microstrip lines on a homogeneous equivalent dielectric substrate with a dielectric constant ϵ_r of 1.05, and for the actual membrane suspended lines are shown in Fig. A.4. The method of using microstrip lines on $\epsilon_r = 1.05$ was done as an approximation for matching the effective dielectric constant of a single membrane suspended line. For the case of coupled lines, this is still a reasonable approximation for the case of the even mode analysis since the majority of the electric field components follow roughly a microstrip mode. However, the odd mode field distribution presents a different problem that cannot be approximated by the conventional microstrip approximation. For the odd mode, a large portion of the electric field is parallel to the membrane. For geometries where the coupled lines are far apart, the lines are relatively decoupled and the presence of the membrane is insignificant. However, if the



(a)



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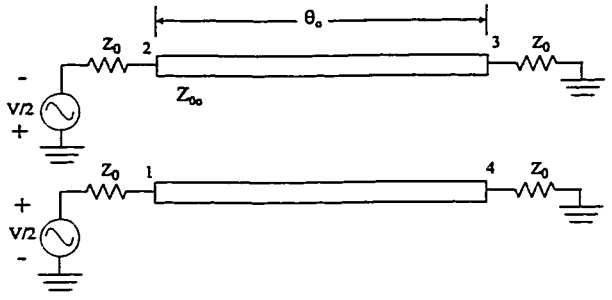


(c)

Figure A.3: Coupled lines with (a) single port excitation and decomposed into an (b) even mode component, and an (c) odd mode component.

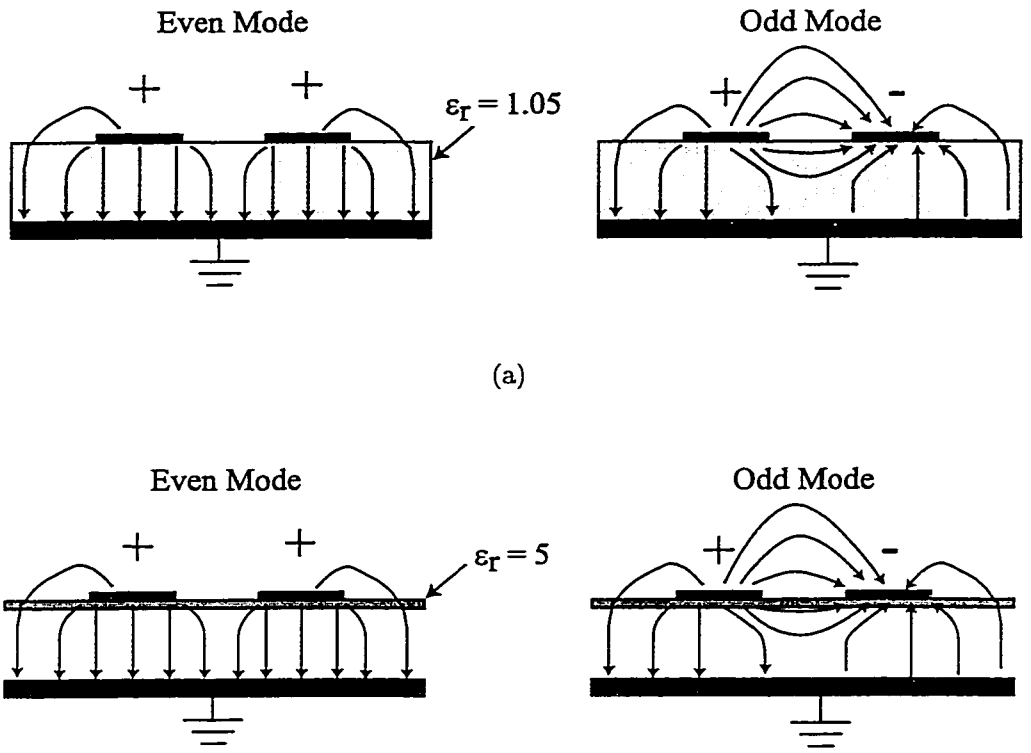


Figure A.4: Even and odd mode field configurations for (a) microstrip on low dielectric to simulated the effects of the membrane, and (b) actual membrane structure.

lines are brought closer together, the membrane becomes much more significant since a larger amount of electric field lines are in the membrane layer. Since the dielectric membrane has a much higher relative dielectric constant ($\epsilon_r = 5 - 7$), the odd mode effective dielectric constant increases and could be much higher than that of the even mode depending on the separation between the lines. This effect is not correctly modeled by the microstrip on a homogeneous dielectric of ϵ_r=1.05. Therefore, the pure microstrip on a dielectric of ϵ_r=1.05 approximation results in a high error in the even/odd mode effective dielectric constants for small gap separations.

Assuming that the coupler has an even mode intrinsic impedance and electrical length of Z_{0e} and θ_{0e}, and an odd mode intrinsic impedance and electrical length of Z_{0o} and θ_{0o}, respectively, the ABCD parameters for a section of coupled line is [81]:

$$\begin{bmatrix} V_{1e} \\ I_{1e} \end{bmatrix} = \begin{bmatrix} \cos\theta_e & jZ_{0e}\sin\theta_e \\ (j/Z_{0e})\sin\theta_e & \cos\theta_e \end{bmatrix} \begin{bmatrix} V_{4e} \\ I_{4e} \end{bmatrix} \tag{A.1}$$

$$\begin{bmatrix} V_{1o} \\ I_{1o} \end{bmatrix} = \begin{bmatrix} \cos\theta_o & jZ_{0o}\sin\theta_o \\ (j/Z_{0o})\sin\theta_o & \cos\theta_o \end{bmatrix} \begin{bmatrix} V_{4o} \\ I_{4o} \end{bmatrix} \tag{A.2}$$

where V_{1e}, I_{1e}, V_{4e} and I_{4e} are the even mode voltages and currents at ports 1 and 4. Also, V_{1o}, I_{1o}, V_{4o} and I_{4o} are the odd mode voltages and currents at ports 1 and 4. Note that this is a completely symmetric structure and it is not necessary repeat this analysis for ports 2 and 3. By inspection of Fig. A.3, the normalized voltage waves leaving the ports of the coupler are given by:

$$b_1 = \frac{1}{2}(\Gamma_e + \Gamma_o) \tag{A.3}$$

$$b_2 = \frac{1}{2}(\Gamma_e - \Gamma_o) \tag{A.4}$$

$$b_3 = \frac{1}{2}(T_e - T_o) \tag{A.5}$$

$$b_4 = \frac{1}{2}(T_e + T_o) \tag{A.6}$$

where Γ_e, Γ_o, T_e, and T_o are the even and odd mode reflection and transmission coefficients, respectively. The ABCD parameters given above are then transformed

into even and odd mode reflection and transmission coefficients. The general equation for the conversion from ABCD parameters to reflection and transmission coefficients is:

$$\Gamma_0 = \frac{A + B/Z_0 - CZ_0 - D}{A + B/Z_0 + CZ_0 + D} \tag{A.7}$$

$$T_0 = \frac{2}{A + B/Z_0 + CZ_0 + D} \tag{A.8}$$

Substituting the values of the ABCD matrix into the above equation gives:

$$\Gamma_{0e} = \frac{j[(Z_{0e}/Z_0) - (Z_0/Z_{oe})]\sin\theta_e}{2\cos\theta_e + j[(Z_{0e}/Z_0) + (Z_0/Z_{0e})]\sin\theta_e} \tag{A.9}$$

$$\Gamma_{0o} = \frac{j[(Z_{0o}/Z_0) - (Z_0/Z_{0o})]\sin\theta_o}{2\cos\theta_o + j[(Z_{0o}/Z_0) + (Z_0/Z_{0o})]\sin\theta_o} \tag{A.10}$$

$$T_{0e} = \frac{2}{2\cos\theta_e + j[(Z_{0e}/Z_0) + (Z_0/Z_{0e})]\sin\theta_e} \tag{A.11}$$

$$T_{0o} = \frac{2}{2\cos\theta_o + j[(Z_{0o}/Z_0) + (Z_0/Z_{0o})]\sin\theta_o} \tag{A.12}$$

The voltage coupling coefficient, k, is defined as the ratio of the square root of the normalized power delivered to the coupled port the that of the power incident on the coupler. Assuming that the coupler is matched ($Z_0 = \sqrt{Z_{0e}Z_{0o}}$), the coupling is:

$$k = b_2 = \frac{1}{2}(\Gamma_{0e} - \Gamma_{0o}) \tag{A.13}$$

$$= \frac{1}{2}\left(\frac{j\left[\sqrt{r} - \sqrt{1/r}\right]\sin\theta_e}{2\cos\theta_e + j\left[\sqrt{r} + \sqrt{1/r}\right]\sin\theta_e} - \frac{j\left[\sqrt{1/r} - \sqrt{r}\right]\sin\theta_o}{2\cos\theta_o + j\left[\sqrt{1/r} + \sqrt{r}\right]\sin\theta_o}\right) \tag{A.14}$$

where

$$r = \frac{Z_{0e}}{Z_{0o}} \tag{A.15}$$

The coupled port does not show a strong change in coupling as a function of $\Delta\theta$, where $\Delta\theta$ is defined as $|\theta_e - \theta_o|$. If $\theta_e = \theta_o = \pi/2$, the coupling will be referred to as k_0 where:

$$k_0 = \frac{\frac{Z_{0e}}{Z_{0o}} - 1}{\frac{Z_{0e}}{Z_{0o}} + 1} = \frac{Z_{0e} - Z_{0o}}{Z_{0e} + Z_{0o}} \tag{A.16}$$

Defining the isolation, I, as the ratio of the square root of the normalized power delivered to the isolated port, b_3 to that delivered to the through port, b_4, [81] is:

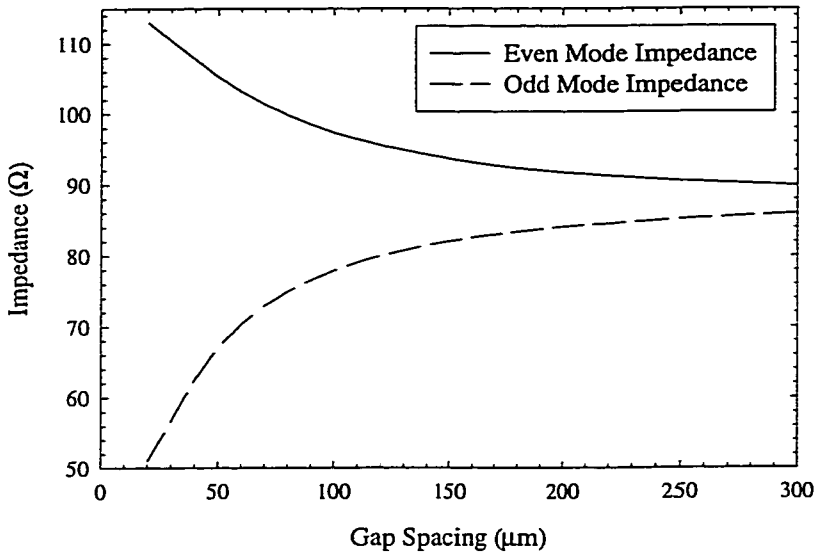
$$I = \frac{b_3}{b_4} = \frac{T_{0e} - T_{0o}}{T_{0e} + T_{0o}} \tag{A.17}$$

$$= \frac{2(\cos\theta_o - \cos\theta_e) + j(1/r + r)(\sin\theta_o - \sin\theta_e)}{2(\cos\theta_o + \cos\theta_e) + j(1/r + r)(\sin\theta_o + \sin\theta_e)} \tag{A.18}$$

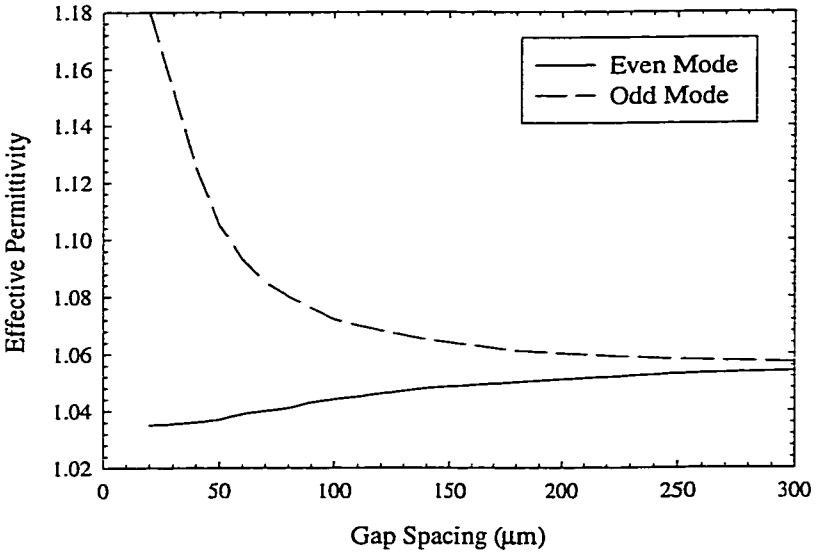
$$= \tan\left(\frac{\theta_e - \theta_o}{2}\right) \frac{2\sin[(\theta_e + \theta_o)] - j(r + 1/r)\cos[(\theta_e + \theta_o)/2]}{2\cos[(\theta_e + \theta_o)] - j(r + 1/r)\sin[(\theta_e + \theta_o)/2]} \tag{A.19}$$

The isolation of a coupler is strongly related to the difference in the even and odd mode electrical length due to the tangent term in the front of the expression, and much less sensitive to errors in the even/odd mode impedance. For short coupling sections, the difference between the even and odd mode electrical lengths are not very large. However, for long, distributed couplers such as the nonuniform membrane supported directional coupler, this phase difference is accentuated due to the long length of the coupler, especially at the higher frequencies.

In order to analyze the effects of the dielectric membrane on the effective even and odd mode phase velocity, a series of full-wave simulations were performed. The simulations used the membrane suspended microstrip with a ground plane height of 50 μm, a shielding cover height of 500 μm, and a membrane thickness of 1.4 μm with ϵ_r=5. The simulations were performed using IE3D [34], a commercial method of moments simulator. The simulations modeled various uniform lines with conductor widths, W=100 μm, and variable gap spacings, G. The isolated microstrip line impedance and effective relative dielectric constant is 85 Ω and 1.05, respectively. The simulations were all performed at 40 GHz (Fig. A.5). For a gap width below 100 μm (tight coupling), the odd mode effective dielectric constant increases considerably. This is due to more fields being confined in the dielectric membrane. The difference in effective dielectric constant results in different electrical lengths for the even and odd modes degrading the coupler isolation.



(a)



(b)

Figure A.5: Simulated even and odd mode (a) impedances and (b) effective dielectric constant for a microstrip line width of 100 μm and varying gaps on a50 μm high ground plane. Simulations were performed at 40 GHz and include the effect of the dielectric membrane.

A.3 Analysis of Wideband Nonuniform Coupler

The wideband nonuniform directional coupler can be analyzed by dividing the coupler into discrete sections and approximating the coupled lines within each section as a uniform line with a width and gap equal to the average width and gap of the nonuniform coupler within that section. For a coupler that is broken up into N sections, the $ABCD$ matrices for even and odd modes of the entire coupler are:

$$\begin{bmatrix} A_e & B_e \\ C_e & D_e \end{bmatrix} = \prod_{n=1}^{N} \begin{bmatrix} A_{en} & B_{en} \\ C_{en} & D_{en} \end{bmatrix} = \prod_{n=1}^{N} \begin{bmatrix} \cos\theta_{en} & jZ_{0en}\sin\theta_{en} \\ (j/Z_{0en})\sin\theta_{en} & \cos\theta_{en} \end{bmatrix} \tag{A.20}$$

$$\begin{bmatrix} A_o & B_o \\ C_o & D_o \end{bmatrix} = \prod_{n=1}^{N} \begin{bmatrix} A_{on} & B_{on} \\ C_{on} & D_{on} \end{bmatrix} = \prod_{n=1}^{N} \begin{bmatrix} \cos\theta_{on} & jZ_{0on}\sin\theta_{on} \\ (j/Z_{0on})\sin\theta_{on} & \cos\theta_{on} \end{bmatrix} \tag{A.21}$$

The coupler was divided into 14 sections and each section was analyzed to find the even and odd mode impedances and effective dielectric constants (Table A.1). The line lengths and effective dielectric constants are then used to find the even and odd mode electrical lengths. The coupler was then analyzed using equations A.20 and A.21 to find the total even and odd mode $ABCD$ matrices of the entire structure. The isolation can then be found from the full even and odd mode $ABCD$ matrices, and equations A.8 and A.17. The calculated isolation is shown in Fig. A.6 and compared with the measured results. The initial simulation was performed assuming matched ports, and agrees well with the average value of the measured isolation. To obtain a more accurate model, the reflection coefficient of a thin film resistor termination network was measured, and the data was added to the simulation at ports 2 and 4 as in the case of the actual measurement performed. The resulting simulation shows a very close agreement with measurements.

Table A.1: Discretized membrane supported nonuniform coupler original design dimensions with full-wave simulated values.

n	Length (μm)	Width (μm)	Gap (μm)	Z_{0e} (Ω)	Z_{0o} (Ω)	ϵ_e	ϵ_o
1	250	98	192	88.8	83.0	1.062	1.079
2	250	98	171	89.4	82.3	1.060	1.080
3	250	98	153	90.8	81.9	1.057	1.080
4	250	97	133	92.0	81.7	1.056	1.081
5	250	97	120	93.0	80.8	1.055	1.082
6	250	97	110	93.6	80.2	1.054	1.082
7	250	96	99	95.0	79.8	1.053	1.083
8	250	96	91	95.8	78.7	1.051	1.087
9	375	96	80	96.8	77.6	1.050	1.091
10	375	95	71	98.6	76.6	1.048	1.096
11	375	95	64	99.4	75.6	1.046	1.104
12	375	94	57	101.2	74.5	1.046	1.112
13	500	94	51	102.4	73.1	1.045	1.126
14	500	93	46	103.2	71.6	1.045	1.134

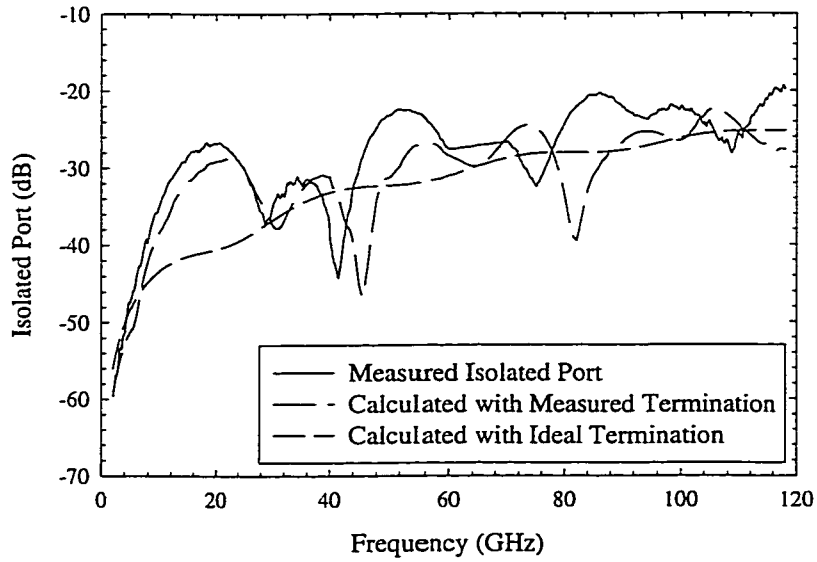


Figure A.6: Simulated coupler isolation. Simulations performed by discretizing the coupler into 14 segments and finding the even/odd mode impedances and effective dielectric constants using a method of moments tool.

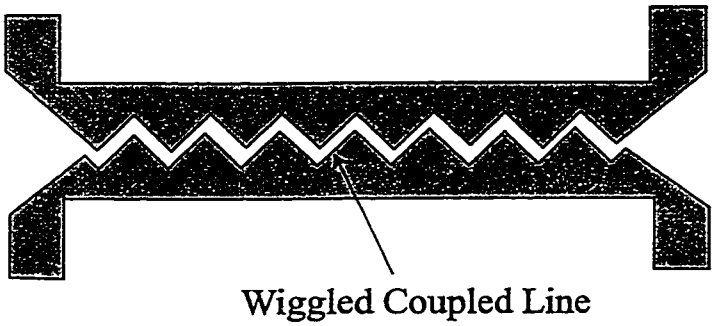
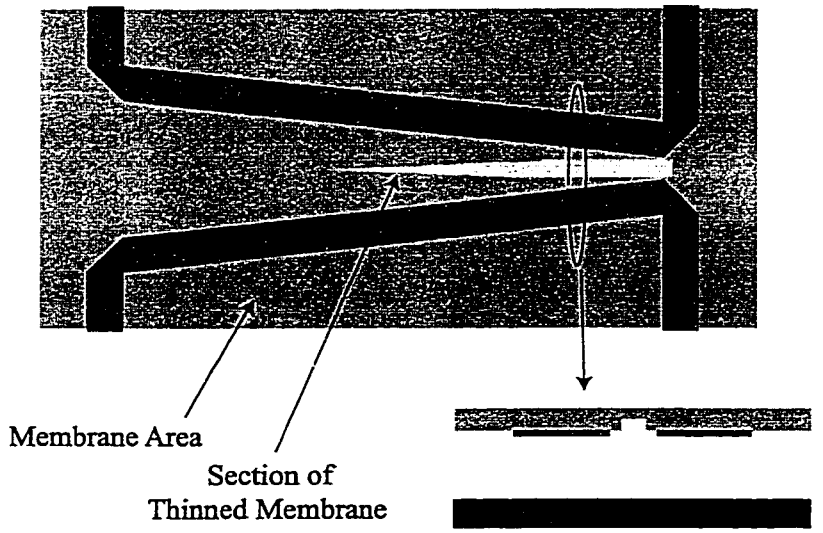


Figure A.7: Phase velocity compensation by wiggling the coupling gaps. The wiggling of the coupled section increases the odd mode effective dielectric constant and is used with conventional microstrip couplers.

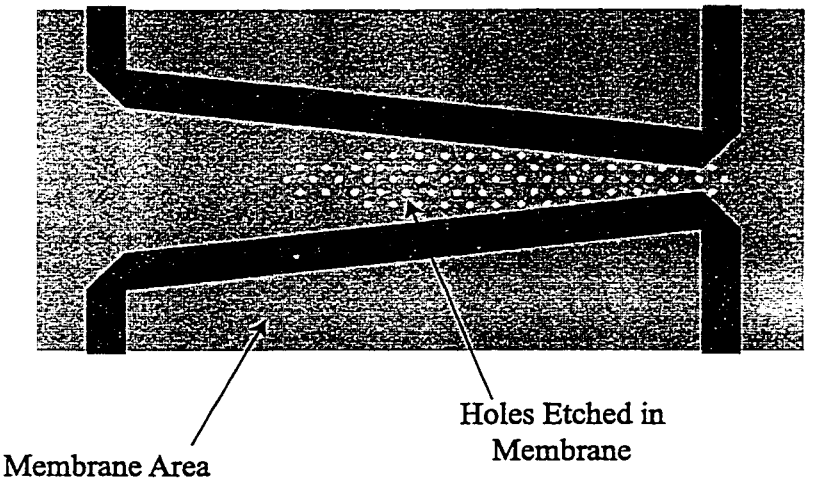
A.4 Recommendations for Future Designs

In the past, high isolation microstrip couplers have been fabricated by "wiggling" the coupled line section [82] (Fig. A.7). The wiggling of the line effectively slows down the odd mode phase velocity while the even mode is unchanged (increases ϵ_{eff} for odd mode only). For conventional microstrip couplers, this is very effective. However, the membrane suspended microstrip coupler has a different problem. For the membrane suspended coupler, the odd mode effective dielectric constant needs to be decreased. Elimination of the membrane within the gap alone would decrease the odd mode effective dielectric constant too much resulting in an odd mode ϵ_{eff} less than that of the even mode. One solution is to decrease the thickness of the membrane in a localized region in between the microstrip lines. The amount of dielectric removed would depend strongly on the gap width (Fig. A.8a). The dielectric membranes used for the membrane suspended microstrip lines are very robust with mechanical strengths in excess of 2×10^5 psi [83] and are under very low stress. Thinning the membrane in a small surface area should not drastically effect the mechanical strength.

Another method for decreasing the odd mode effective dielectric constant to match the even mode would be to selectively etch holes completely through the membrane to result in an overall decrease in the dielectric constant (Fig. A.8b). This has the



(a)



(b)

Figure A.8: Coupler with equalized even/odd mode effective dielectric constants by thinning the dielectric membrane within the coupling region.

added flexibility in that the density and size of the holes can be chosen to result in an effective quasi-static ϵ_r between 5 (no holes) and 1 (all dielectric removed). Both methods allow for an arbitrary shape for the removal (or thinning) of the membrane to allow for an optimized geometry.

APPENDIX B
MILLIMETER-WAVE THIN-FILM RESISTORS

B.1 Introduction

Precision thin-film resistors are required for many planar circuit structures such as matched terminations, power dividers, bias networks, attenuators, etc. Precision resistors are also necessary for development of devices that consist of more than two ports. This would allow for the direct measurement of the two port response with a standard network analyzer with all other ports terminated with a matched load. Since any undesirable reflection from the terminations would appear in the measurement, this is the limiting factor in multiple port test measurements and requires attention.

In the past, Nichrome thin-film resistors have been used [48]. Nichrome is a nickel-chromium allow that is evaporated directly from a single source. However, Nichrome has the disadvantages in that the resistivity of the material changes as the source ages from changes in the alloy composition, it readily oxidizes at room temperature giving a long term drift, limits the allowable succeeding process temperatures to below 200° C, and has a poor temperature coefficient of resistance. As an alternative, tantalum nitride has been investigated.

B.2 Reactive Sputtering of Tantalum Nitride

Thin film tantalum is typically deposited by means of DC sputter deposition with an argon ambient gas. The resistivity of bulk tantalum is approximately 14×10^{-6} Ω cm [84]. This is much too low of a value for any practical use as a thin film resistor. However, by including a partial pressure of nitrogen into the ambient gas, the tantalum sputters into a reactive atmosphere and forms a metallic compound of tantalum nitride. The quality of the tantalum nitride and the resistivity are strong functions of the partial pressure of nitrogen. With no nitrogen flow into the chamber, the deposition is pure tantalum. With increasing nitrogen, the thin film begins to form Ta-N films. B.c.c.-Ta, Ta_2N, TaN, and Ta_5N_6 are formed sequentially with increasing nitrogen flow [85]. The most desirable film is Ta_2N with a resistivity of 250×10^{-6} Ω cm and a temperature coefficient of 0 [86].

The process variables for determining the tantalum film compound include ratio of nitrogen to argon flow, process pressure, and DC sputter current. Several samples were prepared on pieces of carbon tape that were analyzed by X-ray diffraction for varying process parameters. Also, the sheet resistance of each film was determined by means of a four-point probe measurement and the thicknesses of the films were determined by means of a DekTak III Profilometer[1] from sputtered films on glass slides. From the sheet resistance and the thickness measurements, the film resistivity was calculated. In order to get a suitable deposition rate, the current was set at 3 Amps DC. The sputter pressure was set at 11 mTorr to get the highest amount of nitrogen while still maintaining a stable plasma. Table B.1 shows a summary of the results obtained for varying the nitrogen flow ratio.

The percentage of tantalum and nitrogen refer to the atomic concentration. The 10% nitrogen flow gave a concentration of 60% tantalum and 40% nitrogen which yields pure Ta_2N and should give the best temperature coefficient and is therefore

[1]DekTak III Profilometer is a product of Veeco/Sloan Technology, Santa Barbara, CA.

Table B.1: Ta_xN_y film composition and resistivity as a function of nitrogen flow.

N_2 Flow Ratio (% of Ar Flow)	Ta (%)	N (%)	Resistivity (Ω-cm $\times 10^{-6}$)
10	60	40	218
15	58	42	271
20	53	47	317
25	46	54	437

the most desirable for precision terminations.

Another important issue in precision resistors is the ability to trim the values and the long term stability of the termination. Nichrome films oxidize at low temperatures giving an increase in resistance of the film over time as the top portion of the film oxidizes. Tantalum nitride only oxidizes readily at temperatures above 150° C. This greatly improves the long term stability of the resistor. This also allows for high temperature annealing of the film for tuning the value of resistance. The oxide formed on the surface also acts as a passivation layer for the thin resistor.

One of the major disadvantages of tantalum nitride is the contact resistance formed between the tantalum nitride and a titanium/gold metalization. The contact between these metals forms a nonlinear junction. At microwave frequencies, this junction is a very thin capacitance and can be neglected. However, the junction may result in an open circuit at DC, thereby giving erroneous data for DC resistance measurements when annealing. To overcome this problem, a thin layer of Tungsten (W) with 5% titanium (Ti) is deposited on top of the tantalum nitride by means of DC sputtering in an argon ambient. This eliminates any noticeable contact resistance between the Ta_2N and Ti/Au metalizations.

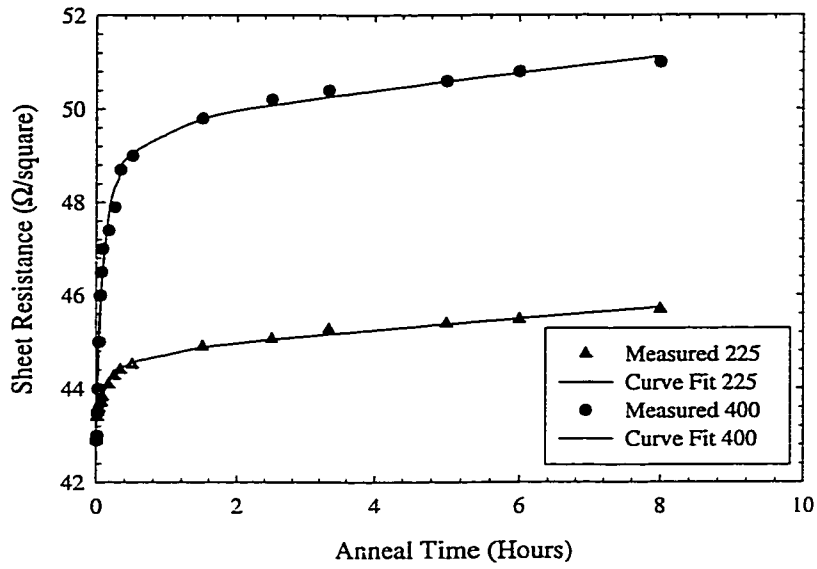


Figure B.1: Sheet Resistance of Ta_2N film with annealing at 225° C and 400° C.

B.3 Tantalum Nitride Resistor Fabrication

The following process recipe describes the formation of tantalum nitride thin film resistors with a contact metalization. The metalization is assumed to be done by a lift-off process of Ti/Au, but this also may be altered for a seed layer and electroplated metal. The process outlined below is for a 50 Ω/sq. thin film resistor. The process uses dry etching to etch the tantalum film. Wet etching could by used with H_2SO_4 as an isotropic etchant. However, this has substantial undercut. By using the dry etching in an RIE, the amount of undercut is minimal with near vertical sidewalls. The process description is broken down into three main steps, namely (1) depositing the tantalum nitride, (2) etching the tantalum nitride, (3) deposition of metal contact layer, and (4) annealing the resistors.

1. Tantalum nitride deposition

   (a) Clean the sample in a sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) solution in a 1:1 combination for 10 minutes. Rinse in DI water and dry

with nitrogen (N_2).

(b) Dehydrate bake the sample on a 130° hot plate for a minimum of 2 min.

(c) Reactively sputter 700 Å of Ta_2N. This corresponds to a sputter pressure of 11 mtorr, a nitrogen ration of 10%, and a current of 3 amps on target three of the University of Michigan SSEL Enerjet sputter machine. The deposition time is 2.5 min. This result in a film with a sheet resistance of 43 Ω/sq.

(d) Without breaking the vacuum, sputter W/Ti(5%) for 1 min at 650 W in an Ar ambient at 7 mtorr. This results in an approximately 100 Å thick layer of W/Ti.

2. Etching the tantalum nitride

(a) Spin coat with Shipley 1813 photoresist (PR) for 30 sec. at 3.5 krpm. Adhesion promoter is not necessary.

(b) Soft bake the sample on a 105° hot plate for 1 min.

(c) Align and expose any square edges or corners of the sample with an edge bead removal mask for 30 sec. at an ultraviolet (UV) light intensity of 20 mW/cm^2.

(d) Develop the sample in a developer solution of MF351:DI water at a concentration of 1:5 for 1 min. to remove edge beads. Rinse in DI water and dry with N_2.

(e) Align a clear-field masks exposing areas where the tantalum nitride film is to be removed. Expose the pattern for 6 sec. at a UV intensity of 20 mW/cm^2.

(f) Develop the resistor pattern in a developer solution of MF351:DI water at a concentration of 1:5 for 1 min. Rinse in DI water and dry with nitrogen

(N_2).

(g) Hard bake the sample on a 130° hot plate for 1 min.

(h) Descum for 1 min in an O_2 plasma with a flow of 20 sccm, pressure of 250 mT, and an RF power of 80 W in the plasma asher.

(i) Etch the exposed W/Ti and Ta_2N in the Semi-Group Reactive Ion Etcher (RIE). The etch is in an SF_6:Ar plasma with gas flows of 10 sccm and 5 sccm, respectively. The process pressure is 10 mT for 5 min. at 100 W. Care must be taken not to over-etch the films. This etch also etches SiO_2 at a rate of 350 Å/min.

(j) Etch the top of the photoresist film to remove any organic residue formed by the Ta_2N etch in an O_2 plasma with a flow of 20 sccm, pressure of 250 mT, and RF power of 180 W for 2 min.

(k) Strip the photoresist in Acetone (ACE) and clean in Isopropyl Alcohol (IPA). Dry with N_2.

3. Contact metalization

(a) Spin coat the sample with Hexamethyldisilazane (HMDS) adhesion promoter and AZ 5214 PR for 30 sec. each at a spin speed of 3.5 krpm.

(b) Soft bake the sample on a 105° hot plate for 1 min.

(c) Align and expose any square edges or corners of the sample with an edge bead removal mask for 20 sec. at an ultraviolet (UV) light intensity of 20 mW/cm^2.

(d) Develop the sample in AZ 312 MIF developer for 1 min to remove the edge bead. Rinse in DI water and dry with N_2.

(e) Align a clear-field masks exposing areas where the metalization is to be removed. Expose the pattern for 4.5 sec. at a UV intensity of 20 mW/cm^2.

(f) Reversal bake: hard bake the sample on a 130° hot plate for 1 min.

(g) Flood expose the sample for 90 sec. at a UV intensity of 20 mW/cm^2.

(h) Develop the pattern in AZ 327 MIF for 45 sec. Rinse in DI water and dry with N_2.

(i) Clean contact areas of thin film resistors in a hydrochloric acid:DI water mixture of 1:1. This cleans the contact areas of organic compounds formed by the PR, HMDS, and developer. Rinse in DI water and dry with nitrogen (N_2).

(j) Evaporate Ti/Au (250/3500 Å) in the SJ-20 e-beam evaporator.

(k) Lift-off the photoresist and undesired metal in ACE.

(l) Clean in ACE and IPA. Dry with N_2.

(m) Etch the exposed W/Ti thin film in hydrogen peroxide (H_2O_2) for one minute. Rinse in DI water and dry with nitrogen (N_2).

4. Anneal the resistors on a hot plate at 400° C for approximately 3 hours. Check the value of resistance periodically during the annealing to get the exact value of 50 Ω/sq.

Once the resistors are annealed, they are very resistant to most chemicals used for semiconductor processing. Also, the resistors are not greatly changed by elevated temperatures used in processing. The initial oxidation formed by annealing forms a capping layer protecting the precision thin film that determines the value of resistance.

A CPW test structure was fabricated with a characteristic impedance of approximately 50 Ω with a center conductor width of 100 μm and a gap width of 65 μm. Two patches of Ta_2N were added at the end of the CPW open circuit with dimensions of 30 μm by 65 μm (2.17 squares) to form two 100 Ω resistors in parallel to ground. The resistor test structure was annealed at 225° C for 4 hours to give a total DC resistance

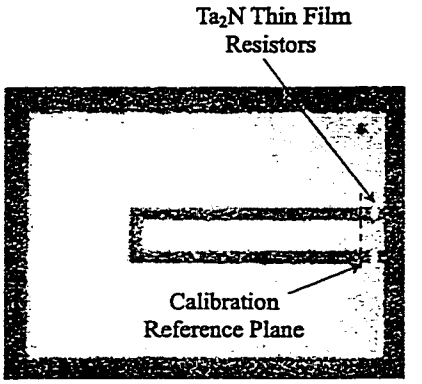


Figure B.2: Fabricated Ta_2N thin film resistor.

of 50.8 Ω. The termination was measured using a TRL [32] calibration technique. The calibration reference plane is 50 μm from the lumped termination. The measured termination performance is shown in Fig. B.3. The termination provides a good match from 2-40 GHz with less than 25 dB return loss.

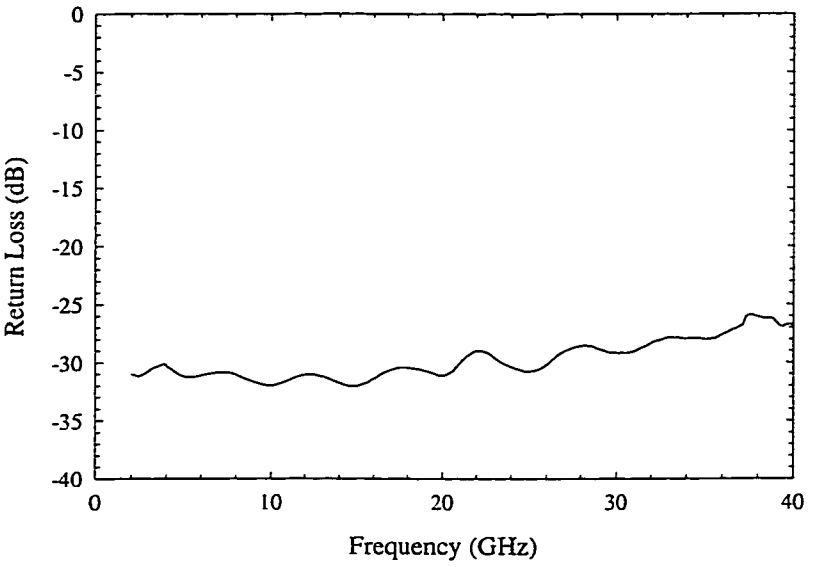


Figure B.3: Measured 50 Ω thin-film termination

APPENDIX C

FABRICATION PROCEDURE FOR MEMBRANE SUPPORTED CIRCUITS

This appendix discusses the fabrication procedure used for the membrane supported circuits discussed in this thesis. The process is used for the membrane suspended microstrip structures as well as with grounded CPW-on-silicon with via holes and air-bridges. This process has a single electroplating step that plates the circuit metal and the air-bridges simultaneously. It also allows for a circuit metal layer which is not electroplated. The non-electroplated circuit metal has a much higher line resolution and smoother metal surface. For thin film metal-insulator-metal (MIM) capacitors, the smoother metal is necessary to prevent pin holes in the capacitor dielectric [86]. This process can also be integrated with the tantalum nitride thin film resistors presented in Appendix B.

C.1 Fabrication of Thin Dielectric Membranes on Silicon Substrates

The thin dielectric membranes used in this work are based mainly on membranes used to suspend antenna and power sensor structures [87], [88]. The membranes are robust enough to withstand most semiconductor processing and to support large,

Table C.1: Film parameters for membrane thin films.

Layer	Thermal SiO_2	LPCVD Si_3N_4	LPCVD SiO_2
Film Stress [40]	300 MPa Compressive	700-1000 MPa Tensile	200-300 MPa Compressive
Relative Dielectric Constant	3.9	7.5	3.9
Etch Rate in TMAH[1]	3 Å/min	Negligible	4 Å/min

suspended metallic circuits. The process described in this section is for standard silicon substrates. However, a similar method can be used with GaAs [89]. The objective in the fabrication of thin film dielectric membranes is to produce a thin dielectric layer that is robust, chemically inert to bulk silicon etchants, and under a slight amount net tension at room temperature.

The thin films used for the dielectric membranes in this work consist of SiO_2 and Si_3N_4. Both films are etched at slow rates in both EDP and TMAH silicon etchants. The SiO_2 can be either thermally grown, deposited using low pressure chemical vapor deposition (LPCVD), deposited by plasma enhanced chemical vapor deposition (PECVD), or reactively sputtered. Si_3N_4 can also be deposited by LPCVD, PECVD, or sputtered. However, the PECVD and sputtered films are not as uniform or repeatable as the thermally grown or LPCVD deposited films and will not be discussed. The growth or depositions of these films is done at high temperature. Since each film (and the substrate itself) has a non-zero coefficient of thermal expansion, a net stress is present in each film at room temperature. The film parameters for these films is given in Table C.1. Note that each of the films have very high compressive or tensile stress. In order to balance the stress, a weighted combination of films is used. By altering the composition of the membrane, the net stress is controlled to result in flat, self-supporting membranes, while preventing too much stress that may rupture the membrane.

A three layer structure is used with thermal SiO_2 as the first layer followed by

[1]Measured etch rated based on 12.5% aqueous solution of TMAH at 85° C.

LPCVD Si_3N_4 and SiO_2. The first thermal layer provides a high quality oxide with excellent adhesion to the substrate. The second layer adds thickness, strength, and tension with the Si_3N_4. The third layer is used to balance the net stress of the membrane and also to relieve the localized stress between the first thermal oxide layer and the high stress Si_3N_4 to avoid problems with adhesion between the films. The original thickness of the films used was based on [83] with a composition of 5000 Å/3000 Å/4000Å of $SiO_2/Si_3N_4/SiO_2$. This resulted in a yield of approximately 75% on free standing membranes that were 8 mm × 8 mm.

The membrane yield was improved by increasing the film thicknesses and optimizing the layer thickness proportions. A test sample was prepared with dielectric thicknesses of 6300 Å/4000 Å/5000 Å. This grows/deposits dielectric on both sides of the sample. The dielectric membrane was then completely removed from one side of the sample. The relative net stress of the film was measured by analyzing the resulting curvature of the wafer [86]. When the film is tensile, the sample bows concave with respect to the membrane side of the wafer. For a compressive film, the sample bows convex. The amount of curvature was measured with a DekTak III Profilometer[2]. The residual stress, σ_R, in the membrane as a function of the wafer deflection, h, on a circular substrate of radius r, is given by [90]:

$$\sigma_R = \frac{E_s}{3(1-\nu)} \frac{h}{r^2} \frac{d_s^2}{d_f} \tag{C.1}$$

where E_s is the Young's modulus of the substrate (130 GPa for silicon [91]), ν is Poisson ratio for the substrate (0.28 [91]), d_s is the substrate thickness, and d_f is the film thickness. The measured deflection for the 1.53 μm membrane on a 500 μm silicon substrate 1100 Å (convex). This results in a residual stress of 0.11 N/mm^2, compressive. The top layer of oxide was then etched 1200 Å in buffered hydrofluoric acid (BHF). This resulted in no measurable deflection indicating that the net residual stress is zero. However, the membranes are to be in slight tension to fully

[2]DekTak III Profilometer is a product of Veeco/Sloan Technology, Santa Barbara, CA.

support the circuits without sagging. The top layer of oxide was etched an additional 300 Å resulting in an oxide thickness of 3200 Å for the top layer. This resulted in a deflection of 500 Å concave with a calculated film stress of 0.05 N/mm^2, tensile. This is the desired membrane after the bulk micromachining steps. Since the etch rate of LPCVD SiO_2 is 4 Å/min. with an etch time of 360 min. for a 400 μm thick wafer in TMAH, an additional 1500 Å of oxide should be added to the desired 3200 Å to compensate for the silicon etching. The total membrane composition before the bulk micromachining process is 6300 Å/4000 Å/4700 Å of $SiO_2/Si_3N_4/SiO_2$. This results in a high membrane yield (>90% for 8 mm × 8 mm membranes) without any noticeable bowing of the membranes even with thick metalization patterns.

C.2 Circuit Fabrication

The fabrication process can be broken down into 12 steps: (1) wafer cleaning, (2) metal lift-off, (3) metal electroplating and air-bridge formation, (4) backside infrared alignment and membrane etch, (5) shielding wafer (bottom substrate) patterning, (6) ground plane substrate (top wafer) alignment mark deposition, (7) ground plane substrate front side patterning, (8) ground plane substrate back side patterning, (9) bulk silicon etching of circuit substrate, (10) bulk silicon etching of the shielding wafer, and (11) etching the ground planes and probe window openings in the top wafer. The process is assuming that the circuit wafer is a high-resistivity, 400 μm silicon wafer with a dielectric membrane layer, and the top and bottom wafers are 525 μm (standard thickness), low-resistivity, silicon wafers with 1.2 μm of thermal SiO_2.

1. Wafer Cleaning - applies to all wafers:

   (a) 1 minute soak in hot acetone (ACE) followed by a 1 minute soak in isopropyl alcohol (IPA).

   (b) Blow dry with N_2. Dehydrate bake for 20 minutes at 130° C in the oven

with a dry N_2 ambient gas.

2. Metal lift-off of circuit metal:

   (a) Spin coat the sample with Hexamethyldisilazane (HMDS) adhesion promoter and AZ 5214 PR for 30 sec. each at a spin speed of 3.5 krpm.

   (b) Soft bake the sample on a 105° hot plate for 1 min.

   (c) Align and expose any square edges or corners of the sample with an edge bead removal mask for 20 sec. at an ultraviolet (UV) light intensity of 20 mW/cm^2.

   (d) Develop the sample in AZ 312 MIF developer for 1 min to remove the edge bead. Rinse in DI water and dry with nitrogen (N_2).

   (e) Align a clear-field masks exposing areas where the metalization is to be removed. This mask includes all circuit metal patterns and sets of alignment marks for both front side and back side alignment. Expose the pattern for 4.5 sec. at a UV intensity of 20 mW/cm^2.

   (f) Reversal bake: hard bake the sample on a 130° hot plate for 1 min.

   (g) Flood expose the sample for 90 sec. at a UV intensity of 20 mW/cm^2.

   (h) Develop the pattern in AZ 327 MIF for 45 sec. Rinse in DI water and dry with nitrogen (N_2).

   (i) Evaporate Ti/Au (250/3500 Å) in the Denton SJ-20 e-beam evaporator.

   (j) Lift-off the photoresist and undesired metal in PRS-1000 photoresist stripper.

   (k) Rinse in DI water.

   (l) Clean in ACE and IPA. Dry with N_2.

3. Metal electroplating and air-bridge formation:

(a) Spin coat the sample with HMDS adhesion promoter and Shipley 1827 PR for 30 sec. each at a spin speed of 3.5 krpm. This gives a uniform coating of approximately 2.9 μm setting the height of the air-bridges [3].

(b) Soft bake the sample on a 105° C hot plate for 1 min.

(c) Align a dark-field mask exposing areas where there is to be electroplated metal except any areas directly under air-bridges or for non-electroplated circuit metal regions (Fig. 3). Expose the pattern for 12 sec. at a UV intensity of 20 mW/cm^2.

(d) Develop the sample in a developer solution of MF351:DI water at a concentration of 1:5 for 1 min. to remove edge beads. Rinse in DI water and dry with nitrogen (N_2).

(e) Hard bake the sample at 130° C on a hot metal plate in the oven with a dry nitrogen ambient gas for 2.5 min. This step is critical for removing all of the solvents from the resist to allow for additional layers to be applied without causing bubbles in the resist. This produces a conformal resist profile.

(f) Descum for 1 min in an O_2 plasma with a flow of 20 sccm, pressure of 250 mT, and an RF power of 80 W.

(g) Evaporate Ti/Au/Ti (250/1000/250 Å) in the Denton SJ-20 e-beam evaporator.

(h) Spin coat the sample with Shipley 1827 PR for 30 sec. at a spin speed of 3.5 krpm. HMDS is not needed since the PR has good adhesion with the Ti layer.

(i) Soft bake the sample at 85° C in the oven for 20 min.

[3]This can be altered for higher or lower air-bridges by altering the spin speed for the photoresist or substituting a thinner/thicker resist.

(j) Align a dark-field mask exposing areas where there is to be electroplated metal including the air bridges. Expose the pattern for 12 sec. at a UV intensity of 20 mW/cm^2.

(k) Develop the sample in a developer solution of MF351:DI water at a concentration of 1:5 for 1 min. to remove edge beads. Rinse in DI water and dry with nitrogen (N_2).

(l) Descum for 1 min in an O_2 plasma with a flow of 20 sccm, pressure of 250 mT, and an RF power of 80 W.

(m) Etch the exposed top Ti layer with a solution of 1:10 HF : DI – H_2O for approximately 10 sec. Rinse in DI – H_2O and dry with N_2.

(n) Electroplate 2 μm of gold through the photoresist mold. DC contact to all features is made through the evaporated seed layer. The gold plating solution used is OroTemp 24[4] composed of 6.87% potassium aurocyanide ($KAu(CN)_2$) and DI water. The solution is heated to 55° C and stirred with a magnetic stirring to improve plating uniformity. The anode is a platinum wire mesh with the circuit wafer acting as the cathode. The plating rate used was approximately 4 μm /hour. Rinse in DI water and dry with N_2.

(o) Flood expose the top layer of photoresist for 30 sec. with UV light at 20 mW/cm^2.

(p) Develop away the top layer of photoresist in a solution of MF351:DI water at a concentration of 1:5 for 1 min. Rinse in DI water and dry with N_2.

(q) Strip the Ti/Au/Ti seed layers in a solution of 1:10 HF : DI – H_2O for approximately 10 sec. for the Ti layer and gold etchant for the gold. Rinse in between each etch. Care must be taken not to over-etch the Ti in

[4]OroTemp 24 is a product of Technic, Inc., 1 Spectacle Street, Cranston, RI.

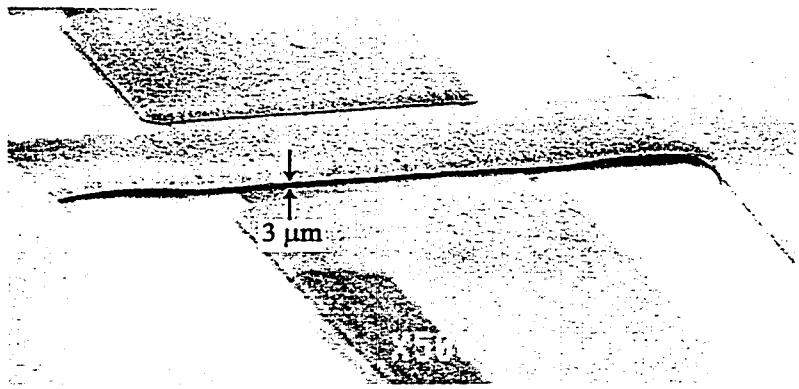


Figure C.1: SEM photograph of fabricated air bridge. The bridge is plated at the same time as the ground plane as well as selected portions of the center conductor.

risk of undercutting the metal patterns. Also, the gold etch attacks the electroplated gold as well as the seed layer. Over-etching of the gold may unnecessarily etch the desired circuit metal. Rinse in DI water and dry with N_2.

(r) Strip the initial layer of photoresist with hot PRS-1000. Rinse in DI water and dry with N_2.

4. Backside alignment and membrane removal (circuit wafer):

(a) Spin coat the front side of the sample with HMDS adhesion promoter and Shipley 1827 PR for 30 sec. each at a spin speed of 3.5 krpm to protect the front of the wafer.

(b) Soft bake the sample on a 105° C hot plate for 1 min.

(c) Hard bake the sample on a 130° C hot plate for 1.5 min.

(d) Spin coat the back side of the sample with HMDS adhesion promoter and Shipley 1827 PR for 30 sec. each at a spin speed of 3.5 krpm to protect the front of the wafer.

(e) Soft bake the sample on a 105° C hot plate for 1 min.

(f) Align a dark-field mask to the back side of the sample using infrared alignment. This mask defines the etch area for the membrane suspended microstrip area as well as the via holes. Expose the pattern for 12 sec. at a UV intensity of 20 mW/cm^2.

(g) Develop the sample in a developer solution of MF351:DI water at a concentration of 1:5 for 1 min. to remove edge beads. Rinse in DI water and dry with nitrogen (N_2).

(h) Hard bake the sample at 130° C on the hot plate.

(i) Etch the LPCVD layer of SiO_2 in buffered hydrofluoric acid (BHF) for 5 min. The etch rate for the LPCVD oxide is approximately 1500 Å/min. This slightly over-etches the oxide ensuring that the silicon nitride layer is fully exposed. Rinse in DI water and dry with nitrogen (N_2).

(j) Etch the LPCVD layer of silicon nitride in a plasma etcher using 25 sccm of CF_4 and 0.5 sccm of O_2 at a pressure of 250 mTorr and a power of 100 W for 10 min.

(k) Etch the layer of thermal SiO_2 in buffered hydrofluoric acid (BHF) for 9 min. The etch rate for the thermal oxide is approximately 1000 Å/min. This slightly over-etches the oxide ensuring that bare silicon is fully exposed. Rinse in DI water and dry with nitrogen (N_2).

(l) Strip the photoresist with hot PRS-1000. Rinse in DI water and dry with N_2.

5. Shielding wafer patterning:

(a) Spin coat the back side of the sample with HMDS adhesion promoter and Shipley 1827 PR for 30 sec. each at a spin speed of 3.5 krpm to protect the front of the wafer.

(b) Soft bake the sample on a 105° C hot plate for 1 min.

(c) Hard bake the sample on a 130° C hot plate for 1.5 min.

(d) Spin coat the front side of the sample with HMDS adhesion promoter and Shipley 1827 PR for 30 sec. each at a spin speed of 3.5 krpm to protect the front of the wafer.

(e) Soft bake the sample on a 105° C hot plate for 1 min.

(f) Align a dark-field mask to the front side of the sample. This mask defines the etch area for the shielding cavities. Expose the pattern for 12 sec. at a UV intensity of 20 mW/cm^2.

(g) Develop the sample in a developer solution of MF351:DI water at a concentration of 1:5 for 1 min. to remove edge beads. Rinse in DI water and dry with nitrogen (N_2).

(h) Hard bake the sample at 130° C on the hot plate.

(i) Etch the layer of thermal SiO_2 in buffered hydrofluoric acid (BHF) for 15 min. The etch rate for the thermal oxide is approximately 1000 Å/min. This slightly over-etches the oxide ensuring that bare silicon is fully exposed. Rinse in DI water and dry with nitrogen (N_2).

6. Ground plane wafer alignment mark deposition: Same as the metal lift off in step 2 except patterning alignment marks on the front side of the ground plane wafer.

7. Ground plane front side alignment:

(a) Spin coat the back side of the sample with HMDS adhesion promoter and Shipley 1827 PR for 30 sec. each at a spin speed of 3.5 krpm to protect the front of the wafer.

(b) Soft bake the sample on a 105° C hot plate for 1 min.

(c) Hard bake the sample on a 130° C hot plate for 1.5 min.

(d) Spin coat the front side of the sample with HMDS adhesion promoter and Shipley 1827 PR for 30 sec. each at a spin speed of 3.5 krpm to protect the front of the wafer.

(e) Soft bake the sample on a 105° C hot plate for 1 min.

(f) Align a dark-field mask to the front side of the sample. This mask defines the ground plane cavities for the structures. Expose the pattern for 12 sec. at a UV intensity of 20 mW/cm^2.

(g) Develop the sample in a developer solution of MF351:DI water at a concentration of 1:5 for 1 min. to remove edge beads. Rinse in DI water and dry with nitrogen (N_2).

(h) Hard bake the sample at 130° C on the hot plate.

(i) Etch 8000 Åof thermal SiO_2 in buffered hydrofluoric acid (BHF) (approximately 8 min.). This leaves 3000 Åof oxide on the ground plane regions. Rinse in DI water and dry with nitrogen (N_2).

8. Patterning of probe window openings:

(a) Spin coat the front side of the sample with HMDS adhesion promoter and Shipley 1827 PR for 30 sec. each at a spin speed of 3.5 krpm to protect the front of the wafer.

(b) Soft bake the sample on a 105° C hot plate for 1 min.

(c) Hard bake the sample on a 130° C hot plate for 1.5 min.

(d) Spin coat the back side of the sample with HMDS adhesion promoter and Shipley 1827 PR for 30 sec. each at a spin speed of 3.5 krpm to protect the front of the wafer.

(e) Soft bake the sample on a 105° C hot plate for 1 min.

(f) Align a dark-field mask to the back side of the sample using infrared alignment by aligning to the alignment marks deposited in section 6. This mask defines the openings for probe access windows. Expose the pattern for 12 sec. at a UV intensity of 20 mW/cm^2.

(g) Develop the sample in a developer solution of MF351:DI water at a concentration of 1:5 for 1 min. to remove edge beads. Rinse in DI water and dry with nitrogen (N_2).

(h) Hard bake the sample at 130° C on the hot plate.

(i) Etch all (1.2 μm) of thermal SiO_2 in buffered hydrofluoric acid (BHF) (approximately 15 min.). This allows for a slight over-etch of the oxide to assure a bare silicon surface. Rinse in DI water and dry with nitrogen (N_2).

9. Bulk silicon etching of circuit wafer:

(a) Heat a 1:1 TMAH : $DI - H_2O$ solution[5] (500 ml) to 85° in a beaker on a hot plate with a temperature feedback probe.

(b) Insert the samples into the TMAH and etch until the membrane is free standing. This solution has a 1.1 μm/min etch rate for the $\langle 100 \rangle$ crystal plane with a $\langle 100 \rangle : \langle 111 \rangle$ selectivity of 25:1. The etch time is 6 hours.

(c) Heat a beaker of DI water to 85° C to use as rinse water. This prevents an abrupt temperature change in the membranes reducing the possibility of shattering. The hot water also help re-dissolve any residue TMAH that may have formed on the sample. Rinse in the hot water for 1 hour and let the water cool to room temperature.

[5]The TMAH is an aqueous solution that is 25% TMAH by weight. The 1:1 TMAH : $DI - H_2O$ reduces the TMAH concentration to approximately 12.5%. The etch rate, quality of etched surfaces, and selectivity of both crystal planes and masking layers are strong functions of the concentration [22] [92] [23]. This concentration has shown to work well for membrane structures.

(d) Rinse the sample again in fresh water, but this time at room temperature.

(e) Do a final rinse in IPA. The final rinse in IPA rinses the water from the sample and allows for an easier drying process. Dry the IPA from the sample with N_2.

10. Bulk silicon etch of the shielding wafer:

(a) The first portion is identical to step 9, but the etch depth is 400 μm[6]. At this point, the sample is rinsed in a similar manner.

(b) Etch the remaining SiO_2 away in BHF for 15 min. This cleans the sample of any imperfections in the oxide mask. This also eliminates any lip of oxide that formed by the undercut of the TMAH etch. Rinse in DI water and dry with N_2.

(c) Sputter coat the shielding wafer with Ti/Au (500 Å/2.7 μm) using a static deposition in the Enerjet sputter tool.

11. Etching of the ground plane wafer:

(a) Etch the probe window openings in TMAH prepared the same as step 9a. The initial etch depth of the probe windows, t_{back}, is given by:

$$t_{back} = t_{sub} - 1.7t_{ground} \tag{C.2}$$

where t_{back} is the etch depth of the initial etching of the probe window openings, t_{sub} is the thickness of the substrate, and t_{ground} is the total depth of the ground plane[7]. Rinse in DI water and dry with N_2.

(b) Remove the remaining 3000 Åof oxide from the ground plane cavities in BHF for 3 min. This also thins masking layer for the probe window open-

[6]The etch depth is measured using a calibrated focus on a microscope.

[7]The added factor of 0.7 takes into account that the etch rate for the rough, unpolished surface in the probe window openings is approximately 0.7 times the etch rate for polished surfaces assuming single polished substrates are used

ings and the ground plane cavities by 3000 Åleaving 9000 Åfor the etch mask. Rinse in DI water and dry with N_2.

(c) Place the sample back in the etchant until the ground planes are etched to the correct depth.

(d) Rinse the sample the same as in steps 9c-d.

(e) Etch the remaining SiO_2 away in BHF for 12 min. This cleans the sample of any imperfections in the oxide mask. This also eliminates any lip of oxide that formed by the undercut of the TMAH etch. Rinse in DI water and dry with N_2.

(f) Sputter coat the shielding wafer with Ti/Au (500 Å/2.7 μm) using a static deposition in the Enerjet sputter tool.

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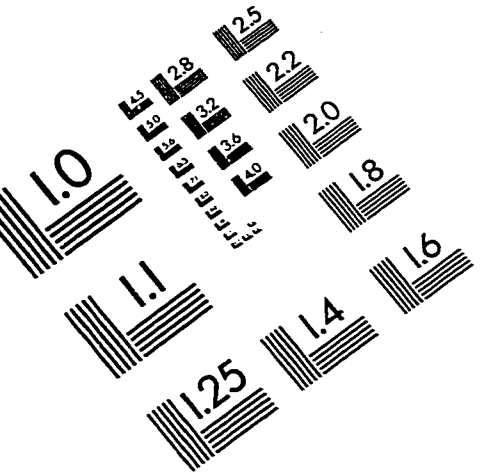
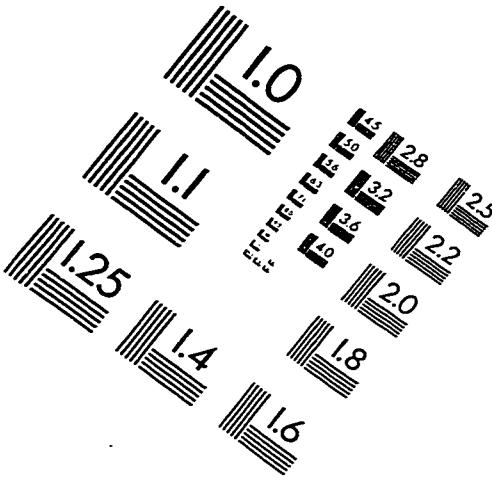
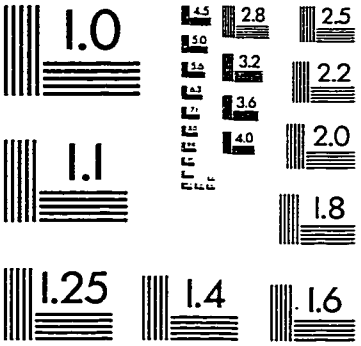
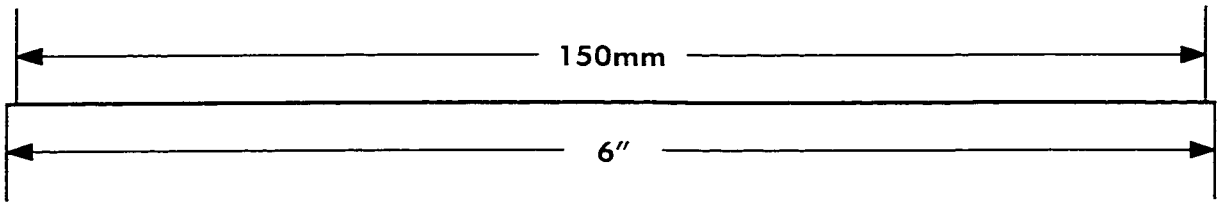
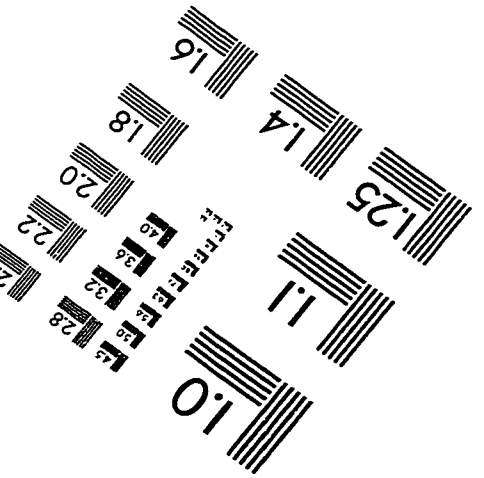
IMAGE EVALUATION TEST TARGET (QA-3)

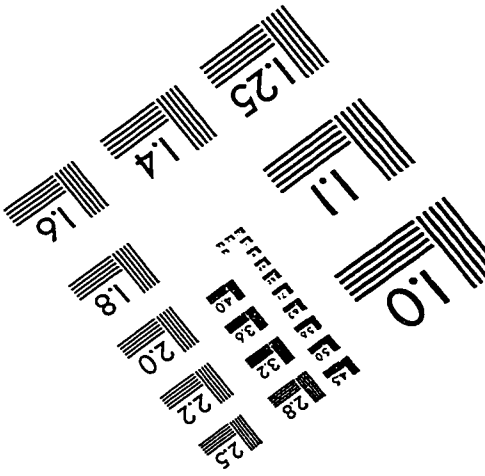












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