Development of High Performance 6-18 GHz Tunable/Switchable RF MEMS Filters and Their System Implications.

by

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To

My Mother, Zahra,

My Father, Fereidoun,

and

My Brother, Kambiz

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CHAPTER 1

Introduction

1.1 Tunable Filter Applications in Microwave/Milimeter-wave Systems

Tunable filter applications in microwave/millimeter-wave systems fall into three major areas: military systems, measurement equipments and communication systems (satellite, cellular radio, etc)[1][4].

Invention of radar systems led to significant development in filters. Basically, one of the critical parts of any military system, such as radars and tracking receivers, is the electronic support measures (ESM) system [2]. The ESM system detects and classifies incoming radar signals by amplitude, frequency, pulsewidth, etc. The electronic countermeasures (ECM) system which is associated with ESM system, can then take appropriate countermeasures, such as jamming. One method of classifying signals by frequency is to split the complete microwave band of interest into smaller sub-bands. This can be done either by using a contiguous multiplexer ,which consists of separate mechanically tunable bandpass filters whose pass-bands cross over at their 3 dB frequencies [3], or an electronically or magnetically tunable filter to scan the whole receive band. Of course, the tuning speed of the filter should be fast enough to keep track of all the signals appear in the whole band of interest.

Magnetically tunable filters are extensively used in microwave instrumentations. One example is a fully integrated front-end for a high performance spectrum analyzer (Fig. 1.1). It contains a magnetically tuned *preselector* followed by a balanced, fundamental mixer. The LO signal (3-22.3 GHz) is supplied to the mixer. Another magnetically tuned resonator is tuned to the LO

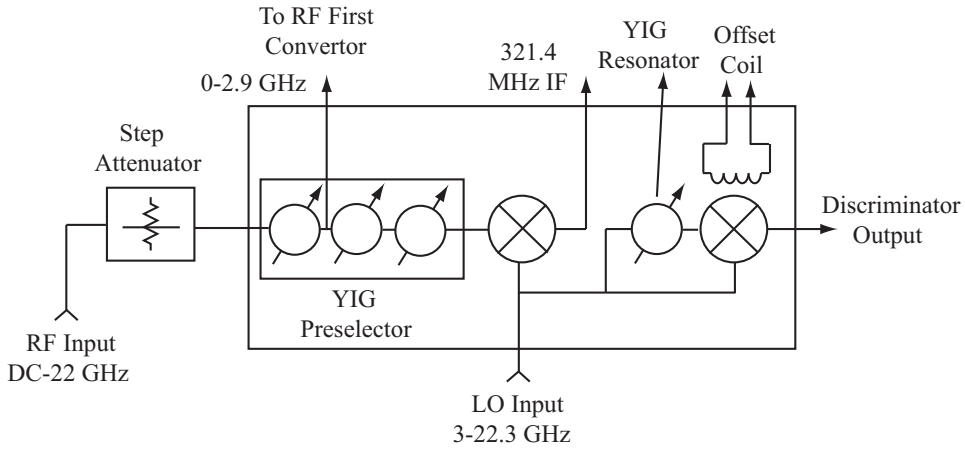


Figure 1.1: Switched tracking pre-selector - mixer.

frequency using the *offset coil* . The resonator acts as a discriminator, generating an error voltage which is fed back to the magnetic tuning circuitry to frequency lock the pre-selector [5][6].

Tunable filters are frequently employed in communication systems. Satellite communication transponders normally use mechanically tunable manifold multiplexers at their transmit and receive bands to combine or split channels in frequency domain [7]. Military radios for multi-band or frequency-hopped transceivers also employ tunable filters in their transmit and receive bands.

1.2 Different Techniques for RF Filter Tuning

Most tunable filters described in the literature fall into three basic types: mechanically tunable, magnetically tunable and electronically tunable filters [4].

Mechanically tunable bandpass filter's large power handling capability and low insertion loss are often important factors if a tunable filter is required for long-distance communication (satellite or transponder) or radar systems. They are usually realized using either coaxial or waveguide resonators [8]. The main disadvantages of these filters are their tuning speed and size. Their tuning speed is very low. They can be tuned manually or electrically if the filter is combined with a remotely controlled motor. Their size is large and they are bulky. In modern highly integrated systems, the bandpass filter is generally subject to serious size constraints, so these filters are not suitable candidates for integrated RF front ends or compact T/R modules.

Magnetically tunable filters have been used in microwave/milllimeter-wave systems for a long

time. The most popular type uses ferromagnetic resonators and gyromagnetic coupling. The first filter of this kind was reported in 1958 [9]. Since they usually contain single-crystal Yttrium-Iron-Garnet (YIG) spheres in their resonators, they are commonly termed YIG filters. They have multi-octave tuning range, spurious-free response, low insertion loss and high quality factor resonators [8][10]. They are often used between 0.5-18 GHz for military and commercial purposes, such as tracking receivers, radars, etc. The design principles for multi-stage YIG filters from 0.5 to 40 GHz are described in [8][11][12]. Magnetic resonator filters have also been developed for millimeter-wave applications. Instead of using YIG spheres, they employ highly anisotropic hexagonal ferrites. The 4-pole filter reported in [5] has been tuned from 50 to 75 GHz with an insertion loss of about 6 dB and a relative bandwidth of 1%. As mentioned above, the important problems associated with YIG filters are size, tuning speed and power consumption. Compare to mechanically tunable filters they have smaller size, but because they are not planar structures, they cannot be used in integrated systems. The YIG filter is tuned by changing the biasing current of the ferromagnetic resonator. This current is in the order of hundreds of milliamperes, which is not acceptable in most modern low power RF transceivers. YIG filters have moderate tuning speed, which is not usually less than 1-2 GHz/ms which is not enough for applications which require very fast tuning (electronic warfare, signal intelligence, etc).

Electrically tunable filters can be tuned very fast over a wide (an octave) tuning range, and they offer compact size and are good candidates for highly integrated RF front ends. The best way of tuning an RF filter electronically is using tunable capacitors as part of the resonator. The capacitor value and the resonator frequency are changed by adjusting the biasing voltage across the tunable capacitor. There are three major technologies applied for this type of RF filter tuning:

(a) *Semiconductor Gallium-Arsenide (GaAs), Silicon (Si) or Silicon-Germanium (SiGe) varactors:* The varactor diode capacitance varies with the reverse bias voltage across the diode. The main advantages of varactor-tuned filters reside in their superior tuning speed and their small size. However, they also have some serious disadvantages. They suffer from poor power handling. Since varactor diodes are nonlinear device, they generate harmonics and sub-harmonics in the presence of large signals and limit the dynamic range of the filter. Due to the low quality factor of varactor diodes at microwave and millimeter-wave frequencies, these filters show considerable amount of loss for 2-40 GHz applications. [13][14][15][16]

(b) *Ferroelectric thin film tunable capacitors:* Ferroelectric materials have two phases of operations: ferroelectric phase and paraelectric phase. In paraelectric phase, the relative dielectric constant remains large ($\epsilon_r \approx 300$) and can be changed with the applied electric field. This enables the fabrication of electronically tunable capacitors at dc-bias level as low as 2-5 V [29]. Two of the most popular thin-film ferroelectric materials are Strontium Titanate (STO) and Barium Strontium Titanate (BST). STO has high tunability at very low temperatures (around 77°K) and needs a huge voltage for tuning. It shows very poor tunability at room temperature. On the other hand, BST can be made highly tunable at room temperature. It is planar and easy to integrate with integrated circuits. Varactor diodes must be reversed biased and this degrades their power-handling capability (diode turns on at large RF swing voltages). BST-based capacitors do not have this limitation, so they are suitable for high-power applications [30]. The recent results for a VHF tunable filter using an improved quality factor BST tunable capacitor ($Q_C \approx 60$) shows a tunability of 57% (176 MHz - 276 MHz) with a capacitance ratio of 2.5 and an insertion loss of 3 dB [31]. The linearity of BST capacitors is not great and is comparable with their varactor diode counterparts.
(c) *Radio frequency micro-electromechanical systems (RF MEMS) switches and varactors:* MEMS-based tunable filters employ either MEMS switches or MEMS varactors. They are suitable for microwave and millimeter-wave miniaturized tunable/switchable filters used in integrated RF front ends. Development of tunable MEMS filters is the main subject of this dissertation. Section 1.3 discusses the main advantages and disadvantages of RF MEMS technology compared to other technologies.

In Table 1.1, the performance of the tunable filters is summarized. From this comparison it is obvious that none of these filters can simultaneously satisfy all the requirements for a "the" perfect tunable filter.

1.3 RF MEMS Technology

Micro-Electro-Mechanical-Systems (MEMS) are micro-scaled devices which provide a link between mechanical and electrical phenomena and are fabricated using micro-fabrication techniques used in the Integrated Circuit (IC) industry. MEMS was initiated in 1970s and have been developed for accelerometers, gyroscopes, pressure sensors, temperature sensors, bio-sensors...etc. The field

Table 1.1: Typical performance parameters of microwave tunable bandpass filters.

Parameter	Mech.	YIG	PIN/FET	BST	RF MEMS
I.L.[dB]	$0.5-2.5$	$3-8$	$3-10$	$3-5$	$3-8$
Unloaded Q	>1000	>500	<50	<100	$<100-500$
Power Handling[W]	500	2	0.2	–	2
Bandwidth[%]	$0.3-3$	$0.2-3$	>4	>4	$1-10$
IIP_3[dBm]	very high	<30	<30	<30	>50
Tuning speed[GHz/ms]	very low	$0.5-2$	10^3	–	10^2
Tuning linearity[MHz]	±15	±10	±35	–	–
Miniaztrization capability	No	No	Yes	Yes	Yes
Millimeter − wave capability	No	Yes	No	No	Yes

of MEMS is extremely diverse and the devices working at microwave frequency are called RF (Radio Frequency) MEMS. Due to its outstanding performance, RF MEMS has immense potential for commercial and defense applications. One of the most important components in the RF/Microwave applications is RF MEMS switch. It is essentially a miniature device which use mechanical movement to achieve an open- or short circuit in a transmission line. RF MEMS switches come in two configurations: metal-contact and capacitive-contact. Fig. 1.2 shows two metal-contact series switches developed by Analog Devices [17] and Lincoln Laboratory [18] respectively with their equivalent circuit model.

Series switch either makes an open circuit in the signal path ($C_{up} < 6$ fF) or a short circuit and the signal goes through the metal-to-metal contact ($R_s < 2\ \Omega$). Metal-to-metal switches are mostly used at DC-40 GHz. On the other hand, capacitive switches achieve the same response but using a metal-dielectric contact. Fig. 1.3 presents a capacitive shunt switch developed by Raytheon [19]. It either allows the signal to pass or shorts the signal to the ground ($C_{down} \ll C_{up}$). Capacitive switches are suitable for 10-200 GHz applications and have a capacitive ratio $C_r = C_{down}/C_{up}$ ratio of 20-100. This ratio is not suitable for some applications such as loaded-line phase shifters [23][24], reconfigurable matching networks [25][26], and wide-band switchable filters [27][28] where a capacitive ratio of 2-5 is needed. In this case, the capacitive ratio can be lowered by placing fixed capacitors in series with capacitive MEMS switches. For some applica-

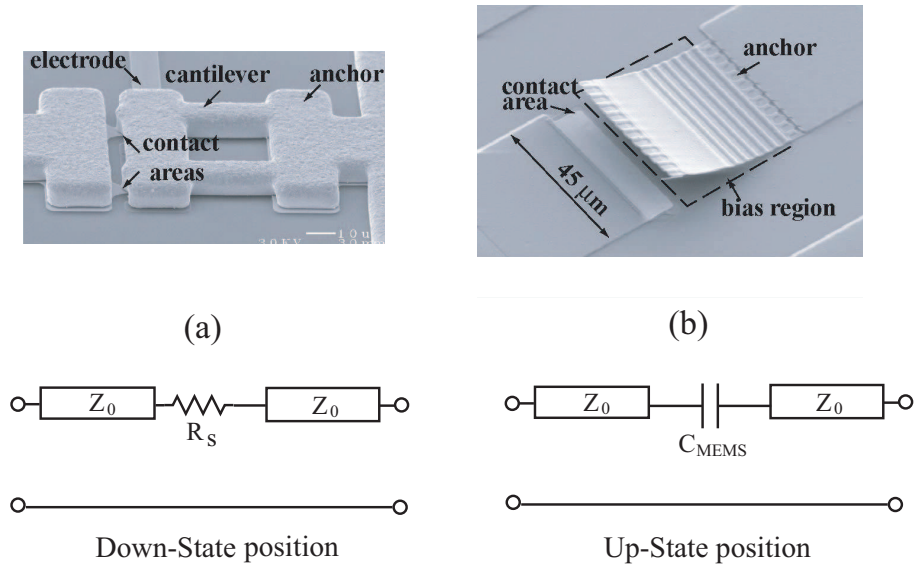


Figure 1.2: Series metal-contact switches developed by (a) Analog Devices and (b) Lincoln Laboratory with their corresponding equivalent circuits.

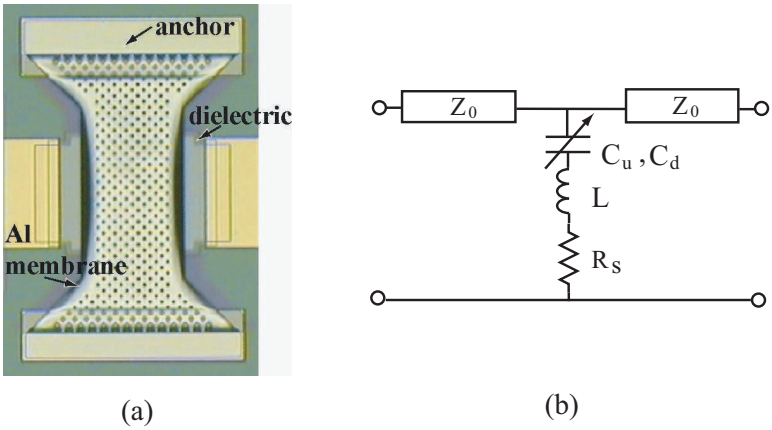


Figure 1.3: Shunt capacitive switch developed by Raytheon: (a) Top view and (b) the corresponding electrical model.

tions, such as tunable filters [45] which continuous capacitance variation is required, analog MEMS varactors have been developed [22], but the C_{down}/C_{up} ratio in this case is limited to 2 due to planarity (fabrication) problems.

There are several ways to actuate the MEMS switches such as electrostatic, thermal, magnetostatic or piezoelectric. Among these actuation mechanism, electrostatic force is widely used due to its simplicity, compactness and low power consumption characteristics. Although MEMS switches have the disadvantages such as medium switching speed (3-100 μs) and low power handling capability ($<$ 1-2 W) compared to solid state and ferroelectric-based devices, they achieve excellent performance such as:

1. *Very Low Insertion Loss:* Since metals are used for conduction instead of semiconductors, RF MEMS switches show very low loss, about 0.05-0.2 dB from 1-100 GHz.

2. *Very High Linearity:* MEMS switches are very linear devices which result in a very low intermodulation products. They are about 30-60 dB better than FET switches, PIN diodes or BST varactors [21].

3. *Extremely Low Power Consumption:* Although a high voltage (20-100 V) is needed for the electrostatic actuation of MEMS switches, there is very little current consumption leading to very low DC power dissipation.

4. *Very High Isolation:* MEMS metal-contact switches are fabricated in an air dielectric, and therefore have very small off-state capacitance (C_{up}) about 1-6 fF, which leads to an excellent isolation up to 40 GHz.

These advantages along with IC-processing compatibility make RF MEMS an enabling technology for low cost and high performance systems in both military and commercial applications such as wide-band tunable/switchable filters, antenna beam-steering systems, reconfigurable matching networks, reconfigurable array antennas, and satellite communications. Most of the current research activities in RF MEMS area concentrate on improving the power-handling capability, reliability, packaging and switching time of the MEMS-based structures. Table 1.2 summarizes the performance comparison of MEMS switches with the current standard technology such as FET switches and PIN diodes. [20]. The cutoff frequency mentioned in the table is the figure of merit for a series switch and $f_c = 1/(2\pi R_s C_{up})$. Fig. 1.4 is an example of RF MEMS application in an integrated multi-band wireless transceiver. Due to the high isolation of MEMS switches, a single-pole double-

Table 1.2: Performance comparison of FET switches, PIN diode and RF MEMS electrostatic switches.

Parameter	RFMEMS	PIN	FET
Voltage[V]	$20-100$	$\pm 3-5$	$3-5$
Current[A]	0	$3-20$	0
Power Consumption[mW]	$0.05-0.1$	$5-100$	$0.05-0.1$
Switching Time	$1-300\ \mu s$	$1-100\ ns$	$1-100\ ns$
C_{up}(Series)[pf]	$1-6$	$40-80$	$70-140$
R_s(Series)[Ω]	$0.5-2$	$2-4$	$4-6$
Capacitance Ratio	$40-500$	10	N/A
Cutoff Freq.[THz]	$20-80$	$1-4$	$0.5-2$
Isolation($1-10$ GHz)	V.High	High	Medium
Isolation($10-40$ GHz)	V.High	Medium	Low
Isolation($60-100$ GHz)	High	Medium	None
Loss($1-100$ GHz)[dB]	$0.05-0.2$	$0.3-1.2$	$0.4-2.5$
Power Handling[W]]	<0.5	<10	<10
IIP_3[dBm]	$66-80$	$27-45$	$27-45$

through (SP2T) MEMS switch is employed to isolate transmitter and receiver paths from each other. In the receive path, RF MEMS switches are used to select a certain low noise amplifier for the desired frequency band. The image reject filter can be either developed as a RF MEMS switched bank filter or a RF MEMS tunable filter. The IF filters after the quadrature mixers are also designed based on MEMS technology. In the transmit path, MEMS switches can select a specific power amplifier and bandpass filter for the band of interest. this topology can also be replaced by a broadband power amplifier followed by MEMS tuning network and bandpass tunable filter in the transmit path. The frequency of voltage controlled oscillator is also programmed by a bank of RF MEMS switches.

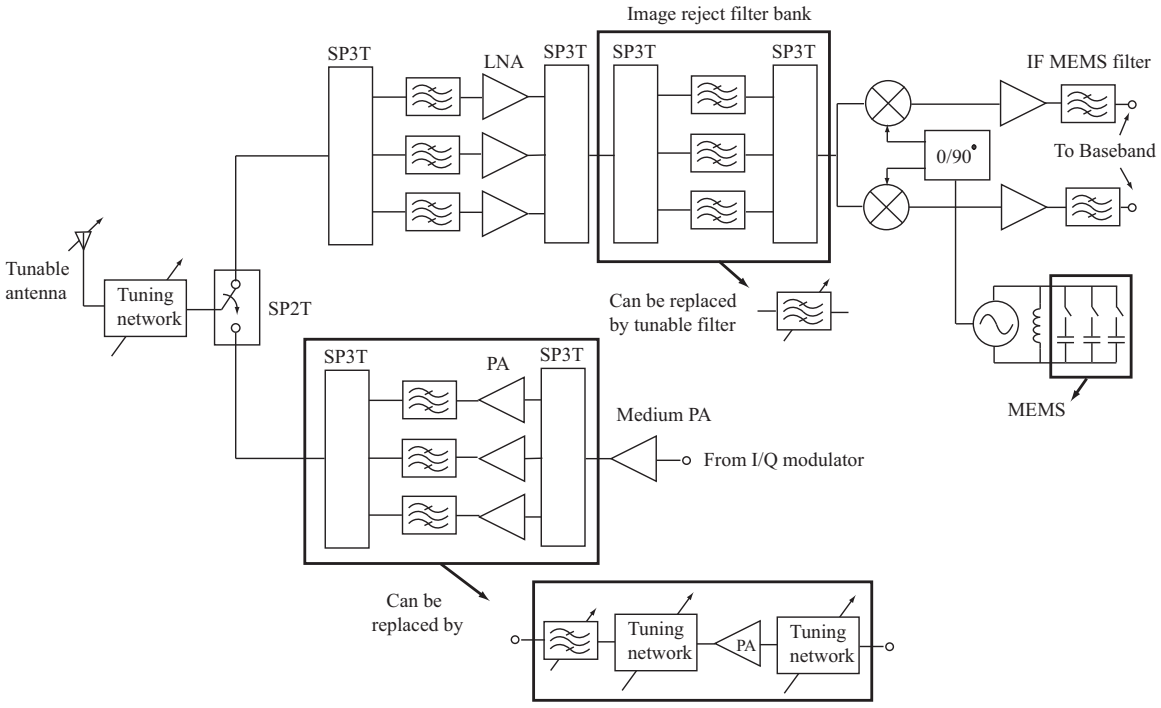


Figure 1.4: The block diagram of a multi-band wireless transceiver using RF MEMS technology.

1.4 Thesis Overview

This thesis comprises the design of different types of fixed and tunable RF MEMS filters from 6-18 GHz, including miniaturized differential filters for C- and Ku-Band applications, differential microstrip 6-10 and 10-16 GHz RF MEMS tunable filters, and coplanar-waveguide 12-18 GHz RF MEMS tunable filter. It also comprises the development of a packaging structure for microstrip RF MEMS topologies.

Chapter 2 covers the theory, design, fabrication, and measured results for miniaturized differential filters on high-resistivity silicon substrate. A novel lumped element topology is developed for a miniaturized filter suitable for differential integrated circuits at C- and Ku-bands. Differential circuits are immune against noise and because they do not generate even order harmonics their linearity is very good [32]. High-Q metal-air-metal (MAM) capacitors are used in the layout of the filter. The MAM capacitor makes the design very compact and improves the quality factor of the filter.

Chapter 3 explains the operation of wide-band microwave tunable filters and presents a microstrip wide-band RF MEMS tunable filter at 6.5-10 GHz. This filter employs the same filter

topology presented in chapter 2. The MAM capacitors are substituted by switched capacitor banks to make the tunable filter, and are based on RF MEMS capacitive switches in series with MAM capacitors. By changing the combination of up-state and down-state RF MEMS switches, the resonant and matching capacitors vary with very fine resolution and result in 16 filter responses that cover the desired frequency band. The measurement results are in very good agreements with simulations. The nonlinear behavior and power handling of the tunable filter is also studied. The two-tone intermodulation test is used to measure IIP_3 of the filler, and the results show a very low intermodulation products and high linearity. The design is also changed for a 10-16 GHz tunable filter and the full-wave simulation results are shown at the last section of the this chapter.

Chapter 4 presents a distributed coplanar waveguide (CPW) tunable MEMS filter which covers the 12-18 GHz frequency band. The half-wavelength CPW resonators are loaded by switched capacitor banks and coupled together by inductive inverters. Each switched capacitor bank includes eight unit-cells (RF MEMS capacitive switch in series with MAM capacitor). By switching the MEMS switches symmetrically around the middle of the resonator the filter is tuned with very fine resolution. The nonlinear behavior of the filter is also studied in this chapter

Chapter 5 covers the microstrip packaging structures for RF MEMS applications. Two different packages are discussed. The difference between the two structures is mostly in the transition design. In the first packaging structure, the transition is based on passing the microstrip line underneath the packaging ring, while in the second one, it is based on connecting the microstrip line inside the package to a coplanar waveguide line on the backside of the wafer using via-holes.

Chapter 6 discusses the RF MEMS system-level response in complex modulation systems such as Wide-band Code Division Multiple Access (WCDMA) systems. This chapter compares the circuit behavior of the RF MEMS switch as varactors with other well-known variable capacitors such as GaAs and BST varactors in typical multi-functional circuits for RF front ends such as impedance matching networks and tunable filters when they are excited by complex modulated signals such as WCDMA signals.

Chapter 7 is the conclusion and future work. The RF MEMS tunable filters can be designed for 2-6 GHz frequency range using novel topologies where many multi-band wireless communication systems are operating. It is also possible to design RF MEMS band-stop tunable filters for different frequency ranges by applying the idea of the switched capacitor bank. The idea of microstrip pack-

aging can also be used to package microstrip RF MEMS reconfigurable networks such as impedance tuners, phase shifters and tunable filters.

CHAPTER 2

Miniaturized Differential Filters For C- and Ku-Band Applications

2.1 Introduction

RF bandpass filters are essential for heterodyne and direct-conversion transceiver architectures. In heterodyne receivers, they are used as channel select filters after the antenna to reduce the level of adjacent channel interferences. They are also used as image reject filters before the first down-converter to reduce the level of image frequency since without this filter, the image frequency appears in the IF-band directly and can be much larger than the desired signal. In transmitters, they are used after power amplifiers to suppress the level of higher order harmonics generated by the nonlinearities in the transmitter circuitry [32][33]. They are typically integrated using off-chip components due to their relatively large size. Recently, miniature bulk acoustic wave resonators have been developed using AlN_3 resonators and have resulted in high-Q (500 - 2000) and excellent performance at 1-2.5 GHz [34]. However, these filters cannot handle a lot of power (typically 1 W) and are not yet demonstrated at 6-12 GHz. The goal of the work in this chapter is to build miniature planar filters, which are compatible with SiGe high-resistivity wafers for 6 GHz and 12 GHz communication systems. The filters must be able to handle power levels of the order of 1-4 W, and be compatible with SiGe fabrication procedures. Also, the filters must be compatible with differential circuits so as to eliminate the use of bulky and lossy off-chip Balun components. This chapter describes the effort in design, simulation, fabrication and measurement of these filters.

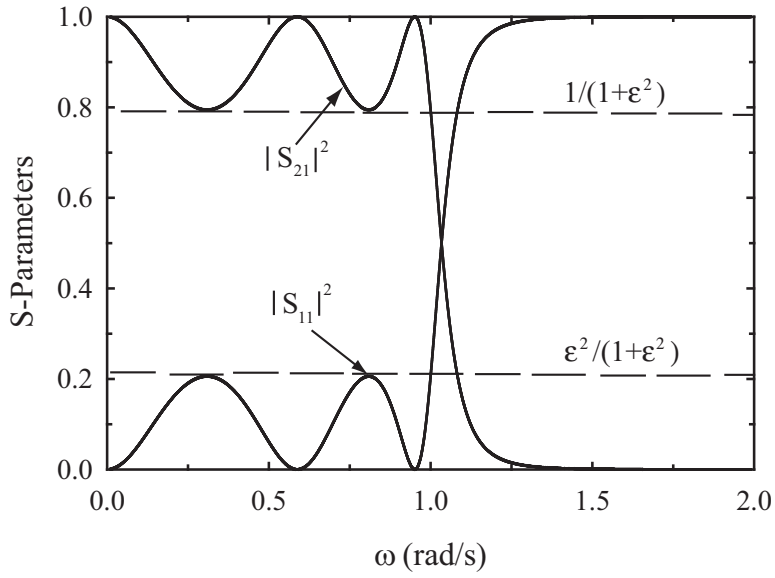


Figure 2.1: Ideal Chebyshev normalized low-pass filter S-parameters.

2.2 Design

2.2.1 Theory and Design Equations

Fig. 2.1 shows the S-parameters of an ideal Chebyshev normalized lowpass filter. It has equal ripples in the pass-band. The insertion loss and return loss at ripple level are normally expressed as

$$IL_{Max} = 10log_{10}(\frac{1}{|S_{21}|^2}) = 10log_{10}(1+\epsilon^2) \tag{2.1}$$

$$RL_{Min} = 10log_{10}(\frac{1}{|S_{11}|^2}) = 10log_{10}(1+\frac{1}{\epsilon^2}) \tag{2.2}$$

Thus the ripple in the pass-band can be controlled by the level of ϵ. To achieve equal-ripple behavior in the pass-band we let

$$|S_{21}(j\omega)|^2 = \frac{1}{1+\epsilon^2 T_N^2(\omega)} \tag{2.3}$$

$$IL = 10log_{10}(1+\epsilon^2 T_N^2(\omega)) \tag{2.4}$$

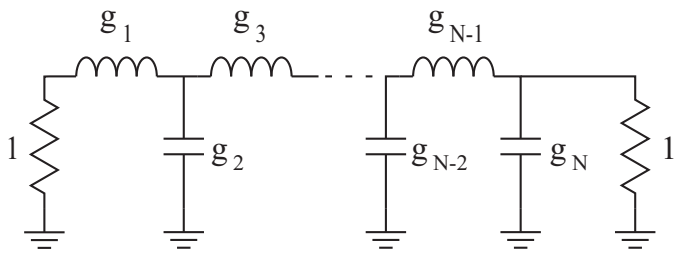


Figure 2.2: Ladder realization of a Chebyshev prototype network.

$T_N(\omega)$ is a function which must obtain the maximum value of 1 at the maximum number of points in the region $|\omega| < 1$ (except at $|\omega| = 1$). To satisfy the above specifications $T_N(\omega)$ must be chosen as [35]

$$T_N(\omega) = cos[N.cos^{-1}(\omega)] \tag{2.5}$$

Where N is the number of $T_N(\omega)$ zeros for $|\omega| < 1$. $|S_{21}(j\omega)|^2$ must be a polynomial in ω domain; otherwise it could not represent the response of a real network. In fact, $T_N(\omega)$ is known as the Chebyshev polynomial and is given by the formula [36]:

$$T_{N+1}(\omega) = 2\omega T_N(\omega) - T_{N-1}(\omega) \tag{2.6}$$

$$T_0(\omega) = 1\ ,\ T_1(\omega) = \omega \tag{2.7}$$

Since all the transmission zeroes for $|S_{21}(j\omega)|^2$ occur at infinity, the network can be synthesized as a low-pass prototype LC ladder network as in Fig. 2.2 [35][8][37]. An alternative realization of ladder networks uses impedance or admittance inverters which results in realizable element values for both the low-pass and bandpass filters at microwave and millimeter-wave frequencies. An ideal inverter is a lossless, reciprocal, frequency-independent, two-port network and its main property is the impedance (admittance) inversion. Fig. 2.3 shows an admittance inverter which is terminated in a load Y_L. By using inverters the Chebyshev LC ladder network can be synthesized entirely with inductors and inverters or capacitors and inverters as shown in Fig. 2.4 [35][8][37]. Explicit formulas for the general N^{th} order Chebyshev inverter coupled lowpass prototype are given in [36]:

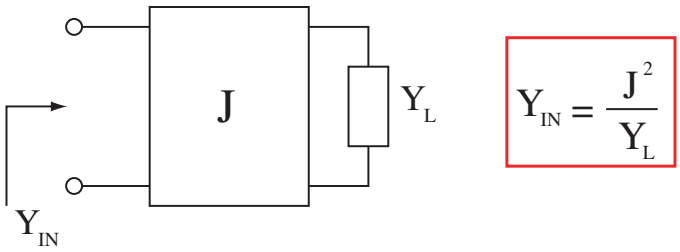


Figure 2.3: Circuit model of an admittance inverter.

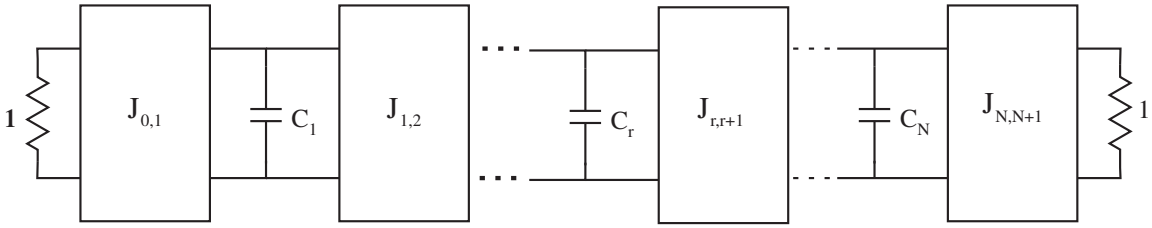


Figure 2.4: Inverter-coupled Chebyshev prototype low-pass filter.

$$\eta = \sinh[(\frac{1}{N})(\sinh^{-1}(\frac{1}{\epsilon})] \tag{2.8}$$

$$C_r = \frac{2}{\eta}.\sin[\frac{(2r-1)\pi}{2N}] \tag{2.9}$$

$$J^n_{r,r+1} = \frac{\sqrt{\eta^2 + \sin(r\pi/N)^2}}{\eta} \tag{2.10}$$

$$J^n_{0,1} = J^n_{N,N+1} = 1 \tag{2.11}$$

$$r = 1 \rightarrow N-1 \tag{2.12}$$

Where η is a function of the ripple in the pass-band and the degree of the filter (N), and is defined to simplify the calculations. Knowing the degree of the filter (N) and the ripple in the pass-band, and the parameter η, the values of C_r and $J_{r,r+1}$ are calculated for a normalized low-pass filter. The next step is to convert the low pass prototype into a bandpass filter with a specified center frequency and bandwidth. The band-edges at $|\omega| = 1$ in the low-pass prototype must map into the band-edges of bandpass filter at ω_1 and ω_2. The transmission zeroes at infinity in the lowpass must now occur at

both $\omega = 0$ and infinity. The mid-band of the lowpass prototype at $\omega = 0$ must map into the center of the pass-band in the bandpass filter. This can be achieved using the following transformation:

$$\omega_{LP} \rightarrow (\alpha)\Big[(\frac{\omega_{BP}}{\omega_0}) - (\frac{\omega_0}{\omega_{BP}})\Big] \tag{2.13}$$

For $\omega_{LP} = 1$ and $\omega_{LP} = -1$ we have

$$-1 = (\alpha)\Big[(\frac{\omega_1}{\omega_0}) - (\frac{\omega_0}{\omega_1})\Big] \tag{2.14}$$

$$+1 = (\alpha)\Big[(\frac{\omega_2}{\omega_0}) - (\frac{\omega_0}{\omega_2})\Big] \tag{2.15}$$

Solving two above equations simultaneously yields

$$\omega_0 = \sqrt{\omega_1 \omega_2} \tag{2.16}$$

$$\alpha = \frac{\omega_0}{\Delta\omega} \tag{2.17}$$

Where ω_0 is the bandpass filter center frequency, α is the bandwidth scaling factor, and $\Delta\omega = \omega_2 - \omega_1$. Applying this transformation to a two-pole inverter-coupled Chebyshev prototype lowpass filter results in a two-pole standard Chebyshev bandpass filter with parallel resonators and J-inverters (Fig. 2.5(a)). The element values for the normalized bandpass filter are calculated from

$$C_{BP}^n = \frac{\alpha C_r}{\omega_0} \tag{2.18}$$

$$L_R^n = \frac{1}{\alpha C_r \omega_0} \tag{2.19}$$

As mentioned before, C_r and $J_{1,2}^n$ are the parallel capacitor and the admittance inverter for a 2-pole normalized low-pass prototype filter [35]. The shunt inductance is inversely proportional to α and for narrow bandwidths, it can be too small to be physically realizable. Therefore, the entire admittance of the filter (including source and load) can be scaled by a (A/α) factor, where A is an

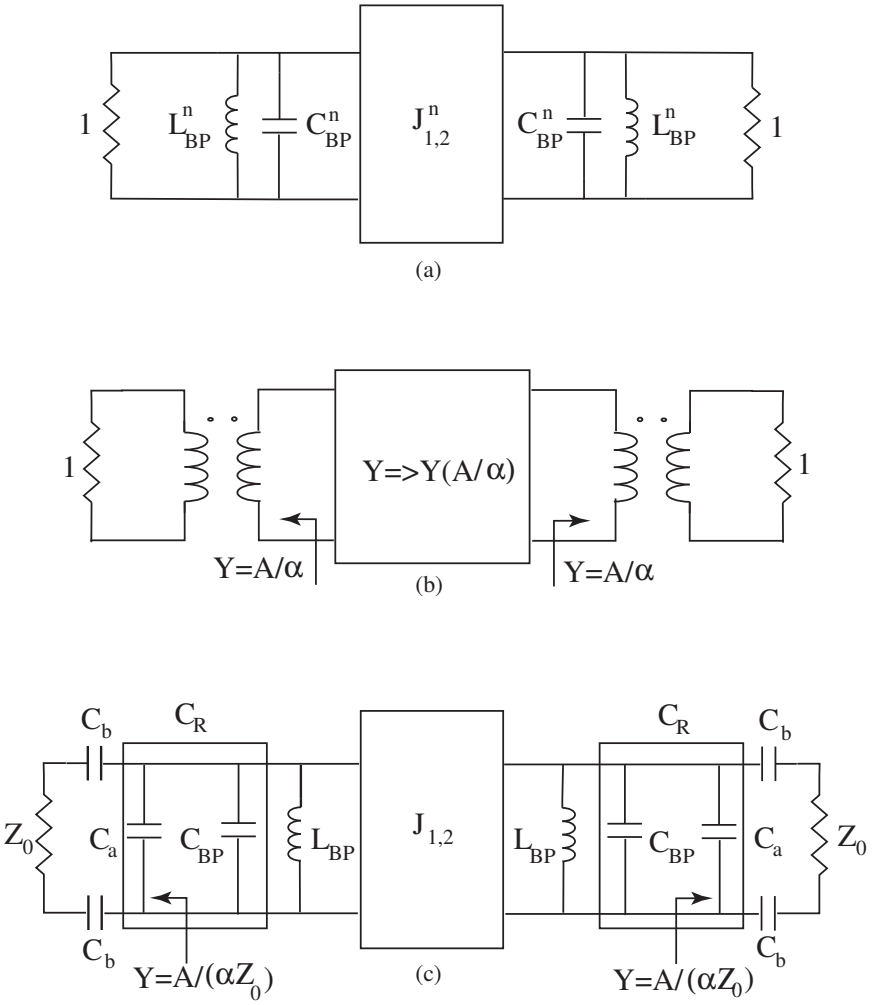


Figure 2.5: (a) A standard Chebyshev bandpass filter, (b) admittance scaling, (c) practical transformer realization using capacitive dividers .

arbitrary scaling factor, to result in realizable element values, and an impedance transformer must be inserted between the filter and its terminations (Fig. 2.5(b)). To realize this ideal transformer at high frequencies, a narrow-band impedance transformer is implemented using C_a and C_b capacitors in a differential fashion (Fig. 2.5(c)). The values of C_a and C_b can be found using the two conditions at the source and load

$$\begin{aligned} Re(Y(j\omega_0)) &= \frac{A}{\alpha Z_0} \\ Im(Y(j\omega_0)) &= 0 \end{aligned} \tag{2.20}$$

Where Z_0 is the differential line impedance at the input and output of the filter (100 Ω for this design). Solving (2.20) gives the values of C_a and C_b [35]

$$C_a = \frac{-\sqrt{\frac{\alpha}{A} - 1}}{\frac{\alpha}{A}\omega_0 Z_0} \tag{2.21}$$

$$C_b = \frac{2}{Z_0\omega_0\sqrt{\frac{\alpha}{A} - 1}} \tag{2.22}$$

C_a is a negative capacitor, but it is always smaller than C_{BP}, so it can be absorbed into C_BP and form the capacitor named C_R.

Fig. 2.6 shows the implementation of the J-inverter and parallel bandpass inductors using a practical transformer. The values of $J_{1,2}$ and L_{BP} can be calculated based on the self-inductance of the transformer (L_R), and the transformer coupling factor (k)

$$J_{1,2} = \frac{\frac{\alpha}{A}}{\omega_0 L_{eq}} \tag{2.23}$$

$$L_{eq} = \frac{L_R(1 - k^2)}{k} \tag{2.24}$$

$$L_{BP} = L_R(1 - k^2) \tag{2.25}$$

Fig. 2.7(a) shows the finalized lumped element differential filter. Using (2.15) through (2.24), the values of C_M, C_R, k, and L_R can be calculated based on ω_0, Z_0, α, A, C_r, and $J_{1,2}$ for a specific frequency. The closed-form equations for the lumped elements of the differential filter of Fig. 2.7(a) are now summarized below

$$C_M = C_b = \frac{2}{Z_0\omega_0\sqrt{\frac{\alpha}{A} - 1}} \tag{2.26}$$

$$C_R = \frac{AC_r}{Z_0\omega_0} - \frac{\sqrt{\frac{\alpha}{A} - 1}}{\frac{\alpha}{A}Z_0\omega_0} \tag{2.27}$$

$$k = \frac{J_{1,2}}{\alpha C_r} \tag{2.28}$$

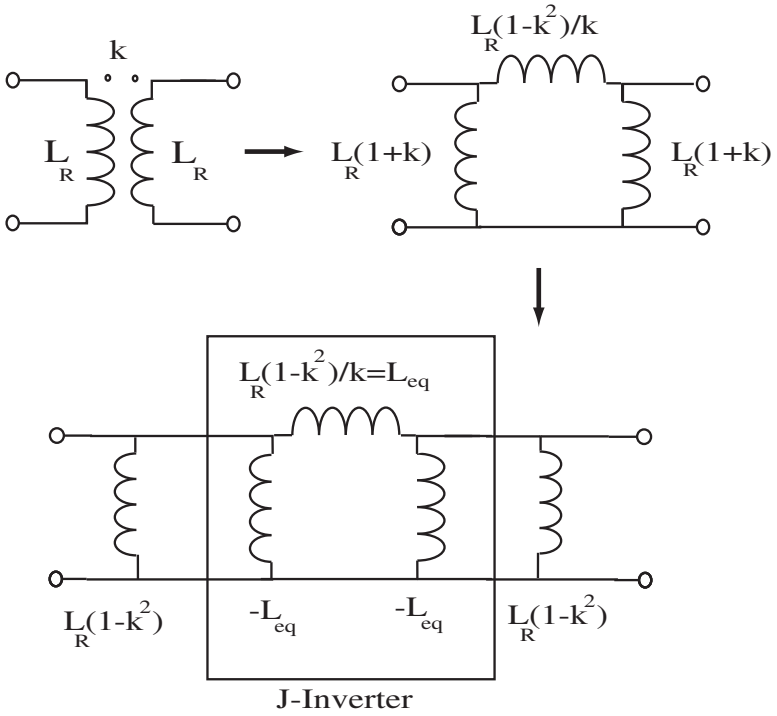


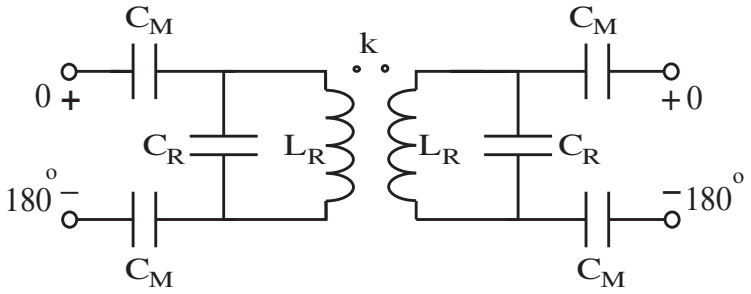
Figure 2.6: J-Inverter implementation using a practical transformer.

$$L_R = \frac{Z_0}{AC_r\omega_0(1-k^2)} \tag{2.29}$$

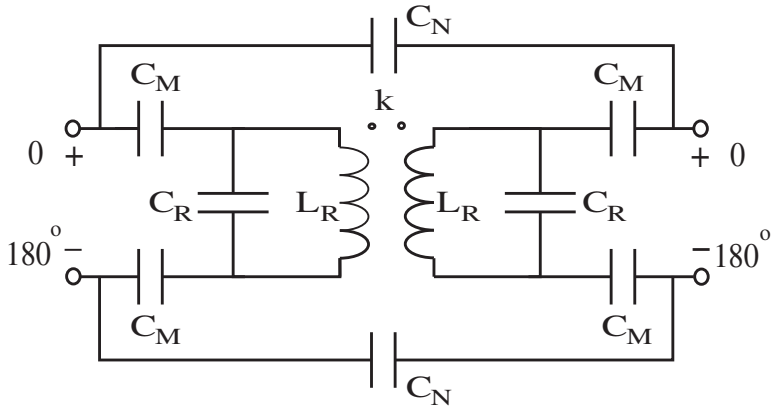
By connecting the input of the differential filter to its output using capacitor C_N (Fig. 2.7(b)) we achieve two transmission zeroes outside the pass-band. The location of transmission zeroes are controlled independently by varying the C_N capacitance value. By using ADS [38] and adjusting the value of C_N the transmission zeroes are located at the desired frequency positions.

2.2.2 Lumped Filter Design and Simulation

Table 6.5 presents the design parameters for C and Ku-band differential two-pole and image reject filters (Fig. 2.7). The input and output impedances are considered 100 Ω differential. The image frequency is the position of the transmission zero at the left side of the pass-band. Table 2.2 presents the lumped element values for the two-pole and image reject filters. These values are calculated using the design equations extracted in the previous section. To achieve realizable element values, the impedance scaling factor, A, is chosen to be 2.5 at the center frequency. Figs. 2.8 and 2.9 show the simulation results for the 6 and 12 GHz two-pole and image reject filters,



(a)



(b)

Figure 2.7: (a) Two-pole bandpass and (b) image-reject differential filters.

Table 2.1: Design parameters for 6 and 12 GHz differential filters.

Filter	f_0 (GHz)	$Ripple$ (dB)	N	$BW(1/\alpha)$	f_{image} (GHz)
C – Band	6	0.15	2	0.1	–
C – Band(I.R.)	6	0.15	2	0.1	5.4
Ku – Band	12	0.15	2	0.1	–
Ku – Band(I.R)	12	0.15	2	0.1	10.4

Table 2.2: Lumped element values for 6 and 12 GHz differential filters.

Filter	L_R (nH)	C_R (fF)	k	C_M (fF)	C_N (fF)
C – Band	1.1	0.51	0.1	0.32	–
C – Band(I.R.)	1.1	0.51	0.1	0.32	0.16
Ku – Band	0.57	0.25	0.1	0.16	–
Ku – Band(I.R)	0.57	0.25	0.1	0.16	0.16

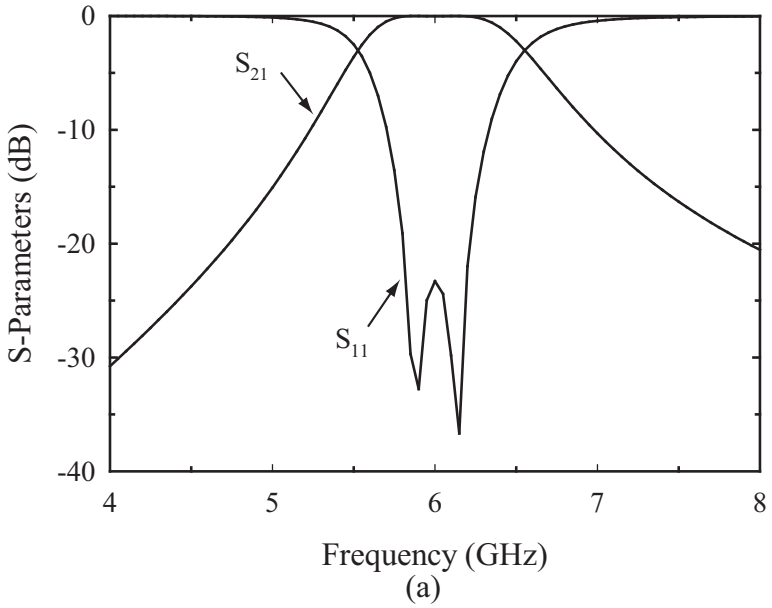
respectively, using Agilent-ADS [38]. These preliminary results prove the validity of the design equations. The filters are considered lossless for this purpose, and the effect of loss is studied in detail in section 2.3.

2.3 Layout Implementation

The major reason to choose these topologies is the good potential of miniaturization. Similar topologies have been used in [39] and [40] to achieve miniaturized filters at 38 and 60 GHz, respectively. The layout implementation is the challenging part of the C and Ku-band filter designs. The substrate is a high-resistivity silicon substrate (ρ = 1000 $\Omega.cm$, ϵ_r = 11.9, thickness = 500 μm) since the filters have to be compatible with new SiGe wafers.

2.3.1 Transformer Implementation

The inductor values at 6 and 12 GHz are around 1.1 and 0.57 nH, respectively. These values are achieved using a 150 μm-wide 2.5 μm-thick gold electroplated microstrip line on the silicon substrate. The length of the microstrip line is 1.2 mm at 6 GHz and 0.7 mm at 12 GHz. This is much



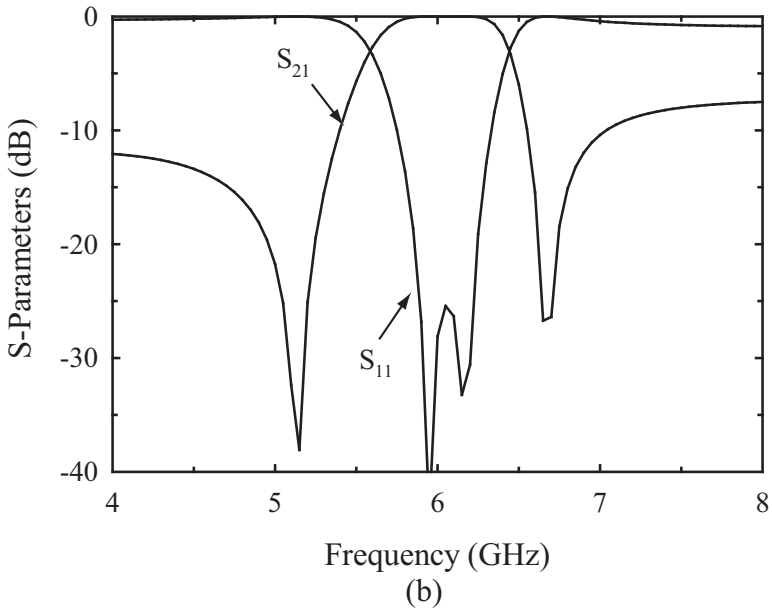


Figure 2.8: Simulated two-pole (a), and image-reject (b) S-parameters for the 6 GHz ideal filters.

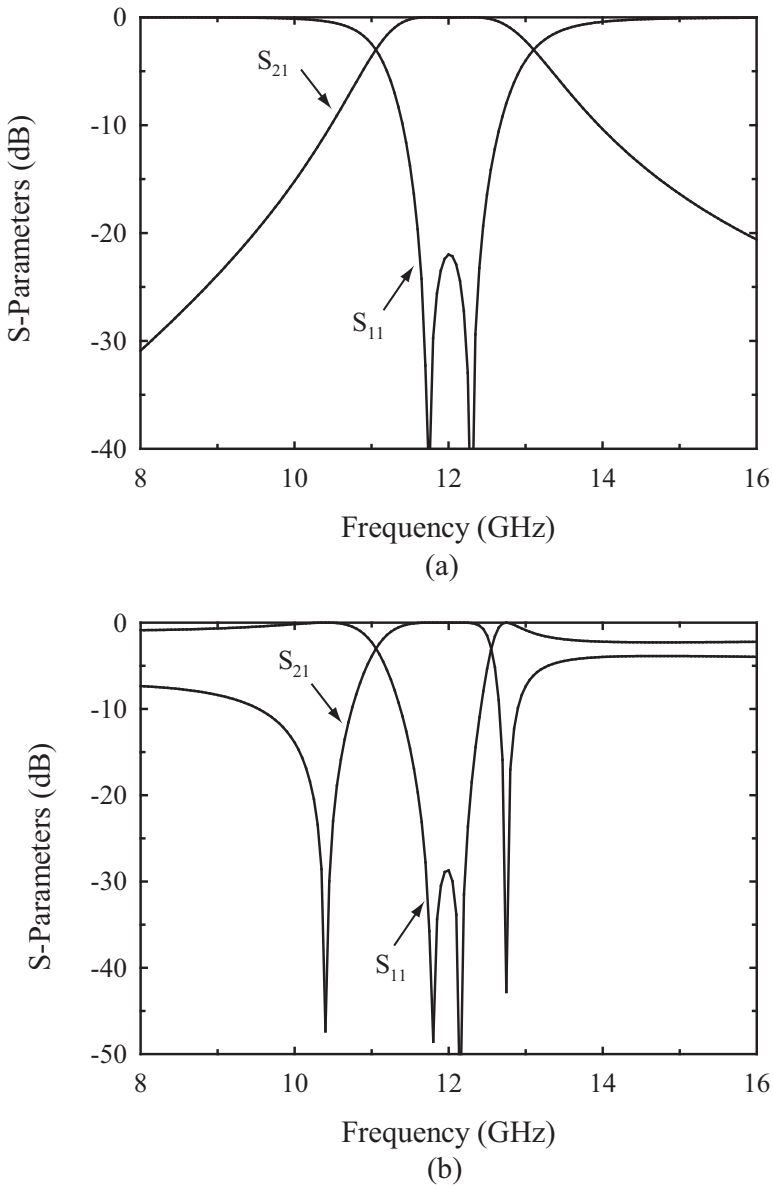


Figure 2.9: Simulated two-pole (a) image-reject (b) S-parameters for the 12 GHz ideal filters.

better than the achievable Q using a small loop inductor at 6 GHz (Q = 15). The corresponding Q of inductors, calculated using full-wave analysis (Agilent-Momentum [38]), is around 40 at 6 GHz (0.57 nH) and 35 at 12 GHz (1.1 nH). To calculate the Q of the inductors, the simulated full-wave S_{11} from the method of Moment is fitted to the simulated S_{11} of a series lumped element RL circuit at the desired frequencies. Based on the values of R and L, the Q of inductor is calculated from:

$$Q = \frac{2\pi f L}{R} \tag{2.30}$$

The transformer with k = 0.1 is designed as a microstrip coupled-line and simulated with Momentum to achieve the desired values of self-inductance, coupling factor and quality factor for each filter. The coupling factor is determined by the distance between the two parallel lines, and is 30 and 40μm at 6 and 12 GHz, respectively. Fig. 2.10 shows the layout of the transformers for the 6 and 12 GHz filters.

2.3.2 Capacitor Implementation

A combination of inter-digital and metal-air-metal (MAM) structure is used to make the high-Q capacitors. Typically, practical MAM capacitors are very low (below 100 fF), and much larger capacitance values are needed (0.5 pF and 0.3 pF). This is achieved using a combination of realizable 100 μm$\times$ 70 μm MAM cells and inter-digital capacitors. The height of the bridges is 1.5 μm, and is obtained using a polyamide (PMMA) sacrificial layer. The layout of each capacitors is also simulated and optimized using Momentum. Fig. 2.11 shows the layout of the parallel capacitors (C_R) for the 6 and 12 GHz filters. The gaps between MAM cells help to remove the sacrificial layer underneath the bridge in fabrication process at the release step. The total capacitor length is still very small (around 400 μm and 340 μm), so the MAM bank is considered as a lumped element at 6 and 12 GHz. The layout for the input/output (C_M) and feedback (C_N) capacitors are implemented in the same way. It is easy to integrate these capacitors using the 1-2 μm-thick oxide layers between metal 2 and metal 3 in the SiGe process.

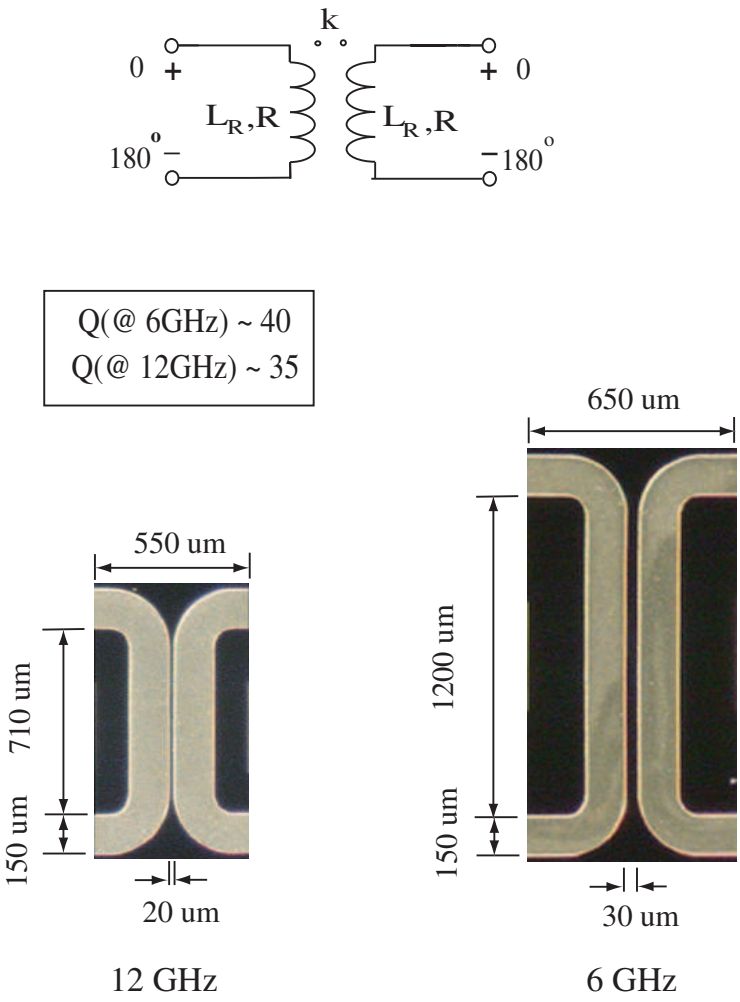


Figure 2.10: Transformer layouts for 6 and 12 GHz filters.

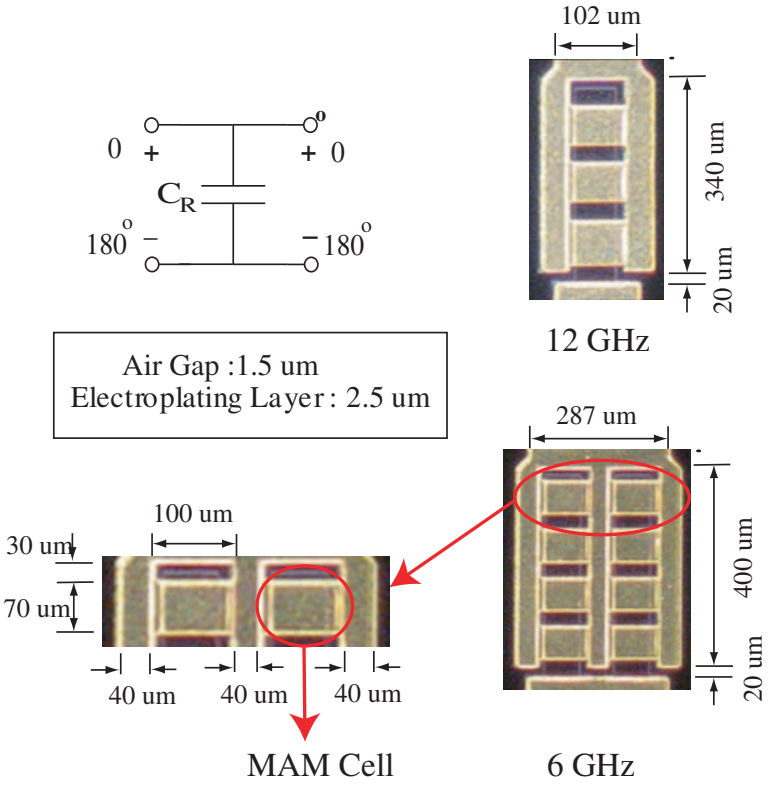


Figure 2.11: Capacitor layouts for the 6 and 12 GHz filters.

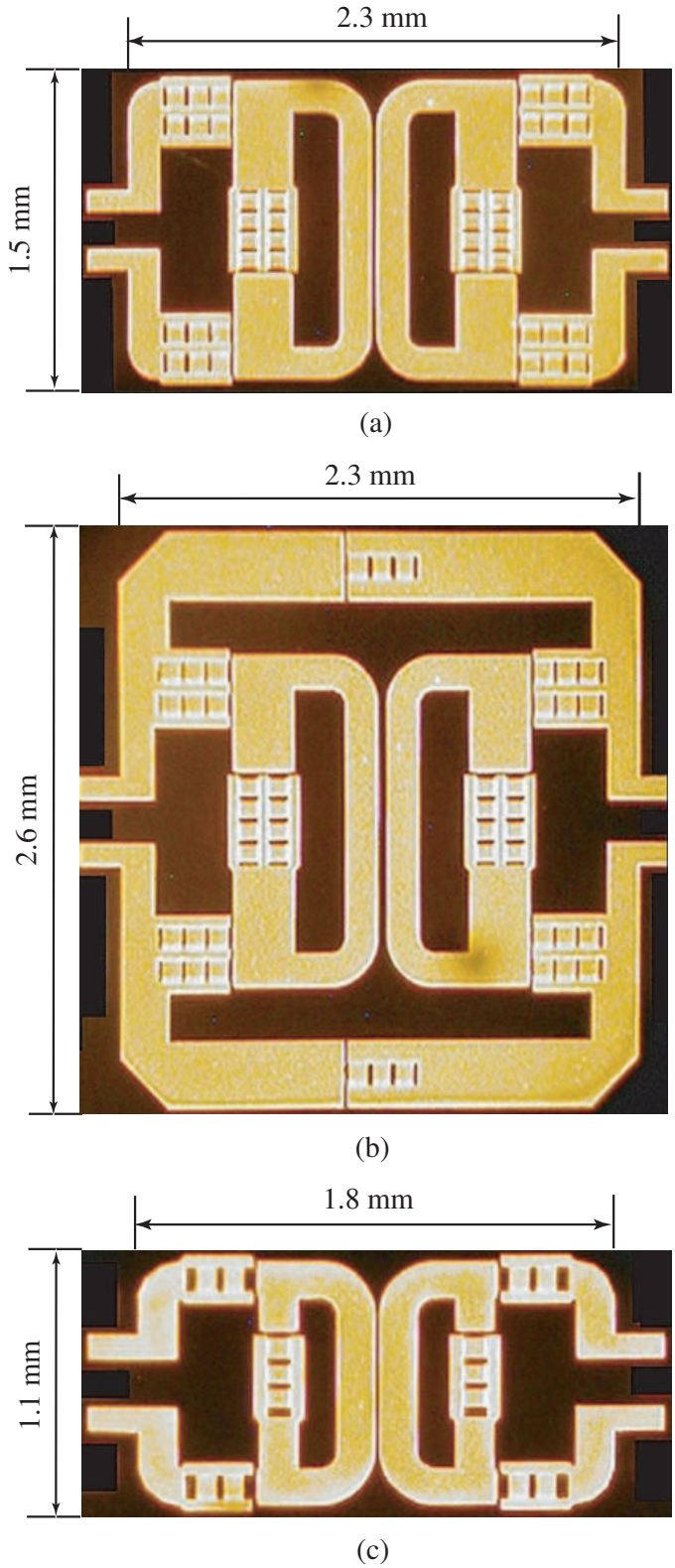


Figure 2.12: Final filter layouts for (a) two-pole bandpass at 6 GHz (b) two-pole bandpass at 12 GHz and (c) image-reject differential filters.

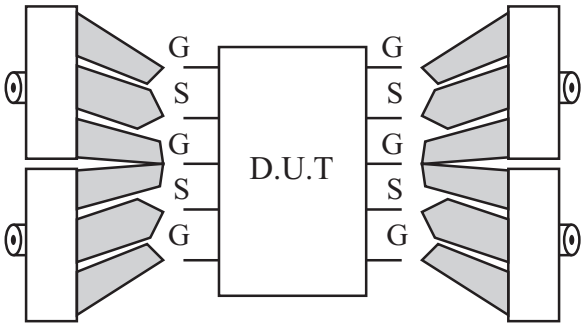


Figure 2.13: GSGSG probe for differential measurement.

2.3.3 Filter Implementation

Fig. 2.12 shows fabricated two-pole bandpass filters for 6 and 12 GHz and an image reject filter for 6 GHz. To consider all the coupling effects, the whole filter is simulated using Momentum. Because the elements are close together, the electromagnetic coupling effects should also be considered in the model of the filter to optimize the filter response. As a result, the final values of the optimized elements, especially C_M, are a little bit different from the values given in Table 2.2. The image reject filter full-wave simulation at 12 GHz does not result in the same position of the transmission zeroes based on circuit simulation. This is due to the parasitic effects of the microstrip lines which connect the feedback capacitor (C_N) to the input and output of the filter. The filters are excited using differential input and output lines, which are compatible with a GSGSG (G $\rightarrow$ Ground, S $\rightarrow$ Signal) differential probe with a pitch of 150 μm (Fig. 2.13). Fig. 2.12 does not show the feeding arrangement due to space considerations, and several different differential feeds are fabricated (with λ_{eff}/4 stub, without stubs, and with a circular ground-plane ring). The best result is obtained without any λ_{eff}/4 stubs or circular ground-plane ring.

2.4 Fabrication

The miniaturized filter is fabricated on a 500 μm high resistivity silicon substrate using microstrip lines and metal-air-metal capacitors. The metal-air-metal capacitor is suspended 1.5 μm above the first metal layer. The microstrip conductor, and the top plate of MAM capacitors are electroplated to 2.5 μm thick using low stress gold solution. Fig. 2.14 shows the major steps in miniaturized filter fabrication:

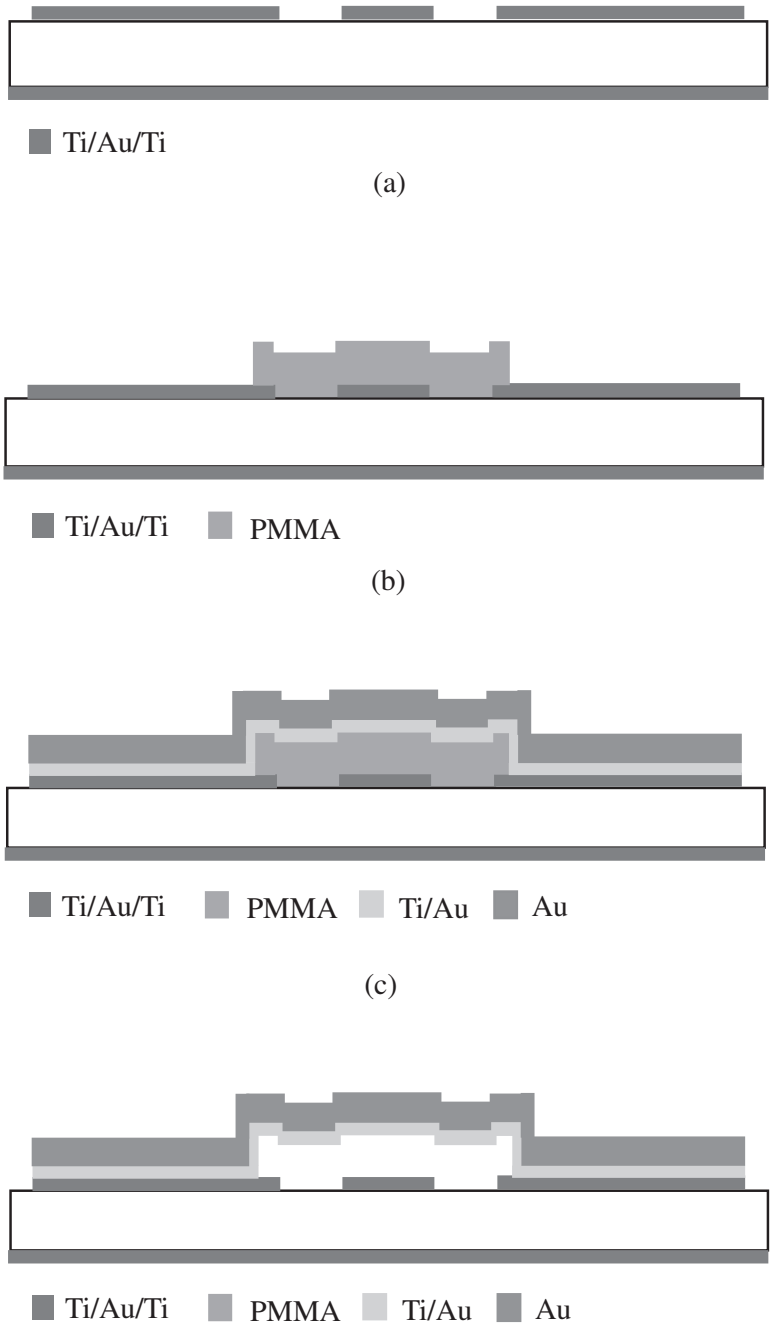


Figure 2.14: Fabrication steps of a miniaturized filter with MAM capacitors.

1) 6000 Å Ti/Au/Ti layer metal evaporation on the back side of the silicon wafer as the microstrip ground plane (Fig. 2.14 (a)).

2) 6000 Å Ti/Au/Ti first metal evaporation to pattern the microstrip lines and the bottom plate of the MAM capacitor (Fig. 2.14(a)).

3) Sacrificial layer deposition to make a 1.5 μm gap between the bottom and top plates of the MAM capacitors (Fig. 2.14(b)).

4) Evaporating 5000 Å Ti/Au layer on top of the sacrificial layer as a seed layer for MAM capacitor top-plate (Fig. 2.14(c)).

5) 2 μm gold electroplating of the microstrip conductor, and the top-plate of MAM capacitors to reduce the ohmic loss and skin depth effect (Fig. 2.14(c)).

6) Removal of the sacrificial layer underneath the top-plate of the MAM capacitors (Fig. 2.14(d)).

2.5 Measured Results

Fig. 2.15 presents the differential filter measurement setup. Two 0-180° hybrid couplers are used as baluns to provide differential excitation for the filters. As is well known, only the odd mode should be generated for differential circuits. The phase and amplitude imbalance for the couplers should be as small as possible. (Gain Balance $<$ 2 dB, Phase Balance $<$ 10°). To measure the 6 GHz filter response, two 4-12.4 GHz couplers are used, and to measure the 12 GHz filter response two 6-26.5 GHz couplers are used [41]. The LRRM differential calibration technique is employed to calibrate out the effect of the cables, the input and output couplers and differential probes.

Fig. 2.16 presents the full-wave simulated and measured response for the 5.6 GHz bandpass and 5.6 GHz image reject filters. Also, Fig. 2.17 shows the simulated and measured response for the 11.6 GHz bandpass filter, all measured in a differential mode. The frequency shows a downward

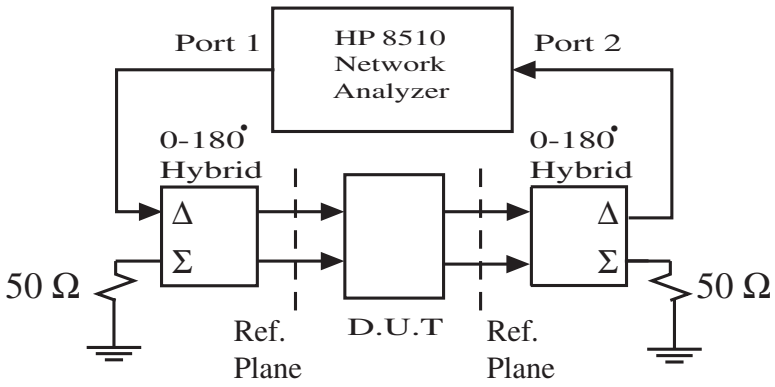


Figure 2.15: Measurement setup to measure differential filter characteristics.

Table 2.3: Summary of measured differential filter characteristics.

Filter	S_{21} (dB)	S_{11} (dB)	BW (%)	Q_u
$C-$ Band (Meas.)	-3.6	< -20	10	25
$C-$ Band (Sim.)	-3.5	< -18	10	30
$C-$ Band.I.R. (Meas.)	-3.6	< -18	10	25
$C-$ Band.I.R. (Sim.)	-3.5	< -17	10	30
$Ku-$ Band (Meas.)	-4.0	< -20	10	20
$Ku-$ Band (Sim.)	-3.8	< -20	10	25

shift since the height of the sacrificial layer was less than 1.5 μm due to process inaccuracy, and the simulations were re-done to take this into account. In general, the response agrees very well with theory.

In the case of the image-reject filter, the transmission null is clearly observed at 4.8 GHz. It is easy to prove that a deep null can only be obtained if the filter is excited differentially with low amplitude and phase errors, which is easy to do using differential amplifiers. The 11.6 GHz filter also shows a very good response and agrees very well with theory. Note that the C and Ku-Band filters are indeed very small (2.3×1.5 mm^2 and 1.8×1.1 mm^2 in area) making them one of the smallest differential filters to-date. Table 2.3 shows a summary of measured characteristics for the filters.

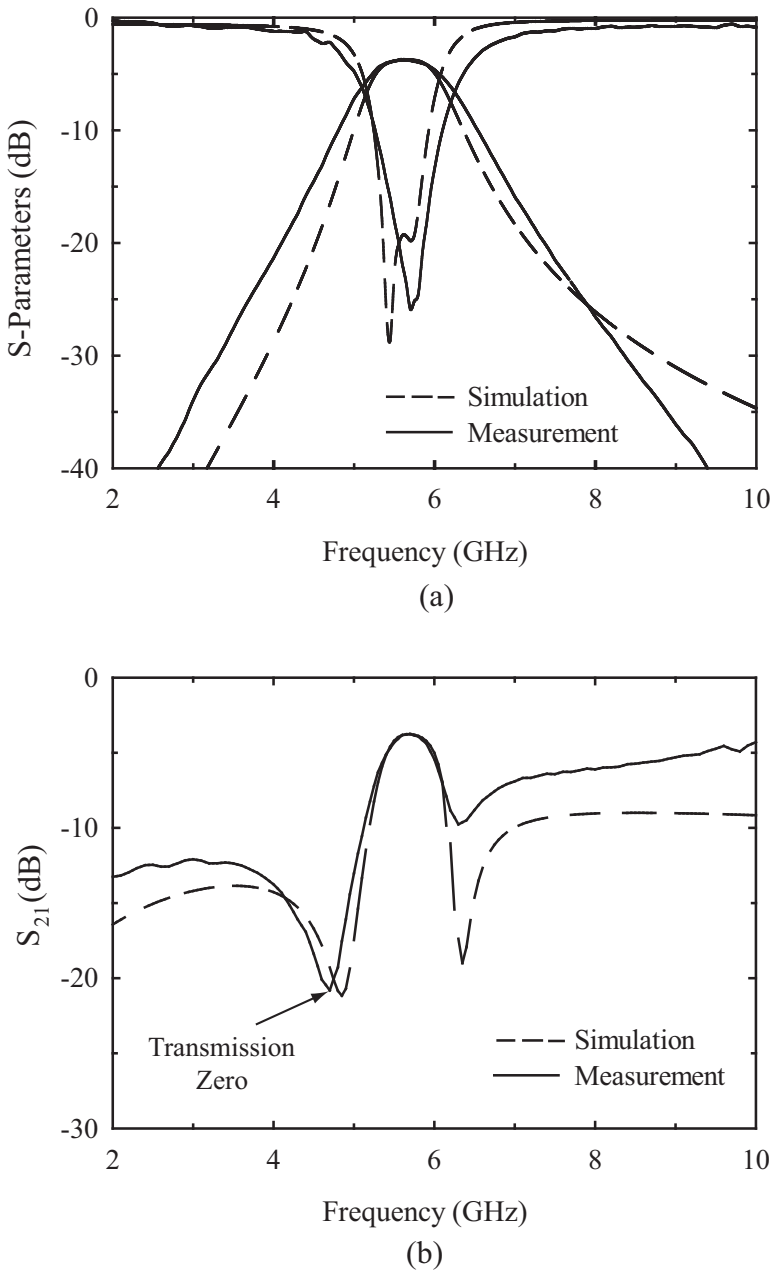


Figure 2.16: Measured and simulated S-parameters for (a) the C-band two-pole filter, and (b) the C-band image reject filter. All measurements are made in a differential mode.

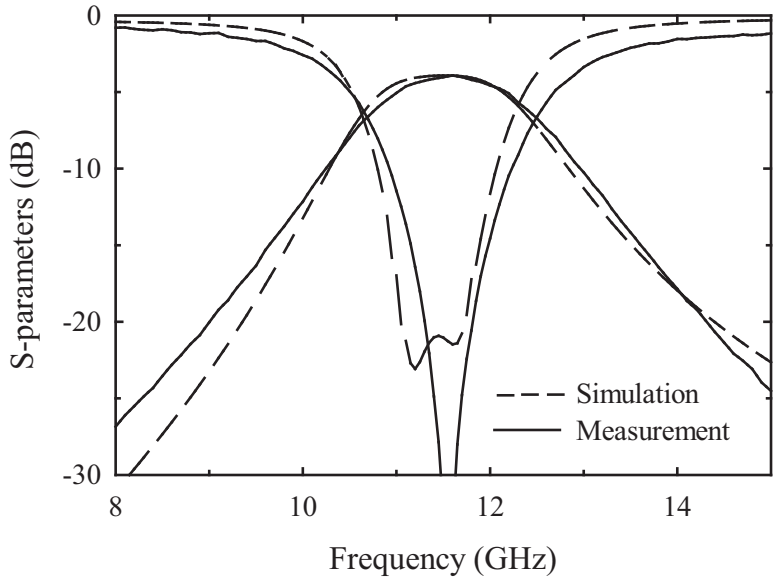


Figure 2.17: Measured and simulated S-parameters for Ku-band two-pole filter, measurement is made in a differential mode.

2.6 Conclusion

A new set of differential filters suitable for C and Ku-Band applications are developed. The filters are integrated on 500 μm-thick high-resistivity silicon substrates which are compatible with the new SiGe processes. A lumped-element approach is used to result in a very small size and high-Q metal-air-metal (MAM) capacitors are integrated in the filter structure for a low-loss design. The measured insertion loss of differential, 6 and 12 GHz, 10% bandwidth, 2-pole Chebyshev filters are 3.6 dB and 4 dB, respectively. An image reject filter at 6 GHz results in an image rejected of 20 dB and an insertion loss of 3.6 dB. These filters are ideal for integration in modern-day SiGe and CMOS transceivers for wireless LAN and satellite communications. Alternatively, the filters could be fabricated on ceramic substrates (ϵ_r=10) for even lower loss response.

CHAPTER 3

Differential 2-Pole 6-10 and 10-16 GHz RF MEMS Tunable Filters

3.1 Introduction

As mentioned in chapter 1, The most practical implementation od a wide-band tunable filter is based on Yttrium-Iron-Garnet (YIG) resonators. Fig. 3.1 shows the measured insertion loss for a 1-2 GHz two-pole YIG tunable filter from Micro Lambda company [42] . The bandwidth and the shape of the filter in the pass-band is approximately fixed for the whole tuning range. The filter has an unloaded Q around 500 due to high-Q magnetic resonators. However, YIG filters are bulky and can not be easily miniaturized for wireless communications. They also consume considerable amount of DC power (0.75 - 5 W depending on the frequency range), and their linearity is not high ($\mathrm{IIP}_3 \approx$ 24 dBm). Fig. 3.2 shows IIP_3 measurements for the 1-2 GHz YIG filter. An alternative to YIG filters is based on miniaturized planar filters with solid-state, ferroelectric or MEMS devices. As discussed in chapter 1, MEMS devices are very good candidates compared to the other ones. MEMS switches and varactors have very low loss, they do not consume any DC power, and their linearity is excellent (IIP_3>40 dBm) [20][21].

There are two different types of frequency tuning methods for MEMS-based filters, analog and digital. Analog tuning provides continuous frequency variation of the pass-band, but the tuning range is limited. For example, the tuning range in [43],[44], [45] is 4.2%, 10%, and 14% respectively. In digital MEMS filters, discrete center frequencies and wide tuning ranges are possible. Young [50], and Brank [51] presented excellent tunable filters with high frequency resolution at 0.8 - 2GHz. However, existing digital MEMS filters at microwave frequencies (f>3 GHz) do not have

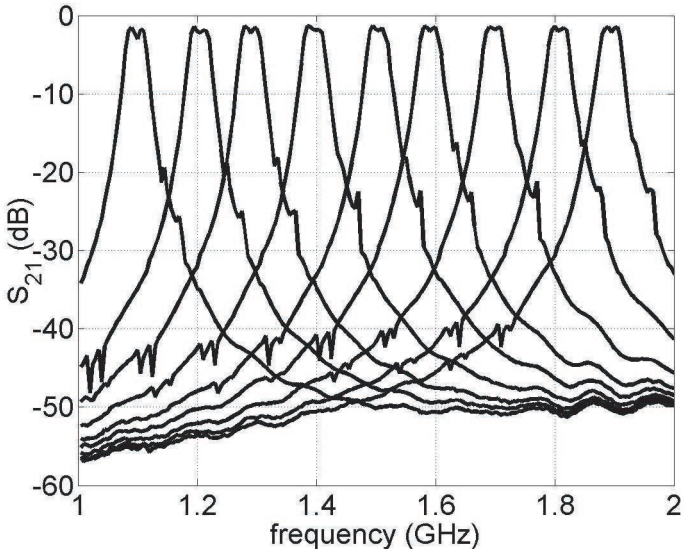


Figure 3.1: Insertion loss of a 1-2 GHz 2-pole tunable YIG filter.

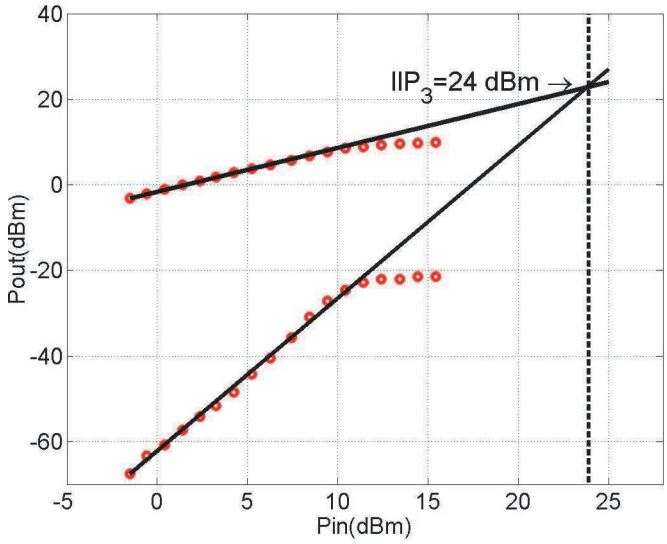


Figure 3.2: IIP3 measurement for a 1-2 GHz YIG filter (f=1.5 GHz).

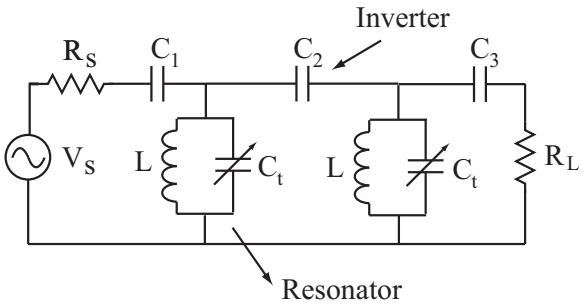


Figure 3.3: Simple bandpass filter tuned by lumped variable capacitances.

enough resolution to result in near continuous coverage of the frequency band. The MEMS filter in [46] shows four states (2-bit filter) and a 44% tuning range, with poor frequency resolution. The filter in [47] has two states (1-bit filter) and can switch from 15 to 30 GHz. Other designs have two states and lower tuning range: 28.5% in [48] and 12.8% in [49].

In this chapter, we present a 4-bit digital differential tunable filter with 44% tuning range from 6.5 to 10 GHz. The frequency band is covered by 16 filter responses with very fine frequency resolution. Practically, this filter behaves like a continuous-type tunable filter. To achieve such a high tuning resolution, capacitive MEMS switches are connected in series with high-Q MAM capacitors to make a capacitor bank. As a result, the capacitor variation can be controlled accurately by choosing the correct values for MAM capacitors. The MEMS capacitor bank is inserted in a lumped differential filter to result in a miniature 6.5-10 GHz tunable filter. A study of nonlinearities for 6.5-10 GHz filter is also presented in this chapter. The chapter concludes by a study of the design and full-wave simulation of a 4-bit, 10-16 GHz differential tunable filter.

3.2 6-10 GHz Filter Design

3.2.1 Tunable Filter Topology

Choosing a right filter topology to tolerate the variation of shape and bandwidth in its pass-band when the filter is tuned over a wide band is a very important design aspect of these kind of filters. Many electronically tunable filters employ variable capacitors. Fig. 3.3 shows a filter configuration that is a convenient way to realize a filter with such tuning capacitors. This topology is based on fixed inductors and fixed coupling capacitors. In many practical applications, it is desired to

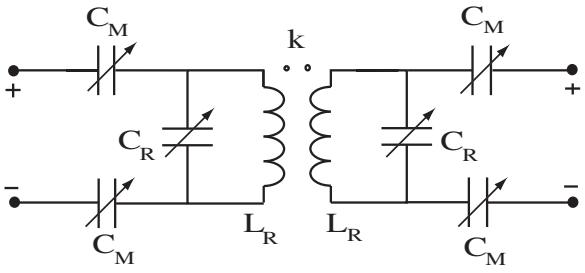


Figure 3.4: Lumped model for a two-pole differential tunable filter with constant fractional bandwidth.

maintain a constant bandwidth (Δf) in the tuning range. Unfortunately, the filter shown in Fig. 3.3 does not show this behavior. As the filter is tuned, the bandwidth of the filter increases with the center frequency, f_0, as f_0^3 [8]. To preserve the shape of the filter pass-band, the external Q's of the end resonators should increase linearly with f_0. The external Q of the filter in Fig. 3.3 decreases with f_0 as $1/f_0^3$. Therefore, the tunable filter in Fig. 3.3 has very strong variation in the pass band width and the shape as the filter is tuned.

References [8] and [15] discuss the condition of obtaining nearly constant bandwidth in tunable coaxial, waveguide filters and stripline comb-line filters respectively. Reference [4] surveys the literature on tunable filters up to 1991 and presents some discussion for obtaining constant bandwidth. References [53] and [54] deal with microstrip versions of the striplines treated in [15]. Reference [52] presents a two-resonator filter structure with *capacitive* tuning and *magnetic* coupling. This combination of *capacitive* tuning and *magnetic* coupling gives a much weaker variation of bandwidth with frequency since the bandwidth tends to vary directly with the center frequency f_0 instead as f_0^3 (as opposed to the case of *capacitive* tuning and *capacitive* coupling). In this case, the external Q's of the end resonators vary as $1/f_0$ (instead of linear variation desired for external Q's) which is still not ideal but is much better than the *capacitive* tuning and *capacitive* coupling case.

The differential filter was discussed in chapter 2 is a type of filter with *capacitive* tuning and *magnetic* coupling, so it has weak bandwidth variation over the tuning range which is desirable as a wide-band tunable filter. To compensate the nonlinear variation of external Q's of end resonators with center frequency, the coupling capacitors at the input and output (C_M) are also considered

Table 3.1: Element values for the tunable lumped filter.

f_0 (GHz)	$6.5-10$	$C_{R(Max)}$ (pF)	0.42
Z_0 (Ω)	100	$C_{R(Min)}$ (pF)	0.14
k	0.072	$C_{M(Max)}$ (pF)	0.21
L_R (nH)	1.4	$C_{M(Min)}$ (pF)	0.09
$\frac{C_{M(Max)}}{C_{M(Min)}}$	2.3	$\frac{C_{R(Max)}}{C_{R(Min)}}$	3.1

tunable (Fig. 3.4). This preserves the shape of the tunable filter pass-band.

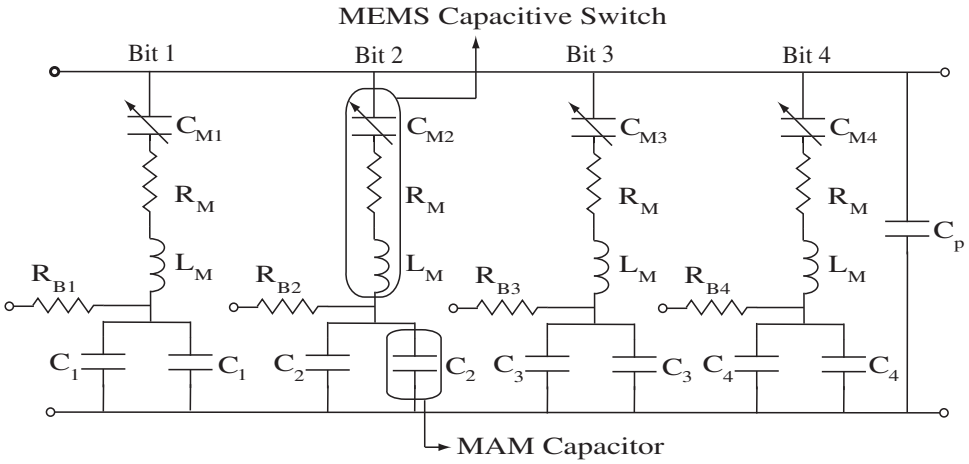
3.2.2 Tunable Filter Design and Simulation

The response of the differential filter of Fig. 3.4 can be tuned over a wide frequency range by varying C_R. As mentioned before, the shape and relative bandwidth of the filter is approximately fixed due to the filter topology, i.e, capacitive tuning with an inductive inverter [55]. The input/output matching is maintained better than 16 dB over the tuning range by varying C_M. Table 3.1 presents the element values of a 2-pole, 5% bandwidth (Chebyshev, equi-ripple), 6.5-10 GHz differential tunable filter. The filter is first designed at 10 GHz using design equations for a two-pole differential filter in chapter 2, with $A = 1.4$ and $Z_0 = 100\ \Omega$. Next, C_R and C_M capacitors are varied to achieve a filter response down to 6.5 GHz using Agilent ADS [38]. To achieve a 40% tuning range or more, $C_{R(Max)}/C_{R(Min)}$ = 3.1 and $C_{M(Max)}/C_{M(Min)}$ = 2.3.

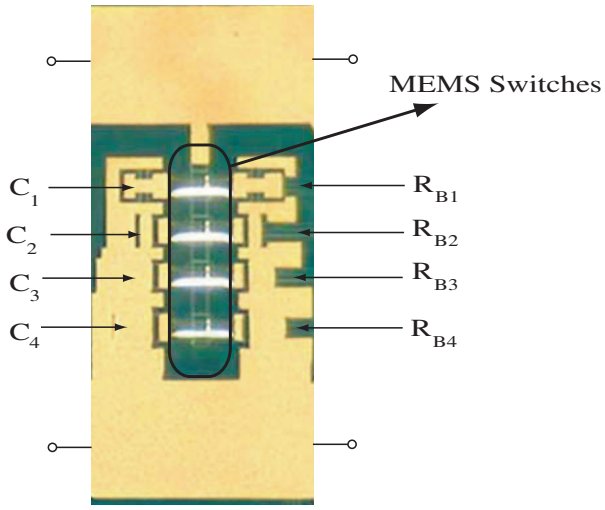
3.2.3 3 and 4-bit Digital MEMS Capacitors

The resonant capacitor C_R is substituted by a capacitor bank with four unit cells (Fig. 3.5). This results in 16 different filter responses using 16 different combination of switches in the up- and down-state positions. C_{Mi} (i=1,...,4), L_M and R_M represent MEMS switches, C_i (i=1,...,4) is half of the MAM capacitor in series with MEMS switch, and C_p is the parasitic capacitance coming from the layout implementation of C_R. Each matching capacitor (C_M) is composed of 3 unit cells, and provides enough capacitive variation to result in a well matched circuit over the whole tuning range.

Fig. 3.6 shows the different values of C_R and C_M for different combination of switches in



(a)



(b)

Figure 3.5: (a) Simplified circuit model, and (b) layout for C_R as a capacitor bank.

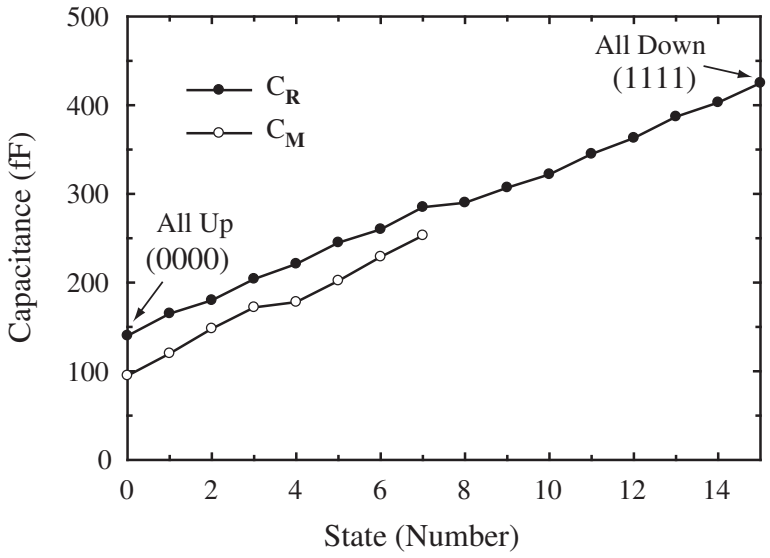


Figure 3.6: Simulated values of C_R and C_M for different switch combinations.

Table 3.2: C_R and C_M element values extracted from Sonnet simulation.

$C_{1(M)}$ (fF)	24	$C_{1(R)}$ (fF)	24
$C_{2(M)}$ (fF)	44	$C_{2(R)}$ (fF)	35
$C_{3(M)}$ (fF)	65	$C_{3(R)}$ (fF)	65
$C_{p(M)}$ (fF)	20	$C_{4(R)}$ (fF)	120
C_M^{up} (fF)	38	$C_{p(R)}$ (fF)	35
C_M^{down} (fF)	720	L_M (pH)	15
–	–	R_M (Ω)	$0.6 - 0.8$

the up- and down-states positions. These values are extracted from *full-wave* simulation of the capacitor bank layouts using Sonnet [56] and fitted to a RLC model. The corresponding unit cell values presented in Table 3.2 are calculated using $X = 1/\omega C$, where X is found from the *full-wave* simulations and includes all inductive (parasitic) effects. C_R varies between 140 fF (State 0, all the switches are up) and 425 fF (State 15, all the switches are down) which is close to the range in Table 3.1. C_M varies between 95 fF (State 0), and 253 fF (State 7), which is higher than $C_{M(Max)}$ in Table 3.1 and provides a safe margin to match the return loss of the filter at lower frequencies.

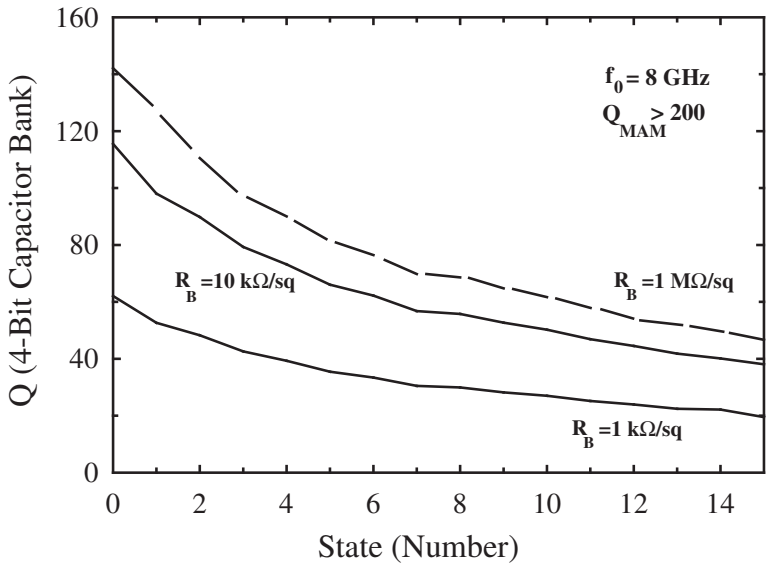


Figure 3.7: Simulated resonant capacitor quality factor for different switch combinations, and bias resistances.

3.2.4 Effect of Bias Resistance on Capacitor Q

The resonant capacitor bank (C_R) quality factor has an important role in determining the unloaded Q of the resonators and the insertion loss of the filter. The MEMS and MAM capacitors are high-Q elements (Q>200) as measured in [23], and do not degrade the unloaded Q of the resonators. However, the bias line resistor has a very strong loading effect on the quality factor of C_R (and the resonator). Fig. 3.7 shows the simulated quality factor of C_R at an arbitrary frequency (f_0= 8 GHz) for different bias line values. This is done using ADS, with the component values in Table 3.2 placed in the circuit model of Fig. 3.5. The simulated impedance is fitted to a simple RC circuit (L is negligible), and the quality factor is defined as [20]:

$$Q = \frac{1}{2\pi f RC} \tag{3.1}$$

where f is the operation frequency, R is the total series resistance including MEMS switches, MAM capacitors, and bias line resistances, and C is the equivalent capacitance. The C_R quality factor doubles if the bias line resistance changes from 1 $\mathrm{k}\Omega/\mathrm{sq}$ to 10 $\mathrm{k}\Omega/\mathrm{sq}$. For higher bias line resistances (up to 1 $\mathrm{M}\Omega/\mathrm{sq}$) the quality factor improvement is only 20%.

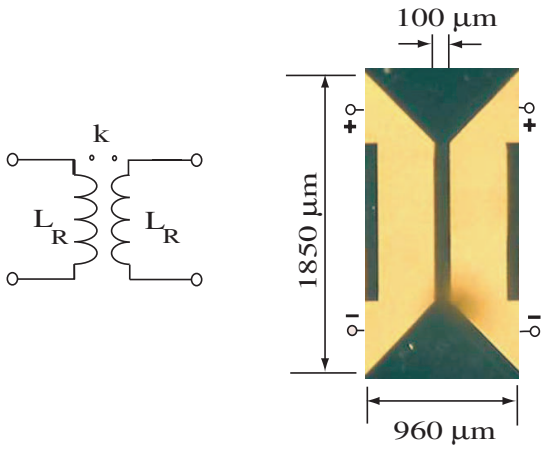
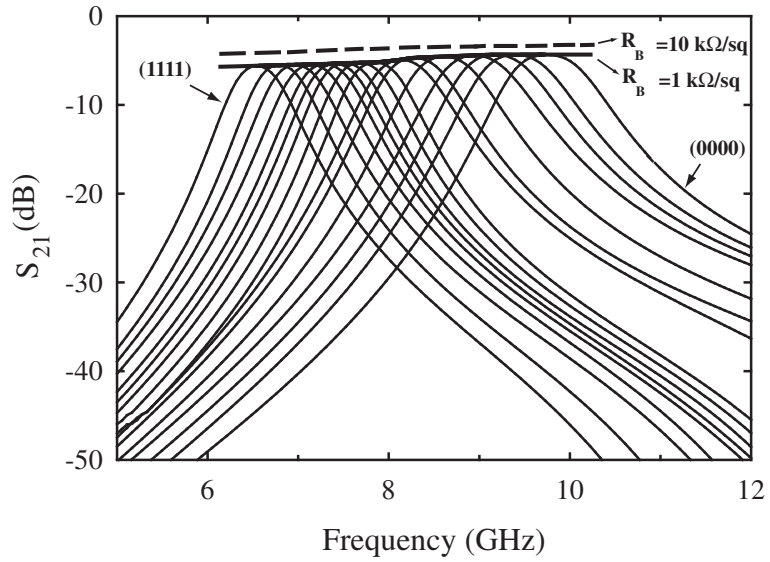


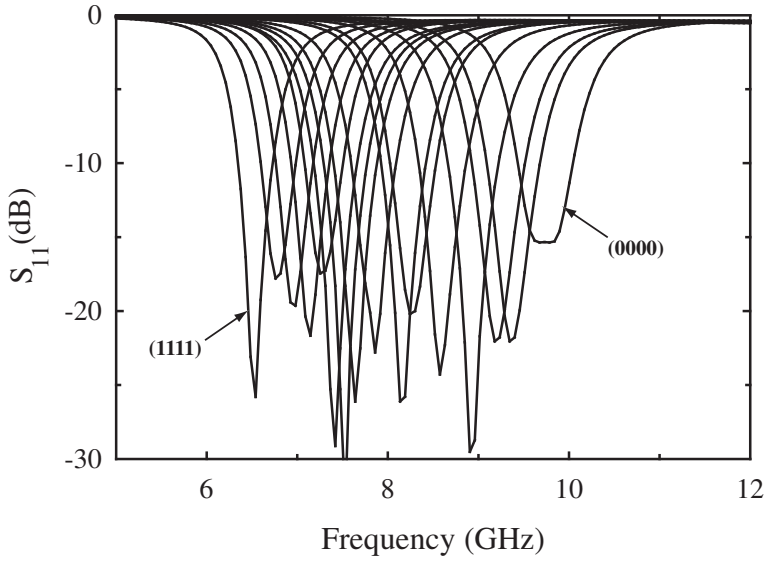
Figure 3.8: Final transformer layout for 6.5-10 GHz tunable filter.

3.2.5 Tunable Filter Simulations

The resonant capacitor (C_R) layout can change both the transformer coupling factor and the inductor values. The amount of desired coupling and inductance is adjusted by changing the length of the inductors and the distance between the two inductors when the coupled ($C_R L$) resonators are simulated together in Sonnet. Fig. 3.8 shows the finalized layout for the transformer after all full-wave optimizations. The simulated Q of the wide microstrip lines (W = 340 μm, L = 1600 μm) on the glass substrate is around 78 at 8 GHz. The whole filter response is then simulated in ADS by cascading S-parameters of the matching capacitors and resonators. The simulated center frequencies and the corresponding states of C_M and C_R are presented in Table 3.3. Fig. 3.9 shows the insertion loss for 16 different states with $\mathrm{R_{bias}}$ = 1 kΩ/sq, and is 4 and 5.6 dB at 9.8 and 6.5 GHz, respectively. The higher insertion loss at 6.5 GHz is due to the low-resistivity bias line which has a strong loading effect when the switches are all in the down-state position. If the value of $\mathrm{R_{bias}}$ increases to 10 kΩ/sq , the insertion loss improves to 3 dB at 9.8 GHz and 4 dB at 6.5 GHz. The effective unloaded Q of the two-pole filter is 50 and 70 for $\mathrm{R_{bias}}$ = 1 kΩ/sq and 10 kΩ/sq, respectively, at 8.1 GHz (state 6). Fig .3.10(a),(b) present the simulated insertion loss of the differential filter for states 0 and 15 from 1-30 GHz, respectively.



(a)



(b)

Figure 3.9: Simulated (a) I.L., and (b) R.L. of the tunable two-pole 6.5-10 GHz filter.

Table 3.3: Simulated center frequencies and the corresponding 16 different states for C_R and C_M. The indexes U/L refer to the upper (U) and lower (L) matching capacitors in Fig.3.4.

f_0 (GHz)	C_R	$C_M(U/L)$	f_0 (GHz)	C_R	$C_M(U/L)$
6.54	1111	111/111	7.86	0111	011/010
6.82	1110	111/110	8.14	0110	011/001
7.04	1101	110/110	8.30	0101	011/000
7.15	1100	110/101	8.63	0100	010/001
7.31	1011	110/011	8.96	0011	001/001
7.42	1010	101/011	9.18	0010	010/000
7.53	1001	011/011	9.40	0001	001/000
7.69	1000	100/011	9.73	0000	000/000

3.3 6-10 GHz Filter Fabrication and Measurement

3.3.1 Fabrication, Implementation and Biasing

The tunable filter is fabricated on a 500 μm glass substrate ($\epsilon_r = 4.6$ and $\tan\,\delta = 0.01$) using MEMS switches and microstrip lines, using a standard RF MEMS process developed at the University of Michigan [23][57][58][59]. The MEMS capacitive switch is based on a 8000 Å sputtered gold layer and is suspended 1.4-1.6 μm above the pull-down electrode. The dielectric Si_3N_4 layer is 1800 Å thick and the bottom electrode thickness is 6000 Å (underneath the bridge). The metal-air-metal capacitors are suspended 1.5 μm above the first metal layer. The microstrip conductor, the bridge anchor, and the top plate of MAM capacitors are electroplated to 2 μm thick using low stress gold solution. The bias lines are fabricated using a 1200 Å thick SiCr layer with a resistivity of 1 kΩ/sq. Fig. 3.11 shows the major steps for the MEMS digital varactor fabrication:

1) 6000 Å Ti/Au/Ti layer metal evaporation on the back side of the silicon wafer as the microstrip ground plane (Fig. 2.14 (a)).

2) Bias line (SiCr) sputtering to pattern the 1 kΩ/square resistive line (not shown in Fig. 3.11).

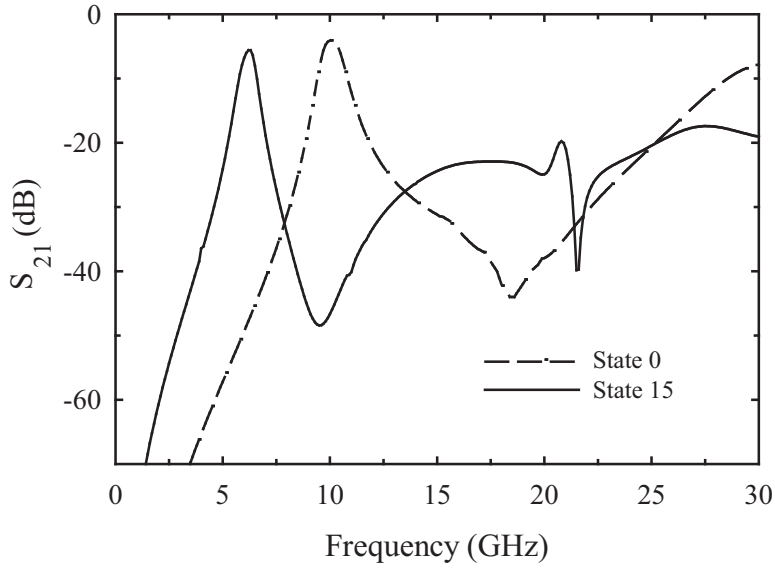


Figure 3.10: Simulated I.L. of the tunable differential filter for states 0 and 15 from 5-30 GHz.

3) 6000 Å first metal layer (Ti/Au/Ti) evaporation to pattern the microstrip lines and the bottom electrode of the MEMS switch (Fig. 3.11(a)).

4) 1800 Å dielectric layer (Si_3N_4) deposition to pattern the isolation layer between the top and bottom electrodes of a capacitive MEMS switch (Fig. 3.11(b)).

5) Sacrificial layer (PMMA) deposition to make the 1.4-1.6μm gap between the suspended membrane and the bottom electrode of the MEMS switch and the top and bottom electrodes of the metal-air-metal capacitors (Fig. 3.11(b)).

6) Sputtering 8000 Å Ti/Au layer on top of the sacrificial layer to fabricate the membrane of the MEMS switch (see Fig. 3.11(c)).

7) 2-3 μm Au Electroplating the microstrip conductor, the bridge anchor, and the top plate of MAM capacitors to reduce the ohmic loss and skin depth effect (Fig. 3.11(c)).

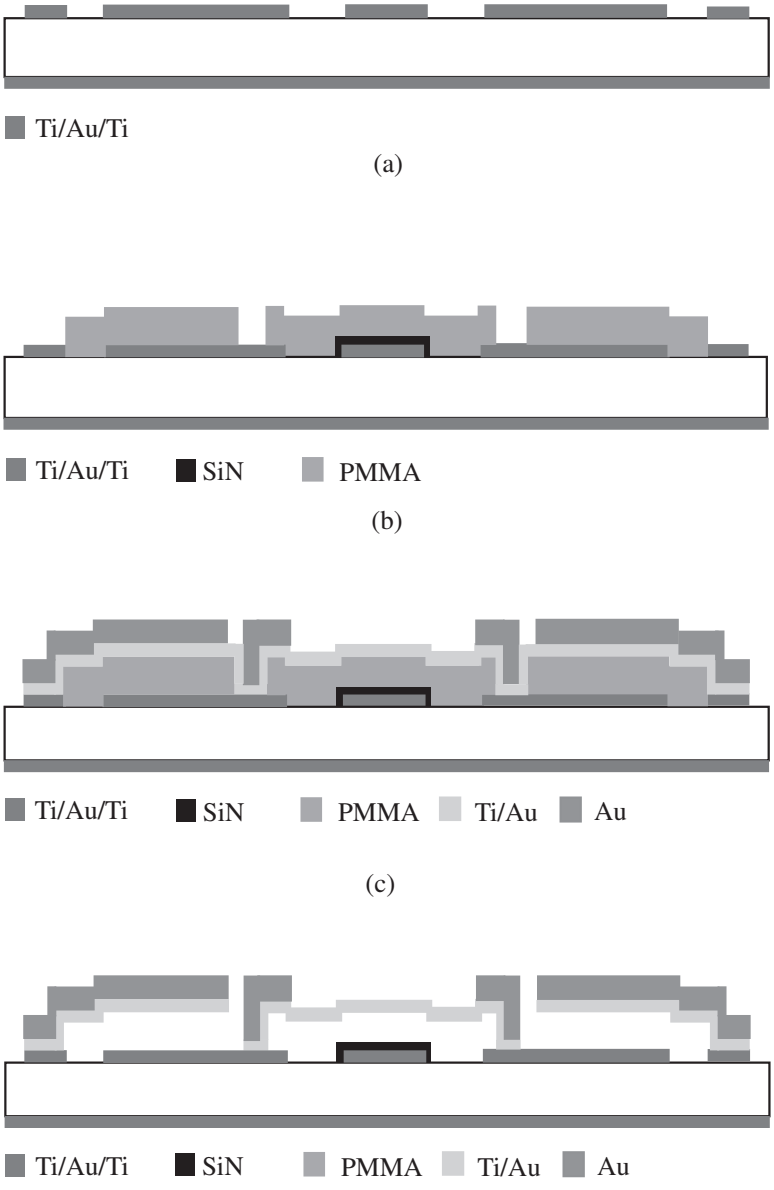


Figure 3.11: Fabrication steps of a digital MEMS varactor.

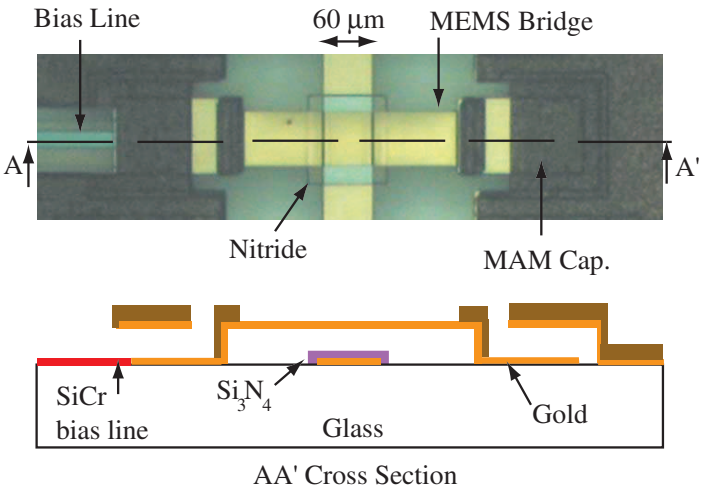


Figure 3.12: Photograph of a unit cell in a digital capacitor bank.

8) Releasing the switch and removing the sacrificial layer (Fig. 3.11(d)).

The center frequency of the tunable filter is directly related to the accuracy of the MAM capacitors (obtained vs. designed values). Since the MAM capacitors are quite large and fully electroplated and the sacrificial layer underneath them is uniform, one can build these capacitors quite uniformly throughout the entire wafer with an accuracy around $\pm 5\%$ in university labs. This can be clearly seen in the agreement between measured vs. simulated center frequencies (Fig. 3.16(a)).

The photograph of a unit cell in a digital capacitor bank is shown in Fig. 3.12. The width, length, and thickness of the bridge are 70 μm, 280 μm, and 0.8 μm, respectively, the bottom electrode width is 60 μm and the gap is 1.5 μm for the bridge and MAM capacitors. The bottom plate of one of the MAM capacitors is connected to the thin-film resistor to bias the bridge. The release height of the MEMS bridge and MAM capacitor is 1.5 μm measured by a light-interferometer microscope. The measured pull-in voltage is V_p = 26 V, with a corresponding spring constant of k =25 N/m [20]:

$$V_p = \sqrt{\frac{8kg_0^3}{27\epsilon wW}} \tag{3.2}$$

where g_0 is the bridge height in the up-state, W is the bottom electrode width, and w is the width of the bridge ($V_p = 26$ V, $g_0 = 1.5$ μm, $A = wW = 70$ μm $\times$ 60 μm). The residual stress of the MEMS switch is $\sigma = 42$ MPa and is calculated from [20]:

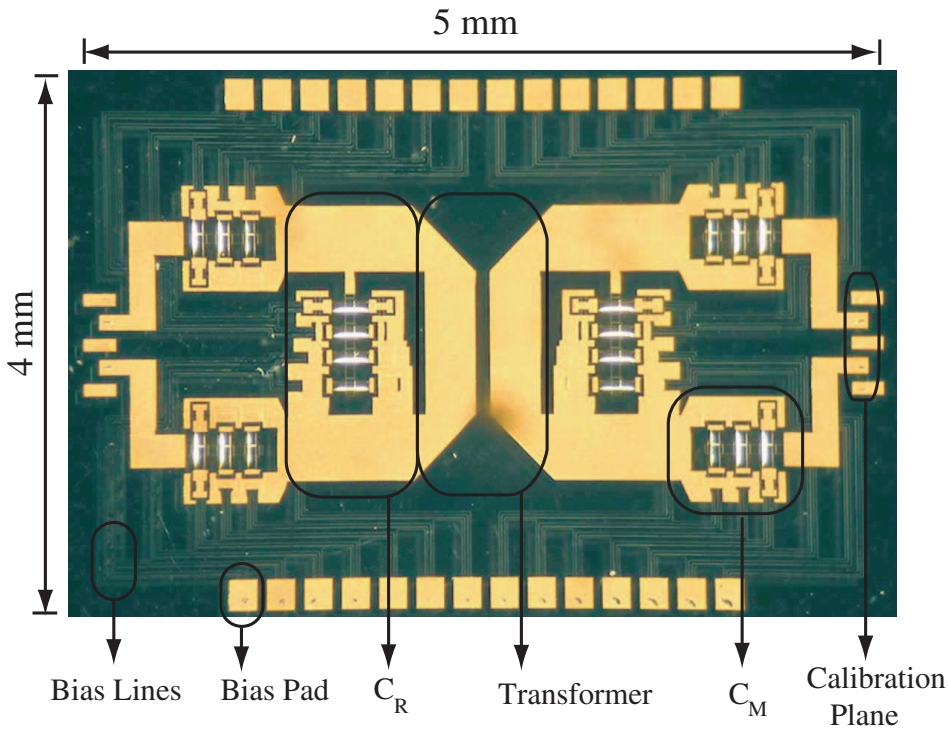


Figure 3.13: Photograph of the complete 6.5-10 GHz 2-pole tunable filter on a glass substrate.

$$k = k' + k'' = 32Ew(\frac{t}{l})^3(\frac{27}{49}) + 8\sigma w(1-\nu)(\frac{t}{l})(\frac{3}{5}) \tag{3.3}$$

where E = 80 GPa and ν = 0.44 are the Young modulus and Poisson ratio for Au, w, t, and l are the width, thickness, and length of the bridge, k' is part of the bridge spring constant related to the stiffness and material characteristics (Young modulus, Moment of inertial) and k'' is part of the bridge spring constant related to biaxial residual stress (σ) and is a result of fabrication process. Normally, for $\sigma > 10$ MPa, k'' is a dominant factor. In this case, $k' = 2.3$ N/m and $k'' = 22.7$ N/m. The mechanical resonant frequency and quality factor of the switch are $f_0 = 72$ kHz and $Q_m = 1$, respectively [20]:

$$f_0 = (\frac{1}{2\pi}).\sqrt{\frac{k}{m_e}} \tag{3.4}$$

$$m_e = 0.4(lwt)\rho \tag{3.5}$$

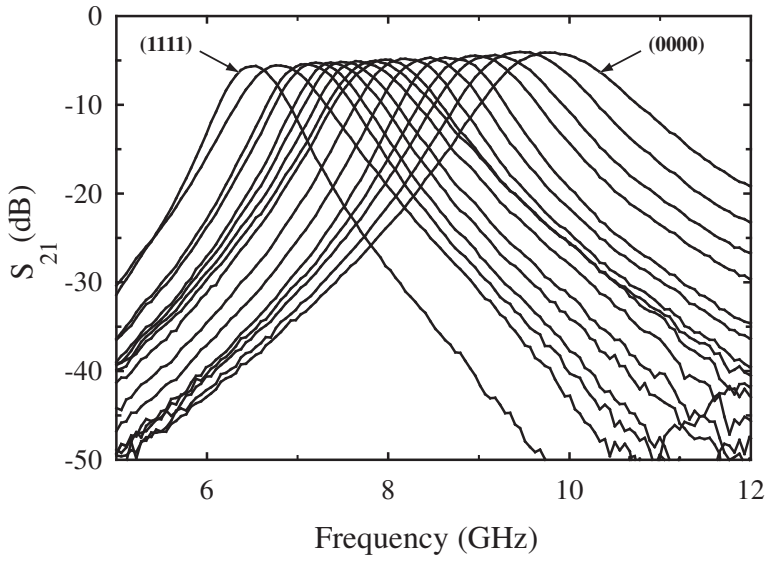
$$Q_m = \frac{k}{2\pi f_0 b} \tag{3.6}$$

where m_e is the effective mass of the bridge, b is the damping factor, and ρ = 19.32 kg/m^3 is the density of the gold. The photograph of the complete 6.5-10 GHz filter is shown in Fig. 3.13. It is composed of a transformer in the middle, two resonant capacitors (C_R), each with 4 unit cells, and four matching capacitors (C_M) each with 3 unit cells. Each switch has a separate SiCr, DC bias line for independent control. The center conductor of each capacitor bank is connected to the DC ground pad through the SiCr line. The filter is excited using differential input and output lines, which are compatible with a GSGSG differential probe with a pitch of $150\,\mu\mathrm{m}$.

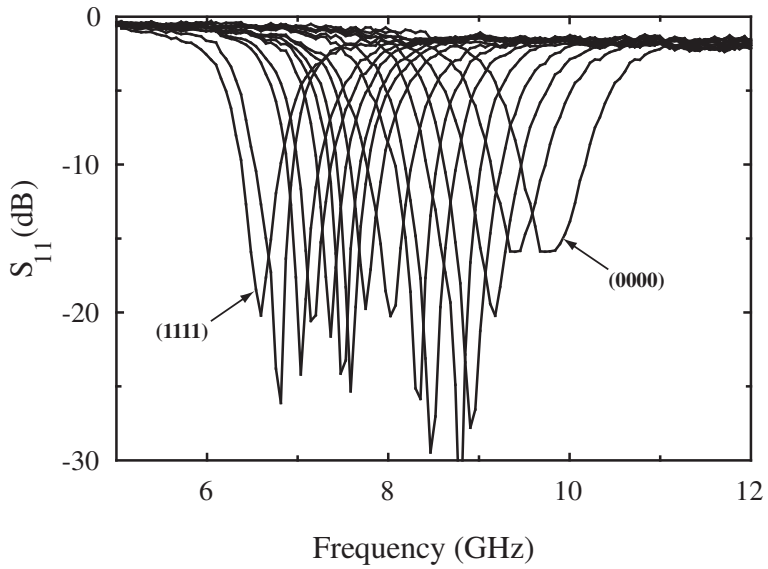
3.3.2 Measurements

The tunable filter is measured using a differential test set-up: Two 0-180° hybrid couplers and two differential probes are used to provide differential excitation for the filters. As is well known, only the odd mode should be generated for differential circuits. The phase and amplitude imbalance for the couplers should be as small as possible (Gain Bal. $\leq$ 2 dB, Phase Bal. $\leq 10^\circ$) for accurate differential measurements [60].

The measurement results are shown in Fig. 3.14 for 16 different states. The insertion loss (Fig. 3.14(a)) is 4.1 dB and 5.6 dB at 9.8 GHz and 6.5 GHz respectively, and the relative bandwidth is approximately fixed for the whole tuning range as expected from the simulation results. The return loss (Fig. 3.14(b)) is always better than 16 dB for the whole tuning range. Fig. 3.15 compares the measured and simulated insertion loss for two arbitrary states at 8.6 GHz (State 4) and 7.1 GHz (State 13). The simulated and measured responses agree very well. For the case of ($\mathrm{R_{bias}}$ = 10 $\mathrm{k\Omega/sq}$), the simulated insertion loss is 1 dB better at 8.6 GHz and 1.4 dB better at 7.1 GHz as compared with the measurements for $\mathrm{R_{bias}}$ = 1 $\mathrm{k\Omega/sq}$. The measured response of a fabricated filter without any bias lines also confirms that the insertion loss improves by 1 dB at 9.8 GHz (all the switches are electroplated in the up-state position) to 1.6 dB at 6.5 GHz (all the switches are electroplated in the down-state position). The simulated and measured center frequency and loss for each of the 16 different states is presented in Fig. 3.16(a). Fig. 3.16(b) shows the relative bandwidth variation for all responses, and is 5.5% at 9.8 GHz (State 0), and 4.7% at 6.5 GHz (State 15).



(a)



(b)

Figure 3.14: Measured (a) I.L., and (b) R.L. of the tunable two-pole 6.5-10 GHz filter.

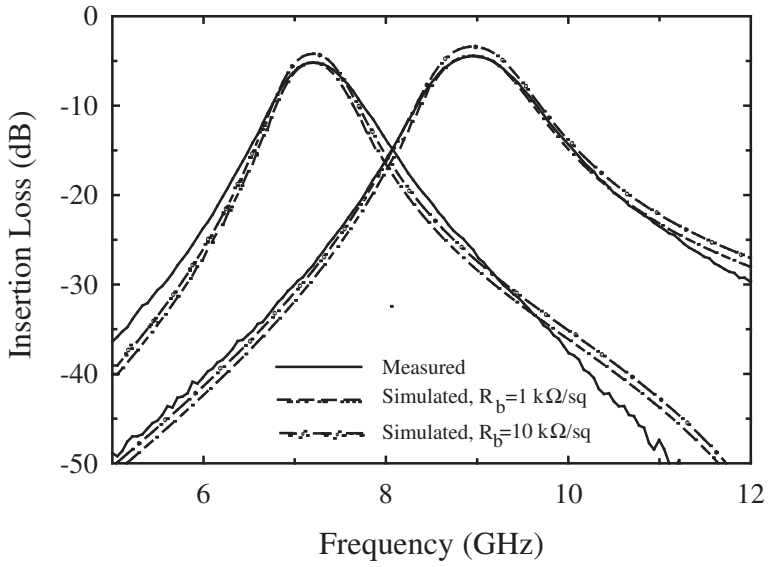


Figure 3.15: Comparison between the measured and simulated insertion loss for two arbitrary states at 7.1 (State 13) and 8.6 GHz (State 4).

3.4 6-10 GHz Filter Nonlinear Characterization

The nonlinear analysis of MEMS switches, varactors and tunable filters has been presented in [21]. This analysis shows that the mechanical force acting on the MEMS bridge is proportional to V_{RF}^2 across the bridge:

$$F_e = F_m = \frac{C_{MEMS}.V_{RF}^2(t)}{2g} = k\Delta x(t) \tag{3.7}$$

$$\Delta x(t) = \frac{C_{MEMS}.V_{RF}^2(t)}{2kg} \tag{3.8}$$

where g is dependent to the bias voltage. For a shunt capacitive switch (Fig. 3.17), small displacement in the bridge height results in a phase modulation at the output voltage [20][21]:

$$\phi_{out}(t) = \phi_0\big[1 - \frac{\Delta x(t)}{g}\big] \tag{3.9}$$

$$\phi_0 = -\frac{2\pi f C_{MEMS} Z_0}{2} \quad for \;\; 2\pi f C_{MEMS} Z_0 \ll 1 \tag{3.10}$$

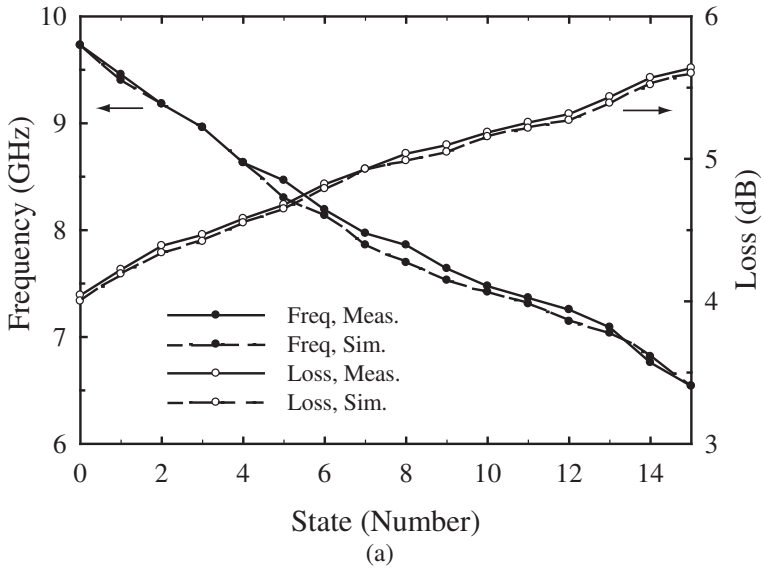


Figure 3.16: (a) Simulated and measured center frequency and loss, and (b) measured relative bandwidth of the 16 filter responses (5.1±0.4%).

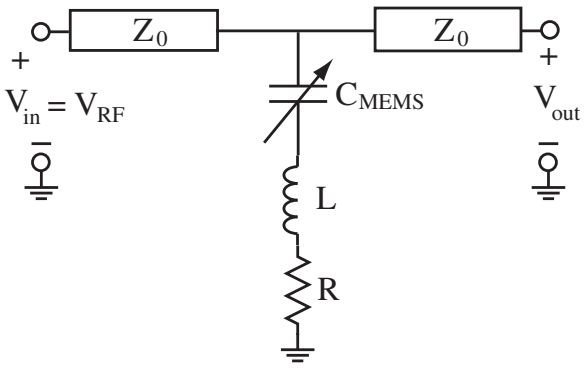


Figure 3.17: A MEMS switched capacitor electrical model.

Under high RF drive conditions, the MEMS bridge capacitance (C_{MEMS}) variation results in a nonlinear behavior of the MEMS switch and the tunable filter consisting MEMS capacitors. This behavior is directly related to dynamic response of the bridge. In the case of a two-tone excitation, (f_1, f_2), the mechanical force at the beat frequency Δf ($f_1 - f_2$) changes the capacitance of the bridge, and the presence of the input tones across the variable capacitor generates the third order intermodulation [20][21]:

$$V_{in}(t) = V_1 sin(2\pi f_1 t) + V_2 sin(2\pi f_2 t) \tag{3.11}$$

$$\begin{aligned} V_{out}(t) \simeq V_1 sin(2\pi f_1 t + \phi_0) + V_2 sin(2\pi f_2 t + \phi_0) - \big(\frac{V_1 V_2 \phi_0 C_{MEMS}}{4kg^2}\big) \\ \times \big[V_1 cos(2\pi(2f_1 - f_2)t + \phi_0) + V_2 cos(2\pi(2f_2 - f_1)t + \phi_0)\big] \end{aligned} \tag{3.12}$$

The IM_3 product level and IIP_3 at $2f_2 - f_1$ and $2f_1 - f_2$ for a MEMS switch are (V_1 = V_2 = V):

$$P_{IM_3} = \frac{P_{sideband}}{P_{signal}} = \big(\frac{V_1 V_2 \phi_0 C_{MEMS}}{4kg^2}\big)^2 \tag{3.13}$$

$$P_{sideband} = P_{signal} \rightarrow \mathrm{IIP}_3 = \frac{V^2}{2Z_0} = \frac{2kg^2}{\phi_0 C_{MEMS} Z_0} \tag{3.14}$$

Fig. 3.18 shows the simulated IM_3 of the shunt capacitive switch used in the differential filter structure versus difference frequency for three different input powers (V_p = 26 V, k = 25 N/m, g_0 = 1.5 μm, σ = 22 MPa, $A = wW$ = 70 μm × 60 μm, f_0 = 72 kHz, C_{up} = 38 fF). The IM_3 level is fixed for bit frequencies below the mechanical resonant frequency of the bridge. Above the mechanical resonant frequency, the IM_3 drops and follows the low-pass mechanical response of the bridge. This phenomenon improves the linear behavior of RF MEMS switch for difference frequencies above the mechanical resonant frequency of the bridge.

Due to the complexity of the filter topology, the preferred method for nonlinear characterization of the filter is to perform some nonlinear measurements and determine the filter IM_3 and IIP_3, and the mechanical response of the MEMS varactors. Fig. 3.19 shows the setup to measure the intermodulation components at the output of the tunable filter. Two tones generated by two synthesizers are combined, and the combined signal is delivered to the MEMS filter differentially through the

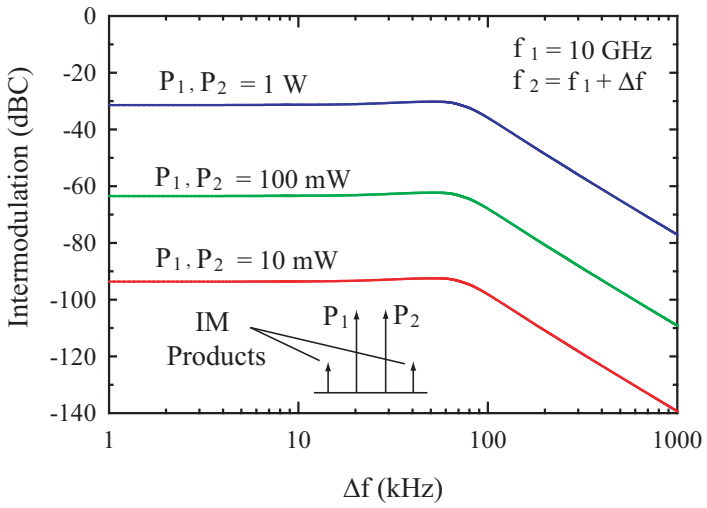


Figure 3.18: Simulated IM_3 level of shunt capacitive switch output power for three different input power levels.

baluns (3 dB couplers) and differential RF probes. The output signals are measured using a spectrum analyzer. Fig. 3.20 shows the output spectrum of the filter when all the switches are in the up-state and the bit frequency is 60 kHz. The IM_3 signal is generated due to the nonlinear behavior of the MEMS switches in the filter.

Fig. 3.21(a) shows the measured output power for the fundamental and the intermodulation components for several values of Δf ($f_1 - f_2$). The measured IIP_3 is $>$ 45 dBm for $\Delta f >$ 500 KHz. The measurement is in the up-state position, (0000), since this state gives the worse IM_3 products. Tunable filters with diode varactors have much lower values of IIP_3 (12 dBm in [13] and 28 dBm in

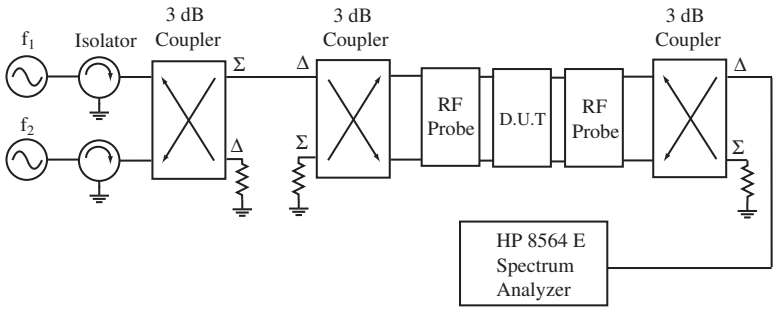


Figure 3.19: Experimental setup for intermodulation measurements ($\Delta f = f_2 - f_1$).

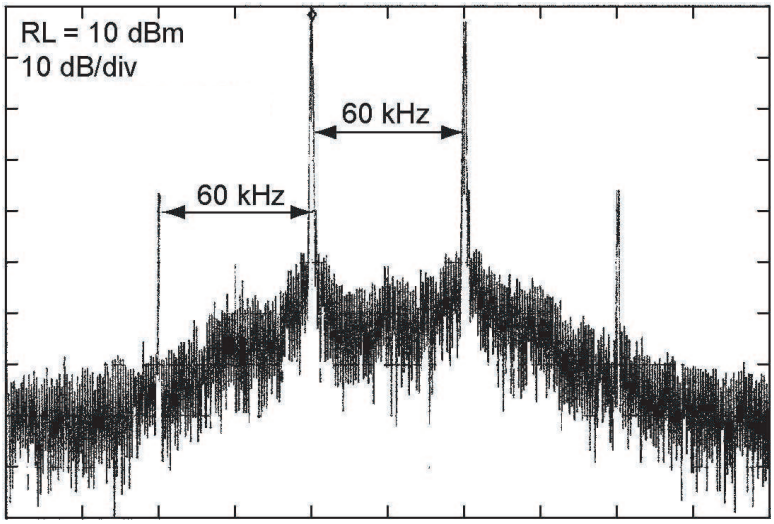
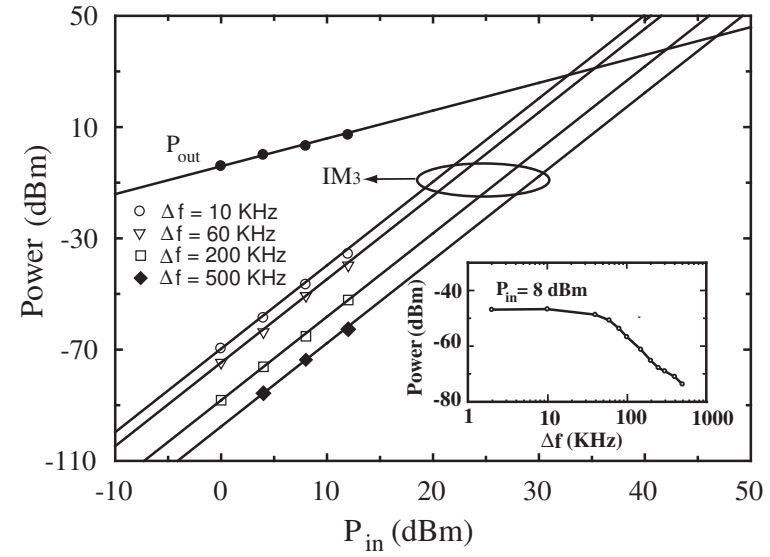


Figure 3.20: The filter output signal spectrum at 10 GHz (Δf= 10 kHz).

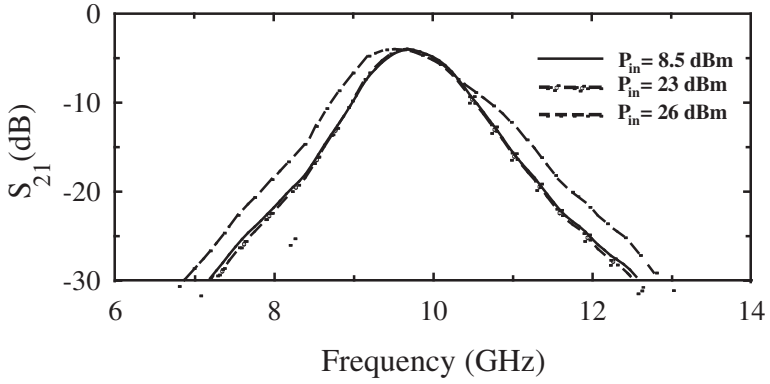
[14]). Fig. 3.21(a) also shows the intermodulation component vs. the difference frequency between input tones (Δf) for $\mathrm{P_{in}}$= 8 dBm (no bias voltage on the bridges). The intermodulation component follows the mechanical response of the bridge, and the $\mathrm{IM_3}$ level drops by 40 dB/decade for $\Delta f > f_0$ which is in agreement with theory [21].

Fig. 3.21(b) shows the measured insertion loss of the filter for three different input power levels ($\mathrm{P_{in}}$ = 8.5, 23, and 26 dBm). Due to the spectrum analyzer (a non-calibrated system), the measured insertion loss value is not the same as Fig. 3.14. The center frequency is at 9.8 GHz and the bias voltage is zero (State 0; (0000)). For $\mathrm{P_{in}} <$ 24 dBm, there is no self actuation effect [20][21], and the filter response does not change with increasing the level of $\mathrm{P_{in}}$. For $\mathrm{P_{in}} >$ 24 dBm, the level of the RF voltage across the MEMS bridges is large enough to self-bias the bridges. As a result, the shape of the filter gets distorted. This filter can therefore handle an input power up to 24 dBm (250 mW). If a higher bias MEMS switch is used ($V_p = 52\ V$), the RF power handling will increase to 1 W before self-biasing becomes an issue.

The maximum power handling of the filter can be well predicted by studying the voltage and current across the MEMS switch for an input power of 200 mW (Fig. 3.22). Using a linear model in Agilent ADS, the rms voltage is calculated to be 12.5 V across $C_{R(4)}$ which is the switch with the largest loading MAM capacitor (State 0; (0000)). The corresponding height change in the MEMS switch is 0.055 μm, and results in 0.97 fF change in the switch and 0.7 fF change in the overall bit-4

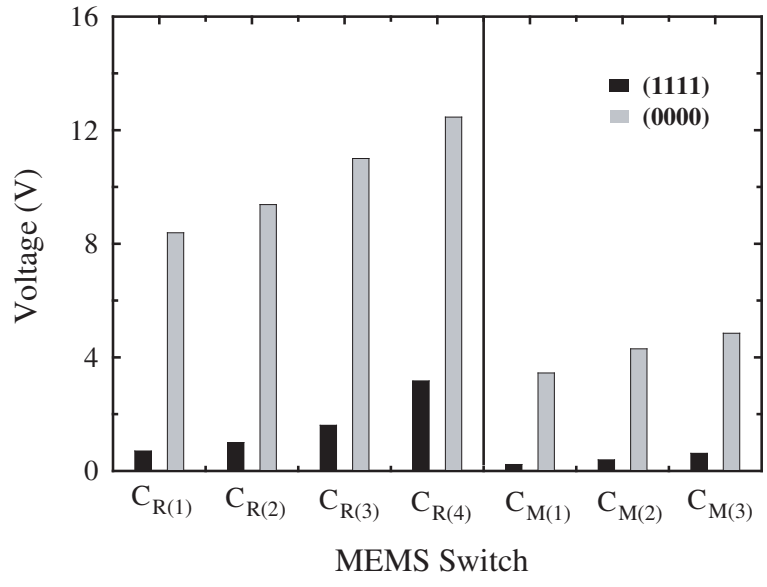


(a)

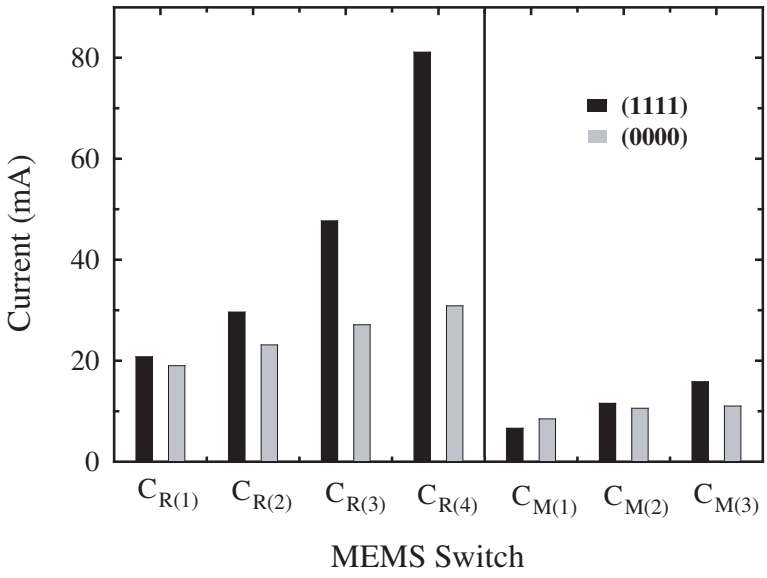


(b)

Figure 3.21: Nonlinear measurements at V_b = 0 V (a) The fundamental and intermodulation components vs. the input power, and the two-tone IM_3 vs. the beat frequency at $f = 9.8$ GHz, (b) filter insertion loss for different values of input power.



(a)



(b)

Figure 3.22: Simulated rms V and I for the input capacitor banks (C_R, C_M). The values for the output capacitive banks are lower by a factor of 2 due to the filter loss.

capacitance. This is small enough that it has no effect on the frequency response (Fig. 3.21(b)). In the down-state position, the rms current in $C_{R(4)}$ is 81 mA for P_{in}= 200 mW, and is well within the acceptable region [20]. However, the rms voltage across the $C_{R(4)}$ is 3.5 V, which is just below the hold-down voltage of $\sim$5 V (the switch remains down even if the DC actuation voltage is removed). It is for these reasons that we predict a $\sim$250 mW power handling capacity for hot-switching (RF is never shut off).

3.5 Improvements in the 6.5-10 GHz filter

The insertion loss and the quality factor of the 6.5-10 GHz tunable filter can be improved in different ways. As mentioned before, increasing the bias line resistance from 1 kΩ/sq to 10 or 20 kΩ/sq improves the filter loss and unloaded quality factor because of lowering the loading effect of the bias line on the switched capacitor bank. Also, the use of quartz substrates which have much lower dielectric loss compared to glass substrate (tan δ (quartz) = 0.001, tan δ (glass) = 0.01) will reduces the loss of the filter. As an example, the 2-pole filter with the center frequency of f_0 = 8.1 GHz (State 6) on glass substrate with 1 kΩ/sq bias line resistance is re-simulated on a quartz substrate with 20 kΩ/sq bias line resistance. Fig. 3.23 compares the simulated insertion loss for two filters. The insertion loss of the filter is improved from 4.8 dB to 2.6 dB. It is seen that 1.6 dB of this improvement is due to increasing the bias line resistance and the other 0.6 dB is due to the lower dielectric loss of the quartz substrate. The quality factor of the filter improves from 50 to 77 by changing the bias line resistance and to 95 by using the quartz substrate.

Employing another type of RF MEMS switch with higher quality factor such as a cantilever capacitive switch with a thick electroplated beam can also improve the filter loss and quality factor. Due to lowering the skin effect of the switch cantilever, the loss of the switch and filter will considerably improve.

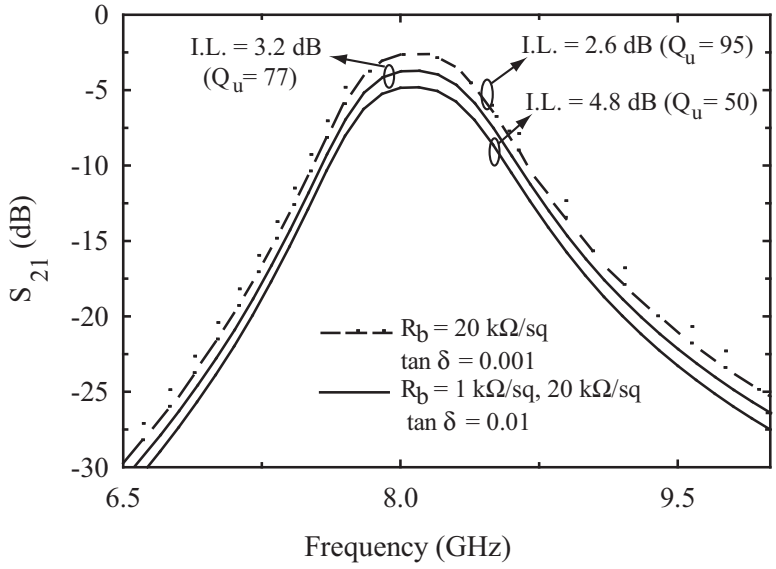


Figure 3.23: The simulated 8.1 GHz filter on glass and quartz substrates with 1 and 20 kΩ/sq bias line resistance respectively.

3.6 10-16 GHz Filter Design and Simulation

3.6.1 Filter Design

The differential lumped filter topology shows excellent performance for the 6.5-10 GHz frequency range. It is important to know the maximum frequency of operation for this layout and the practical limitations for filter implementation at higher frequencies. Theoretically, it is possible to design the tunable filter in Fig. 3.4 with a desirable frequency response and tuning range by just tuning C_R and C_M capacitors, but the physical implementation of the filter elements is not possible for every frequency range. The major practical limitations for filter layout implementation at higher frequencies are:

1) Transformer implementation: As the center frequency goes higher, the inductor values get smaller. As a result, the inductors are shorter, and to achieve the desirable transformer coupling, the inductors should be placed closer to each other. For frequencies above 18 GHz, even by fabricating the inductors as close as possible, the desired coupling cannot be achieved.

2) MEMS switch implementation: As frequency of operation goes higher, the capacitance of each unit cell or the switch up-sate capacitance is getting smaller. This can be achieved by making the capacitor effective area ($A = wW$, w: bridge width, W: electrode width) smaller or the bridge

Table 3.4: Element values for the tunable lumped filter.

f_0 (GHz)	$10-16$	$C_{R(Max)}$ (pF)	0.27
Z_0 (Ω)	100	$C_{R(Min)}$ (pF)	0.09
k	0.072	$C_{M(Max)}$ (pF)	0.12
L_R (nH)	0.82	$C_{M(Min)}$ (pF)	0.06
$\frac{C_{M(Max)}}{C_{M(Min)}}$	2.0	$\frac{C_{R(Max)}}{C_{R(Min)}}$	3.0

Table 3.5: C_R and C_M element values extracted from Sonnet simulation.

$C_{1(M)}$ (fF)	15	$C_{1(R)}$ (fF)	18
$C_{2(M)}$ (fF)	24	$C_{2(R)}$ (fF)	30
$C_{3(M)}$ (fF)	30	$C_{3(R)}$ (fF)	40
$C_{p(M)}$ (fF)	10	$C_{4(R)}$ (fF)	62
C_M^{up} (fF)	25	$C_{p(R)}$ (fF)	20
C_M^{down} (fF)	300	L_M (pH)	20
$-$	$-$	R_M (Ω)	$0.6-0.8$

height (g_0) higher. Decreasing bottom electrode width or increasing the bridge height results in a higher pull-down voltage which is not desirable. Reducing the bridge width does not change the pull-down voltage, but decreases the spring constant of the bridge (k) [20]. One conservative design which results in reasonable amount of pull-down voltage and spring constant and provides the minimum up-state capacitance based on mechanical considerations assumes w = W = 40 μm and g_0 = 1.5 μm. At frequencies above 18 GHz, the finite size of the MEMS bridge also results in a parasitic inductance which limits the tuning performance of the 3 or 4-bit capacitors.

Considering all the above limitations, a differential filter is designed for 10-16 GHz applications. Table 3.4 presents the element values of a 2-pole, 5% (Chebyshev, equi-ripple bandwidth), 10-16 GHz differential tunable filter. Like the 6.5-10 GHz filter, this filter is first designed at 16 GHz using the design equations for a two-pole differential filter in chapter 2, with $A = 1.4$ and $Z_0 = 100\ \Omega$. Next, C_R and C_M capacitors are varied to achieve a filter response down to 10 GHz using Agilent-ADS [38]. To achieve a 45% tuning range or more, $C_{R(Max)}/C_{R(Min)}$ = 3.0 and $C_{M(Max)}/C_{M(Min)}$ = 2.0.

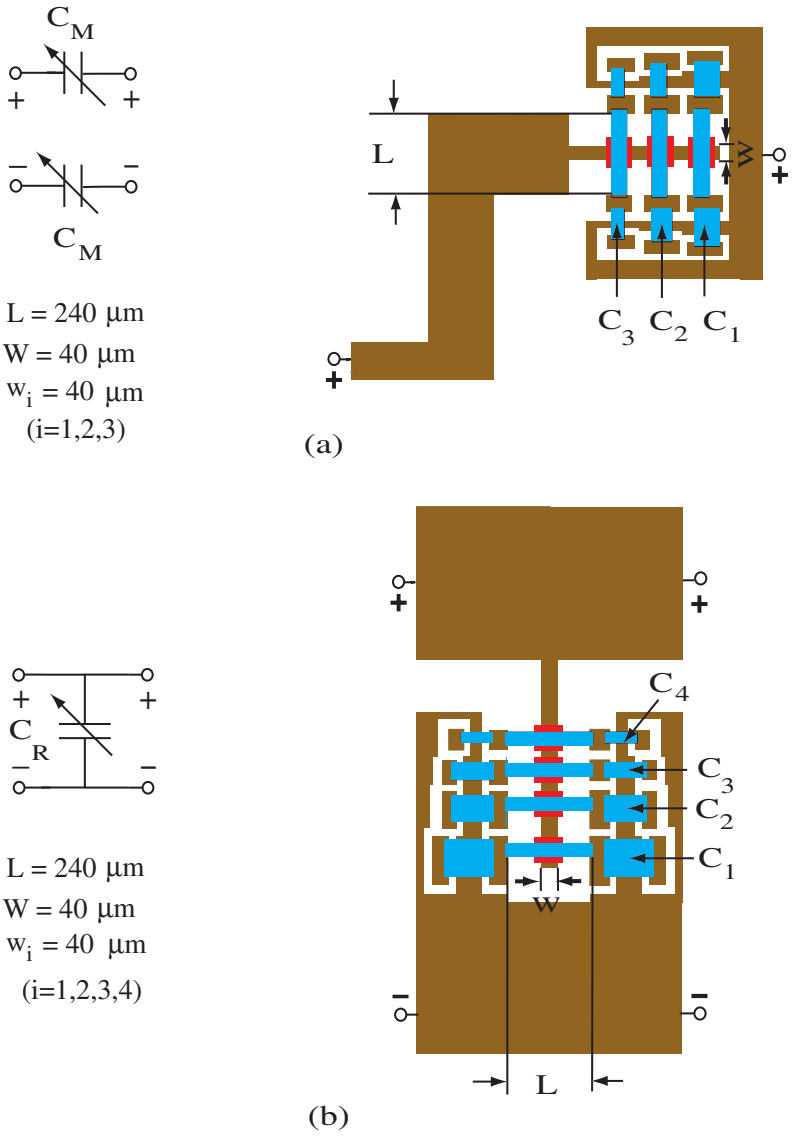


Figure 3.24: Layouts for C_R and C_M as capacitor banks.

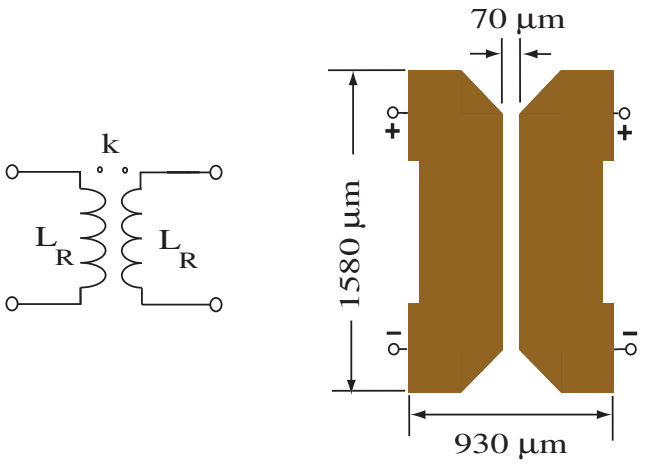


Figure 3.25: Final transformer layout for the 10-16 GHz tunable filter.

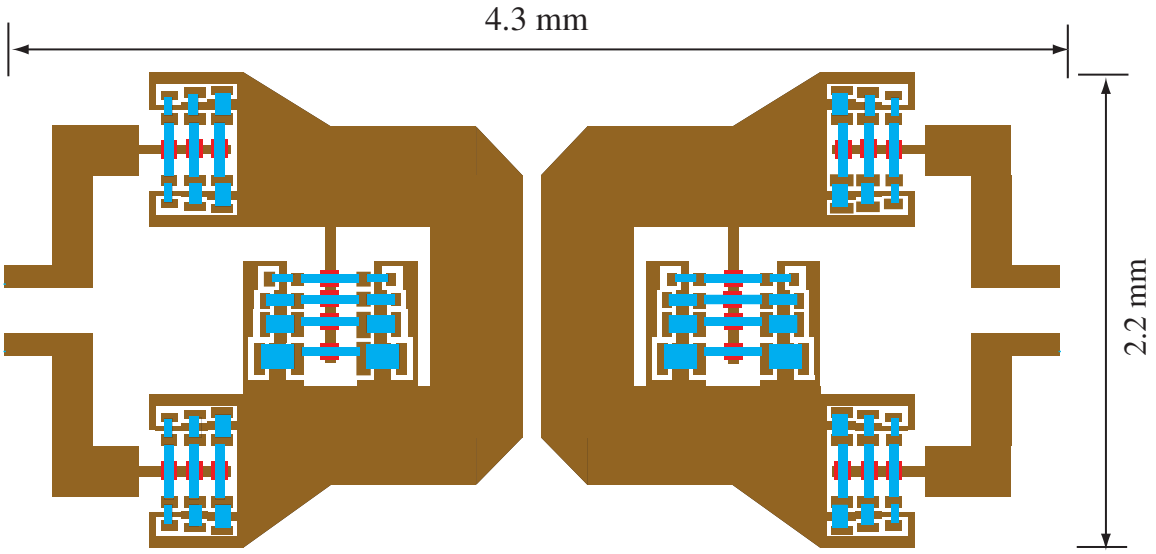


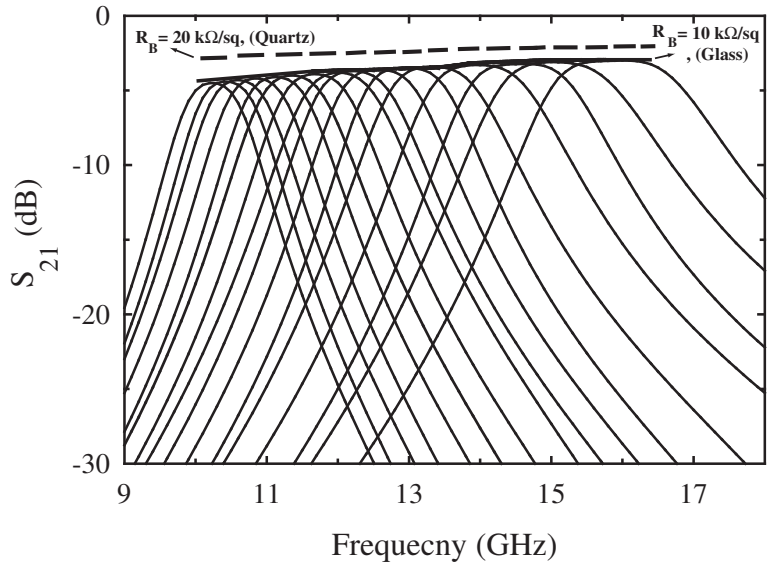
Figure 3.26: Complete layout of the 2-pole 10-16 GHz tunable filter.

3.6.2 Layout Implementation and Full-Wave Simulation Results

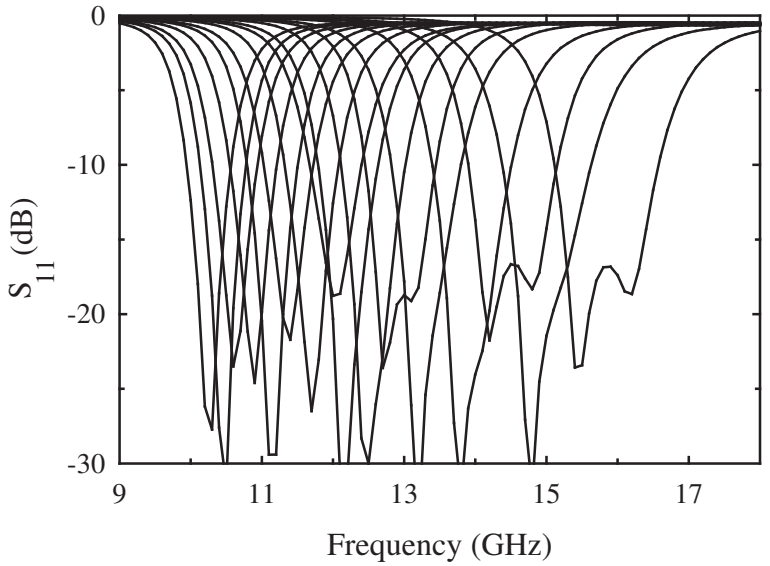
The procedure of layout implementation for this filter is exactly the same as the 6.5-10 GHz filter. The capacitors C_R and C_M are substituted by capacitor banks with four and three unit cells (Fig. 3.24) to provide 16 different filter responses from 10-16 GHz. These capacitor banks are all simulated using Sonnet [56] to provide the maximum and minimum values of C_R and C_M in Table 3.4. Table 3.5 presents the corresponding unit cell element values extracted from Sonnet. Due to the effect of C_R layout on transformer coupling factor and the inductor values the coupled (C_RL) resonators are simulated together in Sonnet. Fig. 3.25 shows the finalized layout for the transformer after all full-wave optimizations. The width of the transformer is wider and the gap between two inductors is smaller as compared to the 6.5-10 GHz transformer. Fig. 3.26 shows the complete layout of the filter. The whole filter response is then simulated in ADS by cascading S-parameters of the matching capacitors and resonators. Fig. 3.27 shows the simulated insertion loss and return loss for 16 different states. The filter is simulated on glass substrate and with a bias resistance of 10 $\mathrm{k}\Omega/\mathrm{sq}$. The insertion loss is 3 and 4.5 dB at 16 and 10 GHz, respectively, and the return loss is better than 16 dB over the whole band. The relative bandwidth is 5.4$\pm$0.4$\%$. By changing the substrate to quartz and the bias line resistance to 20 $\mathrm{k}\Omega/\mathrm{sq}$ the insertion loss improves to 2 dB and 3.2 dB at 10 and 16 GHz, respectively. The fabrication and measurement steps would be the same as the 6.5-10 GHz filter.

3.7 Conclusion

This chapter presents a state-of-the-art RF MEMS wide-band miniature tunable filter designed for 6.5-10 GHz frequency range. The differential filter, fabricated on a glass substrate using digital capacitor banks and microstrip lines, results in a tuning range of 44$\%$ with very fine resolution, and return loss better than 16 dB for the whole tuning range. A novel lumped differential topology is used to miniaturize the filter structure. Resonant capacitor banks with four unit cells (MEMS capacitive switches in series with high-Q MAM capacitors) result in 16 different filter responses next to each other with very fine tuning resolution like a continuous tunable filter. Matching capacitor banks with three unit cells result in a return loss better than 16 dB over the whole band. The measured results are very close to full-wave simulations. The relative bandwidth of the filter is



(a)



(b)

Figure 3.27: Simulated (a) I.L., and (b) R.L. of the tunable two-pole 10-16 GHz filter.

5.1$\pm$0.4$\%$ over the tuning range and the size of the filter is 5 mm $\times$ 4 mm. The insertion loss is 4.1 and 5.6 dB at 9.8 and 6.5 GHz, respectively, for a 1 $\mathrm{k}\Omega/\mathrm{sq}$ fabricated bias line. The simulations show that for a bias line with 10 $\mathrm{k}\Omega/\mathrm{sq}$ resistance or more, the insertion loss improves to 3 dB at 9.8 GHz and 4 dB at 6.5 GHz. The measured IIP_3 level is $>$45 dBm for $\Delta f >$ 500 KHz, and the filter can handle 250 mW of RF power for hot and cold switching. The full-wave simulations for a 10-16 GHz tunable filter show that the lumped capacitor design can be extended up to $\sim$18 GHz on glass substrates with excellent performance.

CHAPTER 4

12-18 GHz RF MEMS Tunable Filter

4.1 Introduction

In chapter 3, we presented 6-10 and 10-16 GHz tunable filters based on a lumped-element design. In this chapter we develop a 12-18 GHz filter based on a distributed design. Distributed filters are easier to implement and realize at higher microwave and millimeter-wave frequencies compared to lumped element filters and they can be easily miniaturized. On the other hand, distributed filters generate higher pass-bands and the second pass-band can drastically reduces the upper rejection band , so specific techniques are used to achieve a broad spurious-free stopband [8]. Lumped element filters do not have higher pass-bands. To design the distributed wide-band tunable filter coplanar waveguide (CPW) resonators are employed, because the RF MEMS switches developed on CPW structures are more broadband compared to their microstrip counterparts and have better frequency response [20]. On the other hand CPW resonators have higher insertion loss compared to microstrip resonators [65]. The RF MEMS tunable filter in this chapter has 40% tuning range from 12.2 to 17.8 GHz. The frequency band is covered by 16 filter responses (states) with very fine frequency resolution so as to behave as a continuous-type filter. To achieve this high tuning resolution, a novel 4-bit MEMS distributed capacitor bank is used to load CPW distributed resonator.

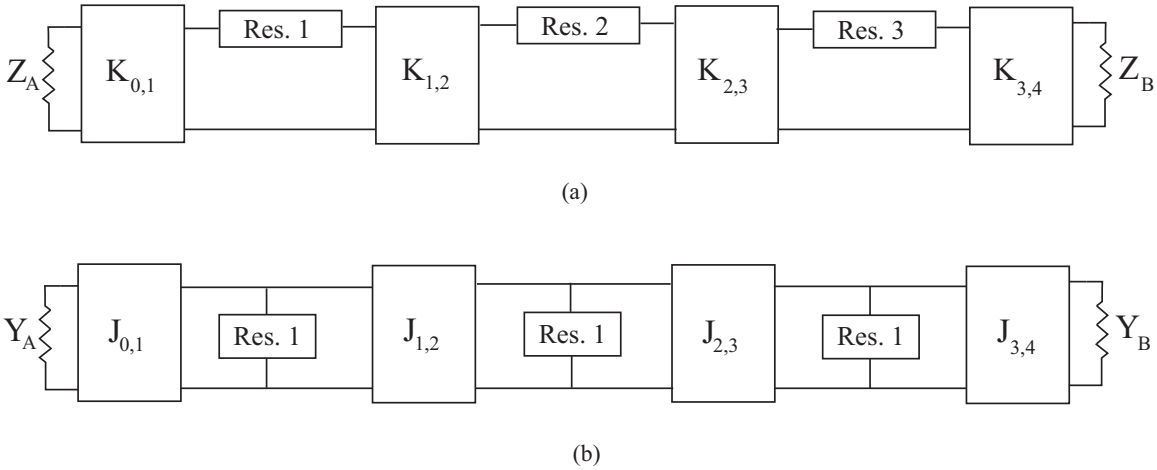


Figure 4.1: End-coupled transmission-line filter using (a) series-type resonators and inductive inverters, (b) parallel-type resonators and capacitive inverters.

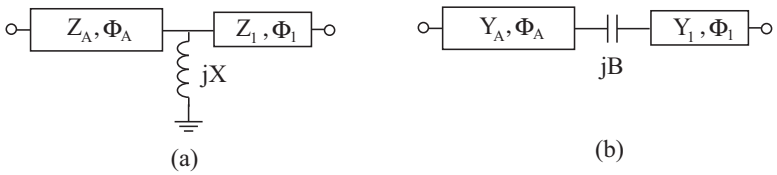


Figure 4.2: Circuit realization of (a) K-inverter using shunt inductor, (b) J-inverter using series capacitor.

4.2 Filter Design

4.2.1 Bandpass Filters and Inverter Design

A ladder combination of series and parallel resonators results in a standard bandpass structure. However, at microwave frequencies this topology is not realizable due to non-practical inductor and capacitor values. Alternatively, bandpass filters may be obtained by combining only one type of resonators through inverters [8][37]. As mentioned in chapter 2, inverters transform a series resonance at their input to a parallel resonance at the output and vice versa. Fig 4.1 shows bandpass filter topologies based on series or parallel transmission-line resonators and inverters. K- and J-inverters are basically the same in terms of their circuit function, but their physical implementation are different, and are typically referred to inductive and capacitive inverters. References [8] and [37] present different circuit implementations of K- and J-inverters. Fig. 4.2 shows simple realizations of inductive and capacitive inverters, suitable for use with transmission-line resonators.

4.2.2 Topology

The transmission-line resonators in Fig. 4.1 can be capacitively tuned using MEMS varactors [45][61]. It is important that the resonator tuning does not affect the coupling mechanism in an uncontrolled fashion. End-coupled half-wave resonators are suitable choices, because the coupling between resonators is implemented in a localized form not a distributed form. This topology provides enough room to integrate MEMS varactors, and the inter-resonator and input/output couplings are achieved through inverters, and not directly affected by the tuning of the resonators. Reference [61] discusses different end-coupled resonator bandpass filter topologies:

1) Filter with capacitive inverters and open-ended half-wave resonators with tapped analog MEMS varactor loading: This filter has two major problems. First, the maximum voltage happens at the end of resonators, so to achieve maximum loading, the tapped varactors should be as close as the end of the resonators, which is hard to implement. Second, the shape and the bandwidth of the pass-band vary strongly with tuning, because the resonance slope parameters and the inverter coefficients vary in different directions upon tuning. As a result, they are not good candidates for wide-band tuning [62]. Fig. 4.3 shows the circuit model for the 2-pole tunable filter with capacitive inverters and

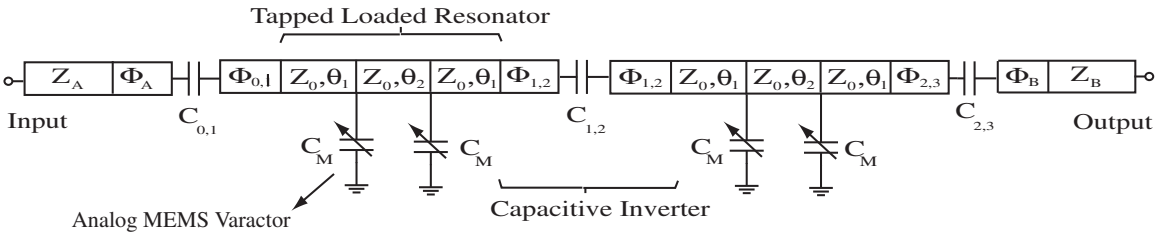


Figure 4.3: The complete circuit model for the 2-pole tunable filter with capacitive coupling and tapped analog MEMS varactor loading .

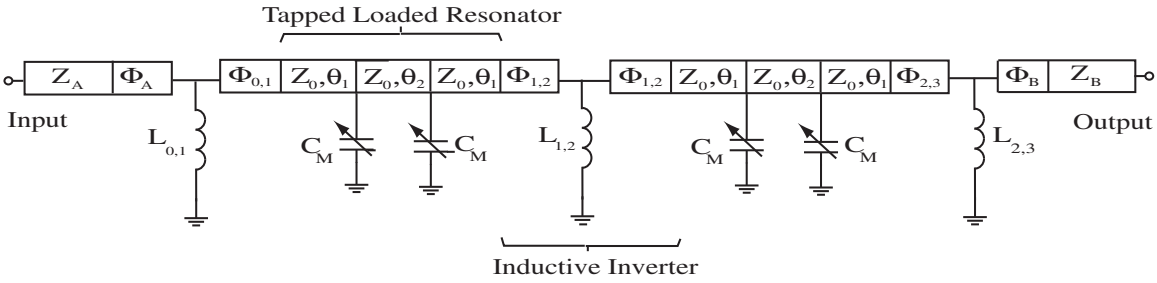


Figure 4.4: The complete circuit model for the 2-pole tunable filter with inductive coupling and tapped analog MEMS varactor loading .

tapped analog MEMS varactor loading.

2) Filter with inductive inverters and short-ended half-wave resonators with tapped analog MEMS varactor loading: As discussed in chapter 3, bandpass filters with capacitive tuning and inductive coupling have weak variation of the passband response over the tuning range and are good candidates for wide-band tuning. An important drawback of this design is the existence of a very close second passband that drastically reduces the upper band rejection of the filter. This is due to the resonance between the inductive inverters and the resonators which show a capacitive behavior above the fundamental resonant frequency. The second passband approaches the lower frequencies when the filter is tuned down, resulting a poor rejection. This is a limitation that makes this design non-practical in spite of its nice tuning behavior. Fig. 4.4 shows the circuit model for the 2-pole tunable filter with inductive inverters and tapped analog MEMS varactor loading.

3) Filter with inductive inverters and short-ended slow-wave MEMS resonators: The center part

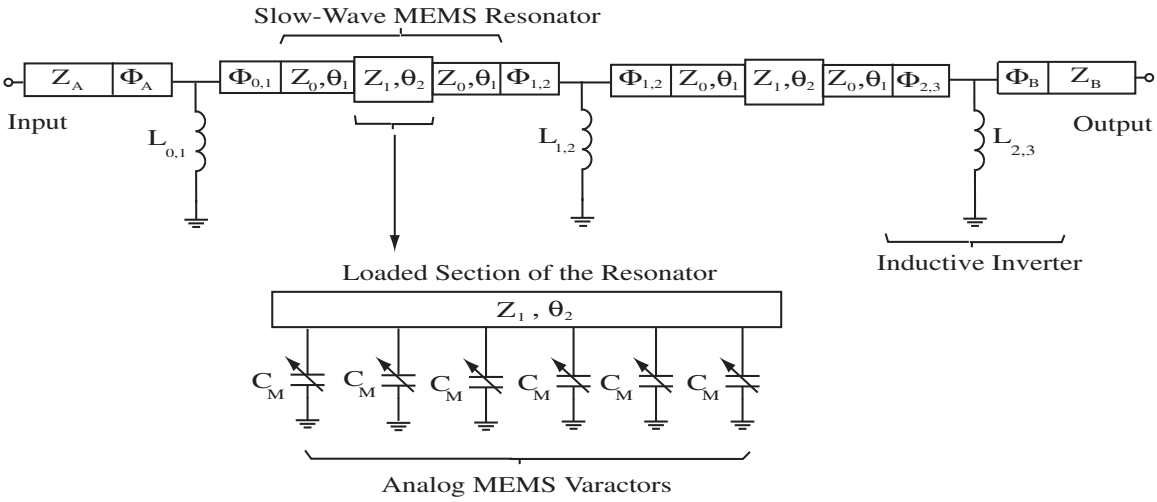


Figure 4.5: The complete circuit model for the 2-pole tunable filter with inductive coupling and slow-wave MEMS resonators.

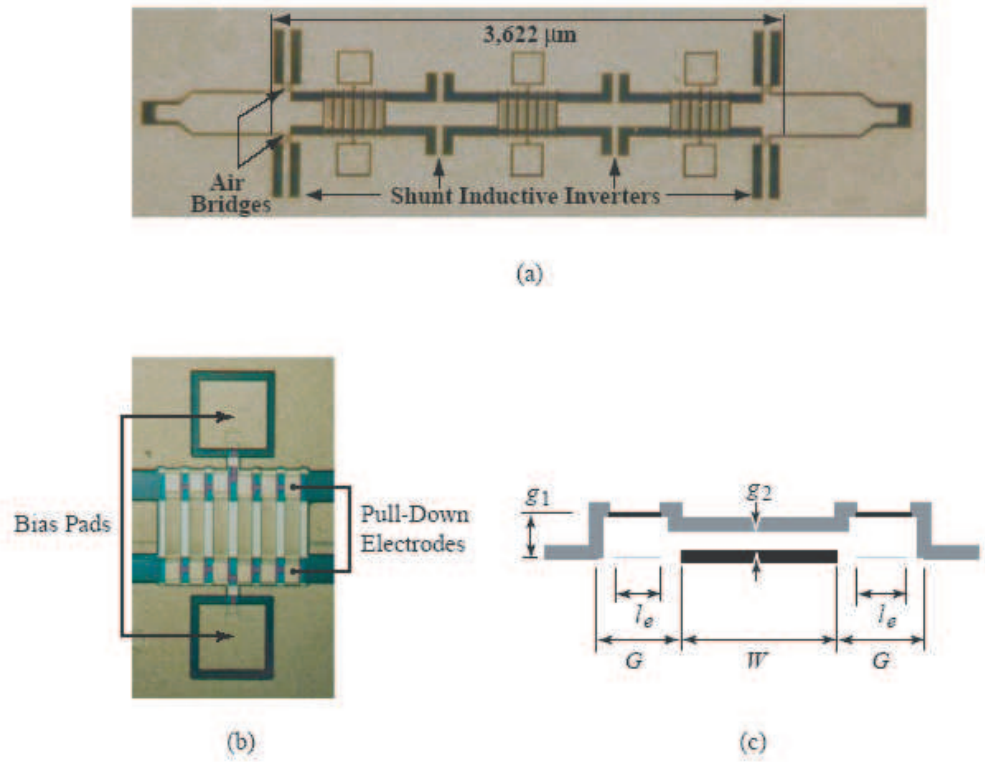
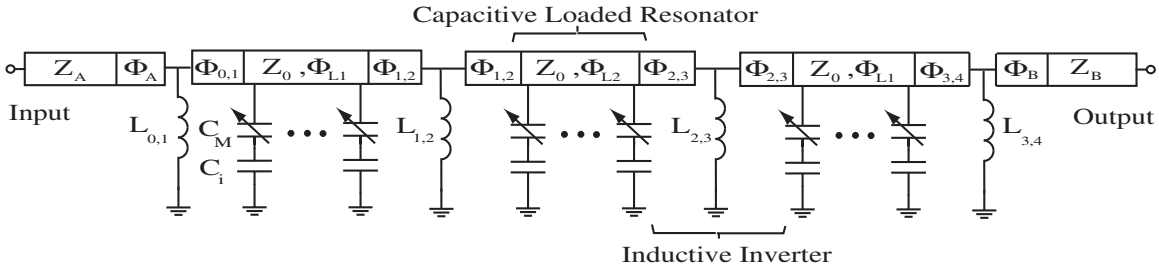


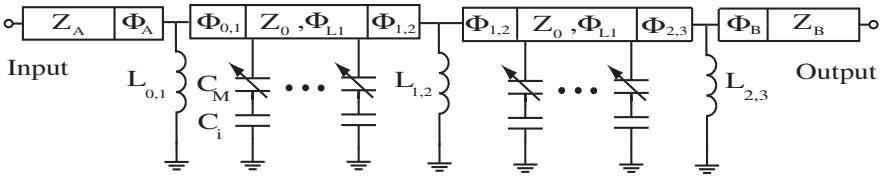
Figure 4.6: The fabricated slow-wave resonator MEMS tunable filter: (a) photograph, (b) tunable slow-wave section, (c) analog MEMS varactor profile.

of the half-wave resonator is loaded by a number of analog MEMS varactors, which results in a slow-wave structure with a smaller effective wavelength and lower characteristic impedance in comparison to the unloaded resonator. Due to the large number of varactors, this type of resonators show a higher tunability as compared to the resonators with tapped loading. Also the short-ended slow-wave resonators are suitable for the inductively-coupled filter, which has a well-behaved tuning. Distributed capacitive loading circumvent the problem of close second pass-band, because the second resonance is eliminated due to loading effect at the center of the resonator. Although this design performs better tunability in comparison to filters with tapped-loaded resonators, it can suffer from limited tunability due to the use of analog MEMS varactors as tuning elements. They may not provide enough capacitance ratio for wide-band tuning.(C_R = 1.3-2.0, 5-15% tuning) [45][22]. Fig. 4.5 shows the circuit model for the 2-pole tunable filter with inductive inverters and slow-wave MEMS resonators. Fig. 4.6(a) shows the photograph of a fabricated 3-pole slow-wave resonator on a glass substrate.Fig. 4.6(b),(c) show 6 individual fabricated MEMS varactors on the loaded section of the CPW line, and the analog MEMS varactor profile, respectively [61].

To achieve all the advantages of the previous designs and also have the capability of tuning from 12 to 18 GHz, a filter with loaded MEMS slow-wave resonators is chosen, but instead of loading the resonator with analog MEMS varactors, digital MEMS switched capacitors are used to load the resonators. Fig. 4.7 presents the circuit model for a two and three-pole loaded resonator tunable filter. Each coplanar waveguide resonator is periodically loaded by 4 switched MEMS capacitors pairs (8 in total). Every switched capacitor is built as a series combination of a MEMS switch with a capacitance ratio of 30-40 and a fixed metal-air-metal (MAM) capacitor (C_i, $i = 1, 2, 3, 4$). The loaded MEMS resonators are coupled through inductive impedance inverters and form a two and three-pole bandpass filter. The inductive impedance inverters are T-combinations of a shunt inductor and two series transmission-lines with negative lengths (Fig. 4.2(a)) [45][61]. The response of the filter can be tuned over a wide frequency range by changing the effective electrical length of the resonators using 16 different combinations (4-bit) of pairs of MEMS switches in the up- and down-state positions.



(a)



(b)

Figure 4.7: Circuit model of (a) a three-pole, and (b) a two-pole loaded resonator tunable filter.

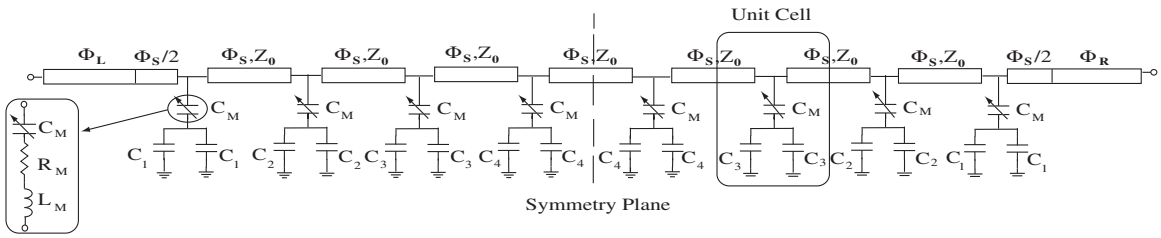


Figure 4.8: Circuit model of a single resonator loaded with 8 capacitive MEMS switches.

Table 4.1: Resonator circuit model element values extracted from ADS simulations.

C_M^{up} (fF)	50	C_M^{down} (fF)	1350	C_1 (fF)	26	C_2 (fF)	31
R_M (Ω)	$0.6 - 0.8$	L_M (pH)	15	C_3 (fF)	43	C_4 (fF)	59
$C_{1(up)}$ (fF)	25.5	$C_{2(up)}$ (fF)	27.6	$C_{1(down)}$ (fF)	50.1	$C_{2(down)}$ (fF)	59.8
$C_{3(up)}$ (fF)	31.5	$C_{4(up)}$ (fF)	35.2	$C_{3(down)}$ (fF)	80	$C_{4(down)}$ (fF)	108.5
$\Phi_{L(Res1)}$	32°	$\Phi_{R(Res1)}$	32°	$\Phi_{L(Res3)}$	32°	$\Phi_{R(Res3)}$	32°
$\Phi_{L(Res2)}$	33°	$\Phi_{R(Res2)}$	33°	Φ_s	4.4°	–	–

4.2.3 Resonator Design

The circuit model of a capacitively-loaded resonator is shown in Fig. 4.8. The loading capacitors are placed in a symmetrical fashion around the middle of the resonator and are actuated in pairs. This results in a symmetrical shape of the standing-wave voltage on the loaded resonator, and therefore, for each state, the maximum voltage level always occurs at the middle point of the resonator. For example, to change the resonant frequency from State-0000 (all the switches are in the up-state position) to State-0001, the two MEMS switches which are in series with MAM capacitors C_1 are pulled down. Due to theresonator symmetry and the fact that the first resonance has a voltage peak at the center, one can use half of the circuit model to find out the resonant condition. The half circuit is obtained by defining a magnetic wall at the symmetry plane in Fig. 4.8. Neglecting the losses in the transmission line and the bridge, the input impedance of the half circuit is given by

$$Z'_{in} = jX'_{in} = j.\frac{N(B_{pi}, \Phi_s, \Phi_L, Z_0)}{D(B_{pi}, \Phi_s, \Phi_L, Z_0)} \tag{4.1}$$

where N and D are real functions of their variables. B_{pi} ($i = 1, 2, 3, 4$) shows the shunt susceptance of a unit cell (MEMS bridge in series with MAM capacitor ($2C_i$, $i = 1, 2, 3, 4$), Z_0 is the characteristic impedance of the unloaded section of the CPW resonator. All loading unit cells have the same electrical distance from each other (Φ_s) with an unloaded t-line impedance of Z_0. Φ_L = Φ_R is the electrical length of the unloaded section of the resonator. The corresponding resonance condition is obtained by forcing X'_{in} = 0 or $N(B_{pi}, \Phi_s, \Phi_L, Z_0)$ = 0. By using the resonance condition and writing a Mat-lab code [64], the required value of the unit cell equivalent capacitance ($C_{i(up)}$, $i = 1, 2, 3, 4$) is determined at a given position which produces a resonance at a given frequency (f_0

= 18 GHz) when all the MEMS switches are in the up-state position.

$$C_{i(up)} = \frac{C_M^{up}.(2C_i)}{C_M^{up} + (2C_i)} \ , \ (i = 1, 2, 3, 4) \tag{4.2}$$

It is assumed that $C_{i(up)}$ is the same for all unit cells. C_M^{up} is the MEMS capacitors in the up-state position and it is the same for all the swtiches, since we are using identical MEMS switches along the resonators. It is also assumed that Φ_s = 4.4° (or 120 μm) at the design frequency to make the loading unit cells realizable, Z_0 = 78 Ω to minimize the CPW-line ohmic loss, and the unloaded electrical length of the resonator Φ_L = Φ_R =$(1/2).(\pi - 8\Phi_s)$. Another quality of interest for a filter designer is the reactance slope parameter of the resonator, x_{in}, which is defined for resonance at ω_0 as [8]

$$x_{in} = \frac{\omega_0}{2}\frac{\partial X_{in}}{\partial \omega} \tag{4.3}$$

The reactance slope can be calculated using the half-circuit input reactance in (4.1) to give:

$$x_{in} = 2x'_{in} = \omega_0 \frac{\partial X'_{in}}{\partial \omega} \tag{4.4}$$

The value of x_{in} is used to determine the inverter ratios in next section. By using the resonator circuit model in ADS [38] (Fig. 4.8) and adjusting the values of C_1, C_2, C_3, C_4 when each MEMS switch is actuated to the down-state position, the resonator covers the 12-18 GHz frequency range. $C_{i(down)}$ is the unit cell equivalent capacitor value when the MEMS switch is in the down-state position

$$C_{i(down)} = \frac{C_M^{down}.(2C_i)}{C_M^{down} + (2C_i)} \ , \ (i = 1, 2, 3, 4) \tag{4.5}$$

where C_M^{down} is the down-state position capacitance. Table 4.1 shows the values for the MEMS capacitors in the up- and down-state positions (C_M^{up} and C_M^{down}), the MAM capacitors (C_1, C_2, C_3, C_4) and the equivalent unit cell capacitance in up- and down-state positions ($C_{i(up)}$, $C_{i(down)}$).

The largest loading unit cells (MAM capacitors C_4 in series with the MEMS switches) are placed close to the middle of the resonator and can shift the resonant frequency from 18 GHz to around 14 GHz when they are pulled down. The smallest loading unit cells are placed farther from the middle of the resonator and are for fine tuning. Table 4.1 also shows the electrical length of the

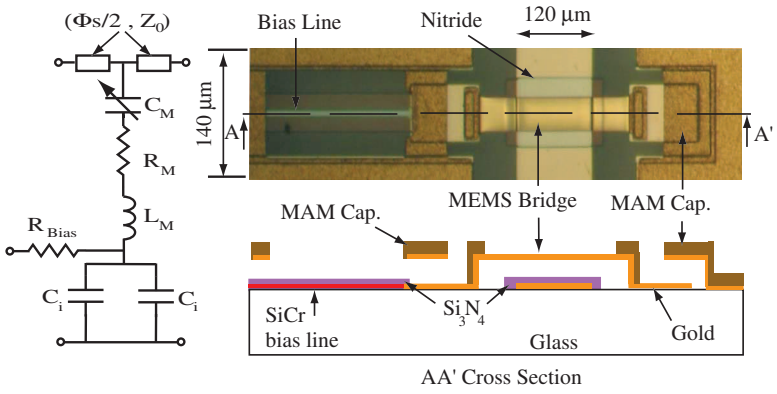


Figure 4.9: Circuit model and the practical realization of a unit cell in a loaded resonator.

unloaded sections for each resonator simulated in ADS (Φ_{Li}, Φ_{Ri}, $i = 1, 2, 3$). Because the MAM capacitors are not the same, $C_{i(up)}$ is not the same for all the unit cells as assumed in the resonance condition, but as can be seen in Table 4.1 ,$C_{i(up)}$ variation is less than 10 fF for different MAM capacitors, which results a small shift in the resonant frequency. This variation can be compensated by tweaking the electrical length of the unloaded section of the resonator in ADS.

A practical realization of a unit cell is shown in Fig. 4.9, and the physical length of each unit cell is 140 μm. The finite width of the bridge and MAM capacitors and the current path over the bridge result in a phase delay which reduces the effective physical length of a unit cell to 100 μm, and the spacing between two adjacent unit cells is 20 μm, and hence $l_s = 120$ μm. Z_0 is assumed to be 78 Ω to minimize the conduction loss of the CPW. The real physical lengths of the unloaded sections will be reduced in the practical realization due to the negative t-line lengths of the inductive inverters.

All resonators are simulated using Sonnet [56] with CPW dimensions of 70/120/70 μm on a 500 μm glass substrate ($\epsilon_r = 4.6$ and $\tan\delta = 0.01$ at 18 GHz). The dimensions of the CPW line are chosen to minimize the conductor loss [65]. The measured unloaded CPW line parameters are $Z_0 = 78$ Ω and $\epsilon_{reff} = 2.8$, and $\alpha_0 = 42$ dB/m at 18 GHz with 2 μm electroplated gold. Table 4.2 shows the transmission line parameters for the four different loaded sections of the resonator [45]. The quality factor for an unloaded resonator is calculated from:

$$Q_0 = \frac{\pi}{\alpha_0 \lambda_{eff}} \tag{4.6}$$

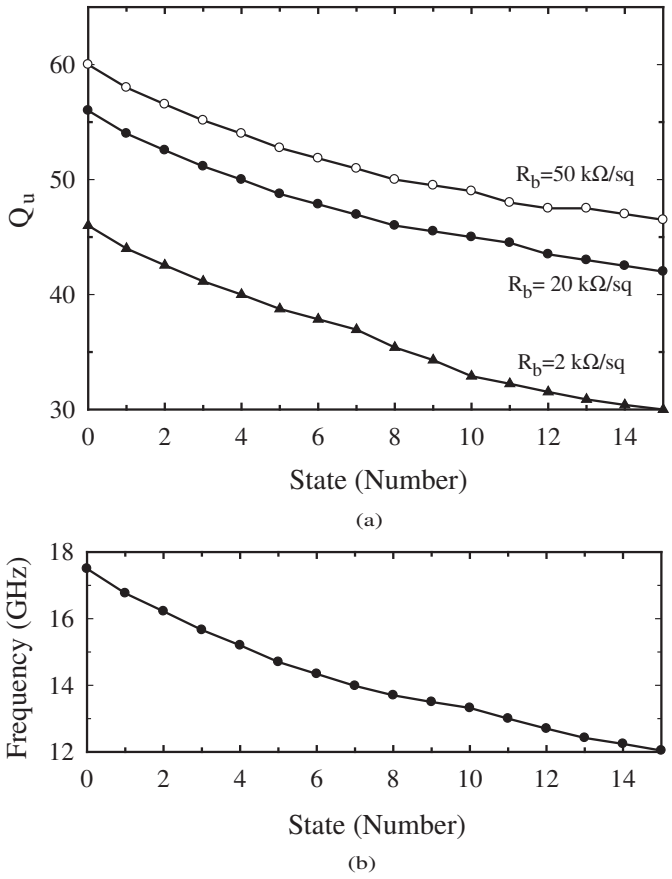


Figure 4.10: Simulated (a) Unloaded quality factor, and (b) resonant frequency for a tunable loaded resonator.

and is 65 at 18 GHz for the unloaded CPW resonator. For the loaded sections, the quality factor is calculated in the up- or down state positions using [63] (assuming R_{bias} =∞):

$$Q_L = Q_0 . \frac{Z_L}{Z_0} \tag{4.7}$$

These values all are presented in Table 4.2. Fig. 4.10(a),(b) show the simulated unloaded quality factor of the loaded resonator for different bias line resistances, and the resonant frequency for 16 different combinations of the switches, respectively. This is done using a single resonator which is weakly coupled to the input and output ports and the simulated resonant frequency and quality factor for each different state is obtained using ADS based on the values of Table 4.1.

Table 4.2: Unit cell circuit-model element values extracted from ADS simulations at 18 GHz.($Z_0 =$ 78 Ω, $\epsilon_{reff} = 2.8$, $\alpha_0 = 42$ dB/m, $Q_0 = 65$)

–	$Z_{i(up)}$ (Ω)	$Z_{i(down)}$ (Ω)	$\epsilon_{i,eff(up)}$	$\epsilon_{i,eff(down)}$	$Q_{i(up)}$	$Q_{i(down)}$
$i = 1$	39.5	30.2	11.0	18.9	33	25
$i = 2$	38.4	27.9	11.7	22.1	32	23
$i = 3$	36.5	24.5	12.9	28.6	30	20
$i = 4$	35	20.6	14.1	40.9	29	17

Table 4.3: Chebyshev filter coefficients for a 2 and 3-pole response with 0.1 dB pass-band ripple.

$Filter$	g_0	g_1	g_2	g_3	g_4
$3-$pole	1	1.0315	1.1474	1.0315	1
$2-$pole	1	0.8430	0.6220	1.3554	–

4.2.4 Inverter Design

The final section of the filter design is the inductive inverter implementation. The goal is to design 2 and 3-pole, 6%, 0.1 dB ripple, Chebyshev filters. Table 4.3 shows the lowpass prototype element values for these filters [8]. For the terminating source and load resistance of $Z_A = Z_B =$ 50 Ω and a fractional bandwidth of ω = 6%, the required values of inverter ratios are calculated using the standard formulas given in [8]

$$K_{0,1} = \sqrt{\frac{x_{in}\omega Z_A}{g_0 g_1}} \tag{4.8}$$

$$K_{n,n+1} = \sqrt{\frac{x_{in}\omega Z_B}{g_n g_{n+1}}} \tag{4.9}$$

$$K_{j,j+1} = \omega\frac{x_{in}}{\sqrt{g_j g_{j+1}}}\ ,\ \big(j = 1 \rightarrow n, (n = 2, 3)\big) \tag{4.10}$$

where x_{in} is the reactance slope of the loaded resonator calculated in 4.2.3. Design equations for the input/output and interstage inductive inverters in Fig. 4.7 are obtained as follows[8][61]

Table 4.4: Input/output and interstage inductive inverter element values for 2 and 3-pole filters at 18 GHz.

Filter	$\Phi_A = \Phi_B$ °	$\Phi_{0,1}$ °	$\Phi_{1,2}$ °	$\Phi_{2,3}$ °	$\Phi_{3,4}$ °
$3-$pole	-23	-14	-5.3	-5.3	-14
$2-$pole	-22.5	-13.5	-6.4	–	–
Filter	$L_{0,1}$ (pH)	$L_{1,2}$ (pH)	$L_{2,3}$ (pH)	$L_{3,4}$ (pH)	–
$3-$pole	204	65	65	204	–
$2-$pole	196	78	196	–	–

$$X_{0,1} = \frac{Z_0}{\sqrt{((K_{0,1}/Z_0)^2 - 1)(Z_A/Z_0)^2 + ((Z_0/K_{0,1})^2 - 1)}} \tag{4.11}$$

$$X_{n,n+1} = \frac{Z_0}{\sqrt{((K_{n,n+1}/Z_0)^2 - 1)(Z_B/Z_0)^2 + ((Z_0/K_{n,n+1})^2 - 1)}} \tag{4.12}$$

$$X_{j,j+1} = \frac{K_{j,j+1}}{\sqrt{1 - (K_{j,j+1}/Z_0)^2}}\ ,\ \big(j = 1 \rightarrow n-1, (n = 2, 3)\big) \tag{4.13}$$

$$p_{0,1} = p_{n,n+1} = -tan^{-1}\Big[\big(\frac{Z_0}{Z_A} + 1\big)\big(\frac{X_{0,1}}{Z_0}\big)\Big] \tag{4.14}$$

$$q_{0,1} = q_{n,n+1} = -tan^{-1}\Big[\big(\frac{Z_0}{Z_A} - 1\big)\big(\frac{X_{0,1}}{Z_0}\big)\Big] \tag{4.15}$$

$$\Phi_A = \Phi_B = \frac{p_{0,1} + q_{0,1}}{2}, \tag{4.16}$$

$$\Phi_{0,1} = \Phi_{n,n+1} = \frac{p_{0,1} - q_{0,1}}{2}, \tag{4.17}$$

$$p_{j,j+1} = -tan^{-1}\Big(\frac{2X_{j,j+1}}{Z_0}\Big), \tag{4.18}$$

$$\Phi_{j,j+1} = \frac{p_{j,j+1}}{2}\ ,\ \big(j = 1 \rightarrow n-1, (n = 2, 3)\big) \tag{4.19}$$

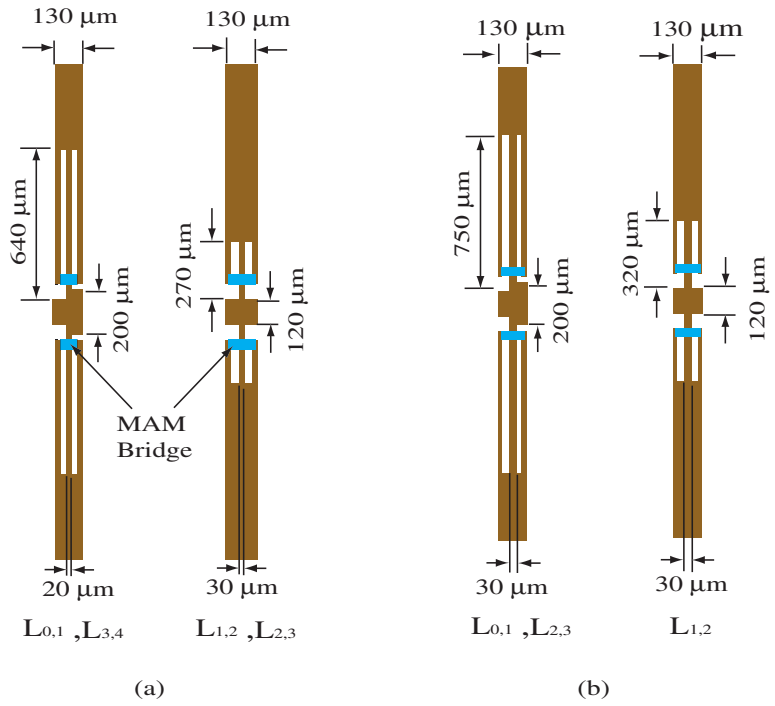


Figure 4.11: Physical realization of (a) three-pole filter (b) two-pole filter inductive inverters.

where Z_0 is the characteristic impedance of the unloaded section of the resonator and $Z_A = Z_B = 50\ \Omega$ are the terminating source and load characteristic impedances. Table 4.4 shows the element values for 2 and 3-pole inductive inverters at 18 GHz. The series transmission lines with negative electrical lengths are absorbed in the unloaded sections of each resonator [8][45]. Shunt inductors are suited for CPW designs, and are created by connecting the center conductor and the ground plane of the CPW line using high impedance (narrow) t-lines [66]. For inductor values grater than 20-30 pH, it is generally necessary to extend the high impedance lines inside the CPW ground plane. In the asymmetric configuration with $Z_A = Z_B = 50\ \Omega$ (port impedance) and $Z_0 = 78\ \Omega$ (filter impedance), at the input/output inverters, these CPW stubs can support slot-line modes and cause radiation. To avoid such a problem, these modes must be grounded by connecting the two halves of the CPW ground at the stub input by a MAM air bridge. Losses can be taken into account by adding a series resistance to the inductor in the circuit model. The physical realization of shunt inductors in CPW transmission lines is shown in Fig. 4.11. The length and width of the inductive short-circuit slots are found using a full-wave simulator (Sonnet).

4.2.5 Simulation Results

Fig. 4.12 shows the simulated insertion loss for 16 different states with $\mathrm{R_{bias}}$ = 2 $\mathrm{k\Omega/sq}$ for a 3-pole filter, and is 5.4 and 8 dB at 17.8 and 12.2 GHz, respectively. Fig. 4.13 shows the simulated insertion loss for 16 different states for a 2-pole filter, and is 4.2 and 6.6 dB at 17.8 and 12.1 GHz, respectively. The higher insertion loss at the lower frequency is due to the higher loss factor of a loaded transmission line and the low-resistivity bias line which has a strong loading effect when all the switches are in the down-state position. The loss is $1-2$ dB better with $\mathrm{R_{bias}}$ = 20 $\mathrm{k\Omega/sq}$ (Figs. 4.12, 4.13). Fig .4.14(a),(b) present the simulated insertion loss of the 3-pole and 2-pole filters for states 0 and 15 from 5-50 GHz, respectively. Both ADS and Sonnet simulators predict the filter second pass-band at 34 GHz for state 15, ($f_0 = 12.1$ GHz), and 43 GHz for state 0, ($f_0 = 17.8$ GHz), respectively. It is seen that the second pass-band in both 2-pole and 3-pole filters is far enough from the main pass-band. As mentioned before, this is because the second resonance is eliminated due to distributed capacitive loading effect at the center of the resonators.

4.3 Fabrication and Measurement

4.3.1 Fabrication, Implementation and Biasing

The tunable filter is fabricated on a 500 μm glass substrate ($\epsilon_r = 4.6$, $\tan\delta = 0.01$) using coplanar waveguide lines and MEMS switches, with a standard RF MEMS process developed at the University of Michigan such as the filter in chapter 3. The width, length, and thickness of the MEMS bridge are $60\,\mu\mathrm{m}$, $280\,\mu\mathrm{m}$, and $0.8\,\mu\mathrm{m}$, respectively and the gap is $1.5\,\mu\mathrm{m}$ for the bridge and MAM capacitors (Fig. 4.9). The bottom plate of one of the MAM capacitors is connected to the thin-film resistor to bias the bridge. The measured pull-in voltage is $V_p = 18$ V, with a corresponding spring constant of $k = 24$ N/m ($V_p = 18$ V, $g_0 = 1.5$ μm, $A = wW = 70\ \mu\mathrm{m} \times 120$ μm), and a residual stress of $\sigma = 41$ MPa. The mechanical resonant frequency and quality factor of the switch are $f_0 = 72$ kHz and $Q_m = 1$, respectively [20]. The mechanical parameters are all calculated using the same equations in chapter 3.

The photographs of the complete 2 and 3-pole 12-18 GHz filter are shown in Fig. 4.15. The 3-pole filter is composed of three resonators each one loaded with 8 unit cells, two inductive inverters

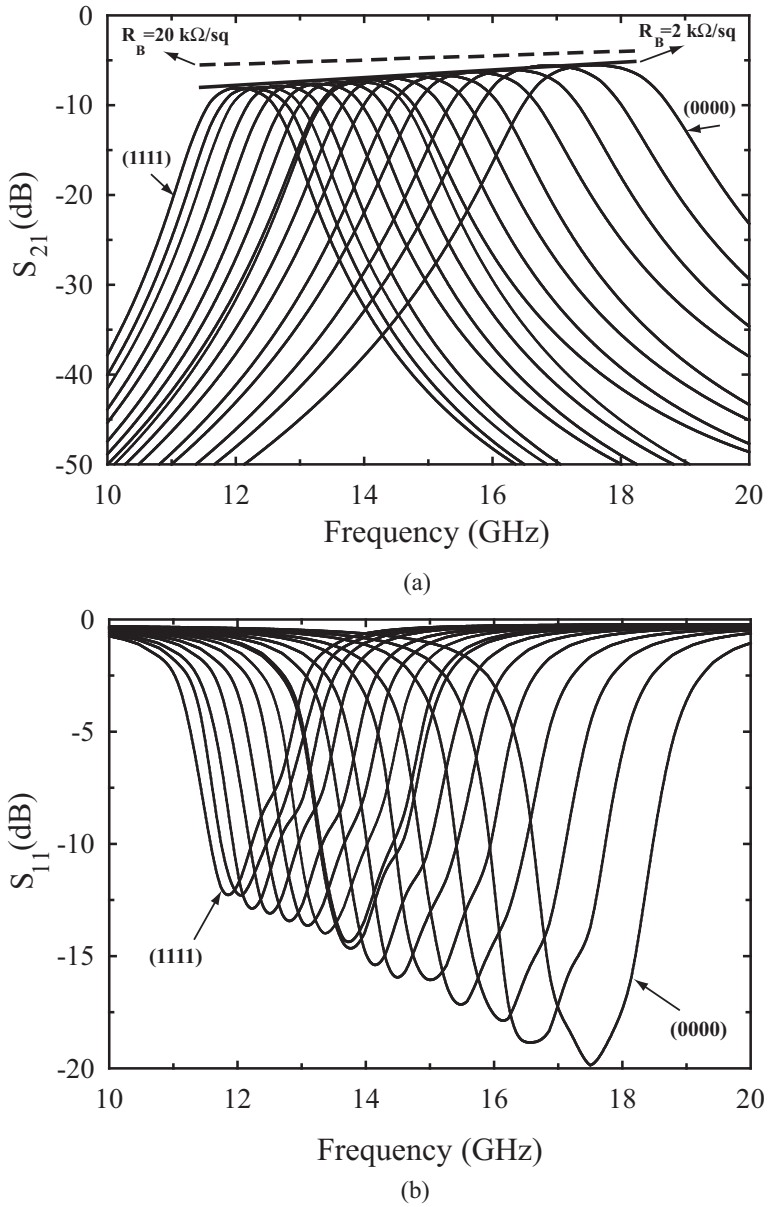
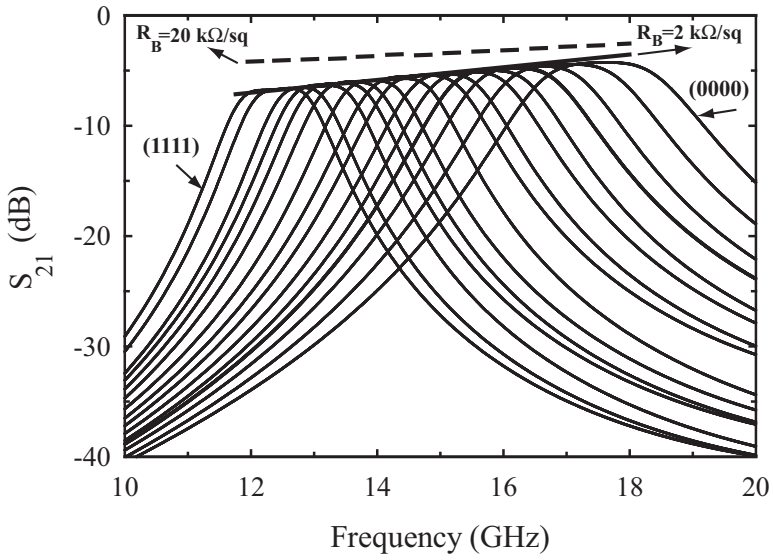
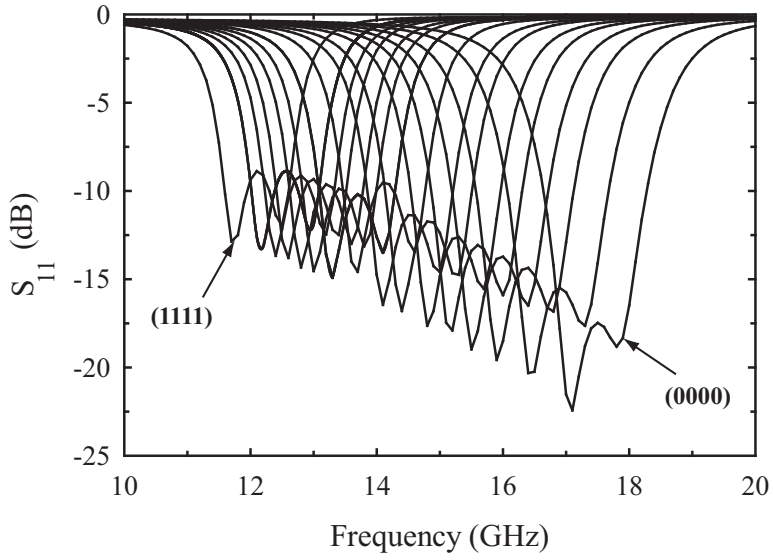


Figure 4.12: Simulated (a) I.L., and (b) R.L. of the tunable three-pole 12-18 GHz filter.

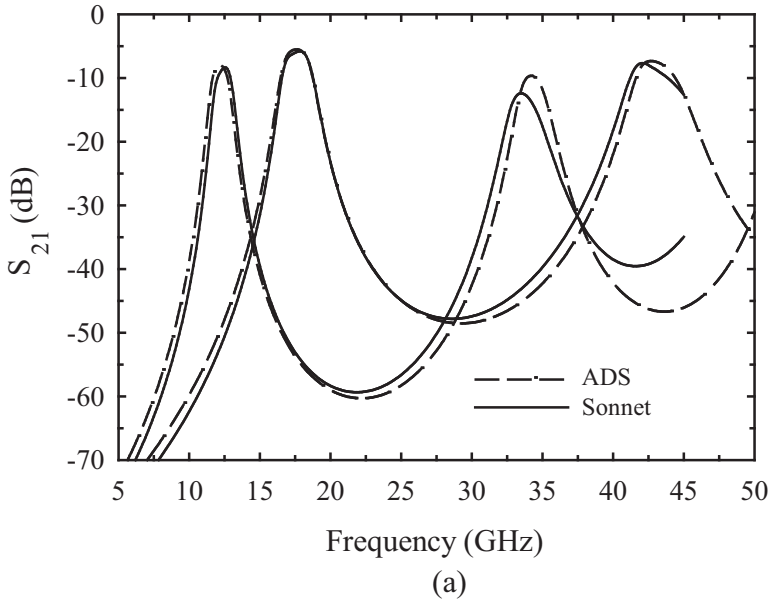


(a)

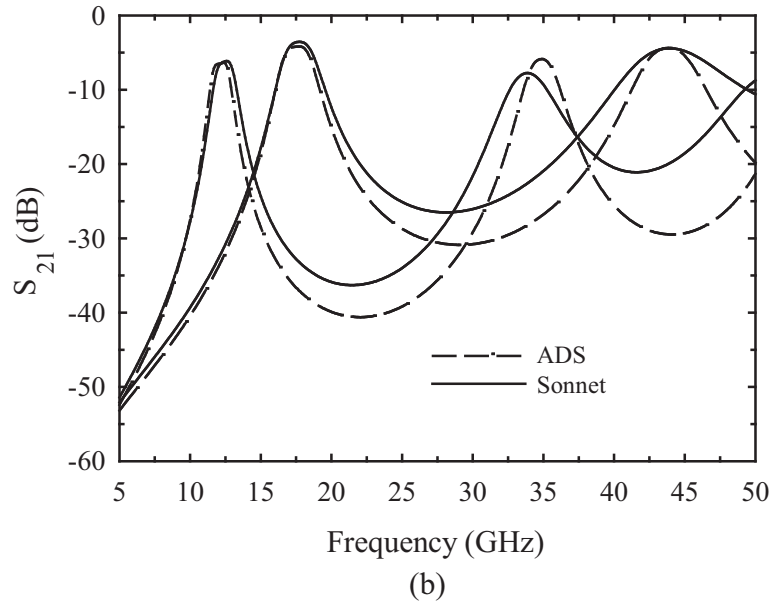


(b)

Figure 4.13: Simulated (a) I.L., and (b) R.L. of the tunable three-pole 12-18 GHz filter.

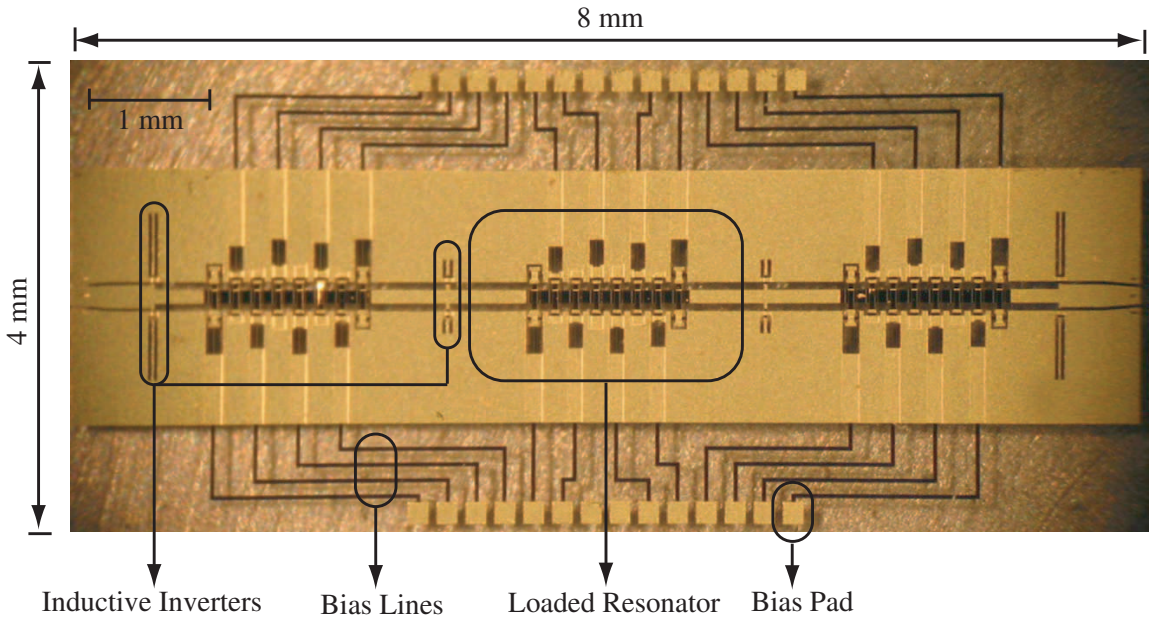


(a)

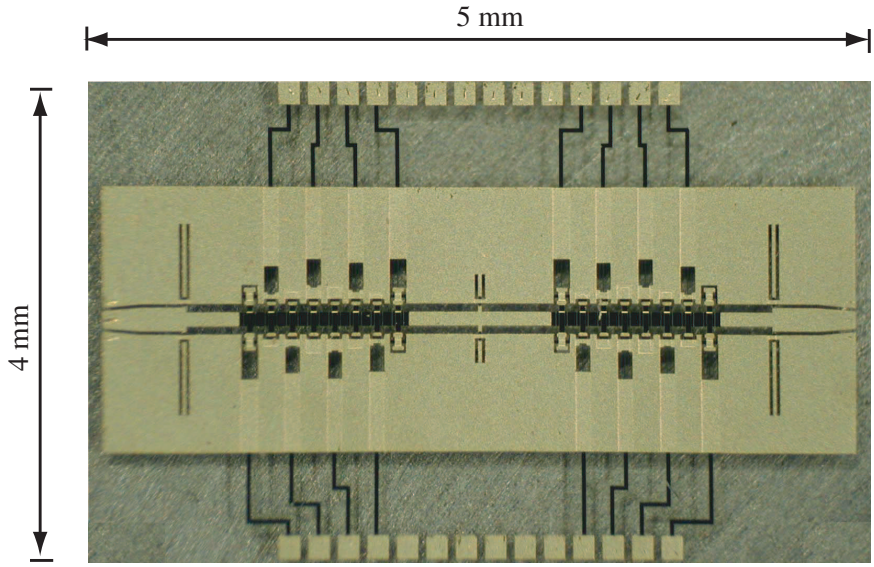


(b)

Figure 4.14: Simulated I.L. of (a) the 3-pole, and (b) the 2-pole tunable filters for states 0 and 15 from 5-50 GHz.



(a)



(b)

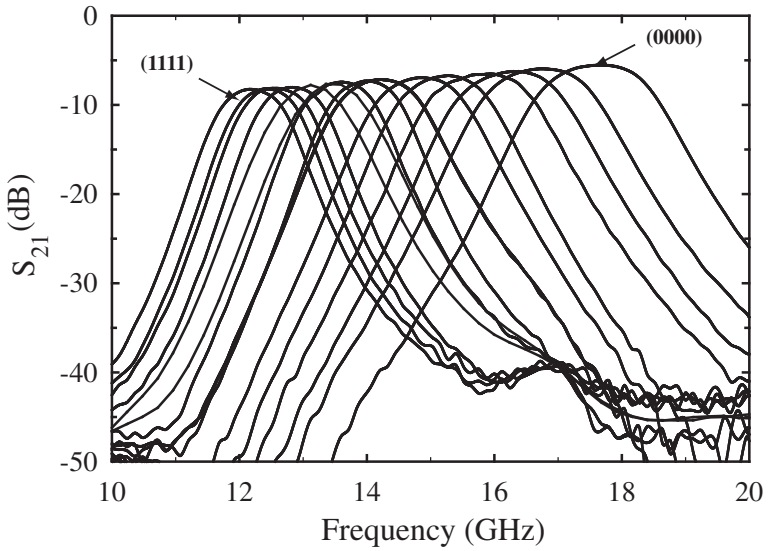
Figure 4.15: Photographs of the complete (a) three-pole and (b) two-pole 12-18 GHz filters fabricated on a glass substrate.

at the input and output of the filter, and two inductive inverter between loaded resonators. The 2-pole filter is composed of two resonators each one loaded with 8 unit cells, two inductive inverters at the input and output of the filter, and one inductive inverter between loaded resonators. Each switch has a separate SiCr DC bias line for independent control. The center conductor of the coplanar loaded resonators is connected to the DC ground pad through the RF probe using a bias tee. The filter is excited using GSG single-ended probes with a pitch of $150\,\mu\mathrm{m}$.

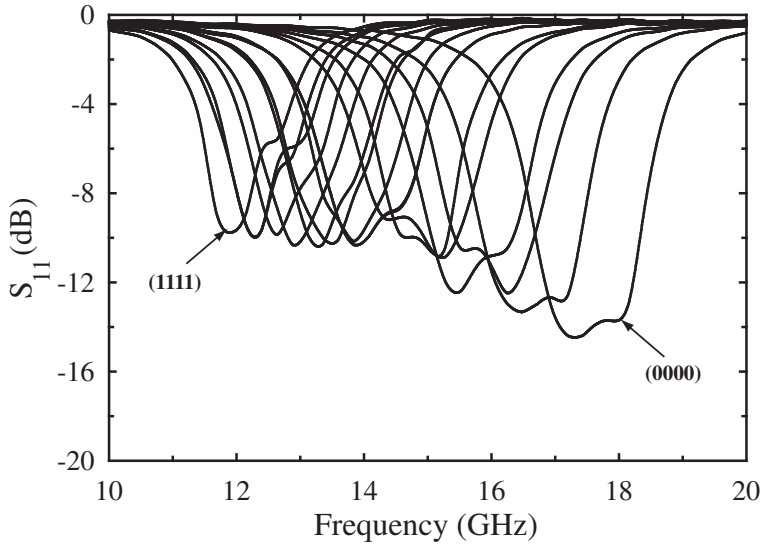
4.3.2 Measurements

The 2 and 3-pole tunable filters are measured using CPW probes and TRL calibration. The measured results are shown in Figs. 4.16 and 4.17 for 16 different states. For the 3-pole filter, the insertion loss (Fig. 4.16(a)) is 5.5 dB and 8.2 dB at 17.8 GHz and 12.2 GHz respectively, and for the 2-pole filter, the insertion loss (Fig. 4.17(a)) is 4.3 dB and 6.8 dB at 17.8 GHz and 12.1 GHz respectively. The relative bandwidth is approximately fixed for the whole tuning range as expected from the simulation results. For a 3-pole filter, the return loss (Fig. 4.16(b)) is better than 10 dB over the whole tuning range. The 2-pole filter has a return loss (Fig. 4.17(b)) which is below 10 dB for 12-15 GHz frequency range.

For the 3-pole filter, the measured center frequency and loss for each of the 16 different states is presented in Fig. 4.18(a). Fig. 4.18(b) shows the relative bandwidth variation for all responses, and is 6.1% at 17.8 GHz (State 0), and 5.3% at 12.2 GHz (State 15). Fig. 4.19 compares the measured and simulated insertion loss for three arbitrary states at 17.8 GHz (State 0), 14 GHz (State 8), and 12.2 GHz (State 15), and the simulated and measured responses agree very well. For the case of ($\mathrm{R_{bias}}$ = 20 $\mathrm{k\Omega/sq}$), the simulated insertion loss is 1.0 dB better at 17.8 GHz, 1.4 dB better at 14 GHz, and 2.2 dB better at 12.2 GHz as compared with the measurements with $\mathrm{R_{bias}}$ = 2 $\mathrm{k\Omega/sq}$. The measured response of a fabricated filter without any bias lines also confirms that the insertion loss improves by 0.8 dB at 17.8 GHz (all the switches are electroplated in the up-state position) to 2.0 dB at 12.2 GHz (all the switches are electroplated in the down-state position). It is seen that the measured filter rejection in the upper stop-band is around 10 dB worse than the simulated one for different states. Because the CPW line grounds are not wide enough, they provide a direct path for leakage currents through their edges between the input and output terminals. They add up to

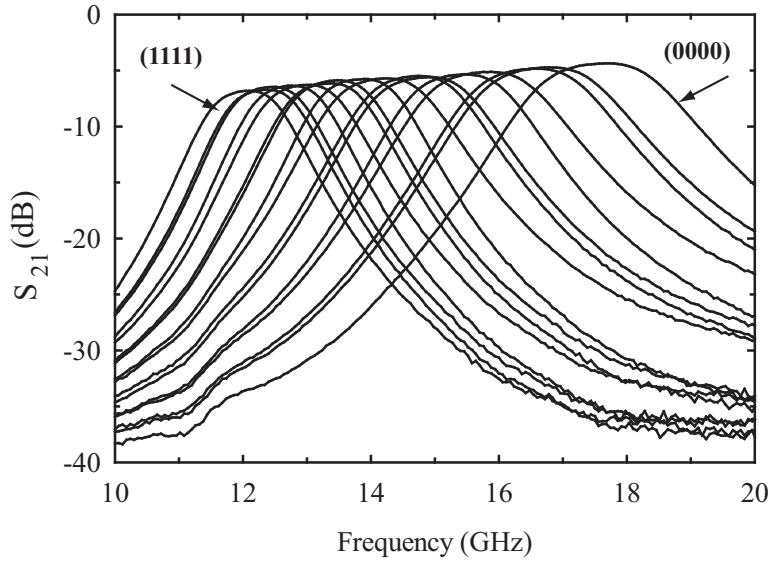


(a)

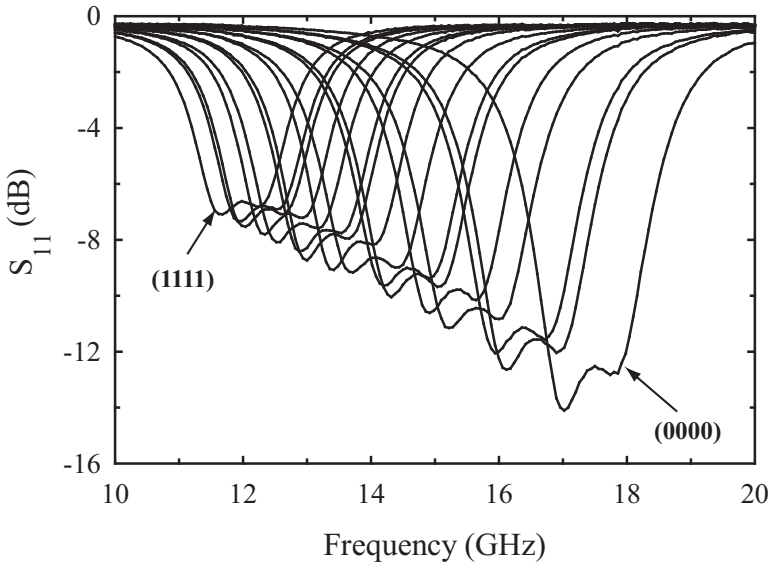


(b)

Figure 4.16: Measured (a) I.L., and (b) R.L. of the tunable three-pole 12-18 GHz filter.



(a)



(b)

Figure 4.17: Measured (a) I.L., and (b) R.L. of the tunable two-pole 12-18 GHz filter.

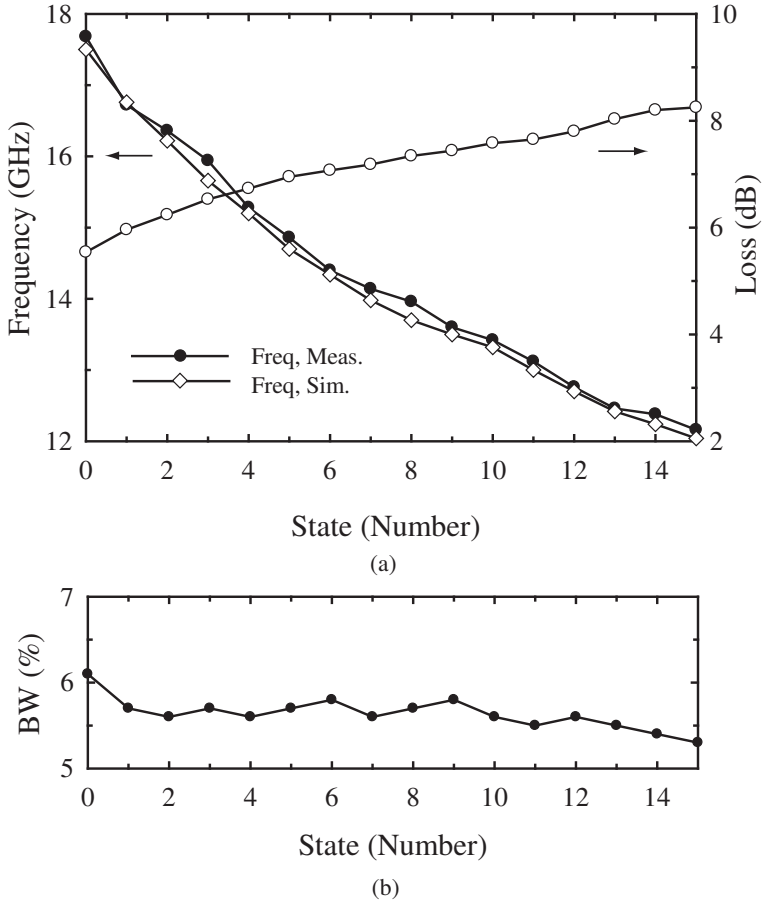


Figure 4.18: (a) Measured center frequency and loss, and (b) measured relative bandwidth of the 16 filter responses ($5.7 \pm 0.4\%$) for the 3-pole filter.

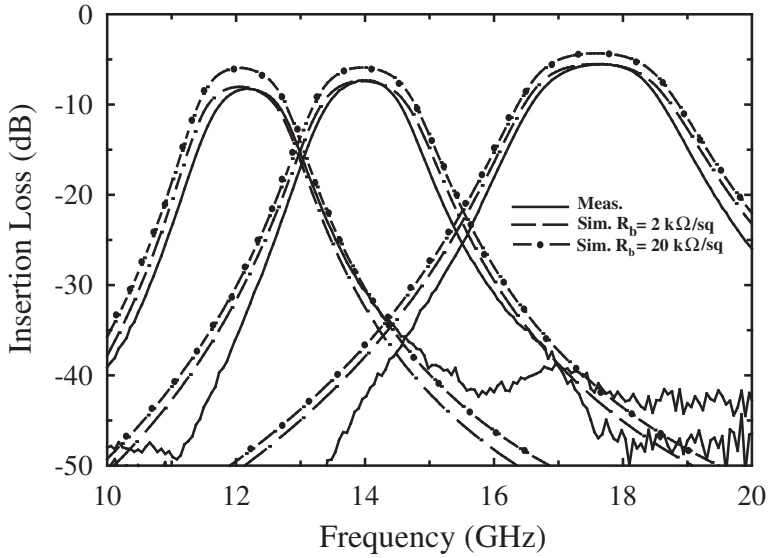
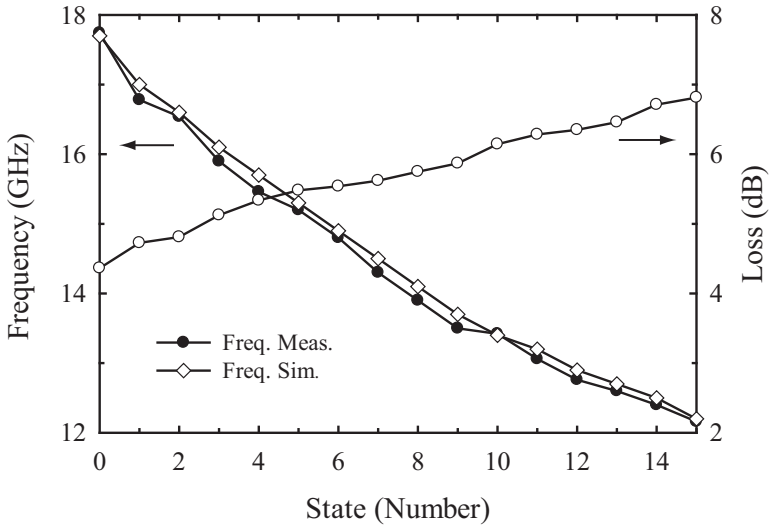


Figure 4.19: Comparison between the measured and simulated insertion loss for three arbitrary states at 12.8 (State 15), 14.0 (State 8), and 17.8 GHz (State 0).

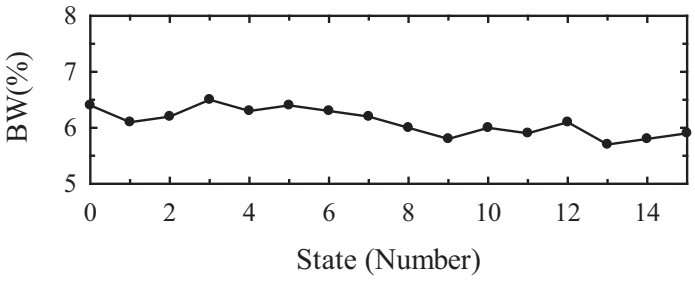
the main signal at the output of the filter and change the filter rejection at the upper stop-band. The effect of leakage currents in the filter upper stop-band does not appear in the simulation results, because the full-wave simulator is not accurate enough to consider these currents at the edge of the CPW ground.

For the 2-pole filter, the measured center frequency and loss for each of the 16 different states is presented in Fig. 4.20(a). Fig. 4.20(b) shows the relative bandwidth variation for all responses, and is 6.4% at 17.8 GHz (State 0), and 5.8% at 12.1 GHz (State 15). Fig. 4.19 compares the measured and simulated insertion loss for three arbitrary states at 17.8 GHz (State 0), 14.8 GHz (State 5), and 12.1 GHz (State 15), and the simulated and measured responses also agree very well for the 2-pole filter. For the case of ($\mathrm{R_{bias}}$ = 20 $\mathrm{k\Omega/sq}$), the simulated insertion loss is again 1.0 dB better at 17.8 GHz, 1.2 dB better at 14.8 GHz, and 2 dB better at 12.1 GHz as compared with the measurements with $\mathrm{R_{bias}}$ = 2 $\mathrm{k\Omega/sq}$.

Table 4.5 shows a comparison between insertion values of two- and three-pole filters at $f_{min} =$ 12.1 GHz and $f_{max} = 17.8$ GHz for R_b = 2 $\mathrm{k\Omega/sq}$ and R_b = 20 $\mathrm{k\Omega/sq}$.



(a)



(b)

Figure 4.20: (a) Measured center frequency and loss, and (b) measured relative bandwidth of the 16 filter responses (6.1±0.4%) for the 2-pole filter.

Table 4.5: Summary of I.L. values for two- and three-pole filters (f_{min} = 12.1 GHz, f_{max} = 17.8 GHz)

Filter (I.L.)	f_{max}	f_{min}
$2-\text{pole}\ (\text{Meas.}, \text{R}_\text{b} = 2\ \text{k}\Omega/\text{sq})$	4.3	6.8
$2-\text{pole}\ (\text{Sim.}, \text{R}_\text{b} = 20\ \text{k}\Omega/\text{sq})$	3.4	4.8
$3-\text{pole}\ (\text{Meas.}, \text{R}_\text{b} = 2\ \text{k}\Omega/\text{sq})$	5.5	8.2
$3-\text{pole}\ (\text{Sim.}, \text{R}_\text{b} = 20\ \text{k}\Omega/\text{sq})$	4.7	6.2

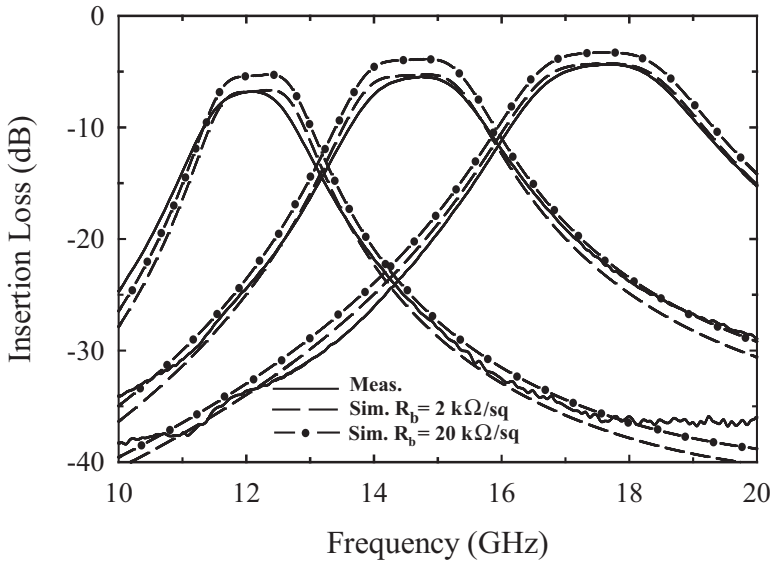


Figure 4.21: Comparison between the measured and simulated insertion loss for three arbitrary states at 12.8 (State 15), 14.0 (State 8), and 17.8 GHz (State 0).

4.4 Nonlinear Characterization

The nonlinear analysis of MEMS switches, varactors and tunable filters has been presented in [21] and in chapter 3. This analysis shows for high level RF signals, the MEMS bridge capacitance self pull-down results in a nonlinear behavior of the tunable filter. In the case of two RF signals, third order intermodulation is generated. To measure the intermodulation components at the output of the tunable filter, the setup shown in Fig. 4.22 is used.

Fig. 4.23 shows the measured output power for the fundamental and the intermodulation components for several values of Δf ($f_1 - f_2$). The measured IIP_3 is $>$ 37 dBm for $\Delta f >$ 200 kHz. The measurement is in the up-state position, (0000), since this state gives the worse IM_3 products. Fig. 4.23 also shows the intermodulation component vs. the difference frequency between input tones (Δf) for P_{in}= 3 dBm (no bias voltage on the bridges). The intermodulation component follows the mechanical response of the bridge, and the IM_3 level drops by 40 dB/decade for $\Delta f > f_0$ which is in agreement with theory [21] (f_0 is the mechanical resonant frequency). This means that IIP_3 is $>$ 77 dBm at a difference frequency of 2 MHz, which is very hard to measure and is quite impressive.

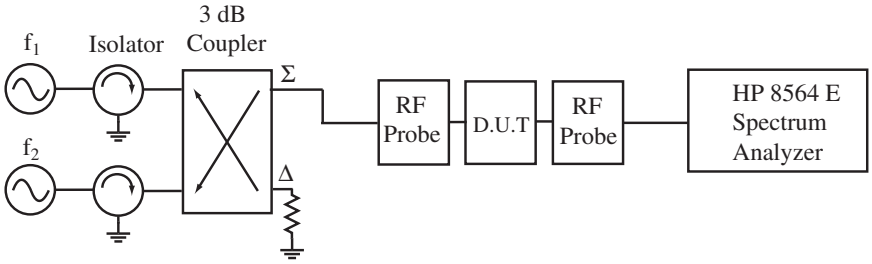


Figure 4.22: Experimental setup for intermodulation measurements ($\Delta f = f_2 - f_1$).

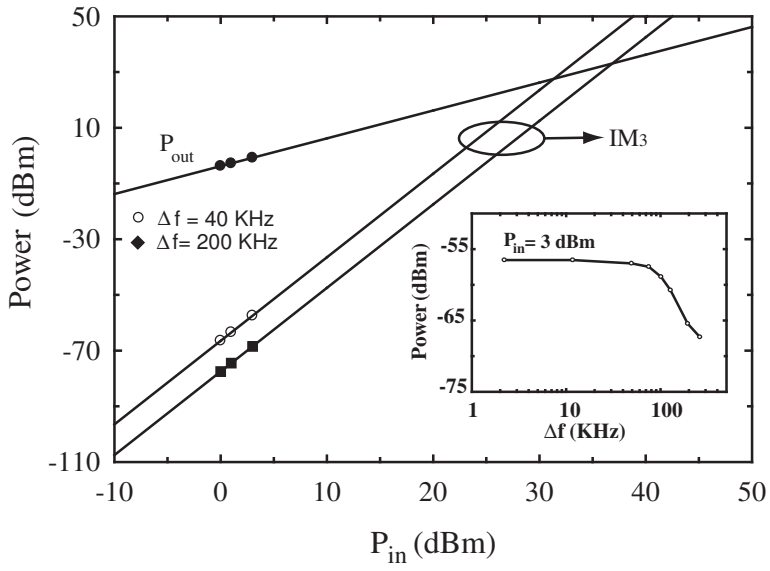


Figure 4.23: Nonlinear measurements at V_b = 0 V: The fundamental and intermodulation components vs. the input power, and the two-tone IM_3 vs. the beat frequency at $f_0 = 17.8$ GHz.

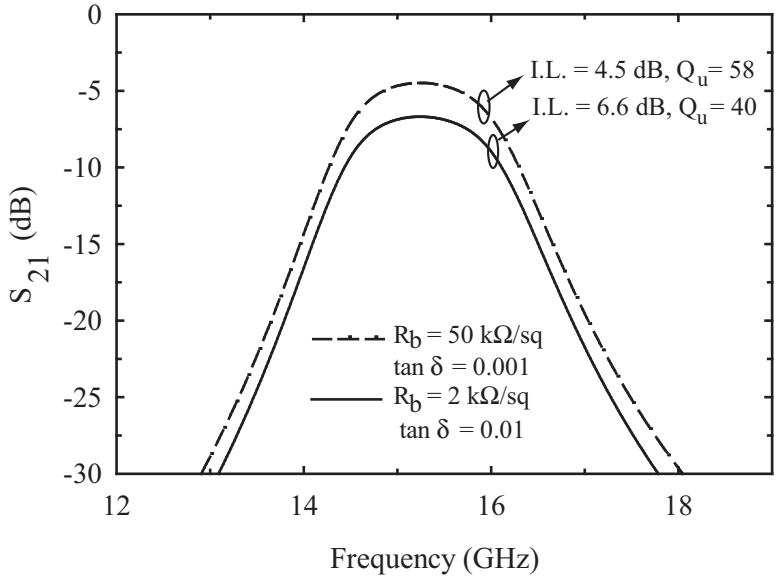


Figure 4.24: The simulated 15.2 GHz filter on glass and quartz substrates with 2 and 50 kΩ/sq bias line resistance respectively.

4.5 Improvements in the 12-18 GHz filter

In this section we discuss some solutions that improve the insertion loss and the quality factor of the 12-18 GHz tunable filter. As mentioned before, increasing the bias line resistance from 2 kΩ/sq to 20 or 50 kΩ/sq improves the filter loss and unloaded quality factor considerably. Using quartz instead of glass substrate also improves the loss (tan δ (quartz) = 0.001, tan δ (glass) = 0.01). As an example, the 3-pole filter with the center frequency of f_0 = 15.2 GHz (State 4) on a glass substrate with 2 kΩ/sq bias line resistance is re-simulated on a quartz substrate with 50 kΩ/sq bias line resistance. Fig. 4.24 compares the simulated insertion loss for two filters. The insertion loss of the filter is improved from 6.6 dB to 4.5 dB. It is seen that 1.5 dB of this improvement is due to increasing the bias line resistance and the other 0.6 dB is due to lower dielectric loss of the quartz substrate. The quality factor of the filter improves from 40 to 54 by changing the bias line resistance and to 58 by employing the quarts substrate.

As mentioned in chapter 3, employing capacitive cantilever RF MEMS switch with a thick electroplated beam instead of fixed beam capacitive switch can improve the filter loss and quality factor. The filter cab be re-designed on a suspended microstrip structure which has higher quality factor compared to the CPW transmission line to achieve better performance [67].

4.6 Conclusion

This chapter presents a state-of-the-art RF MEMS wide-band tunable filter designed for 12-18 GHz frequency range. The coplanar- waveguide filter, fabricated on a glass substrate using loaded resonators with RF MEMS capacitive switches, results in a tuning range of 40% with very fine resolution, and for the case of 3-pole filter, return loss better than 10 dB for the whole tuning range. Four different unit-cell pairs (MEMS capacitive switches in series with high-Q MAM capacitors) are used to load the coplanar waveguide resonators to reduce their effective length and make them tunable in a very wide range. The relative bandwidth of the filter is approximately fixed over the tuning range. The size of the 2 and 3-pole filters are 5 mm $\times$ 4 mm, and 8 mm $\times$ 4 mm respectively. For a 2-pole filter, the insertion loss is 4.2 and 6.8 dB at 18.0 and 12.5 GHz, respectively, for a 2 $\mathrm{k}\Omega/\mathrm{sq}$ bias line. For a 3-pole filter, the insertion loss is 5.5 and 8.2 dB at 17.8 and 12.2 GHz, respectively, for a 2 $\mathrm{k}\Omega/\mathrm{sq}$ bias line. The loss improves to 4.5 and 6.8 dB at 17.8 and 12.2 GHz, respectively if the bias line resistance is increased to 20 $\mathrm{k}\Omega/\mathrm{sq}$. The measured IIP_3 level is $>$37 dBm for $\Delta f >$ 200 kHz.

To our knowledge this is the widest-band planar tunable filter to-date. it is possible to achieve a better return loss, especially at lower frequencies, if the inductive inverters are made tunable. The measured results are very close to full-wave simulations. This work shows that RF MEMS tunable filters are excellent for wide-band designs and result in very low intermodulation levels.

CHAPTER 5

Wafer-Scale Microstrip Package for RF MEMS

5.1 Introduction

A variety of RF MEMS devices such as switches, varactors, and resonators have been demonstrated up to date [20]. While outstanding performance has been reported for RF MEMS devices, their functionality is very dependent to the environmental parameters such as humidity and and small particles [68]. Therefore; they must be encapsulated in a stable environment while they are integrated to a real-life system. Wafer-scale packaging is the only solution for a low cost, low loss hermetic package [69]. One of the big advantages of RF MEMS devices compared to their semiconductor counterparts is their low insertion loss. However, these low loss devices can only be as good as their packaging can allow. To

RF MEMS devices have been implemented on two different types of transmission lines: coplanar waveguide (CPW) and microstrip line. The work on RF MEMS packaging has been mostly focused on RF MEMS devices implemented on CPW transmission lines. The RF transition to the MEMS has been done either by passing the transmission line directly under the sealing ring or using hermetic via-holes. In the first transition, the characteristic impedance of the line under the sealing ring changes due to the loading effect of the ring. The dielectric layer [SiO_2 or benzocyclobutene (BCB)] isolates the sealing ring from the transmission line. Therefore, a specific matching network is required to improve the RF performance of the transition. [71][72][73]. To achieve long-term hermeticity and a planar transition with low step coverage, the line underneath the isolation layer should be thin ($< 1\ \mu$ m). This increases the insertion loss of the package due to skin effect at

higher frequencies. For the via-hole transition, the sealing ring width does not affect the transition and there is no need to use the isolation layer and the matching network, but hermetic via holes are needed inside the package [74][75].

There have been several attempts on wafer-scale CPW line packages using various bonding techniques. Margomenos et al. used gold thermo-compression bonding with 0.6 dB insertion loss of a hermetic via-hole transition up to 70 GHz [76]. At W-band Schobel et al and Min et al. used glass frit bonding and thermo-compression bonding with 0.25-0.5 dB and 0.19-0.26 dB insertion loss of a CPW feed-through respectively [77] [72]. Min et al. reported a DC-50 GHz gold thermo-compression bonding with 0.06-0.1 dB insertion loss [71] and a W-band CPW package with dB insertion loss [72]. Radant MEMS presented a DC-40 GHz packaged switch using glass flirt bonding [78]. Jourdain et al. reported 0.09-0.15 dB insertion loss at 2 GHz with a solder (SnPb) bonding [79].

This chapter presents some efforts to develop a wafer-scale package suitable for RF MEMS devices fabricated on microstrip lines. To achieve a low loss and well-matched package, the number of necessary interconnects to access the device should be minimum and the wire bonds are avoided due to their parasitic inductance [70]. The gold sealing ring around microstrip structures can generate considerable resonances in the pass-band and absorb the energy passing through the line at certain frequencies. To suppress the ring resonances, via-holes are used to connect the gold ring to the ground of the microstrip line. This technique suppresses the ring resonance modes as long as the via holes do not show considerable amount of inductance and act as an acceptable short circuit to the microstrip ground. Two different microstrip packaging structures are studied in this chapter: 1) the RF transition is implemented by passing the microstrip line directly underneath the sealing ring (Fig. 5.1. 2) hermetic via-holes are used as transitions. In this case and this results in a surface mount package, the measured results for the fabricated package is presented and compared to the simulation results.

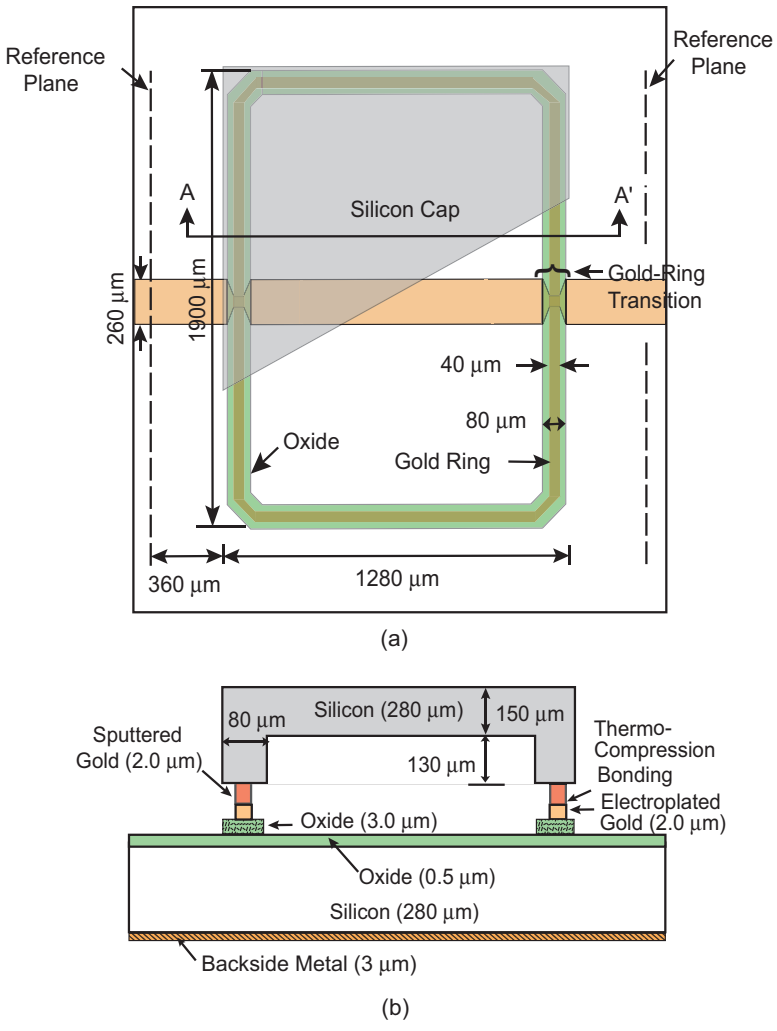


Figure 5.1: (a) Top view and (b) AA' cross section of a packaged microstrip line without via-holes (design 1).

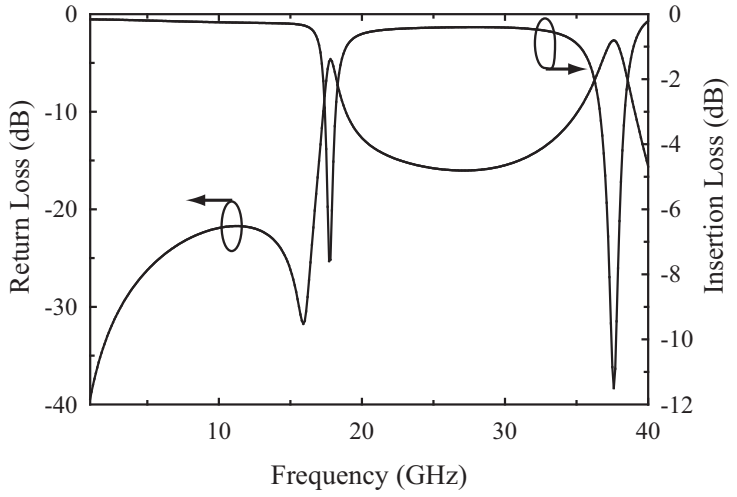
5.2 Microstrip Package: Design 1

5.2.1 Design and Simulation

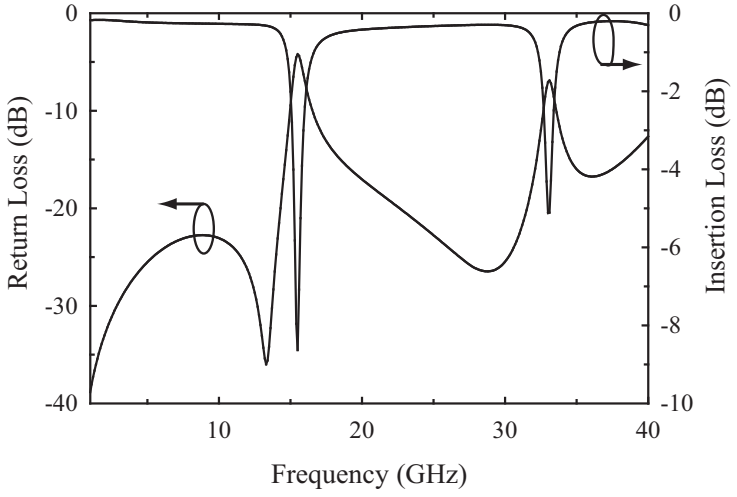
Fig. 5.1 shows two silicon wafers bounded together using gold-gold thermo-compression bonding to make a RF MEMS package. Both top and bottom wafers are 280 μm-thick, 1000 Ω-cm substrates to reduce the line loss. The 260 μm microstrip line on the bottom wafer is designed to provide a 50 Ω transmission line. To remove the impact of placing a silicon cap near the microstrip line or RF MEMS components inside the package, a 130 μm cavity is etched inside the top silicon wafer. Therefore, there is no need to redesign components inside the package. The gold ring over the isolation layer (3 μm of SiO_2) provides the bonding area and sealing for the hermetic package. Because of the loading effect of the sealing ring on top of the oxide layer, the characteristic impedance of the 260 μm microstrip line is not 50 Ω any more and the line is narrowed to 20 μm underneath the ring to compensate for the effect of the capacitive loading of the ring. The microstrip line is inductively tapered to provide good RF matching for the transition. The thickness of the microstrip line underneath the oxide layer is lowered from 3 μm to 0.5 μm to provide a planar sealing ring with minimum step coverage due to hermeticity. Lowering the thickness of the line increases the insertion loss the package.

Fig. 5.2(a),(b),(c) show the s-parameters simulation results for three different sealing ring dimensions: 880 $\times$ 1900 μm^2, 1280 $\times$ 1900 μm^2, 2040 $\times$ 1900 μm^2, from DC-40 GHz using Sonnet, respectively. The RF signal triggers the resonant frequency of the gold ring cavity. The depth of the resonance null in the insertion loss can reach to 9 dB (first resonance) which distorts the frequency response of the package. By increasing the dimension of the sealing ring the resonant frequency shifts down toward lower frequencies. Table 5.1 presents the resonant frequency of the sealing ring for three different package dimensions. Basically, the resonance happens where the circumference of the god-ring equals to integer multiples of guided wavelength.

A practical way to suppress the microstrip package resonance from the pass-band is using via-holes to connect the gold sealing ring to the ground on the back side of the bottom silicon wafer. Ideally, the best place for via-holes are under the ring and oxide layer, and the ring is connected to the via-holes (Fig. 5.3(a)). Due to the inductive effect of the via-hole, it does not provide a pure ground for the ring at higher frequencies, and this affects of the via-holes also affects the frequency



(a)



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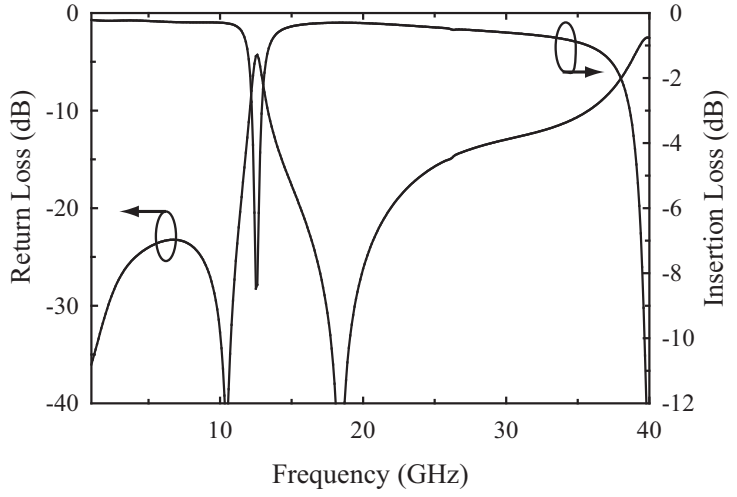


(c)

Figure 5.2: simulated I.L and R.L. of (a) 880 $\times$ 1900 μm^2 (b) 1280 $\times$ 1900 μm^2 (c) 2040 $\times$ 1900 μm^2 microstrip packages without via-holes.

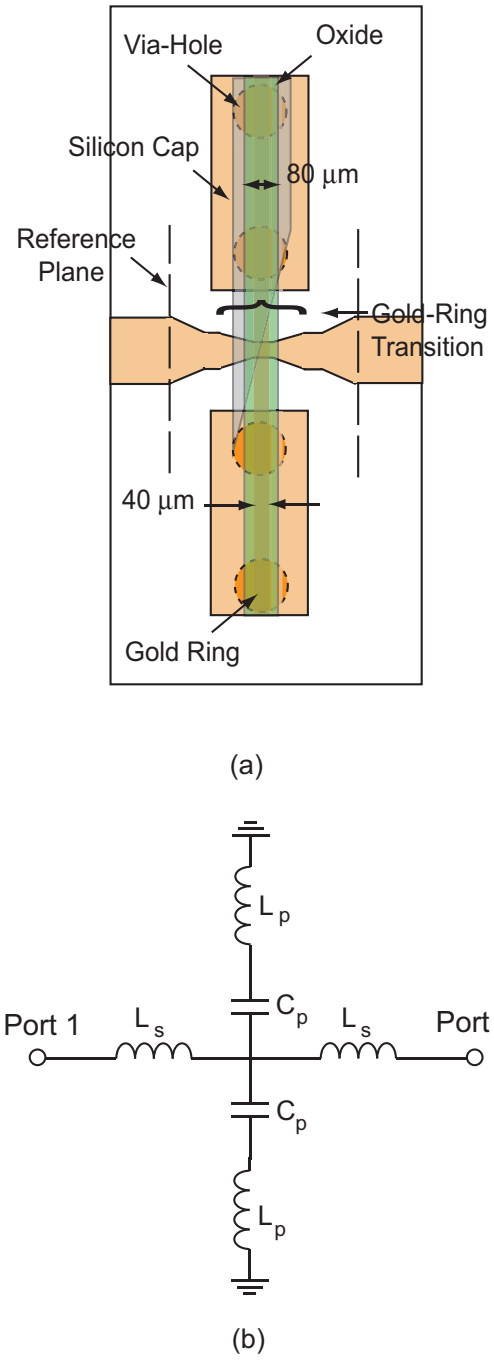


Figure 5.3: (a) Top view of the transition at the presence of the via-holes (b) the equivalent circuit of the transition.

Table 5.1: Gold ring resonance specifications for three different packaging dimensions.

Package	f_R (GHz)	$I.L.$ (dB)	$R.L.$ (dB)
$880 \times 1900 \mu\text{m}^2$	17.7	8.6	4.2
$1280 \times 1900 \mu\text{m}^2$	15.5	7.6	4.8
$2040 \times 1600 \mu\text{m}^2$	12.5	8.5	4.4

response of the transition. Fig. 5.3(a) shows the top view of the microstrip transition through the package at the presence of the via-holes, and Fig 5.3(b) shows the equivalent circuit of the transition. C_p is the capacitor between the ring and the first metal layer, L_P is the via-hole inductance, and L_s is the inductance of the tapered microstrip line under the ring and in the air. The via-hole inductance introduces unacceptable mismatch in the response of the transition. One way to achieve a better match at DC-40 GHz frequency range is to reduce L_P by placing the via holes as close as possible to the microstrip line and adjusting the series inductor (L_s) by appropriate tapering of the microstrip line passing underneath the ring (Fig. 5.3(a)). Fig. 5.8 shows the insertion loss and the return loss of the transition at the presence of the via-holes. The transition behavior is similar to a low-pass filter and is well-matched up to 30 GHz (R.L better than 20 dB)with an I.L better than 0.15 dB up to 30 GHz. For frequencies above 30 GHz, the inductive effect of via-holes start to become dominant. By using a thinner substrate, the via-hole inductance would be improved and it is possible to achieve transitions with wider pass-bands.

Increasing the diameter of the via-hole can also reduce the via-hole inductance, but not as much as reducing the thickness of the substrate. Fig. 5.5 shows the impedance of a via-hole on silicon substrate for different thicknesses (h = 280,180,80 μm) and different via-hole diameters (d = 4,6,8 mils) for DC-40 GHz. Fig. 5.6 shows the inductance of a via-hole on silicon substrate for different thicknesses (h = 280,180,80 μm) and different via-hole diameters (d = 4,6,8 mils) at 30 GHz.

Fig. 5.7 shows a packaged microstrip line with the modified transitions and via-holes which connect the ring to the ground. The via-hole diameter is considered 4 mils for the simulation purposes. Fig. 5.8(a),(b),(c) present the simulation results for insertion loss and return loss of 880×1900 μm^2, 1280×1900 μm^2, and 2040×1900 μm^2 respectively using Sonnet. As can be seen, the resonances are totally suppressed for all three packages and the simulated insertion loss

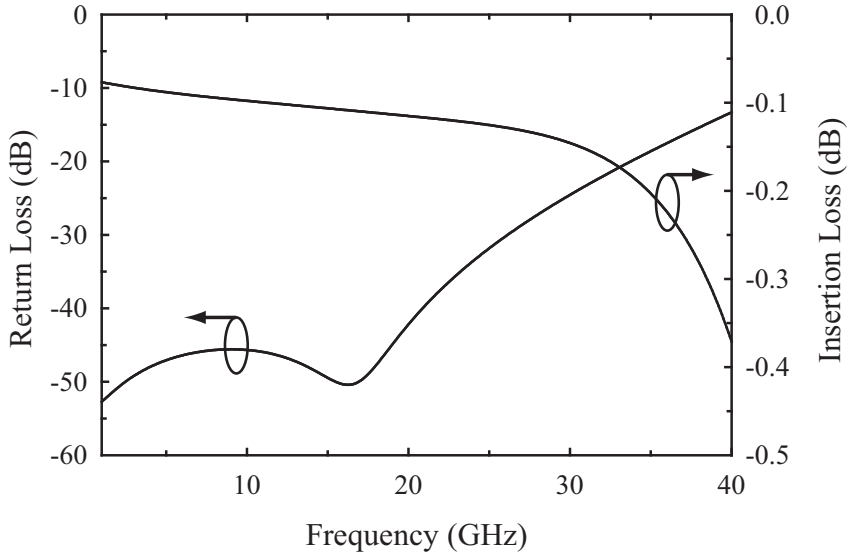


Figure 5.4: I.L and R.L. of the microstrip transition in the presence of the via-holes (280 μm-high silicon substrate).

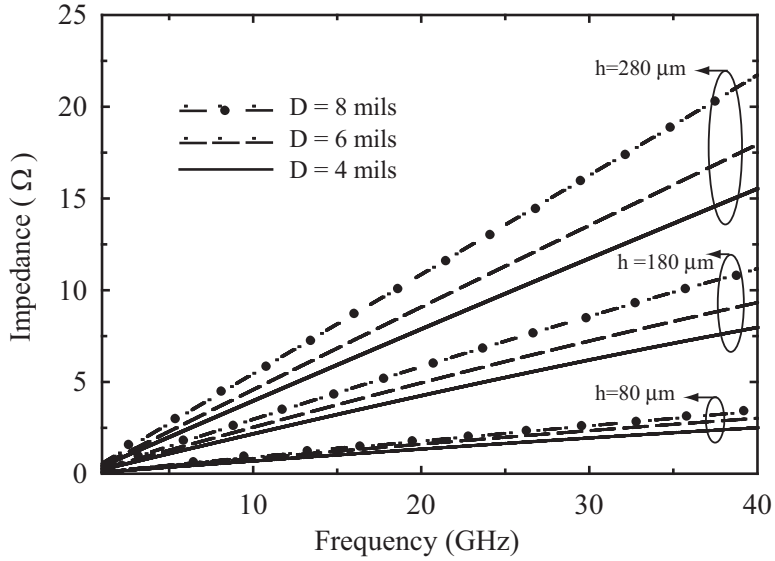


Figure 5.5: Via-hole impedance for 4,6,8 mils via-hole diameters and 280,180,80 μm-thick silicon substrates for DC-40 GHz.

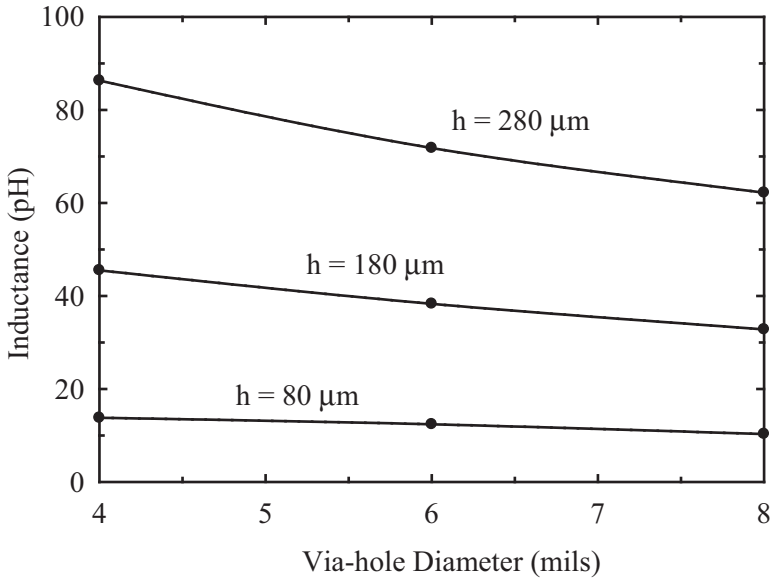


Figure 5.6: Via-hole inductance for 4,6,8 mils via-hole diameters and 280,180,80 μm thick silicon substrates at 30 GHz.

and return loss are better than 3 dB and 20 dB up to 30 GHz for all three cases.

5.3 Microstrip Package: Design 2

This chapter presents a microstrip-based surface-mount package with very low loss up to K-band frequencies with hermetic via-hole transitions. It is shown again that the grounding of the metal sealing ring using via-holes all around the ring removes any parasitic resonance in the package. Also, the grounding increases the isolation between the input and output ports in case of a series switch (open-state position).

5.3.1 Design

The K-band package is composed of a 280 μm-thick silicon cap-wafer which is bonded to a 250 μm-thick alumina wafer using gold-to-gold thermo-compression bonding (Fig. 5.9). An alumina wafer was used since we did not have a hermetic via-hole process on 250 μm thick silicon wafers. Also, its dielectric constant is close to silicon, and this makes it a good demonstrator for a silicon-to-silicon package. A 240 μm-wide microstrip line is used on top of the alumina wafer to achieve a 50 Ω transmission line. A high-resistivity silicon wafer (1000 Ω-cm) is used for the

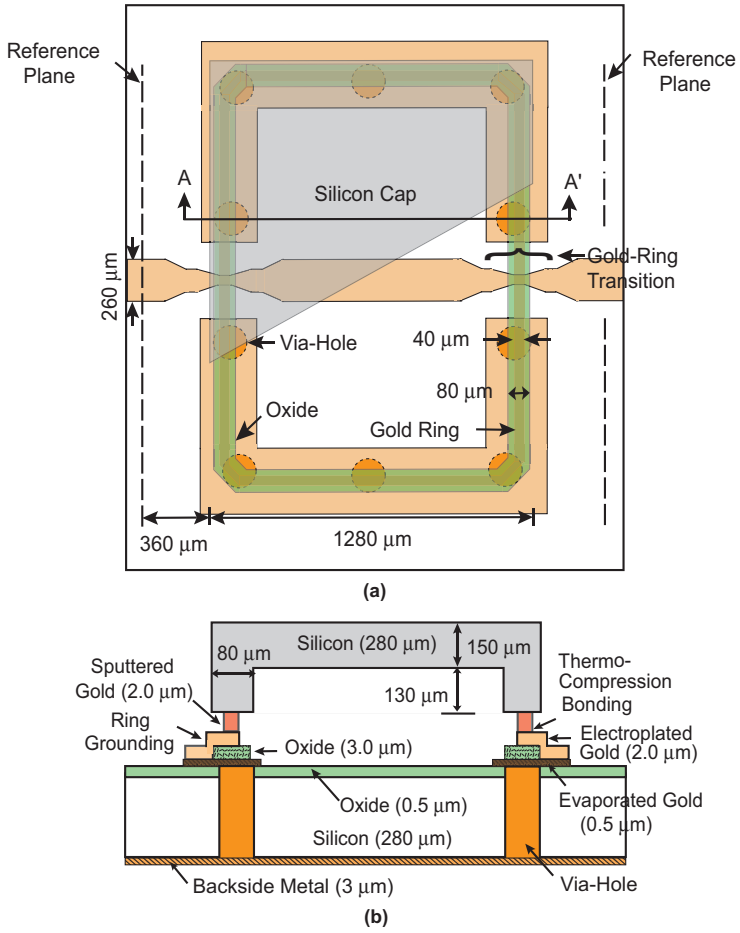


Figure 5.7: (a) Top view and (b) AA' cross section of the packaged microstrip line with via-holes (design 1).

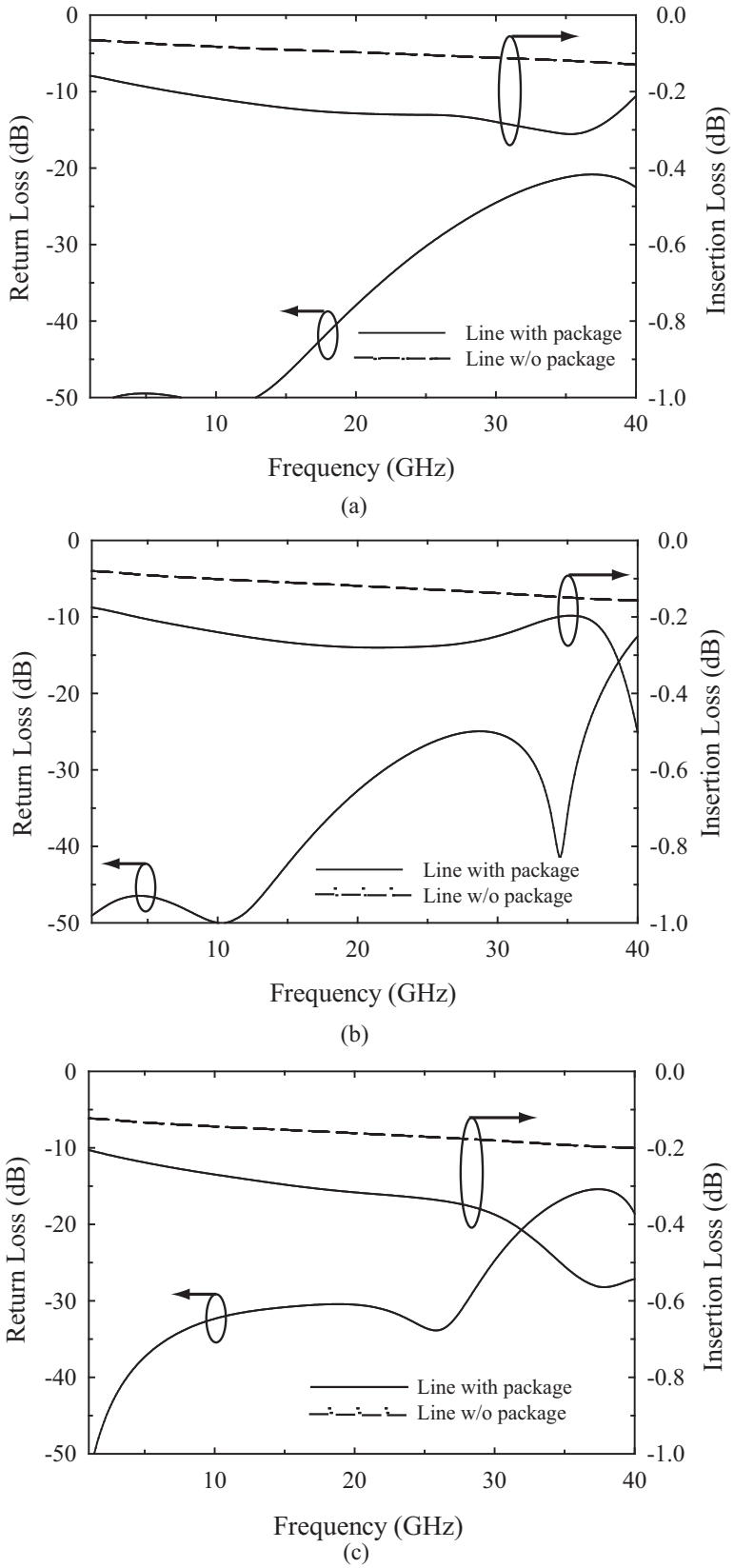


Figure 5.8: I.L and R.L. of (a) 880 $\times$ 1900 μm^2, (b) 1280 $\times$ 1900 μm^2, and (c) 2040 $\times$ 1900 μm^2 microstrip packages with via-holes.

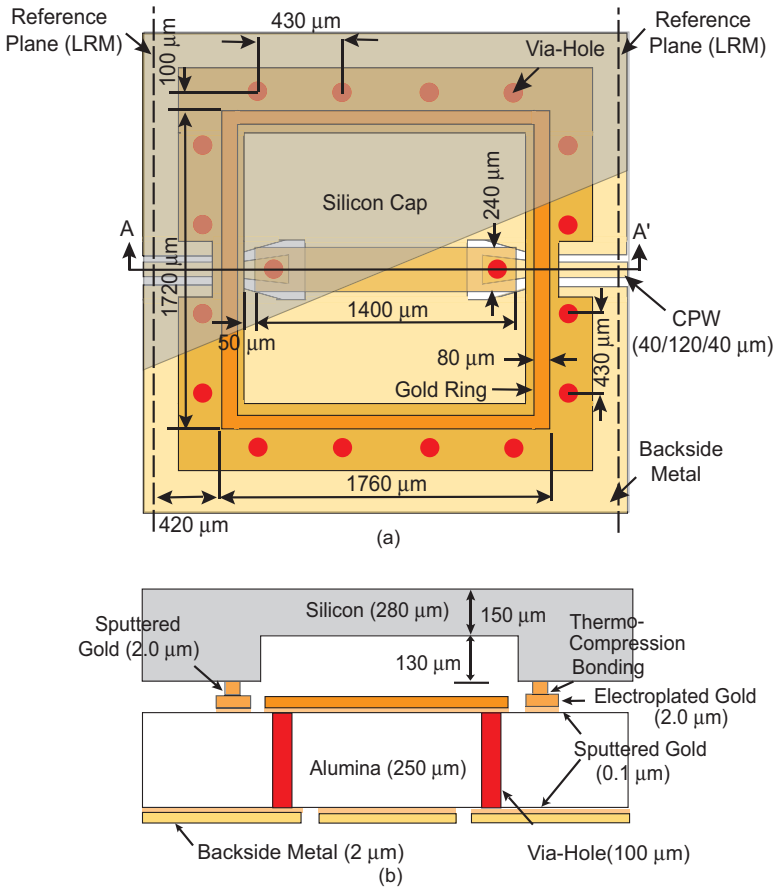


Figure 5.9: (a) Top view and (b) AA' cross section of the packaged microstrip line with via-holes (design-2).

cap wafer and a 130 μm cavity is etched in the cap wafer to remove the impact of placing a silicon wafer in the near proximity of the microstrip lines or RF components. An 80 μm gold ring provides sealing for the hermetic package [80].

The 50 Ω microstrip line on top of the alumina wafer under the etched silicon cap is connected to a CPW line on the back side of the alumina wafer using hermetic via-holes with 100 μm diameter. The 40/120/40 μm CPW line is also a 50 Ω line, and the CPW line dimension is chosen to be less than $\lambda_d/10$ at 26 GHz to ensure single mode operation. The design is optimized using Sonnet and the final dimensions are given in Fig. 5.9. The gold sealing ring is connected to the ground plane on the back side of the alumina wafer using a set of via-holes (Fig. 5.9). Without grounding, one can clearly measure package resonance modes at frequencies where the package circumference equals to multiples of wavelengths. The gold ring grounding also results in very low RF leakage between

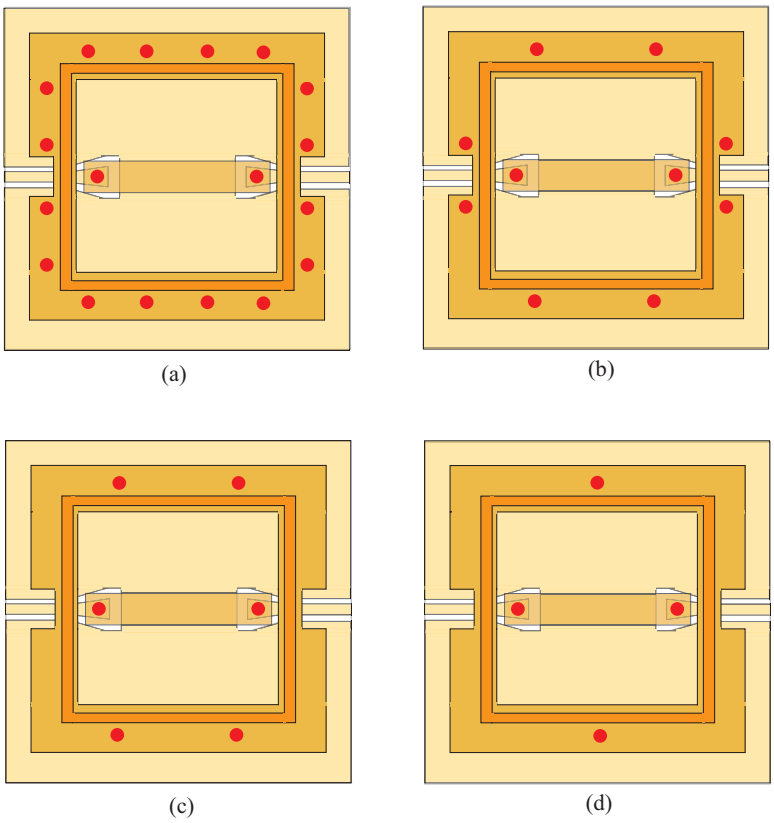


Figure 5.10: Four different grounding via-hole configurations for the microstrip package.

the input and output port transitions in case of a series switch in the up-state position (open). This grounding technique achieves good performance up to around 26 GHz for a 250 μm thick wafer due to the inductance of the via-holes (simulated with Sonnet). If a higher frequency is desired, then the alumina wafer must be reduced to 150 μm or even 50 μm for W-band operation. The package is also simulated in Sonnet with half of the grounding via-holes around the gold ring (Fig. 5.10(b)). The simulations show that reducing the number of via-holes by half (separation of 860 μm instead of 430 μm) does not affect the package response considerably and the S_{21} bandwidth reduces by around 1 GHz (Fig. 5.11(a)). Further reduction of the number of grounding via-holes, especially removing the via-holes close to the microstrip line (Fig. 5.10(c)), increases the inductance between the gold ring and the microstrip ground and introduces sharp resonance modes in the simulated S-parameters (Fig. 5.11(b)). Fig. 5.10(d) presents a specific case with two grounding via holes and the simulated insertion loss for this case is shown in Fig. 5.11(b).

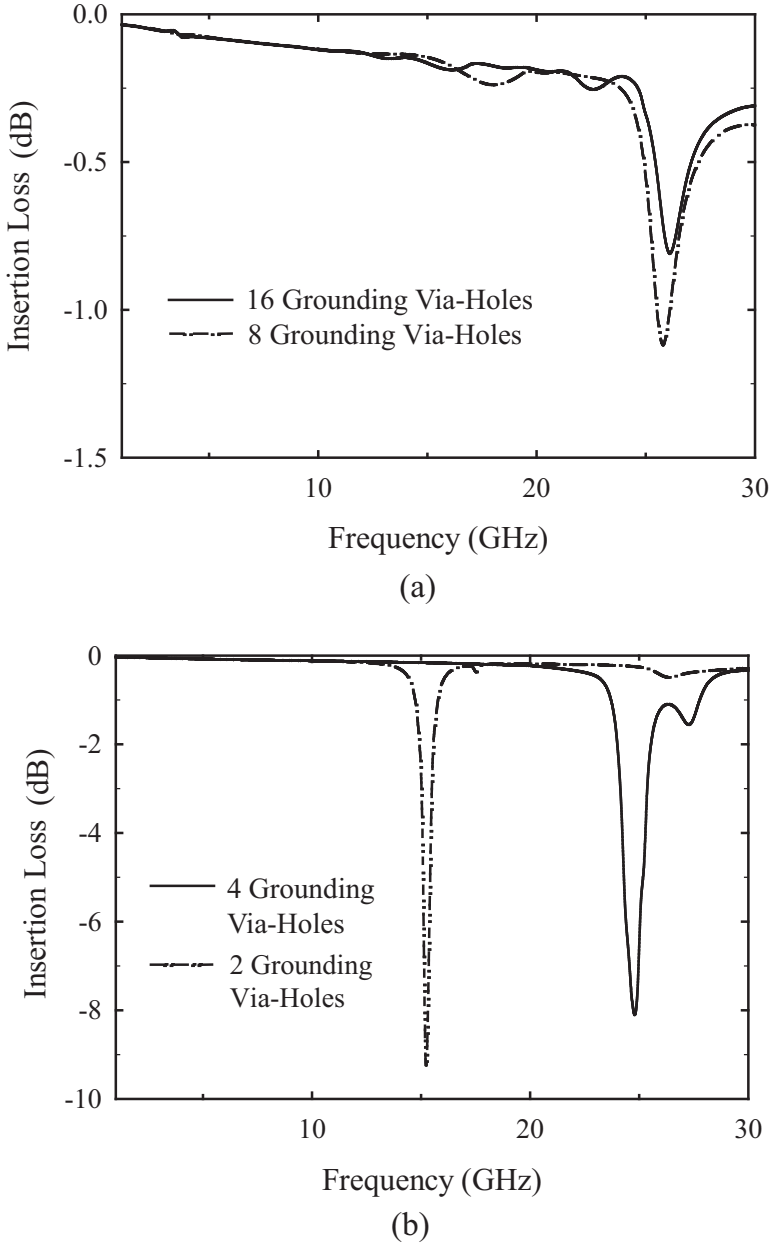


Figure 5.11: Simulated S-parameters for 4 different grounding configurations of the microstrip package (Fig. 5.10).

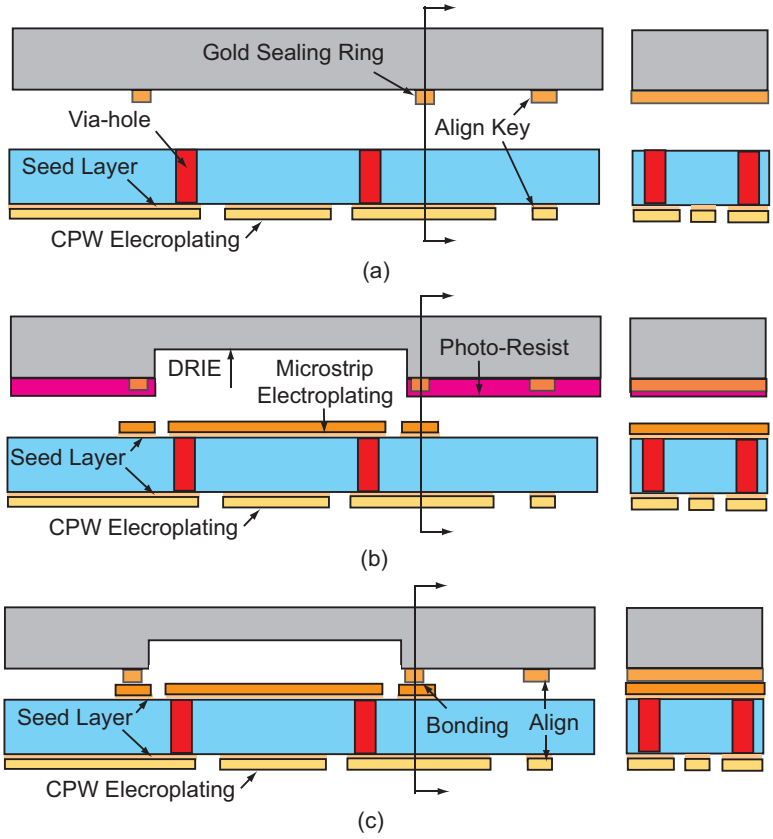


Figure 5.12: Fabrication flow (a)-(c) for the microstrip package; Design no. 2.

5.3.2 Fabrication

The first step is the fabrication of the transition and the grounding via-holes, all with 100 μm diameter on a bare alumina wafer. These are fabricated by Micro-substrates Company [81] using standard ceramic fabrication (laser etching, electroplating). Next, a 200/1000/200 Å Ti/Au/Ti seed layer is sputtered on the back side of the alumina substrate and the CPW line is electroplated to 2 μm (Fig. 5.12(a)). Another 200/1000/200 Å Ti/Au/Ti seed layer is sputtered on the top of the alumina wafer. The microstrip line and the bottom part of the sealing ring are electroplated to 2 μm (Fig. 5.12(b)). On a separate 280 μm cap wafer, a 200 Å / 2 μm Ti/Au layer is sputtered first, and the top part of the sealing ring and bonding alignment marks are patterned with wet etching (Fig. 5.12(a)). Then, a 10 μm photo resist mask is patterned to provide a DRIE mask to etch the 130 μm-high package cavity inside the silicon substrate (Fig. 5.12(b)). The final step of fabrication is the gold-to-gold thermo-compression bonding of silicon and alumina wafers (Fig. 5.12(c)). The wafers are heated up to 320°C and a pressure of 7 MPa is applied for an hour using EV 501 [82]

bonder. This thermo-compression bonding technique is proven to result in high-reliability hermetic sealing [74], [80]. Fig. 5.13 shows the completed package, together with the front and back side of the alumina wafer.

5.3.3 Simulation and Measurement

The measured and simulated S-parameters of a 2.6 mm long packaged microstrip line with and without the grounding via-holes are presented in Fig. 5.14(a) and 5.14(b), respectively. The results clearly demonstrate the effect of the gold-ring grounding: without grounding, a resonance frequency appears around 16.2 GHz where the circumference of the gold-ring equals to one guided wavelength ($\lambda_g = \lambda_0 / \sqrt{\epsilon_{eff}} = 7$ mm), but this parasitic resonance disappears completely with grounding. Also, due to inductive behavior of the via-holes at higher frequencies, the insertion loss drops and the mismatch increases for frequencies greater than 23 GHz.

Fig. 5.15 presents the input/output isolation of a packaged microstrip line with a 60 μm-long gap in the microstrip line. This simulates a series RF MEMS switch in the up-state position. Again, one can clearly see the resonance mode around 16 GHz, and the isolation improves by 13 dB at 16.2 GHz with the gold-ring grounding.

5.4 Conclusion

Two different approaches for microstrip package design are investigated in this chapter. The first approach demonstrates the design and simulation of package with microstrip feed-through transition. The simulation of a packaged microstrip line resulted in an insertion loss better than 0.3 dB and return loss better than 20 dB at DC-30 GHz. The second approach demonstrates the design and fabrication of a microstrip wafer-scale package with via-hole transition for K-band applications and a measurement of a packaged microstrip line resulted in an insertion loss better than 0.5 dB and a return loss better than 18 dB at DC-23 GHz.

For both approaches, The gold-gold sealing ring results in unwanted resonance modes and the gold-ring grounding using via-holes through the bottom wafer removes all resonances. To improve the package bandwidth, a thinner bottom substrate with shorter via-holes should be employed. The depth of the resonance in the insertion loss response for the first package is around 8 dB and for the

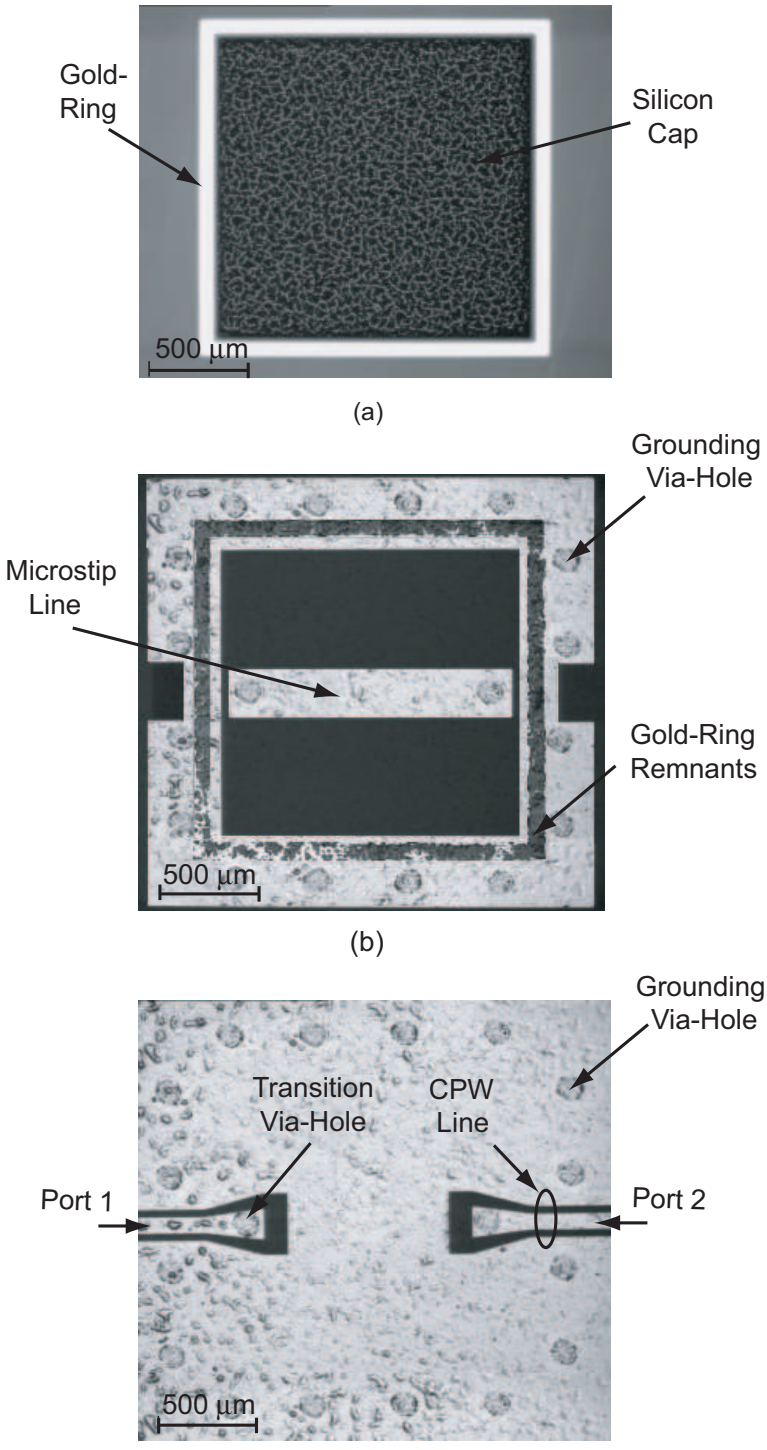


Figure 5.13: Photograph of the (a) silicon-wafer before bonding (b) front-side of the alumina wafer after the cap is removed over the whole package, and (c) the back-side of the alumina wafer .

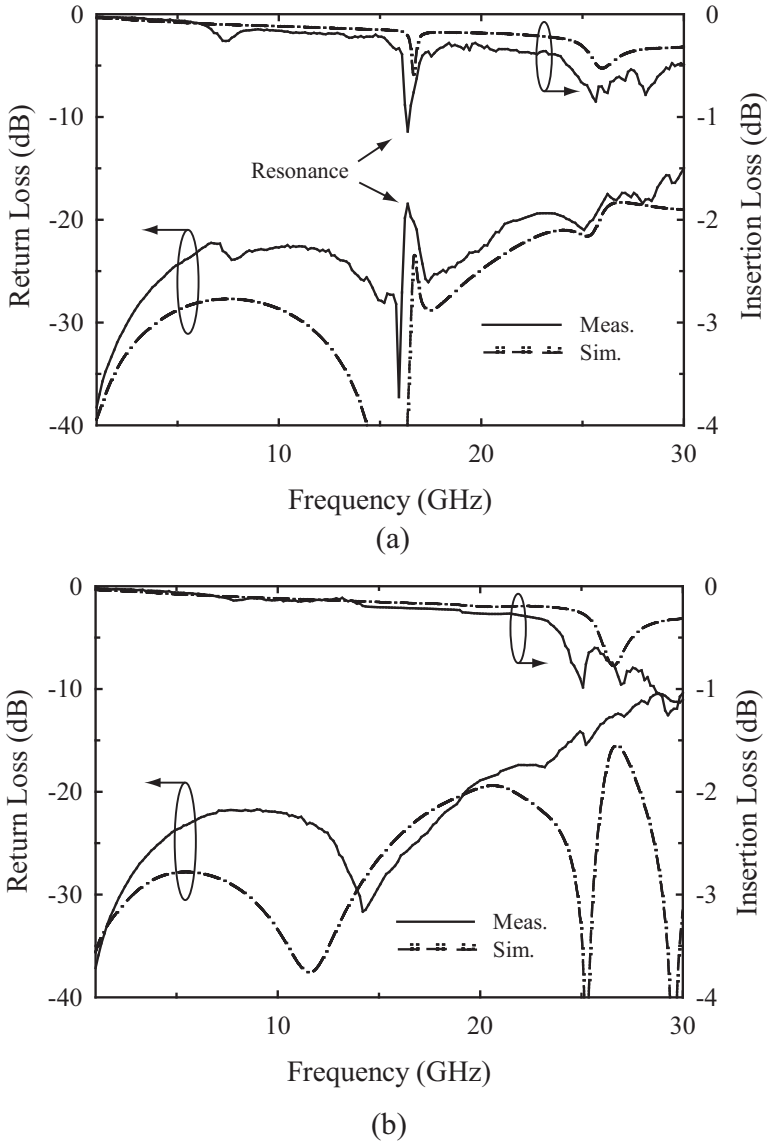


Figure 5.14: Measured and simulated insertion loss and return loss of a microstrip package with (a) and without (b) grounding via-holes.

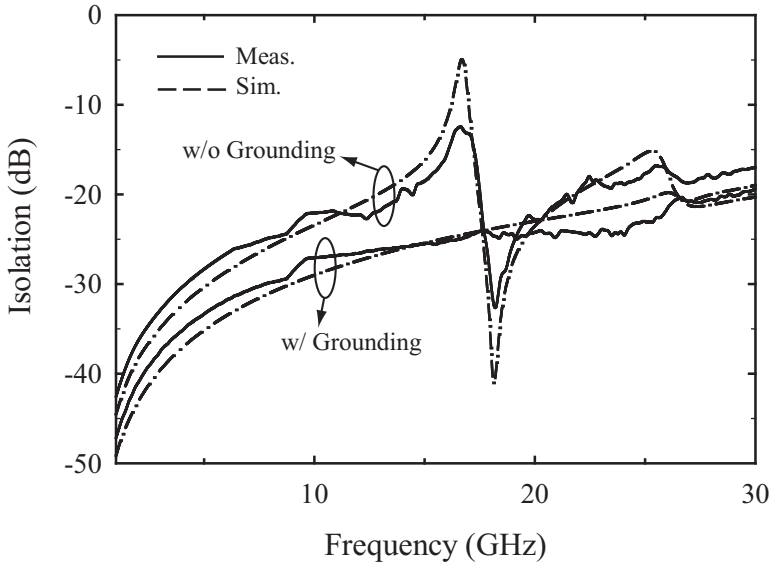


Figure 5.15: Measured and simulated (Sonnet) isolation of a microstrip package with and without grounding via-holes.

second one is around 1 dB. The reason is that the microstrip transition passes exactly underneath the sealing ring in package no. 1 and the RF signal strongly couples to the sealing ring, while in package no. 2 the transition does not pass underneath the ring and the RF signal couples to the gold-ring through the microstrip line and alumina substrate which is much weaker than package no.1. The advantage of the design no. 2 compared to the design no. 1 is the simplicity of the fabrication; there is no need to have a dielectric layer between the sealing ring and the transition. On the other hand, the via-hole transition need to be hermetic in design no. 2.

CHAPTER 6

RF MEMS System-Level Response in Complex Modulation Systems

6.1 Introduction

One of the important applications of RF MEMS devices is in reconfigurable networks as variable capacitors [20]. As mentioned in chapter 1, the advantage of RF MEMS varactors compared to their GaAs and BST counterparts is their excellent linearity. From a system-level point of view, linearity is a major issue in wireless communication system front ends especially those which use specific types of modulation techniques such as GSM and WCDMA [32]. Fig. 6.1 explains that the presence of two tones at the input of a nonlinear circuit with odd nonlinearity terms generates third-order intermodulation tones. As a consequence, by changing the input of the circuit to a modulated signal, the spectrum at the output of the circuit experiences spectral regrowth at the adjacent channel, which is not desirable because of the channel interference phenomenon [32]. A good example of a linear circuit is a RF power amplifier with a reconfigurable matching network at the final stage of a WCDMA transmitter connected to the antenna. The modulation technique used in WCDMA systems is based on digital phase modulation. Abrupt phase transitions in the modulated signal appear in practice as amplitude modulation [32]. As a result, the modulated signal is very sensitive to circuit nonlinearities, especially at the RF power amplifier section. It is therefore critical to design these types of reconfigurable circuits as linear as possible to avoid the adjacent channel interference.

In this chapter, two different multi-functional circuits, a tunable matching network and a tunable filter, are designed using GaAs, BST and RF MEMS varactors for a WCDMA front end centered at 1.95 GHz to investigate and compare their response to a WCDMA signal.

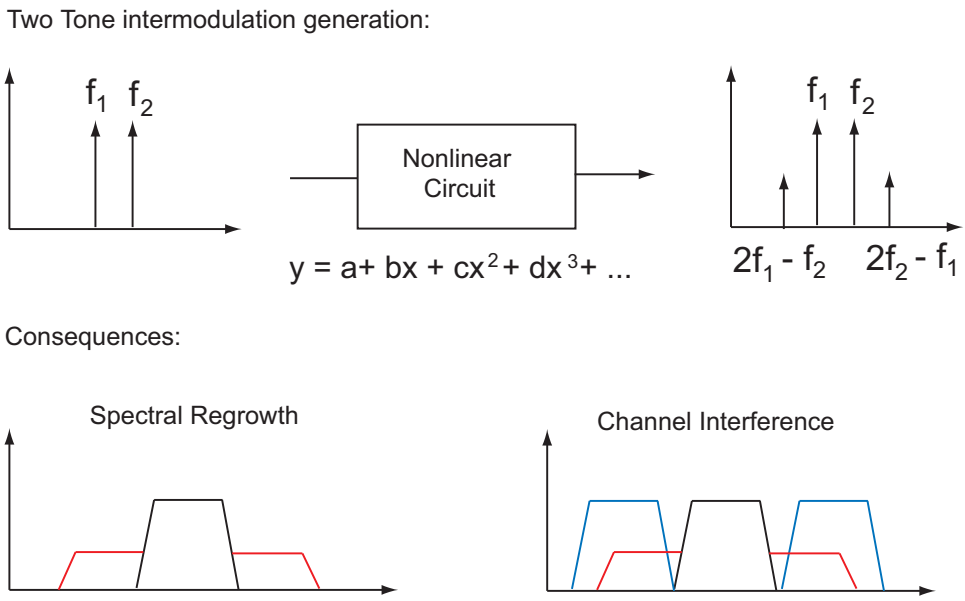


Figure 6.1: The effect of circuit nonlinearity on the spectral regrowth and adjacent channel interference of a WCDMA signal.

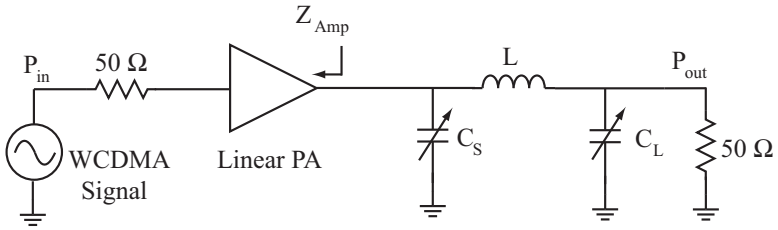


Figure 6.2: The schematic of a WCDMA transmitter front end including a linear power amplifier and a tunable matching network.

6.2 Impedance tuner in WCDMA transceivers

6.2.1 General matching network topology

Fig. 6.2 presents the schematic of a power amplifier with a reconfigurabl matching network. The power amplifier is assumed an ideal linear amplifier with 20 dB of gain and with an input impedance of 50 Ω. The output impedance, Z_{Amp}, and the load (antenna) impedance, Z_{Load}, are assumed 4 and 50 Ω in the ideal case, respectively. To match the 4 Ω to the 50 Ω impedance, a $C_S - L - C_L$ π-network is used (C_S = C_L = 5.7 pF, L = 1.15 nH). In practice, Z_{Amp} and Z_{Load} are variable impedances, so a tunable matching network is necessary to match Z_{Amp} and Z_{Load} for different impedance values. The impedance tuner is designed for two different cases:

1) Z_{Load} = 50 Ω, and Z_{Amp} varies between 2 ± 4j and 6 ± 4j.

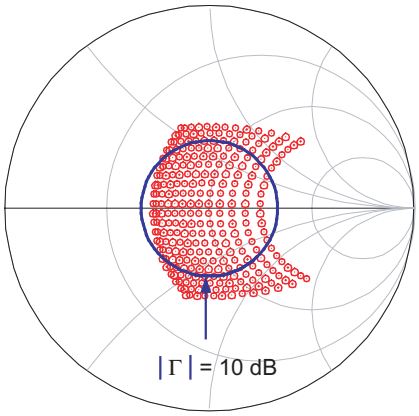
Fig. 6.3(a) shows the power amplifier output impedance locations between 2 ± 4j and 6 ± 4j, seen at the load for C_S = C_L = 5.7 pF, and L = 1.15 nH. All the impedance loci inside the Γ = 10 dB circle are matched to the load with a return loss better than 10 dB, but some of the impedance loci are outside this circle. To extend the matching range, the capacitors C_L and C_S are changed while the series inductor is fixed. Fig. 6.3(b), (c) show the Z_{Amp} impedance loci seen at the load for C_S = C_L = 5.2 pF and C_S = C_L = 6.4 pF, respectively. By changing the shunt capacitors from 5.2 to 6.4 pF, Z_{Amp} is matched to Z_{Load} = 50 Ω while it varies between 2 ± 4j and 6 ± 4j.

2) Z_{Amp} = 4 Ω, and Z_{Load} varies between 25 ± 40j and 85 ± 40j.

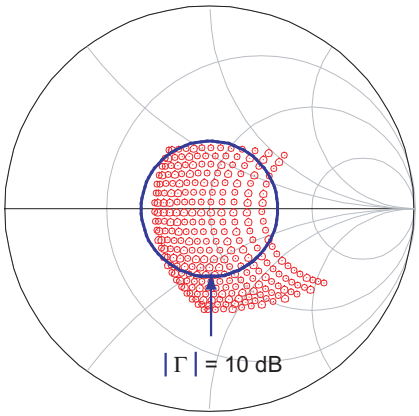
Fig. 6.4(a) shows the different load impedance locations between 25 ± 40j and 85 ± 40j, seen at the output of the power amplifier for C_S = C_L = 5.7 pF, and L = 1.15 nH. Again, all the impedance loci inside the Γ = 10 dB circle are matched to Z_{Amp} with a return loss better than 10 dB, but some of the impedance loci are outside this circle. By changing the capacitors C_L and C_S to 5.2 pF (Fig. 6.4(b)) and 6.4 pF (Fig. 6.4(c)), the matching range is extended.

6.2.2 GaAs, BST, and RF MEMS impedance tuners

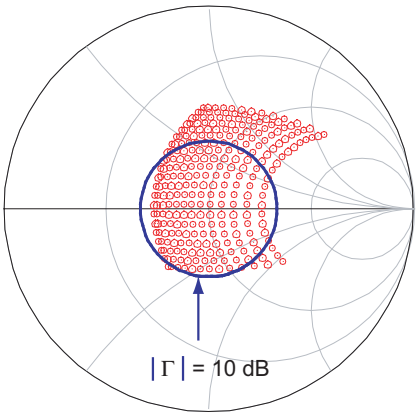
To investigate the effect of the impedance tuner nonlinearity on the WCDMA signal, we consider the case where C_S = C_L = 5.7 pF and substitude the C_S and C_L with three different types of varactors. Fig. 6.5(a) shows the C-V curve for a reversed-biased GaAs varactor. The varactor provides a capacitor ratio of 4 and is biased at 6 V (C_{var} = 1.8 pF) in the matching network to achieve the maximum voltage swing and linearity. Fig. 6.5(b) shows the C-V curve for a ferroelectric or BST varactor [31]. Despite the GaAs, the BST varactor has a symmetric C-V curve and acts as a variable capacitor for both positive and negative voltages across the varactor. It provides a capacitive ratio of 2.4 and is also biased at 6 V (C_{var} = 2.3 pF) to achieve the maximum swing. Fig. 6.5(c) shows the C-V curve for a RF MEMS switch. The switch stays in the up-state position for the bias voltage between -18 to 18 V and the switch capacitance varies from 115 to 150 fF with the bias voltage (capacitive ratio = 1.3). The switch is pulled down for the bias voltages above 18 V or below -18 V, and the switch down-state capacitance is around 3.5 pF. The RF MEMS switches are biased in the up or down state positions in the matching network. The up-state switches are biased at



(a)

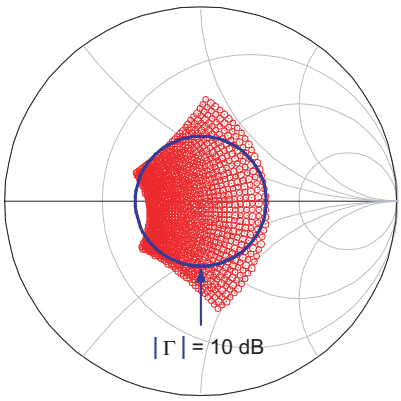


(b)

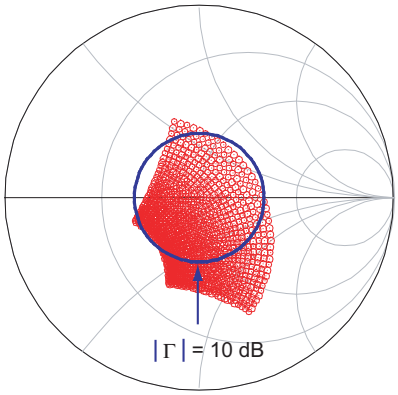


(c)

Figure 6.3: Z_{Amp} impedance loci at the load for (a) C_S = C_L = 5.7 pF (b) C_S = C_L = 5.2 pF (c) C_S = C_L = 6.4 pF. L = 1.15 nH for all cases. The smith chart is 50 Ω.



(a)



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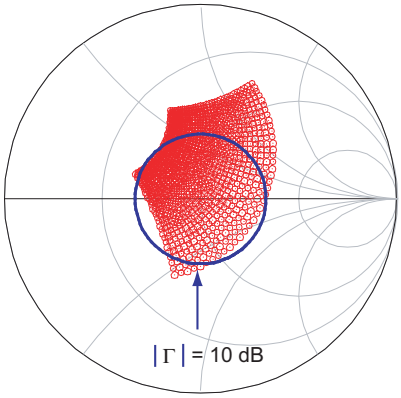


(c)

Figure 6.4: Z_{Load} impedance loci at the output of the power amplifier for (a) C_S = C_L = 5.7 pF (b) C_S = C_L = 5.2 pF (c) C_S = C_L = 6.4 pF. $L = 1.15$ nH for all cases. The smith chart is 4 Ω

Table 6.1: Voltage swing across the varactors at nodes (a) and (b) in Fig. 6.6 for different output powers.

Varactor	V_a(peak)	V_b(peak)
GaAs		
$P_{out} = 10$ dBm	0.3 V	1 V
$P_{out} = 20$ dBm	0.9 V	3.2 V
$P_{out} = 30$ dBm	3.6 V	Compressed (-1.3 V to 14.4 V)
BST		
$P_{out} = 10$ dBm	0.3 V	1 V
$P_{out} = 20$ dBm	0.9 V	3.2 V
$P_{out} = 30$ dBm	2.6 V	Distorted (-3.3 V to 16.7 V)
RF MEMS		
$P_{out} = 10$ dBm	0.3 V	1 V
$P_{out} = 20$ dBm	0.9 V	3.2 V
$P_{out} = 30$ dBm	2.7 V	9.3 V

zero volt to provide the maximum voltage swing and to avoid self-biasing effect. Figures 6.6(a),(b) present the implemented impedance tuner using GaAs, BST varactors, respectively. By changing the biasing voltage of GaAs or BST varactors, the capacitors C_S and C_L vary between 5.2-6.4 pF. Fig. 6.6(c) shows the RF MEMS impedance tuner. Each varactor (C_S, C_L) is implemented as a 2-bit switched capacitor. Each switched capacitor is a series combination of the RF MEMS switch and a fixed 4.2 pF capacitor. When both switches are in the up-state, C_S = C_L = 5.2 pF. By pulling down one of the switches C_L and C_S values change to 5.7 pF (Fig. 6.6(c)). When both switches are in the down state then C_L and C_S values change to 6.4 pF.

As the first simulation step, a single-tone source with different power levels is used in Fig. 6.2 at 1.95 GHz. The circuit is simulated in ADS using harmonic balance nonlinear technique for different impedance tuners. Table 6.1 shows the voltage swing across GaAs, BST and RF MEMS varactors (points (a) and (b) in Fig. 6.6) for different output power levels. The voltage at node (b) is always larger than the voltage at node (a) because node (b) is a higher impedance node, as a result varactors

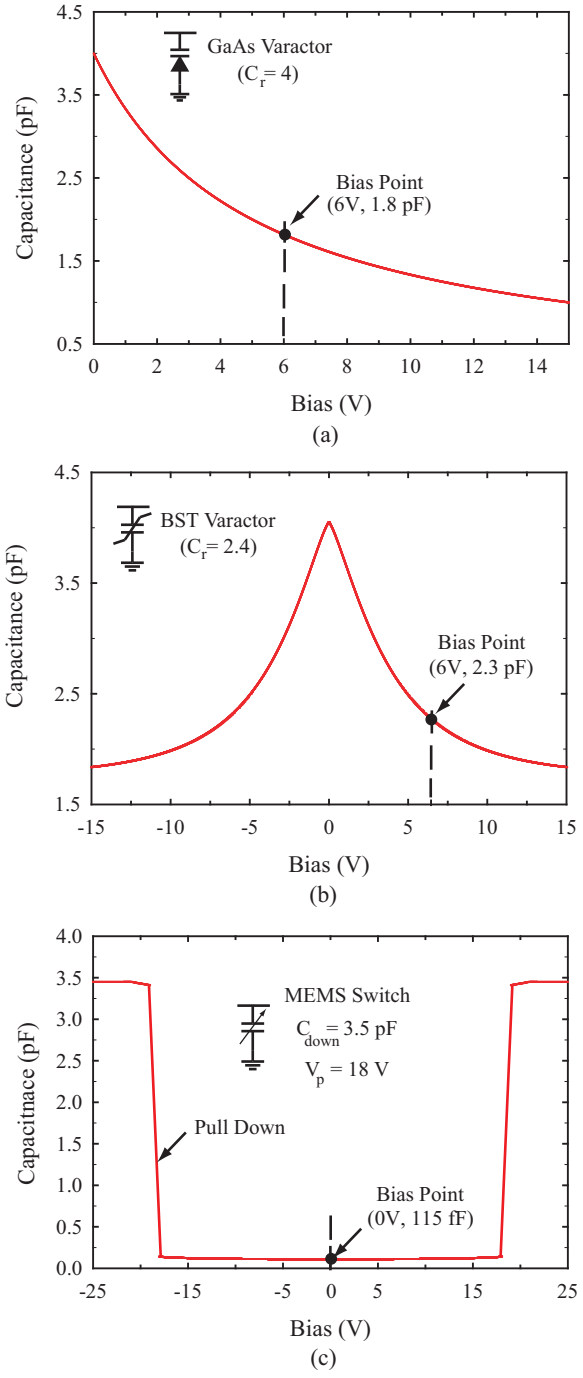


Figure 6.5: Capacitance vs. biasing voltage for a (a) GaAs (b) BST (c) RF MEMS varactor.

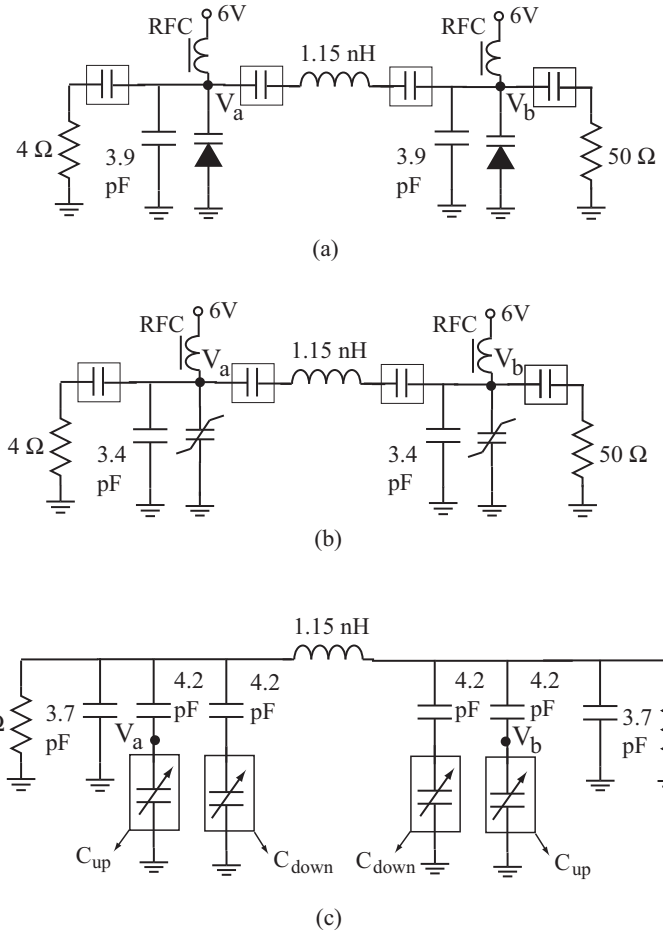


Figure 6.6: (a) GaAs (b) BST (c) RF MEMS tunable matching networks.

connected to node (b) are more strongly pushed to the nonlinear region. For P_{out} =30 dBm, the voltage across the GaAs varactor at node (b) is compressed. Due to the high voltage swing across the varactor, it goes to the ohmic region and clips the voltage. The voltage across the BST varactor at node (b) is distorted for P_{out} = 30 dBm. The signal experiences a huge nonlinearity due to nonlinear C-V curve of the BST varactor. The voltage across the RF MEMS capacitive switch at node (b) reaches to 9.3 V. This voltage is still smaller than the pull-down voltage of the switch, so the switch stays in the up-state position, self-biasing does not occur and the voltage is not distorted.

To see the nonlinear effect of the impedance tuners on the WCDMA signal, we substitute the single-tone source with a WCDMA source at 1.95 GHz with a chip rate of 3.84 Mcps. The circuit is simulated in ADS using envelope simulation technique and the WCDMA spectrum is extracted at the output of the matching network. Fig. 6.7 shows the simulated WCDMA spectrum at the output of GaAs, BST and RF MEMS tuners for P_{out} = 10, 20, and 30 dBm. For P_{out} = 10 dBm , all three tuners are in the linear region so the spectral regrowth at the adjacent channel is negligible for all tuners. By increasing the output power level to 20 dBm, the GaAs and BST tuners are pushed to their nonlinear region while the RF MEMS tuner stays in the linear region. The WCDMA output spectrum for GaAs and BST tuners shows a spectral regrowth of more the 20 dB compared to their MEMS counterpart at the adjacent channel. For P_{out} = 30 dBm, the GaAs varactor connected to node (b) enters to ohmic region. Both the GaAs and BST tuners show extremely nonlinear behavior while the RF MEMS tuner still stays in the linear region. The GaAs and BST tuners show 50 dB and 30 dB spectral regrowth at the adjacent channel compared to the RF MEMS tuner, respectively.

To improve the linearity of the BST impedance tuner, each BST varactor is substituted by an array of similar varactors all biased at 6 V. Figures 6.8(a),(b),(c) show BST impedance tuners with 2×2, 3×3 and 4×4 BST array varactors and Fig. 6.9 presents an impedance tuner with 3×1 array. The equivalent capacitor of each array is 5.2 pF when the varactors are all biased at 6 V. By increasing the number of varactors, the voltage swing across each varactor decreases for the same level of input power compared to a single varactor tuner and the impedance tuner shows more linear behavior. Table 6.2 shows the voltage swing across a single varactor connected to node (a) or (b) inside the array for P_{out} = 20 and 30 dBm. As can be seen, for P_{out} = 30 dBm, the voltage across the varactor tied to node (b) is not distorted except for the 1×1 BST array. This voltage drops as the number of varactors in the array increases.

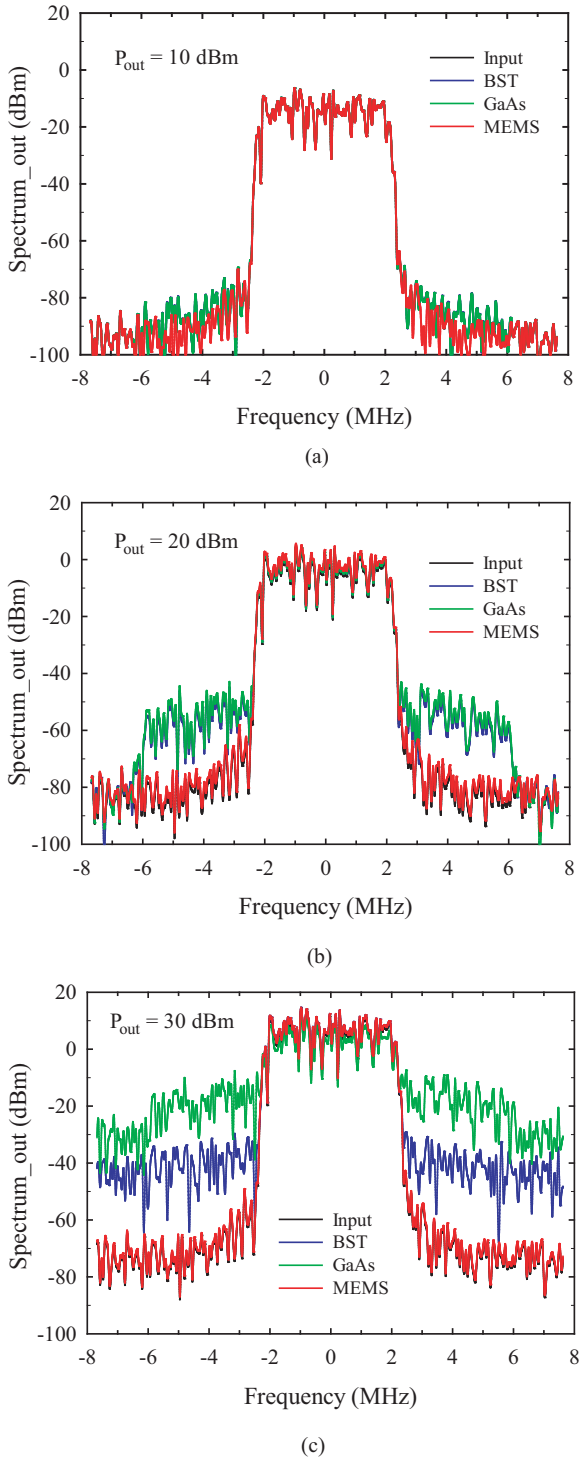


Figure 6.7: Simulated WCDMA spectrum at the output of the impedance tuners for different output powers.

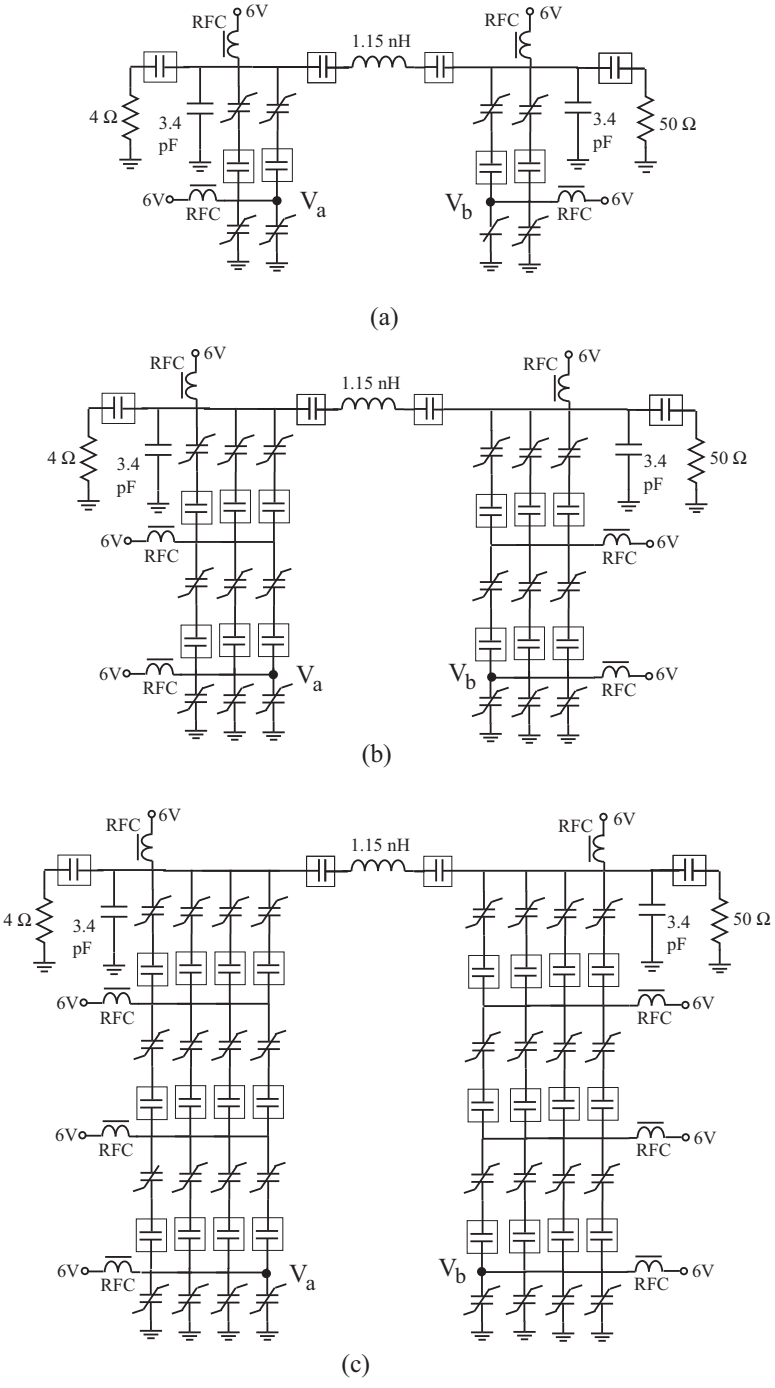


Figure 6.8: Impedance tuners with (a) 2 × 2 (b) 3 × 3 and (c) 4 × 4 BST array varactors .

Table 6.2: Voltage swing across a single varactor inside BST arrays at nodes (a) and (b) for different output powers.

Varactor	V_a(peak)	V_b(peak)
$P_{out} = 20$ dBm		
BST (1 × 1)	0.9 V	3.2 V
BST (2 × 2)	0.45 V	1.6 V
BST (3 × 3)	0.3 V	1.1 V
BST (4 × 4)	0.23 V	0.8 V
BST (3 × 1)	0.3 V	1.1 V
$P_{out} = 30$ dBm		
BST (1 × 1)	2.6 V	Distorted (−3.3 V to 16.7 V)
BST (2 × 2)	1.3 V	5.0 V
BST (3 × 3)	0.86 V	3.3 V
BST (4 × 4)	0.65 V	2.5 V
BST (3 × 1)	0.86 V	3.3 V

Table 6.3: IIP_3 level of BST impedance tuners with different varactor arrays.

Topology (BST)	1 × 1	2 × 2	3 × 3	4 × 4	3 × 1
IIP_3 (dBm)	20	24	27	29	30

To investigate the linearity improvement of the impedance tuner with BST array varactors, a two-tone intermodulation test is done in ADS using two sinusoid signals at f_1 = 1.95 GHz and $f_2 = f_1 + \Delta f$ (Δf = 1 MHz). Fig. 6.10 shows the simulated fundamental and IM_3 output power vs. input power for different BST impedance tuners. The IIP_3 level increases for tuner with larger arrays, but the IIP_3 improvement is not uniform. Table 6.3 shows the IIP_3 level for impedance tuners with different BST array varactors.

Fig. 6.11(a),(b) show the WCDMA output spectrum of the impedance tuners with different BST array varactors for 20 and 30 dBm output power, respectively. For $P_{out} = 20$ dBm, the spectral regrowth at the adjacent channel for impedance tuners with 4 × 4 and and 3 × 1 BST array varactors is suppressed and is very close to the spectral regrowth of a RF MEMS impedance tuner, so their

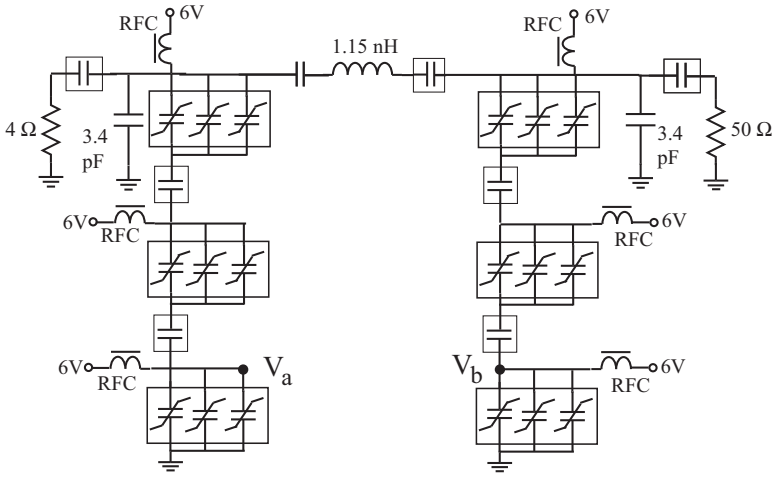


Figure 6.9: An impedance tuner with 3 × 1 BST array varactors.

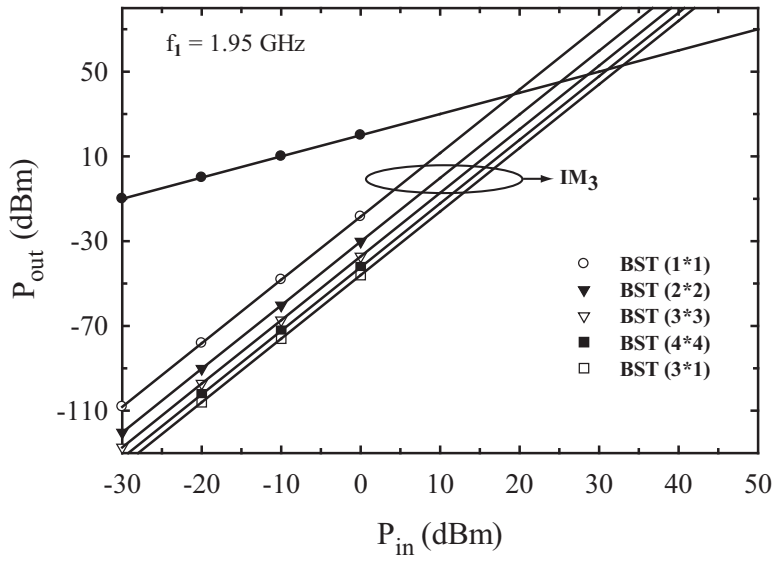
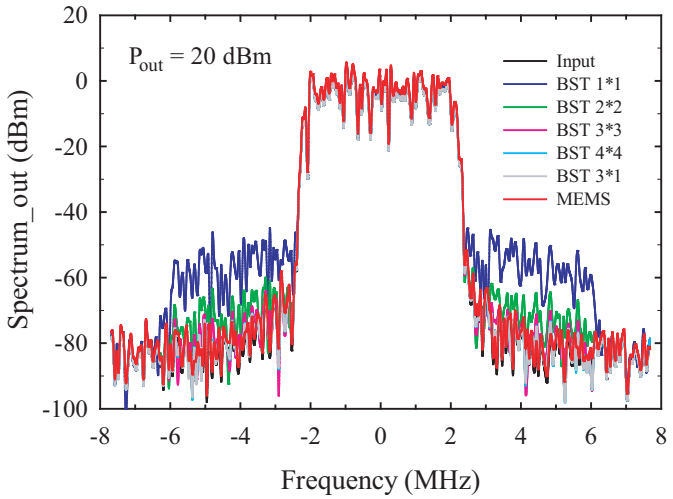
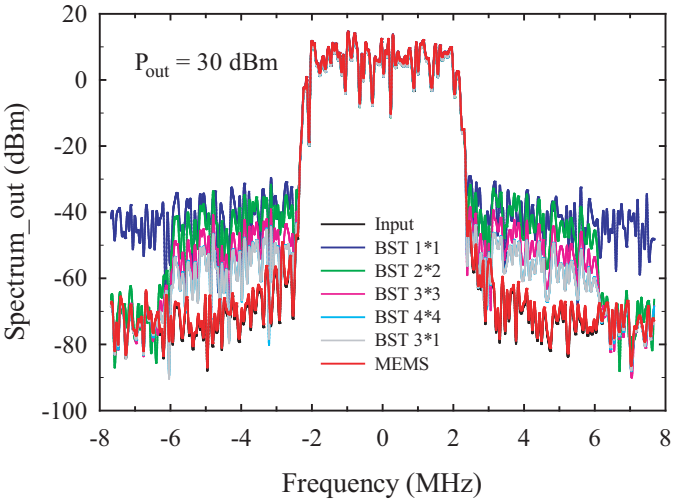


Figure 6.10: Simulated fundamental and IM_3 output power vs. input power for different BST tuners.



(a)



(b)

Figure 6.11: Simulated WCDMA spectrum at the output of impedance tuners with BST array varactors for different output powers.

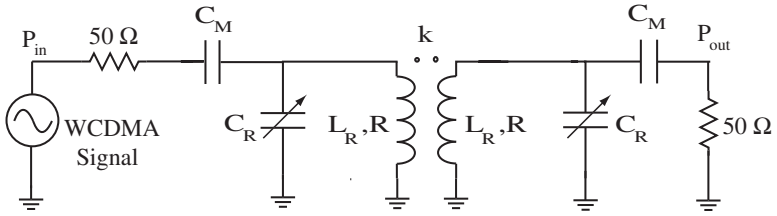


Figure 6.12: The schematic of a two-pole bandpass tunable filter excited by a WCDMA source at 1.95 GHz.

Table 6.4: Tunable filter element values at 1.95 GHz.

ElementValues	C_R (pF)	C_M (pF)	L_R (nH)	R (Ω)	k
–	2.3	0.42	2.48	0.15	0.04

linearity becomes comparable. For $\mathrm{P_{out}} = 30\ \mathrm{dBm}$, 4×4 and 3×1 BST array tuners have lower spectral regrowth compared to other BST tuners, but RF MEMS tuner still shows the lowest spectral regrowth among all other BST impedance tuners.

6.3 Tunable Filters in WCDMA Transceivers

6.3.1 Tunable filter topology

Fig. 6.12 shows the schematic of a two-pole bandpass tunable filter discussed in chapter 3. The filter is designed as a 3 $\%$, Chebyshev filter with a center frequency of 1.95 GHz, and Table 6.4 shows the element values of the filter at 1.95 GHz. The inductors have a resistance of 0.15 Ω, resulting an insertion loss of 1.2 dB in the pass-band (Q_u =200), and the capacitors are assumed lossless. The tuning range is from 1.7 to 2.2 GHz. By changing the shunt capacitor C_R from 1.7 to 3.1 pF, the tuning range is covered and there is no need to tune the matching capacitor, C_M. Fig .6.13(a),(b) show the simulated insertion loss and return loss of the filter, respectively. Table 6.5 presents the bandwidth,insertion loss and the C_R capacitor value for the tunable filter at different frequencies. The filter is excited by a WCDMA source at 1.95 GHz with a chip rate of 3.84 Mcps.

To implement the tunable filter, the tuning capacitor, C_R, is substituted by GaAs, BST and RF MEMS varactors from Fig. 6.5. Fig. 6.14(a),(b) show the tunable filter using GaAs and BST varactors, respectively. Both GaAs and BST varactors are biased at 6 V. Fig. 6.14(c) shows the

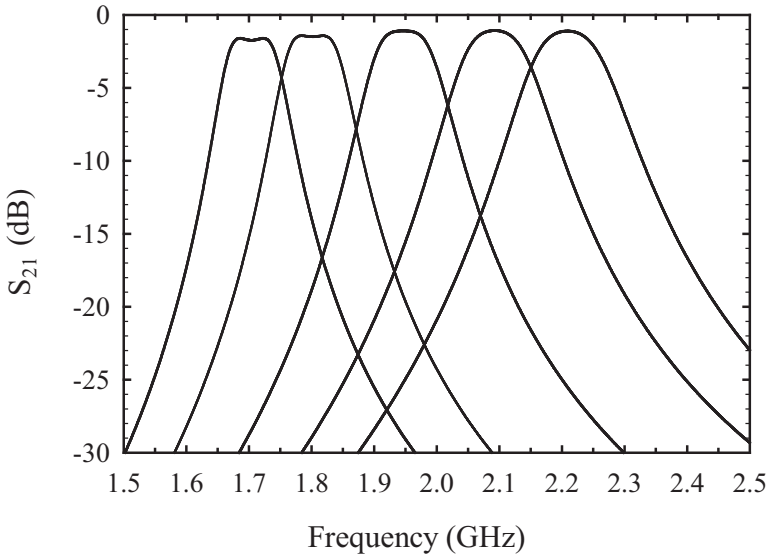
Table 6.5: Tunable filter specs. for different frequencies.

Frequency (GHz)	BW (MHz)	BW (%)	I.L. (dB)	C_R (pF)
1.7	54	3.2	-1.8	3.1
1.8	60	3.3	-1.7	2.7
1.95	58	3.0	-1.2	2.3
2.1	71	3.4	-1.1	2.0
2.2	77	3.5	-1.0	1.7

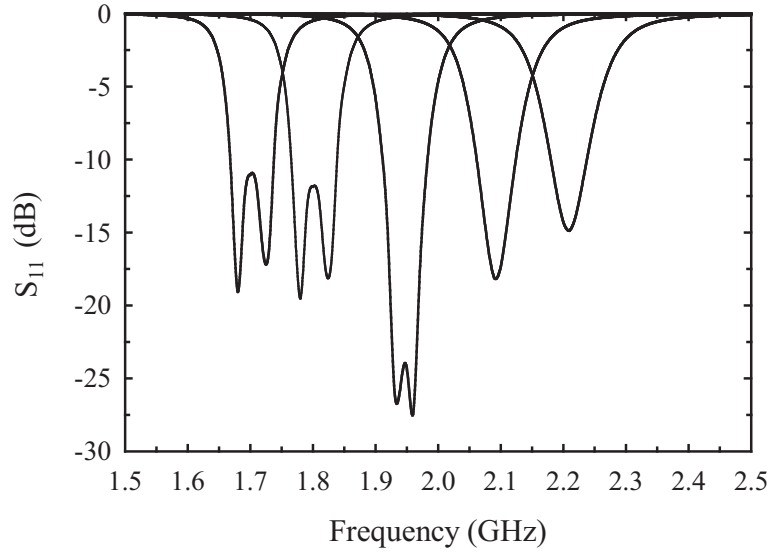
tunable filter using the RF MEMS switches. In this case, the varactor C_R is implemented as a 3-bit switched capacitor. Each switched capacitor is a series combination of the RF MEMS switch and a fixed capacitor. When all three switches are in the up-state, $C_R = 1.7$ pF. By pulling down S1 or S2 C_R value changes to 2.0 pF and the filter center frequency shifts to 2.1 GHz. When S1 and S2 are in the up-state and S3 is in the down-state, $C_R = 2.3$ pF and the filter center frequency is 1.95 GHz (Fig. 6.14(c)). By pulling down S1 or S2 while S3 is in the down-state, C_R and filter center frequency change to 2.7 pF and 1.8 GHz respectively. When both switches are in the down state then C_R value changes to 3.1 pF.

6.3.2 Simulation Results

The filter large signal S-parameters are simulated in ADS for different input power levels. Fig. 6.15(a) shows the GaAs filter large signal S_{21}. For $\mathrm{P_{in}}$ = 10 dBm the filter center frequency is at 1.95 GHz. By increasing the level of the input power to 20 dBm, the filter response experiences a small amount of distortion due to the nonlinear behavior of the GaAs varactors. At $\mathrm{P_{in}}$ = 22 dBm the filter response is distorted and the filter center frequency is not 1.95 GHz. For higher amount of input power, the filter does not behave as a filter any more. For the BST filter at Fig. 6.15(b), the filter response begins to get distorted at $\mathrm{P_{in}}$ = 20 dBm due to the nonlinear behavior of the BST varactors, but it is still negligible. At $\mathrm{P_{in}}$ = 28 dBm, the BST filter response distortion shifts the filter center frequency, but it still acts as a filter. The RF MEMS filter response does not change by increasing the level of the input power even up to 28 dBm (Fig. 6.15(c)). This is due to extremely linear behavior of the RF MEMS switches in the filter structure. For the input power greater than



(a)



(b)

Figure 6.13: The simulated (a) insertion loss, and (b) return loss of the tunable filter covering the 1.7-2.2 GHz tuning range ($Q_u = 200$, I.L.=1.0-1.8 dB).

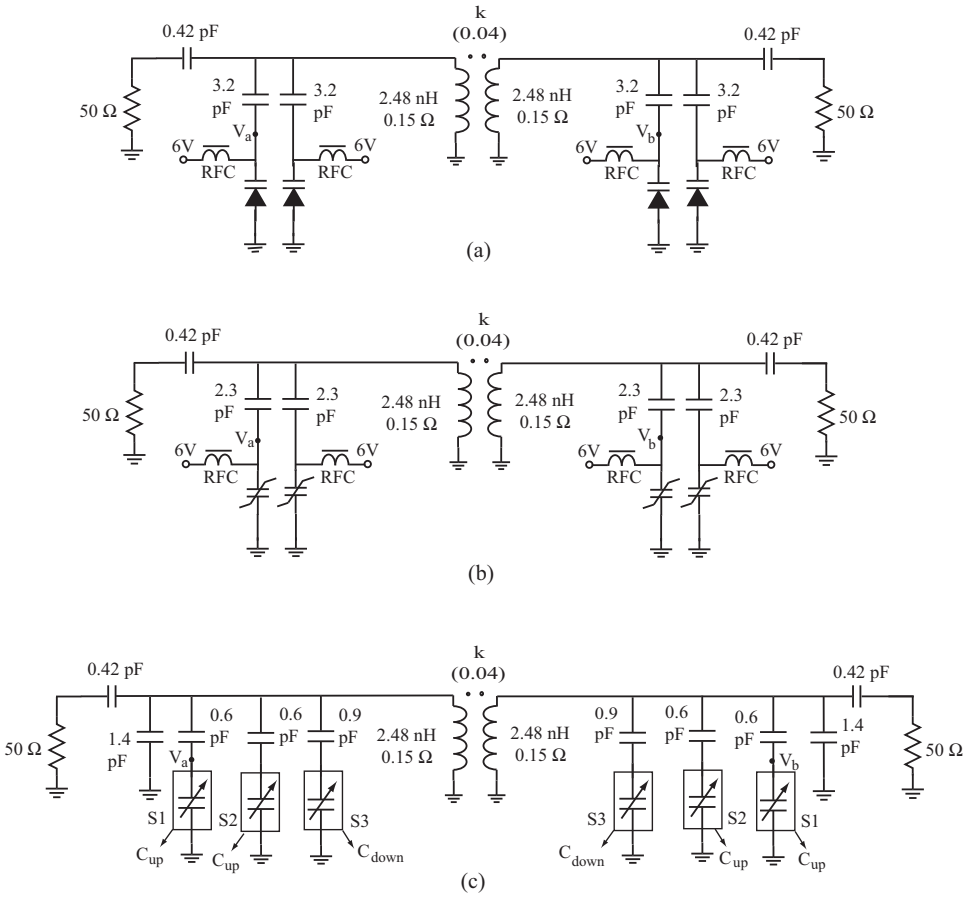


Figure 6.14: (a) GaAs (b) BST (c) RF MEMS Tunable Filters.

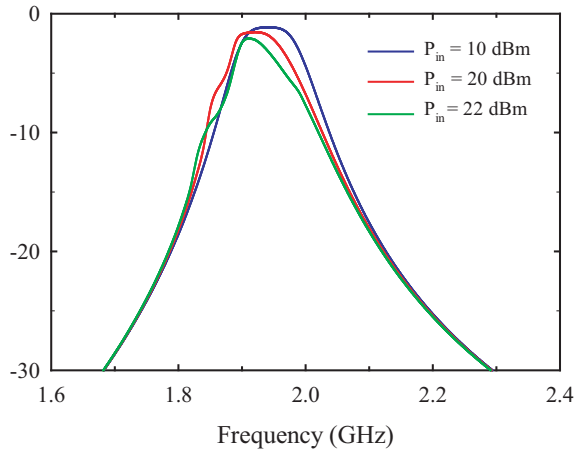
Table 6.6: Voltage swing across a single varactor inside the tunable filter at nodes (a) and (b) for different output powers at $f_0 = 1.95$ GHz.

Varactor	V_a(peak)	V_b(peak)
GaAs		
$P_{in} = 10$ dBm	2.4 V	2.2 V
$P_{in} = 20$ dBm	Compressed (-0.4 V to 15 V)	Compressed (0.6 V to 13 V)
$P_{in} = 22$ dBm	Compressed (-0.6 V to 16 V)	Compressed (0.4 V to 14.0 V)
BST		
$P_{in} = 10$ dBm	1.8 V	1.7 V
$P_{in} = 20$ dBm	6.0 V	5.2 V
$P_{in} = 28$ dBm	Distorted (-10.7 V to 27 V)	Distorted (-5.7 V to 21 V)
RF MEMS		
$P_{in} = 10$ dBm	3.2 V	2.8 V
$P_{in} = 20$ dBm	10 V	9 V
$P_{in} = 28$ dBm	17 V	16.6 V

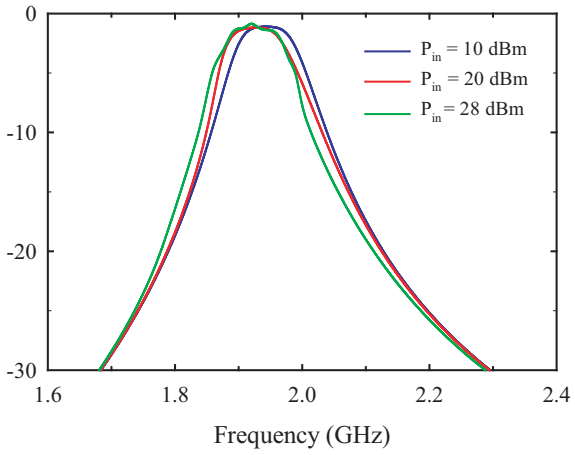
28 dBm, the filter response is getting distorted due to the self-biasing effect of the up-stare MEMS bridges.

Table 6.6 shows the voltage swing across GaAs, BST and RF MEMS varactors inside the tunable filter (points (a) and (b) in Fig. 6.14) for the 1.95 GHz single-tone excitation using harmonic balance simulation in ADS. For $P_{in} = 22$ dBm, the voltage across the GaAs varactor at nodes (a) and (b) is compressed. Due to high voltage swing across the varactor, it goes to the ohmic region and clips the voltage. The voltage across the BST varactor at nodes (a),(b) is also distorted for $P_{in} = 28$ dBm. The signal experiences a huge nonlinearity due to nonlinear C-V curve of the BST varactor. Also for $P_{in} = 28$ dBm, the voltage across the RF MEMS capacitive switch at nodes (a) and (b) reaches to 17 V and 16.6 V. This voltage is still smaller than the pull-down voltage of the switch, so the switch stays in the up-state position, self-biasing does not occur and the voltage is not distorted.

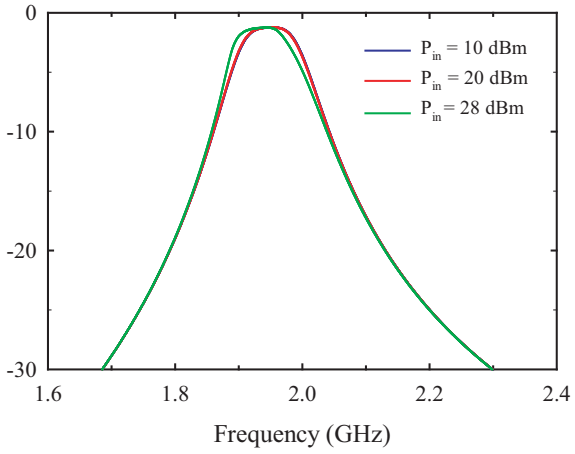
As mentioned before, to improve the linearity of the BST tunable filter, each BST varactor is substituted by a 3×1 array of similar BST varactors all biased at 6 V (Fig. 6.16). To investigate



(a)



(b)



(c)

Figure 6.15: Large signal S_{21} of (a) GaAs (b) BST and (c) RF MEMS tunable filter for different input power levels.

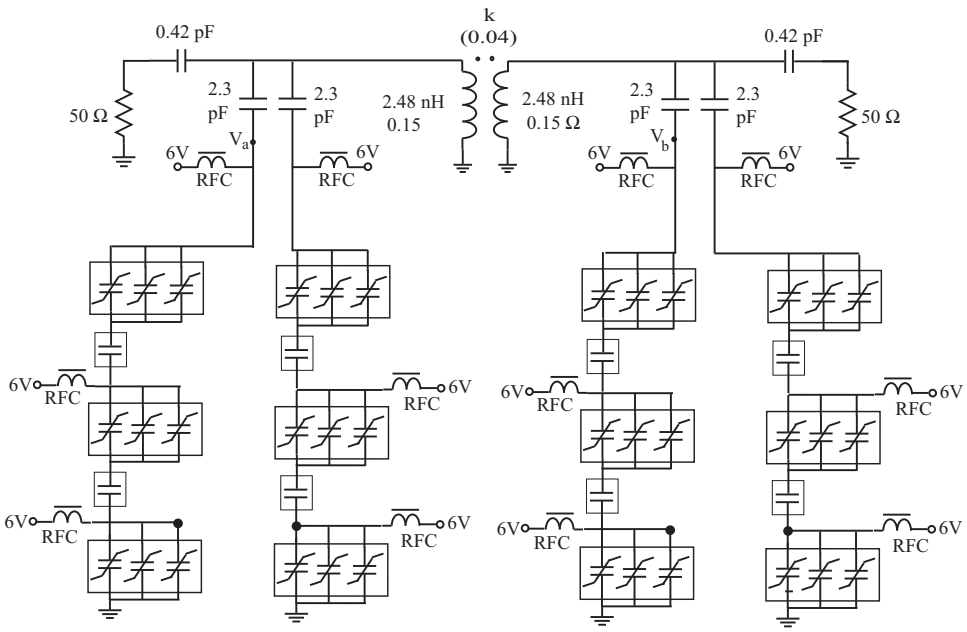


Figure 6.16: A tunable filter with 3 × 1 BST array varactors.

the linearity improvement of the tunable filter with BST array varactors, a two-tone intermodulation test is done in ADS using two sinusoid signals at f_1 = 1.95 GHz and $f_2 = f_1 + \Delta f$ (Δf = 1 MHz). Fig. 6.17 shows the simulated fundamental and IM_3 output power vs. input power for 1 × 1 and 3 × 1 BST tunable filters. As expected, the IIP_3 level increases from 24 dBm for 1 × 1 BST array to 34 dBm for 3 × 1 BST array.

We substitute the single-tone source with a WCDMA source at 1.95 GHz. Fig. 6.18 shows the simulated WCDMA spectrum at the output of GaAs, 1 × 1 and 3 × 1 BST arrays, and RF MEMS filters for different input powers. For P_{in} = 10 dBm , the GaAs and 1 × 1 BST array filters are pushed to their nonlinear region while the 3 × 1 BST array and RF MEMS filters are in their linear region. The WCDMA output spectrum for GaAs and 1 × 1 BST array tunable filters shows a spectral regrowth of more the 30 dB compared to their MEMS counterpart at the adjacent channel, but the 3 × 1 BST array filter is still in the linear region and just shows a spectral regrowth of around 5 dB compared to the RF MEMS filter. For P_{in} = 20 dBm, the GaAs varactors connected to nodes (a) and (b) enter to ohmic region. Both the GaAs and BST filters show nonlinear behavior while the RF MEMS filter still stays in the linear region. The GaAs, 1 × 1 and 3 × 1 BST array filters show 50, 50 and 30 dB of spectral regrowth at the adjacent channel compared to the RF MEMS

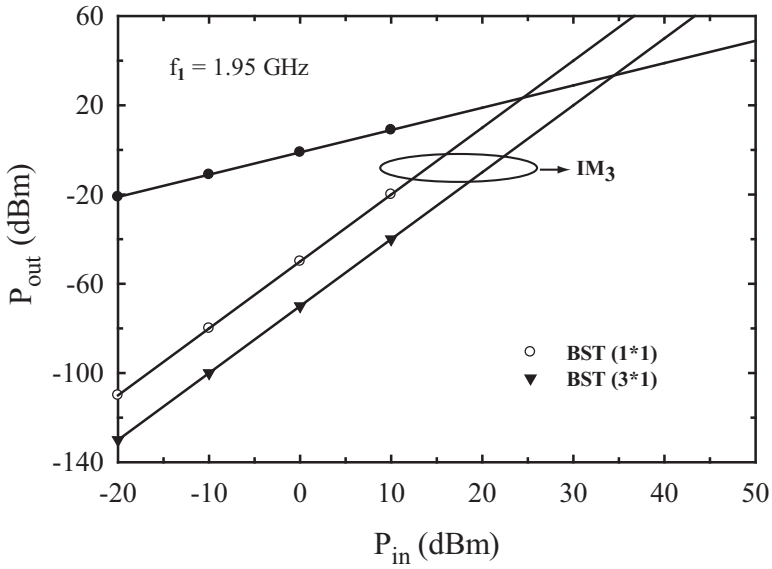


Figure 6.17: Simulated fundamental and IM_3 output power vs. input power for 1×1 and 3×1 BST array tunable filters.

filter, respectively. For P_{in} = 28 dBm, the RF MEMS filter remains surprisingly in the linear region, while both GaAs and BST filters show extremely nonlinear behavior. In this case, the 1×1 and 3×1 BST array filters show around 55 and 40 dB spectral regrowth compared to their RF MEMS counterpart, respectively. The output spectrum of the GaAs filter is not shown in Fig. 6.18(c), because the GaAs filter response is totally distorted at this power level and does not behave as a filter any more.

6.4 Conclusion

This chapter presents the simulation results for GaAs, BST and RF MEMS reconfigurable matching networks and tunable filters in a complex modulation system (WCDMA) front end. Both the RF MEMS impedance tuner and tunable filter have the best linearity among their GaAs and BST counterparts and the WCDMA spectrum at the output of the RF MEMS impedance tuner and tunable filter has the lowest spectral regrowth at the adjacent channel and the lowest adjacent channel interference compared to its GaAs and BST counterparts. Employing the BST array-based varactors instead of a single varactor in the BST impedance tuner, lowers the spectral regrowth considerably, but compared to the RF MEMS tuner, the later still has the lowest spectral regrowth.

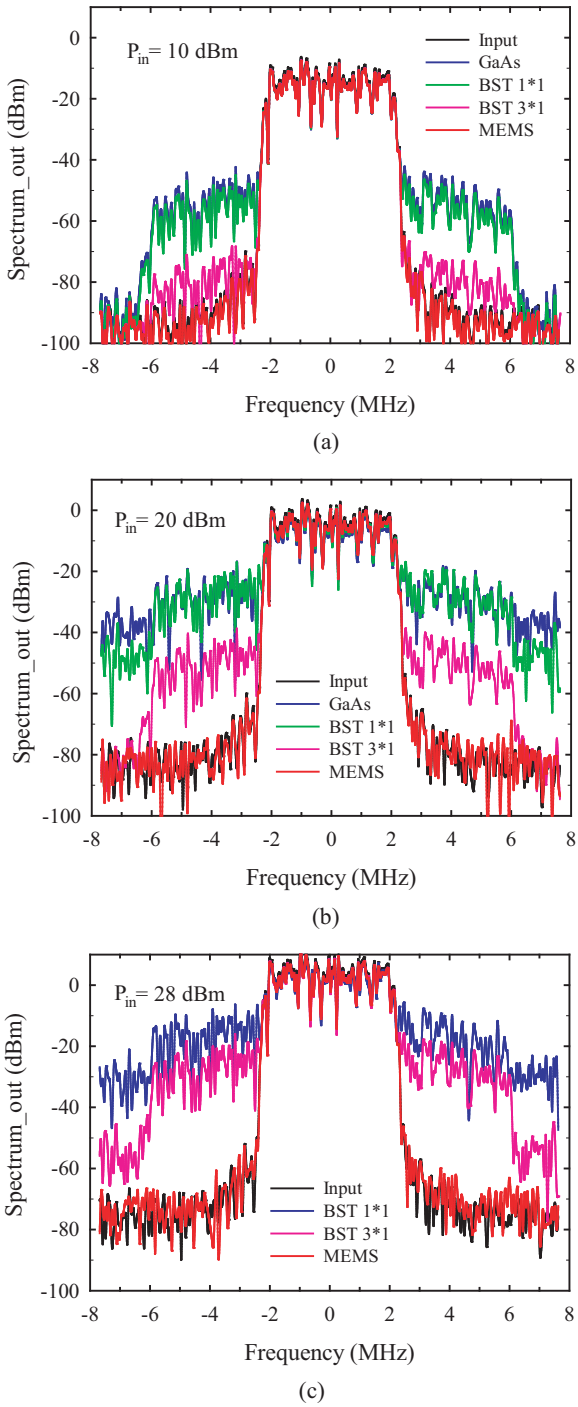


Figure 6.18: Simulated WCDMA spectrum at the output of tunable filters for different output powers.

CHAPTER 7

Conclusion and Future Work

7.1 Conclusion

The major topic in this thesis is the development of RF MEMS wide-band tunable filters for 6-18 GHz applications. Two different categories of state-of-the-art RF MEMS wide-band tunable filter have been designed, simulated, fabricated and measured in this thesis. The first one is a 6.5-10 GHz novel lumped element miniaturized differential filter. The 4-bit RF MEMS switched capacitor banks provide 16 different frequency responses that cover the whole band and result in a tuning range of 44% with very fine resolution. As a result the filter acts such as a contiguous filter for the whole band. The measured insertion loss of the filter varies between 4.1 and 5.6 dB when the tuning frequency varies from 10 to 6.5 GHz. Due to employing 3-bit matching capacitors in the filter topology, the measured return loss is always better than 16 dB over the whole band. The relative bandwidth of the filter is 5.1$\pm$0.4% over the tuning range and the size of the filter is 5 mm $\times$ 4 mm. the second one is another state-of-the-art RF MEMS wide-band tunable filter designed for 12-18 GHz frequency range. It is a filter with coplanar resonators. The resonators are loaded with two adjacent 4-bit RF MEMS capacitive switches at their center in a symmetrical faction, which results in a tuning range of 40% with very fine resolution, and for the case of 3-pole filter, return loss better than 10 dB for the whole tuning range. it is possible to achieve a better return loss, especially at lower frequencies, if the inductive inverters are made tunable. The relative bandwidth of the filter is approximately fixed over the tuning range. The size of the 2 and 3-pole filters are 5 mm $\times$ 4 mm, and 8 mm $\times$ 4 mm respectively. For a 2-pole filter, the insertion loss is 4.2 and

6.8 dB at 18.0 and 12.5 GHz, respectively. For a 3-pole filter, the insertion loss is 5.5 and 8.2 dB at 17.8 and 12.2 GHz, respectively. To our knowledge these the widest-band planar tunable filters to-date. The insertion loss of both filters improve by increasing the resistivity of the fabricated bias lines. The nonlinearity analysis and measurements prove that both filters show extremely linear behavior. The measured IIP_3 levels are >45 dBm ($\Delta f >$ 500 KHz) and >37 dBm ($\Delta f >$ 200 KHz) for 6.5-10 GHz and 12-18 GHz filter, respectively. The measured results are very close to full-wave simulations. This work shows that RF MEMS tunable filters are excellent for wide-band designs and result in very low intermodulation levels.

The other topic discussed in this thesis, is the wafer-scale microstrip packaging for RF MEMS devices. Two different packaging structures are introduced. Both of them are based on putting a high-resistivity silicon cap on top the wafer carrying the microstrip structures, using gold-to-gold bonding and making a hermetic gold sealing ring. For the first design, the microstrip line is passed underneath the sealing ring to access inside the package. The simulation results show huge resonances in the package insertion loss due to the floating metallic ring. by connecting the sealing ring to the backside ground using the via-holes through the 280 μm thick silicon wafer, the unwanted resonances disappear from the package responde. The package insertion loss is better than 0.4 dB up to 30 GHz for different package sizes. Due to the inductive effect of the via-holes, the gold ring grounding is not acceptable after 30 GHz. Using substrates thinner than 280 μm increases the package effective bandwidth. this package is not fabricated due to the complexity of fabrication compared to the second design. For the second design, the hermetic via holes are used to connect the CPW transmission lines on the back side of the alumina wafer to the microstrip structure underneath the silicon cap. Again, the floating sealing ring generates the unwanted resonance in the package pass-band and connecting the ring to the ground using via-holes through the alumina wafer removes this resonance. This package is fabricated and its response is measured. The measured insertion loss of the package with grounded ring is better than 0.5 dB from DC-23 GHz and the return loss is always better than 18 dB for the frequency band. the bandwidth is improved by using a thinner alumina substrate. The package isolation is better than 20 dB from DC-23 GHz.

Finally, the system-level response of reconfigurable front ends in complex modulation systems is investigated. The simulation results for GaAs, BST and RF MEMS reconfigurable matching networks and tunable filters in WCDMA front ends are presented. Both the RF MEMS impedance

tuner and tunable filter have the best linearity between their GaAs and BST counterparts and the WCDMA spectrum at the output of the RF MEMS impedance tuner and tunable filter has the lowest spectral regrowth at the adjacent channel and the lowest adjacent channel interference compared to its GaAs and BST counterparts. Using the BST array-based varactors instead of a single varactor in the BST impedance tuner, lowers the spectral regrowth considerably, but compared to the RF MEMS tuner, the later still has the lower spectral regrowth. As a result, RF MEMS reconfigurable front ends are excellent candidates for complex modulation systems.

7.2 Future Work

7.2.1 2-6 GHz RF MEMS Tunable Filters for Wireless Applications

Many wireless communication system front ends are operating at the 2-6 GHz, and multi-band transceivers are getting more popular in this frequency range. As a result, tunable/switchable filters become key components of these transceivers. Due to great advantages of RF MEMS filters, such as linearity and wide tuning range presented in chapters 3 and 4, it is important to investigate the design and implementation of these types of filters for 2-6 GHz frequency range too. RF MEMS switched capacitors would be again the key tuning elements. The choice of the filter topology is tricky for this frequency range. Using filter topologies in chapters 3 and 4 results in larger filters with unacceptable amount of insertion loss in the pass-band. Park et al.[83] demonstrated a novel miniature planar two-pole microstrip filter with independent electric and magnetic coupling at 2.1 GHz. The independent coupling allows separate control of two transmission zeroes and results in a sharp filter skirt very suitable for wireless communication applications. By substituting the fixed capacitors with appropriate RF MEMS switched capacitors we can achieve RF MEMS tunable filters with very small size and low insertion loss for 2-6 GHz applications.

7.2.2 2-18 GHz Channelizer Using RF MEMS Tunable Filters and a Triplexer

A 2-18 GHz channelizer has many military applications such as wide-band tacking and eavesdropping. Wide-band RF MEMS tunable filters are very good candidates to develop a new generation of channelizers due their excellent linearity. One important issue in RF MEMS channelizer

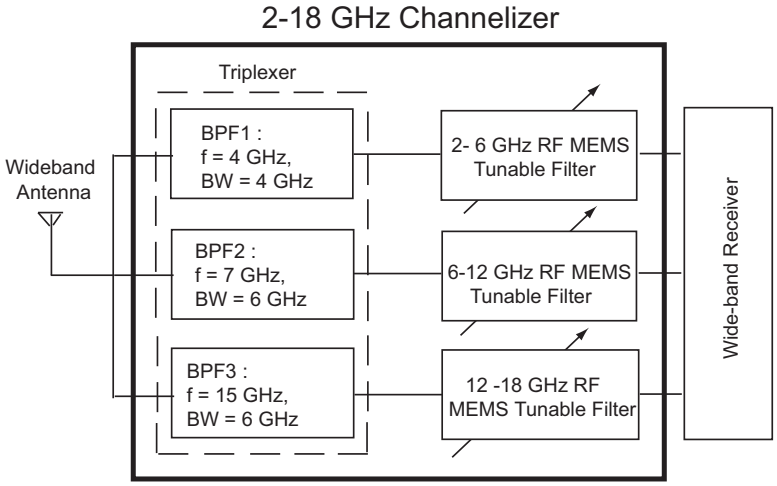


Figure 7.1: Block diagram of a 2-18 GHz RF MEMS tunable channelizer.

development is the relatively low switching speed of RF MEMS devices, but fortunately there is a serious effort to develop mini-MEMS switches with much higher switching speed [84]. Fig. 7.1 shows the general idea of a 2-18 GHz channelizer implemented by three 2-6, 6-12 and 12-18 GHz wide-band RF MEMS tunable filters and a triplexer including three band pass filters centered at 4, 7 and 15 GHz with bandwidth of 4,5,5 GHz respectively.

7.2.3 RF MEMS Band-Stop Tunable Filters

Band stop filters offer high levels of rejection over a narrow band with minimum distortion in the other parts of the spectrum. By complimenting the broadband rejection of the RF MEMS tunable bandpass filters with additional suppression of band stop filters at certain frequencies, it is possible to meet the tight requirements in variable radio configurations such as transmitter-receiver band noise suppression or receiver image rejection. Coverage of the majority of current and emerging telecommunication standards requires a very wide range on tuning, both for band pass and band stop filters. As a result, wide-band RF MEMS band stop filter design and implementation would be a completion of what has been done in this thesis regarding the RF MEMS band pass tunable filters.

A suitable topology for tunable band stop filters consists of resonant stubs coupled via quarter wavelength transmission lines or inverters (Fig. 7.2) [85][86]. The filter center frequency is controlled by the resonant frequency of the stubs. By adjusting the coupling between the stubs while changing their resonant frequency, the filter stop-band frequency is tuned over a wide range without

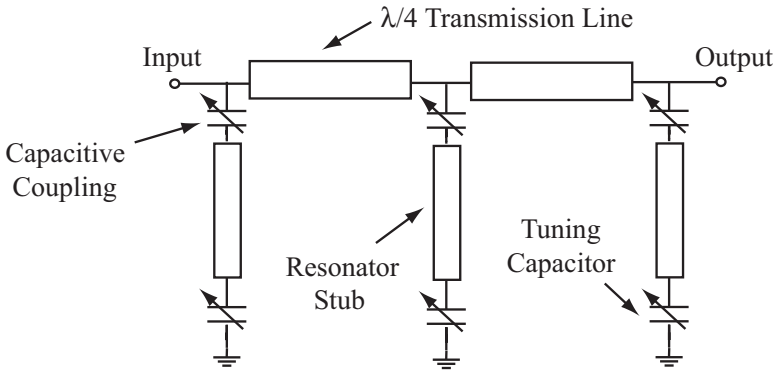


Figure 7.2: The schematic of a RF MEMS band-stop microwave filter suitable for wide-band tuning.

introducing distortion in the filter shape or bandwidth. The tuning capacitors can be implemented using the RF MEMS switched capacitor banks as mentioned in chapters 3 and 4.

7.2.4 Packaging of CPW and Microstrip RF MEMS Reconfigurable Networks

RF MEMS reconfigurable circuits including SPNT switches, impedance tuners, phase shifters and tunable filters, they can also be hermetically packaged by applying the microstrip line (or CPW line) packaging techniques introduced in chapter 5 . Based on the size, topology, frequency range and bandwidth of operation of the circuit, it would be possible to package the whole reconfigurable circuit or parts of it at the wafer scale. For circuit topologies that occupy a large area and it is not possible to package the whole circuit, it is important to design the layout properly to be able to package groups of RF MEMS switches sitting close enough together or single RF MEMS switches independently at the wafer-scale level.

APPENDICES

APPENDIX A

RF MEMS Switched Capacitor Fabrication on Glass Substrates

A.1 Introduction

This appendix presents the fabrication procedure for RF MEMS switched capacitors, which are the building blocks of both 6-10 and 12-18 GHz tunable filters discussed in detail in chapters 3 and 4. The fabrication process is the result of a joint effort with other researches in Prof. Rebeiz's group, mainly Dr. Bryan Hung, Dr. Bernhard Schoenlinner and Mr. Tauno Vaha-Heikkilla.

A.2 Fabrication Steps

A.2.1 High Resistivity Line Sputtering

(1) Clean wafer with acetone and IPA. Blow dry with N_2. Hard-bake at 130°C for 2 min for dehydration.

(2) Spin HMDS adhesion layer at 3000 rpm for 30 sec, spin negative photo-resist 5214 at 3000 rpm for 30 sec. Soft-bake at 105°C for 2 min. Then align and expose for 1.3-1.5 sec. Hardbake at 130°C for 1 min. Flood expose for 60 sec. Develop in 327 developer for 4-5 min. Rinse in cascade DI water for 2 min then blow dry with N_2.

(3) Sputter SiCr (1,200 Å). Parameters: RF Sputtering, Target 2, Pressure = 7 mT, Power = 700 W, Time = 18 min, Speed = 20 rpm. Gas: Ar.

(4) Lift off in hot PRS 2000 (temperature setting = HI, 110°C) overnight. Rinse thoroughly in DI water for 15 mins. Put the sample in the micro-stripper (O_2 plasma) at 150 W for 2 min to remove

photoresist (PR) and other organic scums.

A.2.2 First Metal Layer Deposition Using a Lift-off Process

(1) Hard-bake at 130°C for 2 min for dehydration.

(2) Spin HMDS adhesion layer at 3000 rpm for 30 sec, spin negative photo-resist 5214 at 3000 rpm for 30 sec. Soft-bake at 105°C for 2 min. Then align and expose for 1.3-1.5 sec. Hardbake at 130°C for 1 min. Flood expose for 60 sec. Develop in 327 developer for 4-5 min. Rinse in cascade DI water for 2 min then blow dry with N_2.

(3) Evaporate Ti/Au/Ti= 500/5000/500 Å . Blow substrate surface with N_2 just before putting the sample into the evaporator.

(3) Lift off in hot PRS 2000 (temperature setting = HI) overnight. Rinse thoroughly in DI water for 15 mins. Put the sample in the micro-stripper (O_2 plasma) at 150 W for 2 min to remove photoresist (PR) and other organic scums.

A.2.3 Silicon Nitride Deposition by PECVD

PECVD (Plasma Enhanced Chemical Vapor Deposition) 1800-2000 Å-thick Si_3N_4 with the following parameters: SiH_4 = 100 sccm, NH_3 = 10 sccm, He = 900 sccm, N_2 = 990 sccm , Pressure = 700 mT, Power = 100 W, Temperature = 400°C, Time = 8-10 min.

A.2.4 Silicon Nitride Etch Using Semi-Group RIE

(1) Spin HMDS adhesion layer at 3000 rpm for 30 sec. Spin PR 1827 at 3000 rpm for 30 sec. Soft-bake at 105°C for 2 min. Align and expose for 15 sec. Develop in diluted 351 developer (351:DI=1:5) for 1 min. Rinse in cascade DI water for 2 min and blow dry with N_2. Hardbake at 130°C for 1.5 min. Clean wafer in Plasma O_2 at 150 W for 2 min.

(2) RIE (Reactive Ion Etching) with the following parameters: CF_4 = 40 sccm, O_2 = 1 sccm, Pressure = 100 mT, Power = 100 W, time = 7-9 min.

(3) Strip the photoresist in hot PRS 2000 overnight. Rinse in DI water for 15 mins. Check the nitride areas under microscope. If there is any HMDS scum, descum at 150 W for 3 mins. This should remove the HMDS scums.

A.2.5 PMMA Sacrificial Layer

A. PMMA Layer:

(1) Spin HMDS adhesion layer at 3000 rpm for 30 sec full ramp.

(2) Spin PMMA 950 K, A9 at 2400 rpm for 45 sec full ramp. This results in 1.5 μm PMMA thickness.

(3) Hard-bake at 130°C using the hot plate for 10 min to avoid degassing of the PMMA layer.

(4) Bake at 170 C in oven for 30 min and let it cool down for 10 min.

B. Ti Mask:

(1) Evaporate or sputter 2000 $\mathring{A}$ of Ti.

(2) Spin photoresist 1827 at 3000 rpm for 30 sec full ramp.

(3) Soft-bake at 105°C for 2 min.

(4) Expose 15 sec and develop using 351:DI (1:5). Do not hard-bake. Etch in HF:DI (1:10).

(5) Flood expose 1 min and develop in 351:DI(1:5). Note: Do not hard bake and put wafer in plasma O_2 etcher since it etches the PMMA sacrificial layer too.

C. PMMA RIE Etching and Mask Removal:

(1) Etch PMMA in RIE with the following parameters: O_2 = 20 sccm, Pressure = 20 mT, Power = 50 W, Time = 30 m̃in for 1.5 μm PMMA layer removal.

(2) Etch the Ti mask in HF:DI (1:10). Rinse in DI water for 3 min. Blow dry with N_2.

A.2.6 Bridge Sputtering

Sputter Ti/Au/Ti= 200/8000/200 Å. Parameters: Ti: Pressure = 7 mT, Target 1, Power = 500 W, Time = 5 min, Speed = 20 rpm. Au: Pressure = 9.5 mT, Target 3, Current = 0.5 A, Time = 30 min, Speed = 20 rpm. Gas:Ar.

A.2.7 Electroplating

(1) Spin PR 1827 at 3000 rpm for 30 sec. Soft-bake at 105°C for 2 min. Align and expose for 15 sec. Develop in 351:DI for 1 min. Rinse in DI water for 4 min. Check under microscope. Soft-bake another 2 min at 105° to improve PR adhesion.

(2) Etch top Ti with HF:DI (1:15). This should take a few seconds. Watch for bubble coming out

and color change from grayish to shiny gold. Rinse in DI water for 3 min. Soft-bake for 1 min at 105°C to improve PR adhesion.

(3) Electroplate 2-3 μm of gold. The gold plating solution is BDT 510. Heat the solution to 50°C and use a magnetic stirrer (200 rpm) to increase plating uniformity. The current density and time are set based on the electroplating area and the gold thickness. After electroplating, rinse in DI water and blow dry with N_2. Use Dektak before and after the plating to measure the thickness of gold deposited.

(4) Flood expose the wafer for 1.5 min and develop the resist in 351:DI for 1 min. Rinse in DI water and blow dry with N_2. Check under microscope to see if the photoresist is well developed.

A.2.8 Bridge Lithography

(1) Spin PR 1827 at 3000 rpm for 30 sec. Soft-bake at 105°C for 2 min. Align and expose for 15 sec; develop in 351:DI for 1 min. Rinse in DI water for 4 min. Soft-bake another 2 min at 105°C to improve PR adhesion.

(2) Etch top Ti with HF:DI(1:15). This should take few seconds. Watch for bubble coming out and color change from grayish to shiny gold. Rinse in DI water for 3 min. Soft-bake for 1 min at 105°C to improve PR adhesion.

(3) Etch Au in TFA gold etchant. The color of the gold will turn dull. When etching is complete (usually takes 2-3 min), the wafer will appear grayish (Ti color). Remove from solution every 10-20 sec to check progress. Rinse in DI water for 3 min. TFA gold etchant over etches quickly so be very careful when doing this step.

(4) Flood expose for 1.5 min. Develop in 351:DI for 2 min. Rinse in DI water for 5 min. This removes all the PR on top of the bridges and the ground planes.

(5) Etch Ti in HF:DI (1:15). This takes a few seconds (watch for bubbles), the original wafer color is restored. Rinse in DI water for 3 min.

A.2.9 Bridges Release and Critical Point Drying

(1) Soak in PRS 2000 overnight to dissolve the PMMA sacrificial layer.

(2) Rinse in water for 10 min, no blow drying. Transfer to IPA immediately.

(3) Transfer sample to the Critical Point Drying system and perform CPD according to stated procedure.

APPENDIX B

Microstrip Package Fabrication

B.1 Introduction

This appendix presents the fabrication procedure for the wafer-scale RF MEMS microstrip package, discussed in chapter 5. The fabrication process is the result of a joint effort with Mr, Byung-Wook Min in Prof. Rebeiz's group.

B.2 Fabrication Steps; The Silicon Wafer

B.2.1 Gold Ring Deposition

(1) Clean wafer with acetone and IPA. Blow dry with N_2. Hard-bake at 130°C for 2 min for dehydration.

(2) Sputter Ti/Au = 200/20,000 Å as a seed layer. Parameters: Ti: Pressure = 7 mT, Target 1, Power = 500 W, Time = 5 min, Speed = 20 rpm. Au: Pressure = 7 mT, Target 3, Current = 0.5 A, Time = 10 min, Static. Gas:Ar.

(3) Spin HMDS adhesion layer at 3000 rpm for 30 sec. Spin PR 1827 at 3000 rpm for 30 sec. Soft-bake at 105°C for 2 min. Align and expose for 15 sec; develop in 351:DI (351:DI=1:5) for 1 min. Rinse in DI water for 4 min. Hard-bake for 2 min at 130°C to improve PR adhesion.

(4) Etch Au in TFA gold etchant. The color of the gold will turn dull. When etching is complete (usually takes 9-10 min), the wafer will appear grayish (Ti color). Remove from solution every 45 sec to check progress. Rinse in DI water for 3 min.

(5) Flood expose for 1.5 min. Develop in 351:DI (351:DI=1:5) for 2 min. Rinse in DI water for 5 min. This removes all the PR on top of the sealing rings.
(6) Etch Ti in HF:DI (1:15). This takes a few seconds (watch for bubbles), the original wafer color is restored. Rinse in DI water for 3 min.
(7) Clean in PRS 2000 overnight. Rinse thoroughly in DI water for 5 mins. Put the sample in the micro-stripper (O_2 plasma) at 150 W for 2 min to remove photoresist (PR) and other organic scums.

B.2.2 Cavity Deep Etching

(1) Hard-bake at 130°C for 2 min for dehydration.
(2) Spin HMDS adhesion layer at 3000 rpm for 30 sec. Spin PR 9260 at 4000 rpm for 45 sec. Soft-bake at 110°C for 2 min. Align and expose for 20-25 sec; develop in 400K:DI for 1-2 min. Rinse in DI water for 4 min.
(3) The 4-inch dummy silicon wafer preparation (The main 3-ich silicon wafer is adhered to the dummy wafer, because the existing deep silicon etching machine just works with 4-inch wafers): Spin HMDS adhesion layer at 3000 rpm for 30 sec. Spin PR 1827 at 3000 rpm for 30 sec. Put the 3-inch silicon wafer at the center of the dummy wafer and push the corners of the main wafer until they connect to each other.
(4) Bake at 120 C in oven for 30 min and let it cool down for 10 min.
(5) Deep etch silicon in DRIE for 45 m̃in for approximately 130 μm silicon deep etching.
(6) Clean in PRS 2000 overnight or longer until two wafers are separated from each other. Rinse the 3-inch wafer thoroughly in DI water for 5 mins. Put the sample in the micro-stripper (O_2 plasma) at 150 W for 2 min to remove photoresist (PR) and other organic scums.

B.3 Fabrication Steps; The Alumina Wafer

We assume that the via-holes are fabricated through the alumina wafer before we start the rest of the fabrication process.

B.3.1 Backside Metal Seed Layer Deposition and Electroplating

(1) Clean wafer with acetone and IPA. Blow dry with N_2. Hard-bake at 130°C for 2 min for dehydration.

(2) Sputter Ti/Au/Ti= 200/1000/200 Å as seed layer. Parameters: Ti: Pressure = 7 mT, Target 1, Power = 500 W, Time = 5 min, Speed = 20 rpm. Au: Pressure = 7 mT, Target 3, Current = 0.5 A, Time = 4.5 min, Speed = 20 rpm. Gas:Ar.

(3) Front-side protection: Spin HMDS adhesion layer at 3000 rpm for 30 sec, and then spin PR 1827 at 3000 rpm for 30 sec on the front-side. Soft-bake at 105°C for 2 min. Backside lithography: Spin HMDS adhesion layer at 3000 rpm for 30 sec , and spin PR 1827 at 3000 rpm for 30 sec on the backside. Soft-bake at 105°C for 2 min. Align using the via-hole pattern and expose for 15 sec. Develop in 351:DI for 1 min. Rinse in DI water for 4 min. Check under microscope. Soft-bake for another 2 min at 105° to improve PR adhesion.

(4) Etch top Ti with HF:DI (1:15). This should take a few seconds. Watch for bubble coming out and color change from grayish to shiny gold. Rinse in DI water for 3 min. Soft-bake for 1 min at 105°C to improve PR adhesion.

(5) Electroplate 2-3 μm of gold. The gold plating solution is BDT 510. Heat the solution to 50°C and use a magnetic stirrer (200 rpm) to increase plating uniformity. The current density and time are set based on the electroplating area and the gold thickness. After electroplating, rinse in DI water and blow dry with N_2. Use Dektak before and after the plating to measure the thickness of gold deposited.

(6) Flood expose the wafer for 1.5 min and develop the resist in 351:DI for 1 min. Rinse in DI water and blow dry with N_2. Check under microscope to see if the photoresist is well developed.

(7) Etch Au in TFA gold etchant. The color of the gold will turn dull. When etching is complete (usually takes lees than 1 min), the wafer will appear grayish (Ti color). Remove from solution every 10 sec to check progress. Rinse in DI water for 3 min. TFA gold etchant over etches quickly so be very careful when doing this step.

(8) Etch Ti in HF:DI (1:15). This takes a few seconds (watch for bubbles), the original wafer color is restored. Rinse in DI water for 3 min.

(9) Clean in PRS 2000 overnight. Rinse thoroughly in DI water for 5 mins. Put the sample in the

micro-stripper (O_2 plasma) at 150 W for 2 min to remove photoresist (PR) and other organic scums.

B.3.2 Front-side Metal Seed Layer Deposition and Electroplating

(1) Clean wafer with acetone and IPA. Blow dry with N_2. Hard-bake at 130°C for 2 min for dehydration.

(2) Sputter Ti/Au/Ti= 200/1000/200 Å as seed layer. Parameters: Ti: Pressure = 7 mT, Target 1, Power = 500 W, Time = 5 min, Speed = 20 rpm. Au: Pressure = 7 mT, Target 3, Current = 0.5 A, Time = 4.5 min, Speed = 20 rpm. Gas:Ar.

(3) Backside protection: Spin HMDS adhesion layer at 3000 rpm for 30 sec, and then spin PR 1827 at 3000 rpm for 30 sec on the backside. Soft-bake at 105°C for 2 min. Front-side lithography: Spin HMDS adhesion layer at 3000 rpm for 30 sec , and spin PR 1827 at 3000 rpm for 30 sec on the front-side. Soft-bake at 105°C for 2 min. Align with backside using the via-hole pattern again. Expose for 15 sec. Develop in 351:DI for 1 min. Rinse in DI water for 4 min. Check under microscope. Soft-bake for another 2 min at 105° to improve PR adhesion.

(4) Etch top Ti with HF:DI (1:15). This should take a few seconds. Watch for bubble coming out and color change from grayish to shiny gold. Rinse in DI water for 3 min. Soft-bake for 1 min at 105°C to improve PR adhesion.

(5) Electroplate 2-3 μm of gold. The gold plating solution is BDT 510. Heat the solution to 50°C and use a magnetic stirrer (200 rpm) to increase plating uniformity. The current density and time are set based on the electroplating area and the gold thickness. After electroplating, rinse in DI water and blow dry with N_2. Use Dektak before and after the plating to measure the thickness of gold deposited.

(6) Flood expose the wafer for 1.5 min and develop the resist in 351:DI for 1 min. Rinse in DI water and blow dry with N_2. Check under microscope to see if the photoresist is well developed.

(7) Etch Au in TFA gold etchant. The color of the gold will turn dull. When etching is complete (usually takes lees than 1 min), the wafer will appear grayish (Ti color). Remove from solution every 10 sec to check progress. Rinse in DI water for 3 min. TFA gold etchant over etches quickly so be very careful when doing this step.

(8) Etch Ti in HF:DI (1:15). This takes a few seconds (watch for bubbles), the original wafer color

is restored. Rinse in DI water for 3 min.

(9) Clean in PRS 2000 overnight. Rinse thoroughly in DI water for 5 mins. Put the sample in the micro-stripper (O_2 plasma) at 150 W for 2 min to remove photoresist (PR) and other organic scums.

B.4 Bonding Two Wafers

(1) Align the top and bottom wafers by EV501s aligner using the align keys on the backside of the alumina wafer and the front-side of the silicon wafer.

(2) bond two wafers using EV501s bonder. Parameters: Temperature = 320°C, Pressure = 7 MPa, Time = 1 hour

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