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Development of a Direct-Sampling Digital Correlation Radiometer for Earth Remote Sensing Applications

by

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A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
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To my teachers.
Phyllis Levy
Faith Adams
Darrell Parnell
David Middlebrook

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CHAPTER 1

Introduction: Science Objectives and the Converging Technological Capabilities for an Advanced L-Band Radiometry Mission

1.1 Prologue

Wide bandwidth analog-to-digital conversion has advanced to the point where it could ease the implementation of aperture synthesis radiometer satellites, especially for applications that require improved spatial resolution at L-band frequencies. One potential by-product of this A/D converter technology is a novel *direct RF sampling* radiometer, whose simplified architecture would have a number of inherent advantages in aperture synthesis. In this thesis, I will analyze and implement (through hardware) a prototype direct-sampling digital correlation radiometer system operating at 1.4 GHz so that performance figures like noise-equivalent sensitivity and phase stability can be quantified. To begin, the requirements for the instrument will be put in the context of a remote sensing mission for soil moisture retrieval, which would lead to improvements in the predictive skill of weather and climate models.

1.2 Numerical Weather Prediction with Microwave Radiometry

1.2.1 Soil moisture retrieval

Water stored in soil plays a crucial role in continental weather and near-term climate, mainly because this moisture influences how much latent heat energy is transferred between the land and atmosphere. The mechanisms of evaporation from the soil surface and transpiration through vegetation layers, cumulatively called *evapotranspiration*, move latent heat energy in the form of water vapor into the atmosphere, where this energy may be released later through condensation [52]. In certain regions and at particular times of the year, evapotranspiration can become the dominant component of energy flux from the land to atmosphere. A running knowledge of these flux levels therefore improves predictions of near-term (30–90 day) climate trends, which can have far reaching consequences for regional economies, agriculture and human health.

Several recent climatological studies have been conducted that underscore the dominant influence of soil moisture and evapotranspiration in affecting weather. General circulation models (GCMs) for the central and eastern United States partition energy contributions from the ground into infrared radiation, sensible heat flux, and latent heat flux. Among these three components, $\sim 70\%$ of the mean energy transported from land to atmosphere over a 50-day summer period arises from latent heat flux [64]. There is also a cause-effect relation between soil saturation, evapotranspiration, and precipitation that sets up a positive feedback condition, tending to draw out persistent weather events like drought and flooding. A retrospective study of the drought of 1988 in the Midwestern U.S. using GCMs demonstrated that the time correlation and magnitude of the drought was mainly influenced by anomalies in soil moisture [2]. To compare the relative importance of input boundary conditions in the model, several simulations were run with ground truth data for soil moisture or sea surface temperature turned on or off. Realistic values of soil moisture lead to

the greatest reductions in precipitation and increases in surface temperature, corresponding to the real conditions experienced that summer during the 1988 drought. GCM modeling studies by Koster and Suarez have also shown that variations in precipitation over continents are most affected by moisture and energy transport through evapotranspiration. Persistent precipitation events experienced during the Midwest's Flood of 1993 could be predicted accurately only when antecedent soil moisture data were available at sufficient temporal and spatial resolutions [28].

1.2.2 L-band radiometry

Why lower microwave frequencies are better

Since the 1970's, researchers working in climate physics and remote sensing have realized that L-band (1–2 GHz) radiometry is potentially the most effective tool for mapping soil moisture on a global scale [62]. The main benefit of a satellite-based sensor, especially one at microwave frequencies, is its ability to acquire data consistently with a single instrument that can operate through cloud cover or at night. At a relatively long wavelength of 21 cm (1.4 GHz), the upwelling radiated brightness temperature from the ground will be highly sensitive to the amount of water stored within the top layer of soil due to the large difference between dielectric coefficients for dry soil ($\epsilon_r \approx 3$) and liquid water ($\epsilon_r \approx 80$). The L-band brightness signature will also include radiation emitted by soil as much as 5 cm below the ground surface [24]. This emission depth is significantly greater at L-band frequencies than at higher frequencies because there is less attenuation of upwelling radiation at longer wavelengths. In addition, other factors that can add noise to radiometric measurements of soil moisture, for example, soil surface roughness and scattering from vegetation, become less important at low microwave frequencies [63].

Physically based one-dimensional hydrology/radiobrightness (1dH/R) models have consistently demonstrated the high sensitivity of L-band brightnesses to surface soil moisture, even with overlaying vegetation canopy densities up to 4 kg/m^2 [39]. Results for a 60-day

dry-down simulation in prairie grassland show that the soil brightness makes up 75–80% of the total signature at 1.4 GHz, whereas the corresponding contributions at 19 and 37 GHz are only 10% and 3%, respectively. In contrast to L-band radiometry, 19–85 GHz frequencies provided by satellites that are currently in operation, like the Special Sensor Microwave/Imager (SSM/I), are not effective for determining soil moisture content. Radiobrightness experiments with a ground-based SSM/I simulator show that for prairie with moderate vegetation densities of 2 kg/m^2, the vegetation canopy essentially absorbs all upwelling microwave radiation, masking the signal emitted by the soil [11].

Inverse problem

Entekhabi *et al.* have demonstrated that L-band brightness measurements, coupled with a Kalman filter algorithm, can be used to solve the inverse remote sensing problem [13]—that is, finding soil moisture from a history of brightness temperatures. In this *assimilation* technique, vertical temperature and moisture profiles can be inferred to a depth of tens of centimeters, given a knowledge of soil moisture within the top few centimeters over some period of time. The brightness predicted by a radiative transfer model for the soil is compared with actual measurements, and this difference, or error signal, is used to dynamically correct the state of the soil moisture and temperature profiles. Experimental results with a 1.4 GHz radiometer show that over the course of several precipitation and dry-down events, vertical profile errors can be contained to within 2–8% volumetric soil moisture, to depths of 60 cm [16].

Scaling

There is also evidence that L-band radiometry may avoid some of the scaling problems that arise in remote sensing. Because the relationship between canopy column density and radiobrightness is non-linear, the pixel brightness for regions having heterogeneous landcover may not be a spatially weighted average of the soil brightness temperature. This problem is

relevant for spaceborne measurements, where the footprint of the sensor is relatively large (tens of kilometers) and there is likely to be heterogeneity within the pixel. Test cases were run for tiled vs. homogeneous vegetation patterns using the 1dH/R model. Compared to brightnesses at 19 GHz, L-band brightness temperatures were much less sensitive to the particular distribution of vegetation within the pixel. That is, L-band signatures tended to depend only on the mean density of the vegetation [38]. This suggests that the soil moisture retrieval problem may be simplified by dissociating the spatial distribution of vegetation from radiobrightness models of the land surface, as long as the mean vegetation canopy density is known.

Spatial resolution limits

Although support for an L-band soil moisture radiometer is nearly unanimous among members of the hydrometeorology research community, there has never been a dedicated spaceborne mission [29]. One of the technical obstacles that has slowed the development of such a mission is the need for high spatial resolution capabilities, as shown in Table 1.1 [24]. As a first step, weather and climate modelers would like to achieve spatial resolution on the order of 30 km and a revisit interval of 2–3 days. Eventually, though, the dream is to develop a technology that could evolve toward 10 km (*mesoscale*) spatial resolution or better, allowing significant improvements in the accuracy of operational weather and climate forecasting. For a 21 cm wavelength instrument, this resolution requires a large steerable antenna aperture in excess of 30 m. The mission cost and risk of deploying such a system have so far proved to be prohibitive.

1.2.3 Real aperture sensors

Large real aperture radiometers at 1.4 GHz attaining 30–40 km resolutions have been proposed by several investigators. One example is a satellite imaging system called OSIRIS, which uses a deployable, 6 meter conically scanning mesh reflector antenna to mechanically

Parameter	Requirement
sensitivity	< 1K
absolute accuracy	< 3K
spatial resolution	< 30km baseline mission < 10km ideal mission
revisit time	< 3 days

Table 1.1: L-band radiometer sensor requirements for a soil moisture mission.

steer the beam across the field of view [80]. The drawback to this design is the complexity of controlling large, moving parts: a momentum wheel is needed to balance the angular momentum of the spacecraft as the reflector section rotates at 6 revolutions per minute. Also, electrical conductivity between ribs of the mesh may drift over time with thermal expansion and contraction, causing a change in emissivity [33]. This could critically affect the stability of a radiometer, which is sensitive to associated changes in antenna noise temperature.

Another concept for a high resolution mission named IRIS (Inflatable Radiometer Imaging System) uses inflatable antenna technology [21, 45]. IRIS is an L and S-band pushbroom array composed of a 25 meter inflatable offset reflector and 44 independent radiometers, with feeds arranged along a large, circular truss. While the weight and package volume of the reflector membrane is relatively low, gains in spatial sampling and resolution can only be achieved at the expense of weight added by the network of real aperture radiometers, located below the membrane.

Both OSIRIS and IRIS are based upon complicated and expensive mechanical structures that have yet to be proven in space. The more fundamental limitation of these technologies is their lack of an evolutionary path toward the desired 10 km spatial resolution of an operational sensor. Finer resolution requires a progressively larger real aperture, and eventually the mechanics of either concept become too unwieldy for further development.

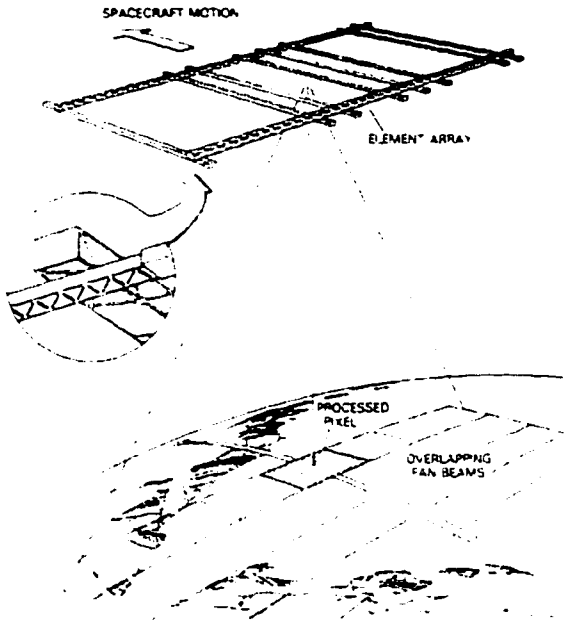


Figure 1.1: Concept for a 1-D pushbroom STAR radiometer (D. M. Le Vine *et al.* [37]).

1.3 Aperture Synthesis Technology

1.3.1 Synthetic thinned array radiometry (STAR)

Several laboratories both in the U.S. and Europe have been developing an alternative technology known as synthetic thinned array radiometry (STAR), which can attain desirable spatial resolutions without the complexity of a filled aperture system [35]. Figure 1.1 [37] shows a conceptual drawing of a pushbroom STAR instrument with one-dimensional aperture synthesis: a sparse array of "stick" antenna elements are used to synthesize a high resolution beam in the cross-track direction, while comparable resolution is generated in the along-track direction using the length of the real aperture. (1-D synthesis is also referred to as a *hybrid* system because it combines both real and synthetic aperture techniques to gain spatial resolution.) Compared to a filled array, a practical 1-D STAR sensor at L-band frequencies can be thinned by 80% while retaining the radiometric sensitivity of a real aperture radiometer.

Aperture synthesis is not a new idea. In fact, it has been used extensively in radio as-

tronomy since the 1950's to achieve high angular resolution with a large ground-based array for imaging cosmic targets [14]. A famous example is the Very Large Array (VLA) radio telescope near Socorro, New Mexico—a Y-shaped variable array of 27 high-gain paraboloid antennas spanning up to 36 km. Only in the last decade have prototype aperture synthesis radiometers been adapted to test their applicability for satellite-based observations of the Earth.

STAR consists of a number of relatively small antenna elements that are distributed in space to form a lightweight, sparse array. Figure 1.2 gives an overview of the aperture synthesis concept. Between every possible combination of receiver element pairs, correlation (multiply and integrate) operations are performed on two received signals. Separation between antennas naturally leads to a phase difference between reception of the two partially coherent signals, and this phase change will vary with the angular position of the pixels, creating an interferometric grating pattern. The ideal *visibility function* generated for a pair of STAR receivers separated by length d_n is defined as [72]

$$V(n) = \int_{FOV} T_B(\theta)\, e^{-j\pi n \sin\theta}\, d\theta, \tag{1.1}$$

where T_B is the brightness image, θ is the angular position from nadir, $n = 2d_n/\lambda$ is the separation between elements in half-wavelengths, and the integration limits are defined by the field of view (FOV) of the antenna elements. The complex exponent in (1.1) represents the even and odd grating lobe patterns of the interferometer, which become finer in resolution as d_n is increased. Physically, the integral can be interpreted as a sample of the magnitude and phase of one particular spatial frequency component in the brightness scene T_B. STAR, in this sense, acts as a spatial Fourier transform that operates on the brightness image. Conversely, a weighted inverse Fourier transform of the visibility samples will generate a reconstructed estimate of the original scene. After visibility data has been telemetered from the satellite downlink, image reconstruction can be performed on the ground where

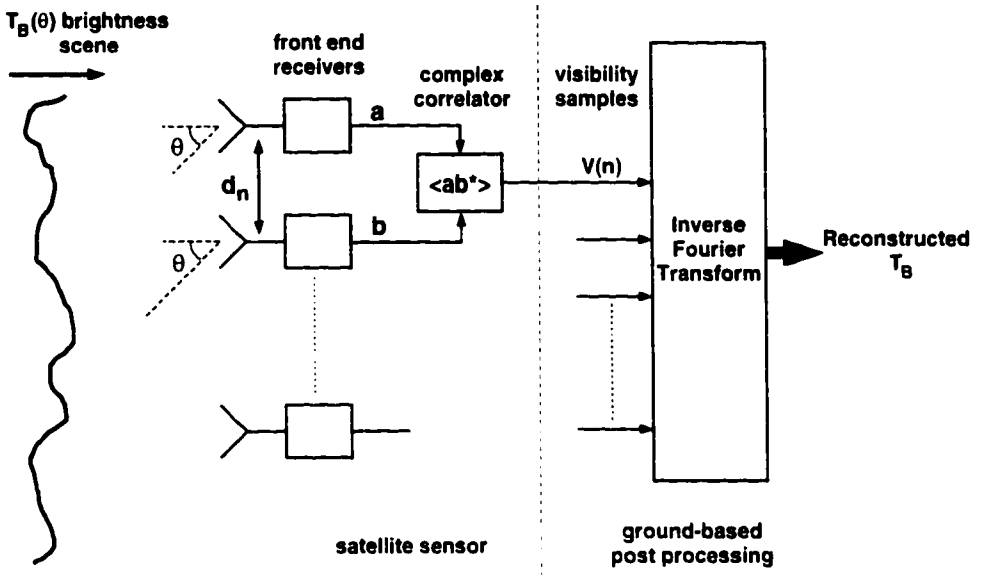


Figure 1.2: Reconstructing a radiobrightness image with STAR.

the economics of managing software complexity become much more relaxed.

1.3.2 Advantages for Earth remote sensing

Interest in STAR blossomed because of its relatively simple hardware and potential for future development. Unlike a large spinning reflector dish, a STAR instrument steers its beam electronically in post processing algorithms, making the array a static mechanical system once it is deployed. The number of receiver elements in STAR is significantly less than what is needed for a phased-array radiometer since redundant element spacings can be removed without degrading the spatial resolution. Also, the mechanical requirements for array flatness can be relaxed if the relative location of each receiver element is known (for instance, by using differential GPS) and taken into account during image reconstruction. Fewer antennas and receivers translate into significant weight and power savings for a satellite. Ruf has conducted a study showing that for a practical one-dimensional L-band STAR radiometer with 10 km resolution, the imager mass and power requirements are only 13% and 17%, respectively, of the estimates for an equivalent filled-array radiometer [58]. Array sparseness and hardware savings become even more pronounced as the maximum baseline

is increased.

1.3.3 Development of 1-D and 2-D instruments

One-dimensional STAR calibration and imaging have been tested extensively with the Electronically Steered Thinned Array Radiometer (ESTAR) [74, 36]. The University of Massachusetts developed the 1.4 GHz ESTAR prototype, which uses five horizontally polarized stick antenna elements and analog correlation circuitry. ESTAR was first deployed onto an aircraft in the early 1990's. Since then, several successful field campaigns have been conducted over watersheds in Arizona and Oklahoma. In the 1997 Southern Great Plains Hydrology Experiment, soil moisture could be estimated to within 3% of ground truth data by combining ESTAR's brightness measurements with a hydrology/radiobrightness inversion model [23].

HYDROSTAR, an L-band satellite radiometer based on the same hybrid aperture principle as ESTAR, was proposed in 1998 as a response to NASA's announcement of opportunity for an Earth System Science Pathfinder mission [12]. The baseline mission would achieve better than 30 km resolution for soil moisture mapping, using 16 stick elements spanning 9 meters in the cross-track dimension.

The next step in array thinning is to make a fully two-dimensional array which synthesizes its beam in both along and cross-track directions. Several laboratories working under the guidance of the European Space Agency (ESA) are developing a 2-D L-band aperture synthesis radiometer, shown in Figure 1.3, for the Soil Moisture and Ocean Salinity (SMOS) mission [35, 26]. According to a feasibility study for SMOS, a Y-shaped radiometer array with 80 elements and 9 m span could attain 30–50 km resolution [5]. SMOS, slated for launch in 2005, is considered a first step toward the goal of deploying a mesoscale L-band radiometer in low Earth orbit. To eventually reach 10 km resolution, a follow-on mission will likely require several hundred elements with a maximum baseline exceeding 30 m [41].

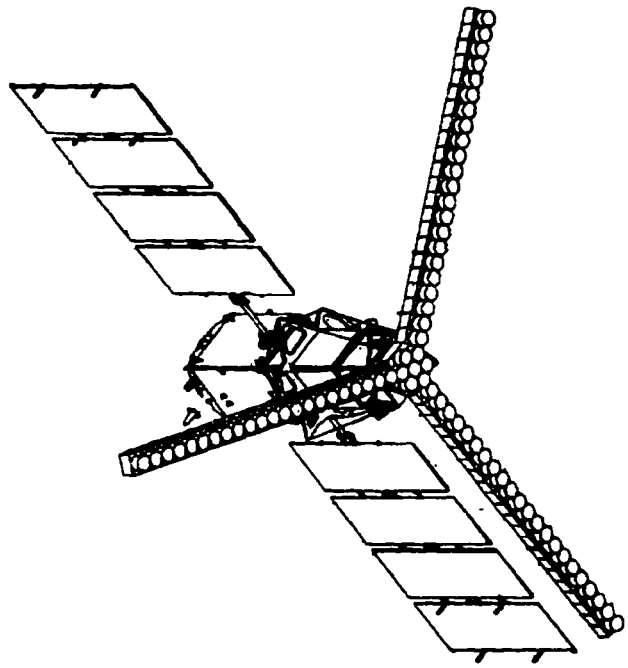


Figure 1.3: The SMOS radiometer: a 2-D configuration for aperture synthesis (Y. H. Kerr and D. M. Le Vine [26, 35]).

1.3.4 Hardware limitations

While the potential for STAR is great, its advantages are offset to some degree by the large number of independent receivers that must be locked in phase and calibrated. The packaging complexity of many discrete microwave mixers, local oscillators, and detector diodes found in a conventional superheterodyne receiver would be cumbersome to design into the array. Because the visibility measurements require running correlations between all element pairs, a constant phase relation must be maintained between all receivers. The designers of an advanced STAR are thus confronted with the task of synchronizing over 100 separate front end modules. Extending long microwave coaxial cabling over many tens of meters is not desirable because of phase changes induced by differential heating and cooling of the spacecraft, and also because complicated harnesses increase mission risk during the deployment phase.

To solve the problem with conventional receiver technology, either the radio frequency

signal demodulation should happen locally at each element, with local oscillators phase-locked to a common timing signal, or a complicated network of phase stable transmission lines must be designed to send each amplified RF signal back to a central receiver for processing. Cabling complexity becomes critical as the maximum baseline for an L-band STAR extends beyond 10 meters.

The question driving my investigation is whether a new receiver technology could be used to solve some of these issues. Is it possible to develop a technology at L-band that would yield more than 100 economical, compact, and reliable receiver modules which preserve RF phase information for beam synthesis—without needing an elaborate network of RF transmission lines?

1.4 The Direct-Sampling Digital Radiometer (DSDR)

1.4.1 Concept

In this thesis, a direct RF sampling digital radiometer (DSDR) with correlation circuitry is presented as a novel and powerful architecture for realizing the potential of STAR technology. The RF signal in DSDR is sampled and digitized immediately after the front end amplification and filtering stages so that all subsequent processing is performed digitally. An example of the direct-sampling scheme is shown in the block diagram in Figure 1.4 for the case of a single-element, total power radiometer. (The concept can also be extended to STAR applications by using two receiver channels and a digital cross-correlator.) Mixer and local oscillator components common to a superheterodyne receiver are replaced by a wideband analog-to-digital converter and relatively low speed synchronous clock. Down-conversion of the RF signal is carried out implicitly by a technique called subharmonic sampling, which exploits the discrete-time nature of A/D conversion; the band of interest can be translated down the spectrum by intentionally undersampling, and therefore aliasing, the RF carrier frequency to a lower IF or baseband frequency [79, 48].

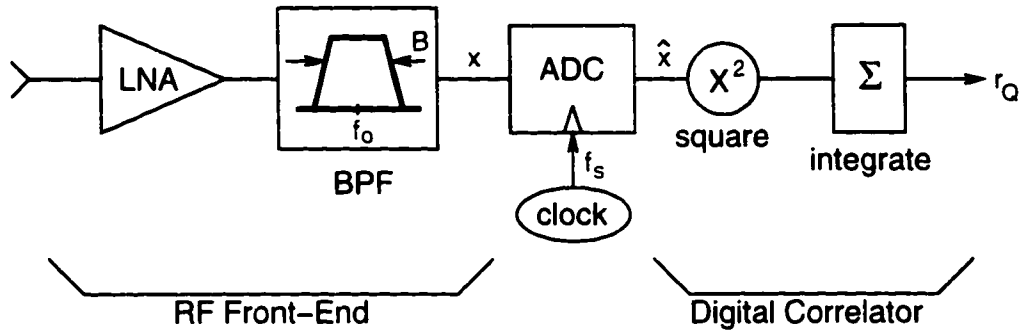


Figure 1.4: The direct RF sampling digital radiometer (DSDR), configured for total power operation.

The principal advantages of DSDR stem from the simplicity of its hardware. By eliminating components like microwave mixers and LOs, and by transferring most of the receiver's processing complexity to the digital domain, the direct-sampling method lends itself to integration onto a multi-chip module, or eventually onto a single chip MMIC. Satellite applications would reap the benefits of lower cost, weight, and packaging volume and of improved reliability from a monolithic, integrated receiver. (For radiometry in particular, a small device package would make it easier to thermally control the receiver for improved stability of the system gain.)

In a STAR instrument, microwave LO distribution signals would be superseded by DSDR's simpler, lower frequency digital clock, whose maximum frequency is defined by the operational bandwidth rather than the RF carrier frequency. This clock, operating in the 10–40 MHz range, could be distributed via fiber optic lines or perhaps even by a wireless network to each receiver element. Elimination of the mixer/LO module has the added benefit of removing sources that may re-radiate from the receiver and interfere with brightness measurements. Imperfect isolation between the RF and LO ports of a mixer can lead to this re-radiation and may manifest itself when the undesired energy is scattered off of a nearby target—for example, during a warm load calibration. But because the clock of an A/D converter is only used for latching the incoming signal and not for coupling of RF and timing signals, the converter is not inherently susceptible to leakage between ports.

DSDR is also well suited for applications requiring high phase stability: high-speed data converters and quartz oscillators typically exhibit a negligible amount of timing jitter relative to the period of an L-band carrier (500-1000 ps). For STAR, a phase-stable, digital receiver-on-a-chip located at each element of the array would offer an elegant solution, eliminating additive noise and phase errors from the network of signals distributed to a central correlator.

1.4.2 Feasibility

Analog-to-digital converter technology has improved to the point where direct RF sampling becomes feasible at the lower frequency end of the microwave spectrum.

Recently the Department of Defense has been involved in developing novel tactical communication systems that digitize early in the receiver's signal chain—at IF or RF frequencies—to realize a compact *software radio* whose band selection and demodulation scheme can be immediately reconfigured in the field [42]. Improvements in the analog input bandwidth of A/D converters in the last few years have spawned several direct-sampling applications for navigation, operating up to L-band frequencies. Brown and Wolt implemented a Global Positioning System (GPS) 1-bit direct RF sampling receiver at 1.575 GHz which could maintain the phase coherence of the carrier signal [6]. Akos and Tsui followed with the development of a multiple bit direct-sampling GPS receiver and experimented with various front end designs to minimize the noise figure [1]. In addition to these aerospace and communications applications, the microwave remote sensing community has recognized that the development of a direct-sampling digital radiometer at 1.4 GHz will become a key area of research and would be of great value for environmental applications like the mapping of soil moisture and sea surface salinity [67]. While initial successes with direct-sampling technology in communications fields are encouraging, it remained to be demonstrated whether noise and phase stability characteristics of a direct-sampling radiometer would be acceptable

for L-band STAR.

1.5 Research Objectives

1.5.1 Issues

Noise limitations

A primary goal of this work is to characterize how sources of noise in the receiver affect the radiometric precision and spatial resolution of a direct-sampling STAR sensor. A model of an L-band DSDR is developed to determine the fundamental noise floor of the receiver. With this basic theory, I can begin to ask which design parameters have the greatest influence on receiver sensitivity, and what trends can be exploited to lighten the burdens on the radiometer hardware without forfeiting performance.

Design tradeoffs

For microwave radiometry, a critical figure of merit is the noise-equivalent sensitivity (NEΔT), a measure of the smallest detectable change in the brightness level of a pixel. Clearly, NEΔT of a DSDR radiometer will be affected to some degree by errors incurred through quantization of the received brightness signal, especially at coarse quantization levels. But how many bits of conversion resolution are enough for adequate sensitivity? Referring to Table 1.1, the NEΔT requirement for retrieving soil moisture information from L-band brightness measurements is less than 1 K. Is DSDR capable of recovering brightnesses with this level of precision when the hardware is implemented onto STAR?

The bit resolution requirement in direct-sampling STAR is constrained by two factors. First, the number of bits available in the sampling head is limited by present-day A/D converter technology: bit resolution varies inversely with analog input bandwidth of the device, and, before the mid-1990's, commercially available converters extending to L-band frequencies only offered 1 or 2 bits per sample. Second, an increased number of bits will lead to a corresponding rise in power consumption and complexity of STAR hardware. For example,

the complexity of flash A/D converter circuitry increases exponentially with bit level; also, multiplication logic units and look-up tables require a greater number of gates per correlation and therefore dissipate more power as the number of quantization levels rises. These power demands will rise dramatically as STAR evolves from 1-D to 2-D synthesis, because the number of correlations increases with the square of the number of array elements. For a 30 km sensor, the added dimension increases the on-board processing requirements from 240 correlations (16 elements) to about 16,800 correlations (130 elements). It is important to understand how many bits are truly needed for these more complex STAR applications so that power consumed and heat generated by the electronics is kept within practical limits.

The ESA has proposed using a single-bit correlation scheme for the SMOS 2-D aperture synthesis radiometer to simplify the digital back end of the receivers [40]. However, because absolute power information in the apparent brightness signal is lost during a 1-bit conversion, an additional square-law detection channel is needed to calibrate the gain of each visibility sample, making the overall system more complicated [3]. Other investigations suggest that one additional bit of converter resolution would be enough to determine this gain with high precision using only digital receivers [59]. This thesis will identify some of the engineering tradeoffs between sensor precision and hardware simplicity associated with DSDR's quantization resolution.

Phase stability

The operation of STAR, which relies on many interferometers working in parallel, will be affected by the phase stability of the received signals. Sources of phase noise in DSDR—for instance, timing jitter between the sampling windows of a pair of data converters—can cause a loss of signal coherence. This *correlation loss* should be modeled and confirmed experimentally for an interferometric radiometer that uses direct-sampling. Another source of phase noise known as *fringe washing* will negatively affect STAR's performance for very

long baselines. Fringe washing arises because of the partially coherent nature of the received brightness signals. As the interferometer baseline becomes large, the time delay between two received channels may exceed the correlation time of the band limited thermal noise, depending on the how far the pixel is from the boresight direction. A loss of correlation at the edges of the brightness scene results, degrading sensitivity and resolution [8, 32]. These phase noise issues should be explored along with possible remedies.

Technology development

How could a prototype L-band DSDR radiometer be designed and tested to validate the statistical models of a direct-sampling receiver? How can the technology be assessed for readiness in remote sensing applications like soil moisture retrieval? A primary research goal is to develop a proof-of-concept DSDR sensor to characterize its capabilities for STAR and other radiometry applications.

1.5.2 Approach

Problem formulation

Ruf has previously derived general expressions for the NEΔT of an analog STAR radiometer by breaking the problem into two parts [60]: (1) solving for the noise floor of each visibility sample, and (2) calculating the noise accumulated in each pixel as all visibility samples are combined in the inverse Fourier transform. Hypothetical studies of various STAR configurations have shown that a sensitivity of 1–2 K is attainable for spaceborne L-band systems that use conventional analog hardware [34].

For STAR, noise-equivalent sensitivity is a complicated function of several variables, including the array sparseness, the number and distribution of redundant element spacings, and even the type of brightness scene. Visibility noise will depend on the value of the corresponding visibility sample and the apparent brightness temperature over the entire FOV. Therefore, in image reconstruction, the noise level in each synthesized pixel is determined

by the brightnesses of all other pixels viewed concurrently. This interdependence between pixels and the complicated noise relations that arise suggest that it is more practical to examine NEΔT for a few special cases of array configurations and brightness distributions.

DSDR will be evaluated in the context of aperture synthesis by looking at two degenerate cases in STAR: a single-element *total power DSDR* and a two-element *correlation DSDR*. The sensitivities of these instruments will be derived for particular T_B distributions and verified experimentally with working prototypes of the 1.4 GHz DSDR. Using an ideal analog radiometer architecture as a benchmark for comparison, the suitability of the direct-sampling method is assessed for advanced, high spatial resolution STAR.

Receiver statistics

The statistical properties of an analog superheterodyne receiver with square-law detector diode have been well known for many years [76]. However, the direct-sampling receiver scheme is not as well understood because of some fundamental differences in receiver statistics: random processes in the signal chain take on quantized rather than continuous values, operations are carried out in discrete-time, and carrier phase information is preserved after detection. The effects of coarse quantization on radiometric sensitivity have been investigated for some radio astronomy applications [10, 31]. But these studies concentrated on fixed converter resolutions of 3 levels or 4 levels (2 bits), and hardware prototypes performed A/D conversion at baseband or IF, not at RF frequencies.

In the DSDR problem formulation, NEΔT is derived in the most general case for arbitrary bit resolution. Analysis of the discrete-time receiver statistics will take into account the effects of RF subharmonic sampling. And central to the development of the 1.4 GHz prototype DSDR, this research will test A/D conversion technology that operates up to microwave analog input frequencies. Sensitivity is derived first for the more straightforward case of a total power DSDR and is followed by the correlation DSDR case. This work also

explores the potential advantages and implications for direct-sampling technology as STAR evolves toward 2-D synthesis applications.

Experiments

DSDR's predicted performance will be confirmed by designing and testing a pair of prototype receivers. The one and two-element DSDRs become testbeds for measuring several figures of merit. For the total power DSDR, these include dynamic range and noise-equivalent sensitivity. For the correlation DSDR, the specifications are visibility noise, fidelity of the visibility grating lobe pattern, phase stability in the A/D sampling head, and fringe washing degradation.

Design philosophy

The DSDR hardware and software developed in this project serve dual purposes: one is the evaluation of the DSDR concept; the other is construction of a final L-band radiometer product for Radiobrightness and Energy Balance Experiments (REBEX) conducted within our research group. The design philosophy adopted to accomplish these goals is an amalgam of several issues, including: lessons learned from our previous radiometer designs; the desire to gain experience with the latest device technologies; a need for expandable, reconfigurable hardware; and outsourcing strategies to lighten the scheduling burden. In this thesis, development of DSDR will be presented chronologically, starting from the benchtop total power radiometer, to the implementation of a mobile truck platform for field evaluation, to the two element correlation DSDR.

Fringe washing remedy

To address fringe washing, a novel correlation receiver technique will be developed and simulated (on a computer) in anticipation of problems that could arise as STAR dimensions become very large.

1.6 Thesis Organization

In Chapter 2, the theoretical receiver statistics for a total power DSDR will be developed to gain an understanding of which design parameters most affect radiometric sensitivity. The statistical model of DSDR is extended to the case of a two-element correlation radiometer in Chapter 3, where expressions for NEΔT and correlation loss will be derived. A novel band-slicing correlation technique is also developed to counteract the fringe washing phenomenon in STAR. Chapter 4 outlines the hardware and software design for the first 1.4 GHz total power DSDR, including the implementation of the field-grade radiometer and truck system. Chapter 5 describes the design of a second, improved DSDR receiver module and its configuration with the first receiver as a correlation DSDR. Finally, in Chapter 6, I will build upon the results from previous chapters to discuss the applicability of DSDR for aperture synthesis and to suggest future research directions.

CHAPTER 2

Sensitivity of a Direct-Sampling Digital Radiometer (DSDR)

2.1 Purpose

In this chapter, I will develop the statistical model for a single channel L-band DSDR and derive a general expression for NEΔT. The sensor considered here performs a *self-correlation*, or power estimate, of the band limited brightness signal and thus operates as a total power radiometer.

Digital correlation radiometry dates back several decades, when radio astronomers recognized that digital computer functions could replace complicated and often unstable microwave hardware used in radio receivers. In 1961, Weinreb developed a single-bit (two level) digital radiometer for autocorrelation spectroscopy [78]. In this design, the downconverted signal is digitized at baseband, split into two channels, and correlated for a number of delay times—with delays generated by a series of D-type flip-flops. The resulting autocorrelation function could then be Fourier transformed via computer to find the power spectrum of the original source. This technique offered a stable and affordable way of achieving a variable filter bank in spectroscopy using only digital hardware and software. And theoretically, quantization noise added by the 1-bit conversion only increased the rms noise level by a factor of $\pi/2$, relative to an analog correlator. Experience showed that the practical advantages of the simpler hardware outweighed this rather small loss in sensitivity.

Other investigators have modeled and developed multi-bit correlators for both spec-

troscopy and interferometry. In 1973, Hagen *et al.* derived the signal-to-noise ratio (SNR) for digital correlators using 3 or 4 quantization levels, which offered improved sensitivities and shorter integration time requirements compared to a 1 bit correlator [19]. In the mid-1980's, D'Addario *et al.* analyzed some non-ideal effects arising in radio interferometers that use a 3-level complex correlator: these effects include indecision region errors, non-zero aperture time exhibited by data converters, and timing skew between receivers.

There is an important distinction between the design requirements for radio astronomy applications and for future Earth remote sensing applications. Digital correlator resolutions of 1–2 bits were acceptable for astronomy, where spectroscopy (autocorrelation) or interferometry (cross-correlation) functions were desired. Greater bit resolutions were not needed for recovering the absolute noise level of the received signal, as the net antenna temperature is generally a constant which is not of interest in radio astronomy. However, in Earth-orbiting STAR, both absolute power and interferometric measurements are needed. If all processing in an advanced STAR instrument is performed digitally, the coarse resolution used in the past in radio telescope designs will probably need to be improved beyond 2 or 3 quantization levels. My investigation begins by looking at the case of a total power DSDR and asking how precisely this digital receiver can estimate noise power.

The radio astronomy studies described above have considered only a few particular quantization schemes with sampling at baseband or IF frequencies. I will derive a more general NEΔT expression for a total power DSDR having arbitrary bit resolution, sampling rate, and receiver bandpass characteristics. Non-ideal effects caused by drifting threshold levels in the A/D converter are also considered. This derivation will take into account the unique requirements of a practical direct-sampling receiver at L-band frequencies, with its limited bit resolution and input bandwidth, and with a low clock rate that significantly undersamples the carrier frequency.

2.2 Direct-Sampling Architecture

The signal flow in a total power DSDR is analyzed by referring back to Figure 1.4. DSDR generates a detected output signal r_Q which represents the estimated noise temperature generated by both antenna and receiver noise components. The receiver is composed of three main sections: an RF front end, which amplifies and filters the analog RF signal before it is sampled; the A/D converter; and the digital correlator, which performs a self-correlation (square and integration) in the case of a total power sensor. The narrow band, zero-mean signal $x(t)$ has a center frequency f_0, a bandwidth B, and is sampled at a rate f_s. By choosing $f_s \ll f_0$, the RF band of interest is translated down in frequency through subharmonic sampling.

It should be mentioned that subharmonic sampling has caused difficulties in the development of direct-sampling technology for some communications applications, where the signal of interest originates from a coherent, human-made source. Out-of-band noise can be aliased into the IF band and degrade the receiver performance. Also timing jitter in the sampling clock can potentially add excessive amounts of noise to the original signal. But in radiometry, where the signal $x(t)$ is only partially coherent, and where the objective is to estimate the mean power rather than to reconstruct the original signal, some receiver design considerations can be relaxed without sacrificing performance. Sampling jitter is not an issue for a total power DSDR because the mean-squared value of x can be recovered without knowing its phase. And while there is aliasing of out-of-band noise, it will be shown that at L-band frequencies it is possible, through careful design of the bandpass filter sections, to bring these noise levels below the intrinsic receiver noise temperature.

As a test case, the sensitivity of an L-band DSDR will be evaluated for $f_0 = 1.41$ GHz and $B = 20$ MHz (within the protected radio astronomy band) and for a typical system noise temperature of 400 K (viewing a natural surface). The bit resolution is estimated given

the commercial specifications for a flash A/D converter having a small-signal bandwidth of 1.4 GHz.

2.3 Receiver Statistics

2.3.1 Quantization bias

An analysis of NEΔT is approached first by examining DSDR's sensitivity to changes in the bias characteristics of the A/D conversion. The narrow-band noise source $x(t)$ is modeled as a zero-mean Gaussian random process having a variance σ^2. Its probability density function (pdf) is then

$$p(x) = \frac{1}{\sqrt{2\pi}\sigma} e^{-x^2/2\sigma^2}. \tag{2.1}$$

The nth value output by the A/D converter is

$$\hat{x}_n = Q[x(t_n)], \tag{2.2}$$

where Q describes the infinite staircase transfer function having a discretization step v_0 (Figure 2.1). and t_n is the sampling time [1]. The normalized signal strength is defined as

$$s = \sigma / v_0. \tag{2.3}$$

Although signal $x(t)$ has an infinite voltage range in theory. practically all of the samples will fall within a range of 6σ (Figure 2.2). So the concept of an *effective number of digitization levels* is introduced:

$$\text{levels of digitization} = 6s = 2^w. \tag{2.4}$$

where w represents the number of bits. (See also Section 3.1.5 for a discussion of the effective number of bits in DSDR and its relation to the performance of a finite, fixed-bit converter.)

[1] It is assumed in modeling the quantization transfer function that the mean value of the sampled waveform $\hat{x}$ is zero. For the actual receiver implementation, neither x nor $\hat{x}$ are necessarily zero-mean variables, but the bias can be computed and subtracted out in the digital processing. (In effect, DSDR calculates the variance of the quantized waveform.) The transfer function shown in Figure 2.1 has already taken this subtraction operation into account.

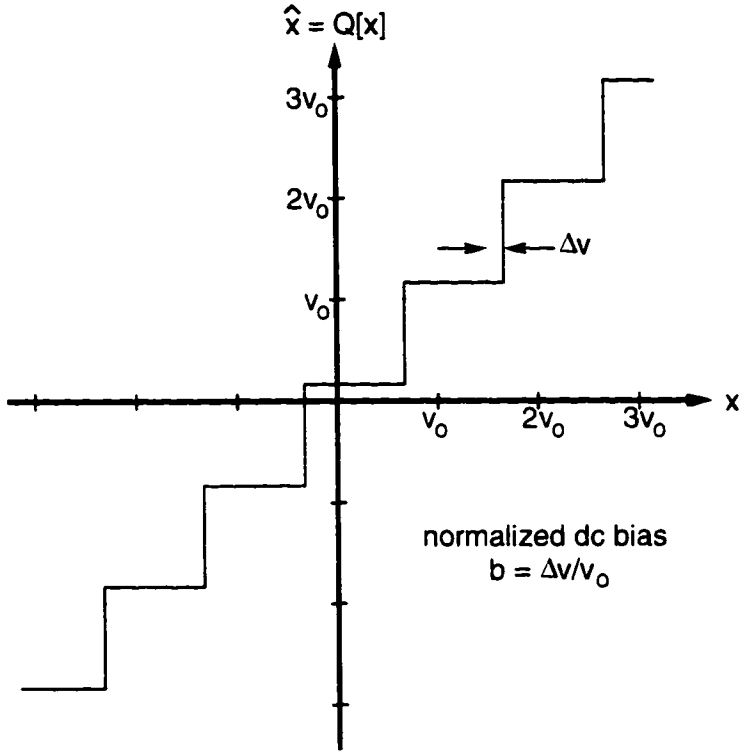


Figure 2.1: Quantization transfer function of the A/D converter. The infinite staircase represents the effective response after biases have been removed from the input and output.

With commercially available flash A/D converter technology, quantization resolutions of at least 4.5 levels (2.2 bits) are possible at 1.4 GHz [65].

Let Δv be the voltage difference between the mean value of x and one of the midpoints of the $Q[x]$ staircase. Without any loss of generality, Δv can be limited to the range from $-v_0/2$ to $+v_0/2$. Let the *normalized dc bias* of the input signal be defined as

$$b = \Delta v / v_0, \quad -1/2 \leq b \leq 1/2. \tag{2.5}$$

If the normalized bias b were to change over time, then pdf of $\hat{x}$ will also change, which in turn could induce an error signal in r_Q and degrade the radiometer's sensitivity.

The effect of dc bias drift is examined by first considering the correlator output signal, which is just the mean-square of N samples over some integration time,

$$r_Q = \frac{1}{N} \sum_{n=1}^{N} \hat{x}_n^2. \tag{2.6}$$

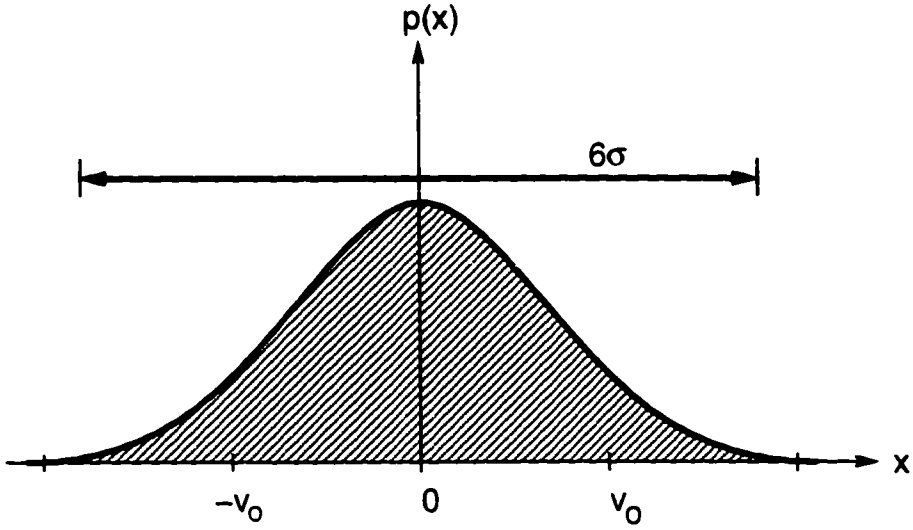


Figure 2.2: Effective range of a Gaussian distributed signal.

Then the signal-to-noise ratio of the detect output is given by

$$SNR_L = \langle r_Q \rangle / \sigma_L = T'_{SYS} / \Delta T_L, \tag{2.7}$$

where σ_L is the standard deviation of r_Q, T'_{SYS} is the total system noise temperature, and ΔT_L is the noise-equivalent sensitivity limited by random fluctuations in dc bias. The expected value of r_Q in (2.7) can be determined by first expressing the pdf of the quantized samples:

$$p(\hat{x}) = \sum_{i=-\infty}^{\infty} W_i \delta[\hat{x} - v_0(i+b)], \tag{2.8a}$$

where the probability weight W_i for each quantized cell is,

$$W_i = \int_{v_0(i+b-1/2)}^{v_0(i+b+1/2)} p(x)dx = \frac{1}{2}\left[\mathrm{erf}\left(\frac{i+b+1/2}{\sqrt{2}s}\right) - \mathrm{erf}\left(\frac{i+b-1/2}{\sqrt{2}s}\right)\right]. \tag{2.8b}$$

Therefore the expected output signal is

$$\langle r_Q \rangle = \frac{v_0^2}{2} \sum_{i=-\infty}^{+\infty} (i+b)^2 \left[\mathrm{erf}\left(\frac{i+b+1/2}{\sqrt{2}s}\right) - \mathrm{erf}\left(\frac{i+b-1/2}{\sqrt{2}s}\right)\right]. \tag{2.9}$$

Suppose that a radiometer could be designed with infinite quantization resolution ($s = \infty$). Then the expected output is just the variance of the Gaussian process in (2.1):

$$\langle r_\infty \rangle = \langle x^2 \rangle = \sigma^2. \tag{2.10}$$

Now let $\langle r \rangle_e$ be defined as the difference (error) between the expected values of the finite and infinite resolution outputs:

$$\langle r \rangle_e = \langle r_Q \rangle - \langle r_\infty \rangle. \tag{2.11}$$

Substituting (2.9) and (2.10) into (2.11), and dividing both sides by v_0^2,

$$\frac{\langle r \rangle_e}{v_0^2} = \frac{1}{2} \sum_{i=-\infty}^{+\infty} (i+b)^2 \left[\mathrm{erf}\left(\frac{i+b+1/2}{\sqrt{2}s} \right) - \mathrm{erf}\left(\frac{i+b-1/2}{\sqrt{2}s} \right) \right] - s^2. \tag{2.12}$$

Figure 2.3 shows a plot of the above function for all unique bias levels. The expected output is extremely sensitive to changes in dc bias when there are fewer than 3 digitization levels. On the other hand, as the relative signal increase beyond 3-4 quantization levels, $\langle r \rangle_e$ approaches a constant value of $v_0^2/12$. This value represents the noise floor limit of the quantization process. Consider that for very large s, $p(x)$ is approximately uniform within the range of each quantization bin,

$$v_0(i+b-1/2) \leq x \leq v_0(i+b+1/2), \tag{2.13}$$

for any integer i. The A/D converter assigns a digitized value of

$$\hat{x} = v_0(i+b), \tag{2.14}$$

which is midway between the upper and lower thresholds of the bin. The quantized signal can be thought of as the sum of the analog input and an error signal x_e,

$$\hat{x} = x + x_e. \tag{2.15}$$

Then this error signal must be a zero-mean, uniformly distributed random variable which can vary from $-v_0/2$ to $+v_0/2$. The variance of x_e is easily shown to be

$$\langle x_e^2 \rangle = \frac{1}{v_0} \int_{-\frac{v_0}{2}}^{+\frac{v_0}{2}} x_e^2 dx_e = \frac{v_0^2}{12}, \tag{2.16}$$

which represents the quantization noise added by the data converter in the large signal limit.

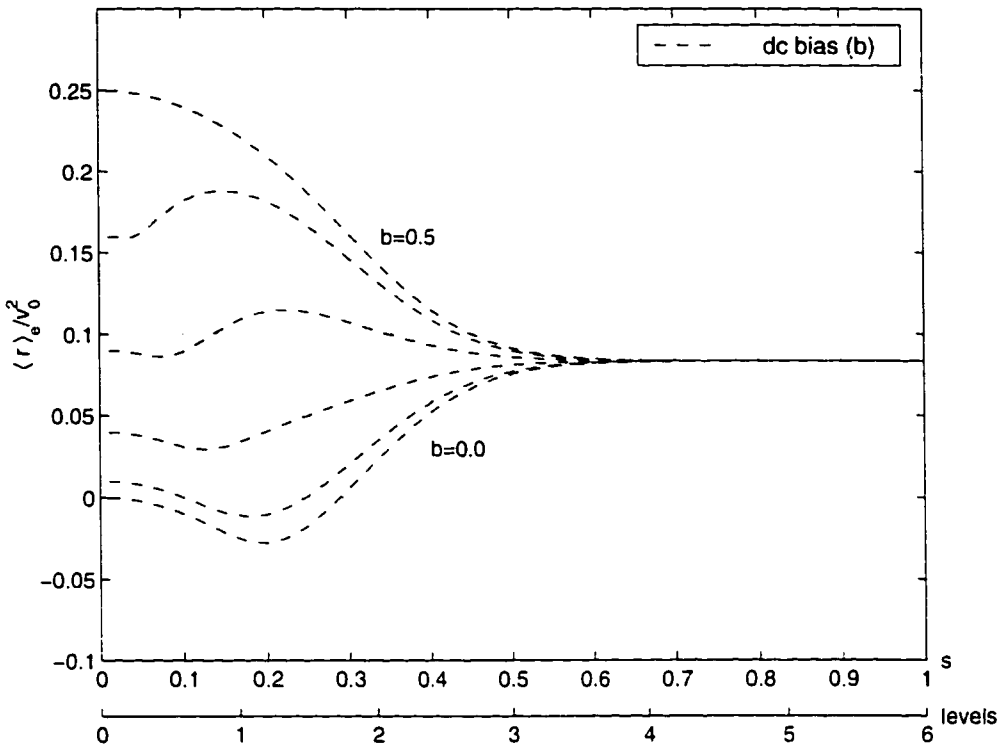


Figure 2.3: Digital correlation error as a function of dc bias (b) and quantization level ($6s$).

The radiometric sensitivity will be derived for the case where the input power is sufficiently large such that

$$\langle r \rangle_e \approx v_0^2/12 \tag{2.17}$$

is a good approximation. It is clear from Figure 2.3 that (2.17) is valid for a resolution greater than 4 digitization levels, or 2 bits of resolution, which will be referred to hereon as the *large signal approximation*:

$$s > 2/3 \quad (> 4 \text{ levels of digitization}). \tag{2.18}$$

To practically realize this large signal limit, a total power radiometer could, for example, be designed with enough gain so that (2.18) is satisfied by amplification of the receiver noise alone. Or noise injection could be applied at the front end to set the A/D input at some constant value greater than 4 levels. Regardless of the technique used, it will be assumed here that the radiometer operates ideally, with no gain fluctuations, in total power mode

and that the input noise level is high enough to satisfy the approximation in (2.17).

In the worst case, the normalized dc bias could have any fixed value over the range $0 \leq b \leq 1/2$ during a brightness measurement. The function f_L is defined to quantify the maximum uncertainty of the correlator output:

$$f_L(s) = \frac{\langle r \rangle_e(s, b = 1/2) - \langle r \rangle_e(s, b = 0)}{v_0^2}. \tag{2.19}$$

This *uncertainty function* is plotted in Figure 2.4 using the result in (2.12). If a set of independent radiometric measurements $\{r_{Q1}, r_{Q2}, \dots\}$ are assumed to be uniformly distributed over the range of uncertainty, $v_0^2 f_L(s)$, then σ_e, the standard deviation of $\langle r \rangle_e$, can be found using the similar formulation in (2.16), yielding

$$\sigma_e = \frac{v_0^2 f_L(s)}{2\sqrt{3}}. \tag{2.20}$$

In the actual receiver hardware, the variation in r_Q would probably be less than (2.20); dc bias drift in a well designed A/D sampler would be considerably less than the typical voltage of one quantization bin (about $v_0 = 15$ mV for an L-band flash converter). Nevertheless, the above simplification helps in assigning a worst case limit to the dc-bias induced NEΔT.

An estimate for $\langle r_Q \rangle$ is obtained by substituting (2.10) and (2.17) into (2.11):

$$\langle r_Q \rangle \approx \sigma^2 + v_0^2/12. \tag{2.21}$$

Since in (2.11) the value of $\langle r_\infty \rangle$ is constant, it follows that $\langle r \rangle_e$ and $\langle r_Q \rangle$ must have the same standard deviation. Therefore

$$\sigma_L = \frac{v_0^2 f_L(s)}{2\sqrt{3}}. \tag{2.22}$$

and the SNR due to dc bias drift is

$$\frac{T'_{SYS}}{\Delta T_L} = \frac{2\sqrt{3}}{f_L(s)} \left(s^2 + \frac{1}{12} \right). \tag{2.23}$$

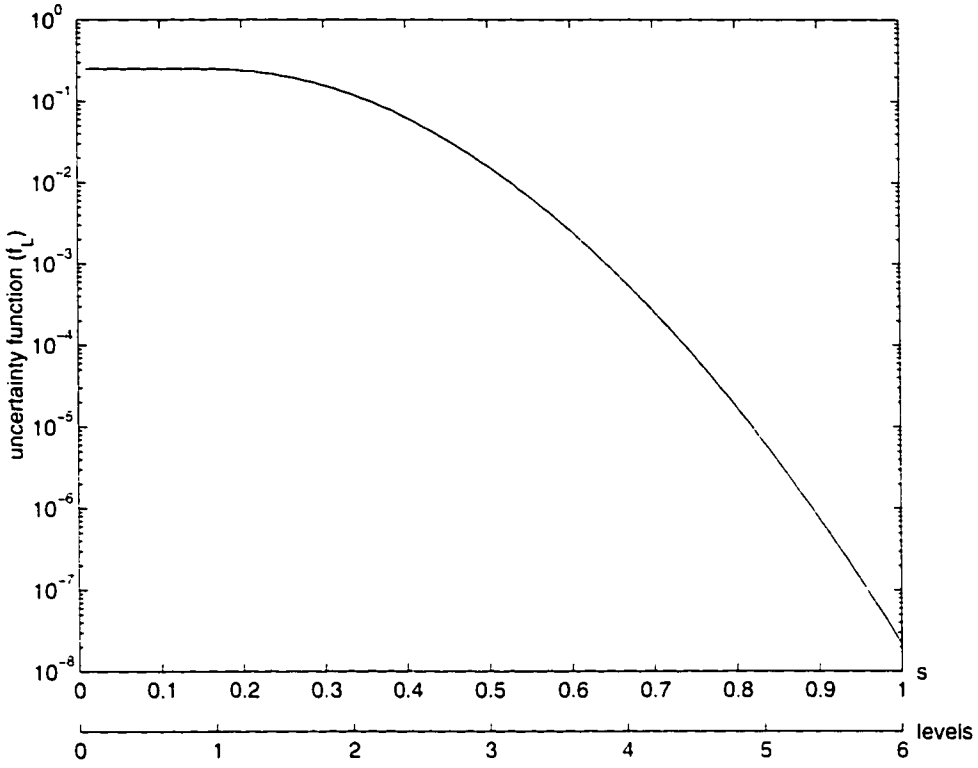


Figure 2.4: Uncertainty in the digital correlator detect output.

T'_{SYS} includes noise from the antenna and analog receiver (T_{SYS}) and quantization noise introduced by the data converter (T_Q):

$$T'_{SYS} = T_{SYS} + T_Q. \tag{2.24}$$

The two components can be expressed as the ratio of noise power before sampling to noise added during quantization:

$$\frac{T_{SYS}}{T_Q} = \frac{\sigma^2}{v_0^2/12}. \tag{2.25}$$

Therefore

$$T'_{SYS} = T_{SYS}\left(1 + 1/12s^2\right). \tag{2.26}$$

and after combining (2.23) and (2.26), the sensitivity is

$$\Delta T_L = T_{SYS} \cdot \frac{f_L(s)}{2\sqrt{3}s^2}. \tag{2.27}$$

For the test case radiometer with a sampling range of 4.5 digitization levels ($s = 0.75$), the dc bias uncertainty function has a value of $f_L = 7 \times 10^{-5}$. Setting $T_{SYS} = 400$ K, ΔT_L is on the order of 0.01 K, which is generally much smaller than other components of NEΔT in a radiometer.

2.3.2 Finite sampling

In the previous section, the digital detect output r_Q was expressed in terms of its *expected value*—and that can only be obtained after an infinite number of samples have been accumulated. Because the signal bandwidth and integration time of any practical radiometer will be finite, these parameters must also be incorporated into the overall NEΔT expression.

Mean and standard deviation of the correlator output

Just as SNR was defined for dc bias drift, it can also be formulated to account for the finite nature of the time-bandwidth product:

$$SNR_F = \langle r_Q \rangle / \sigma_F = T'_{SYS} / \Delta T_F, \tag{2.28}$$

where σ_F is the standard deviation of r_Q and ΔT_F is the sensitivity. The signal and noise components can be solved using an approach similar to the one developed by Thompson *et al.* [75] but extended to the case of a quantized waveform. ΔT_F is derived assuming the large signal condition in (2.18).

The variance of the correlator output signal is

$$\sigma_F^2 = \langle r_Q^2 \rangle - \langle r_Q \rangle^2. \tag{2.29}$$

$\langle r_Q \rangle$ is already known from (2.21). The expected value of r_Q^2 is solved by first plugging in the definition from (2.6):

$$\langle r_Q^2 \rangle = \frac{1}{N^2} \sum_{n=1}^{N} \langle \hat{x}_n^4 \rangle + \frac{1}{N^2} \sum_{n=1}^{N} \sum_{\substack{m=1 \\ m \neq n}}^{N} \langle \hat{x}_n^2 \hat{x}_m^2 \rangle. \tag{2.30}$$

Using the pdf in (2.8), the fourth moment of $\hat{x}$ can be found.

$$\langle \hat{x}_n^4 \rangle = \langle \hat{x}^4 \rangle = \frac{v_0^4}{2} \sum_{i=-\infty}^{+\infty} (i+b)^4 \left[\mathrm{erf}\left(\frac{i+b+1/2}{\sqrt{2}s} \right) - \mathrm{erf}\left(\frac{i+b-1/2}{\sqrt{2}s} \right) \right]. \tag{2.31}$$

From (2.31), it is difficult to tell immediately how the signal level s relates to this fourth moment term. To simplify things, consider an error term which is defined as the difference between quantized and unquantized moments:

$$\langle x^4 \rangle_e = \langle \hat{x}^4 \rangle - \langle x^4 \rangle. \tag{2.32}$$

The fourth moment of x is just

$$\langle x^4 \rangle = \int_{-\infty}^{+\infty} x^4 p(x) dx = 3\sigma^4. \tag{2.33}$$

Combining (2.31)-(2.33) and dividing both sides by v_0^4, the normalized fourth moment error is

$$\frac{\langle x^4 \rangle_e}{v_0^4} = \frac{1}{2} \sum_{i=-\infty}^{+\infty} (i+b)^4 \left[\mathrm{erf}\left(\frac{i+b+1/2}{\sqrt{2}s} \right) - \mathrm{erf}\left(\frac{i+b-1/2}{\sqrt{2}s} \right) \right] - 3s^4. \tag{2.34}$$

A plot of the fourth moment error is shown over the range of possible dc bias levels in Figure 2.5. Notice that for more than 4 levels of digitization, $\langle x^4 \rangle_e$ is insensitive to changes in dc bias. Since the large signal condition is assumed *a priori*, it is useful to find an estimate for (2.34) in the limit as s becomes large.

Recall from Section 2.3.1 that when the input signal becomes much larger than v_0, the quantization error signal x_e behaves like a zero-mean, uniform random variable which is also independent of x. Therefore, applying the relation in 2.15,

$$\langle \hat{x}^4 \rangle \approx \langle x^4 \rangle + 6\langle x^2 \rangle \langle x_e^2 \rangle + \langle x_e^4 \rangle. \tag{2.35}$$

Substituting (2.10), (2.16), and (2.35) into (2.32),

$$\langle x^4 \rangle_e = \sigma^2 v_0^2/2 + \langle x_e^4 \rangle. \tag{2.36}$$

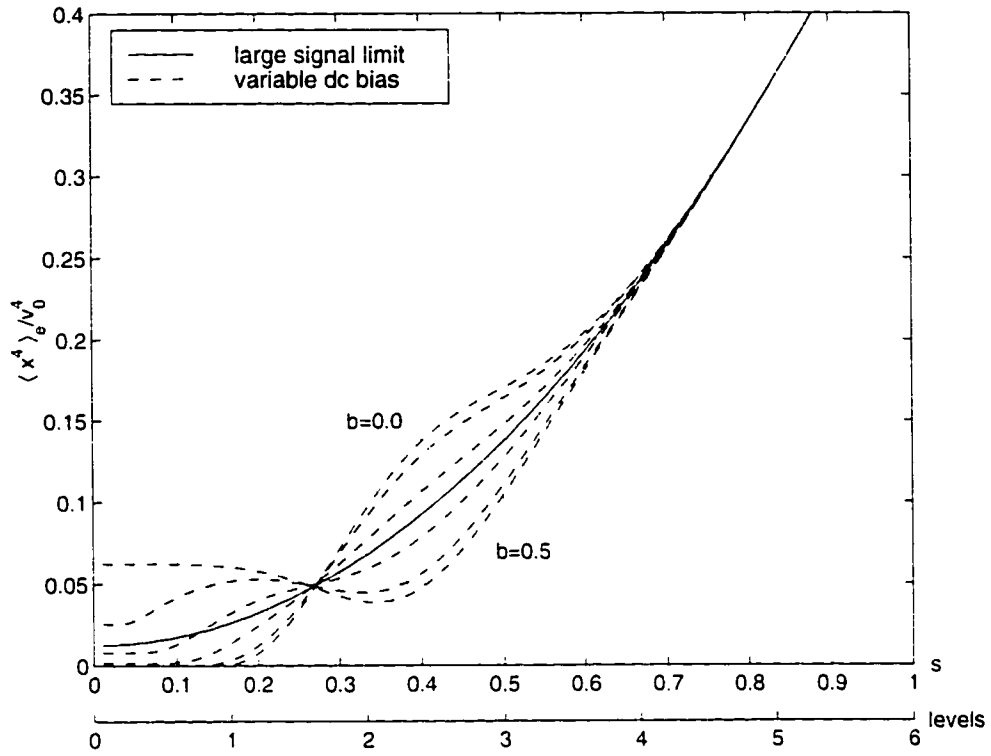


Figure 2.5: Fourth moment quantization error.

where the fourth moment of the quantization error signal is

$$\langle x_e^4 \rangle = \frac{1}{v_0} \int_{-\frac{v_0}{2}}^{+\frac{v_0}{2}} x_e^4 dx_e = v_0^4/80. \tag{2.37}$$

Plugging the result from (2.37) back into (2.36) and dividing both sides by v_0^4 yields

$$\langle x^4 \rangle_e / v_0^4 = s^2/2 + 1/80. \tag{2.38}$$

which is the large signal approximation for (2.34). This estimate is plotted in Figure 2.5 along with the exact solution: as expected, when the input signal exceeds 4 levels of digitization, (2.38) becomes a good approximation.

The fourth moment of the quantized signal can now be solved by substituting (2.33) and (2.38) into (2.32):

$$\langle \hat{x}^4 \rangle = v_0^4 \left(3s^4 + s^2/2 + 1/80\right). \tag{2.39}$$

The 1/80 term in parenthesis is negligible for large signals and can be filtered out:

$$\langle \hat{x}^4 \rangle \approx 3\sigma^4 + v_0^2\sigma^2/2. \tag{2.40}$$

Next, an expression for the second summation in (2.30) is developed. The expected value of the $\hat{x}$ cross products can be estimated using the Gaussian moment factoring relation [81]:

$$\langle \hat{x}_n^2 \hat{x}_m^2 \rangle = \langle \hat{x}_n^2 \rangle \langle \hat{x}_m^2 \rangle + 2\langle \hat{x}_n \hat{x}_m \rangle^2. \tag{2.41}$$

where $\langle \hat{x}_n^2 \rangle$ and $\langle \hat{x}_m^2 \rangle$ are already known from (2.21).

The A/D converter sampling rate can be written as $f_s = 2\gamma B$, where γ is an oversampling factor relative to the Nyquist rate. Then the time interval between samples is

$$\Delta t = \frac{1}{2\gamma B}. \tag{2.42}$$

and the normalized autocorrelation of $\hat{x}$ is

$$R_F(q\Delta t) \approx \frac{\langle \hat{x}_n \hat{x}_m \rangle}{\sigma^2 + \frac{v_0^2}{12}} \tag{2.43}$$

where $q = |n - m|$ represents the spacing between samples n and m. Then (2.41) can be rewritten in terms of the autocorrelation function of the digitized waveform:

$$\langle \hat{x}_n^2 \hat{x}_m^2 \rangle = \left(\sigma^2 + \frac{v_0^2}{12}\right)^2 \left[1 + 2R_F^2(q\Delta t)\right]. \tag{2.44}$$

The results from (2.21), (2.30), (2.40), and (2.44) are substituted back into (2.29), yielding

$$\sigma_F^2 = \frac{2\sigma^4}{N}\left[1 + \frac{1}{6s^2} + \frac{1}{N}\left(1 + \frac{1}{12s^2}\right)^2 \sum_{n=1}^{N}\sum_{\substack{m=1 \\ m\neq n}}^{N} R_F^2(q\Delta t)\right]. \tag{2.45}$$

The solution for R_F is first approached by finding a closed-form expression for R_∞, the autocorrelation function for the infinite resolution case.

$$R_\infty(q\Delta t) = \lim_{s\to\infty} R_F(q\Delta t) = \frac{\langle x_n x_m \rangle}{\sigma^2}. \tag{2.46}$$

From the Wiener-Khinchin relations, the autocorrelation function and the power spectral density of a random process are related through Fourier transforms [50]. If a rectangular

bandpass response is assumed for the front end, then the power spectral density of $x(t)$ would be

$$|X(f)|^2 = \begin{cases} 1 & \text{for } f_0 - \frac{B}{2} \leq |f| \leq f_0 + \frac{B}{2} \\ 0 & \text{otherwise} \end{cases} . \tag{2.47}$$

Therefore the normalized autocorrelation function of x can be found by taking the inverse Fourier transform of the power spectrum:

$$F^{-1}\left\{|X|^2\right\} \sim R_x(t) = \text{sinc}\,(Bt)\cos\,(2\pi f_0 t). \tag{2.48}$$

The solution for the autocorrelation of the digitized signal $\hat{x}$ is not as simple to derive analytically. The non-linear nature of quantization introduces energy at frequencies that are outside of the original band defined in (2.47), making it difficult to characterize the waveform without the use of numerical techniques.

Analog versus digital correlation

The true (analog) correlation of two jointly Gaussian distributed waveforms can be mapped to the digitized correlation using an approach developed previously by Cooper [10] for a 4-level correlator. I will extend this mapping technique to the case of arbitrary bit resolution and combine it with (2.48) to calculate R_F numerically.

The normalized cross-correlation of two infinite resolution, jointly Gaussian signals is defined as

$$\rho = \frac{\langle xy \rangle}{\langle x^2 \rangle}. \tag{2.49}$$

where y is also a zero-mean random process with variance σ^2. Similarly, the normalized cross-correlation of the quantized signals is

$$\rho_Q = \frac{\langle \hat{x}\hat{y} \rangle}{\langle \hat{x}^2 \rangle}. \tag{2.50}$$

The objective is to find the transfer function between ρ and ρ_Q over the range $-1 \leq \rho \leq 1$.

Expansion of the numerator in (2.50) yields

$$\langle \hat{x}\hat{y} \rangle = \sum_{i=-\infty}^{+\infty} \sum_{k=-\infty}^{+\infty} v_0^2 (i+b)(k+b) \int_{v_0(k+b-1/2)}^{v_0(k+b+1/2)} \int_{v_0(i+b-1/2)}^{v_0(i+b+1/2)} p(x,y)dxdy \tag{2.51}$$

where $p(x,y)$ is the bivariate pdf for two jointly Gaussian random variables [70],

$$p(x,y) = \frac{1}{2\pi\sigma^2\sqrt{1-\rho^2}} \exp\left[-\frac{x^2+y^2-2\rho xy}{2\sigma^2(1-\rho^2)}\right]. \tag{2.52}$$

After making a substitution of variables, (2.50) can be written in the form

$$\rho_Q = \frac{\sum_{i=-\infty}^{+\infty} \sum_{k=-\infty}^{+\infty} (i+b)(k+b) I_{ik}}{\pi \sum_{i=-\infty}^{+\infty} (i+b)^2 M_i}, \tag{2.53a}$$

where

$$I_{ik} = \frac{1}{\sqrt{1-\rho^2}} \int_{\frac{k+b-1/2}{s}}^{\frac{k+b+1/2}{s}} \int_{\frac{i+b-1/2}{s}}^{\frac{i+b+1/2}{s}} \exp\left[-\frac{x^2+y^2-2\rho xy}{2(1-\rho^2)}\right] dxdy \tag{2.53b}$$

$$M_i = \mathrm{erf}\left(\frac{i+b+1/2}{\sqrt{2}s}\right) - \mathrm{erf}\left(\frac{i+b-1/2}{\sqrt{2}s}\right). \tag{2.53c}$$

which describes the relation between ρ_Q and ρ for any signal level and dc bias. In general, there is no closed-form expression for I_{ik}, and the integral in (2.53b) must be evaluated numerically.

The sensitivity of ρ_Q to the dc bias term b decreases rapidly as the signal increases past 4 digitization levels. In fact, at the 4.5 level benchmark, ρ_Q fluctuates less than 15 ppm over the range $0 \le b \le 1/2$. To simplify things, the bias is arbitrarily set to $b = 0$ so that the following symmetric properties apply:

$$I_{ik} = I_{(-i)(-k)} \tag{2.54a}$$

$$M_i = M_{(-i)}. \tag{2.54b}$$

Therefore in the large signal limit,

$$\rho_Q \approx \frac{\sum_{i=1}^{\infty} \sum_{k=1}^{\infty} ik \left[I_{ik} - I_{i(-k)}\right]}{\pi \sum_{i=1}^{\infty} i^2 M_i} \quad \text{for } b = 0. \tag{2.55}$$

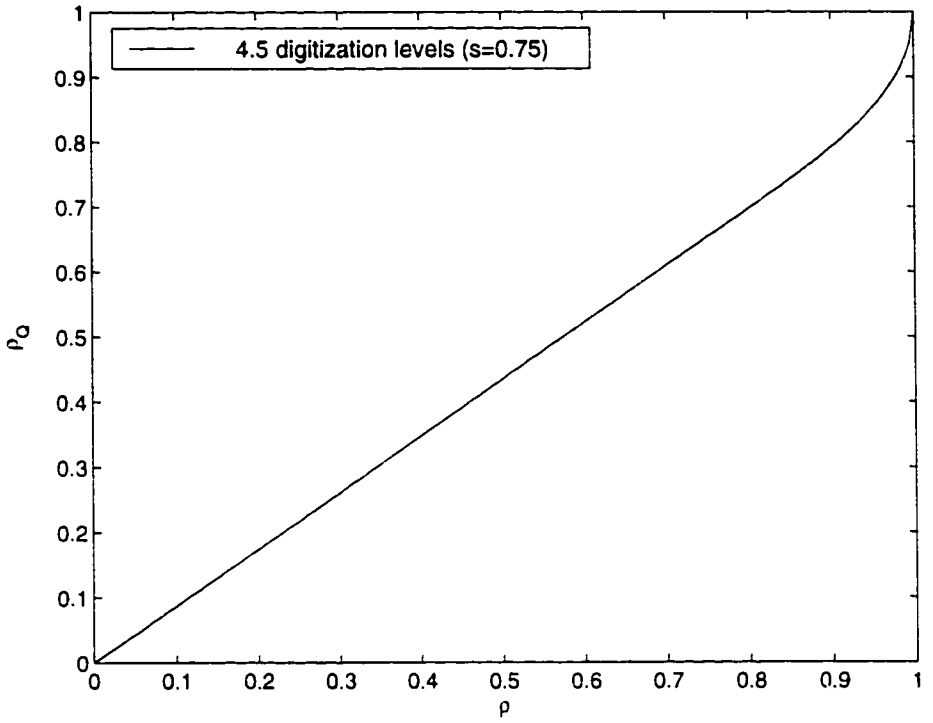


Figure 2.6: Transfer function between analog and digital correlation.

Figure 2.6 shows the relation between ρ_Q and ρ at 4.5 levels. The autocorrelation function is just a special case of a cross-correlation, with $y(t)$ equal to a time-delayed version of $x(t)$. Therefore R_F can be calculated by mapping (2.48) to corresponding values generated by (2.55).

Infinite series approximation

The double summation in (2.45) can be simplified now that the behavior of R_F is better understood. Suppose that a set of N quantized samples are measured, $\{\hat{x}_1, \hat{x}_2, \ldots, \hat{x}_N\}$. For each integer q, there are $2(N-q)$ possible combinations of the cross-product $\hat{x}_i\hat{x}_k$, therefore [75]

$$\sum_{n=1}^{N}\sum_{\substack{m=1\\m\neq n}}^{N} R_F^2(q\Delta t) = 2\sum_{q=1}^{N-1}(N-q)R_F^2(q\Delta t). \tag{2.56}$$

Inspecting the graph in Fig. 2.6.

$$R_F(t) \approx R_\infty(t) \tag{2.57}$$

to within a first-order approximation. Note that the absolute maximum value of R_{∞} is bounded by the sinc function in (2.48),

$$|R_{\infty}(q\Delta t)| \leq \frac{2\gamma}{\pi q} \approx \frac{1}{q}. \tag{2.58}$$

when the sampling frequency is near the Nyquist rate. The results from (2.57) and (2.58) are used to approximate an upper bound for the digital autocorrelation function:

$$R_F^2(q\Delta t) \leq \frac{1}{q^2} \tag{2.59}$$

The number of samples needed to achieve adequate sensitivity is estimated with the ideal relation [76].

$$\Delta T_I = \frac{T_{SYS}}{\sqrt{B\tau}}, \tag{2.60}$$

where τ is the integration time of an analog radiometer. Setting $T_{SYS} = 400$ K, $\Delta T_I = 0.1$ K (good for most geoscience applications), and $N = 2B\tau$ (Nyquist), the number of required samples is on the order of $N = 10^8$. When q is much smaller than N, it can be neglected from the term $(N - q)$ found in (2.56). Otherwise, if q is not negligible, say $q > N/10^2$, then the upper bound of the summed term is

$$(N - q)R_F^2(q\Delta t) < \frac{N}{q^2} < 10^{-4} \ll 1. \tag{2.61}$$

Therefore terms with high values of q are negligible compared to terms with low q values, so

$$\sum_{q=1}^{N-1}(N - q)R_F^2(q\Delta t) \approx \sum_{q=1}^{\infty} NR_F^2(q\Delta t), \tag{2.62}$$

where the infinite series approximation can be made because the upper bound in (2.59) converges rapidly.

Combining (2.56) and (2.62), and substituting back into (2.45), the variance of the output signal is

$$\sigma_F^2 = \frac{2\sigma^4}{N}\left[1 + \frac{1}{6s^2} + 2\left(1 + \frac{1}{12s^2}\right)^2 \sum_{q=1}^{\infty} R_F^2(q\Delta t)\right]. \tag{2.63}$$

Now that the mean and standard deviation of r_Q are known, they are used along with the signal-to-noise expression in (2.28) to solve for the sensitivity:

$$\Delta T_F = T_{SYS}\sqrt{\frac{2}{N}\left[1+\frac{1}{6s^2}+2\left(1+\frac{1}{12s^2}\right)^2\sum_{q=1}^{\infty}R_F^2(q\Delta t)\right]}. \tag{2.64}$$

The above equation can be written in a more familiar form by relating the number of samples to the integration time of the radiometer:

$$N = 2\gamma B\tau. \tag{2.65}$$

Therefore

$$\Delta T_F = \frac{T_{SYS}}{\sqrt{B\tau}}\sqrt{\frac{1}{\gamma}\left[1+\frac{1}{6s^2}+2\left(1+\frac{1}{12s^2}\right)^2\sum_{q=1}^{\infty}R_F^2(q\Delta t)\right]}. \tag{2.66}$$

At the Nyquist rate, the autocorrelation function $R_\infty(q\Delta t)$ in (2.48) has a null for each positive integer q, thus the infinite series in (2.66) vanishes. As expected, the sensitivity approaches that of an ideal radiometer as the resolution of the data converter increases:

$$\lim_{s\to\infty}\Delta T_F = \Delta T_I \quad \text{for } \gamma = 1. \tag{2.67}$$

2.4 Numerical Results

Figure 2.7 shows a plot of the sensitivity ratio $\Delta T_F : \Delta T_I$ for 4.5 level and infinite level resolutions. The narrow band signal is set to the typical specifications $f_0 = 1.41$ GHz and $B = 20$ MHz. Even at a coarse resolution of 4.5 levels, which is only slightly better than 2 bits per sample, the sensitivity at the Nyquist rate is only about 15% worse than the case of infinite resolution detection. It should be noted that ΔT_F fluctuates significantly even when the signal bandwidth is oversampled ($\gamma > 1$). These fluctuations arise because of variations in R_F and R_∞ which gradually diminish as the sampling rate increases. The implication here is that there is some benefit to be gained by sampling above the Nyquist rate of the bandwidth B of the original signal. Also since R_F is determined by the shape of

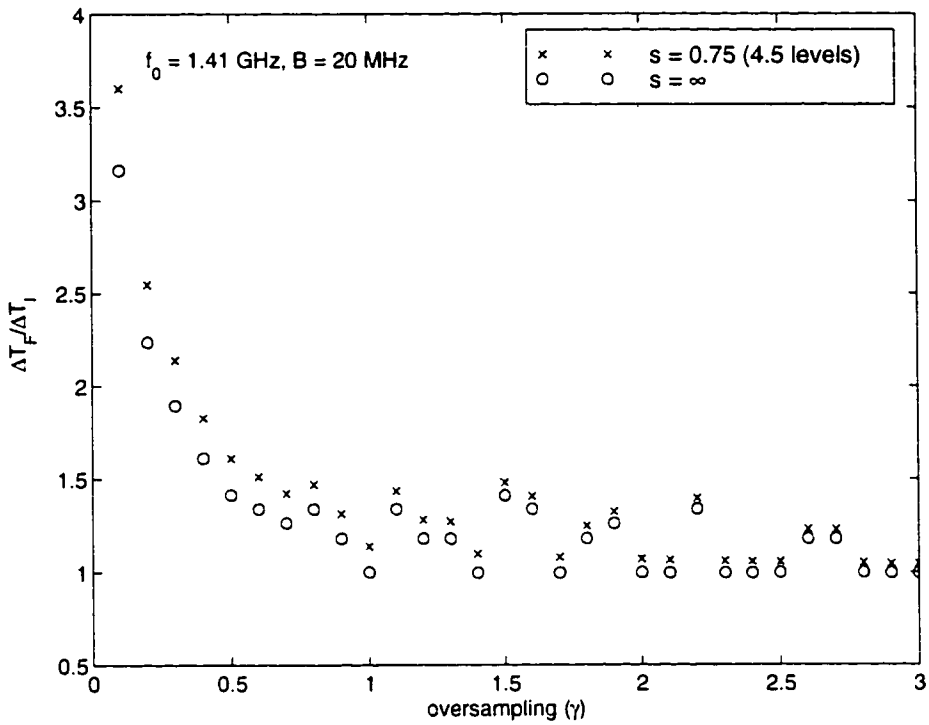


Figure 2.7: Sensitivity (relative to an ideal analog radiometer) at 4.5 level and infinite level resolutions.

the bandpass filter, the characteristic variations in ΔT_F may change if the transfer function in (2.47) is replaced by some other shape (for example, a Gaussian-shaped filter). Thus in Figure 2.7, ΔT_F should be interpreted as being roughly the average sensitivity plotted within a neighborhood of γ. For instance, the relative minima at $\gamma = 1$ should be multiplied by an overrating factor of about 1.2 to reflect the average sensitivity near the Nyquist rate.

In Figure 2.8, the relative sensitivity of the benchmark radiometer is plotted as a function of the number of digitization levels available. The precision improves very rapidly as the resolution increases from 4 levels (2 bits) to 16 levels (4 bits). In fact, at 4 bits the sensitivity is within 1% of the ideal figure given by (2.60). In terms of the design tradeoffs for A/D conversion, there would be some advantage to forfeiting resolution in excess of 3–4 bits to reap the benefits of the wider input bandwidths and higher sampling rates associated with coarse resolution.

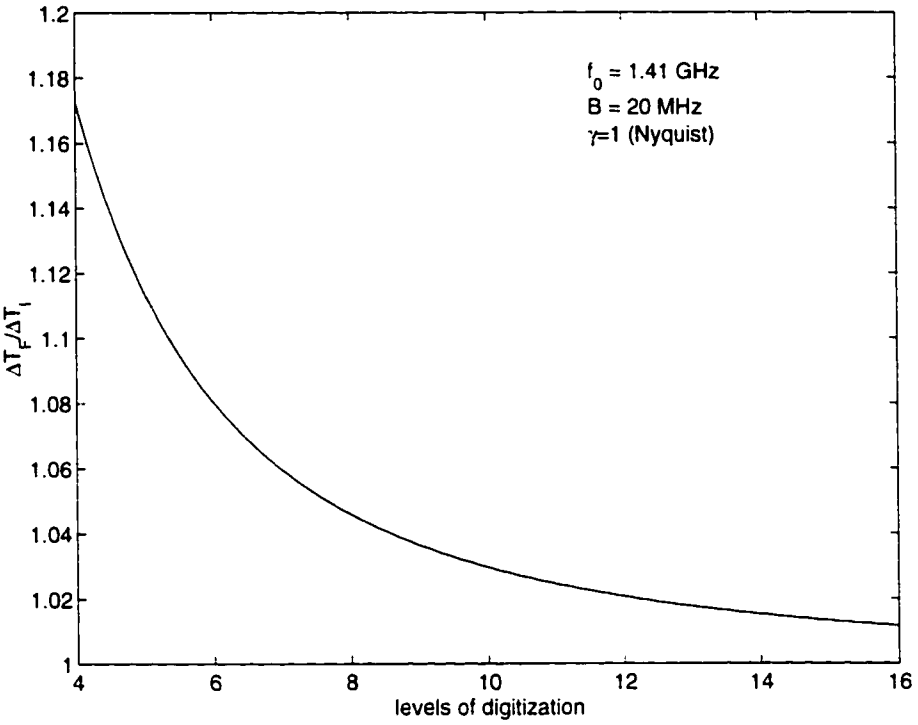


Figure 2.8: Relative sensitivity versus effective number of quantization levels.

The noise sources arising from dc bias drift (2.27) and finite sampling (2.66) are statistically independent, therefore the total NEΔT is the rms summation of these components.

$$\begin{aligned}\Delta T &= \sqrt{(\Delta T_F)^2 + (\Delta T_L)^2} \\ &= T_{SYS}\left\{\frac{1}{\gamma B\tau}\left[1 + \frac{1}{6s^2} + 2\left(1 + \frac{1}{12s^2}\right)^2 \sum_{q=1}^{\infty} R_F^2(q\Delta t)\right] + \frac{f_L^2(s)}{12s^4}\right\}^{1/2} \quad (2.68)\end{aligned}$$

To get a sense for the magnitude of ΔT, suppose that the benchmark system is designed to sample at the Nyquist rate (40 Msamples/sec) and that the integration time is set to 0.5 seconds, which is a typical dwell time for a spaceborne radiometer. Then from (2.68), NEΔT is approximately 0.2 K, which is well below the 1 K sensitivity requirement for an Earth remote sensing mission to map soil moisture.

The next step will be to analyze the more complicated case of a direct-sampling correlation radiometer and gauge its performance in aperture synthesis applications.

CHAPTER 3

Sensitivity and Phase Stability of a Two-Element Correlation DSDR

3.1 Noise-Equivalent Sensitivity Derivation

3.1.1 Problem formulation

The statistical analysis for the total power DSDR in Chapter 2 can be extended to a two-element *correlation DSDR*—the building block for measuring visibility samples in a STAR array. Noise-equivalent sensitivity is derived for the case of a digital correlator viewing a point source in a uniform background, shown in Figure 3.1. This particular brightness scene is useful for characterizing DSDR's impulse response and for comparing the sensitivity with the known capabilities of an analog correlation radiometer.

The detect output of a correlation DSDR resembles the expression in (2.6), except that now there are two identical receiver channels of bandwidth B sampling the Gaussian distributed signals x and y. These analog RF signals are quantized into two data streams, $\hat{x}, \hat{y}$, and are cross-correlated to yield a visibility sample.

$$r_Q = \frac{1}{N} \sum_{n=1}^{N} \hat{x}_n \hat{y}_n. \tag{3.1}$$

Let the point source in the scene have an apparent antenna temperature ΔT. The noise-equivalent sensitivity of the correlation DSDR is then defined as the value of ΔT that would generate a signal output power $\langle r_Q \rangle^2$ equal to the noise power, or variance, of r_Q. We will take ΔT—or any other correlated brightness signal of interest—to be much smaller than the

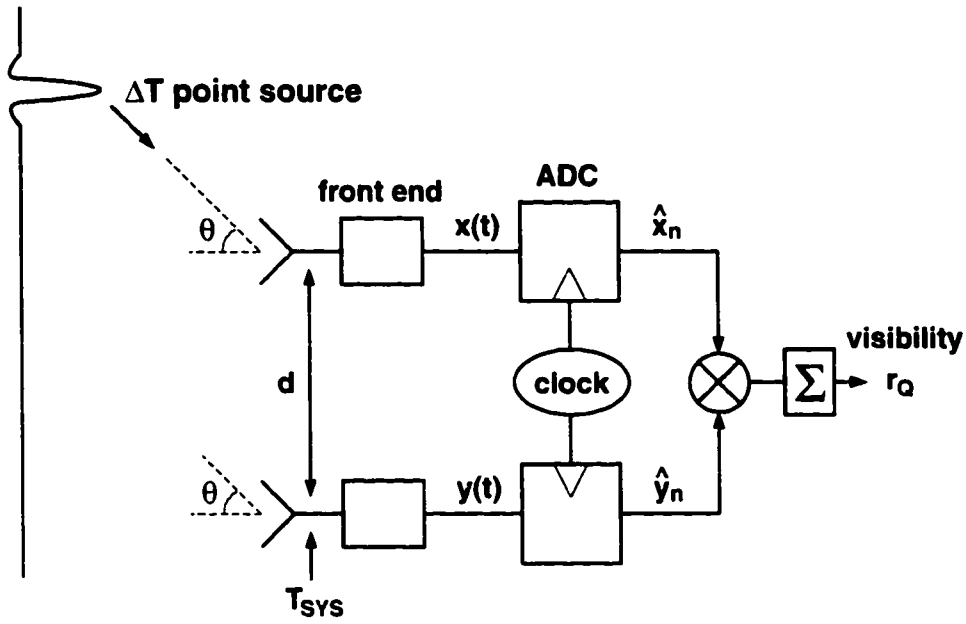


Figure 3.1: Schematic of a correlation DSDR viewing a point source in a uniform background.

uniform background temperature of the scene. This is a reasonable assumption for most of the visibility samples in L-band Earth remote sensing STAR: the apparent brightnesses of soil and vegetation are relatively high, around 150–300 K, and the spectral characteristics of the brightness scene tend to be dominated by dc or low spatial frequency components over the field of view. Therefore, the correlated signal is often much smaller than the system noise temperature of each receiver:

$$\Delta T \cos\phi \ll T'_{SYS}. \tag{3.2}$$

where $\phi = 2\pi\,(d/\lambda)\sin\theta$ is the phase difference between the path lengths from the source to the two antenna elements, separated by distance d. The $\cos\phi$ term in (3.2) represents the dc component produced when two partially coherent, phase delayed signals are multiplied together. As ϕ is varied, the signal strength of the detect output follows the sinusoidal grating lobe pattern discussed in Section 1.3.1. One interesting consequence is that the NEΔT for this type of radiometer will depend on the position of the point source. In fact, for incidence angles yielding $\phi = \pm\frac{\pi}{2}, \frac{3\pi}{2}, \frac{5\pi}{2}, \ldots$, there will be no sensitivity because the

correlated component of the signal will vanish.

The relation in (3.2) is equivalent to saying that the cross-correlation between signals x and y is much less than the power of either signal. If both of these signals are zero-mean variables, each having a variance σ^2, then it follows that the normalized analog correlation coefficient will be relatively small:

$$\rho = \frac{\langle xy \rangle}{\sigma^2} \ll 1. \tag{3.3}$$

The above condition will help simplify the derivation of the signal and noise components of visibility sample r_Q.

3.1.2 Visibility signal

The signal output from the correlation DSDR is defined as the expected value in (3.1):

$$\langle r_Q \rangle = \langle \hat{x}_n \hat{y}_n \rangle . \tag{3.4}$$

Similar to the total power DSDR case, (3.4) will be a complicated function of the analog input level s and the relative dc bias for each A/D converter. As a starting point, the signal can be written as the weighted sum of all possible combinations of the product $\hat{x}\hat{y}$:

$$\langle r_Q \rangle = v_0^2 \sum_{i=-\infty}^{\infty} \sum_{k=-\infty}^{\infty} (i + b_1)(k + b_2) \int_{v_0(k+b_2-1/2)}^{v_0(k+b_2+1/2)} \int_{v_0(i+b_1-1/2)}^{v_0(i+b_1+1/2)} p(x, y)\, dx\, dy, \tag{3.5}$$

where b_1 and b_2 are the relative channel biases (from $-1/2$ to $+1/2$), the limits of integration are determined by the A/D converters' quantization thresholds, and $p(x, y)$ is the Gaussian bivariate pdf defined in (2.52). From the approximation in (3.3), the bivariate distribution can be rewritten as a first-order Taylor expansion:

$$p(x, y) \approx \left(1 + \frac{\rho xy}{\sigma^2}\right) p(x)p(y), \tag{3.6}$$

where $p(x)$ and $p(y)$ are the individual Gaussian pdf's from (2.1).

The simplification in (3.6) is significant because it allows us to separate the double integral in (3.5) and eventually write the expected value of r_Q as a linear function of the

correlation coefficient ρ. Applying the Taylor approximation from above,

$$\int_{v_0(k+b_2-1/2)}^{v_0(k+b_2+1/2)} \int_{v_0(i+b_1-1/2)}^{v_0(i+b_1+1/2)} p(x,y)\,dx\,dy = I_{ik} + \rho J_{ik}, \tag{3.7}$$

where

$$\begin{aligned} I_{ik} &= \frac{1}{2\pi\sigma^2} \int_{v_0(i+b_1-1/2)}^{v_0(i+b_1+1/2)} e^{-x^2/2\sigma^2} dx \int_{v_0(k+b_2-1/2)}^{v_0(k+b_2+1/2)} e^{-y^2/2\sigma^2} dy \\ &= \frac{1}{4}\left[\operatorname{erf}\left(\frac{i+b_1+1/2}{\sqrt{2}s}\right) - \operatorname{erf}\left(\frac{i+b_1-1/2}{\sqrt{2}s}\right)\right] \times \\ &\quad \left[\operatorname{erf}\left(\frac{k+b_2+1/2}{\sqrt{2}s}\right) - \operatorname{erf}\left(\frac{k+b_2-1/2}{\sqrt{2}s}\right)\right] \end{aligned} \tag{3.8}$$

and

$$\begin{aligned} J_{ik} &= \frac{1}{2\pi\sigma^2} \int_{v_0(i+b_1-1/2)}^{v_0(i+b_1+1/2)} x e^{-x^2/2\sigma^2} dx \int_{v_0(k+b_2-1/2)}^{v_0(k+b_2+1/2)} y e^{-y^2/2\sigma^2} dy \\ &= \frac{1}{2\pi}\left\{\exp\left[-\frac{1}{2}\left(\frac{i+b_1+1/2}{s}\right)^2\right] - \exp\left[-\frac{1}{2}\left(\frac{i+b_1-1/2}{s}\right)^2\right]\right\} \times \\ &\quad \left\{\exp\left[-\frac{1}{2}\left(\frac{k+b_2+1/2}{s}\right)^2\right] - \exp\left[-\frac{1}{2}\left(\frac{k+b_2-1/2}{s}\right)^2\right]\right\}. \end{aligned} \tag{3.9}$$

Substituting (3.8) and (3.9) back into (3.5), and factoring out the σ^2 term from the infinite summations, the relation between ρ and the expected visibility sample becomes linear:

$$\langle r_Q \rangle = \sigma^2 \left[A\left(b_1, b_2, s\right) + \rho B\left(b_1, b_2, s\right)\right]. \tag{3.10}$$

where functions

$$A\left(b_1, b_2, s\right) = \frac{1}{s^2} \sum_{i=-\infty}^{\infty} \sum_{k=-\infty}^{\infty} \left(i+b_1\right)\left(k+b_2\right) I_{ik}\left(b_1, b_2, s\right) \tag{3.11}$$

$$B\left(b_1, b_2, s\right) = \frac{1}{s^2} \sum_{i=-\infty}^{\infty} \sum_{k=-\infty}^{\infty} \left(i+b_1\right)\left(k+b_2\right) J_{ik}\left(b_1, b_2, s\right) \tag{3.12}$$

represent offset and gain errors incurred during quantization.

Equations (3.11) and (3.12) can be solved numerically with respect to b_1, b_2, and s to gauge the correlator's sensitivity to changes in signal bias. Also, by taking advantage of the odd and even symmetries of the two functions,

$$A(b_1, -b_2) = A(-b_1, b_2) = -A(b_1, b_2) \tag{3.13}$$

$$B(b_1, -b_2) = B(-b_1, b_2) = B(b_1, b_2), \tag{3.14}$$

the computation expense can be limited to just one quadrant in the b_1-b_2 plane.

A function analysis

According to (3.13), the the A function will have odd symmetry about the axes $b_1 = 0$ and $b_2 = 0$. It follows that A is identically zero along these axes and that the peak-to-peak variation ΔA over the entire domain $(-1/2 \leq b_1, b_2 \leq 1/2)$ is just twice the absolute maximum value of A in any single quadrant.

The behavior of A was studied by computing its response in the first quadrant for various values of signal strength s (Figure 3.2). As s increases, the A function tends toward zero and thus becomes insensitive to bias changes. Also, the absolute maximum occurs at the center point of the quadrant, at $b_1 = b_2 = 1/4$.

Qualitatively, the center peak in the graph can be explained by the large skew (third central moment) in the random processes $\hat{x}$ and $\hat{y}$. We know that, for example, a bias midway between converter thresholds (0) or right at a threshold (1/2) would yield perfect symmetry in the quantized waveforms. The cross-correlation of two zero-mean, symmetric waveforms would not produce an offset error. However, as biases move away from these extremes toward a value of 1/4, the modes of $\hat{x}$ and $\hat{y}$ also approach 1/4, and the pdf's of these two waveforms become skewed. This asymmetry introduce a finite error A, which, as shown in Figure (3.2), tends to worsen as the quantization resolution decreases.

Figure 3.3 shows the maximum deviation ΔA computed over a continuous range of quantization resolutions. The uncertainty decreases exponentially as more levels of resolution are added to the digital correlator. At 4 levels (2 bits), ΔA has a value of $\sim 10^{-8}$, which is negligible compared to the smallest value of ρ that might be resolved with a correlation radiometer. For more than 2 bits of resolution, the change in A becomes vanishingly small. Unlike the case of the single-channel total power DSDR, there is no additive quantization

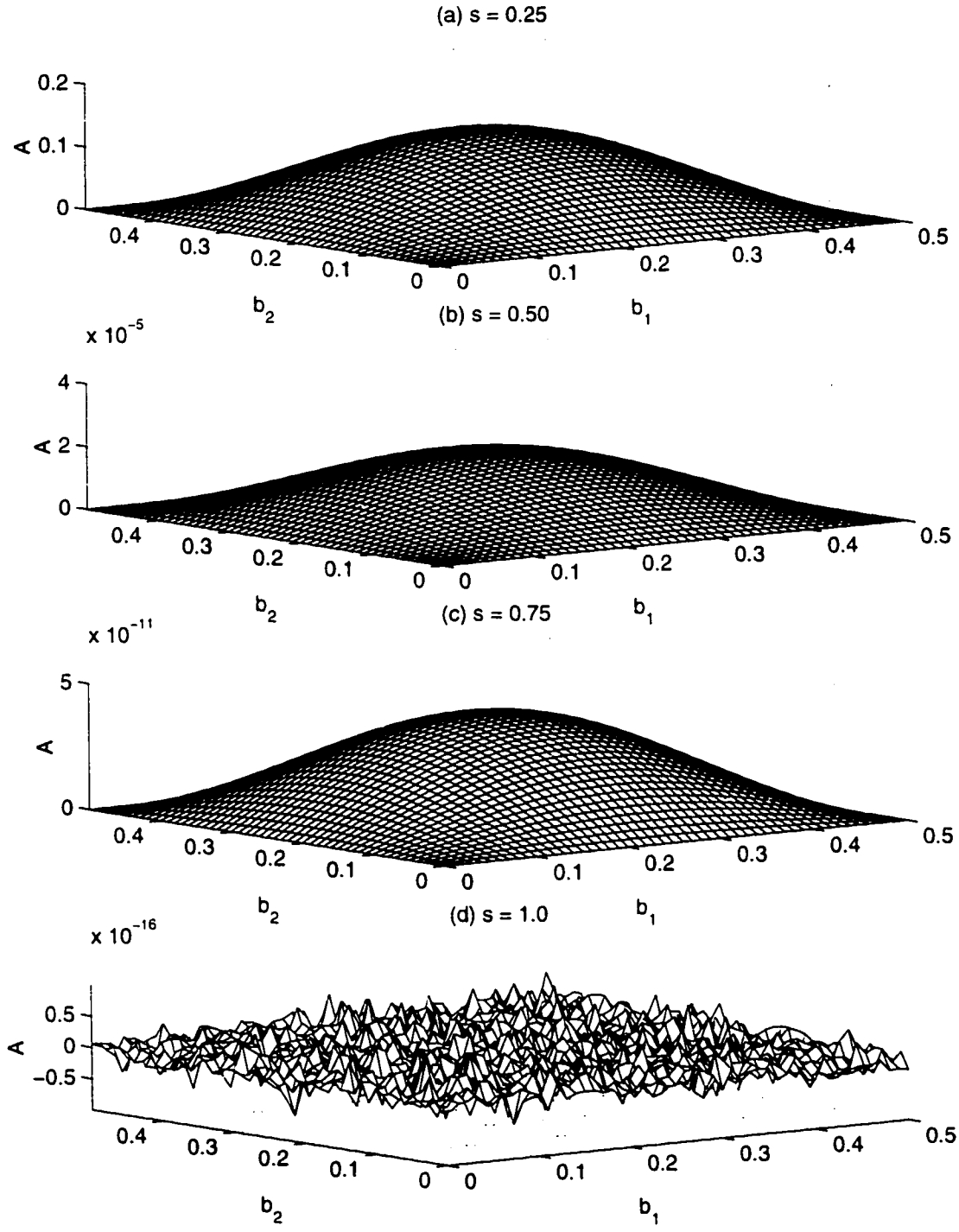


Figure 3.2: The A function (correlator offset error) computed over the first quadrant of the b_1-b_2 plane for relative signal strengths: (a) $s = 1/4$, (b) $s = 1/2$, (c) $s = 3/4$, (d) $s = 1$. The absolute maximum tends to be located at the center of the quadrant ($b_1, b_2 = 1/4$) and rapidly decreases to a negligible value for $s \geq 1$.

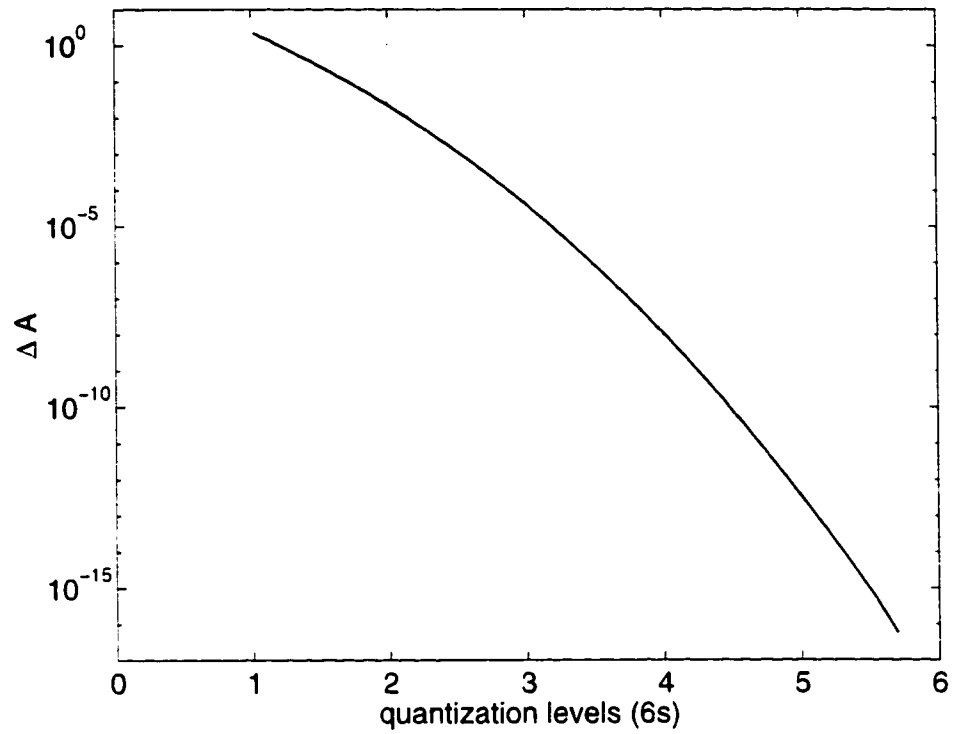


Figure 3.3: Maximum bias-induced deviation in the A function.

noise term generated by the digital correlator for sufficiently large signals. The physical interpretation is that quantization noise sources from the two separate receivers are independent and therefore will have no correlated noise component in r_Q. Equation (3.10) is approximated to reflect the large signal condition, with greater than 2 bits of converter resolution:

$$\langle r_Q \rangle = \rho\sigma^2 B(b_1, b_2, s). \tag{3.15}$$

B function analysis

Another simplification to (3.10) can be inferred by looking at the behavior of the B function, or correlator gain error. $B(b_1, b_2)$ was computed over the first quadrant for several values of s. For each signal level, the minima and maxima always occurred at $b_1, b_2 = 0$ and $1/2$, respectively. This makes intuitive sense: a small, zero-biased signal centered in one

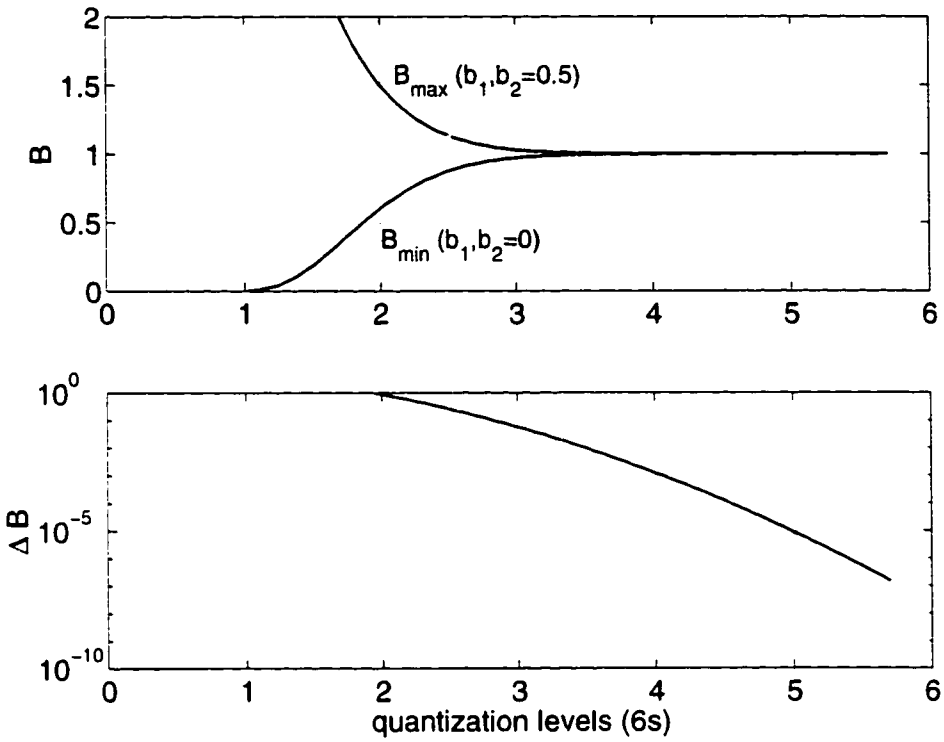


Figure 3.4: Maximum bias-induced fluctuation in the B function.

quantization bin will have its amplitude clipped during the A/D conversion; in contrast, biases centered on the conversion threshold will generate bimodal peaks at $\pm 1/2$ in the pdf of each quantized waveform which effectively amplify the signals. Maximum and minimum values of B are plotted in Figure 3.4 along with the error, or difference, ΔB. The gain error quickly converges to unity and becomes insensitive to changes in bias for greater than 4 levels of resolution: ΔB decreases to $\sim 0.1\%$ at 4 quantization levels and 10 ppm at 5 levels. Therefore in the large signal limit, the visibility signal in (3.15) approaches the case of an ideal analog correlation radiometer, with neither additive noise nor gain errors:

$$\langle r_Q \rangle \approx \rho\sigma^2 = \langle xy \rangle \,. \tag{3.16}$$

In terms of radiometric measurements, (3.16) will be proportional to the correlated component of the brightness signal, $\Delta T \cos\phi$.

3.1.3 Visibility noise

The noise power, or variance, of the visibility output can be solved by closely following the discrete-time statistical analysis presented in Section 2.3.2 for a total power DSDR. As before, it is assumed that the correlation DSDR operates in the large signal region (≥ 2 bits). By definition, the variance of the output r_Q is

$$\sigma_Q^2 = \langle r_Q^2 \rangle - \langle r_Q \rangle^2 . \tag{3.17}$$

This can be expanded using (3.1) and the approximation in (3.16):

$$\sigma_Q^2 = \frac{1}{N^2} \sum_{n=1}^{N} \left\langle (\hat{x}_n \hat{y}_n)^2 \right\rangle + \frac{1}{N^2} \sum_{n=1}^{N} \sum_{\substack{m=1 \\ m \neq n}}^{N} \langle \hat{x}_n \hat{y}_n \hat{x}_m \hat{y}_m \rangle - \rho^2 \sigma^4 . \tag{3.18}$$

The expected value expressions in (3.18) are estimated with the moment factoring relation for jointly Gaussian random variables [81]. For the first term,

$$\langle \hat{x}^2 \hat{y}^2 \rangle \approx \langle \hat{x}^2 \rangle \langle \hat{y}^2 \rangle + 2 \langle \hat{x} \hat{y} \rangle^2 , \tag{3.19}$$

where $\langle \hat{x}^2 \rangle$ and $\langle \hat{y}^2 \rangle$ are both equal to the total power detect output given by (2.21),

$$\langle \hat{x}^2 \rangle = \langle \hat{y}^2 \rangle = \sigma^2 \left(1 + \frac{1}{12 s^2} \right) \tag{3.20}$$

and $\langle \hat{x} \hat{y} \rangle$ is just the correlator output result from (3.4) and (3.16),

$$\langle \hat{x} \hat{y} \rangle = \rho \sigma^2 . \tag{3.21}$$

Combining (3.19)-(3.21), the first term of (3.18) can be rewritten as

$$\frac{1}{N^2} \sum_{n=1}^{N} \langle \hat{x}_n^2 \hat{y}_n^2 \rangle = \frac{\sigma^4}{N} \left[\left(1 + \frac{1}{12 s^2} \right)^2 + 2 \rho^2 \right] . \tag{3.22}$$

Likewise, the second summation in (3.18) can be expanded by Gaussian moment factoring:

$$\langle \hat{x}_n \hat{y}_n \hat{x}_m \hat{y}_m \rangle = \langle \hat{x}_n \hat{x}_m \rangle \langle \hat{y}_n \hat{y}_m \rangle + \langle \hat{x}_n \hat{y}_n \rangle \langle \hat{x}_m \hat{y}_m \rangle + \langle \hat{x}_n \hat{y}_m \rangle \langle \hat{x}_m \hat{y}_n \rangle . \tag{3.23}$$

The first term on the RHS of (3.23) is composed of the digital autocorrelation function R_F, defined previously in (2.43):

$$\langle \hat{x}_n \hat{x}_m \rangle = \langle \hat{y}_n \hat{y}_m \rangle = \sigma^2 \left(1 + \frac{1}{12s^2} \right) R_F(q\Delta t). \tag{3.24}$$

The second term in (3.23) is made up of cross-correlation products between the two digital channels, given by (3.21). The third term is a combination of cross-correlation (ρ) and autocorrelation (R_F) terms; for most values of q, this term will be small because it encapsulates the correlation loss incurred due to both time separation and spatial separation of the received signals. As a first order approximation, this last term will be neglected. Combining (3.21), (3.23) and (3.24), the second series in (3.18) is written as

$$\sum_{n=1}^{N} \sum_{\substack{m=1 \\ m \neq n}}^{N} \langle \hat{x}_n \hat{y}_n \hat{x}_m \hat{y}_m \rangle \approx \sigma^4 \left(1 + \frac{1}{12s^2} \right)^2 \sum_{n=1}^{N} \sum_{\substack{m=1 \\ m \neq n}}^{N} R_F^2 (q\Delta t) + N(N-1)\rho^2 \sigma^4. \tag{3.25}$$

It was shown from (2.56) and (2.62) that, because of the rapid convergence of the R_F^2 series,

$$\sum_{n=1}^{N} \sum_{\substack{m=1 \\ m \neq n}}^{N} R_F^2 (q\Delta t) \approx 2N \sum_{q=1}^{\infty} R_F^2 (q\Delta t). \tag{3.26}$$

Substituting (3.22), (3.25) and (3.26) into (3.18), and neglecting the ρ^2 term for $\rho \ll 1$, the standard deviation of the correlator output is approximately

$$\sigma_Q = \frac{\sigma^2}{\sqrt{N}} \left(1 + \frac{1}{12s^2} \right) \sqrt{1 + 2 \sum_{q=1}^{\infty} R_F^2 (q\Delta t)}. \tag{3.27}$$

3.1.4 NEΔT and implications for STAR

The noise-equivalent sensitivity of the correlation DSDR is found by equating the solutions for signal and noise powers. From (3.16), a correlation DSDR having 2 or more bits of resolution behaves as a linear system with brightness in and visibility data out. Therefore there exists some constant C (in units of K^{-1}) that describes the transfer function:

$$\langle r_Q \rangle = C \Delta T \cos \phi. \tag{3.28}$$

By the definition in (3.3), the normalized correlation coefficient between two signals is the ratio of the correlated component to the total power of each signal:

$$\rho = \frac{\Delta T \cos\phi}{T_{SYS}} \approx \frac{\langle r_Q \rangle}{\sigma^2}. \tag{3.29}$$

Therefore, from (3.28) and (3.29), the system's transfer constant is $C = \sigma^2/T_{SYS}$. Using this ratio, the rms noise level of the correlation DSDR in (3.27) can be expressed as an equivalent input-referred brightness signal.

$$T_{\sigma Q} = \frac{\sigma_Q}{\sigma^2} \cdot T_{SYS}. \tag{3.30}$$

NEΔT is then determined by setting $T_{\sigma Q}$ equal to the correlated input signal $\Delta T \cos\phi$, yielding

$$\Delta T = \frac{T_{SYS}}{\cos\phi\sqrt{2\gamma B\tau}} \left(1 + \frac{1}{12s^2}\right) \sqrt{1 + 2\sum_{q=1}^{\infty} R_F^2(q\Delta t)}, \tag{3.31}$$

where the substitution $N = 2\gamma B\tau$ has been incorporated from (2.65).

The above NEΔT solution is verified for the limiting case of an analog correlation radiometer with infinite A/D resolution ($s \to \infty$) and Nyquist sampling ($\gamma = 1$). It was shown in Section 2.3.2 that if the receiver has a rectangular bandpass response, R_F will have nulls at all non-zero multiples of Δt. Therefore the autocorrelation series vanishes, and (3.31) is reduced to

$$\lim_{s\to\infty} \Delta T_{(Nyquist)} = \Delta T_\infty = \frac{1}{\sqrt{2}\cos\phi} \cdot \frac{T_{SYS}}{\sqrt{B\tau}}. \tag{3.32}$$

which agrees exactly with the known sensitivity for an ideal analog correlation radiometer [30].

The NEΔT results in (3.31) and (3.32) were calculated for a target at boresight using the parameters for a typical L-band spaceborne radiometer: $T_{SYS} = 400$ K, $B = 20$ MHz and $\tau = 0.5$ s. These calculations are compared to the ideal analog sensitivity ($\Delta T_\infty = 89$ mK) in Table 3.1 for a range of correlator resolutions. As in the case of a total power DSDR, the

bit resolution	computed ΔT	% from ideal (ΔT_∞)
2	106 mK	19%
3	92.8 mK	3.8%
4	90.5 mK	1.2%

Table 3.1: Theoretical sensitivity results for a correlation DSDR.

correlation DSDR sensitivity rapidly approaches the ideal performance for 3 or more bits of resolution. These low bit requirements contribute to the overall simplicity of DSDR for aperture synthesis, where there might be up to 100 separate receiver modules and a bank of 10,000 correlators.

3.1.5 Comments on effective bit resolution

In Chapter 2, the number of quantization levels in DSDR was defined in terms of the $\pm 3\sigma$ range of the analog input signal, and it was assumed that the A/D converter had an infinite number of quantization bins. This 6σ scale is only an approximation of the effective resolution of the digitizer. A more rigorous relation between the signal amplitude s and the effective number of bits (ENOB) can be found by equating the signal-to-noise performance of the multibit DSDR with the performance of a fixed-bit correlator, i.e., a correlator which clips its samples beyond a certain voltage range.

Fixed-bit correlators have been studied in detail for applications in radio astronomy [10, 19]. One characteristic of a fixed-bit correlation is that, for 3 or more digital levels, there will be some optimum value of σ/v_0 which yields a maximum SNR. Consider, for example, a 4-level system. As s becomes either very small or very large, the digitizer effectively sees only 2 levels of conversion, resulting in a lower SNR. Between these extremes there exists some gain setting which takes maximum advantage of the information content in all 4 quantization bins. Thompson *et al.* have determined the optimum SNR results, listed in Table 3.2, for digital correlators fixed at 2, 3, and 4 levels, for the case where the normalized correlation coefficient is small ($\rho \ll 1$) [75].

quantization levels	SNR relative to an infinite resolution correlator
2	64%
3	81%
4	88%

Table 3.2: Optimum SNR results for fixed-bit correlators [75].

By contrast, the multibit quantization method used in DSDR does not yield an optimum SNR value. The effective number of bits and the SNR continue to improve as s increases (that is, as long as the signal does not exceed the full scale range of the converter and cause saturation). The question of interest becomes: "What values of s in DSDR would yield the same SNR as the optimized fixed-bit correlators?" In answering this, the relative signal strength s can be mapped to the ENOB in a way that rigorously takes into account the information content of the detected signals.

The SNR of the correlation DSDR for the case $\rho \ll 1$ is found using the r_Q signal and noise solutions, expressed in (3.16) and (3.27). At the Nyquist sampling rate,

$$SNR_Q = \frac{\langle r_Q \rangle}{\sigma_Q} = \frac{\rho\sqrt{N}}{1 + \frac{1}{12s^2}}. \tag{3.33}$$

which can be normalized with respect to the infinite resolution (continuous correlator) case to yield a relative SNR,

$$SNR = \left(1 + \frac{1}{12s^2}\right)^{-1}. \tag{3.34}$$

The inverse solution for the above equation is then

$$s = \sqrt{\frac{SNR}{12\,(1 - SNR)}}. \tag{3.35}$$

The SNR values of 0.64, 0.81, and 0.88 from Table 3.2 then correspond to $s = 0.385$, 0.596, and 0.782, respectively. Given that these represent 2, 3, and 4-level correlations in terms of information content, the equivalent input range can be found for the Gaussian distributed signals detected in a correlation DSDR. For instance, at the two-level setting the effective

number of σ's is

$$\frac{2v_0}{\sigma} = \frac{2v_0}{0.385v_0} = 5.20. \tag{3.36}$$

At 3 and 4 level settings, the number of standard deviations are 5.03 and 5.12. These results retrospectively suggest that, on average, it may be more appropriate to use a range of $\sim 5.1\sigma$, rather than 6σ, to define the effective bit resolution of the correlation DSDR. The effect of the 6σ approximation is that bit resolution values in Table 3.1 were overestimated by $\log_2(6.0/5.1) = 0.23$ bits, and calculations of noise-equivalent sensitivity will err on the conservative side. For example, when it was stated that a 2-bit DSDR performs within 19% of the ideal radiometric sensitivity, this actually means that an optimized, fixed-bit correlator having 4 quantization levels would have a slightly better performance. The margin of error in ENOB may in fact be welcome because variability in signal levels for the fixed-bit correlator will yield results that are sometimes less than optimal.

It is also worth noting that beyond 2-bit resolutions the relative SNR asymptotically approaches 1, so that any error in the ENOB estimate becomes less significant. Referring to Table 3.1 again, it was shown that the correlation DSDR's sensitivity improves from 19% to 4% as the estimated bit resolution varies from 2 to 3 bits. Interpolating between these values, a 0.23 bit resolution error generates only a 3.5% error in the NEΔT estimate.

3.2 Phase Stability in the Sampling Head

In the actual correlation DSDR hardware, the circuitry inside each A/D converter will exhibit some amount of timing jitter, or random variations in sampling. Because the timing variations between the two separate channels are statistically independent, there can be a loss of signal coherence which degrades the sensitivity of the radiometer.

Suppose that two identical signals are injected into the A/D converter sections of the correlation DSDR ($x(t) = y(t)$). The narrowband noise can be represented with the Rice

model [71],

$$x(t) = n_I(t)\cos(\omega_0 t) + n_Q(t)\sin(\omega_0 t), \tag{3.37}$$

where n_I and n_Q are random processes which both have the normal distribution $N(0, \sigma^2)$, and $\omega_0 = 2\pi f_0$ represents the carrier frequency. Then the nth pair of sampled voltages is

$$\hat{x}_n = x\left(t_n + \delta_{xn}\right) \tag{3.38a}$$

$$\hat{y}_n = x\left(t_n + \delta_{yn}\right). \tag{3.38b}$$

where δ_{xn} and δ_{yn} are the sampling jitter times of the first and second A/D converters, and, for simplicity, we assume that the bit resolution is high enough that quantization effects can be ignored. Timing jitter in (3.38) will modify the sampled waveforms as follows:

$$\hat{x}_n = n_I\left(t_n + \delta_{xn}\right)\cos\left[\omega_0\left(t_n + \delta_{xn}\right)\right] + n_Q\left(t_n + \delta_{xn}\right)\sin\left[\omega_0\left(t_n + \delta_{xn}\right)\right] \tag{3.39a}$$

$$\hat{y}_n = n_I\left(t_n + \delta_{yn}\right)\cos\left[\omega_0\left(t_n + \delta_{yn}\right)\right] + n_Q\left(t_n + \delta_{yn}\right)\sin\left[\omega_0\left(t_n + \delta_{yn}\right)\right]. \tag{3.39b}$$

which can be rewritten in a Taylor series expansion for small δ_n,

$$\hat{x}_n \approx n_I(t_n)\cos\left(\omega_0 t_n\right) + n_Q(t_n)\sin\left(\omega_0 t_n\right) + \omega_0\delta_{xn}\left[n_Q(t_n)\cos\left(\omega_0 t_n\right) - n_I(t_n)\sin\left(\omega_0 t_n\right)\right] \tag{3.40a}$$

$$\hat{y}_n \approx n_I(t_n)\cos\left(\omega_0 t_n\right) + n_Q(t_n)\sin\left(\omega_0 t_n\right) + \omega_0\delta_{yn}\left[n_Q(t_n)\cos\left(\omega_0 t_n\right) - n_I(t_n)\sin\left(\omega_0 t_n\right)\right]. \tag{3.40b}$$

Therefore timing jitter generates independent, additive noise terms in the two sampled waveforms. Substituting the above expansion into (3.4), the correlator output signal becomes

$$r_Q = \left\langle\left[n_I(t_n)\cos\left(\omega_0 t_n\right)\right]^2\right\rangle + \left\langle\left[n_Q(t_n)\sin\left(\omega_0 t_n\right)\right]^2\right\rangle = \sigma^2. \tag{3.41}$$

The correlator output can also be calculated for the ideal case where there is no loss of coherence between the two sampling heads—that is, when $\delta_{xn} = \delta_{yn}$ for all n. Then

$$\begin{aligned} r_{Q(ideal)} = \left\langle\hat{x}_n^2\right\rangle &= \left\langle\left[n_I(t_n)\cos\left(\omega_0 t_n\right)\right]^2\right\rangle + \left\langle\left[n_Q(t_n)\sin\left(\omega_0 t_n\right)\right]^2\right\rangle + \\ &\left\langle\left[\omega_0\delta_{xn}n_Q(t_n)\cos\left(\omega_0 t_n\right)\right]^2\right\rangle + \left\langle\left[\omega_0\delta_{xn}n_I(t_n)\sin\left(\omega_0 t_n\right)\right]^2\right\rangle \\ &= \sigma^2\left(1 + \omega_0^2\sigma_\delta^2\right), \end{aligned} \tag{3.42}$$

where σ_δ^2 is the variance of the timing jitter. The *coherence loss* is defined as the ratio of ideal to actual r_Q values [6],

$$CL \equiv \frac{r_{Q(ideal)}}{r_Q} = 10\log_{10}\left(1+\omega_0^2\sigma_\delta^2\right) \text{ [dB]}. \tag{3.43}$$

Presently, L-band flash A/D converter technology is capable of achieving $\sigma_\delta = 2$ ps rms phase stability. According to (3.43), this would yield a negligible correlation loss, on the order of 10^{-3} dB, for a correlation DSDR operating at 1.4 GHz. Timing jitter between data converters is therefore not thought to be a limiting design factor for implementing the direct-sampling architecture onto a STAR sensor.

3.3 A Technique for Alleviating Decorrelation Effects in Very Long Baseline STAR

Another potential source of phase noise can arise in L-band STAR as the design evolves toward larger array sizes. The next-generation arrays that follow the SMOS mission described in Section 1.3, for example, must extend significantly beyond 10 meters to accommodate the $\leq$ 10 km resolution requirement for mesoscale hydrometeorology. But as the maximum baseline is made progressively larger, the time delay between a pair of received signals may exceed the $1/B$ correlation time defined by the system bandwidth of the radiometer, especially when the brightness source is far away from the boresight direction. This decorrelation effect leads to a phenomenon known as fringe washing, which is a loss of brightness information at high spatial frequencies and oblique viewing angles.

Ruf *et al.* have suggested splitting the receiver bandwidth into several smaller subbands before correlation and then individually transforming each visibility sample to reconstruct the image [60]. The smaller bandwidth associated with each correlator naturally leads to an increased correlation time. Depending on the number of band divisions, fringe washing may be reduced significantly without compromising the overall bandwidth and sensitivity of the STAR radiometer. In this section, the band division correlation (BDC) concept shown

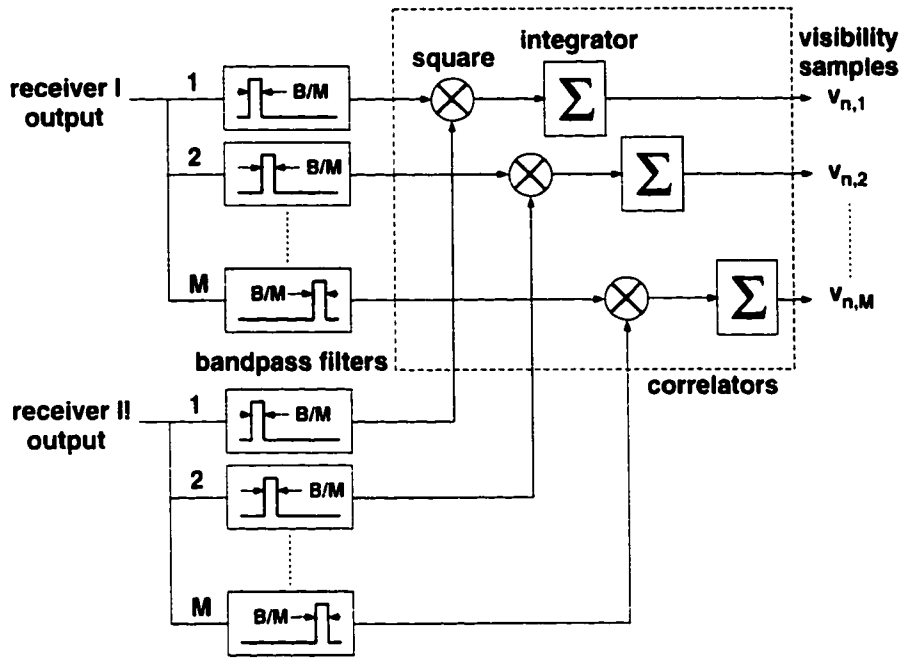


Figure 3.5: Schematic of a band division correlation (BDC) radiometer. The received signals, each having bandwidth B, are divided evenly into M smaller bands to reduce decorrelation effects.

in Figure 3.5 is evaluated in the context of improving STAR's spatial frequency response.

In the following analysis, quantization effects in the correlator will be neglected. (Recall from Figure 2.6 that, to within a first-order approximation, quantized and continuous correlation coefficients are equal for > 2 bit resolution.) It should be noted that the BDC receiver technique is applicable to either analog or digital hardware designs. In practice, though, a multi-channel correlator is vastly simpler to implement in digital hardware using FIR filter techniques than in analog hardware, which would require a bank of discrete microwave components. For DSDR applications, the two receiver outputs denoted in Figure 3.5 can be treated as the large-signal digitized data streams coming from the A/D converter sections.

A model of a one-dimensional STAR sensor in low Earth orbit with a desired resolution of 10 km will be used to compare the point spread functions (PSF) for conventional correlators and for the BDC architecture. For this comparison, a typical L-band satellite having a 2–3 day revisit period is considered with the design parameters: $f_0 = 1.41$ GHz, $B = 20$ MHz,

altitude $h = 700$ km, and a field of view of $\theta = \pm 35°$. To simplify the problem further, it is assumed that all antenna elements are isotropic, the array has a uniform amplitude distribution, and the Earth is flat across the FOV.

3.3.1 Ideal spatial resolution of STAR

The spatial resolution of an ideal STAR which does not suffer from fringe washing is first derived as a basis for comparison. From (1.1), the visibility function of the array can be written as

$$V(n) = \int_{-1}^{1} \frac{1}{\sqrt{1-\mu^2}} T_B(\mu)\, e^{-j\pi n\mu} d\mu \quad \text{for } n = 0, 1, \ldots, N. \tag{3.44a}$$

where

$$\mu = \sin\theta \tag{3.44b}$$

represents the direction sine coordinate and N is the maximum dimension of the array in $\lambda/2$ spacings. Let

$$T'_B(\mu) = T_B(\mu)/\sqrt{1-\mu^2} \tag{3.45}$$

be defined as the modified brightness scene. Then (3.44) is just the Fourier transform of T'_B, and the reconstructed image $\tilde{T}_B$ can be found by taking the inverse Fourier series of the visibility function:

$$\begin{aligned} \tilde{T}_B(\mu) &= \sqrt{1-\mu^2} F^{-1}\{V(n)\} \\ &= \frac{1}{2}\sqrt{1-\mu^2} \sum_{n=-N}^{N} V(n) e^{j\pi n\mu}. \end{aligned} \tag{3.46}$$

Spatial resolution is determined as a function of the maximum baseline spacing N by looking at the response to a point source in the brightness scene. Consider a scene that has a source located at $\mu = \mu_s$,

$$T_B(\mu, \mu_s) = \delta(\mu - \mu_s). \tag{3.47}$$

Plugging (3.47) back into (3.44), the visibility function for the impulse is

$$V(n,\mu_s) = \frac{e^{-j\pi n\mu_s}}{\sqrt{1-\mu_s^2}}, \tag{3.48}$$

and the STAR point spread function becomes

$$\tilde{T}_B(\mu,\mu_s) = \frac{1}{2}\sqrt{\frac{1-\mu^2}{1-\mu_s^2}} \sum_{n=-N}^{N} e^{j\pi n(\mu-\mu_s)}. \tag{3.49}$$

Note that the series in (3.49) has Hermitian symmetry and therefore must be a real quantity. Also, its sequence consists of a geometric progression which has a closed-form solution for the sum,

$$\sum_{n=-N}^{N} a^n = \frac{1-a^{2N+1}}{(1-a)a^N}, \tag{3.50}$$

with $a = e^{j\pi n(\mu-\mu_s)}$. Applying (3.50) and multiplying both the numerator and denominator by the conjugate value $(1-a^*)(a^*)^N$, we have

$$\begin{aligned} \tilde{T}_B(\mu,\mu_s) &= \frac{1}{2}\sqrt{\frac{1-\mu^2}{1-\mu_s^2}} \cdot \frac{1-e^{j\pi(2N+1)(\mu-\mu_s)}}{(1-e^{j\pi(\mu-\mu_s)})e^{j\pi N(\mu-\mu_s)}} \\ &= \frac{1}{2}\sqrt{\frac{1-\mu^2}{1-\mu_s^2}} \cdot \frac{\cos[\pi N(\mu-\mu_s)] - \cos[\pi(N+1)(\mu-\mu_s)]}{1-\cos[\pi(\mu-\mu_s)]}. \end{aligned} \tag{3.51}$$

The pattern in (3.51) has a principal peak value of $(2N+1)/2$ at $\mu = \mu_s$, and it has nulls where the sum of cosine arguments equals an integer multiple of 2π, i.e.,

$$\mu_{null} = \mu_s + \frac{2m}{2N+1} \quad \text{for } m = \pm 1, 2, \ldots . \tag{3.52}$$

Therefore the main lobe of the synthesized beam is delimited by nulls at $\mu_s \pm 2/(2N+1)$, yielding a beamwidth of

$$\Delta\mu = \frac{4}{2N+1}. \tag{3.53}$$

which can be expressed in terms of angular resolution by differentiating (3.44b):

$$\Delta\theta = \frac{4}{(2N+1)\cos\theta}. \tag{3.54}$$

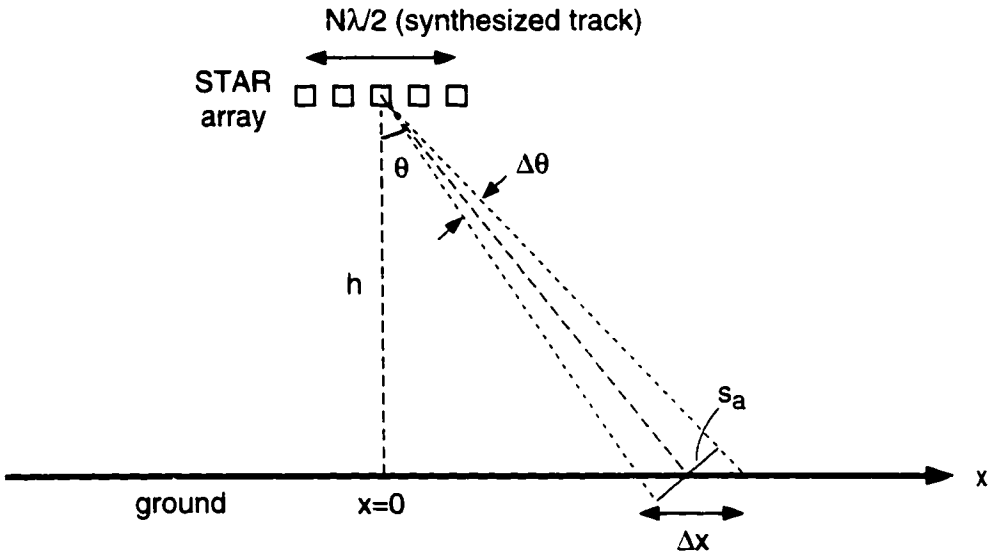


Figure 3.6: Geometry for determining the spatial resolution in STAR.

Figure 3.6 illustrates the geometry for finding the size of the satellite's footprint at an angle θ away from nadir. At an altitude h, the sensor is a distance $h \sec\theta$ away from the pixel. Thus, the arc length of the main beam at ground level is

$$s_a = \frac{h\Delta\theta}{\cos\theta}. \tag{3.55}$$

and the projection on the ground becomes

$$\Delta x = \frac{s_a}{\cos\theta}. \tag{3.56}$$

Combining (3.54)–(3.56), the ideal spatial resolution is expressed as

$$\Delta x = \frac{4h}{(2N+1)\cos^3\theta}. \tag{3.57}$$

Therefore, to maintain at least 10 km resolution at the 35° swath edge would require a STAR array size of $N \approx 255$, or 27 meter span, when the satellite's orbit is at $h = 700$ km. This 27 meter L-band STAR will be our reference model for evaluating the BDC architecture.

3.3.2 Fringe washing phenomenon

Visibility function

For an actual STAR radiometer with finite bandwidth, there will always be some amount of decorrelation between pairs of received signals which worsens as the incidence angle and delay time are increased. This tapering in visibility is described by the fringe washing function [32],

$$\begin{aligned} r_w(\tau) &= F^{-1}\{H_1(f-f_0)H_2^*(f-f_0)\} \\ &= e^{-j2\pi f_0\tau}\int_{-\infty}^{\infty} H_1(f)\,H_2^*(f)\,e^{j2\pi f\tau}df. \end{aligned} \tag{3.58}$$

where H_1 and H_2 are the transfer function responses for the first and second receiver channels. The visibility function in (3.44) can be modified to take fringe washing into account:

$$V(n) = \int_{-1}^{1} \frac{1}{\sqrt{1-\mu^2}} T_B(\mu)\, r_w(\tau)\, e^{-j\pi n\mu} d\mu. \tag{3.59}$$

Assuming that the two receivers exhibit identical rectangular bandpass responses described by (2.47), the fringe washing function is equal to the envelop ($\mathrm{sinc}B\tau$) of the autocorrelation function in 2.48. From the geometry in Figure 3.1, the lag time τ between reception of a brightness signal for two elements separated by $d = n\lambda/2$ is

$$\tau = \frac{d\mu}{c} = \frac{n\mu}{2f_0}. \tag{3.60}$$

Thus fringe washing is related to the element-pair spacing and the angular position of the source,

$$r_w(n,\mu) = \mathrm{sinc}\left(\frac{nB\mu}{2f_0}\right). \tag{3.61}$$

The visibility impulse response for a point source centered at μ_s becomes

$$V(n,\mu_s) = \frac{r_w(n,\mu_s)\, e^{-j\pi n\mu_s}}{\sqrt{1-\mu_s^2}}. \tag{3.62}$$

To examine how fringe washing affects the point spread function in conventional STAR, inverse solutions for (3.59) are found using both Fourier transform and G-matrix approaches.

Inverse Fourier reconstruction

If the effects of fringe washing are neglected in solving for $\tilde{T}_B$, then the impulse response in (3.62) can be substituted directly into the inverse Fourier series (3.46). The brightness estimate resulting from inverse Fourier (F^{-1}) reconstruction is

$$\tilde{T}_B(\mu, \mu_s) = \frac{1}{2}\sqrt{\frac{1-\mu^2}{1-\mu_s^2}} \sum_{n=-N}^{N} r_w(n, \mu_s) e^{-j\pi n(\mu-\mu_s)}. \tag{3.63}$$

After cancelling imaginary components in the above series, the PSF becomes

$$\tilde{T}_B(\mu, \mu_s) = \frac{1}{2}\sqrt{\frac{1-\mu^2}{1-\mu_s^2}} \left[1 + 2\sum_{n=1}^{N} \operatorname{sinc}\left(\frac{nB\mu_s}{2f_0}\right) \cos\left[\pi n\left(\mu - \mu_s\right)\right]\right]. \tag{3.64}$$

The solution in (3.64) will exhibit degraded resolution at large incidence angles, due to the behavior of the sinc function. This is not the best estimate of the original scene because F^{-1} reconstruction does not compensate for tapering of the grating lobe patterns in STAR.

Inverse G-matrix reconstruction

A numerical method is introduced to account for fringe washing and to minimize the error between estimated and actual brightness images. The system of equations in (3.59) for $n = 0, 1, \ldots, N$ is expanded into a set of $2N + 1$ real-valued visibility samples,

$$V_l = \int_{-1}^{1} g_l(\mu)\, T_B(\mu)\, d\mu, \quad l = 1, 2, \ldots, 2N + 1. \tag{3.65}$$

where the g functions represent the even and odd grating lobe patterns of the STAR sensor,

$$g_l(\mu) = \begin{cases} r_w\left[(l-1)/2, \mu\right] \cos\left[\pi\left(l-1\right)\mu/2\right] / \sqrt{1-\mu^2} & \text{for odd } l \\ r_w\left[l/2, \mu\right] \sin\left[\pi l \mu/2\right] / \sqrt{1-\mu^2} & \text{for even } l \end{cases}. \tag{3.66}$$

The brightness scene T_B can be discretized into a set of P pixels spaced at uniform intervals on the μ axis. Then the system of visibility samples is written in matrix form as

$$V = GT, \tag{3.67}$$

where

$$V = \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_{2N+1} \end{bmatrix}, \quad T = \begin{bmatrix} T(\mu_1) \\ T(\mu_2) \\ \vdots \\ T(\mu_P) \end{bmatrix}, \tag{3.68}$$

$$G = \begin{bmatrix} g_1(\mu_1) & g_2(\mu_2) & \cdots & g_1(\mu_P) \\ g_2(\mu_1) & g_2(\mu_2) & \cdots & g_2(\mu_P) \\ \vdots & \vdots & \ddots & \vdots \\ g_{2N+1}(\mu_1) & g_{2N+1}(\mu_2) & \cdots & g_{2N+1}(\mu_P) \end{bmatrix}, \tag{3.69}$$

with pixels located at

$$\mu_p = 2\left(\frac{p-1}{P-1}\right) - 1 \quad \text{for } p = 1, 2, \ldots, P. \tag{3.70}$$

The rows of the G-matrix in (3.69) make up the STAR basis functions (grating lobe patterns) for the various element-pair spacings. It should be noted that the number of points P in the brightness vector is usually oversampled above $2N + 1$ so that the pixel size is fine enough to restore the image. Therefore, the inverse solution for (3.67) is under-determined. There is however a least-squares estimate of T, given by [74],

$$\tilde{T} = G'V, \quad \text{where } G' = G^t \left(GG^t\right)^{-1}. \tag{3.71}$$

G and G' matrices were computed for the benchmark STAR with $N = 255$, using $P \approx 6N$ pixels. The PSF of the sensor can then be found by combining the visibility response in (3.62) with the G' reconstruction technique in (3.71).

Signal degradation

To gauge the effects of fringe washing, the image reconstruction techniques discussed so far can be applied to the most extreme case, where a point source is located on the border of the scene. In Figure 3.7, the normalized point spread functions were computed for a source located 35° from nadir. For the ideal case where there is no fringe washing, the peak response is unity, and, as predicted by (3.57) for the benchmark STAR radiometer, the zero-crossing beam resolution is 10.0 km. Spatial resolution for the F^{-1} reconstruction case, which includes the effects of fringe washing in the visibility calculation, is significantly lower than the ideal response. The decorrelation between received signals in the array causes a 2.5 dB drop in the peak brightness level and a broadening of the beamwidth to 17.0 km. The pixels calculated using G' reconstruction are also plotted with the other two

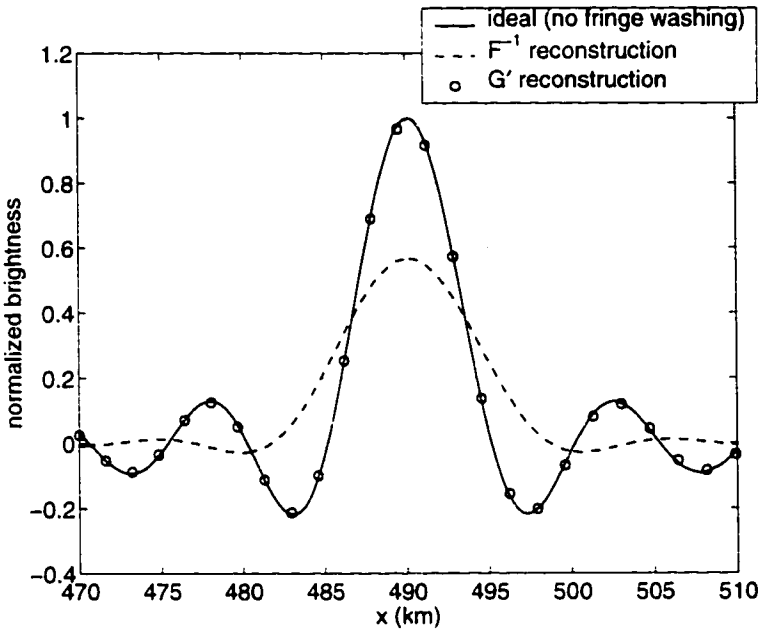


Figure 3.7: Estimations of the 27 meter STAR point spread function for a source located at 35° (490 km from nadir). The spatial frequency response is shown for the ideal (no fringe washing) case and for fringe washing cases where inverse Fourier and inverse G-matrix reconstruction techniques are applied. All PSFs are normalized to yield a peak value of 1 for a point source located at $x = 0$ km.

curves for comparison. Here the point spread function matches the ideal response exactly. As expected, G' reconstruction takes into account and compensates for the tapered grating lobes at large element spacings.

Although G' reconstruction yields the desired signal response, noise in the image will inevitably increase through this method. The estimated brightness in (3.71) is formed by adding a linear combination of inverse basis functions (columns of G') whose amplitudes tend to flare outward at oblique incidence angles. This flaring function is what allows the inversion algorithm to compensate for fringe washing. However, no improvement in SNR is made by boosting a signal that has already incurred some loss: the noise floor will be raised during the processing, along with the brightness signal. Given that SNR is essentially the same for both F^{-1} and G' cases, it follows from Figure 3.7 that, as a consequence of fringe washing, the system sensitivity is reduced by 2.5 dB at $\theta = 35°$.

3.3.3 Band-slicing technique

Estimated point spread function

The BDC receiver in Figure 3.5 can potentially remove the negative effects that arise from fringe washing. Let the original receiver bandwidth B be divided equally into M smaller slices with a bank of bandpass filters. For each subband processed by a correlator, the new fringe washing function will be dilated by a factor of M:

$$r_w(m,n,\mu) = \operatorname{sinc}\left(\frac{nB\mu}{2Mf_m}\right) \tag{3.72}$$

where f_m is the center frequency of each subband.

$$f_m = f_0 + \frac{B}{2M}\left[2m - (M+1)\right]. \tag{3.73}$$

and $m = 1, 2, \ldots, M$ is the subband index. Equation (3.59) is then modified to yield a set of $M \times N$ subband visibility samples:

$$V(m,n) = \int_{-1}^{1} \frac{1}{\sqrt{1-\mu^2}} T_B(\mu)\, r_w(m,n,\mu) \exp\left(-j\pi n f_m \mu / f_0\right) d\mu. \tag{3.74}$$

Using F^{-1} reconstruction, the impulse response for the mth subband is

$$\tilde{T}_B\{m\text{th band}\} = \frac{1}{2}\sqrt{\frac{1-\mu^2}{1-\mu_s^2}}\left[1 + 2\sum_{n=1}^{N} \operatorname{sinc}\left(\frac{nB\mu_s}{2Mf_m}\right)\cos\left[\pi n f_m(\mu-\mu_s)/f_0\right]\right]. \tag{3.75}$$

Each subband contains statistically independent noise, therefore the net brightness is found by summing the power over all subbands,

$$\tilde{T}_B = \sum_{m=1}^{M} \tilde{T}_B\{m\}. \tag{3.76}$$

The normalized estimate of the point spread function is then

$$\tilde{T}_B(\mu,\mu_s) = \frac{1}{2N+1}\sqrt{\frac{1-\mu^2}{1-\mu_s^2}}\left[1 + \frac{2}{M}\sum_{m=1}^{M}\sum_{n=1}^{N} \operatorname{sinc}\left(\frac{nB\mu_s}{2Mf_m}\right)\cos\left[\pi n f_m(\mu-\mu_s)/f_0\right]\right]. \tag{3.77}$$

The reconstructed image can be calculated for the benchmark STAR over a range of band divisions to assess the improvement in spatial resolution.

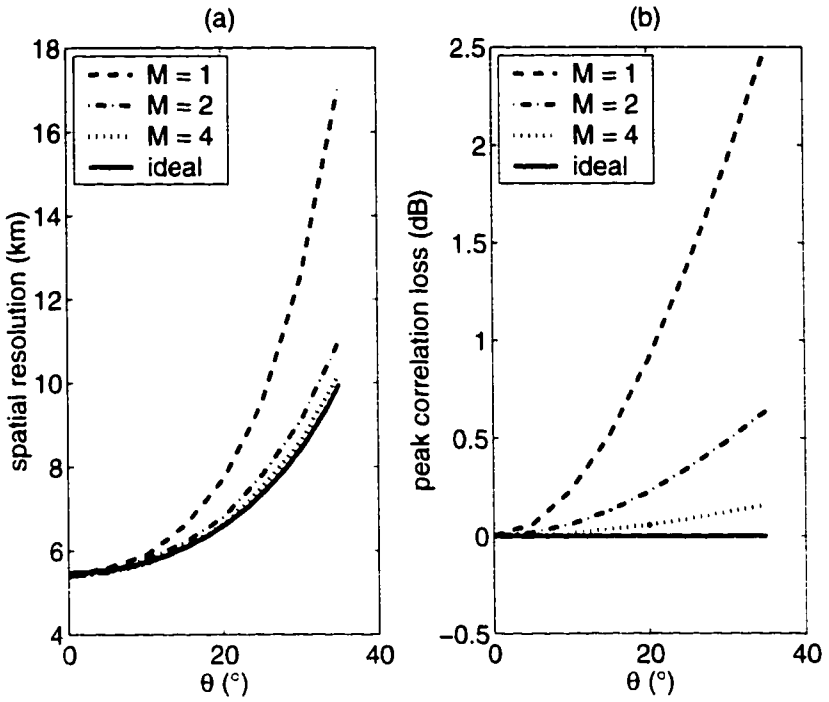


Figure 3.8: (a) Spatial resolution vs. incidence angle for a conventional STAR ($M = 1$), for a BDC instrument with $M = 2$ and 4 divisions, and for the ideal case. (b) Peak level correlation loss for the above cases.

Numerical results

The BDC STAR point spread function in (3.77) was computed over the field of view for several different values of M. Figure 3.8 shows a plot of the resulting spatial resolution and peak correlation loss compared to the ideal case. With just 2 subbands, there is already a marked improvement in resolution from 17.0 km to 11.0 km at 35° incidence; with $M = 4$, the resolution approaches a nearly ideal value of 10.2 km. Also, the correlation loss at the peak of the impulse response is reduced greatly with only a few band divisions. Compared to a conventional STAR with a 2.5 dB correlation loss, the BDC loss figure can be improved to 0.6 dB (for $M = 2$) or as low as 0.2 dB (for $M = 4$).

The STAR sensor considered here quickly converges to the "no fringe washing" case with a relatively small number of subband correlators. This implies that noise in high spatial frequency visibility samples can be reduced more effectively in a STAR sensor that employs

BDC than in a sensor that used conventional correlators and G' post-processing.

Band-slicing was illustrated for the simple case of a uniform array distribution. But in a real world application, some amount of amplitude tapering would be designed into the reconstruction algorithm to reduce side lobe levels (e.g., ringing seen in the ideal response in Figure 3.7) and to improve the efficiency of the synthesized beam. An actual 10 km resolution sensor would therefore require a maximum baseline greater than 27 m. The advantage gained through band-slicing is that, by giving the designer control over the shape of the fringe washing function, spatial resolution requirements can be satisfied over the entire field of view for an appropriate array size and number of band divisions.

The BDC method is especially well suited for present day STAR systems that transfer signal processing complexity away from analog hardware by digitizing the received brightness signals at IF or RF frequencies. Given the availability of DSP integrated circuits that run at 10^9 operations/second, it would be practical to develop L-band BDC radiometers having up to 4 frequency selective bands.

3.4 Summary

The last two chapters have been dedicated to an analysis of the noise statistics and phase stability for direct-sampling digital radiometry. By modeling two important degenerate cases in STAR—the total power radiometer and the correlation radiometer—it was found that direct-sampling at 2–3 bit resolution will yield nearly the same NEΔT as conventional analog receiver technology. Decorrelation due to timing jitter between channels is expected to have a negligible impact on the sensitivity of a correlation DSDR. Also, the digital receiver architecture lends itself to a novel band division correlation processor that can alleviate fringe washing in large STAR arrays.

A/D converter technology will presently support direct digitization of microwave signals extending up to 1.4 GHz with at least 2 bits of resolution and with low timing jitter. From

the theoretical framework developed so far, the results suggest that it would be valuable to build a working L-band DSDR, one whose performance can be tested and eventually assessed for advanced radiometer configurations such as STAR.

CHAPTER 4

The 1.4 GHz DSDR Prototype: Design and Performance Evaluation

4.1 Design Objectives

As a first step toward validating the direct-sampling concept, I set out to design and build a prototype total power DSDR radiometer, operating at 1.4 GHz. A series of experiments were performed with DSDR in the lab and field to characterize the radiometric sensitivity modeled in Chapter 2. Through the design and testing phases, our Microwave Geophysics research group (MGP) has gained experience with direct-sampling and with several technologies that complement it.

Although instrument constraints on power consumption, weight, and processing speed become important for practical satellite applications, these issues will not be considered in the proof-of-concept development of DSDR. For our ground-based system, most of these design constraints can be relaxed without precluding our evaluation of the radiometer's fundamental noise limitations.

This new radiometer system carries a special significance for MGP because it would become the first operational sensor that we have produced at L-band frequencies. As such, the radiometer's potential utility in land-surface hydrology experiments has influenced our choice of requirements and features as the design has evolved. To satisfy some of the short term science objectives within our group, the field-grade version of DSDR will be designed

with flexibility in mind so that the system can be configured for fully polarimetric operation in upcoming field experiments. In the long term, our goal is to build the framework for direct-sampling technology so that it can eventually be integrated into an advanced, multi-element STAR mission.

4.2 Approach

The second tower mounted radiometer system (TMRS2), a suite of 19-85 GHz radiometers developed by Kim in the early 1990's [27], has served as a useful reference for DSDR. By studying Kim's system, I was able to emulate circuit ideas that had been proven in the field and, at the same time, recognize any deficiencies that could be improved upon as I designed my L-band radiometer.

I concluded from lessons learned with the TMRS2 hardware that there would be advantages to making the DSDR electronics more autonomous. First, embedded systems technology has advanced substantially in the last few years, making microcontroller boards less expensive and more compact while offering more features. Design automation tools that accompany these processors allow the user to easily develop and modify the controller's software. And for radiometry, tasks that must be performed in real time, such as receiver temperature control or integration of the brightness signal, can be performed locally by the microcontroller instead of occupying the CPU time of a remote computer.

By adding intelligence to DSDR, the radiometer system can be designed to communicate across several different types of computer platforms. For instance, if radiobrightness looks are processed locally, the results can be telemetered back to a stand-alone computer at a low data rate via a serial link—RS-232 or equivalent. This serial communication protocol is standardized for the IBM PC, Apple, and so on, and for a range of data acquisition software products. DSDR could therefore be adapted to other computer platforms or new software releases.

The DSDR electronics were designed so that, wherever possible, the radiometer's subsystems could be configured through software and firmware, not hardware. Specialized circuitry in TMRS2 has largely been superseded in the new DSDR by firmware stored in the embedded controller's EPROM or by field programmable gate arrays, whose logic can be reconfigured without rewiring connections on a circuit board. With this approach, the radiometer system is expandable and can be modified to work in one of several modes—total power, interferometric, or polarimetric—with minimal changes to the physical hardware.

The limited funding and labor available in a university research group also influenced our approach toward building what would become a rather complex field-grade radiometer system. When it made sense economically and technically, I used off-the-shelf components or at least tried to outsource the design of specialized components. However, when the performance of a commercial product became questionable, or where the use of that product would compromise our capacity to expand the hardware for future needs, I chose to develop my own homemade circuitry.

DSDR comprises several analog and digital circuit boards which must be designed in-house. It became apparent that MGP would have to choose between either building up the infrastructure in the lab to design printed circuit boards (PCBs) or adopting less sophisticated means, like prototyping with "breadboard" panels and wire-wrap connections, to fabricate the DSDR electronics. PCBs have the advantage of offering multi-layered ground planes for high-speed circuitry. PCBs are also well suited for surface-mount components, and, once the design is final, the boards can easily be mass produced. The disadvantages are that there are costs associated with purchasing PCB design automation software, learning how to use that software, and coordinating the board production with an outside vendor. These costs are recovered only by producing large quantities. Furthermore, design errors are usually not found until after the first production cycle, making it necessary to go through several design iterations.

In contrast, wire-wrapped breadboards, though not as attractive for mass production, are inexpensive and easy to modify. Using careful construction techniques described in the next section, these breadboards can be made to reliably operate at clock speeds of 10-20 MHz, which will be shown to be sufficient for the DSDR proof-of-concept. I decided that wire-wrapped panels would be the more expedient solution for building parts of the prototype hardware.

4.3 Hardware Development

4.3.1 Overview

The block diagram in Figure 4.1 shows how the electronic subsystems in DSDR are interfaced to one another. The prototype DSDR operates as a single-channel, total power radiometer, detecting brightness emissions within the protected radio astronomy band from 1400 to 1427 MHz. In addition to direct-sampling, there are several important technologies that have been incorporated into the design: amplitude compensated horn antennas, gallium-arsenide MESFET low noise amplifiers (LNAs), thermoelectric cooling devices (TECs), high speed emitter-coupled logic (ECL), field-programmable gate arrays (FPGAs), and embedded microcontroller systems.

Table 4.1 summarizes the receiver specifications for DSDR. A total power architecture was chosen as being most suitable because, as tests would later show, the dynamic range of the A/D converter at 1.4 GHz would be sufficient to detect the range of brightness temperatures encountered in Earth remote sensing, from cold to hot targets. DSDR uses a somewhat conservative sampling rate of 10 Msamples/second—below the Nyquist rate defined by the 20 MHz receiver bandwidth—so that parasitic high frequency effects could be avoided on the homemade prototype boards. For radiometry, it is not necessary to sample at the Nyquist rate or higher, because the detect output is only an estimate of signal power and not a reconstructed version of the original waveform. While a slower sampling rate will

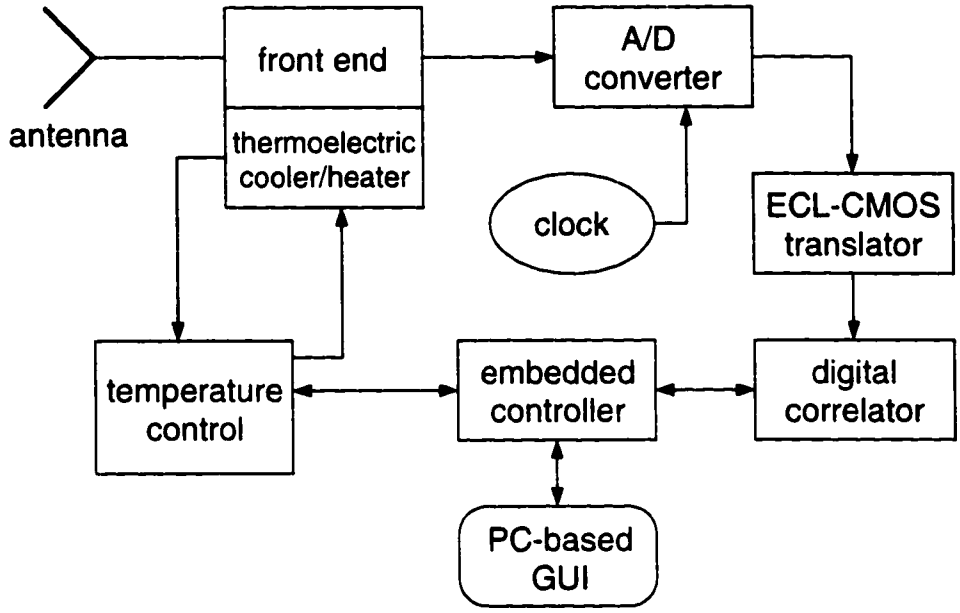


Figure 4.1: Block diagram of the hardware components in the total power DSDR.

center frequency (f_0)	1413.5 MHz
bandwidth (B)	20 MHz
A/D resolution	$\geq$ 2 bits @ 1.41 GHz
sampling rate (f_s)	10 MSPS
system gain (G)	90 dB
receiver noise temperature (T'_{REC})	100 K nominal
temperature stability (ΔT_p)	12 mK rms minimum
NEΔT (3 bit, τ = 1 s)	0.2 K

Table 4.1: L-band DSDR receiver specifications.

require a longer integration time to achieve comparable sensitivity (Section 2.4), integration time can be traded for more reliable circuit operation in the case of DSDR, which operates as a static, ground based sensor, viewing brightness signals that are stationary over short time periods.

The electronic boards and subsystems in DSDR are listed in Table 4.2. Most of the circuitry was fabricated by hand on single-sided, epoxy-glass composite prototype boards having a single ground plane. On-board interconnections were often made using wire-wrapping techniques, especially for the digital circuitry, so that modifications could be made without having to resolder the components. To reduce interference and high frequency

name	description
TEC box	RF front end, thermoelectric cooler/heater, supporting circuitry
A board	SPT7610 A/D evaluation board
G board	power regulation for A/D board
X board	ECL-CMOS translator for digital data stream
M board	embedded microcontroller, FPGA digital correlator
T board	temperature sensing and control
C board	master clock for A/D converter
R board	front end regulation, driver for antenna/reference switch
S board	driver for TEC duty cycle

Table 4.2: Nomenclature for DSDR subsystems.

ringing, special care was taken to buffer all I/O signals with line drivers, to isolate analog and digital ground planes, to provide on-board voltage regulation, and to adequately filter voltage supply lines. The front end electronics were mounted onto a specially machined aluminum plate to provide mechanical and thermal stability. Aluminum cases, electrically tied to chassis ground, enclose every board to minimize EMI and crosstalk. Appendix B contains schematics for the first total power prototype circuitry (DSDR1).

4.3.2 A/D converter

The DSDR proof-of-concept design is centered around the SPT7610, a flash A/D converter made by Signal Processing Technologies (SPT) that features a wide input bandwidth up to 1.4 GHz. Table 4.3 shows the specifications and features for the SPT7610 [65]. Before deciding on this converter, I surveyed a number of devices from different companies. The product search was not always straightforward, partially because the commercial technology for direct-sampling above 1 GHz was just beginning to emerge and its capabilities were not always well defined. [1] Also, many data converters on the market have been oriented toward communications or radar applications that digitize at IF, with requirements that are often the converse of those in radiometry: communications receivers tend to use large resolution

[1] I conducted the search for data converters in the spring of 1997 and, shortly thereafter, froze the design once a suitable device was found. Since then, the technology has advanced rapidly; by early 2000, researchers had developed a radiometer testbed that could directly sample RF waveforms extending up to C-band frequencies, using a recently released silicon bipolar A/D converter [53].

full scale resolution	6 bit
maximum sampling rate	1 GSPS
architecture	flash conversion, ECL logic
small signal bandwidth	1.4 GHz
power dissipation	2.85 W (nominal)
aperture jitter	2 ps rms

Table 4.3: Specifications for the SPT7610 A/D converter.

($\geq$ 8 bits), a high sampling rate (100-500 MSPS), and a modest input bandwidth (50-250 MHz); the requirements for DSDR are the opposite of this—a wide input bandwidth becomes essential while the requirements for quantization resolution and sampling rate can be relaxed.

SPT7610 capabilities

After surveying data converters from several vendors, I found that the SPT7610 offered the highest small signal bandwidth, which is perhaps the most critical specification for DSDR. SPT defines small signal bandwidth as the frequency at which the sampler and digitizer attenuate the analog input waveform by 3 dB, given that this analog signal is set to a level 20 dB below the full input scale of the A/D converter. For example, given that the SPT7610 has a full scale range of 1 Vpp, a resolution of 6 bits, and a small signal bandwidth of 1.4 GHz, the quantization voltage for one least significant bit (LSB) is

$$v_0 = \frac{1\text{ V}}{2^6} = 15.6\text{ mV}. \tag{4.1}$$

the small signal analog input level is defined at 100 mVpp, and the quantization resolution at 1.4 GHz is

$$\frac{100\text{ mV} - 3\text{ dB}}{v_0} = 4.5\text{ levels}. \tag{4.2}$$

From this estimate, the SPT converter would provide at least 2 bits of resolution necessary for directly sampling and digitizing the RF waveform at 1.4 GHz.

ECL technology tradeoffs

The SPT7610 employs high speed technologies that have influenced the design of DSDR. This device uses a flash conversion architecture—that is, a ladder network of comparators that approximates the transfer function described in Section 2.3. Also, the integrated circuit is based on high speed ECL and bipolar silicon technology. Bipolar ICs exhibit excellent frequency performance as the device transconductance is higher than that of MOSFETs, and the input bandwidth is not limited by the presence of gate capacitance. However, speed is gained at the expense of increased power consumption. Unlike CMOS electronics, ECL will dissipate power and generate heat even when the logic gates are static. I chose to trade some power efficiency in exchange for the larger bandwidth associated with this ECL-based chip, which typically dissipates $\sim$ 3 W of power. The diverse set of supply voltages in ECL (-5.2 V negative supply line and -2.0 V reference line) also added circuit complexity to DSDR: special voltage regulators and ECL-CMOS translation circuitry were required to power the SPT7610 and to make its output logic compatible with the other DSDR subsystems.

Evaluation board vs. hand-crafted circuitry

I used the vendor's EB7610 evaluation board, designated hereon as the "A board," to reduce engineering costs and to ensure that the SPT7610 performed up to its specifications. At high frequencies, it is essential to use this kind of multi-layer printed circuit board for proper operation. The board also offers convenient features like built-in reference circuitry, analog-digital noise isolation, and heat sink design for the converter chip. However, some A board functions are superfluous for DSDR operation and end up increasing the complexity of the prototype radiometer. For example, the evaluation board includes a divide-by-16 decimation circuit that discards digital samples from the A/D output to accommodate a conventional D-type board-to-board connector, which can not support data rates as high as

1 GSPS. Consequently, the DSDR sampling clock frequency must be increased by a factor of 16, from 10 MHz to 160 MHz, leading to more complicated circuitry for other sections of DSDR.

4.3.3 Antenna

The L-band antenna in DSDR is based on an amplitude compensated septum horn design with low side lobe levels (SLL) and improved main beam efficiency (MBE). Previously, the radiometers designed by MGP have used standard gain horn antennas, whose first SLL in the E-plane is fixed at -13 dB due to the uniform field illumination in that dimension. Side lobes can cause significant errors in the accuracy of a ground-based radiometer when brightness energy is detected outside of the desired target area. (This problem is especially severe during a cold sky calibration, because the side-lobes may pick up energy from relatively hot targets like trees and buildings.)

For field experimentation, our group also sought an antenna design with relatively high directivity, the capability for dual (horizontal and vertical) linear polarization, low electrical loss, and rugged construction for use in harsh, outdoor environments. After investigating several possible technologies, we decided to outsource the design of pyramidal septum horn antennas, shown in Figure 4.2, to Seavey Engineering. In this design, two metal plates running from the main aperture to the throat of the antenna create an array of 3 smaller apertures aligned along the E-plane. Therefore the field amplitude along this plane is tapered, similar to the cosine field distribution that naturally arises in the H-plane of the TE_{10} guided wave [49]. Given a nearly symmetric, tapered field distribution in both E and H-planes, the far-field pattern of the antenna will exhibit low side lobes and high main beam efficiency.

Table 4.4 lists the septum horn specifications and electrical test results reported by Seavey [43]. Two identical aluminum antennas were produced so that eventually the DSDR

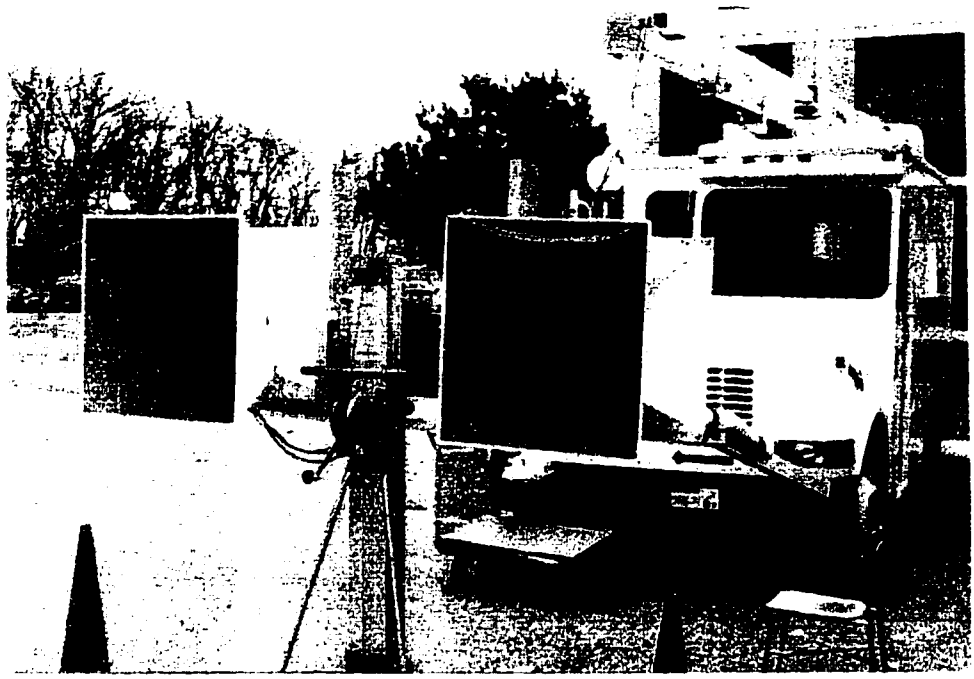


Figure 4.2: The L-band pyramidal septum horn antennas deployed on our truck mounted radiometer system. Two vertical septum plates are visible in each aperture. In this configuration, both antennas are horizontally polarized.

system could be configured to accommodate fully polarimetric (H, V, and cross-pol) brightness measurements. A large $29'' \times 31''$ aperture was needed to attain a high enough gain at 21 cm wavelength for outdoor field studies. Given the large physical dimensions, the antenna actually became the main mounting structure for the radiometer, with DSDR electronics built around a mounting flange welded near the throat of the horn. A polycarbonate window having high transmissivity at L-band frequencies is attached to the face of the aperture to prevent animals or debris from entering the antenna. Also, to maximize the radiation efficiency and thus reduce antenna thermal noise emissions, the inner surface of the horn is coated with a highly conductive, corrosion-resistant gold iridite finish.

Figure 4.3 shows the pattern response from test data taken on an outdoor range. Through the septum design, the E-plane side lobe levels are reduced from -13 dB for a standard gain horn to -20 dB for the Seavey antennas. In both planes, the antenna patterns show good symmetry and comparable half power beamwidth (HPBW) responses

gain	18.9 dBi
E-plane HPBW	22.5°
H-plane HPBW	20.0°
E-plane SLL	−20.0 dB
H-plane SLL	< −30.0 dB
VSWR	1.08 : 1
polarization	linear (H or V)
on-axis cross pol. isolation	−34.0 dB
antenna maximum dimensions	29.25″ × 31.25″ × 44.0″ (H×W×L)
antenna weight	75 lbs.

Table 4.4: Summary of specifications and electrical test data for the Seavey L-band septum horn antennas [43].

of 20-22.5°.

I estimated the antenna's main beam efficiency by assuming azimuthal symmetry for the two measured beam patterns. For a simple, rotationally symmetric pattern, the azimuth angle variable disappears from the calculation, and MBE can be expressed as

$$\eta_M = \frac{\text{main beam solid angle}}{\text{pattern solid angle}} = \frac{\int_0^{\theta_M} F_n(\theta) \sin\theta \, d\theta}{\int_0^{\pi/2} F_n(\theta) \sin\theta \, d\theta}. \tag{4.3}$$

where F_n is the normalized radiation pattern and θ_M delimits the main beam edge, defined at 20 dB below the main lobe peak. MBE is calculated for the two cases representing the two principal plane patterns shown in Figure 4.3, resulting in efficiencies of 89.4% for the E-plane pattern and 96.7% for the H-plane pattern. The actual efficiency will be somewhere between these two figures: as a first-order estimate, the average of these percentages is taken, yielding $\eta_M \approx 93.1\%$ for the L-band septum horn.

4.3.4 Front end

The L-band front end in DSDR is designed to provide about 90 dB of gain and 20 MHz of system bandwidth before detection by the A board. The amplifier chain consists of three GaAsFET LNA modules designed by Miteq Corporation, each module having a 3-stage transistor design. To minimize the receiver noise temperature, the first amplifier module in the signal chain, LNA1, is chosen with a very low noise figure (F_1 = 0.4 dB) and high

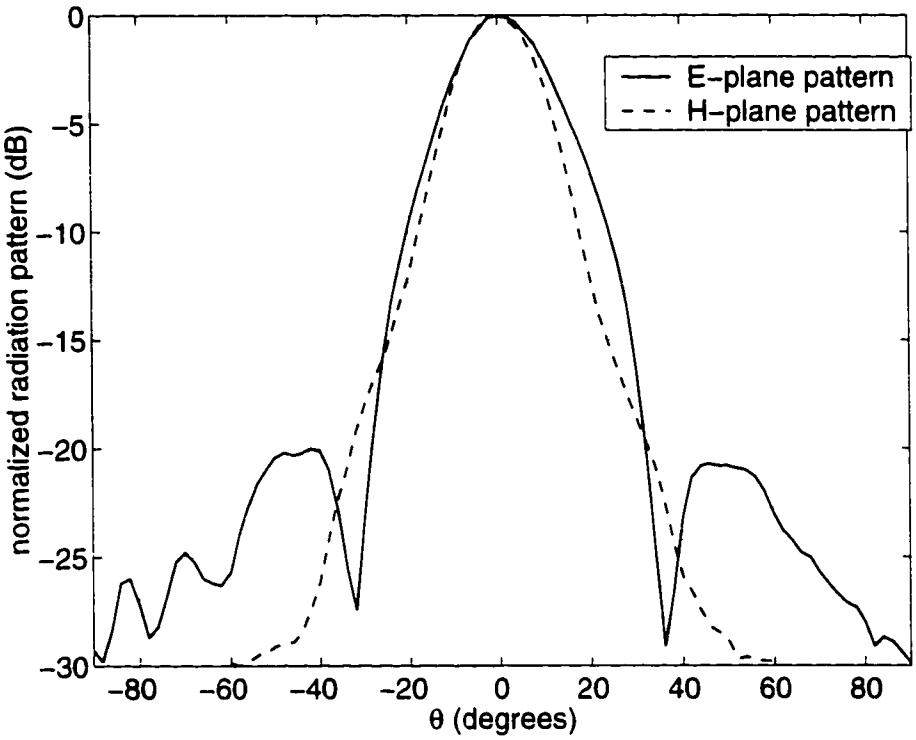


Figure 4.3: E-plane and H-plane radiation patterns for the L-band septum horn antenna.

gain (G_1 = 42.4 dB) at 1.4 GHz, and this LNA is brought in close proximity to the antenna terminal to reduce emissions from lossy cables.

There is an electromechanical microwave single-pole/double-throw (SPDT) switch between the antenna and LNA1 that allows brightness measurements from the antenna or from a temperature controlled coaxial reference load. By periodically viewing this reference load, it is possible to compensate for long term variations in the front end gain which can degrade the accuracy of DSDR over time. A downside to this switch, which will be discussed later in Section 3.6, is that 2.2 W of continuous power must be applied to the solenoid during reference load observations, causing the switch to dissipate heat and interfere with the front end temperature regulation.

Flexible and semi-flexible SMA coaxial cables connect the antenna, SPDT switch, and LNA components and introduce up to L = 0.4 dB of attenuation before LNA1. Given the large gain G_1, noise sources that arise after LNA1 have a negligible effect on the overall

receiver performance, thus the analog receiver noise temperature (referred to the antenna terminal) is

$$T'_{REC} = T_0 (L - 1) + L T_{REC1} \approx 59 \text{ K}. \tag{4.4}$$

where $T_0 = 290$ K is taken to be the standard physical temperature of the receiver and $T_{REC1} = T_0 (F_1 - 1) = 28.0$ K is the noise temperature of the first LNA. [2]

The gain required for the front end can be estimated by considering how much T'_{REC} must be amplified to meet the detection resolution criterion in (4.2). At 4.5 levels of digitization, from (4.1) the ADC sees an rms input voltage of

$$sv_0 = \frac{4.5}{6} (15.6 \text{ mV}) = 11.7 \text{ mV rms} \tag{4.5}$$

which translates to a signal power of

$$P_{ADC} = \frac{(sv_0)^2}{Z_0} = -25.6 \text{ dBm}. \tag{4.6}$$

given that the SPT7610's input impedance is matched to $Z_0 = 50\,\Omega$. From (4.4), the minimum input referred power to the receiver is

$$P'_{REC} = k T'_{REC} B = -107.9 \text{ dBm}. \tag{4.7}$$

where $k = 1.38 \times 10^{-23}$ J/K is Boltzmann's constant. Therefore, the minimum gain requirement for the front end is

$$G_{min} = \frac{L P_{ADC}}{P'_{REC}} \approx 83 \text{ dB}. \tag{4.8}$$

In practice, the LNAs' net gain requirements are usually overestimated so that attenuator pads can be added between amplifier modules in the final design to fine tune the gain. The pads are also needed to improve the impedance match between LNAs and reduce the

[2] In practice, the receiver noise temperature may be greater than the 59 K estimate. I often heated the DSDR front end several 10's of K above room temperature during the hardware testing phase; furthermore, additive noise introduced during the A/D conversion will increase the input-referred noise temperature. In the following experimental sections of this work, I will use $T'_{REC} = 100$ K and $T_{SYS} = 400$ K as realistic upper bounds for the actual DSDR hardware.

chance of oscillation. To be safe, I first selected the 3 LNA modules to have a combined gain of 120 dB, and later, through experimentation, I fine tuned the system gain to $G \approx 90$ dB using coaxial attenuators. This gain provides the optimum dynamic range for DSDR (2-3 bits of sampling resolution) as the apparent antenna temperature of natural targets varies from 0–300 K.

A narrowband cavity resonator filter is designed into the front end to pass frequency components within the 1400–1427 MHz band allocated for passive radio astronomy research. This 5-pole filter has a center frequency of $f_0 = 1413.5$ MHz, a 3 dB bandwidth of $B = 20$ MHz, and a 30 dB bandwidth of 40 MHz to filter out transmissions from adjacent mobile radio bands. The cavity resonator design was chosen for its low insertion loss of ≤ 1 dB at the center frequency. After experimenting with the filter placed at various locations in the front end signal chain, I found that the position between the first and second LNAs gave the best compromise between acceptable dynamic range and receiver noise figure.

For total power radiometry, physical temperature variations in the LNAs can negatively impact the radiometer's precision due the corresponding changes in system gain. (The Miteq amplifiers used here have a maximum temperature coefficient of -0.02 dB/°C per module.) All LNA stages and other front end components that are sensitive to temperature change—for example, the lossy components placed before LNA1—are mounted onto a custom machined $4.5'' \times 6''$ aluminum plate which is coupled to the TEC. Thermally conductive silicon compound is applied between the front end components and cold plate, and all components are bolted down to the plate to ensure good thermal contact.

An auxiliary circuit designated as the R board provides support electronics for the front end. The R board includes a 15 V 3-terminal regulator that supplies power to the LNAs and a 12 V regulator with solid-state relay (SSR) that controls the position of the antenna/reference SPDT switch. Bypass capacitors and ferrite beads are liberally applied to reduce ripple on the power lines.

4.3.5 Temperature control

TEC box

DSDR's front end enclosure, or TEC box, was designed to provide precise thermal regulation, to minimize electromagnetic interference, and to provide mechanical stability for the front end circuitry. Temperature stability becomes critically important for a total power radiometer because even a small change in the physical temperature of the receiver can lead to large fluctuations in gain, thus degrading NEΔT. Historically our group has used a feedback-controlled heat source to add a positive temperature bias for thermal control of the front end. While this method worked reliably for TMRS2 in cold environments like the North Slope of Alaska, it lead to overheating and the eventual failure of the front end electronics in hot environments such as the Midwestern U.S. during the summer season. We sought a new method that would give us the option of controlling the receiver temperature through cooling so that the reliability and noise figure of the front end could be improved.

The effectiveness of thermoelectric cooling devices for radiometer temperature control has been demonstrated previously by Tanner [73]. Tanner's system actually contains two TECs: one for precise temperature control of the low noise amplifiers, and one that provides rough regulation of an antenna/Dicke switch assembly and removes heat energy from the enclosed radiometer system. I adopted a similar technique in our design of the TEC box, which can accommodate either a single or double-TEC system for temperature control. Initially, we chose to use a single thermoelectric device made by Teca Corporation, model AHP-300, to test its stability and heat transfer capabilities.

Figure 4.4 shows the inner assembly for the prototype TEC box. This enclosure is made of an aluminum frame that houses two chambers above and below the thermoelectric cooler; a "cold" chamber on top encloses the L-band front end electronics, and a "warm" chamber below transfers heat out to the antenna mounting flange. The AHP-300 runs off of a 24 Vdc, 6.3 A power source. When fully powered, the TEC removes 78 W of heat from the cold

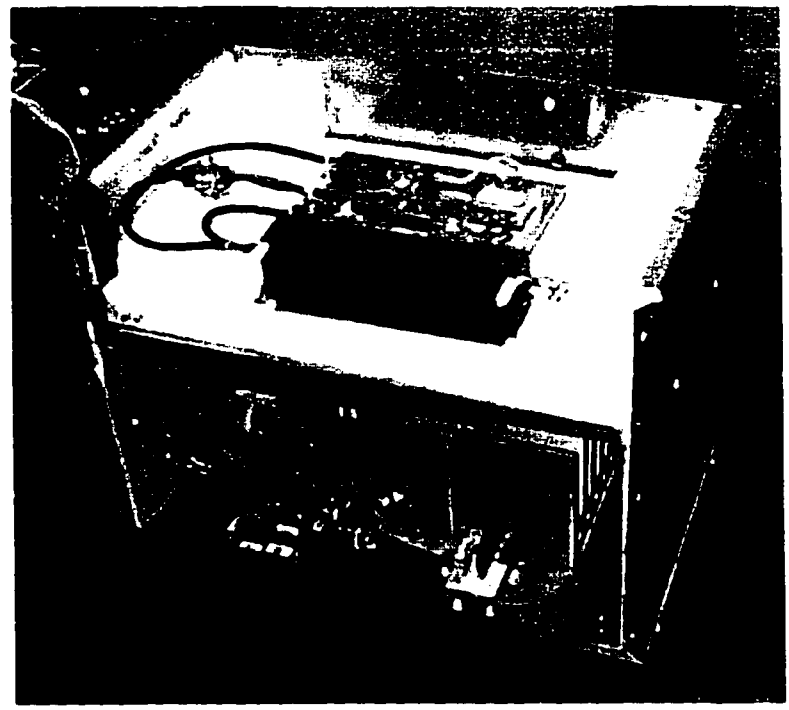


Figure 4.4: The TEC box enclosure with L-band front end and thermoelectric cooling chamber.

junction coupled to the front end plate. In addition to cooling capabilities, this TEC has an embedded 72 W heating element for regulating temperature the traditional way, by adding heat to the system.

The TEC box is mounted as close as possible to the antenna's RF terminal so that the coaxial cabling to the first LNA is kept short. A 6″ semi-flex RG402 cable, connecting the antenna to the front end SPDT switch, introduces 0.07 dB of insertion loss, which only contributes 5 K of equivalent noise temperature to the receiver noise specified in (4.4).

The cold junction of the TEC is a flat, 4.5″ × 6″ metal surface that conforms to the front end aluminum plate. Silicon compound is applied between both metal surfaces before they are bolted together to yield a large contact area and high thermal conductivity. A fan on the underside of the TEC pumps air through the hot junction heat sink fins and circulates this air downward to heat sinks on the bottom of the enclosure. All faces of the metal enclosure, except for the bottom face, are lined with polystyrene insulation so that

the lowest thermal resistance path is directed toward the antenna flange. To further reduce temperature variations and electromagnetic interference, the front end plate is capped with an insulating material that is aluminized on the inner surface.

The output level of the thermoelectric cooler is controlled by switching the 24 V power supply at some duty cycle, from 0% to 100%, whose value is updated periodically by a feedback control system in DSDR. A high current SSR that switches power to the AHP-300 is mounted on the duty cycle driver (S board) residing in the lower chamber of the TEC box.

T board design

The T board is a homemade, mixed-signal CMOS circuit that generates temperature sensing and control signals for the closed-loop thermal regulation of the front end. Communication between T and DSDR's microcontroller is carried out via the *TempCon1* bus, which is comprised of data, address, and chip select lines. In the board layout, I incorporated techniques to reduce crosstalk between the analog and (noisy) digital sections so that the temperature sensing circuitry can achieve high precision.

Before designing the T board, I considered using one of the popular off-the-shelf PID temperature control modules (e.g., from Omega Corporation). Most of these products are intended for manufacturing control systems, though, where the user desires a quick response time but can tolerate low precision (± hundreds of mK) once a settling time is reached. For radiometry, the requirements are the opposite—that is, a slow aging period of 2 hours or more is tolerable before the radiobrightness experiment, but after this time, high temperature stability on the order of 10's of mK is needed to contain the NEΔT. Inquiries to several vendors had cast enough doubt in my mind about the precision of commercial controllers that I decided to design my own controller board and feedback algorithm, with the goal of attaining better than 0.01 K measurement precision.

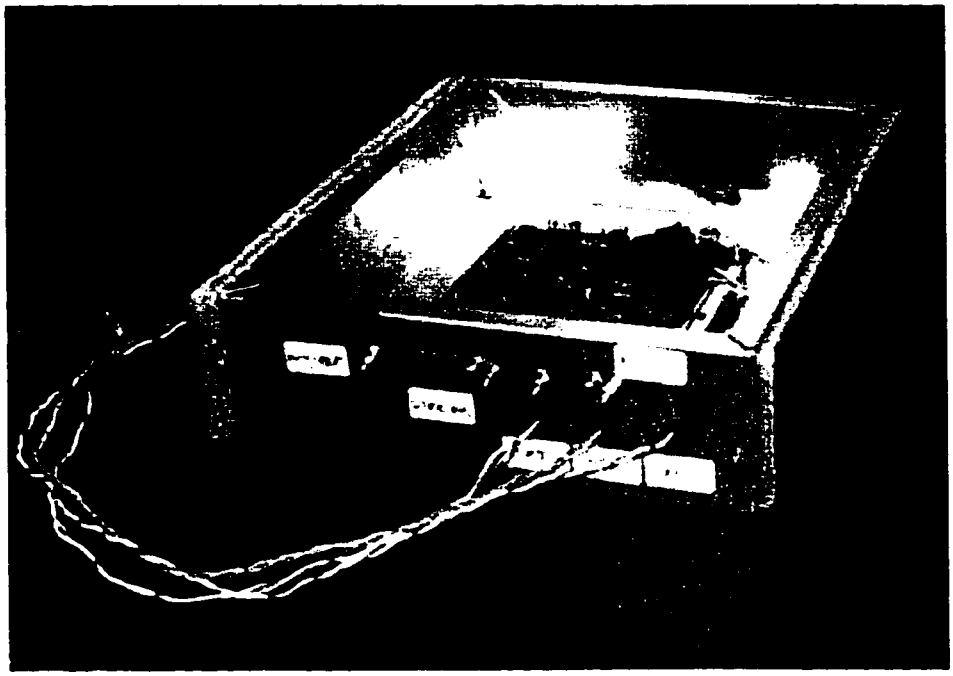


Figure 4.5: T board for temperature sensing and control.

The T board, shown in Figure 4.5, is a blend of circuit ideas that have either been proven in TMRS2 or developed especially for DSDR. The thermal sensing section consists of 44032-type encapsulated thermistors (having $\pm 0.1°C$ interchangeability), along with wheatstone bridge circuitry, to generate a set of analog voltages proportional to the physical temperatures measured at several points in the front end. Three thermistor channels are reserved for measuring the temperatures of the front end plate, reference load, and antenna. The signals generated by these channels are sampled and digitized with a 12-bit A/D converter and are compared to a zero-offset reference signal so that common mode noise can be removed.

A real-time duty cycle generator is designed into the T circuitry to provide precise control of the thermoelectric cooler or heater. This circuit consists of an 8-bit duty cycle register, a digital sawtooth waveform generator, a comparator circuit, and a current amplifier to drive the TEC's solid-state relay. When the DSDR microcontroller writes a byte value (0–255) to the duty register, this value is compared to the sawtooth wave, which has a period of about 5 s. Counter values less than the duty byte produce an ON signal and values greater

than the duty byte produce an OFF signal. The resulting duty cycle waveform, ranging from 0–100%, is buffered and sent to the S board driver, thus defining the time-averaged output of the TEC. By updating this duty cycle value periodically, DSDR can make fine adjustments in the effective amount of heat removed from the front end.

The topology of power and ground buses on T were specially arranged to reduce crosstalk between the analog and digital circuitry for precise temperature measurements. First, separate voltage regulators are used for the digital logic and for the ±5 V bipolar power lines of the thermistor network. Second, the A/D converter circuitry employs a separate ground plane and single point analog-digital ground connection in order to isolate digital switching currents from the sensitive analog section.

PID feedback algorithm

I devised a proportional-integral-differential (PID) algorithm, similar to the one in Kim's TMRS2 system, to provide closed-loop control for the physical temperature of the front end. The PID control algorithm processes the error signal between the desired (set) temperature and the actual (measured) temperature of the front end. Given the error signal's present value, its history, and its instantaneous rate of change, the controller can dynamically respond to front end temperature fluctuations by adjusting the TEC's duty cycle to minimize this temperature error.

PID processing software is stored in the program space of the M board's microcontroller. Once per minute, the controller polls the T board for new temperature data, calculates a new duty cycle value, and writes this updated value to the T board register. The optimal choice for proportional, integral, and differential feedback coefficients depends on the response of the front end thermal mass to outside driving forces that add or remove heat from the system.

In the frequency domain, the PID control transfer function which operates on the tem-

perature error signal is

$$H_{PID}(s) = K\left(1 + \frac{1}{T_I s} + T_D s\right), \tag{4.9}$$

where K, T_I, and T_D are the proportional, integral, and differential feedback coefficients and $s = j\omega$ represents the frequency. One useful rule of thumb for making a good "first guess" for these coefficients is given by the Ziegler-Nichols tuning criteria. This rule states that for a system having an open-loop step response rate R and lag time L, the PID coefficients which best emulate a critically damped, closed-loop response are [15]

$$K = 1.2/RL, \quad T_I = 2L, \quad T_D = 0.5L. \tag{4.10}$$

The rules in (4.10) can be combined with trial-and-error experimentation to fine tune these coefficients for a highly precise, steady-state temperature response.

Initial testing

The absolute accuracy and relative precision of the temperature sensors were tested by applying the thermistors to the aluminum front end plate and measuring short term temperature variations. Each thermistor measurement is an average of 10 separate samples, which are converted using the manufacturer's resistance-to-temperature transfer curves. The final T board sensing circuit exhibited an rms deviation of 4 mK and an absolute accuracy error of ≤ 0.25 K over ~ 10 s time.

In the preliminary design, I found that thermal pulsing from the TEC's duty cycle would register as a detectable signal and cause errors in the plate thermistor readings. In fact, using an aluminum plate thickness of $1/4''$ and a duty period of 10 s, the temperature signature that arose from powering the TEC on and off caused peak fluctuations of 70 mK that propagated through the plate in 5 s time—exactly 180° out of phase with the switching TEC. To improve the stability of the feedback system and attenuate this thermal pulsing, I retrofitted the front end onto a thicker $3/8''$ aluminum plate (having a larger heat capacitance) and decreased the duty cycle period to about 5 s.

I tested the open-loop step response of the thermoelectric cooling system, loaded with the front end electronics, beginning from an unpowered condition and then applying a constant duty cycle at $t = 0$. With the hot junction of the TEC exposed to ambient air, the step response had a reaction rate of $R = -6.5°C$/minute at 100% duty. Assuming a lag response time of $L \approx 1$ minute, which is defined by the update period of the PID software, I calculated suitable temperature control coefficients using the relations in (4.10). DSDR's closed-loop thermal control performance will be discussed in Section 4.6.1.

4.3.6 Microcontroller/correlator (M) board

The M board contains the central processing and control logic that allows DSDR to function autonomously. This board includes a Z-World SmartCore microcontroller and Altera EPF10K20 FPGA that oversee radiometer control, data acquisition, telemetry, and digital correlation operations. The firmware for the SmartCore and EPF10K20 are completely in-system programmable so that many M board functions can be changed without modifying the hardware.

Figure 4.6 shows the M board attached to its enclosure. One of the principal advantages of the M design is its flexible, open architecture that allows us to reconfigure the circuit for single or dual-channel radiometry. Initially I designed this system to perform a self-correlation on a single data stream for total power radiometry. In addition, the board was designed with a second set of expansion ports and chip select logic, allowing M to interface with a duplicate DSDR receiver for correlation radiometry.

Embedded microcontroller

The SmartCore module is an 8-bit, Z180-based controller that can be programmed in C or assembly language using a Windows software development tool. All circuitry is contained on a compact ($2'' \times 1.75''$) double-sided surface mount board, which includes 128 Kbytes of flash EPROM program space, 32 Kbytes of static RAM, a power supervisor circuit, real

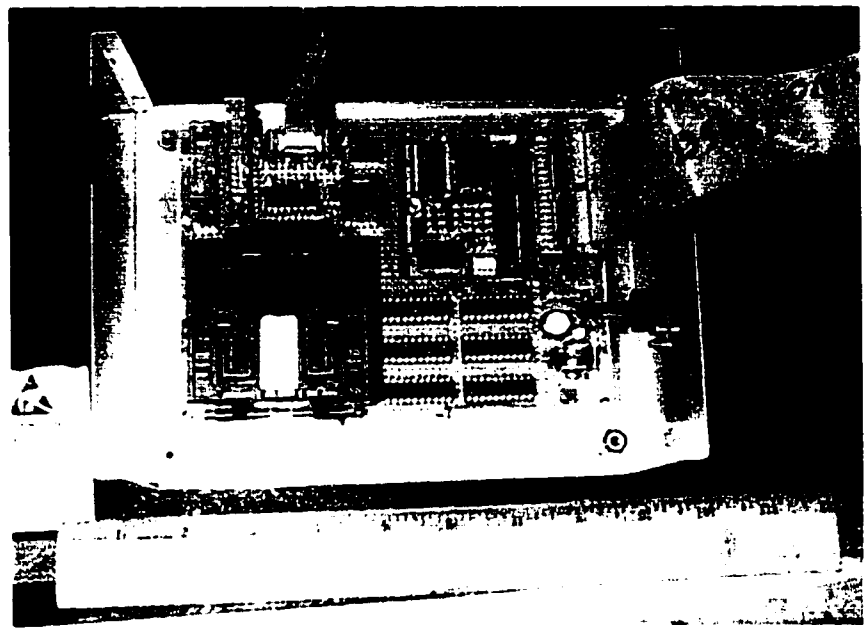


Figure 4.6: Photograph of the mounted M board. The SmartCore microcontroller, located in the upper right area, contains the program instructions that coordinate data acquisition and control with all other DSDR subsystems. The square prototyping socket located in the lower left section houses the EPF10K20 FPGA chip, which performs a digital self-correlation (total power detection) on data coming back from the A board.

time clock (RTC), and a demultiplexer for external chip selection.

The SmartCore is mounted on the top side of the M board through a piggyback socket. Support circuitry was added to the M board to enhance the features of the SmartCore. For instance, a 3 V lithium cell provides backup power for the RTC, which is used as a time stamp for DSDR experiments. If main power drops below a certain level, a power failure interrupt circuit sends a warning to the processor, allowing the SmartCore to do housekeeping tasks before shutdown. An on-board RS-232 transceiver chip provides a serial port to the PC for data acquisition and control. The SmartCore data and address buses control the flow of data between the T board (via the TempCon1 bus), the FPGA digital correlator, and the RS-232 transceiver. Bus signals that enter or exit the M board are buffered with line drivers to provide some noise isolation between M and other boards in DSDR.

Digital correlator

The digital correlation circuitry for DSDR was developed on the EPF10K20 field-programmable gate array. This circuit estimates the mean-squared power of the received brightness signal by performing a self-correlation (square and accumulate) operation on the digital data output from the A board.

Software correlator. Before deciding on an FPGA-based design, I developed and tested a preliminary, low-speed software correlator and considered other possible methods for processing the digitized data stream. The software correlator consists of a SmartCore assembly language routine which loads the A board's 6-bit output directly onto the microprocessor's data bus at a rate of 20 ksamples/s and calculates the self-correlation value, r_Q, using a multiplication look-up table (LUT) and accumulation register. While the sampling rate was too low to attain adequate NEΔT, this simple correlator helped confirm the linearity of DSDR over a wide dynamic range (see Section 4.6.2).

Hardware correlator. A number of technology tradeoffs had to be considered before finally settling on the fast (10 MHz) correlator design. Should I use a digital signal processor (DSP), application specific IC (ASIC), FPGA, or even a PC to do the correlation? PCs were ruled out because they would defeat the goal of autonomous, real-time processing. Generally, integrated circuits that are directly masked onto a silicon substrate, like DSPs and ASICs, have higher speed performance than reconfigurable devices like FPGAs; each programmable switch between logic elements in an FPGA has an associated resistance, capacitance, and electrical length which increase transition times and reduce maximum operating frequencies [61]. Still, present day FPGA devices can operate at clock rates up to 80 MHz—which is more than sufficient for the L-band DSDR. And the ability to design and *modify* almost any digital circuit (within the resources of the chip), whether it is a processing core or miscellaneous glue logic, made the implementation of FPGAs very attractive.

For the first-cut FPGA correlator design, I investigated whether Altera's MAX7000 family of devices would be suitable. These chips are considered to be the most convenient to program because they have non-volatile configuration memory that remains intact even when power is lost. However, the MAX7000 was limited to a low gate density (2,500), and the logic elements were not designed for register intensive applications like digital correlation. In the end, I chose instead the FLEX10K family's EPF10K20—an SRAM-based technology—because it offered greater resources ($\sim$ 20,000 gates) and its architecture has built-in embedded array blocks for large, specialized functions like multipliers and digital filters. The main drawback is that configuration of the device becomes more complicated due to the volatile memory: the FPGA's firmware must be reloaded upon every power cycle.

FPGA design file. The correlator output for a total power DSDR was defined in (2.6) for a zero-mean random process x. For the actual hardware, though, there will be a mean signal detected by the A/D converter that needs to be subtracted out. More generally,

$$r_Q = \left\langle (\hat{x} - \langle \hat{x} \rangle)^2 \right\rangle \approx \frac{1}{N} \sum_{n=1}^{N} \hat{x}_n^2 - \frac{1}{N^2} \left(\sum_{n=1}^{N} \hat{x}_n \right)^2 . \tag{4.11}$$

Therefore the digital correlator requires two accumulators: one that can calculate the sum of the quantized samples (*first order accumulator*), and one that calculates the sum of the square of these samples (*second order accumulator*).

I used Altera's MAX+PLUS II design automation software to create the hierarchical structure for the digital correlator and to configure the EPF10K20. Figure 4.7 shows the graphic design file named *digcorr* which I developed using these design tools. At the top level, there are several logic blocks that perform basic functions: (1) *square*—calculates the square of the two's complement digital word output by the A/D converter; (2) *accum* (first order) and *accum2* (second order) accumulators—these are separate 32-bit registers for integrating the sampled data and the square of the sampled data; (3) *count*—a loadable, 28-bit counter that determines the correlator's integration time and initiates the self-correlation;

and (4) *serial*—a 64-bit parallel-in/serial-out register that rolls the accumulator bits back to the SmartCore. I wrote these logic blocks using the Altera Hardware Description Language (AHDL) and took advantage of several useful parameterized modules built into the AHDL library.

High speed design issues. As mentioned before, a conservative sampling rate of 10 MSPS was chosen for the FPGA correlator to alleviate some of the engineering burdens in the design of a high speed breadboard. Wire-wrapped panels still behave well at 10 MHz because the circuit geometry on the M board is small compared to the electrical length of signal rise times. The EPF10K20, which comes in a 240-pin quad flat package, required a special adapter for mounting the chip to a wire-wrapped board. Due to the long bond wires running inside this adapter, significant inductance is added to the signal traces which can lead to excessive ringing for clock rates above 10 MHz. The latency time of the 32-bit accumulators also limits top speeds. Some addition operations in *digcorr* can take up to 80 ns, depending on how many carry bits are generated in the operation. (This latency problem was later solved by pipelining the data that flows between logic blocks.)

I faced some challenges trying to mount the FPGA's pin grid array adapter to the wire-wrapped M board. The 240-pin package occupied a large amount of board real estate and left little room for adding power buses, ground buses, and bypass capacitors near the pins. To solve this layout problem, I used conductive tape and solder to bridge a bus pattern between pads. Ceramic chip bypass capacitors, which greatly reduce high frequency noise on the power and ground lines, were mounted between adjacent pads on the back side of the board and soldered in place. In this way, I was able to create low impedance circuit board traces for the FPGA on a prototyping board. Ground bounce problems, which can cause unpredictable bugs in the finished hardware, are often averted by paying attention to these layout details and by using a ground plane.

Simulation and testing. The digital correlator design was verified with MAX+PLUS

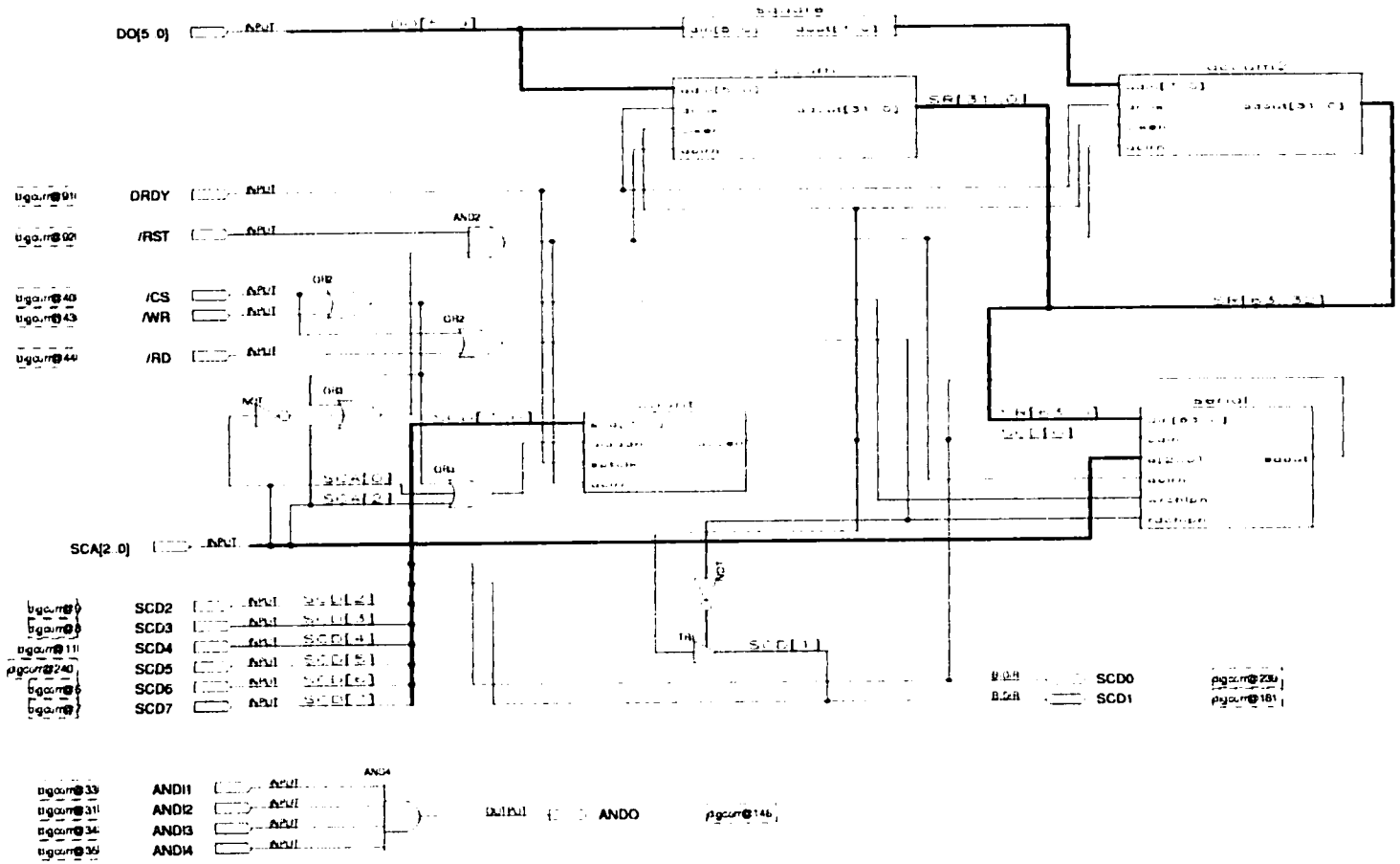


Figure 4.7: Top level graphic design file for the FPGA-based digital correlator (*digcorr*).

timing simulations. Figure 4.8 shows the results from a simple test, where a 4-word data stream $\{1, 2, 3, 4\}$ was loaded into the correlator at a rate of 10 MHz. Chip select and address lines were toggled to emulate the serial transfer protocol from the FPGA to the SmartCore. The sequence of output bits show that the accumulator result agrees with what was expected: the first order accumulator contains a value of 10, which is just the sum of the sequence. Simulations were also run for a range of possible input values to confirm that the multiplier would always generate a result in under 100 ns.

Once the simulations were finished, I downloaded the *digcorr* firmware from the Altera development tool to the EPF10K20 via a JTAG port. The dc input voltage to the A board was varied over the full conversion range (from -1 V to 0 V) to verify that the accumulators generated correct results over the range of possible digital values (from -32 to $+31$ using a 6-bit, two's complement word). This initial test confirmed that the digital correlator operated correctly on a static bit pattern.

Configuration EPROM. Because the EPF10K20 uses static RAM to store its configuration data, the M board eventually needed to have an on-board, read only memory that could configure the FPGA each time that power is applied to DSDR. At first I considered using a conventional EPROM, but programming fixtures were expensive (around \$2,000–\$3,000) and inconvenient to use because the memory chip must be removed from M each time it is programmed. In early 1999, Altera released a new flash EPROM chip called EPC2 which is in-system programmable and which communicates directly with the serial configuration port built into the EPF10K20. In the summer of 1999, I was able to integrate the EPC2 into the M board design so that the digital correlator could boot up on its own, untethered from the lab PC, allowing us to deploy DSDR into the field.

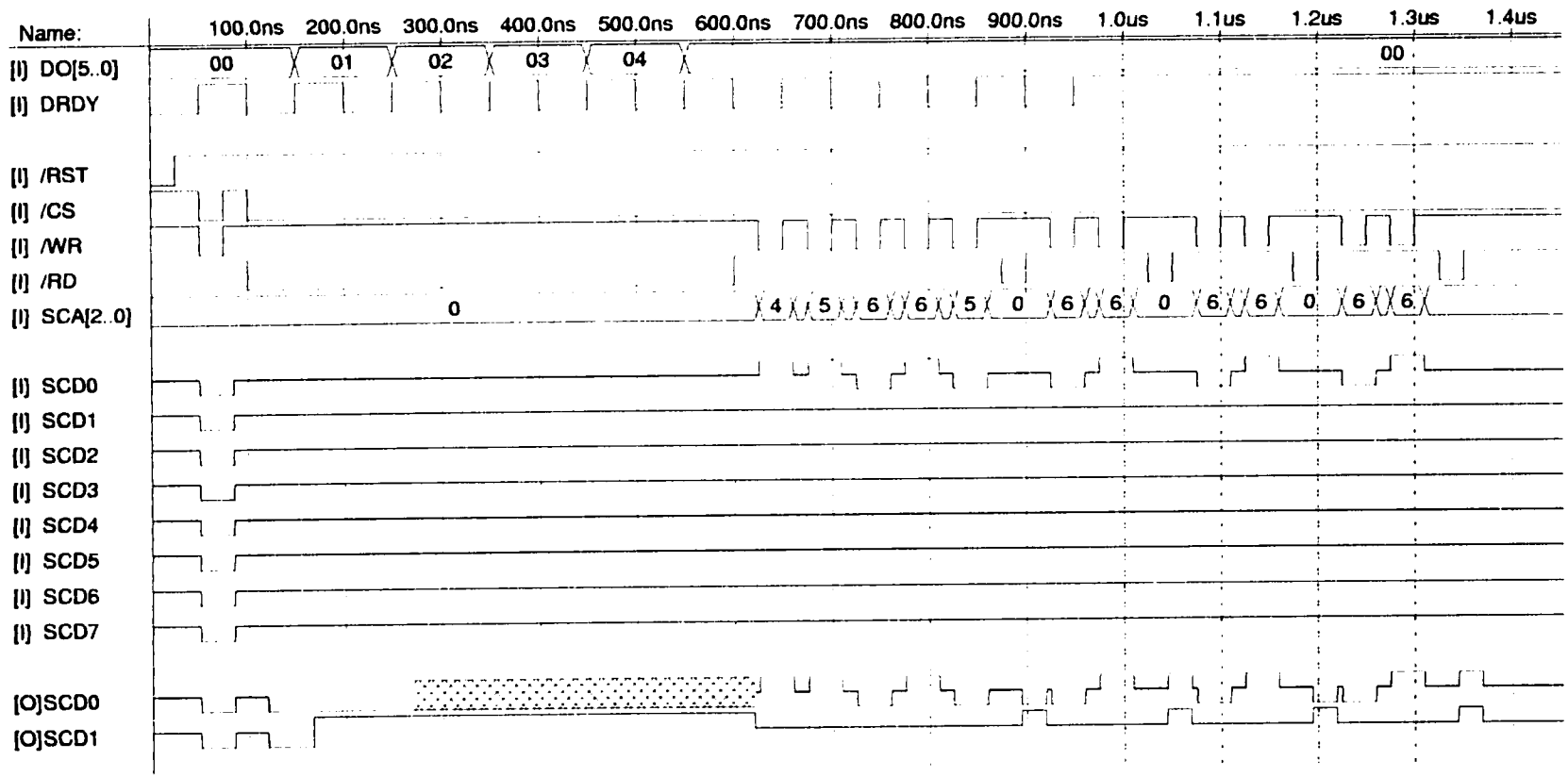


Figure 4.8: Digital correlator timing simulation. The input data sequence $\{1, 2, 3, 4\}$ is loaded from 150–550 ns. Next, the result from *accum* is rolled out one bit at a time as the SmartCore addresses the *serial* register using SCA[2..0], /RD, and /WR (address, read, and write lines). An output sequence $\{0, 1, 0, 1\}$ can be observed on the SmartCore data line, SCD0, each time /RD is asserted from 900–1400 ns. Taking the least significant bit first, the sequence of bits on SCD0 represents the expected binary value 1010 $(1 + 2 + 3 + 4)$.

4.3.7 Other electronic boards and components

G board

The G board provides regulated dc power to the ECL circuitry on the A board. Motorola's LM337, an adjustable, high current, negative voltage regulator, is used in several places to convert ±9 V input lines into −5.2 V analog power, −4.5 V digital power, and −2.0 V reference lines for the A/D converter. Also, a +5 V regulator supplies power to an A board heat sink fan for cooling the SPT7610. Ferrite beads were applied between the analog and digital grounds of the G board to reduce crosstalk noise that could affect A/D conversion. Given the large load current requirements for the ECL circuitry (ranging from 0.5–1.2 A for each voltage regulator), the G board circuitry was designed to keep the IC junction temperatures down for improved reliability: techniques included assembling the LM337s to large heat sinks and reducing dropout voltage by applying a resistive load at each regulator input.

X board

Digital data that is output from the A board must be converted from ECL levels (−0.9 V logic high, −1.7 V logic low) to CMOS compatible levels (5 V logic high, 0 V logic low) before the data can be processed by the M board. The X board serves as an ECL-CMOS translator that interfaces between A and M for this purpose.

Two Motorola MC10125 translator chips receive differential input data at 10 MHz from the A board, representing the 6-bit digitized sample and a "data ready" signal that indicates when the sample is valid. The MC10125s generate TTL compatible outputs which are then buffered through a CMOS line driver. I added an array of 33 ohm series terminations to the line driver outputs, before these lines leave the X board, to improve impedance matching and reduce reflections and ringing that can occur at the transmitting end of an electrically long cable [25]. The physical layout of the ribbon connection going from X to M is arranged

Figure 4.9: The G board voltage regulation circuitry (left) and the A/X board assembly (right) for analog-to-digital conversion at L-band frequencies.

so that there are alternating, adjacent signal-ground pairs. Having signal and ground in proximity to one another tends to reduce the cable's inductance and therefore yields a larger bandwidth for transmitting the digital data. In the X board design, I selected ECL devices from the so-called 10K family, which are purposely designed to have relatively slow rise and fall times ($\sim$ 3.5 ns). Parasitic high frequency effects in the wire-wrapped circuitry can be avoided with these slower switching speeds.

The completed circuit boards for G, A, and X are shown in Figure 4.9. In the photo, the X board has already been enclosed in a small EMI shield that lies immediately to the left of the A evaluation board.

C board

The A evaluation board from SPT includes circuitry that decimates the data output by a factor of 16. Therefore, to attain the desired 10 MSPS data rate for DSDR, I needed to design a clock (C) board that could generate a higher frequency signal, running at 160 MHz, with ECL-compatible voltage levels. The C board comprises a 160 MHz quartz crystal

oscillator, a TTL-to-ECL translator chip, and on-board voltage regulators for the ECL and CMOS power supply lines. A 50 Ω matching network and SMA connector serve as an output port for the C board clock. The ground plane of the C board is tied directly to the analog ground of the A evaluation board to prevent digital crosstalk, which can cause the A/D converter to mistrigger. The TTL-ECL translator also provides several unoccupied output ports that can be used for future expansion to synchronize the two-channel correlation radiometer.

Enclosures

Aluminum cases enclose every board in DSDR to minimize electromagnetic interference. Also, these enclosures are connected to chassis and signal grounds to eliminate electrostatic (capacitive) coupling between the subsystems. Eventually each box will serve as metal fixture that can be secured to a weatherproof, field-grade DSDR enclosure.

Power supplies

All of the electronics in DSDR are powered by linear Acopian supplies that run off of 120 Vac. Linear power supplies are preferred because they do not generate high frequency noise that can interfere with the radiometer's performance, as do switching power supplies or regulators [66]. A ±9 Vdc regulated supply powers the A evaluation board and all of DSDR's digital logic boards. An 18 Vdc regulated supply is used for the L-band front end. A 24 Vdc/10 A supply, which powers the TEC, is the only unregulated supply in DSDR. Regulation is not necessary in this case because the feedback loop in the temperature controller compensates for droop in the TEC power output. Furthermore, weight and power efficiency can be saved by choosing an unregulated supply.

4.4 Software Development

The software development philosophy for DSDR closely parallels the approach already outlined in Section 4.2 for the radiometer hardware. Most data processing and housekeeping tasks are performed locally, at the DSDR radiometer. At the PC end, a graphical user interface handles the presentation of the data and controls other science instruments (besides the microwave sensors) that make up the mobile field system for our REBEX experiments. Two software products called *RaDOS* and *FluxMon2* were created to realize this approach for data acquisition and control.

4.4.1 RaDOS

RaDOS (Radiometer Operating System) is a command-line interpreter which I wrote in the Dynamic C language for the SmartCore. Its main purpose is to control and monitor the DSDR subsystems. It is also meant to interface with a more sophisticated, user friendly GUI for the PC. With RaDOS, the user can, for example, control the radiometer's physical temperature or acquire radiobrightness counts by typing a series of text-based commands at the PC's terminal.

During field campaigns, other electronic devices (an IR sensor, antenna rotator) that share a common PC serial port with DSDR are also deployed. Therefore the RaDOS communication protocol needed to accommodate multiple devices on the same line while avoiding bus conflicts. To accomplish this, the PC is programmed to act as the master device that communicates with other instruments via an optically isolated, half-duplex RS-485 link. DSDR is slaved to the laptop PC through RaDOS software: DSDR is programmed only to "speak when spoken to" by the PC; it never initiates a data transfer through the serial port by itself.

Table 4.5 summarizes the functions developed for the RaDOS command-line interpreter. These commands allow the user to enable and disable temperature control, define the set

command	description
FT! *temp*	Sets the command temperature to *temp* and enables temperature control.
FDC! *duty*	Sets the TEC duty cycle to the constant value *duty*, thereby disabling temperature control.
TD?	Queries the temperature data array which contains date and time stamps, thermistor readings, set temperature, and current duty cycle.
CORR! *count*	Loads the digital correlator integration counter with value *count* and initiates a brightness measurement.
CORR?	Queries the correlator status. Returns 0 if a correlation is in progress. Otherwise returns date/time stamps and raw data from the correlator output.
RFSW! *mode*	Sets the RF front end switch to *mode* (either antenna or reference load).
RFSW?	Queries the current status of *mode*.

Table 4.5: RaDOS commands.

temperature, define the radiometer's integration time, initiate a correlation, read the number of counts back from the correlator, and set the front end SPDT switch to antenna or reference load positions. A unique identification header precedes each command to indicate that the PC is addressing DSDR.

The RaDOS software also handles the transfer of data from the FPGA accumulators to the SmartCore. After initiating a correlation, the SmartCore periodically polls a status bit from the FPGA to check if the correlation is finished. Upon completion, the SmartCore serially rolls the result out from the 64-bit register in *digcorr* and calculates the correlator output value. The result is telemetered back to the PC once DSDR has received a query on the RS-485 serial line for correlation data. This method for processing and delivering data allows the SmartCore and PC to perform other tasks unhindered while correlations run in the background.

Clearly the separate functions in RaDOS—the command-line interpreter, the digital correlator, and temperature control algorithms—must run simultaneously. I implemented a real time kernel (RTK) in RaDOS which assigns an interrupt address and timer to each software function. After a certain number of ticks from the microprocessor's system clock,

an interrupt is asserted to call the appropriate function. For instance, every 60 s a routine is called to measure thermistor temperatures, calculate the new PID control values, and update the TEC duty cycle; every 1 s the serial receive buffer is checked and, if occupied, the string is parsed by the command-line interpreter.

The source code for RaDOS version 0.0, for total power radiometer operation, is listed in Appendix E. Future revisions of RaDOS will include algorithms to control a two-element correlation DSDR.

4.4.2 Flux Monitor (FluxMon2)

FluxMon2 is a virtual instrument designed for data acquisition and control of the field-grade radiometer hardware. The user interface and C code was written in the LabWindows/CVI language from National Instruments. With FluxMon2, the user can select one of several graphical panels for DSDR temperature control, calibration, brightness measurements, or antenna rotation. Data sets telemetered from DSDR are displayed numerically and graphically on a laptop PC and are written to a hard drive. Most of the code is organized into modular functions (serial I/O, string formatting, error handling, etc.) that are shared by the various panels, allowing the software to be adapted for future needs.

Temperature control. The temperature control panel allows the user to: (1) set the command temperature to enable the feedback controller, (2) disable the controller by setting a fixed duty cycle for the TEC, and (3) monitor the temperature of the front end plate, reference load, and antenna. Temperature and duty values, updated once per minute by a software interrupt, are graphed with respect to time to indicate whether a steady-state response has been reached.

Calibration. The calibration panel includes GUI buttons and switches for taking radiobrightness measurements while a hot or cold load fills the antenna beam. The transfer function between correlator counts and brightness temperature is approximated with the

linear relation

$$T_B = m_0 r_Q + b_0, \tag{4.12}$$

where m_0 and b_0 are gain and offset coefficients. After measuring the r_Q outputs for both hot and cold targets, two equations and two unknowns are generated, leading to the solution

$$m_0 = \frac{T_{B(hot)} - T_{B(cold)}}{r_{Q(hot)} - r_{Q(cold)}}, \quad b_0 = \frac{T_{B(cold)} r_{Q(hot)} - T_{B(hot)} r_{Q(cold)}}{r_{Q(hot)} - r_{Q(cold)}}. \tag{4.13}$$

These coefficient are stored in memory and recalled during radiobrightness experiments to calculate the T_B data.

Radiobrightness. The user can acquire and record L-band brightness data with the brightness panel. Control widgets include a toggle switch for selecting either random access or periodic measurements, buttons for selecting the antenna and/or matched reference load during brightness looks, and a numerical display that sets the integration time. After FluxMon2 transmits a correlation command to DSDR, a software interrupt polls the correlator's status flag once per second and, if the integration is finished, FluxMon2 will parse the received data. (Therefore, other system events in FluxMon2 can be processed concurrently while the correlation is in progress.) Raw data from the first and second order accumulators, the brightness temperatures computed from (4.12)-(4.13), and time stamp data are displayed on screen and stored to the PC's hard drive.

Elevation rotator. The rotator panel lets the user control the elevation angle of the septum horn antennas once DSDR is deployed onto our truck mounted radiometer system. This panel shows the present angle, desired (set) angle, and speed settings for the elevation rotator motor. Current angle information is read via the PC's serial port from an inclinometer mounted onto the DSDR/rotator assembly. Likewise, the PC can send command data to a control box that moves the rotator to the specified angle. Thus, the rotator panel acts as a feedback servo that can lock onto the desired elevation angle set by the user.

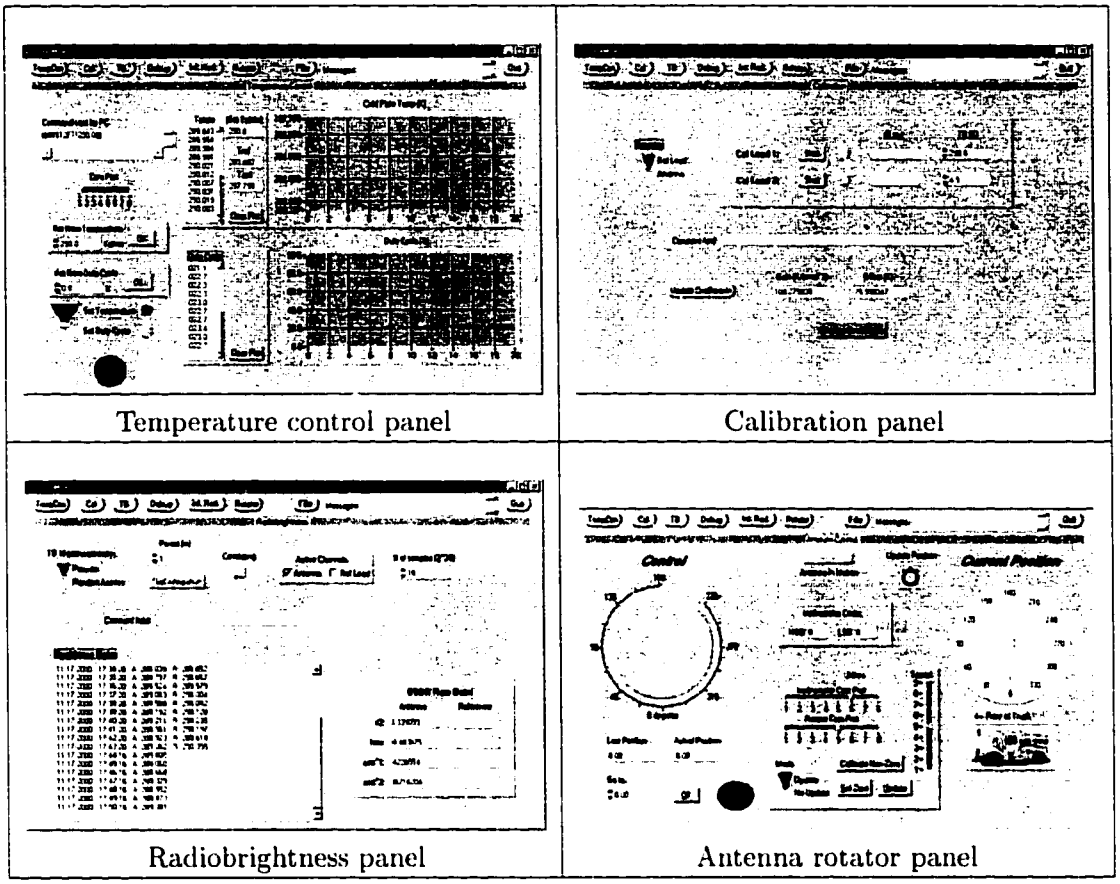


Figure 4.10: FluxMon2 graphical interfaces for DSDR data acquisition and control.

Screen shots from the FluxMon2 GUI panels are shown in Figure 4.10. Presently FluxMon2 contains 1,750 lines of source code.

4.5 Field-Grade Implementation: The Truck Mounted Radiometer System

4.5.1 Truck with hydraulic boom

In previous REBEX field campaigns, our microwave radiometer system had always been deployed onto a 10 m stationary tower for long term (3–12 month) studies over relatively homogeneous terrain. Assembly of this tower mounted system was laborious, often requiring 4 person-days of effort at the start of each experiment. Recently, our group's research interests have shifted toward shorter-term studies in more complex agricultural areas that have high spatial variability over a few kilometers distance. In order to carry out the next

phase of experiments, we needed a mobile radiometer platform for DSDR so that a variety of terrain types could be surveyed efficiently. We purchased a special truck chassis, integrated with a hydraulic aerial lift, as part of our new Truck Mounted Radiometer System (TMRS).

I lead our group's effort in specifying and purchasing a *Reach All* truck from NorStar Inc., which has a 40 foot telescoping, hydraulically powered fiberglass boom and enclosed laboratory workspace (Figure 4.11). We needed a vehicle that could improve the mobility of the L-band sensors while also providing a safe and comfortable environment for field work. MGP considered competing bids from several manufacturers before the purchase. Some vendors offered articulating booms which could reach all the way to the ground, making it convenient to dock with the DSDR hardware. However, these models either exceeded our $100,000 budget or the 26,000 lbs. gross vehicle weight limit for a standard driver's license, or the large size of the stowed boom precluded the integration of an enclosed cab. The NorStar truck and boom unit was fortunately just $1,000 shy of our budget limit and offered the following important features:

- enclosed cab for laboratory work space
- 17,700 lbs. vehicle weight rating (below the commercial driver's license restriction)
- up to 40 ft. ground-to-platform boom height
- 750 lbs. load capacity for boom
- internal 7.5 kW diesel generator with 120 Vac power output
- torsion bar stabilizer (no outriggers required)
- cat-track conduit for power and communication bus cables

The main disadvantage is that the NorStar boom is non-articulating and therefore can not reach down to the ground: MGP would have to design a mechanism to lift the DSDR payload 12 feet above ground, where the boom resides in its parked position.

4.5.2 DSDR chassis preparation

Before DSDR was deployed outdoors, the radiometer electronics were fitted with weatherproof enclosures and cables to withstand harsh environments. Two 9″-wide aluminum

Figure 4.11: The NorStar truck with hydraulic aerial lift, which would become the platform for our Truck Mounted Radiometer System (TMRS).

racks, shown in Figure 4.12, were devised to house the various DSDR boxes and provide mechanical rigidity when the chassis is moved or rotated. The 9″ racks were assembled in water-tight aluminum "suitcases" made by Zero Corporation to protect the electronics from rain and snow. We also used military-grade, weatherproof Deutsch connectors with gasket interfaces to run communications and power lines between the Zero cases.

The two assembled Zero cases are bolted on opposite sides of the septum horn mounting flange, as shown in Figure 4.13. In this final configuration, the front end port is positioned within 6 inches of the antenna terminal, allowing a relatively short, low-loss coaxial connection to the receiver.

4.5.3 Elevation rotator

We added an elevation angle positioner into the TMRS design to set a range of incidence angles for DSDR calibration and measurements. The MT-1000 rotator, from M-Squared

Figure 4.12: Homemade 9″ aluminum racks house the various subsystems in DSDR. The rack shown on the left contains the receiver and temperature control electronics; the rack on the right includes the digital correlation circuitry, embedded controller, clock, and power supplies.

Figure 4.13: Weatherproof Zero cases attached to the mounting flange of the septum horn antenna.

Industries, is a electric wormgear positioner which provides 360° rotation and up to 4500 in-lbs of torque. The rotator's speed and direction are set with a control module that interfaces between the serial port of the laptop PC and the rotator motor. A digital inclinometer, mounted to the rotator, sends elevation angle data back to the PC at a resolution of ±0.15°. Up to two DSDR units can be mounted to the axle that extends from either side of the rotator's drive gear.

A custom designed plate, welded to the positioner, interfaces with an aluminum mounting sleeve on the end of the NorStar boom. For the initial outdoor tests with the total power DSDR prototype mounted on the rotator's starboard side, we added a second septum horn antenna with dummy load on the port side as a counterbalance.

4.5.4 Loading boom

MGP fabricated an aluminum A-frame loading boom and attached this structure to a pair of steel pivots on the front bumper of the NorStar truck. Using a winch and cable, the operator can hoist the boom with rotator/DSDR assembly from ground level to a 12 foot height, where the rotator docks with the truck's hydraulic boom (Figures 4.14–4.15).

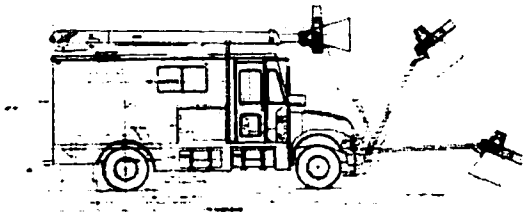


Figure 4.14: Mechanical design concept for the TMRS loading boom.

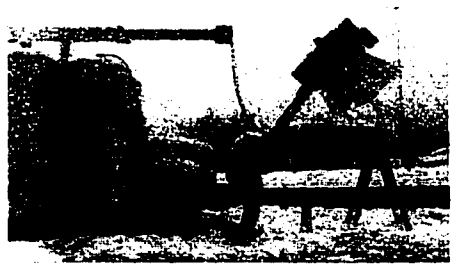


Figure 4.15: Loading boom docking process. The user lifts the DSDR payload, attached to a steel cable, by turning a winch located near the front bumper.

A prototype setup using a manual crank was eventually retrofitted with an electric motor, running off of 12V battery power, which can lift payloads up to 750 lbs.

4.5.5 Mobile lab preparation

To keep the truck's bidding price low, we had to forgo additional amenities in the rear cab until after the purchase. Since then, our group has converted the truck's interior into a working lab for field experiments.

We installed electrical breakers and wiring that distribute power from the on-board 7.5 kW diesel generator to several 120 Vac outlets arranged along the rear walls of the truck. Acoustic shielding was added to the generator compartment, significantly dampening noise and vibration inside. We constructed a waterproof ceiling port to run the RS-485 communication line and 120 Vac power from the mobile lab, through the boom's cat-track, to the rotator and radiometer. Fixtures and cabling for a video camera and infrared sensor were also assembled onto the TMRS boom.

TMRS experiments will often be conducted in extreme environments (for example, arctic regions during the winter or the southern U.S. plains during the summer season). We installed thermal insulation, a ceiling air conditioner, and a diesel Espar heater to make the environment inside the truck habitable for people and computer equipment.

4.6 DSDR Measurements and Characterization

4.6.1 Temperature stability

The closed-loop temperature response for DSDR was first tested with the thermoelectric cooler and front end assembled on a bench top in the lab. The TEC operated efficiently here because air from the hot junction could be purged directly into the ambient environment. The first cut calculations for PID coefficients were made using the open-loop step response results described in Section 4.3.5; afterwards, I refined the coefficients through trial-and-error experimentation to reach the most stable steady-state response. Also, the PID software algorithm was modified to prevent the integrator from saturating (and causing oscillations) when there is a large difference between actual and desired temperatures. A plot of the controller's response is shown in Figure 4.16 for a set temperature of 10°C. The rms deviation in physical temperature, calculated within a ± 10 minute window, approaches an average value of 13.6 mK once the cold plate has stabilized.

Next, the temperature controller was tested with DSDR electronics enclosed in Zero cases and mounted to the septum horn antenna. I soon discovered a serious thermal design flaw, stemming from the inadequately low heat transfer rate from the TEC roughing chamber to the outside ambient air. The thermal conductivity of the junction between the TEC box and antenna mounting flange was too low to dissipate heat that was internally generated. Consequentially, as the system aged, both hot and cold junction temperatures of the TEC rose monotonically, resulting in thermal runaway.

At this time, we were preparing for a TMRS shakedown experiment during the winter of 2000. To expedite the deployment of DSDR, I decided that the thermal runaway problem could best be averted by using the cold weather to our advantage—that is, by controlling the front end with heating as opposed to cooling. The resistive heating element embedded in the TEC has a significantly greater efficiency than does the TEC itself. Therefore, a temperature bias can be added to the front end without overheating the rest of the DSDR

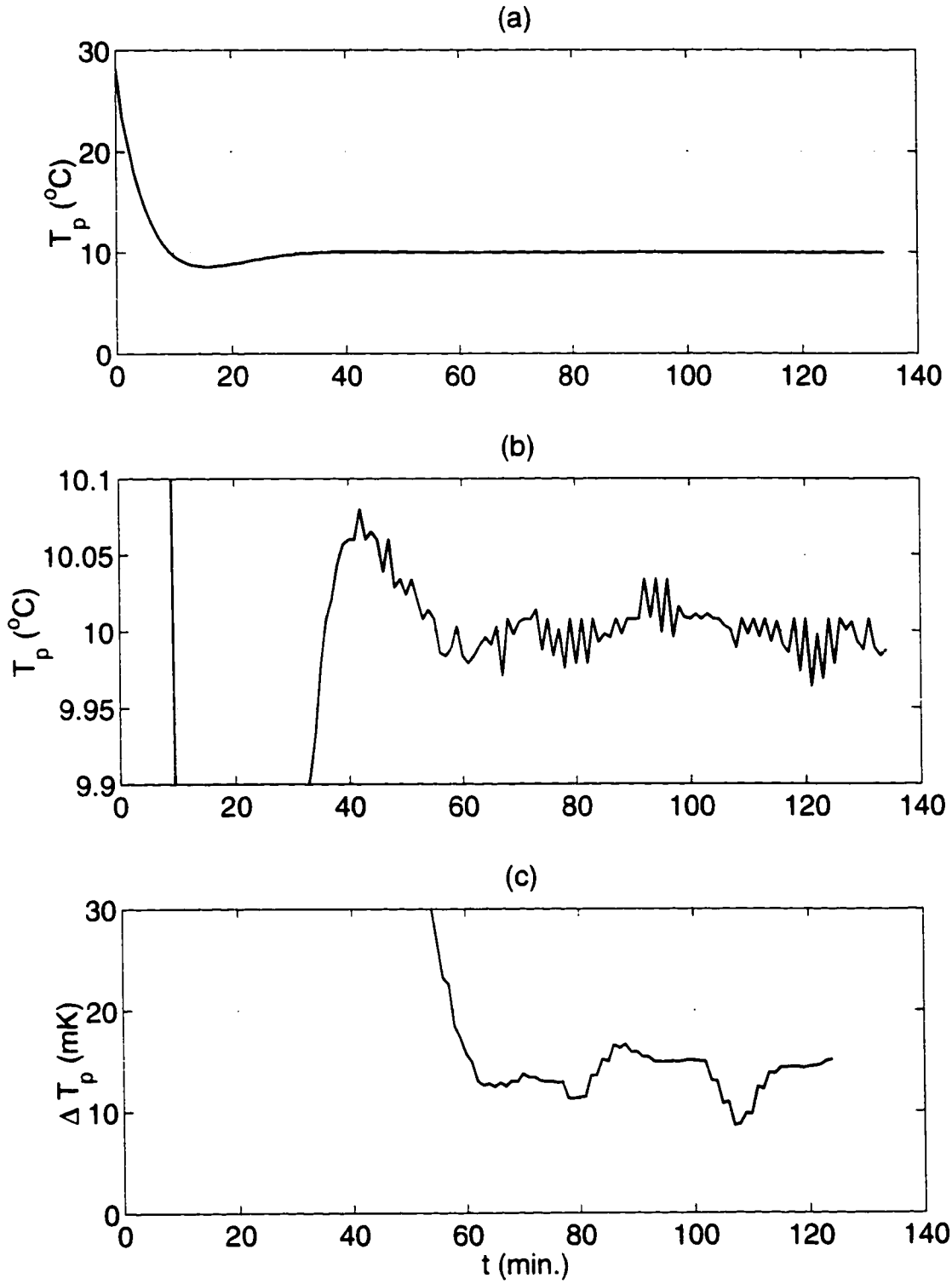


Figure 4.16: Closed-loop thermal response for the benchtop TEC assembly. (a) Plate physical temperature vs. time; (b) a close-up of the preceding graph, centered around the 10°C set temperature; (c) the rms temperature error computed over a 20 minute window.

chassis. The TEC module was rewired for heater control, and the PID coefficients were retuned. The final temperature response is shown in Fig. 4.17 for the field grade DSDR. After the system has aged for about 2 hours, the physical temperature variation reaches an average value of 12.1 mK rms.

Receiver temperature fluctuations will cause a change in the system gain (ΔG) which, in turn, degrades the overall NEΔT. For a total power radiometer, the output error will be proportional to this gain change:

$$\frac{\Delta T_G}{T_{SYS}} = \left|\frac{\Delta G}{G}\right|. \tag{4.14}$$

where ΔT_G is the noise-equivalent sensitivity component due to temperature fluctuations. I used the vendor's specifications to estimate a net temperature coefficient of $TC_{gain} = -0.06$ dB/°C for all LNAs in the front end. Therefore, for every 1°C change in physical temperature,

$$\frac{G + \Delta G}{G} = -0.06 \text{ dB}. \tag{4.15}$$

and the corresponding change in detected brightness temperature is

$$\left(1 - \frac{G + \Delta G}{G}\right) T_{SYS} = 5.49 \text{ K/°C}. \tag{4.16}$$

taking $T_{SYS} = 400$K. Thus ΔT_G can be found by multiplying the front end's physical temperature variation, ΔT_p, by the factor in (4.16).

Temperature regulation results for the heater controlled, field-grade DSDR are shown in Table 4.6 under several test conditions. In the first two tests, the front end SPDT switch is set to only one channel (reference or antenna) during the entire experiment; in the third test, DSDR switches between the two channels every minute. Note that the stability of the controller is essentially the same whether DSDR is in an environmentally controlled lab or deployed outdoors on the truck, where there are large variations in air temperature. However, the temperature stability is most significantly degraded when the SPDT switch is

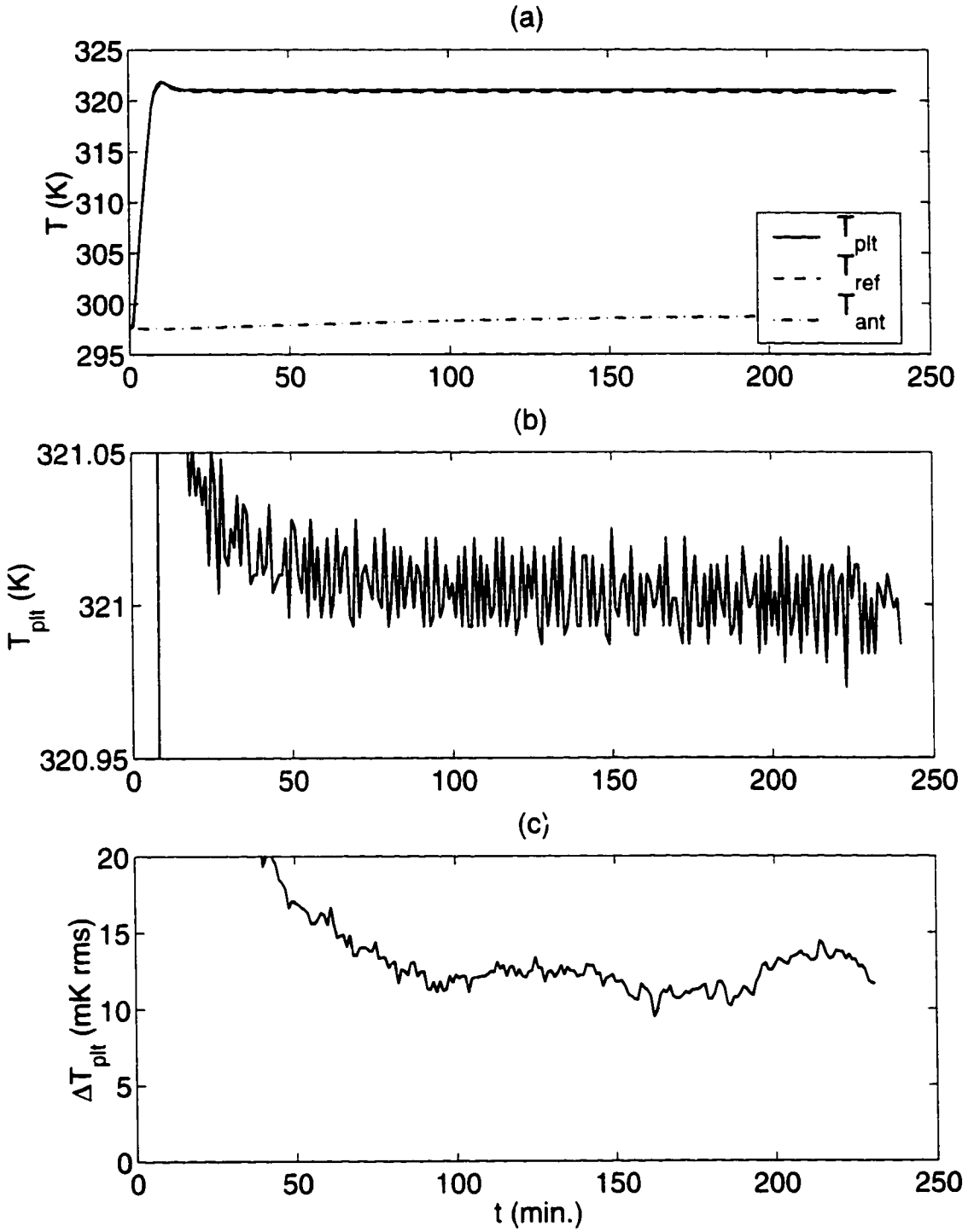


Figure 4.17: Temperature response of the field-grade DSDR radiometer using the heater control. (a) Plate, reference, and antenna responses for a set temperature of 321.0 K; (b) close-up of the plate temperature response; (c) rms fluctuation in the plate temperature.

test	condition	ΔT_p	ΔT_G
1	indoor response (no SPDT switching)	12.1 mK	66.4 mK
2	outdoor response (no SPDT switching)	12.7 mK	69.7 mK
3	outdoor response (with SPDT switching)	59.0 mK	324 mK

Table 4.6: Front end thermal stability results for DSDR.

used to take periodic looks at both the antenna and reference loads. As mentioned before, this switch is a failsafe device which dissipates more than 2 W of power whenever it is set to the reference (normally open) channel. Therefore, switching introduces an undesired thermal pulse in the front end plate which is eventually picked up by the plate thermistor and added to the feedback signal. A permanent solution to this problem would require a redesign of the front end, using a switch that does not dissipate power when it is static. In the meantime, we decided that for field experimentation, the benefits of periodically viewing the reference load for long term calibration outweighed the short term degradation in ΔT_G imposed by the thermally noisy switch.

4.6.2 Dynamic range

DSDR's dynamic range was verified in the lab using the software correlator described in Section 4.3.6. For this test, a matched load was connected to the front end input to simulate the brightness temperature of a beam-filling blackbody target. An adjustable attenuator was added between the front end and the A/D converter sections to confirm that r_Q varies linearly with the input signal power. Also, to compare the correlated result to the true signal power s^2, the A/D input signal is switched by means of an electromechanical RF relay to an HP8592L spectrum analyzer for power measurements. The spectrum analyzer's resolution bandwidth and averaging factor are increased to 3 MHz and 3000 points, respectively, to improve the measurement precision.

Figure 4.18 shows the self-correlation response for small signals near the dc bias noise

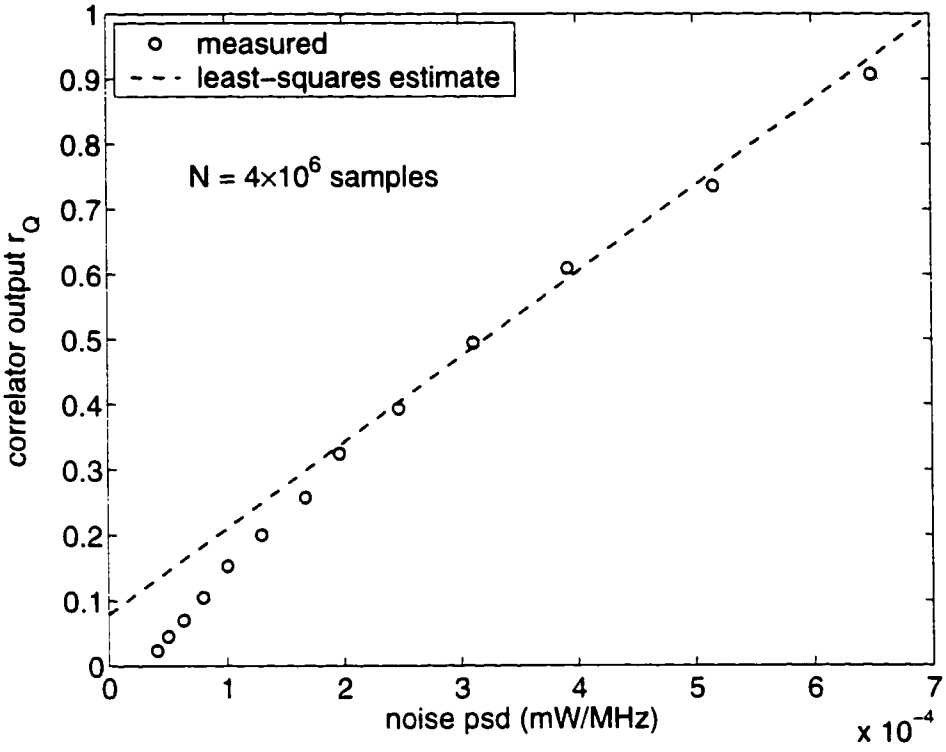


Figure 4.18: Total power DSDR small-signal response.

floor. Each measured data point represents the correlator output integrated over 4 million samples. [3] For signal levels greater than 2 bits ($r_Q > 0.5$), the approximation in (2.21) should become valid:

$$\langle r_Q \rangle = s^2 + \frac{1}{12}. \tag{4.17}$$

I confirmed the above relation by plotting, along with the experimental data, a linear least-squares estimate for data points exceeding a correlation of 0.5. As expected, the y-intercept value of 0.079 closely matches the 1/12 quantization noise floor factor predicted in (4.17).

In Figure 4.19, data points were also measured for $r_Q > 1$ to gauge the upper limits of the dynamic range. Even for correlation values as high as 5, the converter showed no signs of compression or other non-linear behavior. Therefore, with at least 10 dB of dynamic range

[3] I defined r_Q as a mean-squared voltage in Chapter 2 to clarify the relation between bias voltage and detect output. However, in the real world, the correlator output will be dimensionless—just as digitized samples have no inherent dimension. A normalization factor of v_0^2 can be applied to r_Q expressions (e.g., equations 2.6, 4.11) to reflect the actual output values generated by DSDR.

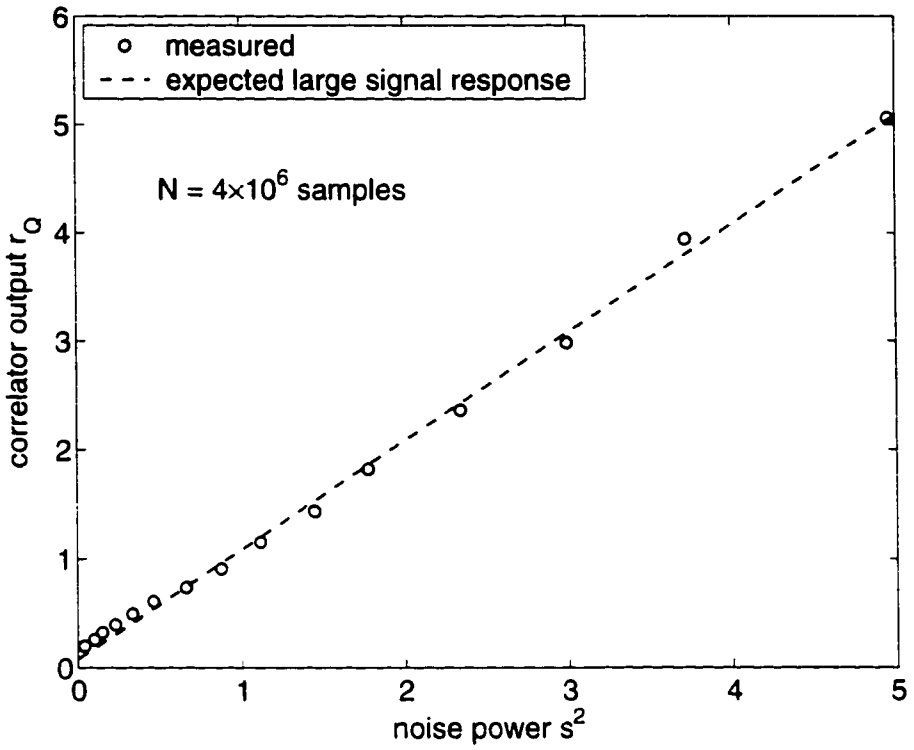


Figure 4.19: DSDR large-signal response ($0.5 \leq r_Q \leq 5.0$).

available (from $r_Q = 0.5$ to 5.0), a total power DSDR design is suitable for Earth remote sensing applications at L-band frequencies, where the system noise temperature typically falls within the 50–350 K range.

4.6.3 Sensitivity to quantization bias variations

The output of the software correlator was measured for two extreme biasing cases, $b = 0$ and $b = 1/2$, by adjusting an externally supplied dc voltage tied to a bias-T circuit on the A board. The difference between r_Q outputs for the two cases can then be calculated and compared to the correlator uncertainty function predicted by (2.19).

Uncertainty function data were taken over a range of signal levels and plotted in Figure 4.20, along with the theoretical response. Measurements taken below 3 quantization levels (1.6 bits) agree closely with the theory, but for larger signals the data begin to run into the noise floor limits of the experiment. The theoretical noise floor, indicated by the

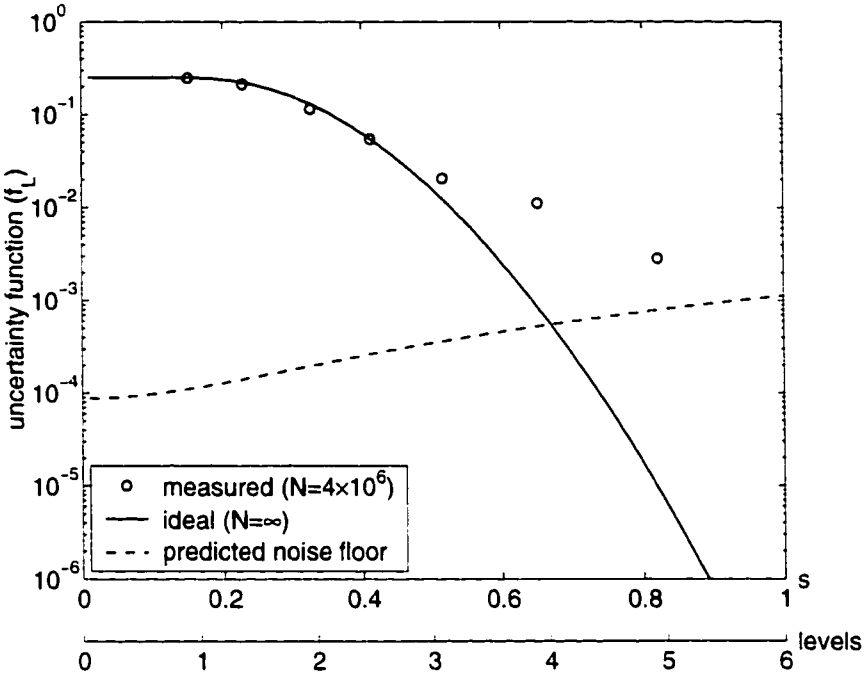


Figure 4.20: Correlator uncertainty due to dc bias fluctuations.

dashed curve, was estimated from variations that naturally arise from the finite integration length and receiver gain fluctuations (see equations 2.64 and 4.14). Still, there is some discrepancy between the actual and predicted noise floor when the sampling resolution exceeds 3 levels. As I will discuss in the following sections, the first phase of the DSDR hardware design was laden with several critical problems which could cause spurious fluctuations in r_Q and degrade the signal-to-noise ratio of the output.

4.6.4 Noise-equivalent sensitivity

I investigated DSDR's sensitivity performance once the FPGA hardware correlator had been implemented on the M board. For this experiment, a set of independent r_Q samples were measured while the receiver viewed a thermally regulated, matched reference load (i.e., a constant brightness source). The SNR of the detect output and NEΔT can then be found by calculating the mean and standard deviation of the r_Q data set. As in the previous tests for dynamic range and dc bias, the signal source input to the A/D board can be varied in

strength to test the performance for a range of bit resolutions.

DSDR's predicted NEΔT , including noise components from quantization, finite integration time, dc bias drift, and gain fluctuations, can be computed using the theory presented so far. Recall that the FPGA digital correlator samples at 10 MHz, or one-fourth of the 40 MHz Nyquist rate for the analog input signal $x(t)$. Because the sampling interval exceeds the $1/B$ correlation time (50 ns) of the narrow band noise, successive samples will have almost no statistical dependence on one another. In fact, for a sampling factor of $\gamma \leq 1/4$, the autocorrelation series $\sum R_F^2$ in (2.66) shrinks to less than 10^{-2} and can be neglected from the analysis. Thus, the sensitivity component in (2.64) due to finite sampling and quantization is approximated by

$$\Delta T_F = T_{SYS}\sqrt{\frac{2}{N}\left(1+\frac{1}{6s^2}\right)}. \tag{4.18}$$

In the worst case limit, the sensitivity component due to dc bias fluctuations, ΔT_L, is given directly by (2.27). The noise due to gain fluctuations, ΔT_G = 66.4 mK, is known from Table 4.6.

Detect output measurements were recorded over a range of bit resolutions with the integration interval set to N = 10.5 Msamples. Figure 4.21 shows the r_Q values for several data sets, with each set monitored once per minute. It is important to reiterate that when these sensitivity experiments were conducted in the lab, the receiver design was at a stage where sporadic and unexpected fluctuations in r_Q could be observed over time. To study the fundamental sensitivity limits of the hardware, I proceeded by taking a longer data record (about 6 hours for each bit resolution), and by inspection, I selected 100 continuous minutes of apparently non-spurious data for the analysis. The empirical NEΔT is found from these data using the general definition of detect output SNR (analogous to equation 2.7) and total system noise temperature (2.26), yielding

$$\Delta T_{(meas)} = \frac{T'_{SYS}}{SNR} = T_{SYS}\left(1+\frac{1}{12s^2}\right)\frac{\sigma_Q}{\langle r_Q\rangle}, \tag{4.19}$$

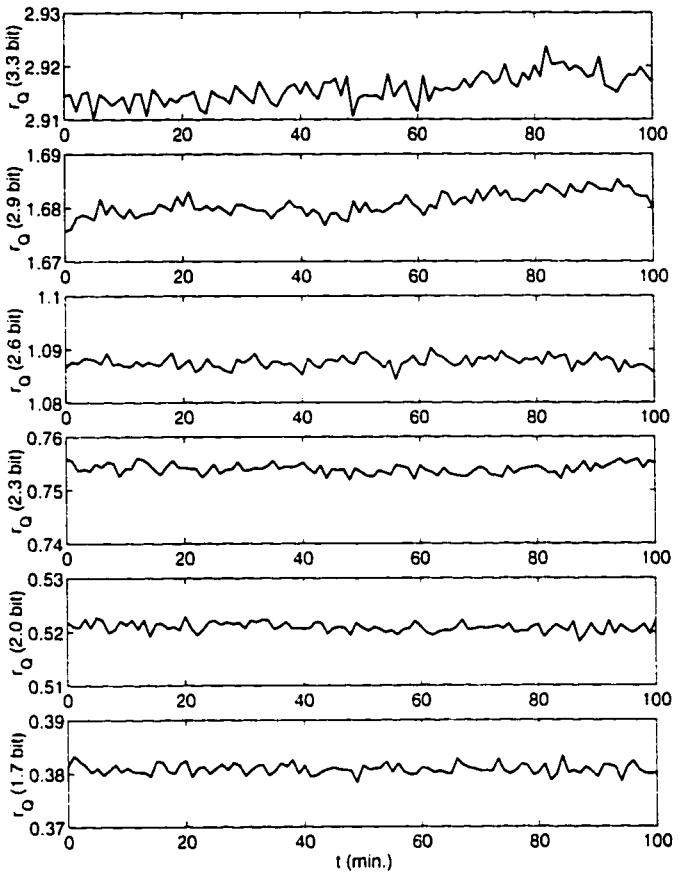


Figure 4.21: Measured variations in r_Q for 1.7-3.3 bit conversion.

where σ_Q is the standard deviation in the r_Q data.

The theoretical and experimental sensitivity results are plotted in Figure 4.22 as a function of the A/D converter's bit resolution. As the resolution is increased beyond 3 bits, NEΔT measurements approach the ~ 0.2 K sensitivity estimate in (4.18). However, as the resolution decreases below this point, the empirical sensitivity is degraded significantly, and a widening gap can be observed between measurement and theory.

The discrepancy in NEΔT may be caused by non-Gaussian additive noise at the analog input of the A/D converter which imposes a lower bound on the detect output fluctuations. (For instance, this noise could arise from crosstalk between digital and analog sections of the receiver.) Notice for example that the empirical NEΔT tends to quadruple in power when the resolution is decreased by 1 bit: interpolating between data points, the sensitivity

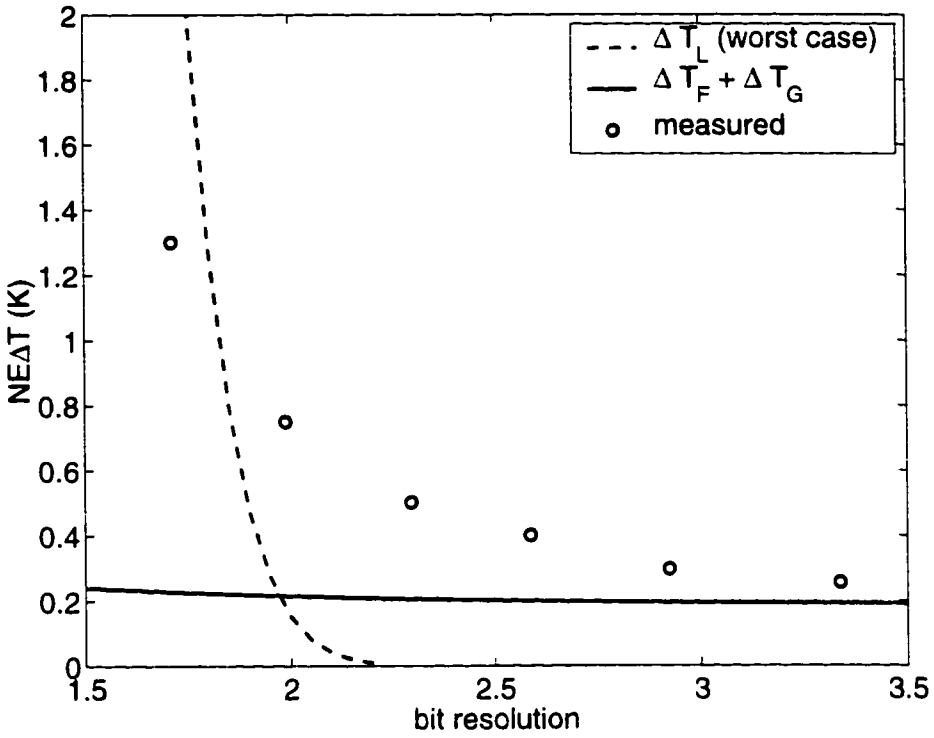


Figure 4.22: Theoretical and experimental NEΔT results for the field-grade DSDR.

increases from $\sim$ 0.43 K at 2.5 bit resolution to $\sim$ 1.7 K at 1.5 bit resolution. A one bit reduction also corresponds to a four-fold (6 dB) reduction in signal power. Because NEΔT and the detect output SNR are inversely related, it follows that the noise energy in r_Q remained essentially constant over the 1.5–2.5 bit range. Indeed, a qualitative look at Figure 4.21 suggests that the variations in r_Q tend to bottom out as the resolution falls below 2.6 bits.

In Section 4.7, I will discuss several design modifications that were made to reduce additive noise sources in DSDR. Also, these design changes will be carried over into the fabrication of the second DSDR receiver to determine whether NEΔT performance can be improved at coarse resolutions.

4.6.5 TMRS shakedown

In the winter of 2000, we deployed and tested DSDR for the first time onto our truck system, parked outside of the Space Research Building on North Campus. Excessive noise in the detect output signal prevented us from acquiring accurate radiobrightness data during this shakedown. But the outdoor tests proved essential, as we gained valuable insight through calibration and sky brightness experiments that pointed toward possible causes of instability in the radiometer design.

Calibration

DSDR calibration involves hot load (ambient absorber) and cold load (sky) measurements illustrated in Figures 4.23 and 4.24. For the hot load target, we constructed a $1\text{m} \times 1\text{m}$ polystyrene tray filled with Eccosorb microwave absorbing material that was placed in front of the antenna aperture. A thermometer is inserted into the blackbody absorber to measure the physical temperature and estimate the apparent brightness temperature. For the cold load, the sky can be used as a reliable L-band calibration source as long as there is no precipitation. Radiative transfer models of the downwelling brightness temperature $T_{B(sky)}$ predict a nearly constant value of 4.9 K from atmospheric emissions and cosmic background radiation, even for varying cloud cover and surface air temperature [77]. There is also a diurnal variation in $T_{B(sky)}$—up to 2 K change—due to non-thermal emissions from the plane of the Milky Way galaxy [44], but I will be neglecting this effect.

Sky test

After calibration, DSDR was rotated to zenith to observe the stability of sky brightness measurements over a 24 hour period. The recorded antenna and reference load brightnesses (T_A and T_{REF}) are plotted in Figure 4.25. The data exhibit unacceptably large variations of 10 K or more that can be attributed to sensor instability. First, the T_A data could not represent the actual brightness signature received by the antenna because the reference load

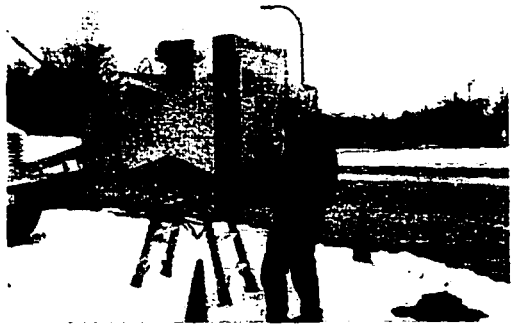


Figure 4.23: During hot load calibration, the aperture is filled with blackbody absorbing material at a known physical temperature.

Figure 4.24: Viewing the zenith sky brightness for cold load calibration. Radiative transfer models predict a consistent downwelling brightness temperature of 4.9 K at 1.4 GHz (with or without cloud cover).

is also changing erratically. Second, there appears to be a strong correlation between T_A and T_{REF} fluctuations, indicating that the noise sources are introduced after the SPDT switch in the front end. By studying the nature of this correlation, it may be possible to compensate for receiver fluctuations given the history of T_{REF}—just as a switched reference load is used to improve stability in a Dicke radiometer.

Figure 4.26 shows a scatter plot of the raw r_Q data output from the antenna and reference load during the diurnal sky experiment. The data points cluster along two main lines that describe different error mechanisms in the DSDR receiver. First there is a "gain" line having a slope of ~ 3.1, which is comparable to the ratio of average values for $r_{Q(ref)}$ and $r_{Q(sky)}$ over the course of the measurements. Thus errors along this line are caused by proportional (gain) changes for both hot and cold references. The second "offset" line has a slope of 1.3; a slope near unity suggests that the errors are caused by additive noise sources in DSDR that change both hot and cold brightness values equally. With both gain and offset error modes, there is no perfect correction scheme for recovering the true antenna

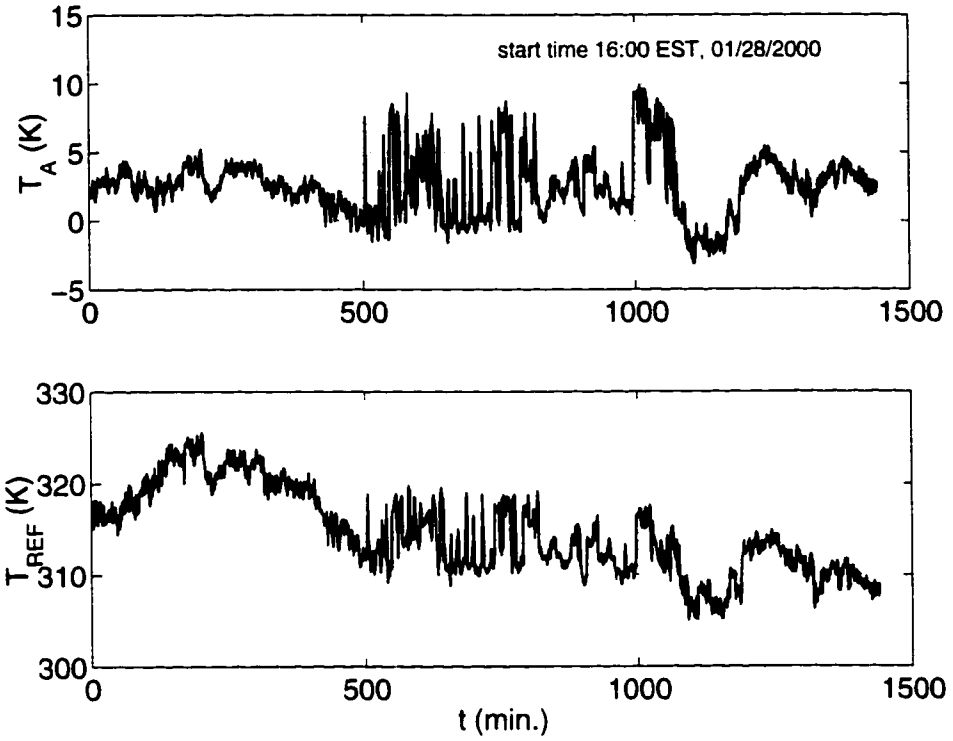


Figure 4.25: Antenna and reference load brightnesses recorded during the TMRS diurnal sky experiment. DSDR's elevation angle is set at zenith.

temperature as DSDR only provides one known degree of freedom, embedded in the T_{REF} data.

Design flaws

The results from lab and field experiments have led us to hypothesize several possible causes of instability in the receiver. Gain fluctuations in r_Q may be traced back to temperature changes in the A/D converter and mechanical stresses on the coaxial cabling between the front end and A board. The comparator slew rate in flash A/D converters is somewhat sensitive to physical temperature and can have the effect of altering the system gain over time. Lab tests have shown that r_Q can increase by as much as 3% when the SPT7610 package is point cooled from ambient operating temperature to $-50°C$. As for the microwave interconnections, significant changes in signal reflection and transmission can occur when the cables are flexed or stressed, resulting in large errors before A/D conversion. Later, I

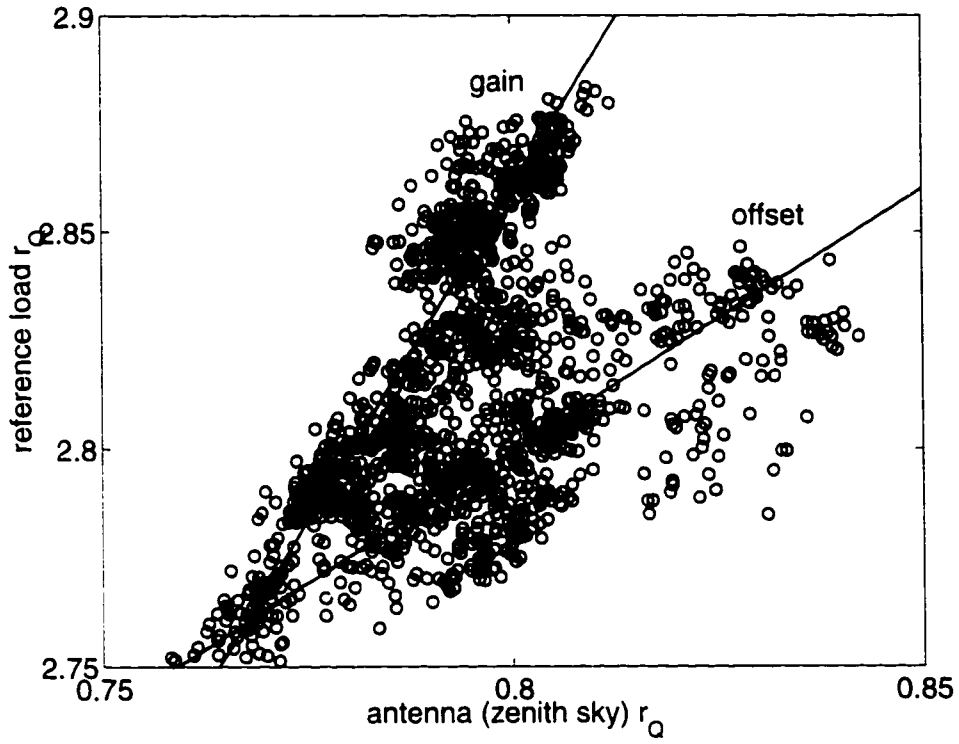


Figure 4.26: Scatter plot of $r_{Q(sky)}$-$r_{Q(ref)}$ data from the diurnal sky experiment.

found that r_Q could change drastically—on the order of 0.1-0.3 dB—by applying moderate force to a bulkhead coaxial interface on the A board. Flexible cabling and thermal gradients inside the radiometer may compound problems once DSDR is mounted onto the truck and rotated in elevation.

Offset fluctuations in the receiver may arise from poor isolation between the analog front end and other components in DSDR. The design started with a faulty grounding scheme which had all local grounds from the various circuit boards connected directly to the chassis. Consequentially, the front end shared a common impedance path with electrically noisy circuits, including the digital boards, relays and fans. Noise currents injected before the A/D converter could be detected as an unexpected jump in offset.

Electrical ground connections were often made by unreliable means—for example, with the bolts and screws that secure the aluminum enclosures to the mounting rack. Return current paths in the front end may then be affected by variables like mechanical stress or

corrosion, which are difficult to control in the field. (Later I discovered that the detected reference load brightness can increase ~ 7 K just by shorting the TEC box to the mounting rack with a glob of aluminum foil. Clearly, large errors could be introduced by altering the path of noise currents on the rack of the chassis.) Ott has commented on the importance of reliable ground connections in sensitive electronic equipment [46]:

> If the installation does not provide a good ground connection to the rack or panel, it is best to eliminate the questionable ground, and then provide a definite ground by some other means, or be sure that there is no ground at all. Do not depend on sliding drawers, hinges, and so on, to provide a reliable ground connection. ... Improperly made ground connections may perform perfectly well on new equipment but may be the source of mysterious trouble later.

Due to the wideband capabilities of LNA1, it is possible for out-of-band noise sources to cause the front end to saturate. The gain of the first amplifier is essentially flat over 1–2 GHz, with less than 1 dB rolloff over this range. Any change in the strength of interfering signals from fixed or mobile radio sources, or from within DSDR itself, could be manifested by a jump in the offset value of r_Q.

Transients generated by the switching temperature controller may be one of the largest sources of interference coming from inside DSDR. For the heater control, the on-off transition in duty cycle induces a momentary 25×10^3 A/s change in load current which can be picked up by the receiver through inductive coupling.

The outdoor winter tests revealed some practical design problems at very low ambient temperatures. Below $-10°$C, we observed unusually large oscillations in detected brightnesses—for example, see Figure 4.25 data from midnight ($t \approx 500$ min.) to 6:00 am ($t \approx 850$ min.). Also, low temperatures occasionally resulted in a loss of communication with the temperature control circuitry. (This was remedied by increasing the set temperature of the TEC box to heat the adjacent T board.) Another problem was the misconfiguration of the FPGA digital correlator. Often the M board had to be warmed with a heat gun before configuration data could be successfully loaded from the EPC2 to EPF10K20. I suspect

that many of the malfunctions encountered during the winter shakedown were symptoms of poor electrolytic capacitor performance at low temperatures. Inadequate filtering of power and reference lines often leads to oscillations that can disable electronic systems.

4.7 Design Improvements

Lessons learned from DSDR lab tests, the winter shakedown, and a summer REBEX-7 campaign in Southeast Michigan helped pinpoint a number of design problems in the prototype hardware and firmware. In this section, I will enumerate the main modifications that were made to counteract these problems and improve the radiometer's performance.

4.7.1 Duty cycle squelch

I first suspected duty cycle transients as a source of noise after noticing that the monitored r_Q data showed fewer abrupt changes when temperature control was off. To test this theory, the stability of $r_{Q(ref)}$ was compared for two cases: (a) with the DSDR duty cycle running continuously, and (b) with the duty cycle blanked out, or squelched, during the radiometer's integration time (Figure 4.27). The results show considerable improvement in short term stability using duty cycle squelch. While there are still some precipitous jumps in case (b), there also can be seen, for the first time, several continuous hours of non-spurious r_Q readings.

RaDOS 0.0 was revised to blank the temperature duty cycle during each correlation. It should be mentioned that the blanking period introduces some error into the closed-loop temperature control, as the actual time-averaged power of the heater or cooler will be less than the expected power at the end of each update period. This error is usually insignificant, though, for an integration time $\tau \leq 1$ s.

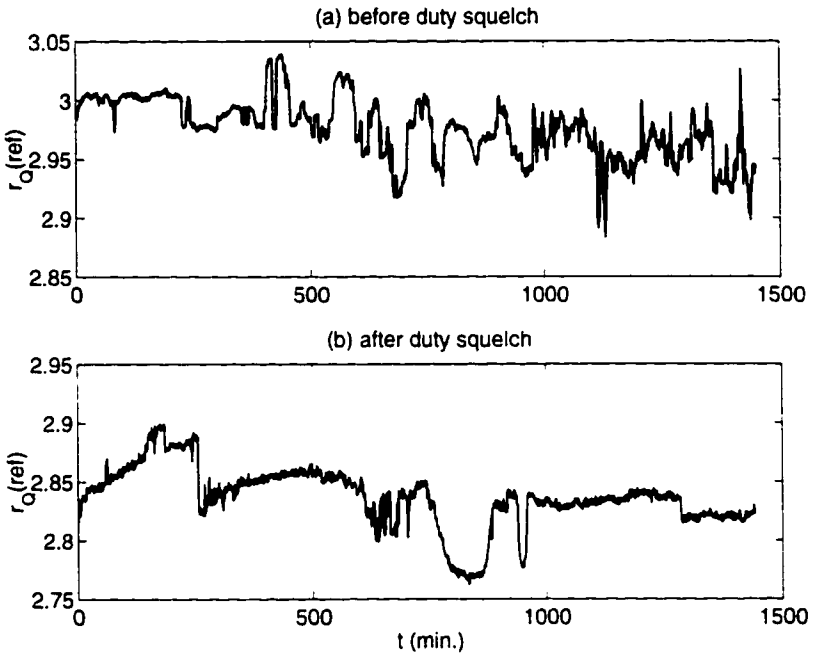


Figure 4.27: Comparison of the reference load r_Q stability (a) before and (b) after applying the duty squelch countermeasure.

4.7.2 Bias-T network

Early in the tests, an unexpected increase in NEΔT was observed for larger bit resolutions ($\geq$ 2.5 bits). The root cause of this problem was traced back to a mismount on the EB7610 evaluation board, causing a large impedance mismatch in the bias-T network that preceded the A/D converter. This was remedied by mounting an RF choke inductor between the dc reference line and ac input to the SPT7610.

4.7.3 Line filters

A common-mode filter was added to the 120 Vac line that powers DSDR to reduce conducted line noise, which may interfere with radiometer operation. Also, ferrite beads were added onto the front end LNA power (+15 Vdc) and ground lines to filter out undesired high frequency noise.

4.7.4 Reliability of FPGA configuration

As mentioned, the configuration protocol between the EPC2 EPROM and EPF10K20 would occasionally fail during the power up sequence. This problem may be caused by a slow 5V (Vcc) rise time on the M board: Altera specifies a rise time of no more than 100 ms to ensure proper configuration, but the rise time for DSDR was longer—approximately 140 ms—due to the large capacitance of the SPT7610 fan. I added a circuit to the G board which would gradually apply the fan load over a 1 s period, thereby reducing the FPGA's Vcc rise time to 65 ms.

Configuration problems continued even after the G board modification, particularly when the M board was cold. While investigating the failure mechanism, I discovered that a status line on the serial bus running from the EPF10K20 to the EPROM would spontaneously change state in the middle of data transmission, halting the configuration and disabling DSDR. However, by applying heat to the FPGA, this status line would remain in its enabled state during the entire loading sequence. For deployment outdoors, A 50 W silicon heater with heat sensitive fuse and fan were attached inside the M box so that the case temperature could be raised to 50–60°C.

4.7.5 Digital correlator version b (*digcorrb*)

I made several revisions to the digital correlator to create a new design, named *digcorrb*, for improved performance (Figure 4.28). First, all data were pipelined through a number of flip-flop registers, synchronized to a global clock, to ensure a stable and predictable flow of data between the various logic modules. A 6-bit register was also added at the front of the correlator so that bits from the A board could be latched in the middle (most stable) period of the data transition cycle. A new 28-bit *down-counter* module was designed to solve some timing inconsistencies found in the original *count* module, which defines the integration time. Specifically, the old logic would overcount the correlation by several samples due to

imperfect timing from an asynchronous enable signal. The *down-counter* solves this problem by breaking up "load" and "enable" functions into two separate operations that must be initiated externally (by the SmartCore bus), and by synchronizing the accumulator enable signal to the global clock. When *digcorrb* was later tested with a static bit pattern, it was confirmed that the circuit always counted to the desired sample length.

4.7.6 Grounding

DSDR's ground topology was modified in the Spring of 2000 to improve the isolation between the analog front end and other circuitry. Ground leads from the various DSDR boxes were tied back to signal ground on the Acopian supplies in a "star" configuration so that these return paths would not overlap. Signal and chassis grounds were separated, wherever possible, before reaching the service entrance of the 120 Vac power source: the front end plate and TEC were electrically isolated from one another using a mica spacer and nylon screws; ground patterns on M, T, X, R, and C boards were cut away to prevent a direct short to chassis ground through the metal standoffs; bulkhead coaxial connectors with isolated shrouds were added to A and C cases to prevent noise currents from leaking back to the input of the first LNA. The questionable electrical connection between the aluminum DSDR boxes and the mounting rack was replaced with a braided grounding strap, secured with screws and self-clinching nuts to the metal surface.

4.7.7 TEC efficiency

DSDR had to be prepared for cooling operation before the REBEX-7 experiment, conducted in Britton, Michigan during the summer season. We improved the radiometer's rate of heat flow by mounting heat sinks and a fan on the outside of the Zero case, directly below the TEC box, and then cutting an aperture into the mounting flange of the antenna. With this new configuration, the sink assembly protrudes outside of the enclosure, where it can be purged with ambient air. The single TEC ran efficiently over the summertime diurnal

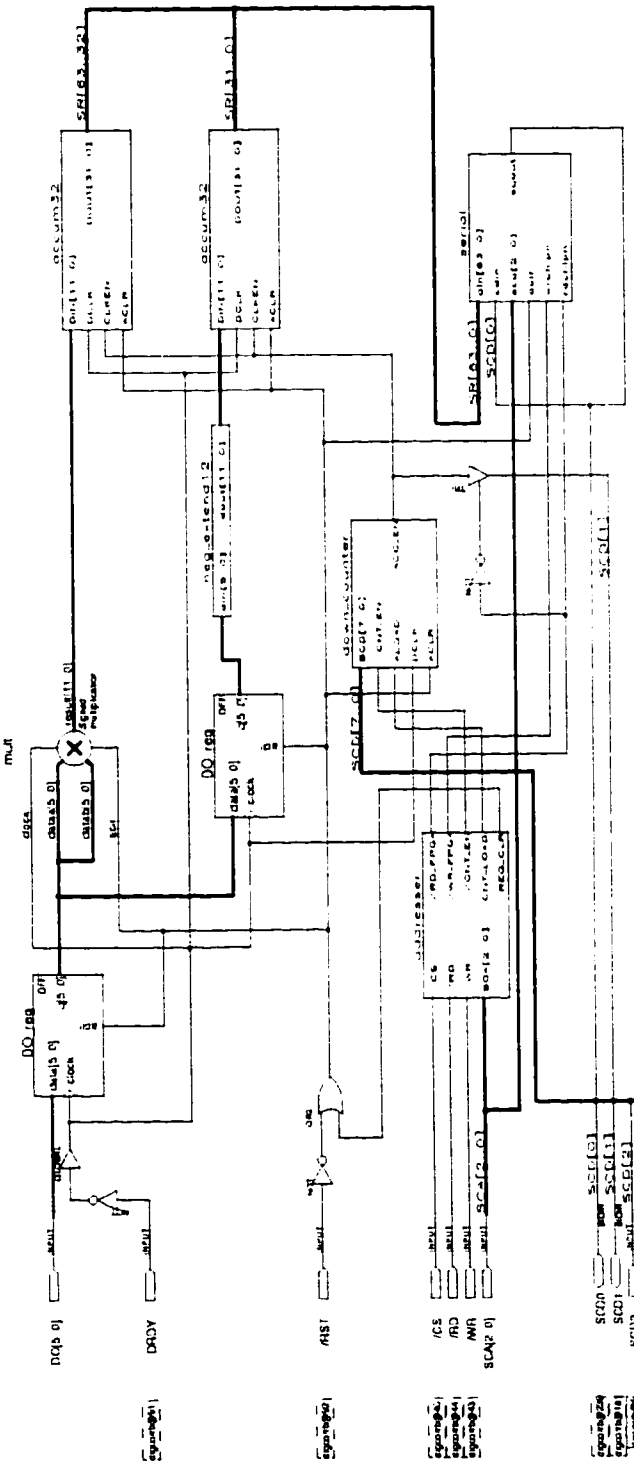


Figure 4.28: Top-level graphic design file for *digcorrb*.

cycle, although the controller output occasionally saturated at 0% or 100% duty during the coldest or hottest times of the day.

4.7.8 Front end pre-filter

Other research groups experimenting with L-band radiometer systems have documented the effectiveness of placing an RF bandpass pre-filter before the receiver's first amplification stage. One example is the L-band Scanning Low-Frequency Microwave Radiometer, a phased array system deployed onto a low flying aircraft for ocean salinity experiments over the Chesapeake Bay. During initial airborne experiments conducted by the University of Massachusetts, radiobrightness data were severely corrupted by ground-based, human made RFI sources, which caused the first stages of amplification in the front end to saturate. The detection of undesired RFI was eliminated on subsequent flights by adding a pre-filter [18].

During REBEX-7, we added a 2-pole cavity resonator bandpass filter, centered at 1413.5 MHz, in front of the first LNA module to reduce the effects of out-of-band noise sources. (Figure 4.29 shows the jury rig assembly for DSDR1.) This pre-filter provides a gradual rolloff of 1 dB at ±20 MHz and 30 dB at ±275 MHz. The exact bandwidth and shaping factor were chosen out of necessity to keep the device size small for front end assembly modifications and to control the receiver noise temperature; a low-order filter design turned out to be the most practical solution, as it offered a compact package size ($1.75'' \times 1.5'' \times 0.625''$) and low center frequency insertion loss (0.75 dB). For fabrication of the second DSDR receiver, the pre-filter will be machined directly to the front end plate to improve the regulation of its physical temperature and thermal noise emission.

4.8 Summary

This chapter has traced the design chronology of the first operational L-band DSDR radiometer from conception to deployment in the field. Lab tests show the total power hardware performing near the fundamental sensitivity limits predicted in Chapter 2. How-

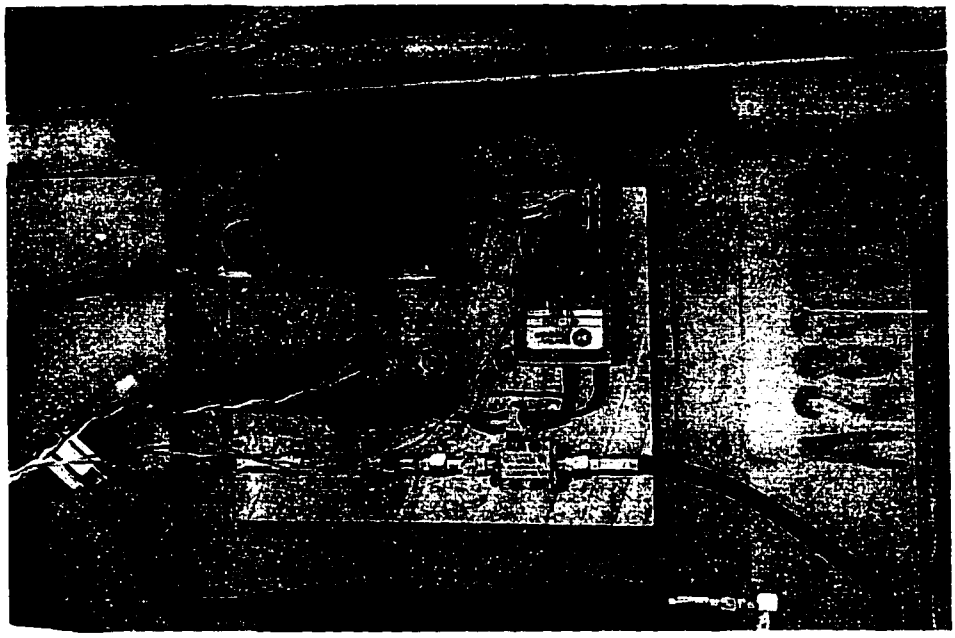


Figure 4.29: Photo of the modified DSDR1 front end after the RF pre-filter has been added. The pre-filter, shown as the rectangular package in the upper left corner of the cold plate, is connected between the antenna/reference switch and the first LNA with coaxial cables.

ever, there were also a number of production problems discovered, particularly during field evaluation, that affected the sensor's stability and reliability. Many flaws in the prototype design could be inferred from data analysis and have since been corrected. Experience gained in this study will be applied toward the design and fabrication of the second receiver channel (DSDR2) for the two-element correlator.

CHAPTER 5

Configuring DSDR as a Cross-Correlation Receiver

5.1 Fabricating the DSDR2 Receiver

The second DSDR receiver was designed to interface with the first channel so that together the two could operate as a correlation radiometer. The features in DSDR2 combine lessons learned in the previous chapter with some new design ideas that reduce circuit complexity. While the two receivers are not exact duplicates of each other, an effort was made to design the circuitry for backward compatibility; such a configuration has helped in the troubleshooting and characterization of the correlator. In this section, the unique features of the DSDR2 hardware and software will be presented. (See also Appendix C for circuit diagrams specific to the second receiver.)

5.1.1 New front end

Latching microwave switch

To solve the front end temperature stability problem described in Section 4.6.1, a microwave SPDT switch that uses a latching mechanism was added to the DSDR2 front end in place of the failsafe switch that had been used previously. This new device can switch between antenna or reference channels with only a momentary (15 ms) pulse to its solenoid, controlled via the RaDOS software. The net heat injected into the front end plate during a brightness measurement cycle is thus much less than the heat generated by the failsafe switch, which requires continuous current during the reference load integration time. The

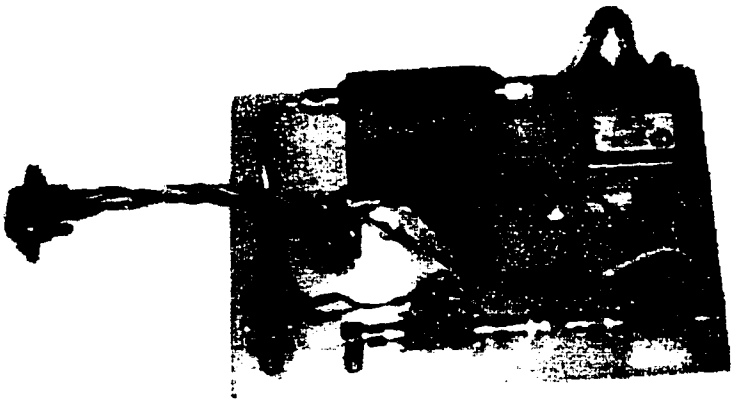


Figure 5.1: DSDR2 front end assembly with design revisions: latching SPDT switch, RFI pre-filter, and local 3-terminal regulator.

performance of the front end temperature control with the new SPDT switch will be evaluated in Section 5.3.1.

Pre-filter assembly

The front end pre-filter described in Section 4.7.8 reduced the influence of out-of-band noise sources. In DSDR2, the front end was redesigned so that this pre-filter could be directly mounted to the thermal plate, allowing its noise temperature to be regulated along with other lossy components. Mounting holes were machined into the new plate to bolt the filter in place, and, as with the LNA packages, silicon compound was applied between the filter-plate interface to increase thermal coupling to the TEC.

Location of LNA regulator

The 3-terminal regulator that powers the LNA chain was moved directly to the front end plate in the DSDR2 design. This arrangement avoided the long ($\sim$ 50 cm) power leads found in DSDR1, which ran from the R board to the front end. Twisted pair leads that supply dc power to sensitive circuitry generally should be kept as short as possible to prevent high frequency ringing and inductive pickup from adjacent wire harnesses [47]. Figure 5.1 shows the complete assembly for the new DSDR2 front end.

5.1.2 T2 board

Success with the FPGA digital correlator in DSDR1 had convinced me that reconfigurable logic would also be a valuable tool for the second temperature control board (T2). The circuit in T2 was modified to integrate most of the digital functions for the duty cycle driver and addressing logic onto a single FPGA—the Altera EPM7128S. This device is from the MAX7000 family (discussed in Section 4.3.6), which uses the same floating gate programming technology found in EEPROM chips. Therefore, configuration is only required once, during the design phase; afterwards, the FPGA will automatically power up in user mode for DSDR operation in the field. Non-volatile memory storage simplifies the circuit operation and improves the reliability, as there is no need for an initial boot-up sequence.

Figure 5.2 shows the graphic design file for *tempcon*, the digital temperature controller configured onto the EPM7128S. In this design, two independent control channels were added to permit dual TEC operation for future expansion, similar to the arrangement in Tanner's Advanced Water Vapor Radiometer [73] that was described in Section 4.3.5. One duty cycle generator is dedicated to the front end TEC, while another generator controls the roughing chamber TEC for heat transfer outside of the radiometer's enclosure. An addressable latch in *tempcon* provides clock and data signals for communication with the thermistor A/D converter and also serves as a line driver for the new microwave SPDT switch.

Most of the digital logic on the original T board was composed of common medium-scale integration (MSI) chips. By introducing the FPGA into the T2 design, the chip count in the temperature control circuit could be reduced significantly, from 13 to 6 ICs; at the same time, the flexible nature of the FPGA allows T2 to evolve as the user's needs change. The T2 signal I/O is configured to be backward compatible with the T board, so both boards are interchangeable in single-TEC radiometer systems. A photograph of the completed T2 board is shown in Figure 5.3.

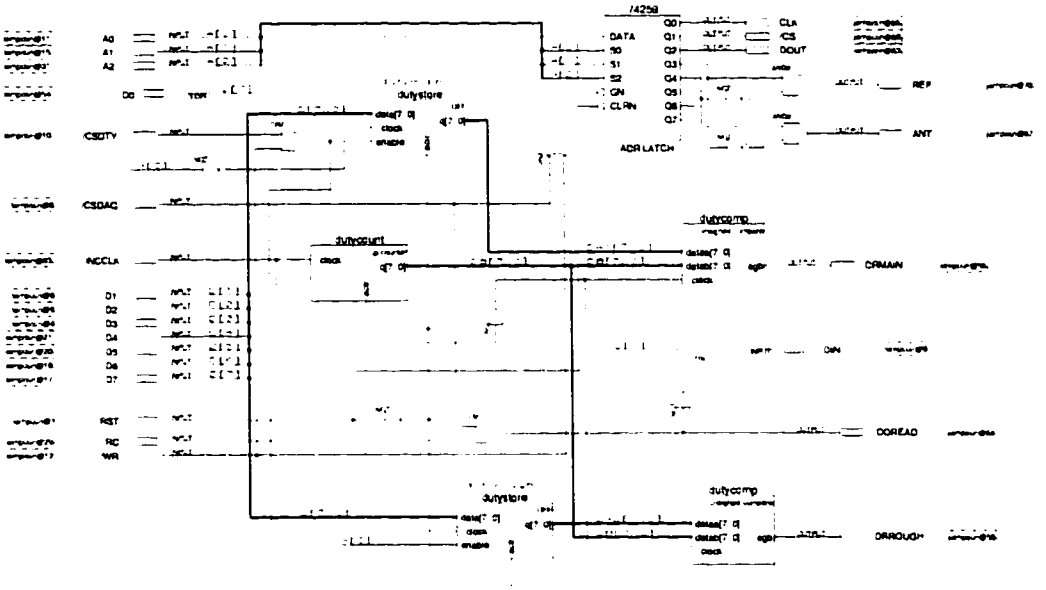


Figure 5.2: Graphical design file for *tempcon*, an FPGA-based temperature control circuit for the second DSDR.

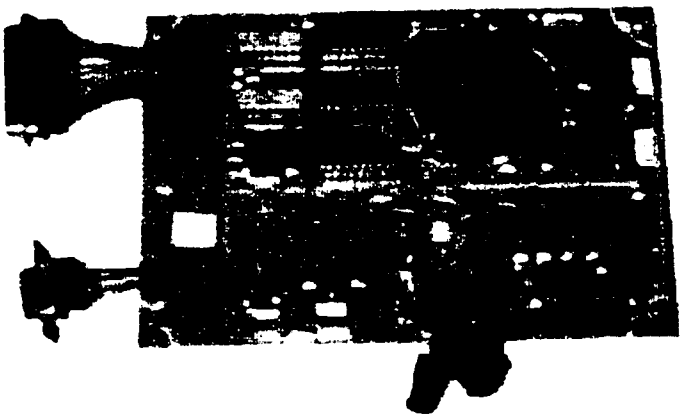


Figure 5.3: Photo of the mounted T2 temperature controller board.

5.1.3 Digital cross-correlator

On the M board, the EPF10K20 firmware was revised to handle the cross-correlation processing between two digital channels. This processing is analogous to the case of a total power DSDR, except that now the quantity of interest is the covariance between the pair of received signals:

$$r_{Q12} = \langle (\hat{x} - \langle \hat{x} \rangle)(\hat{y} - \langle \hat{y} \rangle) \rangle \approx \frac{1}{N} \sum_{n=1}^{N} \hat{x}_n \hat{y}_n - \frac{1}{N^2} \left(\sum_{n=1}^{N} \hat{x}_n \right) \left(\sum_{n=1}^{N} \hat{y}_n \right). \tag{5.1}$$

Note that the end terms in (5.1) are just the first order accumulator values for DSDR1 and DSDR2. Therefore, the total power detect outputs r_{Q1}, r_{Q2} and the cross-correlation output r_{Q12} can be processed simultaneously with five accumulators.

I created a new FPGA design file called *digcorrc*, which includes two total power detect modules (*tpdetect*) and one cross-correlation module (*ccdetect*) for the correlation DSDR processing. (See Appendix D for the design file listing.) To conserve resources within the EPF10K20, the input data streams for both channels are truncated from 6 to 5 bits. The gate count is further reduced in the *tpdetect* sections by using ROM look-up tables instead of arithmetic multipliers to square the incoming data. For the cross-correlation processing, *ccdetect* uses a 5 × 5 bit signed multiplier and a standard 32-bit accumulation register. All together, a total of 160 bits of information are generated over each integration period by five 32-bit accumulators. The parallel-input/serial-output shift register, *serial2*, concatenates the raw data from the accumulators and serially transmits the 160-bit word back to the SmartCore.

5.1.4 Other boards and modifications

I procured an additional A/D evaluation board (A2) and built duplicate circuit boards for the DSDR2 ECL power supply (G2) and ECL-CMOS translator (X2). The R2 board was also upgraded with a pair of solid-state relays to drive the new front end switch.

To make DSDR work as a cross-correlator, the C board was modified to generate a

second, identical 160 MHz clock signal that feeds into the A2 board. One potentially serious complication that arises from the divide-by-16 decimation feature on A and A2 is that, when power is first applied, the correlation DSDR can randomly start up in one of 16 possible timing conditions—with up to ±50 ns delay between samplers. This symptom, which I dubbed "DSDR roulette," required careful monitoring of the 10 MHz timing signals returning from the decimation circuitry to the M board during correlation experiments. But in a flash of serendipity, this design flaw could also be used to advantage for characterizing the fringe washing function over a wide range of delay times. The details of the fringe washing tests and some of the related findings will be discussed later in Sections 5.4–5.5.

5.2 Software Revisions

The original RaDOS 0.0 code was modified to confirm the operation of DSDR2 as a stand-alone (total power) radiometer and to test the effectiveness of a number of design changes. The ramp-up version of RaDOS is similar to version 0.0, except that addresses for the temperature sensors, duty cycle driver, and front end switch have been changed to select those devices from DSDR2 rather than DSDR1. Because the functions of the command-line interpreter are the same for either total power radiometer, DSDR2 in stand-alone mode can be controlled directly from FluxMon2.

Next, I wrote a new version of the DSDR software, called RaDOS 1.0, which controls the two radiometer channels for cross-correlation measurements. In this version, both receivers are fully addressable, and two separate temperature control algorithms can run concurrently using the SmartCore's real-time kernel. The protocol with the digital correlator has also been upgraded to retrieve the full 160-bit accumulation register and compute the floating point values for r_{Q1}, r_{Q2}, and r_{Q12}.

RaDOS 1.0 is intended for developing the correlation DSDR in the lab. To expedite the lab tests, I bypassed the command-line interpreter and instead connected the SmartCore

microcontroller directly to one of our benchtop PCs, via a serial interface bus. RaDOS can be modified and recompiled on the fly with this setup, using the SmartCore's software development tool for Windows. Correlator output data from DSDR is redirected to a standard I/O terminal and eventually logged to a hard drive, where it can be retrieved later for analysis.

5.3 Stand-Alone DSDR2 Measurements

5.3.1 Temperature stability

The results from several DSDR2 temperature control tests, summarized in Table 5.1, confirm the improved performance with the latching front end switch. For all tests, the physical temperature of the receiver was regulated down to 290 K with the thermoelectric cooler. Cycling through antenna and reference brightness measurements once per minute, and integrating each channel over 1 s, the front end stabilized to within $\Delta T_p = 37.1$ mK rms of the set temperature (as measured by the plate thermistor). For comparison, refer back to the 59.0 mK result for DSDR1, listed in Table 4.6. The effectiveness of the switch is actually greater than these numbers suggest, but is masked by errors arising from the blanking of the TEC duty cycle during integration: DSDR2 exhibited a comparable temperature stability of 31.4 mK for the case of no SPDT switching and 1 s integration, whereas the stability improved significantly to 11.8 mK when there was no SPDT switching *and* no integration. The full benefit of the latching switch may eventually be realized by implementing a linear controller for the TEC and eliminating duty cycle squelch.

5.3.2 Detect output stability

The total power detect output r_{Q2} was monitored over a 24 hour period while the receiver viewed a matched load at 290 K (Figure 5.4). For this experiment, I set the integration time to ~ 1 s ($N = 10.5$ Msamples), the converter resolution to 3.2 bits, and the brightness update period to 1 minute. There is a distinct improvement in the stability of the detect

test	condition	ΔT_p	ΔT_G
1	no SPDT switching, no r_{Q2} integration	11.8 mK	64.8 mK
2	no SPDT switching, $r_{Q2(ant)}$ integration	31.4 mK	172 mK
3	SPDT switching, $r_{Q2(ant)}$ and $r_{Q2(ref)}$ integration	37.1 mK	204 mK

Table 5.1: Physical temperature stability of the DSDR2 front end (ΔT_p) and the associated NEΔT component from gain variations (ΔT_G).

output compared to the original performance of DSDR1, which exhibited unexpected offset and gain fluctuations (for example, refer back to Figure 4.27). Qualitatively, the DSDR2 data show excellent short term stability, with fluctuations that are characteristic of white Gaussian noise. Long term drifts, possibly due to aging of the electronics and microwave cabling outside of the TEC enclosure, are generally monotonic over time and could be removed through calibration by comparing antenna and reference load brightnesses.

The detect output SNR was estimated by finding the mean and standard deviation of r_{Q2} over a 20 minute window of data, and then averaging these results over the entire 24 hour period. These calculations yield an empirical SNR of 32.3 dB, which comes close to the theoretical value of $SNR_F = 33.6$ dB, predicted with (2.28) and (4.18). The remaining discrepancy of 1.3 dB is attributed to receiver gain errors from the duty cycle squelch countermeasure. Given the 1 s integration time, the noise equivalent sensitivity due to gain fluctuations is approximately 172 mK from Table 5.1, test case 2, and the corresponding SNR is

$$SNR_G \approx \frac{T_{SYS}}{\Delta T_G} = \frac{400 \text{ K}}{0.172 \text{ K}} = 33.7 \text{ dB}. \tag{5.2}$$

The total SNR of the detect output from statistical noise components and from changes in gain is given by

$$SNR_{(net)} = \left[\left(\frac{1}{SNR_F} \right)^2 + \left(\frac{1}{SNR_G} \right)^2 \right]^{-1/2} = 32.1 \text{ dB}, \tag{5.3}$$

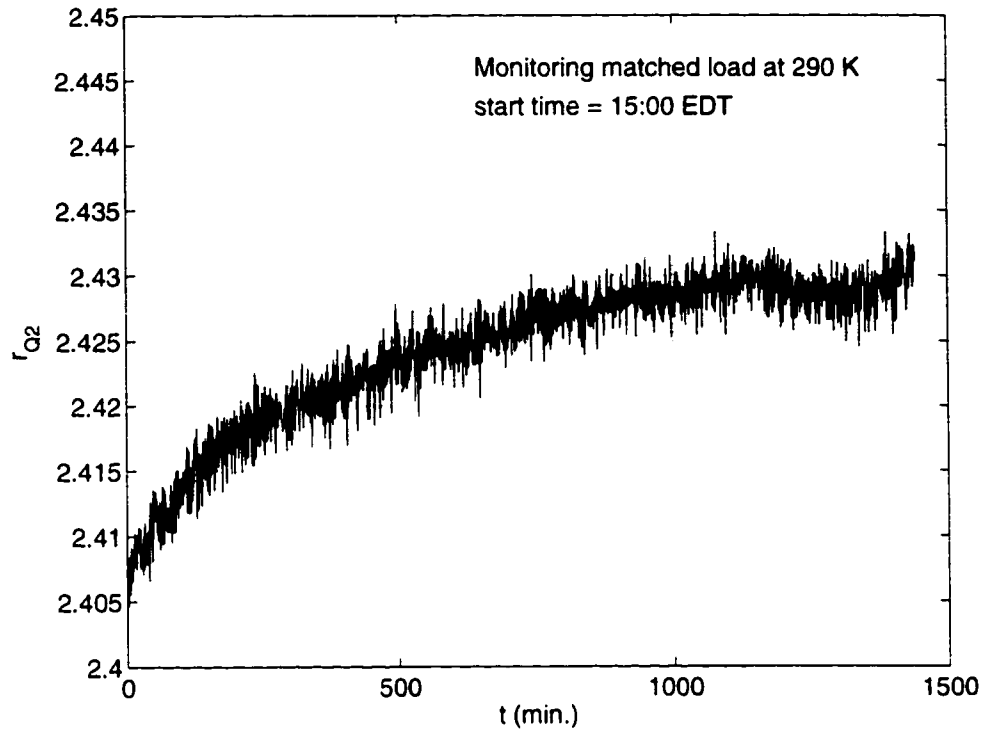


Figure 5.4: 24 hour monitor of the DSDR2 detect output signal.

only 0.2 dB away from the actual measured value. In the next section, the empirical NEΔT will be studied in detail for the case of a shorter integration time setting, where $\Delta T_G << \Delta T_F$.

5.3.3 NEΔT vs. bit resolution

The sensitivity of DSDR2 was measured for various bit resolution settings by following a procedure similar to that outlined in Section 4.6.4. Eleven separate r_{Q2} data sets, each 180 minutes in duration, were recorded over a range of gain settings while DSDR2 monitored a thermally regulated reference load. The integration length was shortened to $N \approx 1.0$ Msample to reduce the effect of temperature errors caused by duty cycle blanking. Using (4.19), the empirical NEΔT can then be inferred from the mean signal $\langle r_{Q2} \rangle$ and standard deviation σ_{Q2} of each data set.

The experimental sensitivity results are plotted in Figure 5.5 along with the theoretical

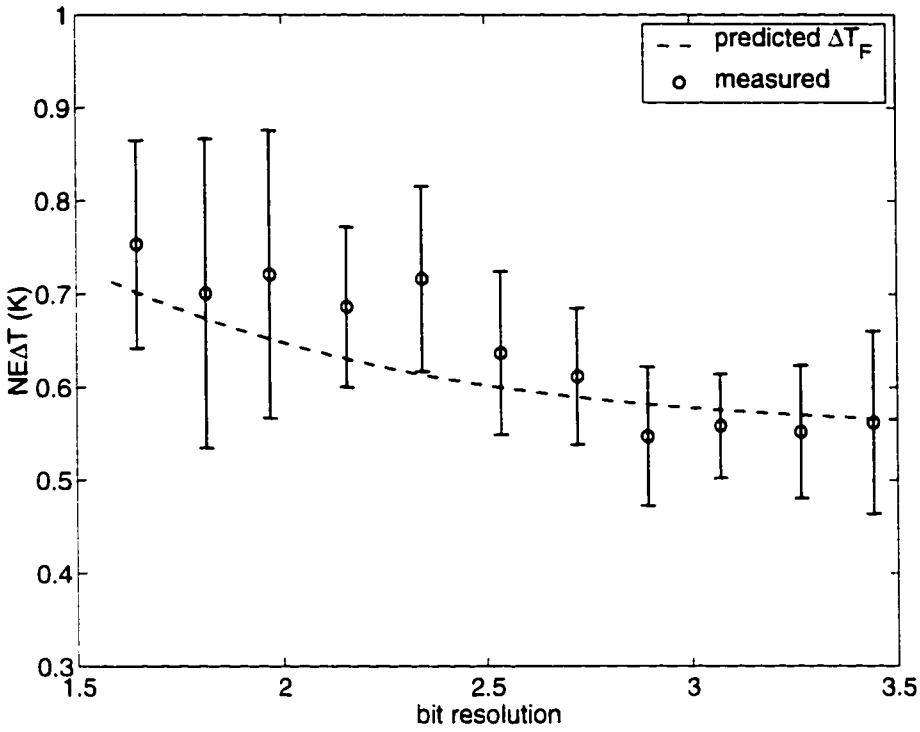


Figure 5.5: Predicted and measured sensitivity results for DSDR2, operating in total power mode. Here, T_{SYS} is taken to be 400 K, and the effective integration time of the radiometer is set to 0.025 s (referenced to the Nyquist rate). The error bars denote ± 1 standard deviation in NEΔT data collected over a 180 minute period and computed locally over a 20 minute window.

curve predicted by the total power DSDR analysis, given a typical system noise temperature of 400 K. On average, the measured NEΔT for each bit setting is within a few hundredths Kelvin of the predicted value; the maximum discrepancy at 2.3 bits is no greater than 0.1 K, or 18% error, and generally the expected sensitivity falls within ± 1 standard deviation of each data set. The agreement between predicted and measured NEΔT indicates that most of the interference problems encountered during the DSDR1 sensor investigation have been solved through design changes enumerated in the last two chapters, and that the upgraded DSDR2 hardware is performing near its fundamental sensitivity limit.

5.4 Characterization of the Correlation DSDR

5.4.1 Noise-floor measurements and NEΔT

Isolation

To begin looking at the noise floor of the correlator hardware, I connected a pair of reference loads to the two receivers to measure the signal r_{Q12} and its standard deviation σ_{Q12}. Ideally, the output signal should be zero in this case because the two loads act as independent noise sources. The actual hardware will yield some non-zero offset value, though, which is a measure of the cross-correlation purity between receivers.

Visibility measurements were taken with DSDR1 and DSDR2 adjusted for 2.2 bit sampling resolutions. Because there is always some difference between the receiver gains, detect output values r_{Q1} and r_{Q2} are not exactly equal. The most general definition of the correlation coefficient takes this imbalance into account by normalizing with respect to the geometric mean of the signal powers [51]:

$$\rho = \frac{\langle xy \rangle}{\sqrt{\langle x^2 \rangle \langle y^2 \rangle}} \approx \frac{r_{Q12}}{\sqrt{(r_{Q1} - 1/12)(r_{Q2} - 1/12)}}. \tag{5.4}$$

With the two receivers synchronized, DSDR generated $\rho = -27.1$ dB, indicating good cross-correlation isolation between receivers. (Measured isolation values of -30 dB or less are considered excellent.) In an actual STAR experiment, this offset value would be calibrated out of each visibility sample.

Theoretical sensitivity

Variations in r_{Q12} were also investigated to determine the noise-equivalent sensitivity. Recall from Chapter 3 that the noise riding on the correlator output can be expressed as an equivalent input-referred noise temperature by substituting (3.27) into (3.30). For the DSDR hardware, which exhibits a weak autocorrelation function at the relatively low 10

MHz sampling rate, this input temperature is approximately

$$\Delta T_{CORR} = \frac{T_{SYS}}{\sqrt{N}} \left(1 + \frac{1}{12s^2}\right). \tag{5.5}$$

According to (3.31), ΔT_{CORR} represents the sensitivity for a source at boresight—a useful benchmark for evaluating the correlation DSDR. Also, as the signal resolution s becomes large, ΔT_{CORR} will be a factor of 1.5 dB better than the total power DSDR sensitivity expressed in (4.18). The empirical sensitivities for both total power and correlation cases can be measured simultaneously with the hardware to verify these relations.

Experimental results and discussion

As in Sections 4.6.4 and 5.3.3, a series of noise floor experiments were conducted over resolution ranges from 1.7–3.4 bits to study the effect of quantization. For each bit setting, 180 minutes of continuous, spurious-free r_Q data were collected and analyzed. The observed sensitivity of the correlation DSDR can then be calculated by combining (3.30) and (5.4) to yield

$$\Delta T_{12(meas)} = \sigma_{Q12} \cdot \frac{T_{SYS}}{\sqrt{\langle x^2 \rangle \langle y^2 \rangle}} = \frac{\sigma_{Q12} T_{SYS}}{\sqrt{(r_{Q1} - 1/12)(r_{Q2} - 1/12)}}. \tag{5.6}$$

The empirical sensitivities for total power DSDR1, total power DSDR2, and the correlation DSDR are plotted in Figure 5.6, along with the corresponding theoretical sensitivity relations from (4.18) and (5.5). The total power data fall within ≤ 0.15 K of the theoretical NEΔT, roughly matching the experimental error range in Figure 5.5. The cross-correlation sensitivity measurements show excellent agreement with the theoretical curve and confirm that, for negligibly small ρ, the performance will improve by a factor of $\sqrt{2}$ over the total power case.

The apparent robustness of the cross-correlation data has to do with the statistics of viewing two uncorrelated sources. Gain fluctuations in either receiver channel will cause a proportional change in the output variance, σ_{Q12}, but will not affect the signal, which is

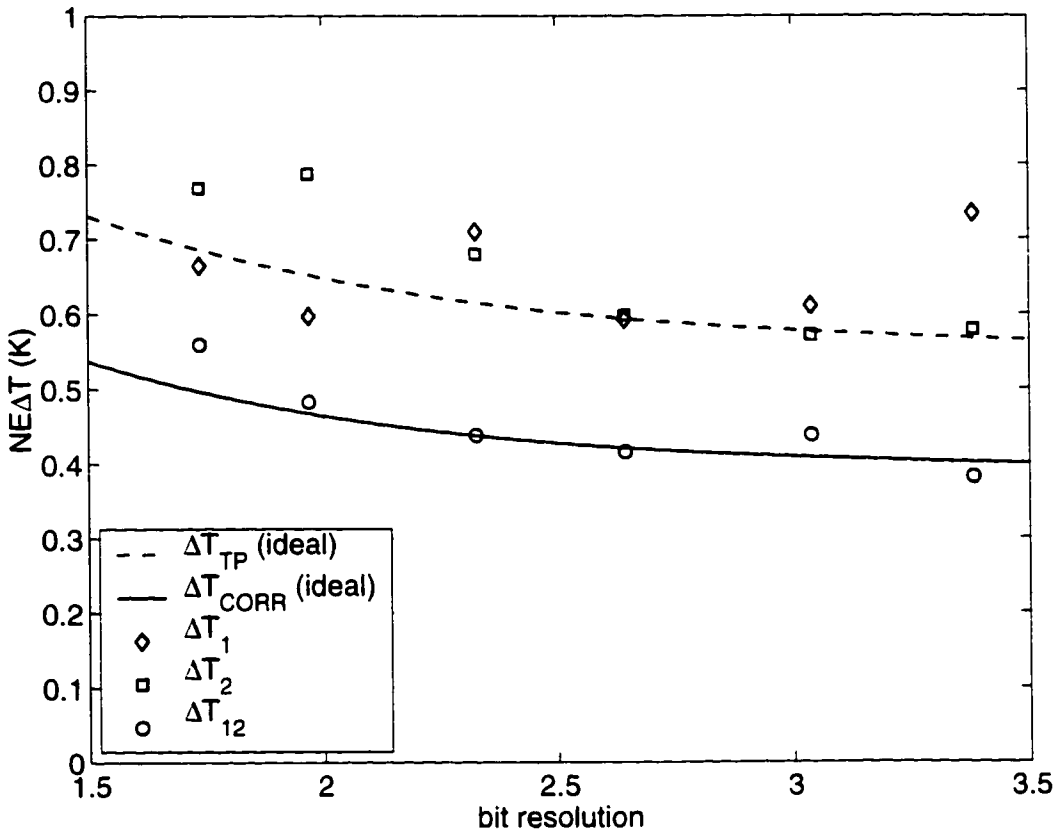


Figure 5.6: Sensitivity results for the two-channel DSDR system viewing a pair of independent noise sources. The dashed and solid curves represent the theoretical noise limits of the total power and correlation DSDRs, respectively. The empirical sensitivities are calculated and plotted for channel 1 total power (ΔT_1), channel 2 total power (ΔT_2), and cross-correlation (ΔT_{12}) cases. For all experiments, $N = 10^6$ and $T_{SYS} \approx 400$ K.

essentially zero. However, a change in gain would directly affect total power signals r_{Q1} or r_{Q2}. As an example, suppose that there is a 1% increase in the power gain of DSDR1: the average value of r_{Q12} would stay at zero, while the variance of r_{Q12} would increase by 1%—a modest change in NEΔT; on the other hand, there would be a 1% jump seen in the detect output r_{Q1}, which would cause a disproportionately large degradation in sensitivity. I observed a similar condition during the noise floor experiments. Even though a few mysterious bugs remained in the DSDR1 hardware and occasionally causes spurious shifts in the r_{Q1} output, the recorded r_{Q12} data showed no discernible change in mean value or standard deviation.

The stability of r_{Q12} will, however, be affected by receiver gain changes once there is some correlation between the pair of signals. Also, the statistical variation in r_{Q12} will increase as the correlation becomes progressively larger; take for instance the limiting case, $\rho = 1$, at which point the correlation DSDR becomes mathematically identical to the total power DSDR. Thus the results in Figure 5.6 for correlation and total power sensitivities can be treated as the lower and upper bounds of the radiometer's performance in STAR, where a variety of signal sources are encountered.

5.4.2 Phase coherence

A pair of partially correlated noise sources were injected into DSDR to investigate the phase stability of the instrument (see Figures 5.7 and 5.8). The correlated noise component is generated by a noise diode and Wilkinson power divider that equally splits the signal between the two DSDR receivers. An adjustable phase shifter is added to the DSDR2 clock for control of the relative phase difference between samplers; therefore the user can sweep through part of a grating lobe cycle and measure the peak correlation value, which, in the case of STAR, represents the in-phase component of a complex visibility sample. Comparing the theoretical and experimental peak values of ρ will indicate how well the

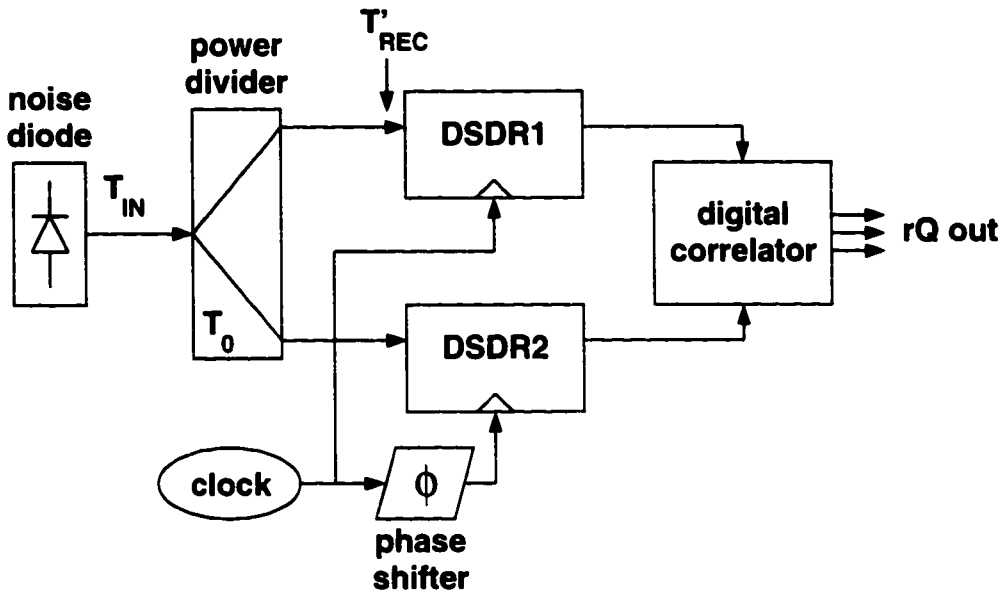


Figure 5.7: Block diagram of the experimental setup for measuring phase coherence.

correlation DSDR can maintain phase coherence.

Correlation model

There are three types of noise sources that can be detected by the DSDR receivers in Figure 5.7: correlated, uncorrelated, and anticorrelated noise. The correlated noise is the common component generated with the diode and 3 dB power divider; for an input noise temperature T_{IN} and cable losses L_C between the power divider and receivers, the correlated temperature is

$$T_{CORR} = T_{IN}/2L_C. \tag{5.7}$$

Uncorrelated noise arises from sources that are unique to each DSDR channel, like the front end receiver noise and emissions from cables; if the hardware is at a physical temperature T_0, the uncorrelated noise temperature will be

$$T_{UC} \approx T'_{REC} + T_0\,(1 - 1/L_C)\,. \tag{5.8}$$

Anticorrelated noise, or noise with a 180° phase difference between channels, is generated internally by the Wilkinson power divider and will lead to the detection of a negative

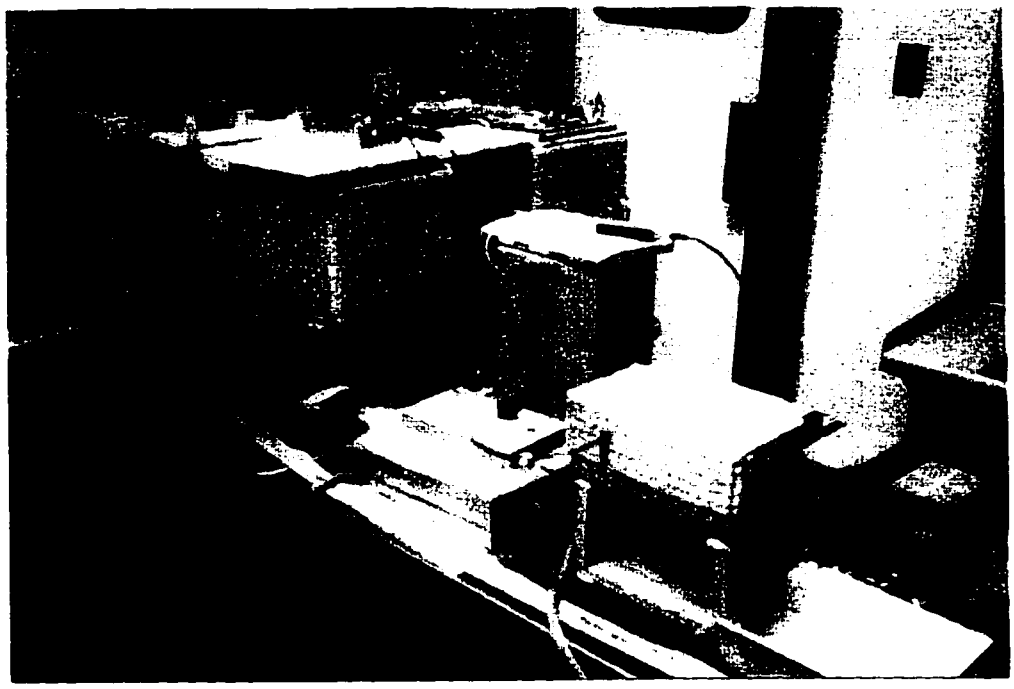


Figure 5.8: Running a correlation DSDR experiment in the lab.

brightness temperature component.

Consider the circuit for a 3-port Wilkinson power divider having a characteristic impedance Z_0. Ideally, the only thermal noise generator in the circuit is an impedance matching resistor $R_w = 2Z_0$ connected between the output ports [55], producing a mean-square voltage

$$\overline{v_w^2} = 4kT_0BR_w. \tag{5.9}$$

If it's assumed that all 3 ports are impedance matched to ideal, noiseless loads, the fields generated by v_w in the two legs of the divider will have odd symmetry. Therefore the circuit can be modeled using the equivalent odd-mode representation in Figure 5.9, which has zero potential along the axis of symmetry.

The equivalent noise temperature T_{EQ2} emitted out of port 2 can be found. The $\lambda/4$ transmission line, shorted to ground at the input side, will look like an open circuit at the output port. Therefore the power delivered to the port 2 load is determined by a resistive

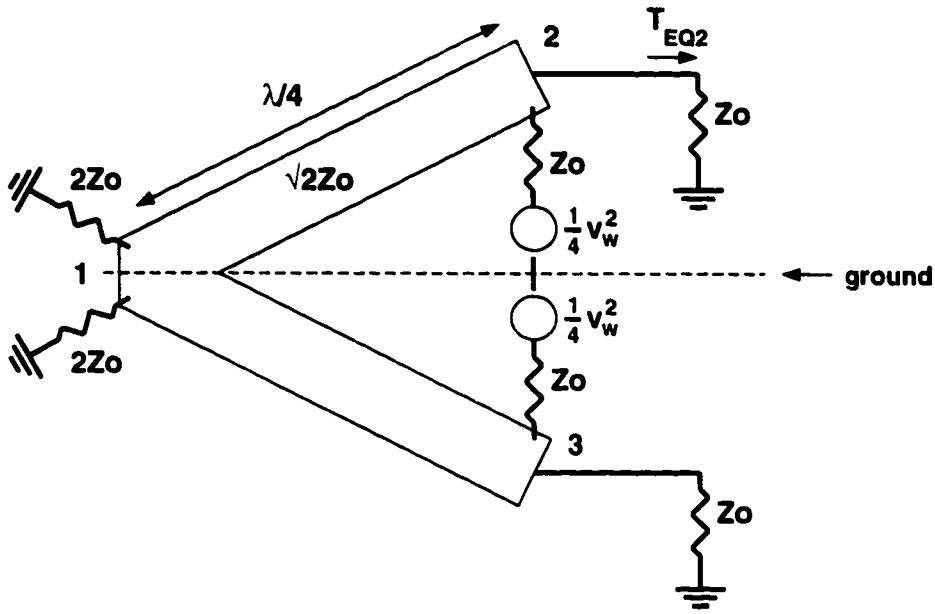


Figure 5.9: Model for anticorrelated noise in a Wilkinson power divider. The internal resistor connected between ports 2 and 3 generates thermal noise sources that are 180° out of phase.

divider,

$$P_2 = kT_{EQ2}B = \frac{1}{2}\left(\frac{\overline{v_w^2}/4}{2Z_0}\right), \tag{5.10}$$

implying an output noise temperature of

$$T_{EQ2} = \frac{\overline{v_w^2}}{16kBZ_0} = T_0/2. \tag{5.11}$$

Similarly, due to odd symmetry, port 3 will emit a noise temperature of equal magnitude but opposite phase ($\rho = -1$); correlating the two ports together yields a *negative* temperature of $-T_0/2$. For the correlation DSDR experiment, the effects of lossy cables are factored into (5.11) to solve for the remaining anticorrelated noise component,

$$T_{ANTI} = -T_0/2L_C. \tag{5.12}$$

Applying the results from (5.7), (5.8), and (5.12), the coefficient ρ can be written as the ratio of correlated power to total power:

$$\rho = \frac{T_{CORR} + T_{ANTI}}{|T_{CORR}| + |T_{ANTI}| + |T_{UC}|} = \left[1 + 2L_C\left(\frac{T'_{REC} + T_0}{T_{IN} - T_0}\right)\right]^{-1}. \tag{5.13}$$

A coaxial pad with attenuation $L_D = 5$ dB was inserted between the noise diode and power divider to keep the receivers from saturating and to improve the impedance match. The noise diode has an excess noise ratio (ENR) of 15.2 dB at 1.4 GHz. Therefore, at the ambient temperature $T_0 = 290$ K, the noise temperature following the attenuator is

$$T_{IN} = T_0 \left(\frac{ENR}{L_D} + 1 \right) = 3330 \text{ K}. \tag{5.14}$$

Given a receiver noise temperature of $T'_{REC} = 100$ K listed in Chapter 2 and a nominal cable loss of 0.8 dB, the peak correlation coefficient is expected to be

$$\rho = \left[1 + 2(1.20) \left(\frac{100 + 290 \text{ K}}{3330 - 290 \text{ K}} \right) \right]^{-1} = 76.5\%. \tag{5.15}$$

Correlation measurement

DSDR's "grating lobe" pattern was measured by sweeping the relative phase ϕ of the two receivers over 0–255°, using the microwave phase shifter. For this experiment, the correlator resolution was set to 3.3 bits. I confirmed beforehand that the hardware had powered up with both decimation circuits synchronized to prevent the DSDR roulette symptom from causing any unexpected losses. Once the sensors had stabilized, r_Q data were recorded on two separate passes to rule out any variations due to gain or offset drifts.

Figure 5.10 shows the data logged for r_{Q1}, r_{Q2}, and r_{Q12} as the phase is varied over approximately three-quarters of one RF cycle. The coinciding, sinusoidal patterns in both passes of r_{Q12} confirm DSDR's basic operation as a correlation receiver and show good repeatability in the measurements. From the top graph, the absolute magnitude of r_{Q12} has a peak value of 2.09 at $\phi \approx 170°$. The second graph indicates that measurement errors between the first and second r_{Q12} data sets do not exceed ± 0.025.

The bottom two graphs show some variation in total power detect outputs r_{Q1}, r_{Q2} over the course of the experiment. The 2% drop in the first r_{Q1} data set around $\phi = 0$–40° is characteristic of the sporadic shifts seen in DSDR1, yet it has little effect on the

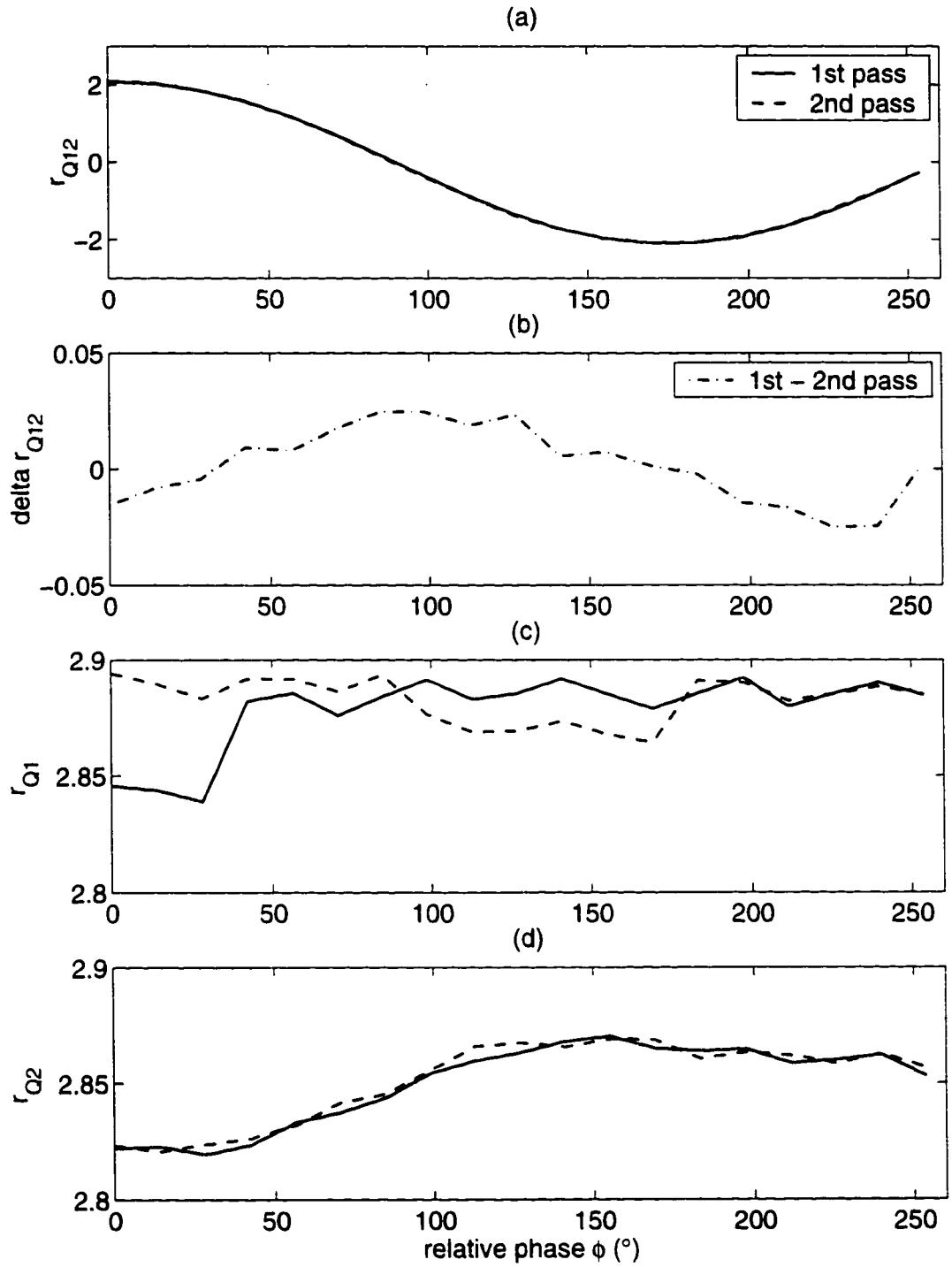


Figure 5.10: Measuring a partially correlated noise source with DSDR while the clock phase is varied between receivers: (a) grating lobe pattern generated by the cross-correlator, (b) cross-correlation measurement error, (c) DSDR1 total power detect output, (d) DSDR2 total power detect output. The measurements were performed twice to confirm repeatability. Phase stability can be assessed by looking at the peak strength of $|r_{Q12}|$ relative to the detect output signals r_{Q1} and r_{Q2}.

stability of the cross-correlator data. This suggests that the fluctuations in DSDR1 are caused by changes in receiver noise rather than gain—for instance, there may still be some RF crosstalk problem between the front end and neighboring circuitry. The r_{Q2} data show a reproducible change in detected power that varies periodically with the cross-correlation data. This is probably caused by leakage from the 160 MHz sampling clock to the RF input of channel 2: as DSDR2's sampling clock is shifted, the A2 converter detects either "hot" parts of the RF signal (where digital switching noise coincides with the sampling time) or "cold" parts of the signal (where the switching noise is in between samples). The measurement setup in the lab represents the most extreme case for this type of interference, though; in STAR, the phase of the sampling clock is fixed, and any detected offset arising from clock interference is removable through calibration.

Given a peak cross-correlation value of $|r_{Q12}| = 2.09$ and average detect output values $r_{Q1} = 2.88$ and $r_{Q2} = 2.85$, the empirical correlation coefficient can be found from (5.4):

$$\rho_{(meas)} = \frac{2.09}{\sqrt{(2.80)(2.77)}} = 75.1\%. \tag{5.16}$$

This result matches very well with the correlation coefficient anticipated in (5.15). (The 0.1 dB discrepancy is small enough that it could be attributed to errors in my estimates of the experiment parameters T_{IN}, T'_{REC}, L_C, and so on.) What this means for the correlation DSDR hardware is that it can maintain a high level of phase stability between the pair of distributed receivers and, consequentially, the sensor is capable of recovering visibility signal information with little or no loss. It also follows that there is little mismatch between the phase responses of each receiver, or at least if there is a difference, it is roughly linear with frequency in the passband. Otherwise, we could imagine that the peak correlation energies at different frequencies within the passband would not all line up at the same value of ϕ, and the net grating lobe pattern would have a smaller than ideal amplitude. The negligible loss in ρ also offers tangible proof of good phase matching between the cavity resonator

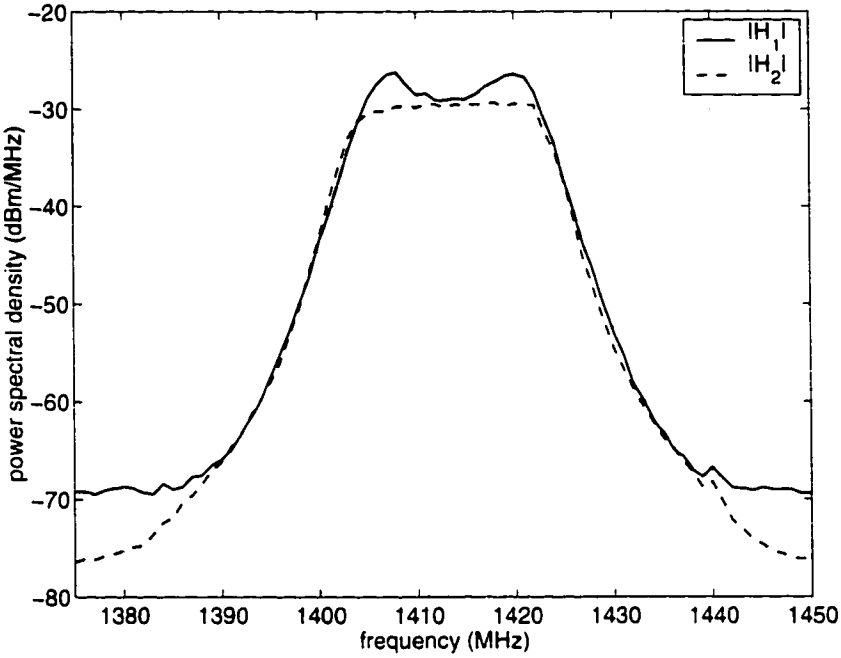


Figure 5.11: Magnitude of the frequency response for DSDR1 and DSDR2 front end receivers (before digitization).

filters in DSDR1 and DSDR2.

5.4.3 Fringe washing function

Recall from (3.58) that the fringe washing function is related to frequency responses H_1, H_2 of the two DSDR receivers through a Fourier transform. I estimated the magnitudes of these responses—at least in the analog domain—by redirecting the output signal from each front end to a spectrum analyzer while the noise diode and power divider were connected. The power spectral densities of the two analog output channels were measured over 1375–1450 MHz, as shown in Figure 5.11. Assuming a negligible phase imbalance between the channels, the fringe washing function r_w can be determined by transforming the product of the two magnitudes H_1 and H_2:

$$r_w(\tau) = e^{-j2\pi f_0 \tau} \int_{-\infty}^{+\infty} |H_1(f))|\,|H_2(f)|\, e^{j2\pi f \tau} df. \tag{5.17}$$

An end-to-end fringe washing measurement was also performed by taking advantage of

the DSDR roulette timing problem described in Section 5.1.4. The sampling delay time τ between receivers can take on approximately 16 unique settings, from -50 ns to $+50$ ns, with incremental shifts equal to the 6.25 ns period of the system clock. To measure the rolloff in ρ caused by fringe washing, the correlation experiment with the diode/divider network in Section 5.4.2 was repeated over a range of delay times, using 3.3 bit sampling resolution: for each data point, the hardware was power cycled to generate a rough jump in τ, then fine tuning was done with the phase shifter to determine the maximum correlation. These measurements are normalized to unity at $\tau = 0$ to trace out the shape of the autocorrelation function.

Figure 5.12 shows the fringe washing function results from the correlation DSDR experiments. The solid line is a plot of the expected (analog) response derived from (5.17). Notice that the curve closely resembles a sinc function with a correlation length of 50 ns—exactly what we would expect from receivers having a 20 MHz rectangular bandpass response. The end-to-end fringe washing measurements, which are plotted alongside the sinc curve, take on a distinct and unforeseen characteristic, though. Instead of having a gradual, tapered response as τ moves away from zero, there is a rather sharp, almost triangular-shaped dropoff in the strength of the correlation. (There is also an asymmetry in the data that suggests some phase imbalance between the DSDR channels.) The correlation time and system bandwidth technically have not changed: on average, the first zero-crossings of the fringe washing data still intersect near ± 50 ns. Yet the strange compression of τ_w observed in the time domain hints at the possibility that, in the frequency domain, the passband has been stretched beyond its original range. The next section will explore the link between this phenomenon and DSDR's digital receiver architecture.

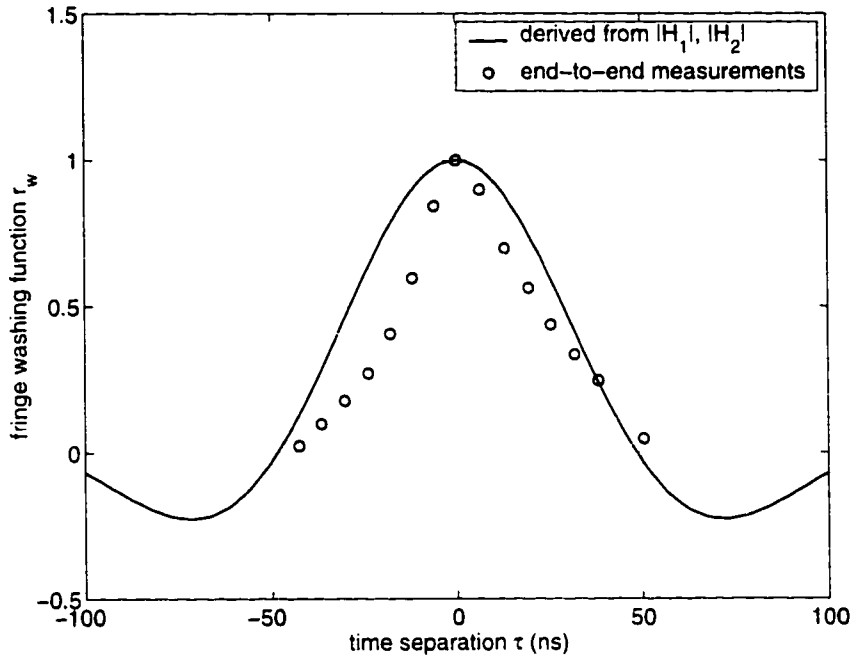


Figure 5.12: The correlation DSDR fringe washing function determined from (1) the analog frequency response of each receiver, (2) direct (end-to-end) measurements at 3.3 bit resolution. The discrepancy between the two cases points to an unexpected loss of coherence for a finite time separation τ between digital samplers.

5.5 Interpreting discrepancies in fringe washing

5.5.1 How quantization affects the autocorrelation and power spectrum of a signal

The distortion in fringe washing can be understood by looking back at the derivations in Chapter 2 which relate the analog correlation coefficient ρ to its digital counterpart, ρ_Q. Equation (2.55) described this transfer function for arbitrary bit resolution and for a signal bias of zero. (Recall that the relation was solved and plotted in Figure 2.6 using 2.2 bit resolution.) As it was noted earlier, the autocorrelation R_F of the quantized waveform can be found by plugging R_∞ into the ρ-ρ_Q transformation, since an autocorrelation function is just a special case of the correlation between two random processes.

The kink in the ρ-ρ_Q curve near unity in Figure 2.6 helps to explain the peculiar shape of DSDR's fringe washing function. If a smoothly varying function such as the ideal sinc

response,

$$r_{w(ideal)}(\tau) = \mathrm{sinc}B\tau, \tag{5.18}$$

is applied to the transformation, the distortion caused by the kink will generate a sharp, non-differentiable peak at $\tau = 0$. Furthermore, because the change in ρ_Q with respect to ρ is greatest for correlation values near 1, the rolloff in fringe washing will be most severe in the neighborhood of small τ. This also happens to correspond to the area immediately away from the boresight direction in aperture synthesis radiometry. Would the most important part of the radiometric image then suffer the most from blurred vision? Figure 5.13(a) shows the ideal fringe washing function described by (5.18), along with the transformed fringe washing functions for 1, 2, and 3 bit resolutions. As the bit resolution decreases, the loss of coherence from $\tau = 0$ to $1/B$ becomes worse, and the shape of the predicted fringe washing function begins to resemble the curve measured with DSDR.

The non-linear nature of the quantization process causes some signal energy to be displaced out of the principal passband B. The power spectral densities of the quantized signals are found by applying a Fourier transform to each autocorrelation function (see Figure 5.13(b)). As quantization resolution is decreased, more energy is transferred out of the main passband (shown from 0 to 10 MHz) and spread over a broad range of frequencies. It is this *bandwidth spreading* phenomenon that is ultimately responsible for degrading the coherence between the two DSDR channels. Although the physics behind this result is not surprising, it has important ramifications for digital STAR, which must be able to maintain signal coherence over a wide field of view.

5.5.2 Implications for STAR correlators having coarse resolution

Because fringe washing depends on the bandpass spectrum but not on the center frequency f_0, the analysis presented for the L-band DSDR is just as relevant for similar radiometer systems that mix down to an intermediate frequency before digitization. The

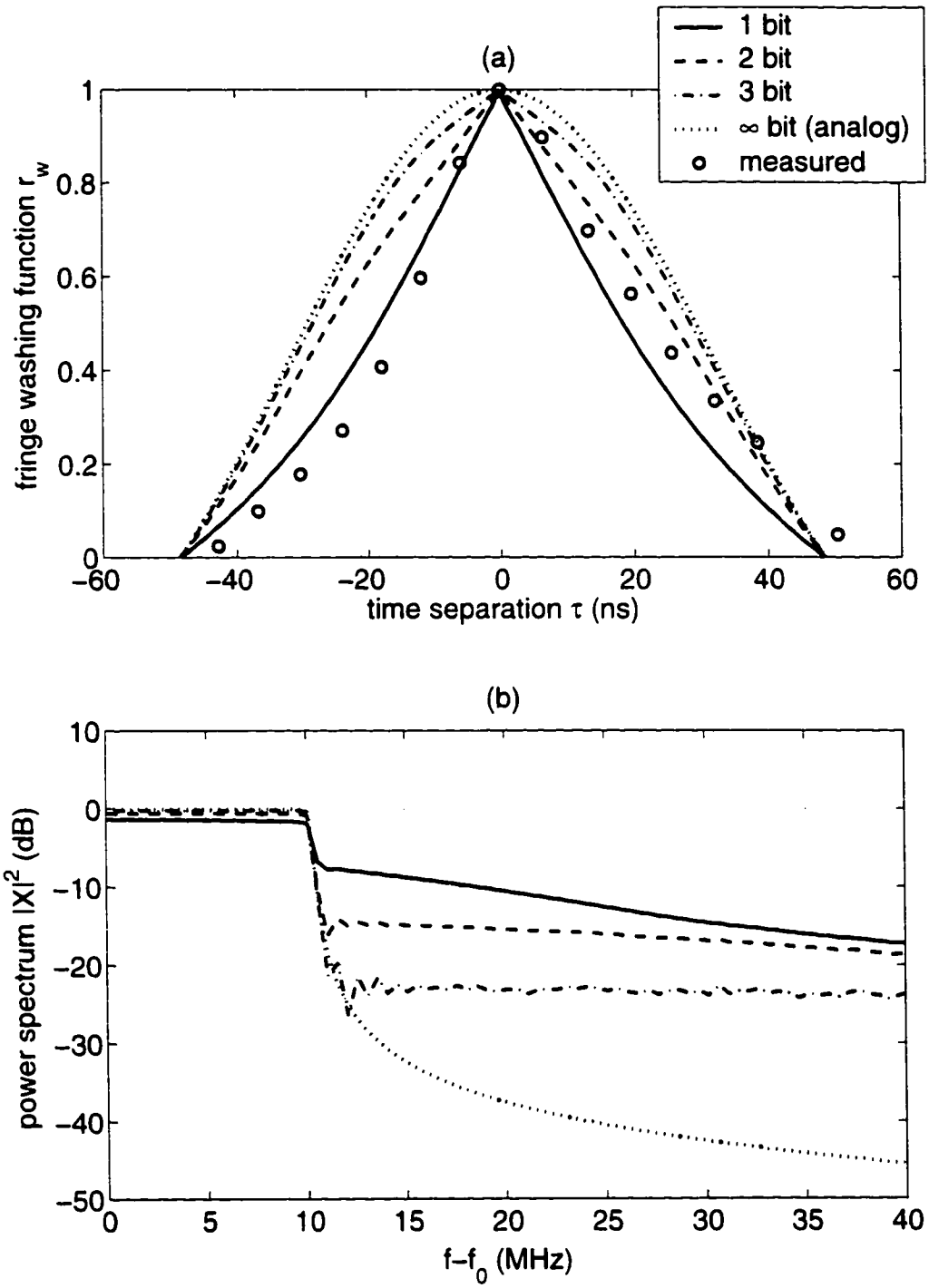


Figure 5.13: (a) Fringe washing modeled over a range of bit resolutions. Experimental data from Figure 5.12 are included for comparison. (b) The corresponding power spectral densities of the quantized waveforms. At coarse resolution, non-linearities in the A/D conversion cause the spectrum to be spread over a range of frequencies (*bandwidth spreading*).

most noteworthy example is the L-band SMOS aperture synthesis array, discussed in Chapter 1. SMOS relies on a 1-bit IF sampling scheme to minimize design complexity in the A/D converter and digital correlator sections. But 1-bit quantization is also the coarsest possible resolution and, as seen in the previous section, the most severe in terms of coherence loss.

Experimentation with DSDR is significant in that it represents the first end-to-end characterization of fringe washing in a *digital* L-band correlation radiometer. Some fringe washing studies have been performed previously for demonstration instruments related to the SMOS project, like the 36 element, 1-bit correlation STAR sensor being developed by the Helsinki University of Technology [56]. However, these investigations have been limited to determining fringe washing in the analog domain only, using the measured amplitude and phase response of IF surface acoustic wave filters.

Recognizing that the bandwidth spreading problem may impact the performance of SMOS, it is useful to look at how a fixed 1-bit correlation radiometer will further alter the fringe washing function. This type of receiver uses a simple 2-level comparator (signed operator) to convert from the analog to digital domain:

$$\hat{x} = \begin{cases} +1/2 & \text{if } x \geq 0 \\ -1/2 & \text{if } x < 0 \end{cases} . \tag{5.19}$$

For this special case, there exists a closed form solution for ρ_Q known as the Van Vleck relationship [75]:

$$\rho_Q = \frac{2}{\pi} \sin^{-1} \rho. \tag{5.20}$$

By setting ρ equal to the ideal fringe washing function in (5.18), the corresponding fringe washing pattern of the digital correlator, $r_{w(1bit)}$, can be found. The relative change in gain between ideal and quantized cases defines the *excess coherence loss*,

$$\text{excess } CL = \frac{r_{w(ideal)}}{r_{w(1bit)}} = \frac{\pi}{2} \cdot \frac{\text{sinc} B\tau}{\sin^{-1}(\text{sinc} B\tau)}. \tag{5.21}$$

The above relation is plotted in Figure 5.14 for a correlation radiometer with 20 MHz bandwidth.

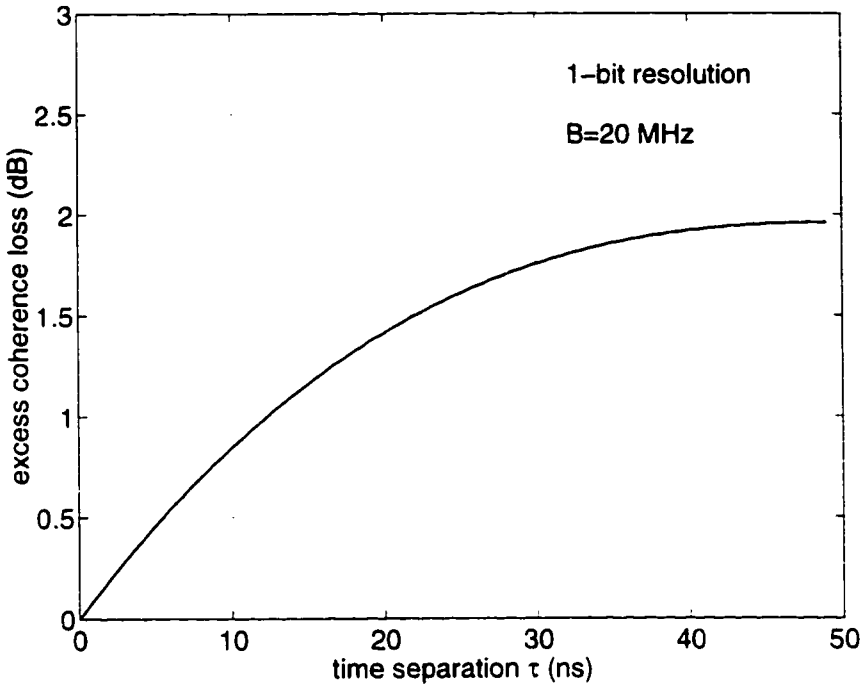


Figure 5.14: Excess coherence loss in the fringe washing function. The vertical axis represents the loss incurred by going from an ideal analog correlation radiometer to a 1-bit digital correlator, where the system bandwidth equals 20 MHz for both cases.

To quantify the loss in (5.21), consider a hypothetical 1-bit STAR radiometer that has a maximum baseline of 10 m—comparable in size to SMOS. As the synthesized beam is steered 35° away from boresight, the lag time between the outermost receivers stretches to 19 ns. From Figure 5.14, this delay translates into an extra 1.4 dB loss in visibility information *in addition to* the 1.1 dB loss already incurred through $r_{w(ideal)}$. This level of degradation does not necessarily forbid the implementation of 1-bit correlators for remote sensing STAR. But it does point out that if the effects of bandwidth spreading are not thoroughly modeled, the visibility signal-to-noise ratio at higher spatial frequencies may be worse than expected. It would be worthwhile to explore whether the quantization resolution should be increased beyond 1 bit, or whether alternative techniques such as the band-slicing algorithm from Section 3.3 should be employed, to lessen the impact of excess coherence loss.

5.5.3 Other sources of nonlinearity in DSDR

Bandwidth spreading can account for some of the characteristics in the correlation DSDR's fringe washing function, yet discrepancies remain between the measured data and the modeled responses in Figure 5.13(a). The data, taken at 3.3 bit resolution, actually seem to fit more closely with the curves drawn at 1 or 2 bit resolutions. There may be limitations in the receiver statistics theory due to other sources of nonlinearity and interference in the actual hardware.

One practical problem is that the direct-sampling A/D converter does not have a perfect staircase transfer function with an equal step size for each LSB. Differential nonlinearity can introduce additional distortion in the digital output waveform which might exacerbate bandwidth spreading (see Figure 5.15) [22]. The SPT7610's differential linearity, specified at ± 0.5 LSB, is not negligible on the scale of the coarse quantization ranges used to test DSDR, and may need to be considered in the autocorrelation models.

Assuming that there is a noticeable mismatch between quantization transfer schemes in DSDR1 and DSDR2, how would this complicate the phase relationship between the H_1 and H_2 transfer functions? Any imbalance in phase could cause asymmetry in fringe washing, as was observed in the correlation DSDR measurements.

My receiver statistics models may also be limited by deterministic interference coming from clocks and digital switching noise. It was assumed that the input signal entering the A/D sampler is a perfectly Gaussian distributed random variable. However, the discovery of additive noise sources in DSDR1 (Section 4.6.4) and coherent detection in DSDR2 (Section 5.4.2) suggest otherwise. How would the altered shape of the analog input distribution change the statistical properties of DSDR? A future goal is to implement a high speed analyzer that can record the digital data stream in real time, to pick out interfering signals and to measure the true probability density function.

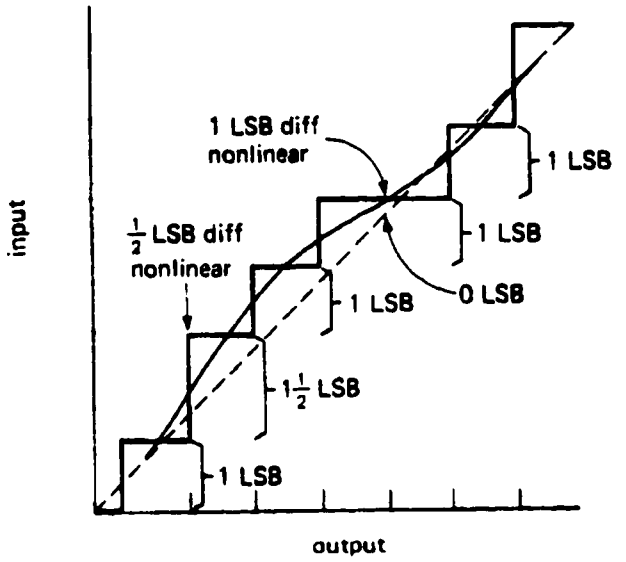


Figure 5.15: Illustration of differential nonlinearity effects in an A/D converter (adapted from P. Horowitz and W. Hill, 1989) [22].

The unexpected behavior in fringe washing underscores the importance of thoroughly investigating the end-to-end performance of upcoming radiometry missions such as SMOS. It is also recommended that future studies should examine DSDR's sensitivity to some of the non-ideal aspects of digital detection.

CHAPTER 6

Conclusions

"If you haven't found something strange during the day it hasn't been much of a day."

—*John A. Wheeler*

6.1 Contributions and Findings

Investigations of the direct-sampling concept have led to the following new developments: (1) the derivation of general noise-equivalent sensitivity expressions for self-correlation and cross-correlation DSDR radiometers in terms of arbitrary bit resolution, subharmonic sampling rate, and response to signal bias; (2) modeling the effects of phase noise sources in a correlation DSDR, and creating techniques to reduce the impact on sensitivity and spatial resolution performance in aperture synthesis radiometry; and (3) design, fabrication, and characterization of the first operational L-band correlation DSDR radiometer.

Direct-sampling traces its origins back to research activities in radio astronomy, Earth remote sensing, and communications. By combining techniques from these disciplines, a novel receiver architecture has been developed which will ease the implementation of advanced, high spatial resolution radiometry missions at L-band frequencies.

Overview

DSDR operates at a level of radiometric sensitivity and phase stability that is suitable for L-band Earth remote sensing applications. With the bulk of the signal processing contained in digital circuitry, direct RF sampling would naturally lead toward a simplified,

flexible receiver-on-a-chip for STAR. An optimum balance between circuit complexity and acceptable noise level was achieved with 2–3 bits of quantization resolution. Within this range, the need for analog detection circuitry at lower bit resolutions could be avoided, as could the expense of increased complexity in the digital correlator at higher resolutions. Through a series of tests, it was demonstrated that the technology for wideband A/D converters presently available on the market will permit accurate and stable detection of signal power and phase at 1.4 GHz. A central conclusion is that, using DSDR technology, the system noise temperature T_{SYS} and correlation coefficient ρ can be recovered without having to rely on analog detection circuitry. This is a departure from the hybrid analog/digital detection scheme used in SMOS and similar airborne demonstration missions.

Hardware operation

The L-band A/D converter operated with a sufficient analog input bandwidth and dynamic range for total power detection of natural brightness targets (T_{SYS} = 50–400 K). For the two-channel correlation DSDR, coherence tests verified the basic operation of the sensor and demonstrated that reliable and repeatable cross-correlation measurements could be made near 1.4 GHz. Further experiments with DSDR reinforced that the direct-sampling method is suitable for either total power or correlation radiometer configurations.

Radiometric sensitivity

Receiver statistics models were developed for both total power and correlation DSDRs to quantify the noise-equivalent sensitivity. It was inferred from this analysis that: (1) beyond 2 bits of quantization, the output signal for either radiometer becomes insensitive to changes in analog input bias, relative to the thresholds of the sampler. (2) Using a 3 bit correlator, NEΔT approaches within $\sim$ 4% of the sensitivity figure for an ideal analog radiometer; there is a minimal improvement beyond 3 bit resolution because DSDR rapidly converges to the ideal sensitivity. (3) A limited amount of sensitivity degradation arises

from subharmonic sampling of the RF input signal, due to the interdependence between voltage samples taken over the integration period; for typical L-band applications where the Nyquist sampling rate is near 40 MHz, this degradation will translate into $\sim 20\%$ loss in NEΔT compared to the case of continuous-time detection.

Receiver statistics models were validated through lab and field experiments using the prototype DSDR hardware. Empirical NEΔT of the stand-alone total power DSDR and the two-channel correlation DSDR were predicted to within worst case errors of 0.7 dB and 0.4 dB, respectively, using 2 or more bits of sampling resolution; in many instances, the agreement between experiment and theory was much closer. By studying the noise floor performance for two special correlation conditions, $\rho = 1$ and $\rho \ll 1$, the upper and lower sensitivity bounds of a correlation DSDR could be identified and assessed for STAR applications.

Phase stability and fringe washing

With both channels of the correlation DSDR synchronized, the sensor could recover the correlated power component between a pair of injected signals with less than 0.1 dB loss. This implies a high level of phase stability between the two distributed sampling circuits in DSDR1 and DSDR2.

However, an unexpected loss of coherence was discovered in the fringe washing measurements when a variable lag time was introduced between the samplers. The fringe washing function suffered an excess coherence loss caused by bandwidth spreading—that is, a broadening of the power spectrum when the signal is quantized. And as bit resolution decreased, fringe washing degradation became worse.

The DSDR coherence loss results are especially significant for upcoming aperture synthesis missions because: (1) these data represent the first end-to-end fringe washing measurements to be documented for an L-band digital correlation radiometer; and (2) the

band spreading mechanism identified here would equally affect the performance of an IF-sampling digital receiver, like the one proposed for the European Space Agency's SMOS mission. Without properly modeling the effects of bandwidth spreading, there will be an unanticipated loss of sensitivity over the field of view. This problem may be alleviated either by increasing the quantization resolution, or by implementing a new band-division correlator concept developed in this thesis.

Systems design

There were a host of design and production problems encountered in the first DSDR instrument which caused an unacceptable level of noise in the detect output. With essentially all of the receiver gain at RF frequencies, it was particularly important to filter undesired noise sources (both radiated and conducted), to eliminate switched-mode circuitry for power and temperature regulation, and to isolate ground paths between the sensitive analog front end and the noisier digital electronics. After a number of design changes were made to the second DSDR receiver, the radiometer showed a marked improvement in stability. It was later proven that the modified correlation DSDR system could achieve a level of sensitivity near the fundamental noise limit.

6.2 Future Work

Receiver statistics limitations

The models developed for DSDR do not consider some practical effects that may arise in the actual A/D sampler. For instance, the transfer function for a practical A/D converter will have an uneven step size (differential nonlinearity) between quantization thresholds; this changes the probability distribution of the sampled data and further distorts the input signal. (The additional distortion and band spreading of the quantized waveform may in fact explain the remaining discrepancies between the predicted and measured fringe washing curves for DSDR.) Also, interference from other sections of the circuitry, especially due to

digital switching, can inject periodic noise pulses in front of the A/D converter. Thus the statistical properties of the digitized data are not necessarily stationary over time.

Insight could be gained by designing a data recorder with some amount of memory depth into the next version of the digital correlator. This way, DSDR could capture the true time-varying behavior of the digitized samples to see how the signal properties deviate from the ideal assumption of a stationary, Gaussian random process. Further analyses might look at how the actual response of the digital signal affects phase imbalance between receivers, bandwidth spreading, and fringe washing.

Improving phase coherence

Very coarse quantization in STAR—for instance, the 1-bit correlation scheme in SMOS—causes an excess loss in sensitivity over the field of view. What is the most efficient method for overcoming this problem in an operational instrument? One obvious solution would be to use more bits in the A/D converter and digital correlator, although this would tend to reduce the analog input bandwidth of the sampler and thus drive us further away from the goal of direct RF sampling. Another way is to keep the simple 1-bit converter, and instead implement a band-division correlation processor *after* digitization, where the added circuit complexity is more affordable. Band-slicing has the effect of reducing the radiometer's time-bandwidth product—the argument that determines the rolloff rate in the fringe washing function. By "stretching" this curve in the time domain, excess losses can be ameliorated. The band division correlator modeled in this thesis for the case of continuous (analog) detection could be extended to the digital case to quantify the improvement in fringe washing.

Multiple element arrays

The hardware developed for this dissertation included two DSDR receiver elements with one real (in-phase) digital correlator. To fully test the imaging capabilities of STAR, the

direct-sampling technique needs to be integrated into a multiple-element array with complex (in-phase and quadrature) correlators for each pair of receivers.

Over the next three years, the Microwave Geophysics Group will manage the design of a 10-element, two-dimensional STAR instrument at 1.4 GHz that uses the direct-sampling receiver architecture. This new sensor, named STAR-Light, will be deployed onto a light aircraft for arctic land surface hydrology studies and for validation of direct-sampling in aperture synthesis radiometry.

Digital processing techniques can be used to detect complex visibility samples without the need for a separate, phase-shifted clock and A/D converter. For instance, a Hilbert transform can be applied to one channel of the correlator to introduce a 90° phase shift [57]. In another method, the analog input signal is bandpass sampled above the Nyquist rate, and the I/Q signal components are recovered in the digital domain by separately processing even and odd samples [20]. These methods will be evaluated for the STAR-Light project.

Monolithic integration

The DSDR prototype was designed at a systems level to prove the direct-sampling concept. But to make this technology practical for spaceborne missions, the receiver eventually needs to be integrated onto a single chip. Within the next few years, the prognosis for monolithic integration looks encouraging.

Compound semiconductor technology like SiGe could greatly enhance carrier mobility, reduce the noise figure in integrated amplifier stages, and allow mixed analog and digital circuit integration [17]. For silicon CMOS technology, device cutoff frequencies continue to rise as fabrication processes shrink to submicron scales, making microwave applications all the more practical [7].

Low power, integrated A/D converter devices are also emerging as solid-state processes scale down in size. Recently, researchers have fabricated a 6-bit CMOS converter having an

analog input bandwidth of 600 MHz and a power consumption of 500 mW [4]—significantly less than the typical 3 W rating attainable with silicon bipolar technology. Because DSDR only requires 3 bits of quantization, a CMOS converter is conceivable with even lower power consumption and wider input bandwidth.

Perhaps the biggest obstacle limiting the integration of the L-band DSDR receiver is the large package size of the narrowband filter required over 1400–1427 MHz. Filter order and size could be diminished somewhat by oversampling the analog input signal and performing more of the passband filtering operation in the digital domain. Alternatively, new microelectromechanical systems (MEMS) filters could be employed before A/D conversion. Recent advances in MEMS technology may soon lead to a revolutionary, high-Q microwave filter integrated onto silicon: Nguyen has demonstrated a 160 MHz polysilicon MEMS filter with a quality factor of 9,400 [9]; it is thought that gigahertz range filters should be feasible in several years for development of an integrated receiver-on-a-chip.

Other frequencies and operating modes

Direct-sampling becomes an increasingly attractive solution for radiometry at higher microwave frequencies, beyond 1.4 GHz, as the input bandwidth and sampling rate of A/D converters continue to improve. Piepmeier has recently demonstrated a C-band direct-sampling receiver test bed which can digitize a 6.8 GHz carrier signal at a resolution of 2.8 bits (7 levels) [53].

Given DSDR's phase stability and its potential for higher frequency operation, other burgeoning areas in Earth remote sensing such as polarimetric radiometry would benefit from this architecture. Upcoming missions for the retrieval of ocean wind speed and direction need to accurately measure the third and fourth Stokes parameters over a range of frequency bands, from 6.8 to 37 GHz [54, 68, 69]. Direct-sampling technology for aperture synthesis is readily transferred to polarimetry; the only difference is that in the latter, the

cross-correlation is taken between co-located, horizontally and vertically polarized elements.

Where does DSDR technology ultimately lead? The philosophy of "going digital" as soon as possible after the antenna is a paradigm shift away from the complexity and inflexibility of conventional microwave hardware, toward a *software radiometer* that can be reconfigured to operate in a number of modes. With sufficient processing power, a future instrument may be able to instantly alter its frequency band, or switch between interferometry, polarimetry, or spectroscopy, just by changing software.

APPENDICES

APPENDIX A

List of Acronyms and Abbreviations

1dH/R One-Dimensional Hydrology/Radiobrightness Model

AHDL Altera Hardware Description Language

BDC band division correlation

CL coherence loss

digcorr digital correlator design file for the FPGA

DSDR Direct RF Sampling Digital Radiometer

ECL emitter-coupled logic

ENOB effective number of bits

ENR excess noise ratio

ESA European Space Agency

ESTAR Electronically Steered Thinned Array Radiometer

FOV field of view

FPGA field programmable gate array

GCM General Circulation Model

GPS Global Positioning System

HPBW half-power beamwidth

IRIS Inflatable Radiometer Imaging System

JTAG protocol standard for FPGA configuration

LSB least significant bit

LUT look-up table

MBE main beam efficiency

MEMS microelectromechanical systems

MGP Microwave Geophysics Group

MMIC monolithic microwave integrated circuit

MSI medium-scale integration

NEΔT noise-equivalent sensitivity

OSIRIS Ocean Salinity Soil Moisture Integrated Radiometer Radar Imaging System

PID proportional-integral-differential [feedback algorithm]

PSF point spread function

REBEX Radiobrightness and Energy Balance Experiment

RFI radio frequency interference

RTC real time clock

RTK Real Time Kernel for SmartCore microcontroller

SINAD signal-to-noise and distortion

SLL sidelobe level

SMOS Soil Moisture and Ocean Salinity [Radiometer]

SPT Signal Processing Technologies, Inc.

SSM/I Special Sensor Microwave/Imager

SSR solid-state relay

STAR synthetic thinned array radiometry

TEC thermoelectric cooler

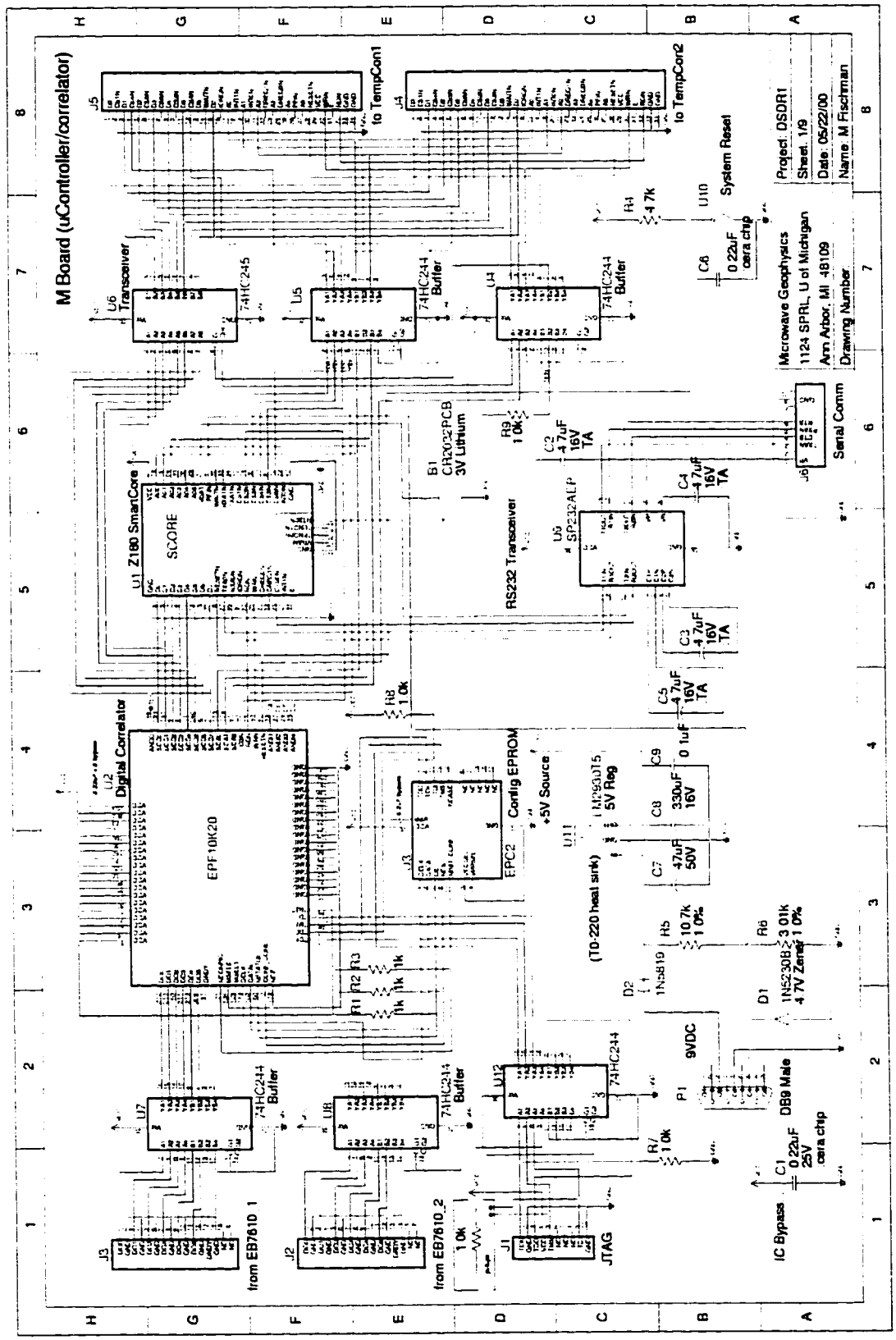
TempCon DSDR temperature control bus

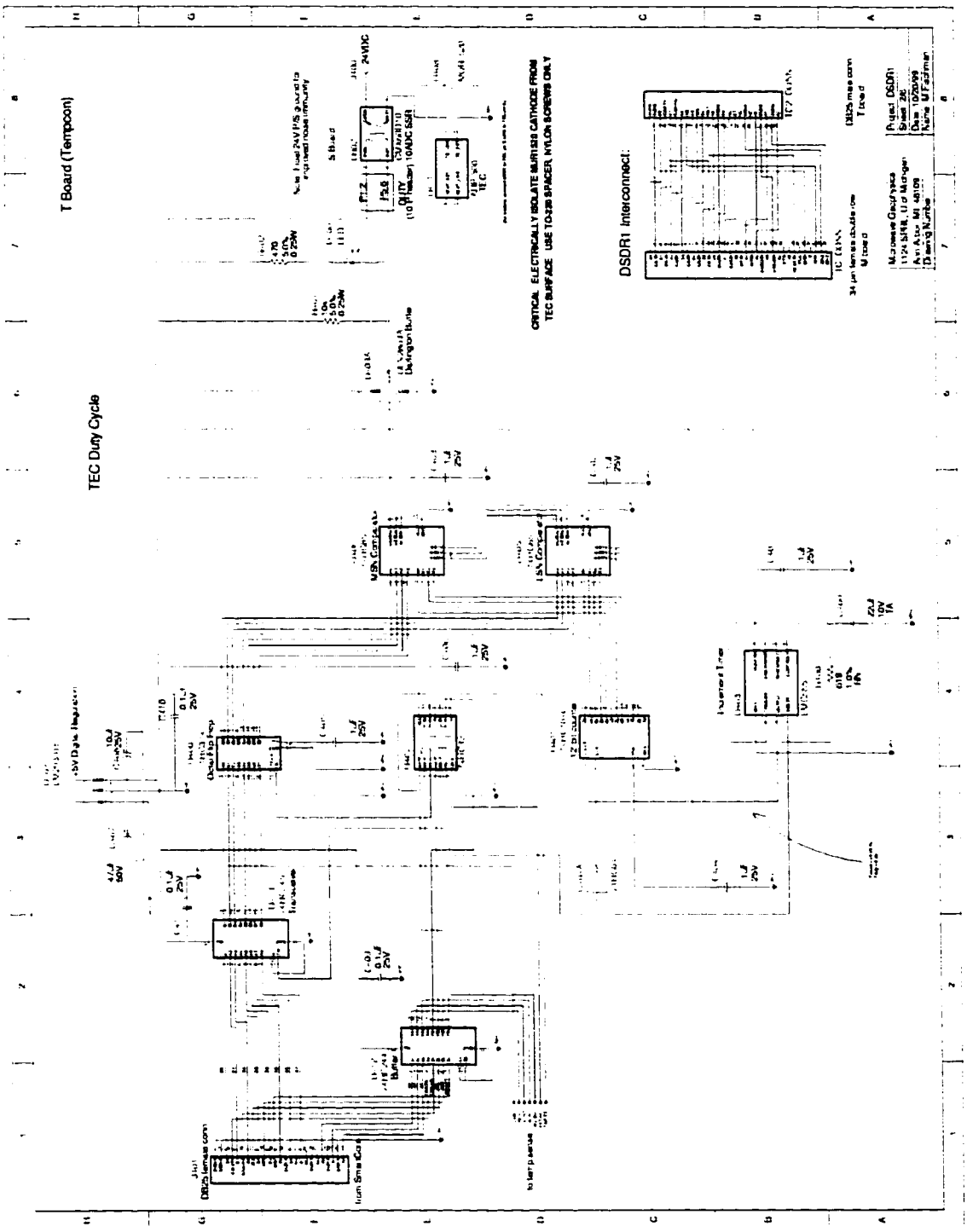
TMRS Truck Mounted Radiometer System

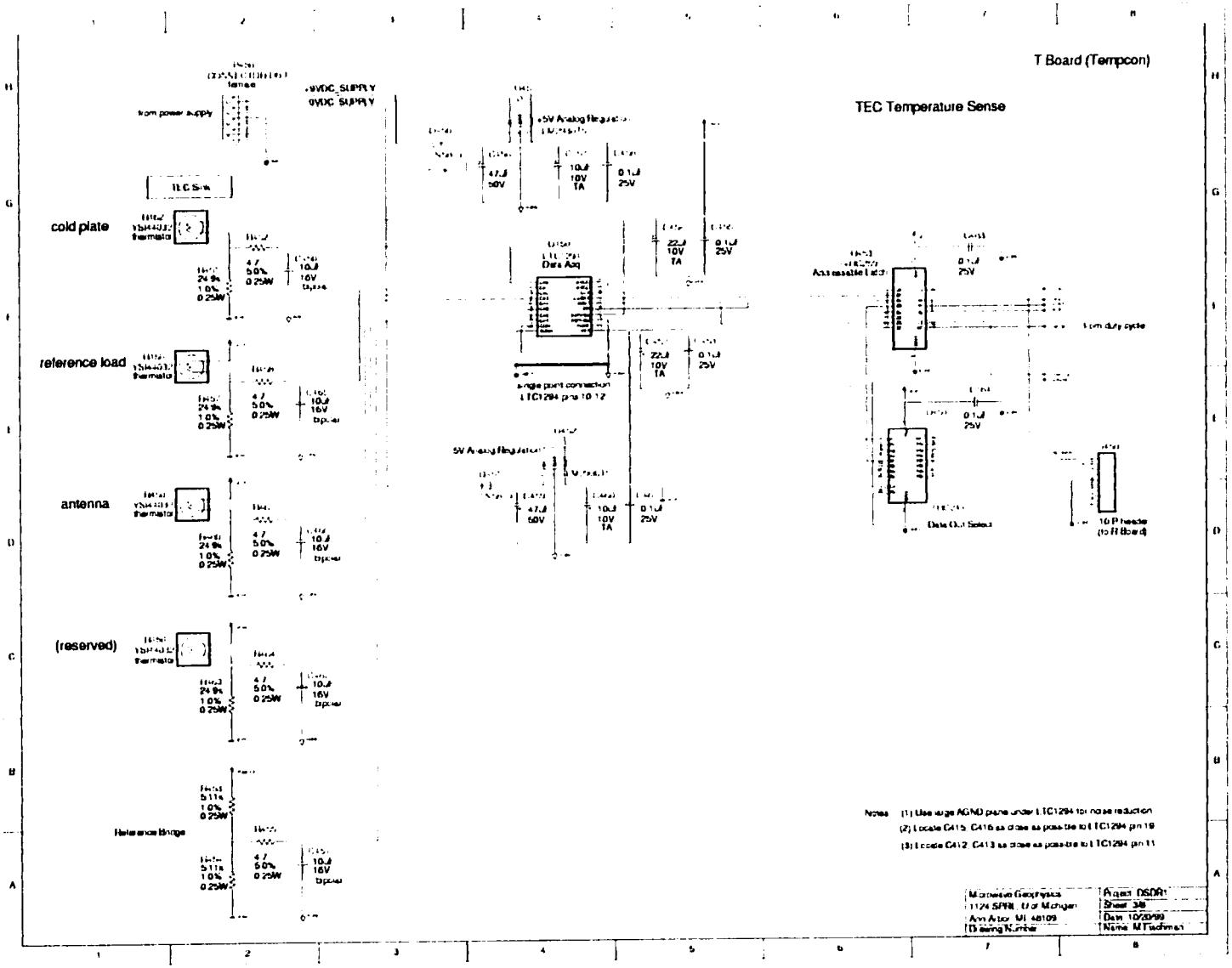
VLA Very Large Array

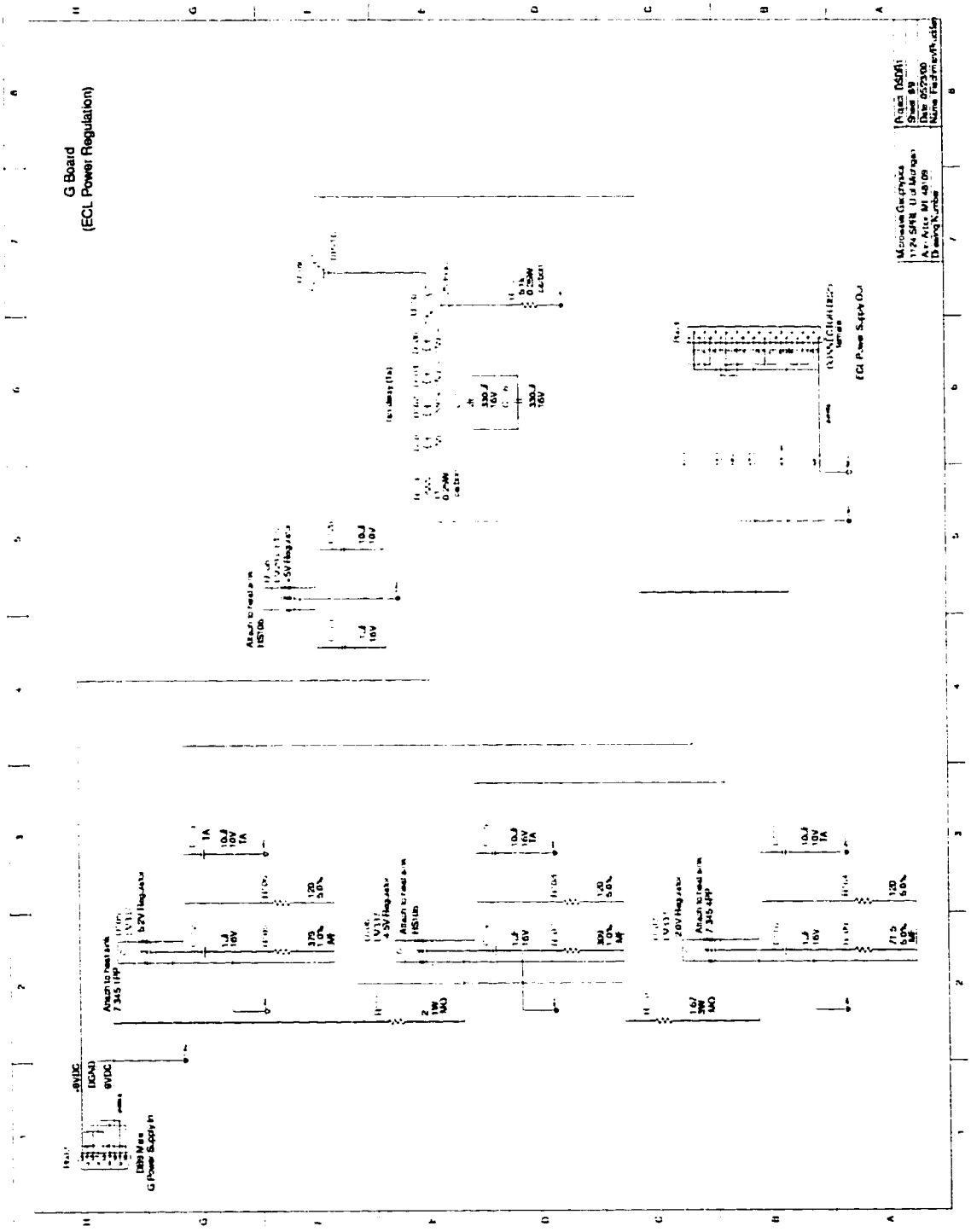
APPENDIX B

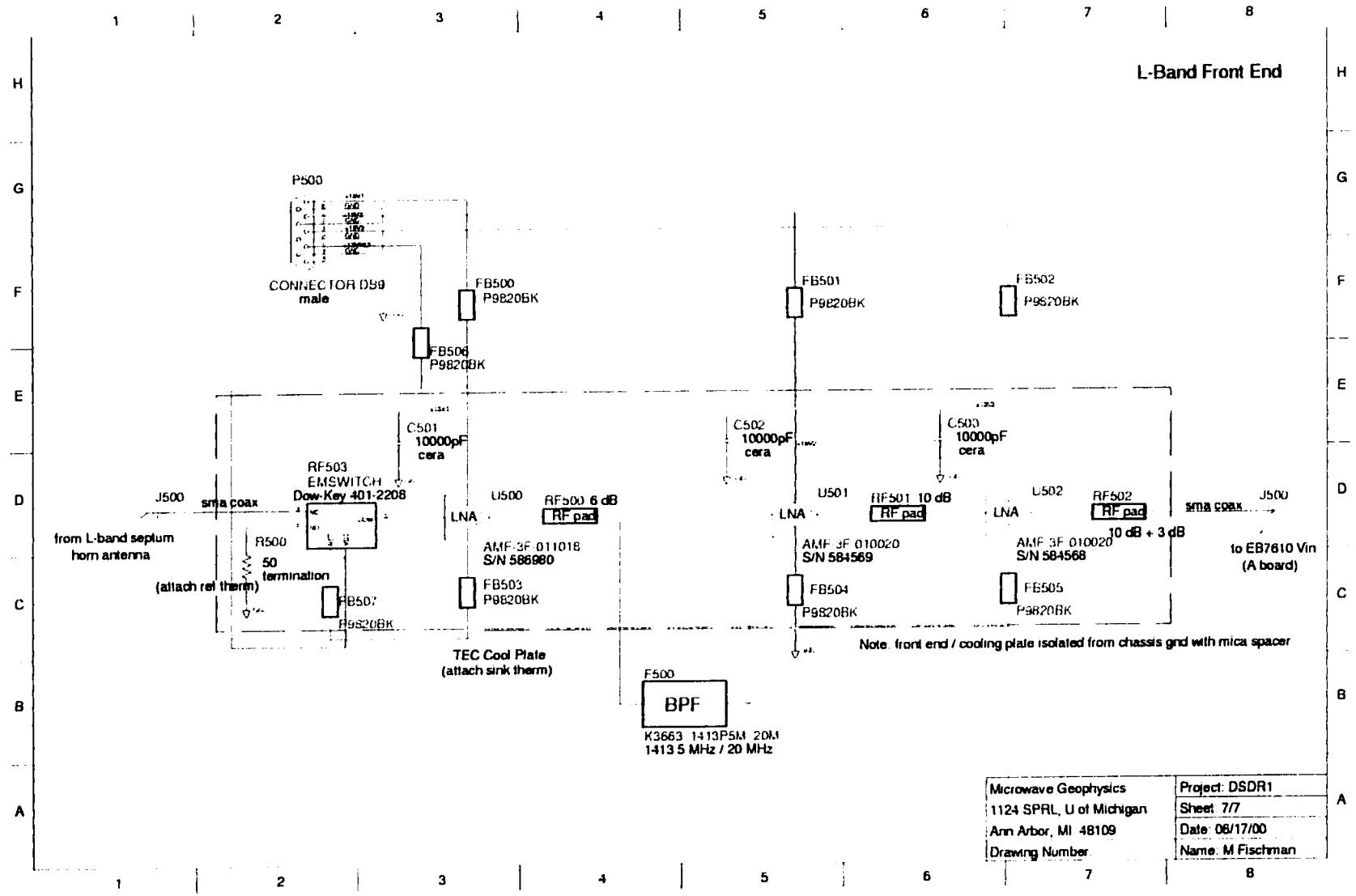
DSDR Receiver 1 (DSDR1) Schematics

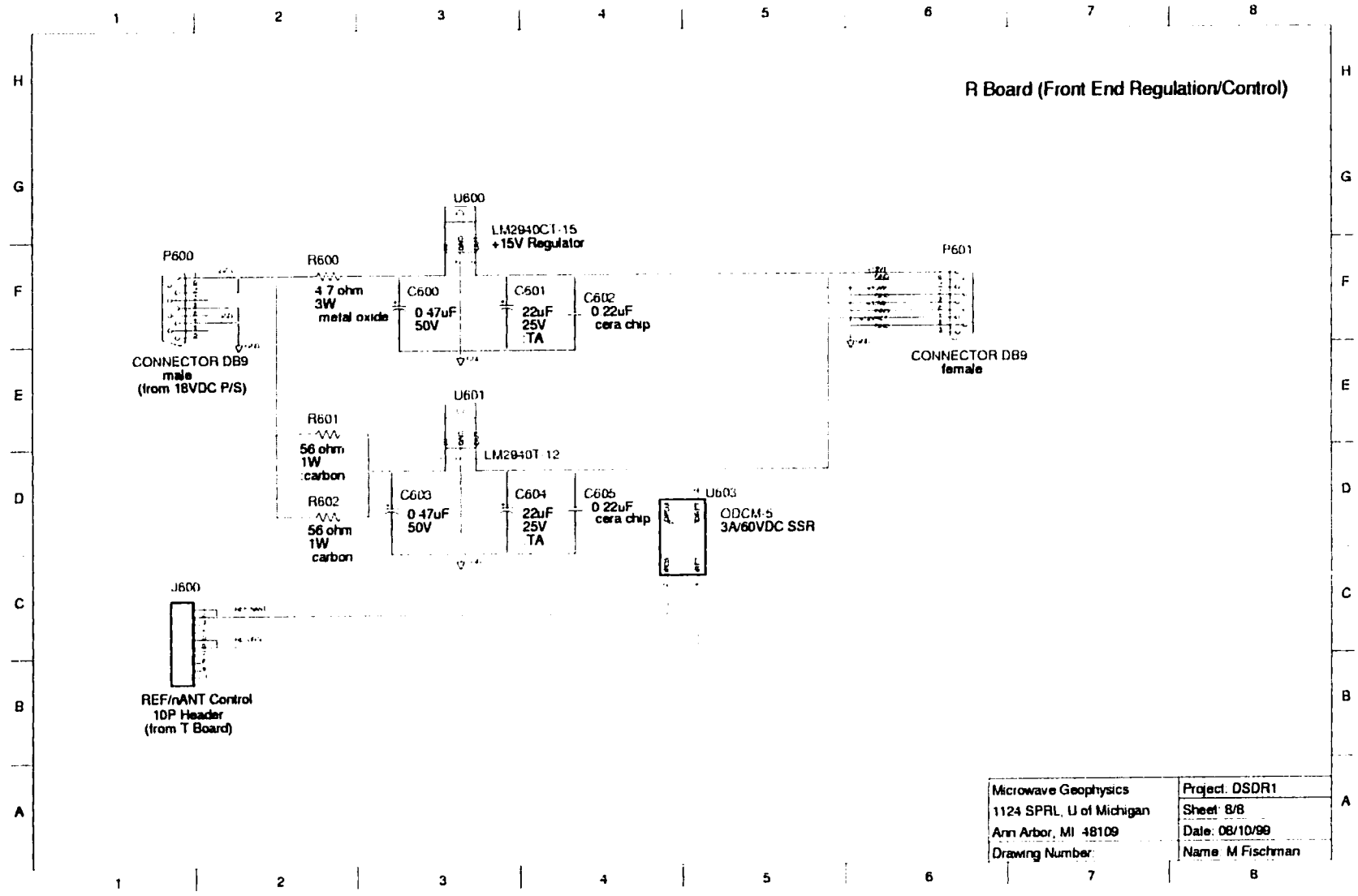

M Board (uController/correlator)
U1 Z180 SmartCore
SCORE
U2 Digital Correlator
EPF10K20
U3 Config EPROM
EPC2
U4 74HC244 Buffer
U5 74HC244 Buffer
U6 Transceiver
74HC245
U7 74HC244 Buffer
U8 74HC244 Buffer
U9 SP232ALP
RS232 Transceiver
U10 System Reset
U11 LM2937IT5 5V Reg
(TO-220 heat sink)
U12 74HC244
B1 CR2032PCB 3V Lithium
J1 JTAG
J2 from EB7610_2
J3 from EB7610_1
J4 to TempCon2
J5 to TempCon1
J6 Serial Comm
P1 9VDC
D1 1N5230B 4.7V Zener
D2 1N5819
R1 1k
R2 1k
R3 1k
R4 4.7k
R5 10.7k 1.0%
R6 3.01k 1.0%
R7 10k
R8 10.0k
R9 10k
C1 0.22uF 25V cera chip
C2 4.7uF 16V TA
C3 4.7uF 16V TA
C4 4.7uF 16V TA
C5 4.7uF 16V TA
C6 0.22uF cera chip
C7 47uF 50V
C8 330uF 16V
C9 0.1uF
IC Bypass
DB9 Male
Project: DSDR1
Sheet: 1/9
Date: 05/22/00
Name: M Fischman
Drawing Number
Microwave Geophysics
1124 SPRL, U of Michigan
Ann Arbor, MI 48109


T Board (Tempcon)
TEC Duty Cycle
DSDR1 Interconnect


T Board (Tempcon)
TEC Temperature Sense
cold plate
reference load
antenna
(reserved)
Reference Bridge
+9VDC_SUPPLY
9VDC_SUPPLY
from power supply
+5V Analog Regulator
LTC1294
Data Acq
single point connection
LTC1294 pins 10,12
5V Analog Regulator
Assessable Latch
from duty cycle
Data Out Select
10 P header
(to R Board)
Notes (1) Use large AGND plane under LTC1294 for noise reduction
(2) Locate C415, C416 as close as possible to LTC1294 pin 19
(3) Locate C412, C413 as close as possible to LTC1294 pin 11
Michigan Geophysics
1174 SPRL, U of Michigan
Ann Arbor, MI 48109
Drawing Number
Project DSDR1
Sheet 3/8
Date 10/20/99
Name MTechmeier


G Board
(ECL Power Regulation)


L-Band Front End
P500
CONNECTOR DB9
male
FB500
P9820BK
FB506
P9820BK
C501
10000pF
cera
RF503
EMSWITCH
Dow-Key 401-2208
J500
sma coax
from L-band septum
horn antenna
R500
50
termination
(attach ref therm)
FB507
P9820BK
LNA
U500
RF500 6 dB
RF pad
AMF-3F-011018
S/N 586980
FB503
P9820BK
TEC Cool Plate
(attach sink therm)
F500
BPF
K3663-1413P5M-20M
1413.5 MHz / 20 MHz
FB501
P9820BK
C502
10000pF
cera
C503
10000pF
cera
U501
RF501 10 dB
RF pad
LNA
AMF-3F-010020
S/N 584569
FB504
P9820BK
FB502
P9820BK
U502
RF502
RF pad
10 dB + 3 dB
LNA
AMF-3F-010020
S/N 584568
FB505
P9820BK
sma coax
J500
to EB7610 Vin
(A board)
Note: front end / cooling plate isolated from chassis gnd with mica spacer
Microwave Geophysics
1124 SPRL, U of Michigan
Ann Arbor, MI 48109
Drawing Number
Project: DSDR1
Sheet: 7/7
Date: 06/17/00
Name: M Fischman


R Board (Front End Regulation/Control)
U600
LM2940CT-15
+15V Regulator
P600
R600
4.7 ohm
3W
metal oxide
C600
0.47uF
50V
C601
22uF
25V
TA
C602
0.22uF
cera chip
P601
CONNECTOR DB9
male
(from 18VDC P/S)
CONNECTOR DB9
female
U601
LM2940T-12
R601
56 ohm
1W
carbon
R602
56 ohm
1W
carbon
C603
0.47uF
50V
C604
22uF
25V
TA
C605
0.22uF
cera chip
U603
ODCM-5
3A/60VDC SSR
J600
REF/nANT Control
10P Header
(from T Board)
Microwave Geophysics
1124 SPRL, U of Michigan
Ann Arbor, MI 48109
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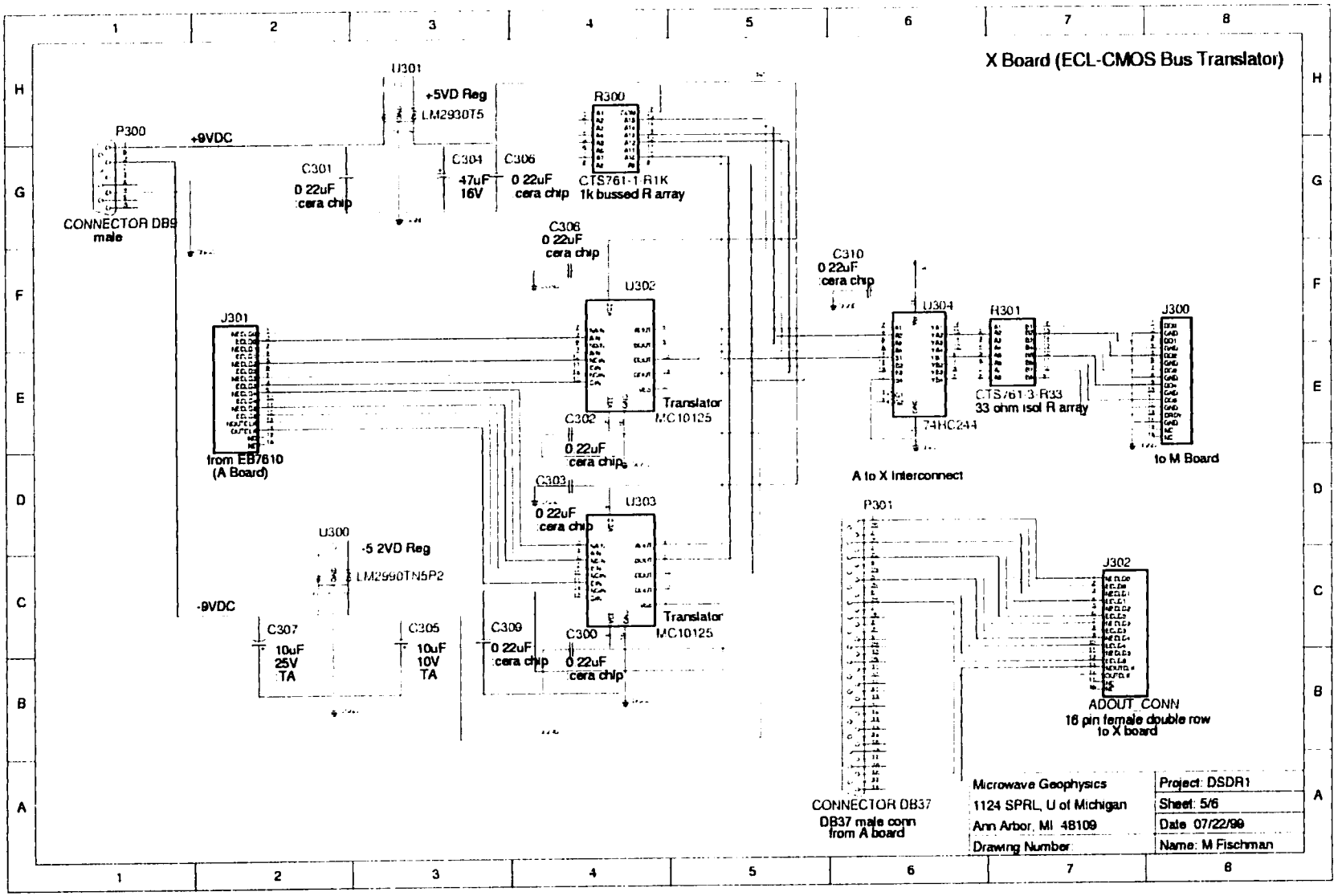
X Board (ECL-CMOS Bus Translator)
U301
+5VD Reg
LM2930T5
P300
+9VDC
CONNECTOR DB9
male
C301
0 22uF
cera chip
C304
47uF
16V
C306
0 22uF
cera chip
R300
CTS761-1-R1K
1k bussed R array
C306
0 22uF
cera chip
U302
J301
from EB7610
(A Board)
Translator
MC10125
C302
0 22uF
cera chip
C303
0 22uF
cera chip
U303
Translator
MC10125
C300
0 22uF
cera chip
U300
-5 2VD Reg
LM2990TN5P2
-9VDC
C307
10uF
25V
TA
C305
10uF
10V
TA
C309
0 22uF
cera chip
C310
0 22uF
cera chip
U304
74HC244
R301
CTS761-3-R33
33 ohm isol R array
J300
to M Board
A to X Interconnect
P301
J302
ADOUT_CONN
16 pin female double row
to X board
CONNECTOR DB37
DB37 male conn
from A board
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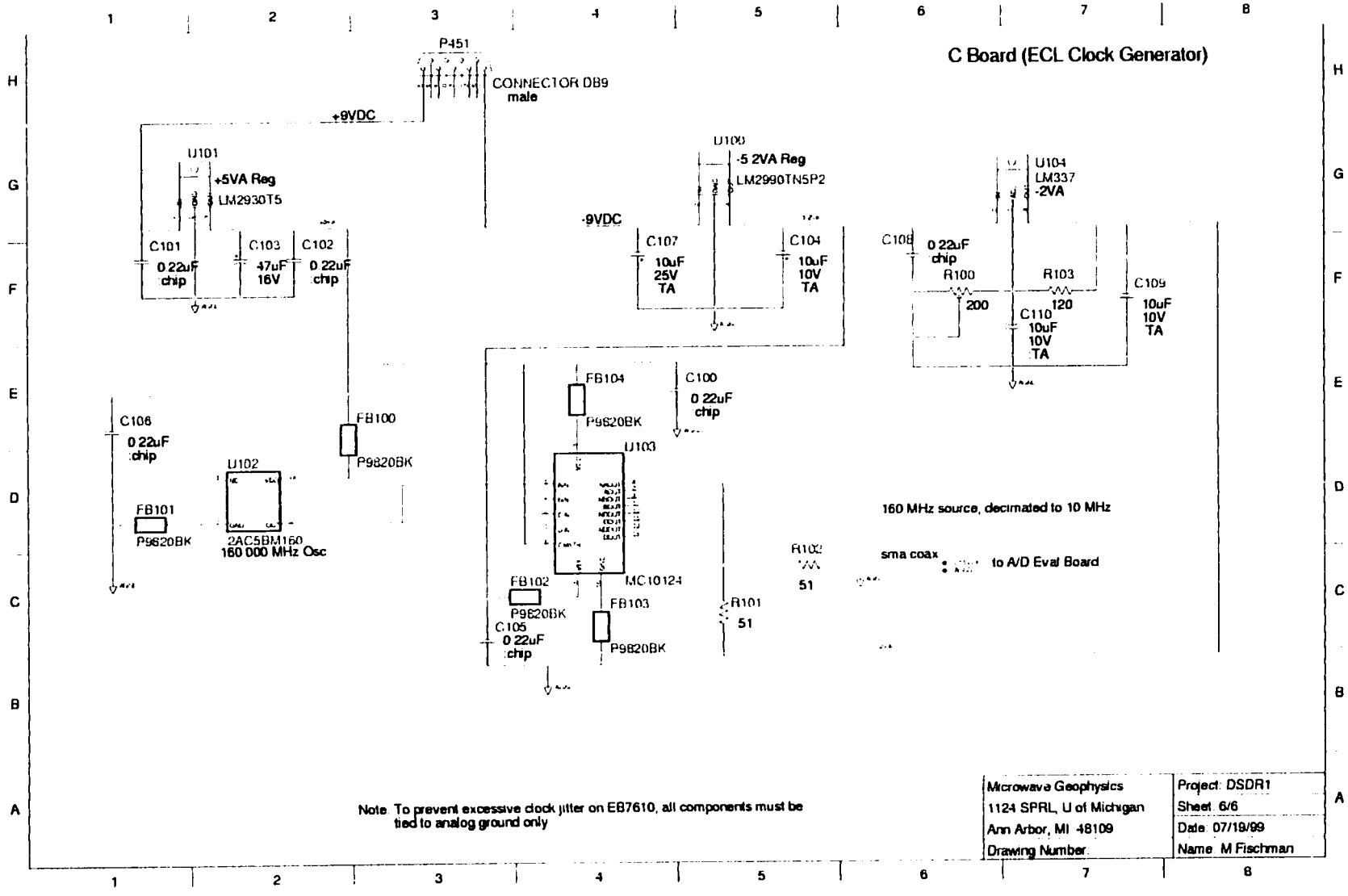
Ann Arbor, MI 48109
Drawing Number
Project: DSDR1
Sheet: 5/6
Date: 07/22/99
Name: M Fischman


C Board (ECL Clock Generator)
P451
CONNECTOR DB9
male
+9VDC
U101
+5VA Reg
LM2930T5
C101
0 22uF
chip
C103
47uF
16V
C102
0 22uF
chip
-9VDC
U100
-5 2VA Reg
LM2990TN5P2
C107
10uF
25V
TA
C104
10uF
10V
TA
U104
LM337
-2VA
C108
0 22uF
chip
R100
200
R103
120
C110
10uF
10V
TA
C109
10uF
10V
TA
FB104
P9620BK
C100
0 22uF
chip
U103
C106
0 22uF
chip
FB100
P9620BK
U102
2AC5BM160
160 000 MHz Osc
FB101
P9620BK
160 MHz source, decimated to 10 MHz
sma coax
to A/D Eval Board
R102
51
FB102
P9620BK
MC10124
FB103
P9620BK
C105
0 22uF
chip
R101
51
Note: To prevent excessive clock jitter on EB7610, all components must be tied to analog ground only
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1124 SPRL, U of Michigan
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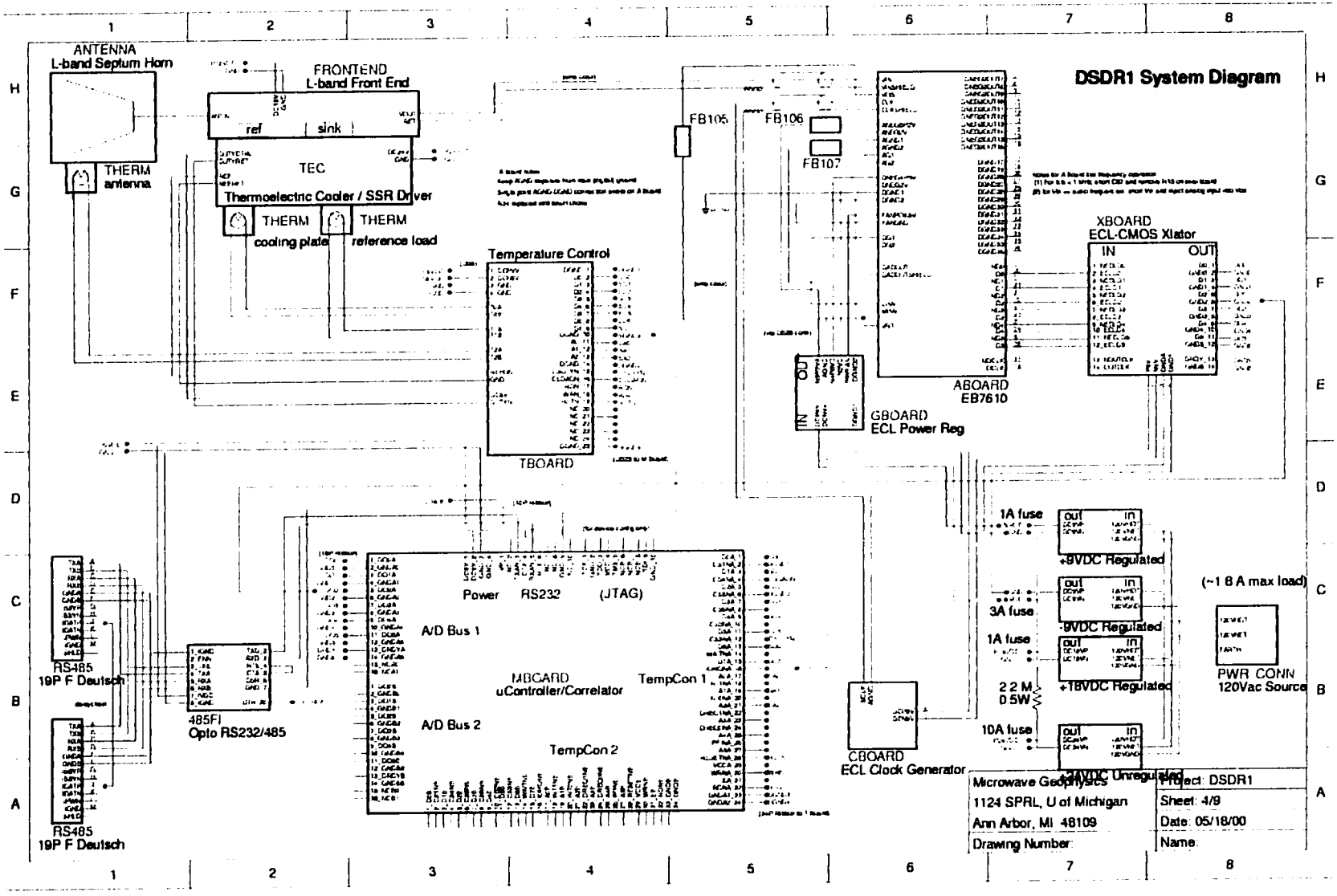
Drawing Number:
Project: DSDR1
Sheet: 6/6
Date: 07/19/99
Name: M Fischman


DSDR1 System Diagram
ANTENNA
L-band Septum Horn
THERM
antenna
FRONTEND
L-band Front End
ref
sink
TEC
Thermoelectric Cooler / SSR Driver
THERM
cooling plate
THERM
reference load
Temperature Control
TBOARD
FB105
FB106
FB107
ABOARD
EB7610
XBOARD
ECL-CMOS Xlator
IN
OUT
GBOARD
ECL Power Reg
1A fuse
+9VDC Regulated
3A fuse
-9VDC Regulated
1A fuse
+18VDC Regulated
2.2 M
0.5W
10A fuse
+24VDC Unregulated
(~1.8 A max load)
PWR CONN
120Vac Source
Power
RS232
(JTAG)
A/D Bus 1
MBCARD
uController/Correlator
TempCon 1
A/D Bus 2
TempCon 2
CBOARD
ECL Clock Generator
RS485
19P F Deutsch
485FI
Opto RS232/485
RS485
19P F Deutsch
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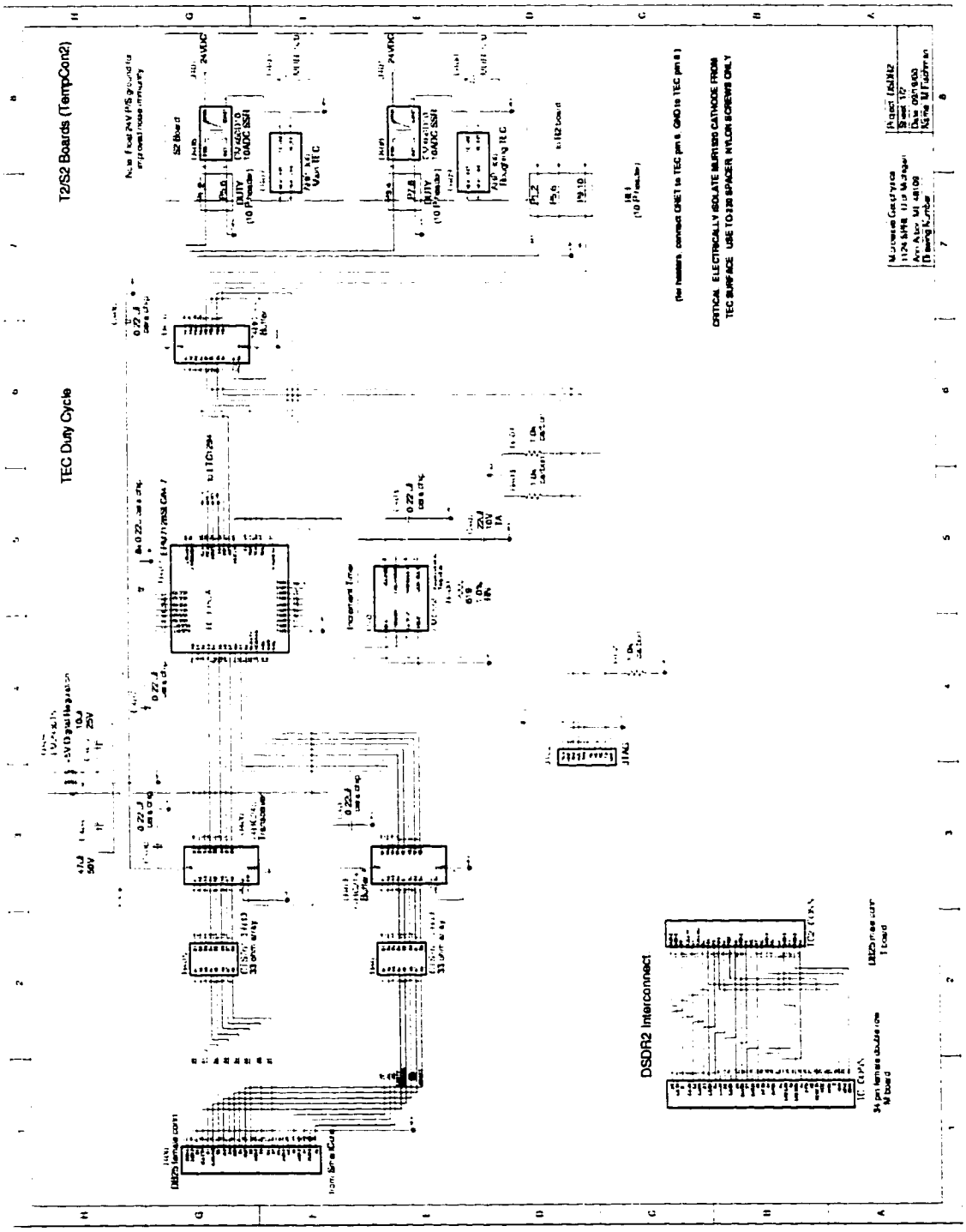
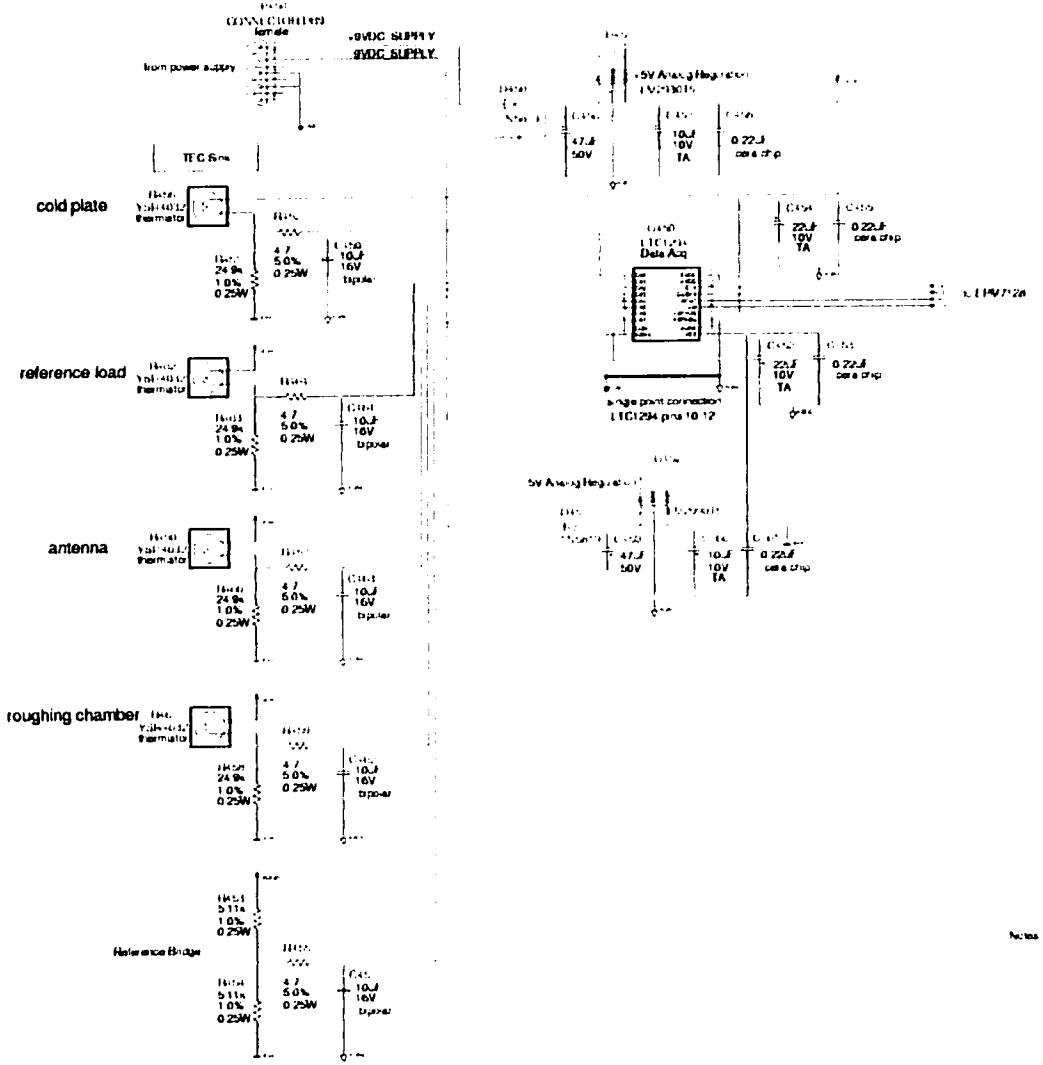
Ann Arbor, MI 48109
Drawing Number:
Project: DSDR1
Sheet: 4/9
Date: 05/18/00
Name:

APPENDIX C

DSDR Receiver 2 (DSDR2) Unique Schematics

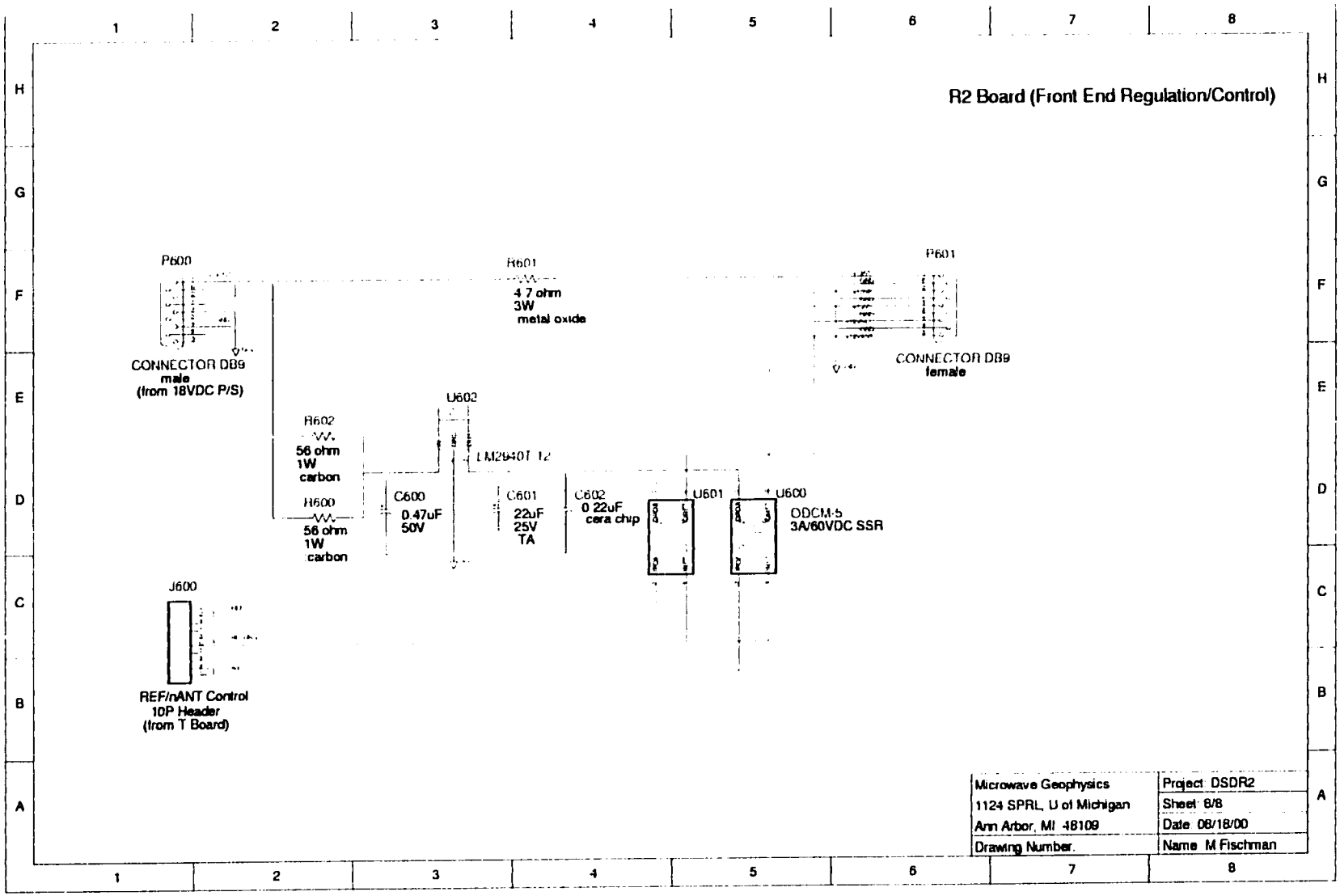

T2/S2 Boards (TempCon2)
TEC Duty Cycle
DSDR2 Interconnect

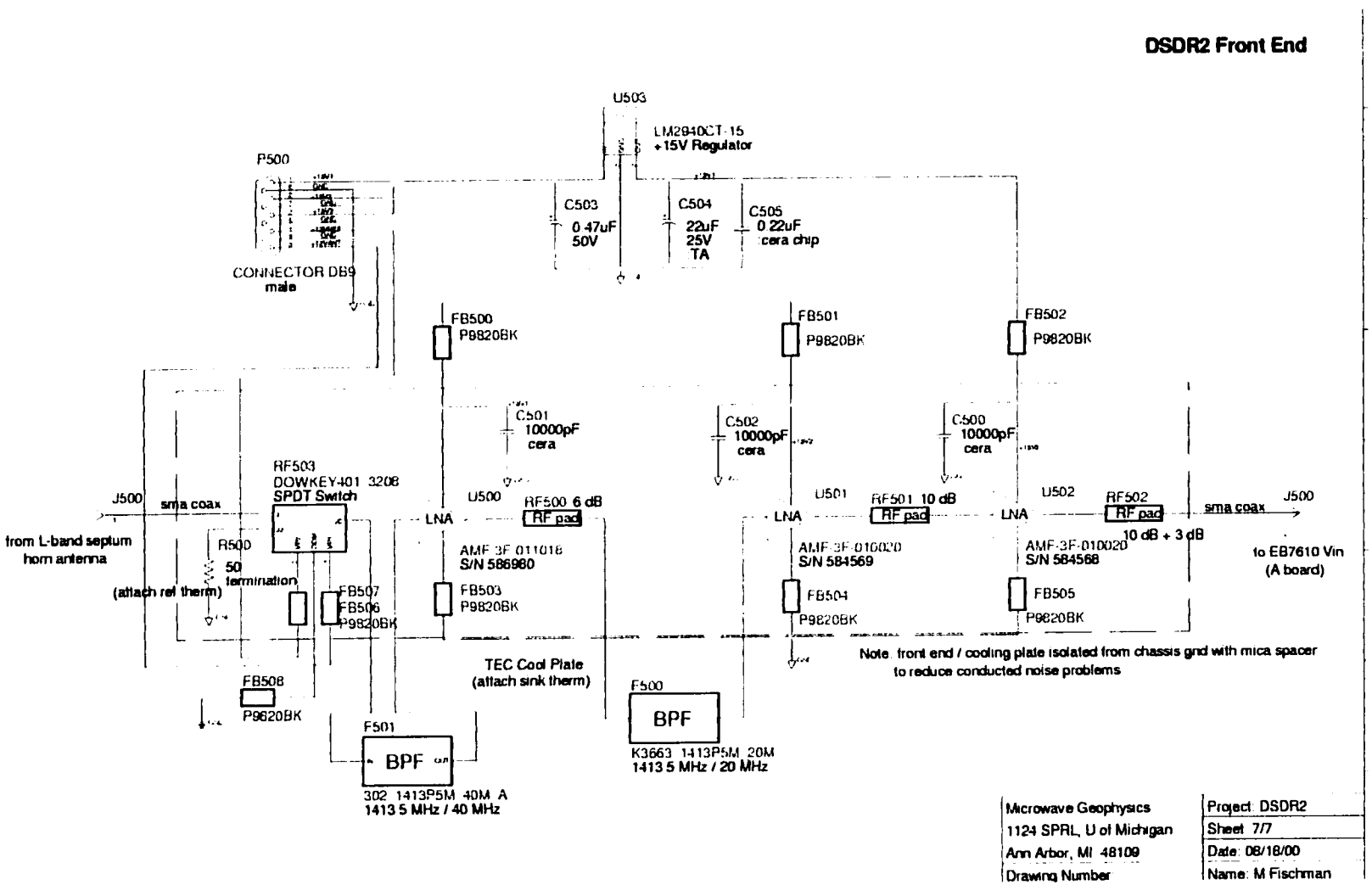
TEC Temperature Sense



Notes (1) Use large AGND plane under LTC1294 for noise reduction
(2) Locate C454 C455 as close as possible to LTC1294 pin 19
(3) Locate C452 C453 as close as possible to LTC1294 pin 11

Microwave Geophysics 1124 SRR, U of Michigan Ann Arbor, MI 48109 Drawing Number	Project DSDR2 Sheet 22 Date 05/19/00 Name M Fischman


R2 Board (Front End Regulation/Control)
P600
CONNECTOR DB9
male
(from 18VDC P/S)
R601
4.7 ohm
3W
metal oxide
P601
CONNECTOR DB9
female
U602
LM2940T-12
R602
56 ohm
1W
carbon
R600
56 ohm
1W
carbon
C600
0.47uF
50V
C601
22uF
25V
TA
C602
0.22uF
cera chip
U601
U600
ODCM-5
3A/60VDC SSR
J600
REF/nANT Control
10P Header
(from T Board)
Microwave Geophysics
1124 SPRL, U of Michigan
Ann Arbor, MI 48109
Drawing Number.
Project: DSDR2
Sheet: 8/8
Date: 08/18/00
Name: M Fischman

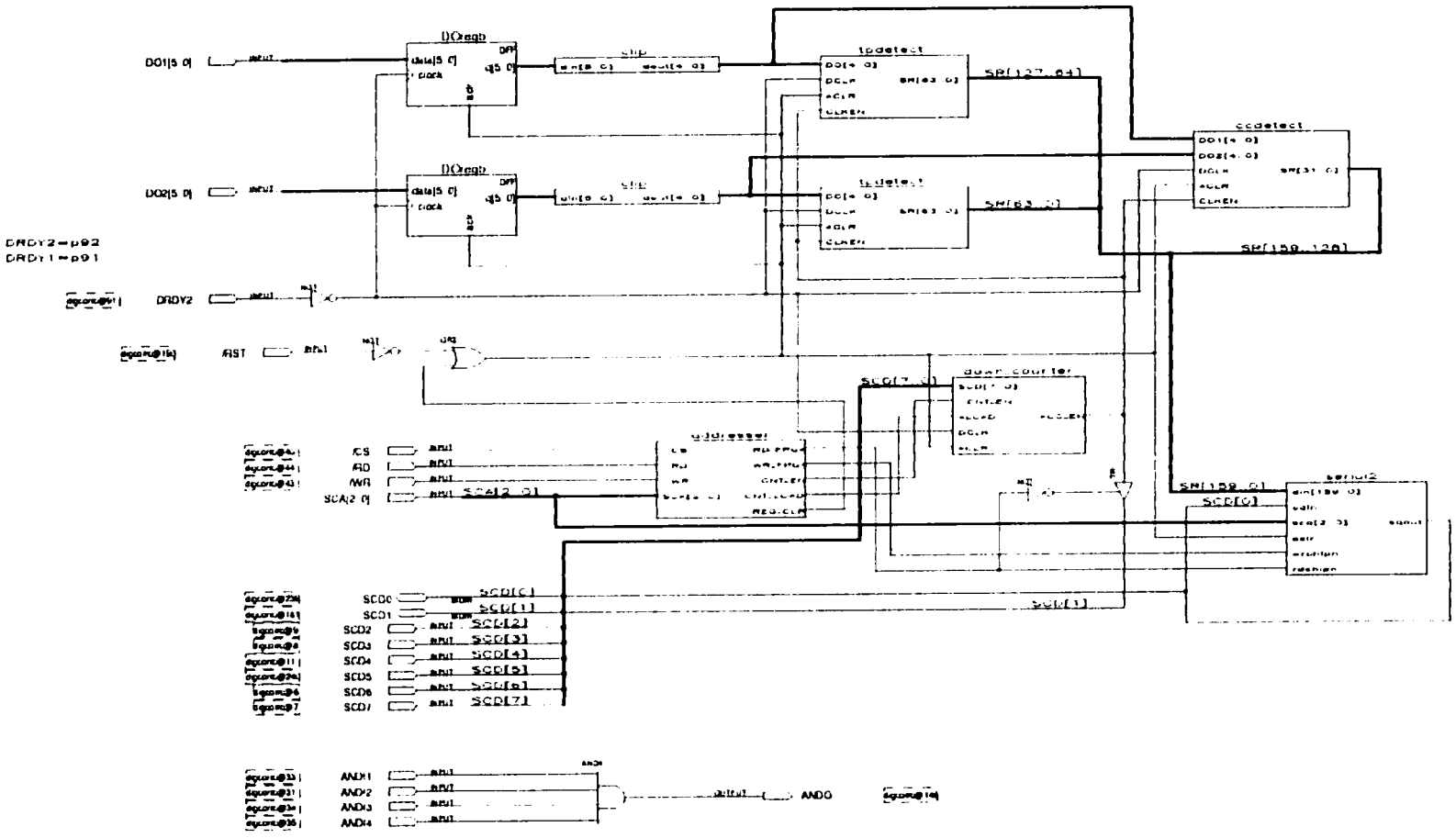

DSDR2 Front End
U503
LM2940CT-15
+15V Regulator
P500
C503
0.47uF
50V
C504
22uF
25V
TA
C505
0.22uF
cera chip
CONNECTOR DB9
male
FB500
P9820BK
FB501
P9820BK
FB502
P9820BK
C501
10000pF
cera
C502
10000pF
cera
C500
10000pF
cera
RF503
DOWKEY-401 3208
SPDT Switch
J500
sma coax
U500
RF500 6 dB
RF pad
U501
RF501 10 dB
RF pad
U502
RF502
RF pad
10 dB + 3 dB
sma coax
J500
LNA
LNA
LNA
from L-band septum
horn antenna
R500
50
termination
(attach ref therm)
AMF-3F-011018
S/N 586980
AMF-3F-010020
S/N 584569
AMF-3F-010020
S/N 584568
to EB7610 Vin
(A board)
FB507
FB506
P9820BK
FB503
P9820BK
FB504
P9820BK
FB505
P9820BK
Note: front end / cooling plate isolated from chassis gnd with mica spacer
to reduce conducted noise problems
TEC Cool Plate
(attach sink therm)
FB508
P9820BK
F500
BPF
K3663-1413P5M-20M
1413.5 MHz / 20 MHz
F501
BPF
302-1413P5M-40M-A
1413.5 MHz / 40 MHz
Microwave Geophysics
1124 SPRL, U of Michigan
Ann Arbor, MI 48109
Drawing Number
Project: DSDR2
Sheet: 7/7
Date: 08/18/00
Name: M Fischman

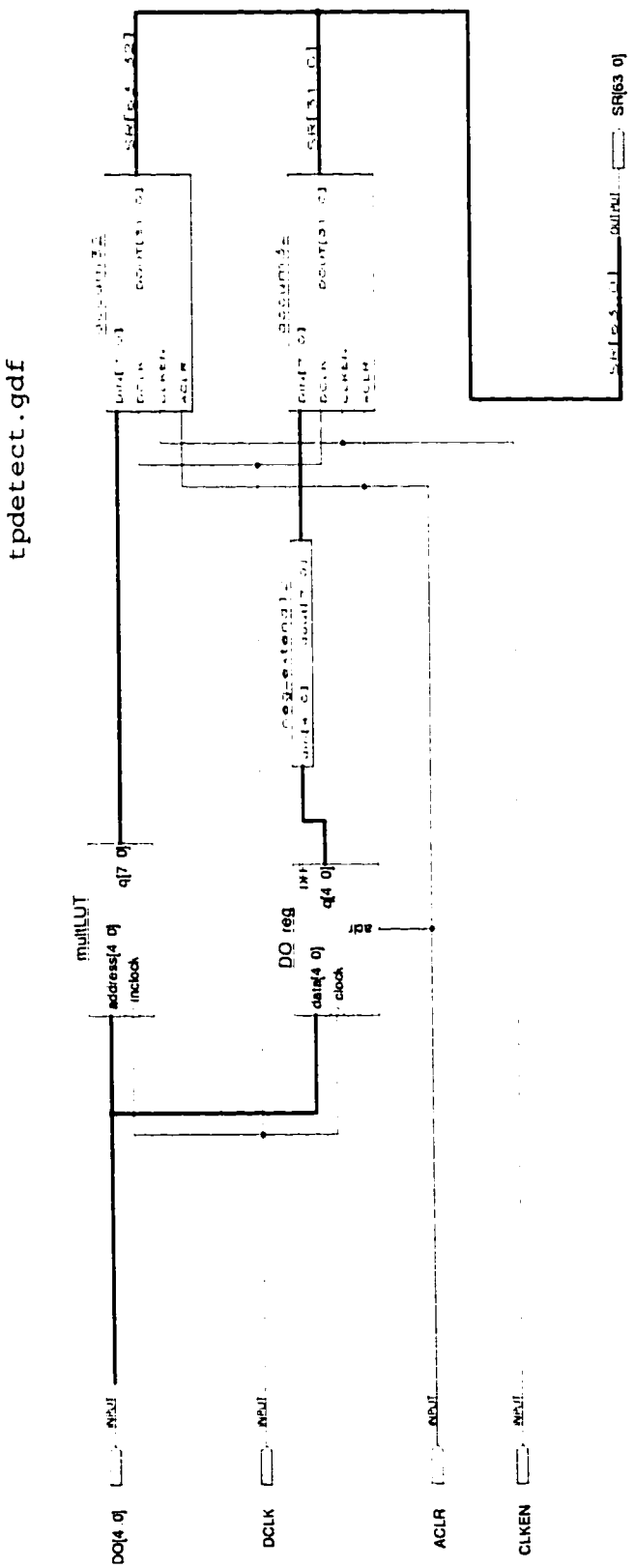
APPENDIX D

EPF10K20 Digital Cross-Correlator Design Files (*digcorrc*)

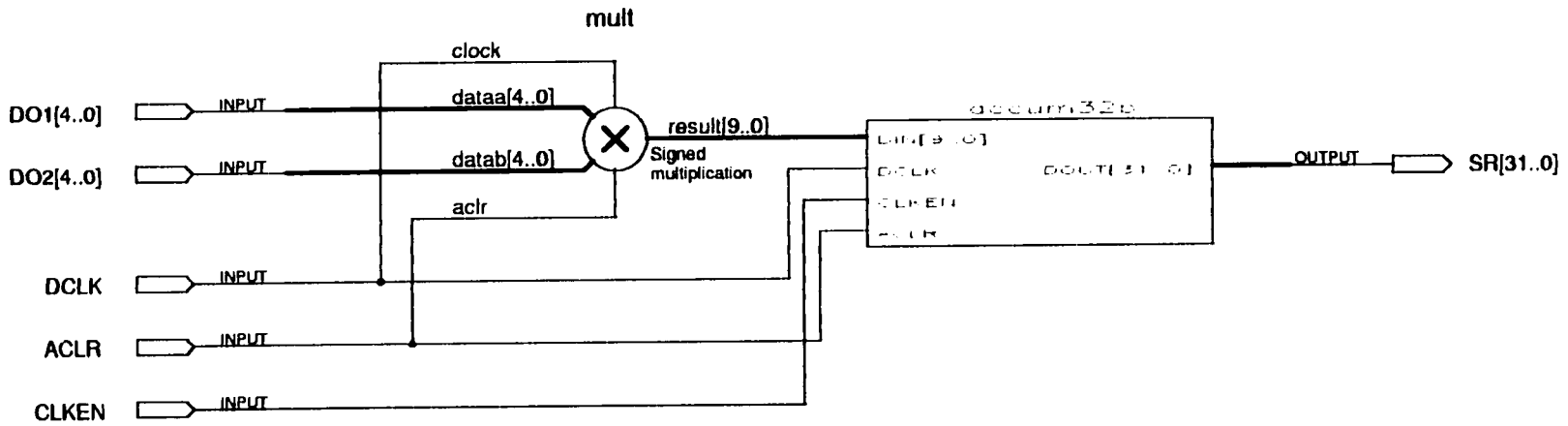
D.1 Graphic Design Files

digcorrc.gdf

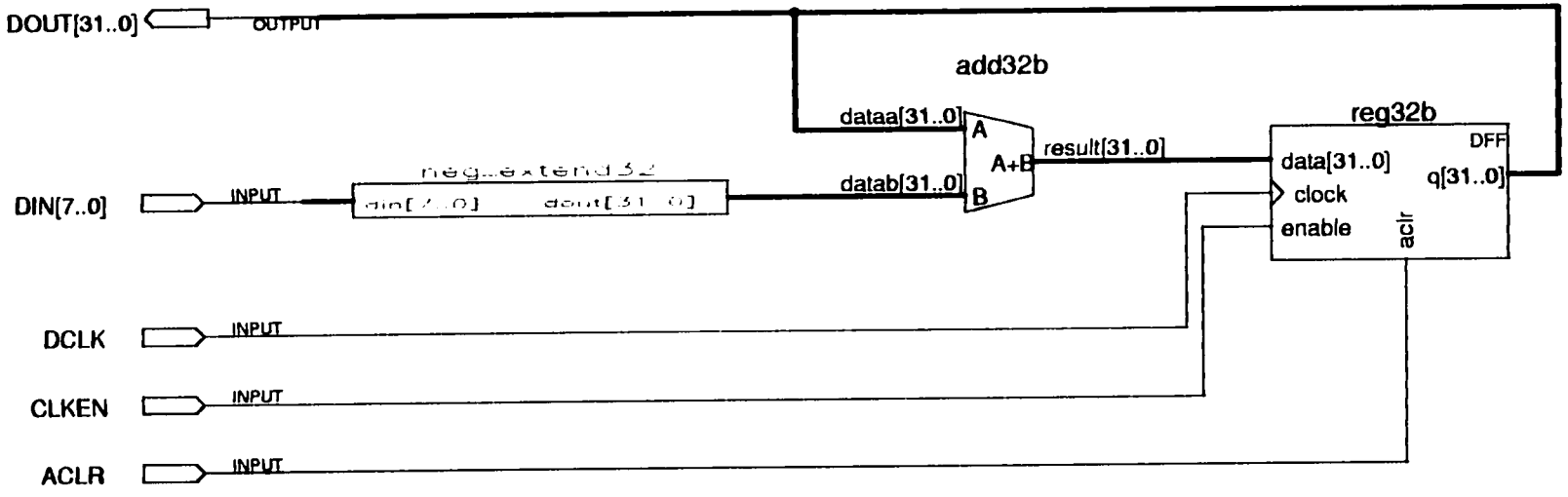


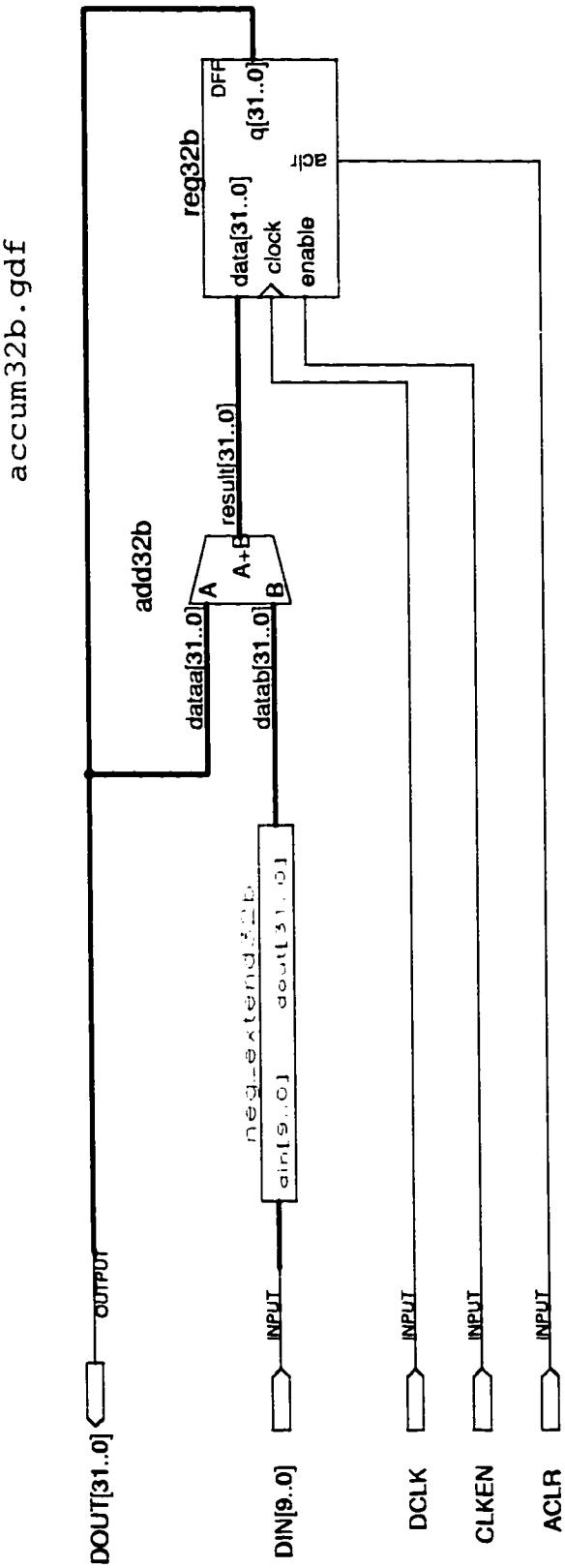

tpdetect.gdf
multLUT
address[4 0]
inclock
q[7 0]
DQ reg
data[4 0]
clock
q[4 0]
aclr
DQ[4 0]
DCLK
ACLR
CLKEN
INPUT
SR[63 0]

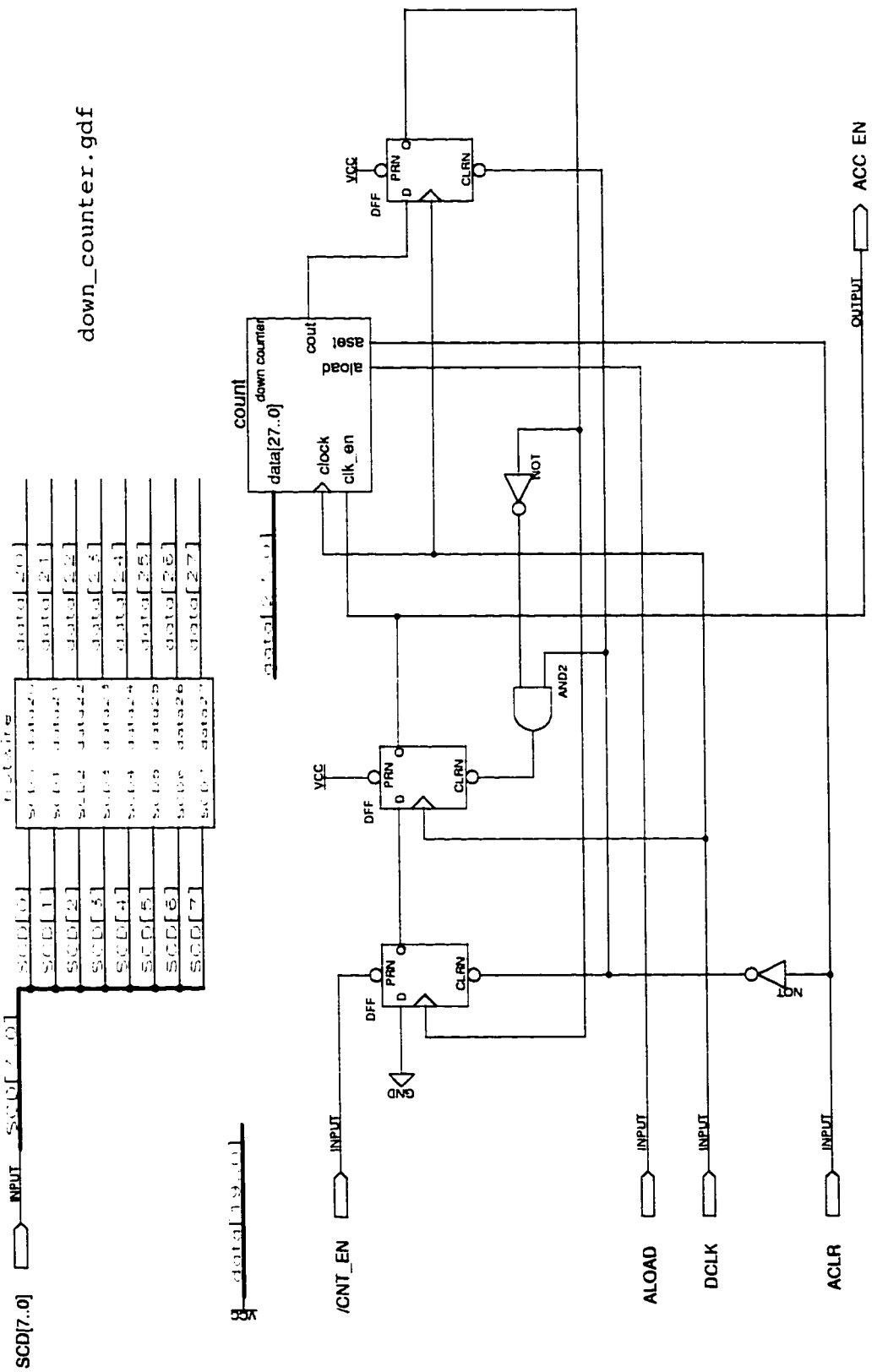
ccdetect.gdf



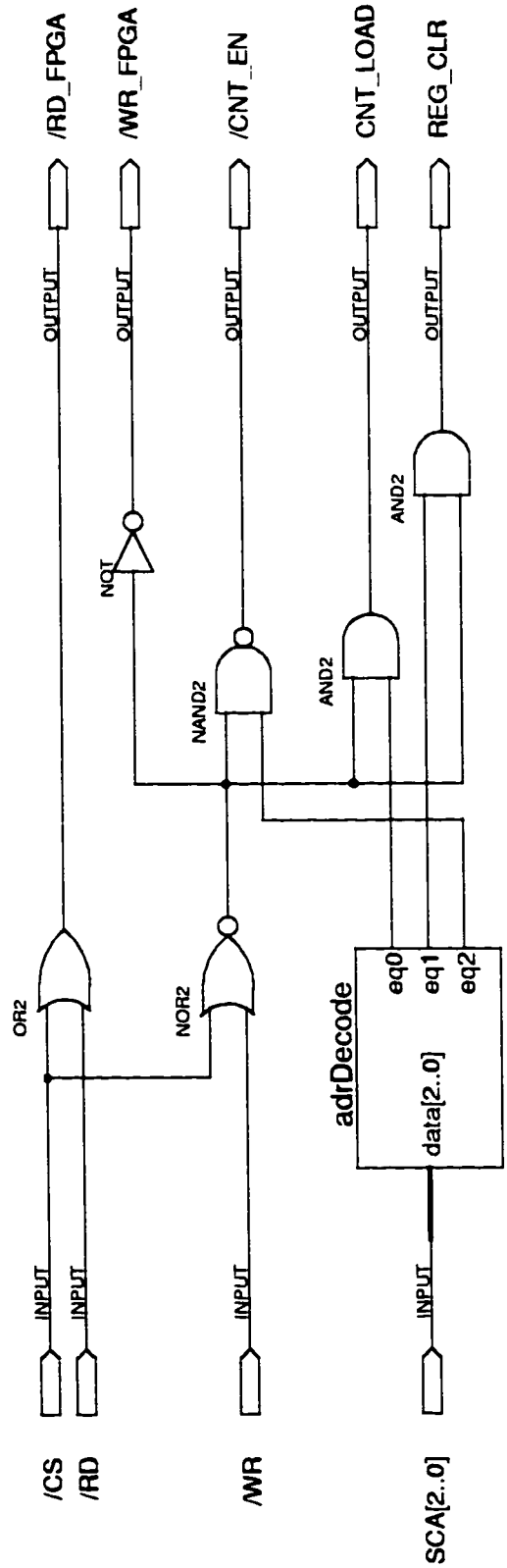
accum32.gdf


DOUT[31..0]
OUTPUT
add32b
dataa[31..0]
A
A+B
result[31..0]
reg32b
DFF
data[31..0]
q[31..0]
clock
enable
aclr
DIN[7..0]
INPUT
neg_extend32
datab[31..0]
B
DCLK
INPUT
CLKEN
INPUT
ACLR
INPUT


accum32b.gdf
reg32b
DFF
q[31..0]
aclr
data[31..0]
clock
enable
add32b
A+B
A
B
result[31..0]
dataa[31..0]
datab[31..0]
OUTPUT
INPUT
DOUT[31..0]
DIN[9..0]
DCLK
CLKEN
ACLR


down_counter.gdf
SCD[7..0]
INPUT
/CNT_EN
ALOAD
DCLK
ACLR
ACC EN
OUTPUT
count
down counter
data[27..0]
cout
aload
aset
clock
clk_en
VCC
DFF
PRN
CLRN
NOT
AND2

addresser.gdf



D.2 Hardware Description Language Files

```
INCLUDE "lpm_shiftreg.inc";
SUBDESIGN serial2
-- serially shift 160-bit data from correlation DSDR to SCore data bus
-- bits 0-31: 32-bit accum^1 for DSDR2
-- bits 32-63: 32-bit accum^2 for DSDR2
-- bits 64-95: 32-bit accum^1 for DSDR1
-- bits 96-127: 32-bit accum^2 for DSDR1
-- bits 128-159: 32-bit cross corr accum for correlation DSDR
-- M Fischman  Nov 2000
(
    din[159..0]             : INPUT; -- parallel data in from 4 32-bit
                                        accumulators
    cdin                    : INPUT; -- control data bit for shift register
    sca[2..0]               : INPUT; -- address bus from SCore
    aclr                    : INPUT; -- asynchronous clear for registers
    wrchipn                 : INPUT; -- active (low) when both chip select and
                                        write are enabled
    rdchipn                 : INPUT; -- active (low) when both chip select and
                                        read are enabled
    sqout                   : OUTPUT; -- serial data (single bit) output
)

VARIABLE
    shiftreg: lpm_shiftreg WITH (LPM_WIDTH=160, LPM_DIRECTION="right");
    -- 160-bit shift register for correlation DSDR
    -- sr[31..0] = DSDR2 1st order accum
    -- sr[63..32] = DSDR2 2nd order accum
    -- sr[95..64] = DSDR1 1st order accum
    -- sr[127..96] = DSDR1 2nd order accum
    -- sr[159..128] = correlation DSDR cross-corr accum
    sren                    : LATCH; -- for shift register enable signal
    srld                    : LATCH; -- for shift register load signal
    srck                    : LATCH; -- for shift register clock signal
    denable                 : NODE; -- enable for addressable latch / decoder
                                       (active high)
    qouten                  : TRI;  -- buffer output data to d0 (of SCore bus)

BEGIN
--  Set up parallel in / serial out register
    shiftreg.data[159..0] = din[159..0]; -- parallel d in
    shiftreg.clock = srck.q; -- data in / data out clock controlled by SCore
    shiftreg.enable = sren.q; -- function enable controlled by SCore
    shiftreg.load = srld.q; -- load signal (1=parallel load in, 0=serial shift
                               out) controlled by SCore
    shiftreg.aclr = aclr;
--  Set up addressable latches / decoder logic which let SCore control shiftreg
    sren.d = cdin; -- control data input (D0 of SCore data bus)
    srld.d = cdin;
    srck.d = cdin;
    denable = wrchipn NOR !SCA[2]; -- decoder/latch enable (active high) allows
                                      SCore to write to latches
    sren.ena = denable AND !SCA[1] AND !SCA[0]; -- write to enable sig if adr=4
    srld.ena = denable AND !SCA[1] AND SCA[0];  -- write to load sig if adr=5
    srck.ena = denable AND SCA[1] AND !SCA[0];  -- write to clock sig if adr=6
--  Set up tri-state buffer for serial data out
    qouten.in = shiftreg.shiftout; -- single-bit serial data out
    qouten.oe = !rdchipn;
```

```
    sqout = qouten.out;
END;

SUBDESIGN clip
-- Clip a 6-bit signed word to a 5-bit signed word
-- (positive clip at +15, negative clip at -16)

(
    din[5..0]                       : INPUT;
    dout[4..0]                      : OUTPUT;
)

BEGIN

IF !(din[5] XOR din[4]) THEN
    dout[4..0] = din[4..0];
ELSIF din[4] THEN
    dout[4..0] = H"F";
ELSE
    dout[4..0] = H"10";
END IF;

END;

SUBDESIGN neg_extend12
-- Turn a 5-bit signed word into an 8-bit signed word
(
    din[4..0]       : INPUT;
    dout[7..0]      : OUTPUT;
)

BEGIN
dout[4..0] = din[4..0];
CASE din[4] IS
    WHEN 0 =>
        dout[7..5] = H"0";
    WHEN 1 =>
        dout[7..5] = H"7";
END CASE;
END;

SUBDESIGN neg_extend32
-- Turn a 8-bit signed word into a 32-bit signed word
(
    din[7..0]       : INPUT;
    dout[31..0]     : OUTPUT;
)

BEGIN
dout[7..0] = din[7..0];
CASE din[7] IS
    WHEN 0 =>
        dout[31..8] = H"000000";
    WHEN 1 =>
        dout[31..8] = H"FFFFFF";
END CASE;
END;

-- multLUT.mif
```

```
-- ROM file for "square" look-up table for a 5-bit signed input
-- ouput size is one byte
-- M Fischman  Nov. 2000

DEPTH = 32;
WIDTH = 8;

ADDRESS_RADIX = HEX;
DATA_RADIX = HEX;

CONTENT
    BEGIN
        0   :   0;
        1   :   1;
        2   :   4;
        3   :   9;
        4   :   10;
        5   :   19;
        6   :   24;
        7   :   31;
        8   :   40;
        9   :   51;
        A   :   64;
        B   :   79;
        C   :   90;
        D   :   A9;
        E   :   C4;
        F   :   E1;
        10  :   FF;
        11  :   E1;
        12  :   C4;
        13  :   A9;
        14  :   90;
        15  :   79;
        16  :   64;
        17  :   51;
        18  :   40;
        19  :   31;
        1A  :   24;
        1B  :   19;
        1C  :   10;
        1D  :   9;
        1E  :   4;
        1F  :   1;
    END;
```

APPENDIX E

RaDOS 0.0 Source Code

```
// RaDOS version 0.0 (08/14/1999)
// DSDR Radiometer Operating System
// FPGA correlator with temperature control (uses preemptive
// multitasking kernel)
// Self-correlation (square and accumulate) for total power rad operation
// Includes command interpreter for RS-232 communication (port 0)
// M Fischman
// last update: 01/12/2000

#define  NTASKS      7         // set up real-time kernel for TempCon & comm
#define  RUNKERNEL   1         // interrups
#use     RTK.LIB
#use     VDRIVER.LIB

#define  NWRITE      0x4040    // address to write integration counter value N
                               // N = (D[7..0]+1)*2^20
#define  REGCLEAR    0x4041    // address to clear all registers in digcorr FPGA
#define  ENABLE      0x4042    // address to initiate integration counter
#define  DCREAD      0x4040    // address to read DigCorr data and status output
                               // D0 = serial data out
                               // D1 = accumulate enable (logic low when accum
                               // finished)
#define  SERREG      0x4044    // 64-bit serial register containing acc1, acc2
                               // offset adr 0, D0 = serial reg enable
                               // offset adr 1, D0 = parallel load in (1) serial
                               // read out (0)
                               // offset adr 2, D0 = clock for load/read ops
#define  LTCSEL      0x40c0    // LTCSEL = adr for reading from/writing to
                               // TempCon ADC (/CS4)
                               // For write mode:
                               // LTCSEL = clock
                               // LTCSEL+1 = /chip_select
                               // LTCSEL+2 = data_in
#define  RFSWADR     0x40c3    // address for RF front end switch (antenna or
                               // reference load)
#define  DUTYADR     0x4080    // DUTYADR = address for writing duty cycle byte
                               // (/CS3)
#define  PLATE       0         // offset for cold plate thermistor
#define  REF         1         // offset for reference load thermistor
#define  ANT         2         // offset for antenna thermistor
#define  RBRIDGE     7         // offset for resistor bridge
#define  NTHERMARY   141       // number of points in thermistor-
                               // temperature array
```

```
#define  MINTEMP     -40       // minimum tabulated temperature of
                               // 44032 thermistor (C)
#define  MINTEMPK    233.15    // min temp of 44032 thermistor (K)
#define  MAXTEMPK    373.15    // max temp of 44032 thermistor (K)
#define  MINDUTY     0.        // minimum duty cycle
#define  MAXDUTY     100.      // maximum duty cycle
#define  NAVG        10        // number of temperature samples averaged
#define  NAN         999       // not a number / undefined value for temp or duty
#define  YOUREOUT    3         // maximum number of temp sensing errors allowed
#define  ZEROCELS    273.15    // zero celsius temperature (in K)
#define  TBUFSIZE    384       // size of serial port Z0 transmit buffer
#define  RBUFSIZE    384       // size of " receive buffer
#define  DBUFSIZE    128       // size of buffer for formatted "Dprintf" to
                               // serial port
#define  ZEROCHAR    0x30      // ASCII zero (0)
#define  ONECHAR     0x31      // ASCII one (1)
#define  CR          0x0d      // ASCII carriage return
#define  LF          0x0a      // line feed
#define  SPC         0x20      // space bar
#define  NUL         0x00      // null character (end of string in C)
#define  STX         0x02      // start of text
#define  ETX         0x03      // end of text
#define  ATTENSC     "\x02$89$12"   // header received when PC addresses
                                    // SmartCore
#define  ATTENPC     "\x02$12$89"   // header sent when SmartCore addresses PC
#define  TAIL        "\x0d\x0a\x03" // tail sent at end of command line
// RaDOS text commands:
#define  FIXTEMP     "FT!"     // command to set the front end
                               // physical temperature
#define  TDARRAY     "TD?"     // command to query the temperature data array
#define  FIXDUTY     "FDC!"    // command to set the duty cycle
#define  SETRFSW     "RFSW!"   // command to set RF switch (to antenna or
                               // ref load)
#define  ASKRFSW     "RFSW?"   // command to query RF switch status
#define  STARTCORR   "CORR!"   // command to initiate radiometer correlation
#define  ASKCORR     "CORR?"   // command to query correlation status
#define  FLTSIZE     16        // maximum buffer size for floating point string
#define  HALFDUTY    0x7f      // 50% duty cycle for TEC
#define  FULLDUTY    0xff      // 100% duty cycle for TEC
// PID tuning history:
// (1) fall 1998-summer 1999:
// TEC cooling control w/ TEC assembly in open, ambient air environment
// (no enclosures)
// RRATE=-6.5 C/min/duty, LLAG=3.0 min
#define  RRATE       5.4          // TEC response rate (C/min/duty)
#define  LLAG        1.1          // TEC lag time (min)
// #define  KDCOEFF     0.17      // proportional term (duty/C)
// #define  TICOEFF     2.0       // integral term (min)
// #define  TDCOEFF     1.5       // differential term (min)
#define  MINUTE      2400         // number of ticks elapsed in 1 minute
                                  // (using virtual driver)
#define  SECOND      40           // number of ticks elapsed in 1 second (")
#define  ONEMEG      1048576L     // integer value for 2^20
#define  DATETIMELEN 17           // length of formatted string for
                                  // date/time stamp
#define  DTYSTRLEN   6            // string length for duty cycle info

#define  Dprintf_z0  Dwrite_z0(dbuf,strlen(dbuf))  // macro for output to
                                                   // serial port
```

```
void  sendtstat();
void  datetimestr(char *datetime);
void  spc2zero(char *a);
void  showintro();
void  correlate(int Nmsb);
void  resetcorr();
void  toggleclock();
unsigned int   sectime();  // returns number of seconds since last
                           // Tempcon update
void  set_clock(int state);
int   read_1294(int chno);
float *getthmdat();
float *gettmpdat();
float getthermtemp(int a);
float r2t(float r, float *tval, float *rval);
float dig2r(int d1, int d2, int a);
void  dutyupdate(float *dutyval);
void  dotempcon();         // temperature control task
void  cli();               // serial port command line interpreter
int (*Ftask[2])() =  {dotempcon, // task 0
                      cli};)     // task 1

// RaDOS global variables:
float tplate,tref,tant; // thermistor temps for cold plate, reference load,
                        // and antenna
float comtemp;          // command temperature (C)
int   tempconflag;      // temperature control flag
                        // 1 = temperature control on
                        // 0 = temperature control off (fixed duty cycle)
float rQ;               // digital correlator output (levels)
float offset;           // dc offset of RF input signal (levels)
unsigned long int acc[2];  // first-order ([0]) and second-order ([1])
                           // 32-bit accumulators
int   rcflag;           // reset correlator flag: 1=reset 0=no reset (valid
                        // data present)
int   ncorr;            // radiometer correlation status flag
                        // 0 = correlation in progress or correlation
                        // result invalid
                        // 1 = correlation result ready/valid
int   nb;               // most significant byte of # of correlated samples
                        // actual # of samples N=(nb+1)*2^20
char  ref_nant;         // RF front end switch status
                        // 'R' = reference load
                        // 'A' = antenna
float duty;             // current duty cycle (output from control Xfer func.)
int   dutybyte;         // duty cycle byte from 0 (always off) to 255
                        // (on time = 255/256)
float kd; // proportional coeff. (duty/C)
                        // note: duty is defined from 0 (always off) to
                        // 1 (always on)
float ti;               // integral coeff. (min*C/duty)
float td;               // differential coeff. (min)
float *rary,*tary;      // thermistor resistance vs. temperature arrays
int   nreset;           // initial operation flag for TempCon PID controller
                        // (0=init/reset)
char  tbuf[TBUFSIZE];   // transmit buffer for serial port
char  rbuf[RBUFSIZE];   // receive buffer for serial port
char  dbuf[DBUFSIZE];   // buffer output to serial port / terminal
```

```
main (){
   int i;

   // load service routine for serial comm into interrupt vector table
   #if ROM==0
      reload_vec(14, Dz0_circ_int);
   #endif
   // RS-232 setup:
   // 8 data bits
   // 1 stop bit
   // no parity
   // CTS/RTS off
   // 9600 baud (may increase later)
   // echo off
   Dinit_z0(rbuf, tbuf, RBUFSIZE, TBUFSIZE, 4, 9600/1200, 0, 0);
   // set serial receiver in ASCII mode (remove backspace chars)
   z0binaryreset();
   rary = getthmdat();     // set up thermistor-temperature data
   tary = gettmpdat();
   kd = 1.2/(RRATE*LLAG);  // set up PID coefficients
   ti = 2*LLAG;
   td = 0.5*LLAG;
// kd = KDCOEFF;
// ti = TICOEFF;
// td = TDCOEFF;
   nreset=0;      // set flag to initialize/reset PID state variables
   comtemp=NAN;   // set (command) temperature is initially undefined
   duty=0.;       // temperature duty cycle initially zero
   dutybyte=0;
   tempconflag=0; // temperature control is initially off
   resetcorr();   // reset correlation variables
   ncorr=1;
   ref_nant='A';  // front end initially looking at antenna
   for(i=0;i<30000;i++);   // wait about 1 s for other boards to stabilize
   showintro();   // show introductory RaDOS screen on terminal
   outport(RFSWADR,0);
   outport(DUTYADR,0);     // clear duty cycle
   dotempcon();   // initial temperature control and sensing operation
   VdInit();      // set up virtual driver and real-time kernel
   run_every(0,MINUTE);    // run temperture control update every minute
   run_every(1,SECOND);    // check serial port receive buffer every second
// Background:
   for(;;)
      if(!ncorr){
         outport(DUTYADR,0);  // turn off temp control during correlation
         for(i=0;i<3000;i++); // wait about 100 ms for heaters and fan to
                              // shut off
         correlate(nb);       // start correlation for the given
                              // integration time
         outport(DUTYADR,dutybyte);    // reenable temp control w/ current
                                       // duty cycle
         ncorr=1;             // set flags showing that correlation result is
                              // ready and valid
         rcflag=0;
      };
}

// Reset registers for correlator
```

```
void resetcorr()
{
   rQ=0.;
   offset=0.;
   acc[0]=0;
   acc[1]=0;
   rcflag=1;
}

// DSDR command-line interpreter
// Every second this task checks RS-232 receive buffer and then parses command
// line sent by PC
void cli()
{
   int i,j,temp;
   char rbufcopy[RBUFSIZE];      // copy of receive buffer
   char tempbuf[16]; // temporary buffer for parsing string in rbufcopy
   char **tailptr;   // used for strtod() (string to floating-point) conversion
   char datetime[DATETIMELEN];   // formatted string for date and time stamp
   float f;                      // temporary storage

   // check if there's a message terminated by ETX character
   if(Dread_z0(rbufcopy,ETX)){
      // check if header is addressing DSDR
      if(!strncmp(rbufcopy,ATTENSC,i=strlen(ATTENSC))){
         j=0;        // OK, start parsing the SmartCore command
         do{
            tempbuf[j]=rbufcopy[i];
            i++; j++;
         }
         // commands always end with ! or ?
         while(tempbuf[j-1]!='!' && tempbuf[j-1]!='?' && tempbuf[j-1]!=CR);
         if(tempbuf[j-1]==CR)
            tempbuf[j-1]=NUL;
         else
            tempbuf[j]=NUL;
         if(!strcmp(tempbuf,TDARRAY))  // "get temperature data" command
            sendtstat();      // show current status from temperature data array
         else if(!strcmp(tempbuf,FIXTEMP)) {    // "set temperature" command
            if((f=strtod(rbufcopy+i,tailptr))>=MINTEMPK && f<=MAXTEMPK){
               comtemp=f;
               sendtstat();
               tempconflag=1;
            } else {
               sprintf(dbuf,"%sER01$argument out of range%s",ATTENPC,TAIL);
               Dprintf_z0;
            }
         } else if(!strcmp(tempbuf,FIXDUTY)) { // "fix duty cycle" command
            if((f=strtod(rbufcopy+i,tailptr))>=MINDUTY && f<=MAXDUTY){
               tempconflag=0;
               duty=f/100.;
               dutyupdate(&duty);
               // the command temperature becomes an undefined quantity now
               comtemp=NAN;
               sendtstat();
            } else {
               sprintf(dbuf,"%sER01$argument out of range%s",ATTENPC,TAIL);
               Dprintf_z0;
            }
```

```
        // "start radiometer correlation" command
        } else if(!strcmp(tempbuf,STARTCORR)) {

           if((temp=atoi(rbufcopy+i))>=0 && temp<=255){
              ncorr=0;    // set flag showing that correlation is in progress
              nb=temp;    // set up integration time
              sprintf(dbuf,"%sCORR0%s",ATTENPC,TAIL);
              Dprintf_z0;
           } else {
              sprintf(dbuf,"%sER01$argument out of range%s",ATTENPC,TAIL);
              Dprintf_z0;
           }
        // "query radiometer correlation" command
        } else if(!strcmp(tempbuf,ASKCORR)) {
           // tell the PC if the correlation result isn't ready yet
           if(!ncorr || rcflag){
              sprintf(dbuf,"%sCORR0%s",ATTENPC,TAIL);
              Dprintf_z0;
           } else { // if correlation's done, send valid data back to PC
              datetimestr(datetime);
              sprintf(dbuf,"%sCORR1$%s$%c$%.6f$%.6f$%ld$%ld%s",ATTENPC,
                 datetime,ref_nant,rQ,offset,acc[0],acc[1],TAIL);
              Dprintf_z0;
           }
        } else if(!strcmp(tempbuf,SETRFSW)) {  // "set RF switch" command
           if(rbufcopy[i]=='A' || rbufcopy[i]=='R'){
              if(rbufcopy[i]!=ref_nant)
                 resetcorr();
              // ref_nant= 'A' (antenna) or 'R' (ref load)
              ref_nant=rbufcopy[i];
              // RF switch on (ref load) or off (antenna)
              outport(RFSWADR,(ref_nant=='R'));
              sprintf(dbuf,"%sRFSW%c%s",ATTENPC,ref_nant,TAIL);
              Dprintf_z0;
           } else {
              sprintf(dbuf,"%sER01$argument out of range%s",ATTENPC,TAIL);
              Dprintf_z0;
           }
        // "query RF switch status" command
        } else if(!strcmp(tempbuf,ASKRFSW)) {
           sprintf(dbuf,"%sRFSW%c%s",ATTENPC,ref_nant,TAIL);
           Dprintf_z0;
        } else {          // error: command not found
           sprintf(dbuf,"%sER00$%s: command not found%s",ATTENPC,tempbuf,TAIL);
           Dprintf_z0;
        }
     }
  }
}

// Send temperature control status out to serial port
void sendtstat()
{
   char datetime[DATETIMELEN];      // formatted string for date and time stamp
   char dtystr[DTYSTRLEN];          // formatted string for duty cycle value

   datetimestr(datetime);           // get date and time string
   sprintf(dtystr,"%5.1f",duty);    // format duty cycle string
   spc2zero(dtystr);
```

```
   sprintf(dbuf,"%sTD%s$%7.3f$%7.3f$%7.3f$%5.1f$%s%s",ATTENPC,datetime,tplate,
      tref,tant,comtemp,dtystr,TAIL);
   Dprintf_z0;
}

// Generate formated string for date and time stamp
void datetimestr(char *datetime)
{
   struct tm now;       // the current time

   tm_rd(&now);         // get current time and format strings for output
   sprintf(datetime,"%2d%2d%4d$%2d%2d$%2d",now.tm_mon,now.tm_mday,now.tm_year,
      now.tm_hour,now.tm_min,now.tm_sec);
   datetime[4]='2'; datetime[5]='0';   // make year Y2K compliant
   spc2zero(datetime);                 // add leading zeros to date and time
}

// Turn leading spaces into leading zeros for terminal display
void spc2zero(char *a)
{
   int i;

   for(i=0;i<strlen(a);i++)
      if(a[i]==SPC)
         a[i]=ZEROCHAR;
}

// Introductory message
char *introtext[] =  {
   "\x0d\x0a",
   "RaDOS 0.0 (1999 Fischtronics, Inc.)\x0d\x0a",
};

// Show introductory screen on terminal
void showintro()
{
   int i;

   for(i=0;i<2;i++)
      while(!Dwrite_z0(introtext[i],strlen(introtext[i]))) hitwd();
}

// Return number of seconds elapsed since last Tempcon update
unsigned int sectime(){
   void time[6];                 // 6 byte timer
   char *timebyte;
   unsigned long int tickstime;  // number of ticks since last Tempcon update
                                 // (once/minute)
   unsigned int sec;             // number of seconds since last Tempcon update
   gettimer(time);
   timebyte = time;
   tickstime = 65536L*((unsigned)timebyte[2])+256L*((unsigned)timebyte[1])+
      ((unsigned)timebyte[0]);
   tickstime += 16777216L*((unsigned)timebyte[3]);
   sec = (tickstime%MINUTE)/40;
   return(sec);
}

// Perform digital self-correlation using EPF10K20 FPGA
```

```
void correlate(int Nmsb){  // Nmsb=0-255 (most sig byte); true # of samples
                           // N=(Nmsb+1)*2^20
   int i,j;
   long int sacc1;       // signed value for first-order accum
   float flacc1,flacc2; // floating point values for first, second order accums
   int corrstatus;       // digcorr status byte (D0=serial data out,
                         // D1=accumulator enable)
   long int N;           // true number of samples during correlation
   float Nfl;

   acc[0]=0;             // clear accums
   acc[1]=0;
   Nfl=0.;
   outport(REGCLEAR,0);     // reset all internal registers on FPGA
   outport(NWRITE,Nmsb);    // write integration time to digital correlator
   outport(ENABLE,0);       // enable integration counter
   do
      corrstatus=inport(DCREAD);
   while
      (corrstatus&2);       // standby while correlation in progress
// Retrieve accumulated data from the 64-bit serial register:
   outport(SERREG,1);       // enable serial register for single bit rollout
                            // into D0
   outport(SERREG+1,1);     // set mode for parallel load from acc1, acc2
                            // acc1 = lower 32 bits
                            // acc2 = upper 32 bits
   toggleclock();           // toggle clock for parallel load in
   outport(SERREG+1,0);     // set mode for serial read out
// begin serial read out (roll right, LSB first)
// roll out acc[0] (1st order) first, then roll out acc[1] (2nd order)
   for(j=0;j<2;j++){
      for(i=0;i<32;i++){
         acc[j]=(acc[j]>>1)+0x80000000*(inport(DCREAD)&1);  // roll in bit right
         toggleclock();
      }
   }
// Show correlation results
   N = (Nmsb+1)*ONEMEG;     // exact number of samples integrated
                            // (after digcorrb upgrade, MF 06/01/00)
   Nfl=N;
   sacc1=acc[0];            // convert acc1 to signed floating-point value
   flacc1=sacc1;
   flacc2=acc[1];           // convert acc2 to floating-point value
   rQ=(flacc2-flacc1*flacc1/Nfl)/Nfl;
   offset=flacc1/Nfl;
}

// Toggle serial register clock low then high
void toggleclock(){
   outport(SERREG+2,0);
   outport(SERREG+2,1);
}

// Temperature sensing and control task
// Once a minute, read thermistor data and load new duty cycle value
// into TEC driver.
void dotempcon()
{
   float error;         // current temperature error term
```

```
   float eacc;          // error accumulator (for integration term)
   float eaccrg;        // storage for old error accumulator
   float eprev,ediff;   // previous error value (for differential term)

   // get thermistor temps for reference load and antenna
   tref=getthermtemp(REF);
   tant=getthermtemp(ANT);
   // get average cold plate temp
   if((tplate=getthermtemp(PLATE))!=NAN && tempconflag){
      error = comtemp-tplate; // find error signal
      if(nreset){
         // store old integrator value in case of integration windup
         eaccrg=eacc;
         eacc+=error;   // calculate integral (summation) of error signal
         // calculate derivative (difference) of error signal (C/min)
         ediff=error-eprev;
      } else {
         eaccrg=0.;           // initially clear integrator (for antiwindup)
         eacc=0.5*error;      // reset parameters for initial operation
         ediff=0.;
         nreset=1;
      }
      // calculate new duty cycle
      if((duty=kd*(error+eacc/ti+td*ediff))>=1. || duty<=0.){
         // if duty is saturated, disable integrator
         // (for anti-integration windup)
         eacc=eaccrg;
         // recalc duty w/ previous integrator value
         duty=kd*(error+eacc/ti+td*ediff);
      }
      // update new duty cycle value and write to TempCon driver
      dutyupdate(&duty);
      eprev=error;
   }
}

// dutyupdate takes a valid floating point duty value (0-1) and converts it
// into the corresponding byte value (0-255), then updates the TempCon duty
// cycle driver
void dutyupdate(float *dutyval)
{
   dutybyte = floor(256.*(*dutyval)+0.5);
   if(dutybyte<0)
      dutybyte=0;
   else if(dutybyte>255)
      dutybyte=255;
   *dutyval = 100.*dutybyte/256.;   // round off floating point duty cycle value
   if(!tempconflag || ncorr)        // update duty cycle as long as we received
                                    // a "fix duty command"
      outport(DUTYADR,dutybyte);    // or if correlation isn't in progress
}

// get thermistor temperature (in Kelvin)
// a = input channel for TempCon A/D converter
float getthermtemp(int a)
{
   int i;               // temperature sample counter
   int errcnt;          // temp sense error counter
                        // If errcnt exceeds YOUREOUT, then record temp as NAN
```

```
                        // (sensing error)
   float t1,tavg;       // temperature samples
   int dotherm0,doref;  // 12-bit data from thermistor and reference bridge

   i=0; errcnt=0; tavg=0.;
   do {                          // get digital data, convert to temp.
      dotherm0=read_1294(a);     // average temp. over NAVG samples
      doref=read_1294(RBRIDGE);
      t1=r2t(dig2r(dotherm0,doref,a),tary,rary);
      if(t1==NAN)
         errcnt++;
      else{
         tavg+=t1;
         i++;
      }
   }
   while(i<NAVG && errcnt<YOUREOUT);
   if(errcnt==YOUREOUT)
      tavg=NAN;                  // error: temperature sensor out of range
   else
      tavg /= NAVG;
   return(tavg);
}

// Convert test and reference digital words to thermistor resistance value
// a = input channel for TempCon A/D converter
float dig2r(int d1, int d2, int a){
// d1 = 12-bit word from test channel
// d2 = 12-bit word from reference channel
// both d1, d2 are bipolar, 2's complement
   float vref = 5.03;      // reference voltage of 1294
   float vcc = 5.03;       // +5V analog supply
   float vee = -5.00;      // -5V analog supply
// bias resistor values for channels 0,1,2,3
// (plate, reference, antenna, reserved):
   float rs[4] = {24840.0, 24850.0, 24940.0, 24820.0};
   float r1 = 5120.0,r2=5130.0;     // bridge reference resistors
   float delv,rtherm;               // delta-v of wheatstone bridge, calculated
                                    // thermistor value

   delv = (d1-d2)*vref/2048;
   rtherm = rs[a]*(((vcc-vee)*r1-delv*(r1+r2))/((vcc-vee)*r2+delv*(r1+r2)));
   return rtherm;
}

// Convert thermistor R value into physical temperature (K)
float r2t(float r, float *tval, float *rval){
   int i,j;
   float t0;
   i=0;

   if(r>rval[0])           // return an error if temp < -40 C ~ 233 K
      t0=NAN;
   else{
      // scan thru resistance table at 10 C increments
      while(r<rval[i] && i<NTHERMARY)
         i+=10;
      if(i>=NTHERMARY)     // return an error if temp > +100 C ~ 373 K
         t0=NAN;
```

```
      else if(r==rval[i])
         t0=tval[i];
      else{
         j = i-10;
         // scan thru resistance table at 1 C increments
         while(r<rval[j] && j<NTHERMARY)
            ++j;
         if(j>=NTHERMARY)
            t0=NAN;
         else if(r==rval[j])
            t0=tval[j];
         else        // interpolate to find temp.
            t0=tval[j-1]+(r-rval[j-1])/(rval[j]-rval[j-1]);
      }
   }
   return(t0); // return temperature value in Kelvin
}

// Set up resistance array for 44032 type thermistor
float *getthmdat(){
   static float thar[NTHERMARY]={
      884600.,830900.,780800.,733900.,690200.,649300.,611000.,575200.,541700.,
      510400.,481000.,453500.,427700.,403500.,380900.,359600.,339600.,320900.,
      303300.,286700.,271200.,256500.,242800.,229800.,217600.,206200.,195400.,
      185200.,175600.,166600.,158000.,150000.,142400.,135200.,128500.,122100.,
      116000.,110300.,104900.,99800.,94980.,90410.,86090.,81990.,78110.,74440.,
      70960.,67660.,64530.,61560.,58750.,56070.,53540.,51130.,48840.,46670.,
      44600.,42640.,40770.,38990.,37300.,35700.,34170.,32710.,31320.,30000.,
      28740.,27540.,26400.,25310.,24270.,23280.,22330.,21430.,20570.,19740.,
      18960.,18210.,17490.,16800.,16150.,15520.,14920.,14350.,13800.,13280.,
      12770.,12290.,11830.,11390.,10970.,10570.,10180.,9807.,9450.,9109.,8781.,
      8467.,8166.,7876.,7599.,7332.,7076.,6830.,6594.,6367.,6149.,5940.,5738.,
      5545.,5359.,5180.,5007.,4842.,4682.,4529.,4381.,4239.,4102.,3970.,3843.,
      3720.,3602.,3489.,3379.,3273.,3172.,3073.,2979.,2887.,2799.,2714.,2632.,
      2552.,2476.,2402.,2331.,2262.,2195.,2131.,2069.
   };
   return(&thar[0]);
}

// Set up temperature array for 44032 type thermistor (units in Kelvin)
float *gettmpdat(){
   int i;
   static float tear[NTHERMARY];

   for(i=0;i<NTHERMARY;i++)
      tear[i]=i+MINTEMP+ZEROCELS;   // ZEROCELS term converts it to K
   return(&tear[0]);
}

// Read a 12-bit (bipolar, two's complement) word from a channel of the 1294
int read_1294(int chno){
   int j,k,control,value;
   char bit;

   // read channel # chno in bipolar mode, MSB first
   control=0xc3+32*(chno%2)+8*(chno/2);
   value=0;
   outport(LTCSEL+1,0);          // assert CS on LTC1294
   outport(LTCSEL+2,0);          // set the DIN bit to 0
```

```
   set_clock(0); set_clock(1);   // toggle clock a couple of times
   set_clock(0); set_clock(1);
   for(j=7;j>=0;j--){            // send control word (MSB first)
      set_clock(0);
      outport(LTCSEL+2,control>>j);
      set_clock(1);
   }
   outport(LTCSEL+2,0);          // set DIN to 0
   set_clock(0); set_clock(1);   // toggle clock once before data read
   for(k=0;k<12;k++){            // read 12 bits output from ADC (MSB first)
      set_clock(0);
      set_clock(1);
      bit=inport(LTCSEL)&1;
      value=(value<<1)+bit;      // get bits 0 thru 11
   }
   outport(LTCSEL+1,1);          // clear LTC1294 CS
   if(value>=2048)
      // convert 12-bit 2's complement to signed integer
      value=value-4096;
   return value;
}

void set_clock(int state){       // toggle clock to zero or one (state)
   if(state)
      outport(LTCSEL,1);
   else
      outport(LTCSEL,0);
}
```

APPENDIX F

Correlation DSDR Address Map

chip select	base address	item	offset	op	data bus
CS1	04000h	reserved	—	—	—
CS2	04040h	load digcorr integration counter	00h	WR	$N = (D[7..0] + 1) \times 2^{20}$
		digcorr global register clear	01h	WR	don't care
		enable digcorr integration counter	02h	WR	don't care
		digcorr serial interface	04h	WR	D0 = enable
			05h	WR	D0=1: parallel load in D0=0: serial read out
			06h	WR	D0 = load/read clock
		digcorr data	00h	RD	D0 = serial Dout D1 = accum enable
CS3	04080h	tempcon1 duty cycle	00h	WR	dutymain = D[7..0]
			01h	WR	dutyrough = D[7..0]
CS4	040C0h	tempcon1 DAQ	00h	WR	D0 = DAQ clock
			01h	WR	D0 = DAQ CSn
			02h	WR	D0 = DAQ serial Din
			00h	RD	D0 = therm serial Dout
		DSDR1 front end switch	03h	WR	D0=0: antenna D0=1: reference
CS5	04100h	tempcon2 duty cycle	00h	WR	dutymain = D[7..0]
			01h	WR	dutyrough = D[7..0]
CS6	04140h	tempcon2 DAQ	00h	WR	D0 = DAQ clock
			01h	WR	D0 = DAQ CSn
			02h	WR	D0 = DAQ serial data in
			00h	RD	D0 = therm serial Dout
		DSDR2 front end switch	03h	WR	D0=0: ref pulse off D0=1: ref pulse on
			04h	WR	D0=0: ant pulse off D0=1: ant pulse on

Notes

digcorr	=	digital correlator
dutymain	=	main duty cycle
dutyrough	=	roughing chamber duty cycle
tempcon1	=	receiver 1 temperature control
tempcon2	=	receiver 2 temperature control
CS	=	chip select
DAQ	=	data acquisition
RD	=	read
WR	=	write

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