# High Performance 12-24 GHz RF Front-End Components Fabricated in a Commercial SiGe Bipolar Process

**by**

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To those who tell me I can't.

# ACKNOWLEDGEMENTS

As I near the end of my formal education, I am forced to reflect back on the long journey that has lead to this point. In my sixth grade English class I was given the assignment to write my autobiography. In this account, written when I was 12 years old, I wrote that I would receive my Ph.D. in 2003 from Purdue University in the area of geology. I only missed the date by one year and the school by a a few hundred miles, and as for geology, I liked playing with rocks. At the time, I am sure I did not understand what was involved with earning a Ph.D., but I did know that I wanted to strive to be the best. Fast forward 15 years and I have nearly completed this chapter of my life and I am ready to take on the new challenges that await me, but first I must acknowledge those who inspired me along the way.

First, I must thank my thank my mother who never discouraged me from taking on a challenge and for forcing me to use my own resources to to answer questions. As a child if I did not know the answer and I consulted her for help, she would simply tell me to "look it up." To this day I still find myself exhausting all of my own resources before asking anyone for help.

Next, I must thank all of the wonderful educators at Rose-Hulman Institute of Technology. Who could imagine that one of the top undergraduate engineering schools in the county is nestled amongst the corn fields in rural Indiana. While at Rose-Hulman it was not apparent, but upon leaving I realized that I had received a world class engineering education. Rose-Hulman is unlike any other school, the purpose of the faculty is not to do engineering research but rather improve engineering education and foster a community of learning. All of the faculty were wonderful but there are several that I must acknowledge by name. Dave Voltmer and Frank Acker are two faculty that were the instructors for my electromagnetics and circuits classes. They laid a solid foundation upon which I would build in the following years. I must also acknowledge Julia Williams in the department of

Humanities and Social Sciences, who was my instructor for freshman composition and later technical communication. In addition to her unique sense of humor that I thoroughly enjoy, she was instrumental in helping me hone my writing skills before I realized their importance in engineering.

I have had several internships and co-ops but none were as important as the summer between leaving Rose-Hulman and arriving at the University of Michigan. This summer was spent working for Conexant Systems, and at the time I had no experience in RF or IC design. However, James Young took a risk on me in hopes that I could help with the design of a BiCMOS GPS receiver. By the end of the summer I had learned to use the Cadence tools and had completed the layout of nearly all of the RF and analog baseband components. This experience has proved invaluable to me and I still draw upon it today and I am very thankful to James for this unique opportunity.

Next, I must thank my academic advisor, Gabriel Rebeiz. I foolishly decided to attend the University of Michigan without first securing a source of funding. One month before I arrived I was forced to send a mass email to many of the faculty in circuits and electromagnetics introducing myself and asking for funding. Only one person responded and that was Gabriel. He had recently began an RFIC research effort and was looking for students. He took a risk and hired me sight unseen via email but I think it is safe to say that this risk has paid off for both of us.

I often get asked by those outside of the research group, "What is it like to work for Gabriel?" From what they see on the outside they assume that it must be difficult and somewhat unpleasant, but in general this is not the case. In the beginning he can be very tough, but this makes you a better researcher. He also adapts his management style to each student as necessary. If the student is self-motivated and can work independently he leaves you alone, but if a student needs motivation he will be glad to provide it. Despite the occasional last minute slide for a presentation that he has known about for weeks and his unwavering aversion to using 12 point font, working with Gabriel has been an excellent experience and I am better researcher than I might have been otherwise.

I must also thank J.-P. Lanteri for the providing the financial support from M/A-COM to fund the work done in this thesis. Without this access to the Atmel MPW and engineering fabrication runs this work would not have been possible. Also, Ian Gresham was instrumental in my work, serving as my contact at M/A-COM and providing research di-

rection as well as technical guidance with respect to the details of the SiGe process in which all of my work was fabricated.

In my time at the University of Michigan, I have made many friends both in and out of the Radiation Lab. There are too many to name individually, but there are a few that I must mention. The first couple years of graduate school is very difficult, juggling classes, teaching and research while adapting to a new place, but Renee Wung and Helena Chan made it a little more pleasant that it would have been otherwise. They were always there to drag me out of the lab to go Dominick's or another fine Ann Arbor establishment. I must also thank my good friend Bryan Hung, we have spent many long hours discussing everything from circuit design to the finer points of western pop culture and colloquialisms of the English language. With regards to research, his questions always make me think and I am better designer because of it.

No acknowledgement would be complete without recognizing the staff of the Radiation Lab and the EECS Department. Karen Kirchner, Mary Eyler, Susan Charnley, Karla Johnson and Richard Carnes put forth an extreme amount of effort to keep the organization within the Radiation Lab and their work does not go unnoticed. Finally, Beth Stalnaker and Karen Liska may be the two most helpful people in the EECS department, from the day you arrive as a new graduate student without funding and without any idea how to even register for classes until the day you leave with your degree in hand, they are there to answer all of your questions.

Timothy Michael Hancock
Ann Arbor, Michigan
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# TABLE OF CONTENTS

# LIST OF TABLES

# LIST OF FIGURES

**Figure**

# LIST OF APPENDICES

**APPENDIX**

# CHAPTER 1

# Introduction

## 1.1 Historical Developments in the Design of Radio Frequency Integrated Circuits (RFIC)

The bipolar junction transistor was invented in 1947 and saw many improvements until the 1970s where it reached a plateau. In the late 1970s, there was a renewed interest in bipolar transistors for their use in mainframe computers which led to an increase in research and development. This resulted in the diffused bipolar junction transistor being replaced by a bipolar device fabricated using ion-implantation. Later, with the advent of low temperature epitaxial growth allowing in-situ doping, ion-implanted BJTs eventually gave way to the bipolar structure that is familiar today, the double-polysilicon self-aligned bipolar junction transistor [1]. Scaling and manufacturing technology allowed this structure to improve throughout the 1980's but it was clear that continuing to reduce the base width to increase transistor speed would be problematic.

By the late 1980's, before the proliferation of SiGe BJTs and sub-micron RF CMOS, silicon BJTs were available with an $f_T$ of 10-20 GHz for an ion-implanted bipolar device [2]. As the 1990's approached, sub-micron device technology was becoming a reality. For CMOS the decreasing gate lengths resulted in faster MOS transistors for both digital and analog applications. This lithography scaling had less of an impact on bipolar performance and it would be the development of the SiGe base that revitalized silicon bipolar transistors for the world of RF design. In the short time span from 1990 to 1993, the state-of-the-art bipolar technology at IBM went from having an $f_T$ of 40 GHz for a traditional ion-implanted Si base to an $f_T$ of 117 GHz for an epitaxially grown SiGe base [3].

Clearly active device technology was improving but RFIC design would not become a reality until high quality passive components were realized on a silicon substrate. Capacitors are easily implemented in silicon processes due to their thin-film nature, however planar inductors posed a problem. Planar inductors on silicon substrates were investigated in the 1960's at Motorola, however due to the low operating frequencies, large values of inductance were needed and resulted in consuming too much area on a silicon chip and achieved only poor performance at best [4]. By the early 1990's, the increasing speed of transistors and aggressive lithographic scaling led to a re-investigation of planar inductors on silicon substrates for high-Q applications.

One of the road blocks to integrated inductors on silicon substrates was the capacitance of the inductor windings to the lossy substrate below. Initially, silicon bipolar processes were a much better candidate than their CMOS counterparts for the implementation of integrated inductors because the substrate doping in a bipolar process is typically greater than 10 $\Omega$·cm. As early as 1990, quality factors in the range of 3-8 and self-resonant frequencies well into the gigahertz range could be achieved [5]. CMOS transistors were traditionally fabricated on highly doped substrates (0.01 $\Omega$·cm) to eliminate latch-up, and this resulted in planar spiral inductors with very low quality factors and self-resonant frequencies. This forced would-be RFIC designers using CMOS to explore other avenues that included using bond wire inductance and post-processing such as bulk micro-machining [6, 7]. While these techniques can produce extremely good results, due to the additional cost and/or fabrication tolerances, the more exotic approaches have not been adopted by the semiconductor industry [8].

As it became clear that the substrate doping would be a hurdle for silicon RFIC design, the semiconductor industry began making integrated circuit processes more RF friendly in search of complete system-on-chip (SOC) designs. Some of the steps that have been taken in the last ten years include, thicker metal for inductor implementation, larger distance of the thick metal from the substrate, copper interconnect, lower doped substrate and deep trench isolation. Today a commercially available SiGe BiCMOS process with 0.18 $\mu$m feature size can offer deep-submicron CMOS, a bipolar device with an $f_t$ of 120 GHz, high quality thin film resistors and capacitors and 3-7 layers of metal interconnect, one of which is 4 $\mu$m thick copper which is more than 10 $\mu$m from the silicon substrate that has a doping of greater than 10 $\Omega$·cm.

In addition to the improved device technology, there has been impressive improvements in electromagnetic simulation tools and computing power. In the 1980,s the Numerical Electromagnetics Code (NEC) was available for wire antennas and there were some method of moments tools for planar microwave circuits. Commercially available planar EM tools broke onto the scene in 1989 with the introduction of EMsim and Sonnet[1] and was later followed by Ansoft HFSS[2] for 3D problems [9]. Today the most popular planar analysis tools are Sonnet and Agilent's Momentum,[3] both of which use a variation on the Method of Moments. These tools have allowed RFIC designers to analyze different inductor structures in a timely fashion and optimize designs whereas early planar inductors were designed using approximated closed-form expressions [10].

## 1.2 Atmel SiGe Technology

The work presented in this thesis is fabricated in a commercial SiGe bipolar process offered by the Atmel Corporation. Initially this work started in the SiGe2-basic process and later migrated to the SiGe2-RF process as it became qualified. SiGe2-RF offers two HBTs with a unity current gain cut-off frequency ($f_t$) of 50 GHz and 80 GHz with a collector-emitter breakdown voltage ($V_{CEBO}$) of 4 V and 2.5 V respectively. Both transistors have a maximum oscillation frequency ($f_{max}$) of 90 GHz. Initially the foundry provided a Gummel-Poon SPICE model deck for 'the NPN transistors. Subsequently they have provided complete design kits for both the Advanced Design System (ADS) platform and SpectreRF in Cadence. The first release of the SiGe2-RF design kit offered models based on measured results for only the HBTs, resistors and a lateral silicon PNP. As the process has matured, the models have improved to include all of the devices such as a varactor diode, Schottky diode and multiple ESD devices. In addition, a Gummel-Poon or HICUM model can now be selected for the HBT. The Gummel-Poon model is typically only used in non-critical components where simulation speed is essential (low-frequency digital design). For all of the designs in this thesis, the HICUM model is used because it offers a more realistic view of the device performance, modeling such things as the collector-base avalanche current that leads to collector-emitter breakdown.

[1]Sonnet 9.52, Sonnet Software Inc., North Syracuse, NY, 1986-2004
[2]HFSS 9.2, Ansoft, Pittsburg, PA, 1984-2004
[3]Momentum, Agilent Technologies, Palo Alto, CA, 1983-2004

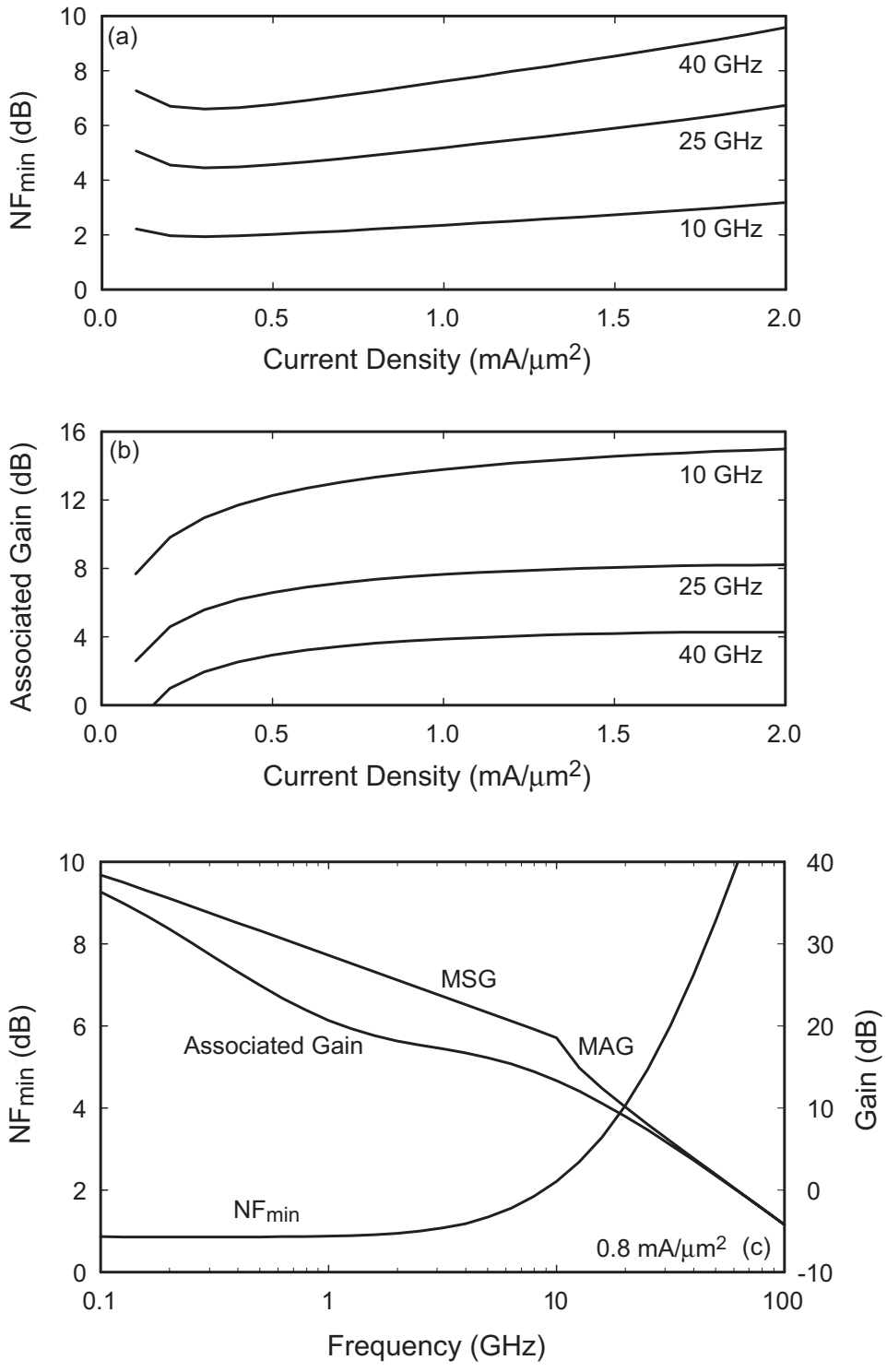



Figure 1.1: Simulation showing the performance of the the 80 GHz device over variations in current density and frequency.

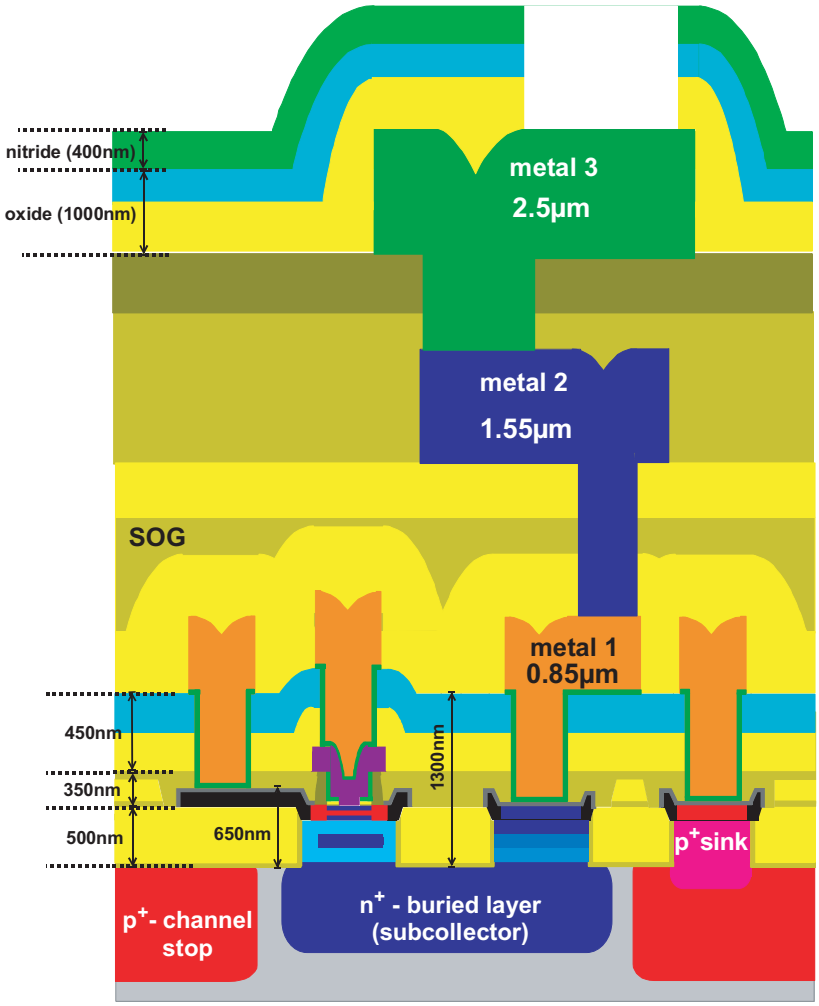



Figure 1.2: Cross section of Atmel's SiGe2-RF process.

With an ($f_t$) of 80 GHz, the transistor is usable for practical designs up to about 30 GHz. Using the HICUM model, Fig. 1.1 shows the performance of a transistor with emitter dimensions $0.5 \times 10\,\mu\text{m}^2$ over variations in current density and frequency. At 25 GHz this device can achieve a minimum noise figure ($NF_{min}$) of 4.5 dB with an associated power gain of 7 dB. At X-band the performance improves dramatically with an $NF_{min}$ of 2 dB and greater than 12 dB of associated gain. The peak $f_t$ of the device typically occurs above a current density of 1.2 mA/ $\mu$m$^2$ and then begins to fall off rapidly, therefore most designs are biased at about 0.8-1.2 mA/ $\mu$m$^2$ to avoid $f_t$ roll-off over process and temperature variation.

At RF frequencies the passive components play an important role in the performance of the overall design. The SiGe2-RF process has a three-metal stack-up (Fig. 1.2). The available capacitor is a silicon nitride capacitor with a capacitance density of 1.1 fF/ $\mu$m$^2$.

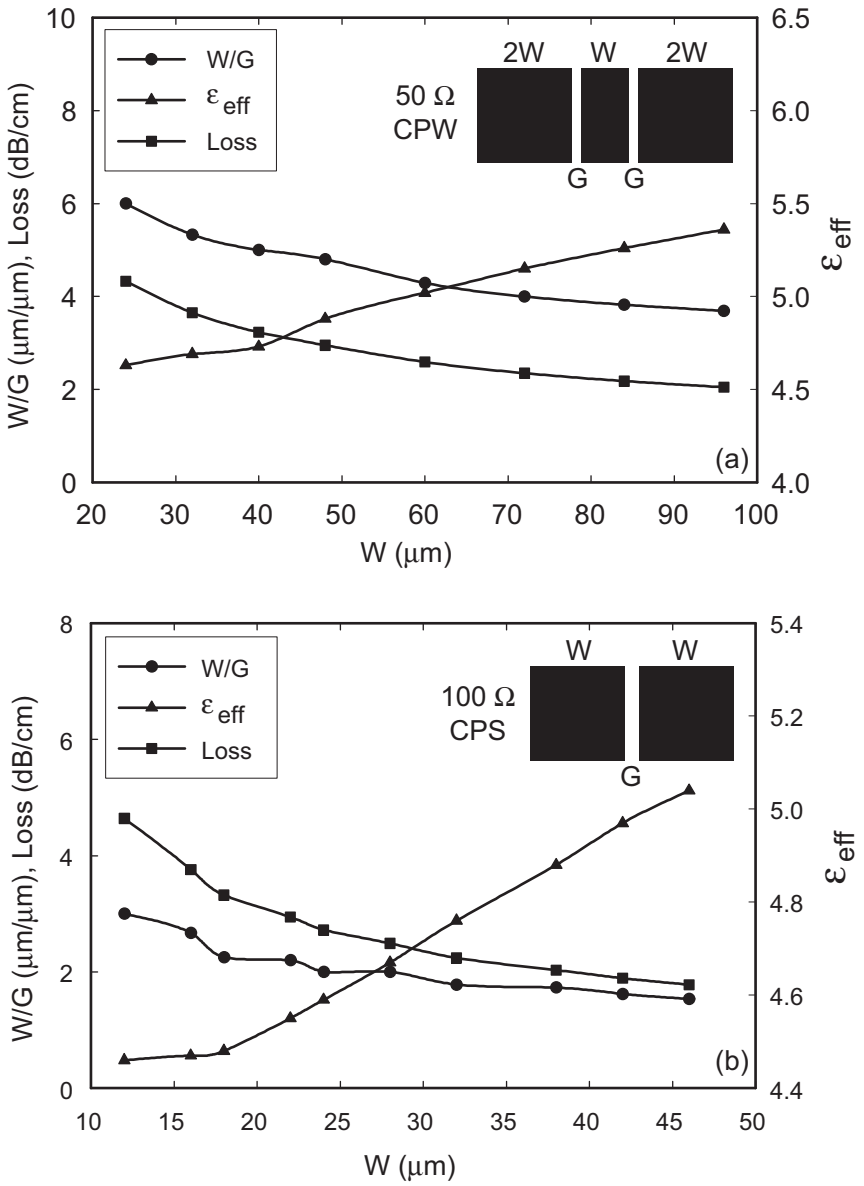



Figure 1.3: Simulations of (a) 50 Ω CPW and (b) 100 Ω CPS in the Atmel SiGe2-RF process.

Although advertised as an MIM capacitor, the bottom plate is implemented with a doped poly-silicon layer with a sheet resistance of 4 Ω/□ and a top plate implemented with metal 1. This results in mediocre capacitor performance at RF frequencies due to the series resistance and bottom plate parasitics. For small values of capacitance, a high quality capacitor can be implemented in the silicon dioxide between either metal 1 and 2 or metal 2 and 3. Although too late to be used for any designs in this thesis, by the summer of 2004 a true MIM capacitor was made available by the foundry. The structure of the capacitor has

metal 1 as the bottom plate, followed by 66 nm of silicon nitride for a capacitance density of 0.93 fF/$\mu$m$^2$. The top plate is an additional thin-film metal layer connected to metal 2 with vias.

The substrate is high resistivity-silicon (1000 $\Omega$·cm) that approximates a semi-insulating substrate which is normally only found in a III-V technology. This allows for moderately high-Q inductors and allows the use of transmission lines if necessary. For single-ended designs, coplanar waveguide (CPW) sections can be used as interconnect whereas for differential designs coplanar slot lines (CPS) are used. Fig. 1.3 shows a simulation of a 50 $\Omega$ CPW and 100 $\Omega$ CPS. It is interesting to note that the effective dielectric constant ($\varepsilon_{eff}$) is in the range of 4-5, indicating the majority of the electric field lines are contained in the silicon dioxide ($\varepsilon_{eff} = 3.9$) and not the silicon ($\varepsilon_{eff} = 11.9$). This means that the majority of the loss is due to the metal and that the high resistivity substrate is not an absolute necessity. Metal 2 and Metal 3 are 1.55 $\mu$m and 2.55 $\mu$m thick, respectively, with Metal 3 located 5.4 $\mu$m above the substrate. For the designs presented, the metal interconnect including the inductors and capacitors are simulated in Sonnet and their S-parameters are placed in ADS together with the transistor models provided by the foundry. The final layout is done in Cadence.

## 1.3 Thesis Overview

Radio Frequency Integrated Circuits (RFIC) have traditionally been defined as designs in the low gigahertz range and were typically implemented in a silicon (BJT or CMOS) process. The RFIC engineer typically approaches the design from a low frequency IC background and uses design methodology based on node voltages and currents. In contrast, Monolithic Microwave Integrated Circuits (MMIC) technology typically refers to designs at frequencies greater than a few gigahertz and are implemented using gallium arsenide (GaAs) or indium phosphide (InP) devices. The MMIC designer typically uses a methodology where distributed elements such as transmission lines are common practice, port impedances are 50 $\Omega$ and the use of power waves is more common than nodal voltages.

As SiGe and CMOS have advanced in the last five years, the distinction between RFIC and MMIC has become blurred. Silicon technology now dominates the cell phone (<2 GHz) and wireless LAN (<6 GHz) markets. Commercial and military systems at X- and K-band

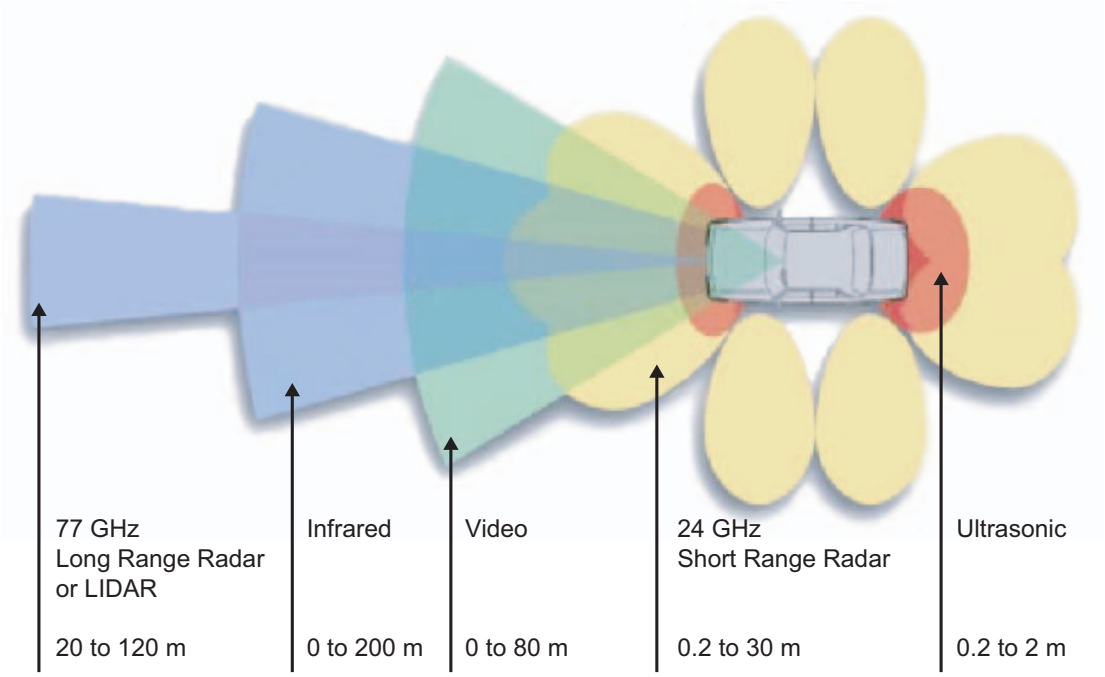



Figure 1.4: The use of different sensor technologies to improve the safety of automobiles and the ranges at which they are effective.

are being re-investigated to determine if a re-design of the system in silicon would be a better solution since due to the silicon infrastructure in the semiconductor industry, silicon is almost always a viable solution, and if not now, then in the near future. This has lead to what can be referred to as *silicon MMIC design*. These designs draw from the lower frequency RFIC techniques and also rely on the use of traditional microwave theory. In this thesis, both RFIC and MMIC techniques are used to meet the objective of demonstrating the design and analysis of high performance SiGe microwave components at frequencies in the range of 12-24 GHz.

The majority of the work in this thesis is motivated by the development of an automotive radar solution at 24 GHz [11]. In the near future automobiles will mostly likely have several sensor technologies available to them. Fig. 1.4 shows where these systems may come into play for making the automobile safer. For long range detection ($>$ 100 m), 77 GHz radar and LIDAR are available but only for very narrow beam width applications where a beam that is 2-3° wide is scanned over less than a 10° sector. To supplement the long range radar information, infrared and video solutions are available. However, optical systems suffer from two drawbacks: 1) they are significantly effected by inclement weather (fog, low visibility,

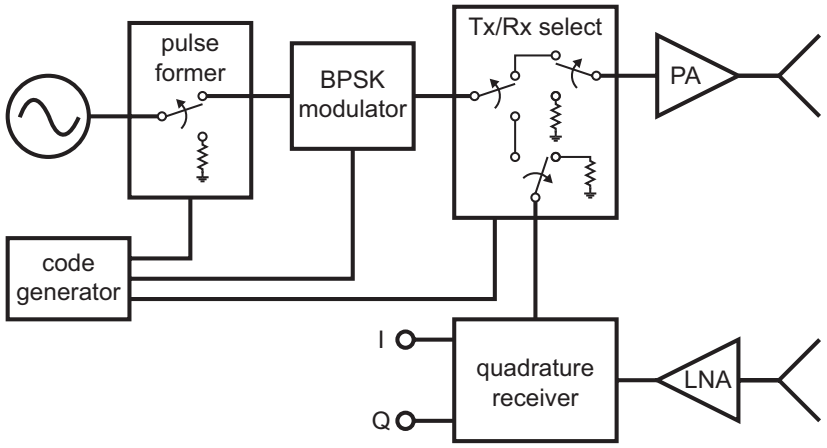



Figure 1.5: Block diagram of a 24 GHz pulsed radar chip set for automotive applications.

etc.) and 2) they must be mounted with an unobstructed view such as on the dashboard. Ultrasonic systems are available for use as parking aids but have a limited range of less than a couple of meters. To provide a solution out to 30 meters, 24 GHz radar is the technology of choice. This is advantageous for several reasons: 1) it is non-optical and can be mounted out of plain sight behind bumper fascias, 2) less susceptible to inclement weather and 3) performance will likely improve as IC device technology improves in the years to come.

A simple block diagram of a 24 GHz pulsed radar is shown in Fig. 1.5. The block diagram implements a time-domain reflectometer that is used to determine where in space/time a target is located. The output of an oscillator is pulsed to form wavelets of RF energy with pulse-widths as short as 500 ps wide. There is also the option to phase modulate long pulses with a 500 ps chip rate to maintain optimum spectral density of the radiated energy. The modulated waveform is amplified and transmitted where subsequently the energy will reflect off targets and return to the receive antenna. The radar return is then amplified and correlated with a copy of the original modulated waveform that has been delayed by time $t_1$. Once correlated, the signal is sampled and processed to determine if there is a detectable target in that particular range bin that corresponded to the time delay $t_1$. This process is then repeated for each range bin (different time delays) to fill in a complete radar range map.

Two of the key components in the radar transmitter that are addressed in this thesis are the oscillator and the RF switching circuits. The oscillator must have a tuning range large enough to overcome any process and temperature variation (7-10%) and have a high output power (4-6 dBm) to drive the subsequent electronics. The RF switching circuits are

essential to the radar working properly at close ranges and RF envelope rise-times less than 100 ps are needed. In addition there is no time for the oscillator or amplifiers to recover from any transients caused by load pulling so it is also necessary that the RF switching circuits be absorptive.

Chapter 2 starts with an overview of the design and optimization of Voltage Controlled Oscillators (VCOs) at microwave frequencies. First, background information is provided on the progression of integrated VCO designs, followed by a discussion of the cross-coupled differential pair and its use as a core oscillator topology. Next, two popular phase-noise models will be presented (Leeson and Hajimiri) to determine the sources of phase-noise as well as some mitigating strategies. Finally, the design and measurement of a 24 GHz SiGe VCO is presented including the design of a circular differential inductor for use in the LC resonator. The compact differential VCO at 22.8 GHz has an average output power of 2.2 dBm, a SSB phase-noise of -104 dBc/Hz at 1 MHz offset and a FOM of -175 dB while maintaining a small footprint of only $230 \times 290\,\mu\text{m}^2$.

Some oscillator work is continued in Appendix A where a novel superharmonic bilateral coupling topology is presented to mutually injection lock two 6 GHz oscillators together forcing the two oscillator outputs into a quadrature phase state. The QVCO was fabricated along with a single VCO for comparison. The QVCO layout is compact and occupies an area of only $810 \times 485\,\mu\text{m}^2$ without pads. Based on measurements of the VCO and QVCO, the coupling does not decrease the tuning range or increase the power consumption and the phase-noise is decreased by 3 dB as predicted by coupled-oscillator theory. The QVCO has a 24% tuning range with a maximum output frequency of 5.92 GHz and an average output power of -5.3 dBm.

In Chapter 3, the design and analysis of a SiGe differential absorptive SPDT switch topology at 24 GHz is presented. An RF envelope switching time of 70 ps is achieved through the use of differential current steering to switch the RF path. The switching time of the RF envelope is analyzed analytically and agrees well with simulated and measured results. The SPDT switch achieves 1.9 dB of gain in the pass band and an isolation of 35 dB while remaining matched at its ports (absorptive). In addition, measured results for a single-ended SPDT are presented and compared to the differential design to illustrate that the differential topology suppresses clock feed through (baseband leakage). Finally, the switching performance of the differential SPDT is measured at 7 GHz to demonstrate

the feasibility of using this topology in the 3.1-10.6 GHz UWB band for sub-nanosecond pulse formation.

Chapter 4 presents the design and measurement of a 12 GHz phase shifter with integrated LNA in SiGe. A digital 180° phase shift is integrated into the LNA using a switched high-pass/low-pass network. The remaining phase shift is achieved with an analog phase shifter using varactors that implements a novel *constant-impedance* tuning technique which tunes the phase while simultaneously compensating for mismatch introduced by the variable load capacitance. The phase shifter has a measured gain of $3.7 \pm 0.5$ dB at 11.5 GHz with a noise figure of 4.4 dB. The phase shifter has more than 360° of phase shift and the relative phase shift is flat with frequency within ±10° over more than 1 GHz of bandwidth centered at 11.5 GHz. The analog control lines for individual phase shifter cells were adjusted independently to demonstrate that a 4-bit digital phase shifter could also be implemented with good performance.

A phase shifter with topology similar to the design in Chapter 4 was implemented differentially at 24 GHz in Appendix B. The differential topology allows the use of a Gilbert cell as the 180°-bit since a wire-inversion is equivalent to a 180° phase shift in a differential circuit. The remaining 180° is implemented using the *constant-impedance* tuning technique introduced in Chapter 4. The design is presented with simulations results as well as some measured results. The measured design did not perform as expected and reasons for the degradation in performance is provided.

Chapter 5 concludes the thesis with a summary of the work presented as well as some future work for applications at X and K-band using both SiGe and CMOS together in an advanced BiCMOS process.

# CHAPTER 2

# Fully Integrated SiGe Voltage Controlled Oscillator (VCO) Design at K-band Frequencies

## 2.1 Introduction

Voltage controlled oscillators (VCOs) are a key component in RF systems and it has only been in the last decade that fully integrated VCOs have become a reality using silicon technology. While ring and relaxation oscillators could be implemented in silicon, they do not meet the stringent phase noise requirements of communication systems. Fully integrated low phase noise VCOs require on-chip implementation of LC tanks or transmission line resonators and for many years were exclusively available only in III-V technologies due to the semi-insulating substrate.

The stringent phase noise requirements of mobile communications would mean that the VCO would be the limiting component in realizing a fully integrated transceiver (outside of the final power amplifier). The first fully integrated VCO in silicon was presented in 1992 at 1.8 GHz using a modified Colpitts topology and interpolative tuning with two slightly mistuned LC resonators to increase the tuning range [12]. The low inductor quality factor (Q=5) and large number of transistors in the signal path resulted in mediocre phase noise results (-88 dBc/Hz at 100 kHz offset). Today, VCOs are regularly implemented on-chip to realize fully integrated transmitter and receiver chips.

It was clear from the work of Leeson, published in 1966, what factors contribute to the phase noise. His work presented a simple model of a feedback oscillator and has come to be known as the Leeson equation [13].

$$\mathcal{L}(\Delta\omega) = \frac{2FkT}{P_s}\left[1 + \left(\frac{\omega_o}{2Q_L\Delta\omega}\right)^2\right] \tag{2.1}$$

where $\mathcal{L}(\Delta\omega)$ is the phase noise at an offset frequency of $\Delta\omega$, $k$ is Boltzman's constant, $T$ is the temperature, $F$ is an empirical noise factor for the active device(s), $P_s$ is the power dissipated in resonant tank, $\omega_o$ is the frequency of oscillation and $Q_L$ is the loaded quality factor of the resonator. From Leeson's simple model, it is clear that there are three main ways to reduce the phase noise: 1) increase the power dissipated in the resonator ($P_s$), 2) decrease the noise contributed by the active device(s) ($F$) and 3) increase the quality factor of the resonator ($Q_L$).

## 2.2 The Differential Negative-Resistance Cell as an Oscillator Topology

Although silicon bipolar technology was in limited use by industry for RF designs, it was the research done at universities in the area of RF CMOS that began to drive new discoveries [14]. In the area of phase noise, it was clear that the noise from the active devices could be reduced simply by reducing the number of devices in the oscillator core. In bipolar designs, it was common to generate a negative-resistance cell through positive feedback often using active buffers in the feedback path, thus increasing the device count and therefore the noise [15, 16]. In the area of integrated CMOS VCOs a simpler approach was taken. One of the first examples used a simple cross-coupled NMOS pair to implement the negative-resistance cell with a PMOS tail current source to providing bias current through on-chip spiral inductors [17]. There are many variations on this topology that use cross-coupled NMOS or PMOS or both, with and without tail current sources, and each have their own trade-offs. The advantages of this topology are that it is relatively simple to implement, is self-biased at the gate, and allows a large voltage swing at the drains of the CMOS FETs.

When active buffers are used in the feedback path of a bipolar negative-resistance cell, they also provide a DC level shift to allow a large voltage swing at the collectors of the BJTs. When the buffers are removed to reduce the noise, a simple cross-coupled differential pair is left just as in CMOS (Fig. 2.1a). Neglecting the transistor parasitics and assuming $\beta$ is large, the input impedance of the negative-resistance cell is

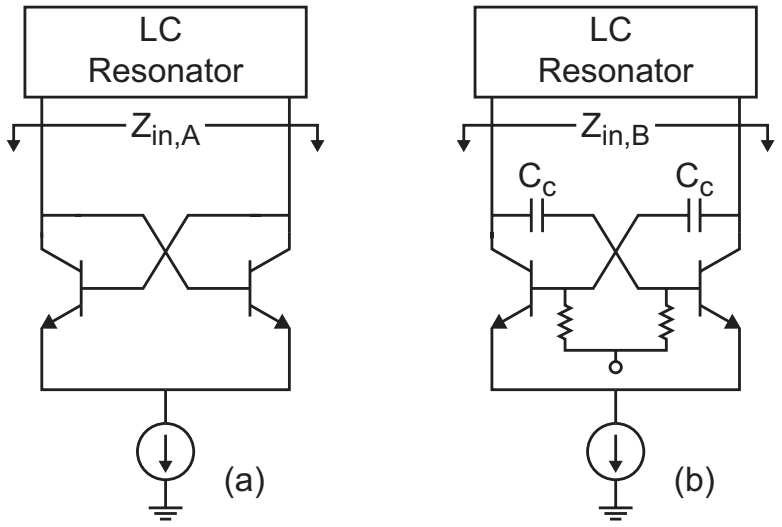



Figure 2.1: The cross-coupled differential pair for use as a negative resistance cell in oscillator design, (a) DC cross-coupling, (b) AC cross-coupling.

$$Z_{in,A} = -\frac{2}{g_m} \Bigg\| \frac{2}{j\omega C_\pi}. \tag{2.2}$$

This bipolar implementation has several drawbacks: 1) the negative resistance is determined entirely by the collector bias current making it difficult to simultaneously optimize the loop-gain and swing, 2) the capacitance $C_\pi$ is directly in parallel with the LC tank and can limit the operating frequency and 3) the two transistors are DC cross-coupled resulting in the swing at the the collector limited to approximately 400 mV before the transistors saturate during a portion of the swing. In general, this should be avoided due to the degradation in performance of a saturated bipolar device.

The bipolar cross-coupled differential pair can be improved by using a capacitive divider in the feedback path (Fig. 2.1b) [18]. Using this configuration, the input impedance of the negative-resistance cell becomes

$$Z_{in,B} = \left( -\frac{2}{g_m A_c} \Bigg\| \frac{2}{j\omega C_\pi A_c} \right), \tag{2.3}$$

where $A_c$ is the capacitance division ratio,

$$A_c = \frac{C_c}{C_c + C_\pi}. \tag{2.4}$$

This has several advantages over the DC cross-coupled differential pair: 1) with the base voltage chosen properly, the voltage swing is only limited by the collector-emitter

breakdown voltage ($V_{CEBO}$) that is 2-5 V in a modern SiGe device, and 2) adjusting the value of $C_c$ can be used to trade off loop-gain for reduced capacitance at the output node. Unlike CMOS, once the collector bias current is chosen, the transconductance ($g_m$) of the device is fixed. Using the capacitive divider in the feedback path allows the designer to reduce the loop gain from a value that may be excessive to one which is just sufficient for oscillator start-up, while at the same time maintaining a large bias current for improved phase noise and output power. The capacitively cross-coupled bipolar differential pair is the basis for the designs in this chapter.

## 2.3 Phase Noise Optimization

When the resonator is off-chip, whether it is implemented with a microwave resonator ($\lambda/2$ line, dielectric puck, cavity) or with an LC tank at lower frequencies, the quality factor can be quite high (100-10,000) and the effect of $P_s$ and $F$ in (2.1) are less of a concern. As the mid to late 1990's saw more low-Q LC resonators integrated on-chip, increasing $P_s$ and decreasing $F$ became more important to reducing phase noise and spawned a great deal of research to optimize the phase noise of fully integrated LC oscillators.

Although Leeson's equation (2.1) is helpful in understanding some of the trade-offs in oscillator design, it is difficult to calculate the phase noise without knowing the the excess noise factor ($F$) of the active device *a priori*. The model presented by Leeson (and later others) [13, 19], made an important assumption that the once the oscillator reaches steady-state it can be modeled as a linear time-invariant (LTI) system. This simply means that the active amplifying device is considered linear and the total noise contributed by the combination of the active device(s) and the resistive losses at the frequency of oscillation ($\omega_o$) are simply shaped by the high-Q feedback network transfer function. This ignores the up-conversion of low frequency $1/f$ noise as well as noise in bands harmonically related to the fundamental frequency of oscillation. Although it was understood that these noise sources created phase noise, their contribution was often lumped into the excess noise factor ($F$) for a given oscillator topology.

The work of Hajimiri and Lee proposed a more general phase noise model that lifted the assumption of an LTI system [20]. Their model is linear time-variant (LTV) because the conversion of noise to phase noise is dependent on when the noise is injected into the

oscillation period. This is easily understood by considering the analogy of a child on a swing. The swing moves back and forth in an oscillatory fashion and the child imparts an impulse of energy into the oscillation by pumping his legs at specific times. This pumping is akin to the energy in an electronic oscillator needed to sustain oscillation. If the child kicks his legs at the peaks of his swing, the amplitude is altered but he continues to swing at the same frequency. The child quickly learns to keep his legs straight and together as they swing past the zero-crossing of his oscillation when the swing is closest to the ground. If the child were to kick his legs as he passed the zero-crossing, his speed would be significantly altered by that impulse of energy. The same is true in an electronic oscillator: there are times during the oscillation's period when it is more sensitive to an impulsive perturbation. This was recognized by Hajimiri and Lee and resulted in the introduction of what they called the Impulse Sensitivity Function (ISF). This is a periodic function that describes how sensitive the phase of an ideal oscillation is to an impulsive input. Each noise source has its own ISF, and the ISF is the transfer function that determines how that noise source is converted to phase noise at the output node of the oscillator.

The ISF is readily obtained through a SPICE level simulation, and if all of the noise sources are known, then the phase noise can be directly calculated. Fortunately, the ISF is periodic and can be decomposed into Fourier series so that the phase noise analysis can be done in the frequency domain. This directly results in the noise at frequencies harmonically related to the frequency of oscillation ($n\omega_o$) being converted to phase noise proportional to the appropriate Fourier coefficient that describe the the ISF. Also, oscillators are inherently non-linear resulting in some of the noise sources being cyclostationary. A cyclostationary process can be represented by $i_n(t) = i_{n0}(t) \cdot \alpha(\omega_0 t)$, where $i_{n0}(t)$ is a stationary process (white or colored), while $\alpha(\omega_0 t)$ is a periodic deterministic function. The deterministic function $\alpha(\omega_0 t)$ can be multiplied by the ISF to get an effective ISF for that particular cyclostationary noise source.

With this improved understanding, effort was put into reducing the phase noise of fully-integrated oscillators to make them acceptable for mobile communication applications. For the bipolar cross-coupled differential pair topology (Fig. 2.1b) and the CMOS equivalent, phase noise is contributed by three sources: 1) the resistive losses in the LC resonator, 2) the noise from the differential pair transistors and 3) the noise injected by the current source. In a bipolar implementation the noise due to the differential pair is dominated by the shot

noise of the device and the base resistance. The shot noise ($2Iq$) is directly proportional to the bias current while the power dissipated in the resonator is proportional to $I^2$, and thus increasing the bias current will decrease the effect of the shot noise component of the noise to carrier ratio in the transistor[1]. Reducing the base resistance will also decrease the noise contribution of the differential pair but the circuit designer can only do this by increasing the number of base fingers for the device. This has the effect of increasing the base-collector and base-emitter junction capacitance and will result in a trade-off with the frequency of oscillation or the tuning range.

The noise of the bias current source at the emitters of the differential pair translates to phase noise through several mechanisms and can be analyzed in two different ways: 1) The ISF which characterizes the tail current noise source can be used to calculate its contribution directly [21]. 2) More intuitively, the cross-coupled differential pair and transistor current source can be viewed as a single balanced mixer where the noise of the current source mixes with the fundamental frequency of oscillation. The noise in the current source at $f_o$ is down-converted to baseband and up-converted to $2f_o$, both of which are rejected by the bandpass response of the LC resonator. However, the noise in the current source at $2f_o$ is down converted to the frequency of oscillation [22]. Half of this noise power is AM noise and half is PM noise that directly contributes to the phase noise. Similarly, the baseband noise in the current source is up-converted into AM sidebands around the frequency of oscillation. This AM noise, in conjunction with the down-converted AM noise from $2f_o$, can undergo AM-PM conversion by way of any mechanism which changes the phase of the oscillation through amplitude variation by means of the nonlinear C-V characteristics of tuning varactors and the base-collector junction capacitance of the bipolar transistor [22, 23]. Furthermore, the baseband noise from the current source can modulate the bias point of the differential pair resulting in a an FM modulation which also appears as phase noise [23, 24].

Several approaches have been used to mitigate the effect of the noise in the transistor current source. The first technique focuses on eliminating the noise at $2f_o$ that is down-converted to the frequency of oscillation. This is done by filtering the tail current using a low-pass filter (Fig. 2.2) [22, 23]. A capacitor can be placed in parallel with the current

[1]This is only true when the oscillator is operating in current-limited regime and will be discussed in more detail in Section 2.5.

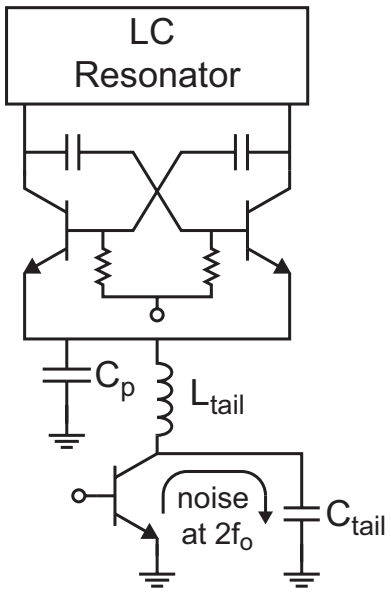



Figure 2.2: Tail current noise filter for reduction of injected noise at $2f_o$ or baseband noise if $C_{tail}$ is large and off-chip.

source and thus eliminating the noise at $2f_o$ and an inductor is placed in series with the current source and designed to resonate with parasitics ($C_p$) at $2f_o$ to present the differential pair with a high-impedance at the second harmonic. This however can only eliminate the noise at $2f_o$ because of the on-chip size limitations of $C_{tail}$. If off-chip filtering is permitted, $C_{tail}$ can be made very large to reduce the baseband noise contribution [25]. If the baseband noise is not filtered, then the AM-PM conversion must be reduced. This can be done by linearizing the varactor used for tuning and is typically done with a fixed capacitor in series with the varactor at the expense of reduced tuning range [23]. In CMOS (or BiCMOS), a switched capacitor bank can be used for coarse tuning in parallel with a small varactor at the expense of increased tuning complexity [22].

## 2.4 Oscillator Design at Microwave Frequencies

One of the first fully integrated microwave oscillators in SiGe was published in 1996. This design was a single-ended 38 GHz oscillator implemented entirely with CPW transmission lines. It took up an astounding 1.4 mm $\times$ 2.2 mm and achieved a maximum output power of 2 dBm with a phase noise of only -55 dBc/Hz at an offset of 100 kHz. The high phase noise was presumably due to surface defects in the molecular beam epitaxy (MBE) grown

base region [26]. Although this design was very large with sub-par phase noise performance, it was an indication of the direction of microwave design in the years to come.

As the cut-off frequency of SiGe transistors began to increase, it afforded new opportunities for microwave design and researchers began investigating oscillator performance at frequencies greater than 20 GHz. With increasing frequency of oscillation, there was a need for very small inductor values and some felt that these could be better implemented with high impedance transmission line sections rather than traditional spiral layouts used at lower frequencies. Several designs used either coplanar striplines (CPS) or coplanar waveguides (CPW) to implement the inductance resulting in only moderate quality factors and/or very large layouts. Also, many of these designs took a more traditional microwave approach to oscillator design using a common-base configuration to implement a negative resistance or reflection type design [27, 28, 29, 30]. While all of these oscillators are feasible design solutions, the huge body of work on phase noise and oscillator design at low RF frequencies had not been used to optimize an oscillator at K-band frequencies. The remainder of this chapter will be devoted to the design of a fully integrated SiGe VCO at 24 GHz for automotive radar applications.

## 2.5 Circuit Design

Based on discussions with M/A-COM, the design specifications required the VCO to be compact, have a large tuning range to compensate for process variation and a high output power (4-6 dBm) to drive both the Tx and Rx paths in the radar. The capacitively cross-coupled differential pair was chosen as the topology to implement the 24 GHz SiGe voltage controlled oscillator (VCO) due to the large body of previous work at low RF frequencies. The oscillator uses emitter followers as a buffer stage to provide the required output power and the varactor diode available in the process is used for frequency tuning (Fig. 2.3).

The differential VCO design employs transistors $Q_1$ and $Q_2$ connected in a positive feedback configuration to obtain a differential negative resistance in parallel with a differential LC tank. The capacitors $C_1/C_2$ reduce the loop gain the capacitive loading at the collector nodes. The input capacitance of $Q_1$ is approximately 400 fF, thus with $C_1$=100 fF, the capacitance at each collector node from the loading of the bases is reduced to 80 fF. Due to the differential operation, this is only 40 fF in parallel with the resonator.

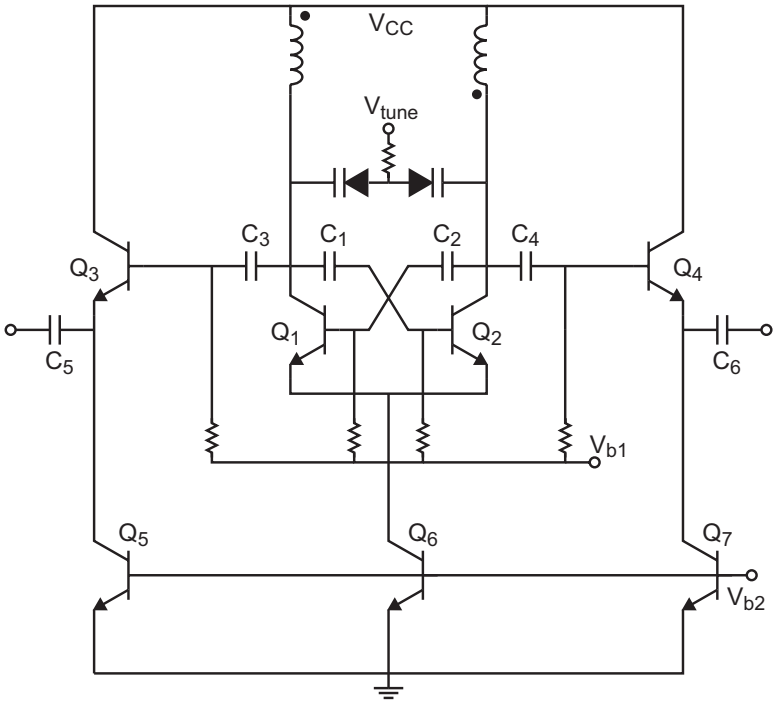



Figure 2.3: Schematic of the fully integrated 24 GHz differential SiGe VCO.

| | |
|---|---|
| $Q_1$, $Q_2$ | $11\,\mu\text{m} \times 0.5\,\mu\text{m}$ |
| $Q_3$, $Q_4$ | $10\,\mu\text{m} \times 0.5\,\mu\text{m} \times 2$ |
| Varactor | C=255-150 fF<br>Q=16-20 |
| $C_1$, $C_2$ | 100 fF |
| $C_3$, $C_4$ | 250 fF |

Table 2.1: Component values used in the 24 GHz VCO design.

The capacitors $C_3$, $C_4$ are DC blocks but also play an important role in determining the output coupling to the buffers. Because of the reduced transistor gain at 24 GHz ($f_t/f_o \approx 3$), the emitter follower in the buffers cannot present the oscillator core with a high impedance, especially when the buffers are driving a 50 Ω load. If the value of $C_3$, $C_4$ is initially increased from a very small value, the output power will begin to increase as the output coupling increases. However once the resistive portion of the input impedance of the $C_3$, $Q_3$ combination becomes comparable to the losses in the the oscillator core, the output buffers become over coupled and excessively load the VCO core. Any further increase in $C_3$, $C_4$ will reduce the output power and can only be corrected by increasing the tail current of $Q_1$, $Q_2$. Also, increasing $C_3$, $C_4$ increases the total capacitance in parallel with the LC

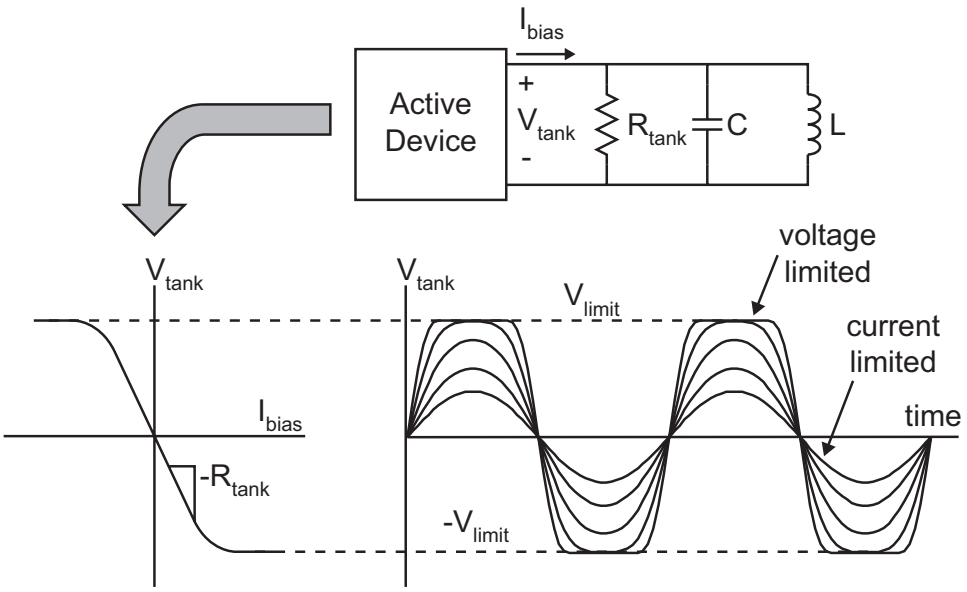



Figure 2.4: Simple model of a negative resistance oscillator.

tank and results in a trade-off of the resonant frequency, tuning range and output power.

In short, increasing the size of the transistors, capacitors and bias currents will increase the output power at the expense of reducing the oscillation frequency. Therefore, once the transistor current density was chosen, the transistor and capacitor sizes were increased to improve the output power until frequency of oscillation began to drop below 24 GHz.

The phase noise of the core VCO is optimized using the technique proposed by Ham and Hajimiri and the procedure is reviewed here for completeness [31]. The negative resistance oscillator is modeled as a lossy resonator in parallel with a non-linear negative resistance (Fig. 2.4). Assuming the tail bias current for the cross-coupled differential pair fully commutates from one side to the other, the amplitude of the voltage swing is $V_{tank} = I_{bias}R_{tank}$. Therefore increasing the bias current will increase the voltage swing and thus decrease the phase noise. The phase noise will cease to decrease when $V_{tank} = V_{limit}$ and any further increase in $I_{bias}$ will be waste of power. The voltage $V_{limit}$ is determined by the non-linearities of the active device and is not necessarily symmetric about the x-axis. For the bipolar cross-coupled differential pair this non-linearity is caused by the onset of saturation during a portion of the voltage swing when the base-collector junction becomes forward biased. This can be represented by the following equation that relates the noise-to-carrier ratio (NCR) to the design parameters inductance and bias current.

$$NCR = \frac{\langle v_n^2 \rangle}{V_{tank}^2} \propto \begin{cases} \left(L/R_{tank}^2\right)/I_{bias}^2 & \text{current limited} \\ L & \text{voltage limited} \end{cases} \tag{2.5}$$

If operating in the current limited regime, an increase in the current will decrease the NCR, however choosing the value of inductance is not as clear. Typically for large spiral inductors the Q decreases as the inductance increases, this results in the expression $L/R_{tank}^2$ increasing with for an increase in inductance. However at microwave frequencies where very small inductors are used, the opposite is true and $L/R_{tank}^2$ decreases with increasing inductance. Illustrated in Fig. 2.5, it is clear if the inductance is too large the oscillator will operate in the voltage limited regime and if the inductance is too small, the Q will be very poor resulting in not enough loop gain to start-up oscillation. Choosing a value of inductance that places the oscillator at the boundary between the current limited and voltage limited operation optimizes the phase noise.

To increase the frequency of operation or the tuning range it is necessary to decrease the tank inductance which is in contradiction to optimizing the phase noise. However, increasing $I_{bias}$ will tend to shift the curve in Fig. 2.5c to the left and thus allow for a smaller inductor to be used. The current can be increased and the inductances decreased in an iterative fashion to achieve the desired result. However this is a technique of diminishing returns because eventually $L/R_{tank}^2$ will begin to increase faster than $I_{bias}^2$ thus increasing the phase noise and rendering the loop gain marginal for start-up. In this design the the inductance was reduced to increase the frequency of operation and the tuning range while maintaining a loop gain of about 3 for start-up. The loop gain was estimated with an approximate hand calculation and the oscillator was observed to start-up in a reasonable amount of time ($< 10$ ns) in a transient simulation.

The VCO tuning is achieved with the use of a reverse-biased varactor diode formed from a base-collector junction with an additional processing step to optimize varactor performance. Due to the poor performance of the MIM capacitor in this process, the varactor was DC-coupled to the tank to eliminate the additional loss and parasitic capacitance that is associated with using a series coupling capacitor. The varactor is a single finger device with dimensions of $10\,\mu$m wide and $25\,\mu$m long. This results in a capacitance ratio of about 1.7:1 with an approximate minimum capacitance of 150 fF and a Q in the range of 16-20 at 24 GHz.

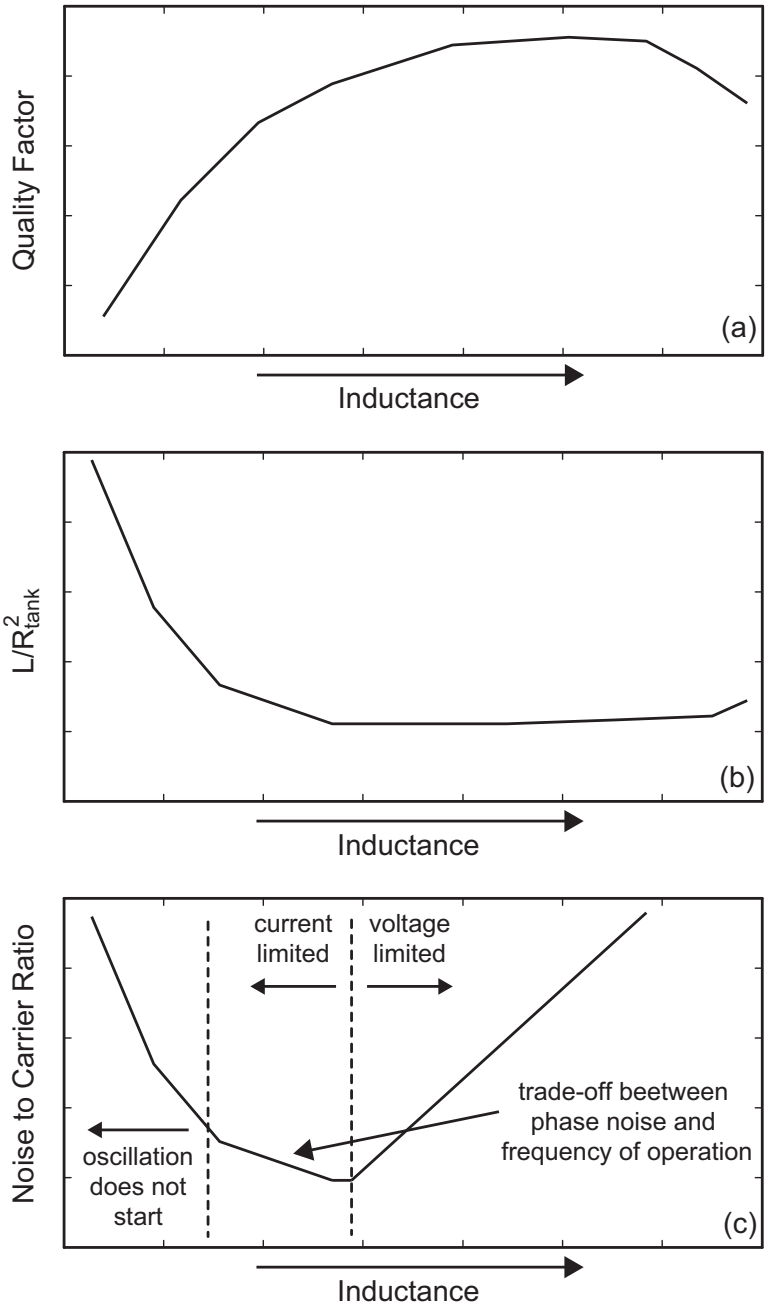



Figure 2.5: Effect of an increase in tank inductance on (a) inductor Q, (b) $L/R_{tank}^2$ and (c) noise-to-carrier ratio.

## 2.6 Differential Inductor Design

The inductor was implemented differentially and provides advantages over its single-ended counterpart (Fig. 2.6) [32]. The layouts use a conductor width of 8 $\mu$m and an inner diameter of 32 $\mu$m with the arrows indicating the direction of current flow for a differential

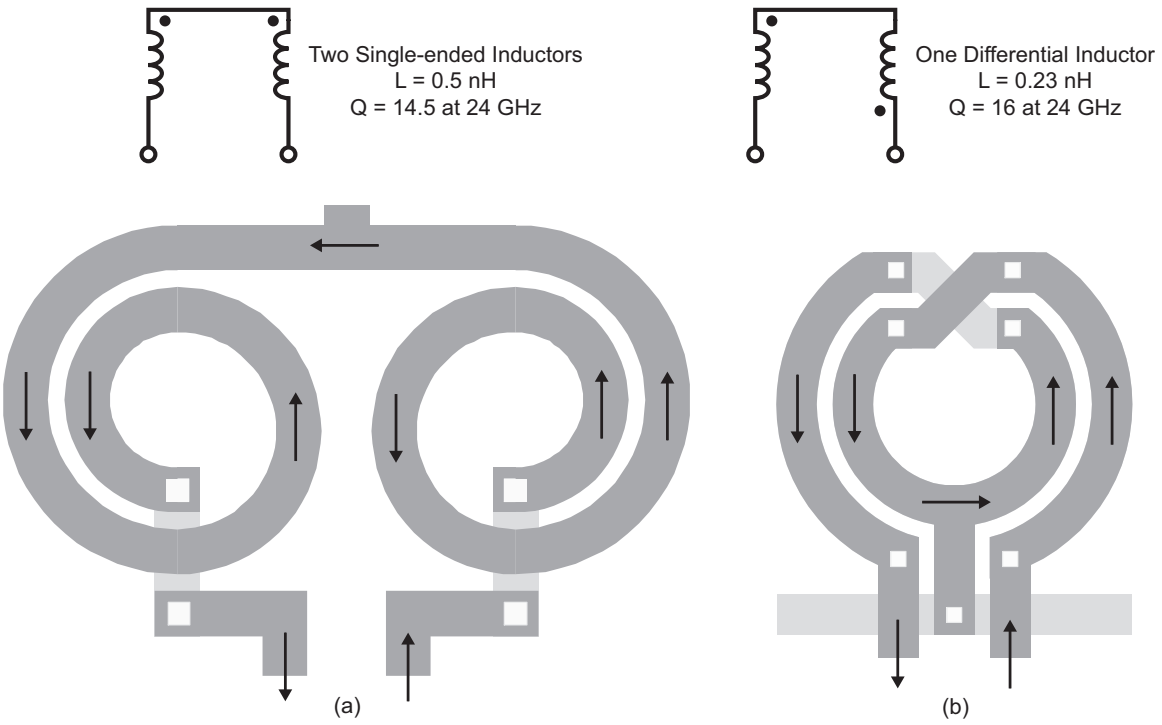



Figure 2.6: Comparison between (a) two single-ended inductors and (b) one differential inductor with the same conductor width and inner diameter.

excitation. In the case of two single-ended inductors, care must be taken with regard to the spacing between the two inductors. As the two independent inductors are moved closer to each other, the inner windings begin to couple out of phase as indicated by the opposite direction of the currents. This will result in a negative mutual coupling and thus reduce the overall inductance and quality factor. When using the differential inductor, the coupling between the turns is always positive, leading to an increase in inductance and quality factor.

Also, as the required inductance decreases, the interconnect between the two single-ended inductors can add a significant amount of unwanted inductance and resistance. This interconnect is inherently included in the differential layout, improving the performance and resulting in a reduced area. While the differential inductor topology can improve the quality factor over two single-ended inductors, the differential structure also allows the designer to reduce the inductance while maintaining the same quality factor. As was done here, more than a 2:1 decrease (0.5 nH to 0.23 nH) in inductance was achieved while increasing the Q slightly (14.5 to 16).

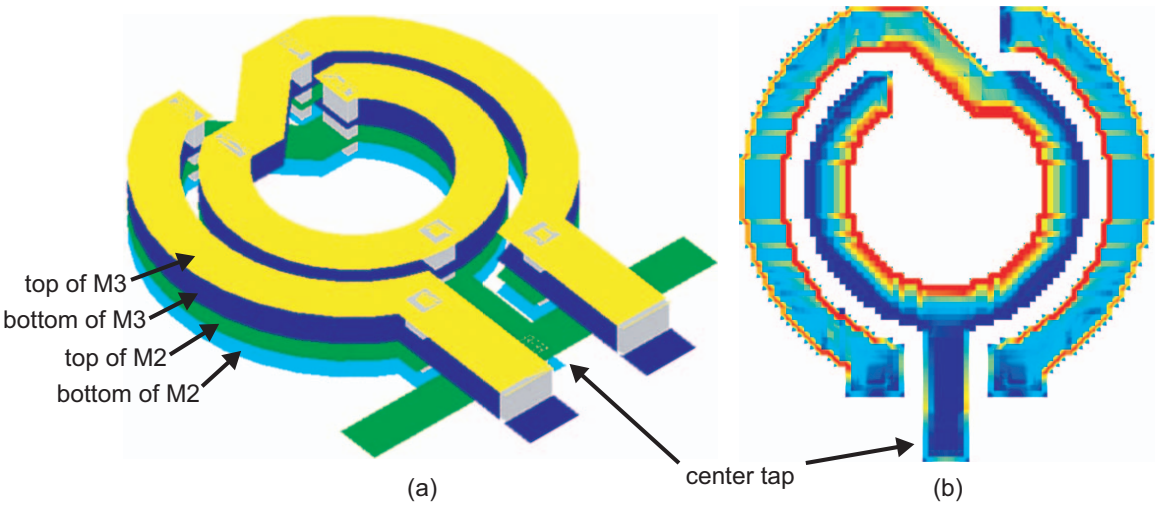



Figure 2.7: Differential inductor, (a) 3D rendering showing the use of the thick metal approximation and (b) the current density on one of the windings.

The inductor in Fig. 2.6b is the topology used in the 24 GHz VCO. The windings are implemented in both metal 3 and metal 2 connected with vias at the endpoints near the crossovers to reduce the series resistance with only a small increase in the inter-winding capacitance. The inductor is simulated in Sonnet using a thick metal approximation where the top and bottom of each metal layer is represented by a zero-thickness conductor with twice the sheet resistance [2].

Fig. 2.7a shows a 3D rendering of the inductor where the four metal layers can be clearly seen. The metal beyond the center tap has no effect on the inductance when excited differentially. This can be seen in Fig. 2.7b by observing that there is no appreciable current density on the center tap when the inductor is under differential excitation. The center tap is where the supply voltage $V_{CC}$ is injected and is brought to both sides of the inductor to reach the $V_{CC}$ pad to maintain symmetry. Although this additional metal in series with $V_{CC}$ does not effect the differential mode operation, it can have small effect on the second harmonic. Fig. 2.8 shows the Sonnet simulation of the quality factor of the inductor in Fig. 2.7 with a self-resonant frequency above 130 GHz.

[2] All 3D-planar EM simulators model conductors as a metal layer of zero thickness. Sonnet uses the DC sheet resistance and the bulk conductivity of the metal to model the ohmic losses as a function of frequency. In IC design where metal thickness is on the same order of magnitude as the conductor width and conductor spacing, it is necessary to take into account the finite thickness of the metal. The *thick metal approximation* uses multiple layers of conductors (typically two) to model the finite metal thickness. More details on this technique can be found in the Sonnet User's Guide [33].

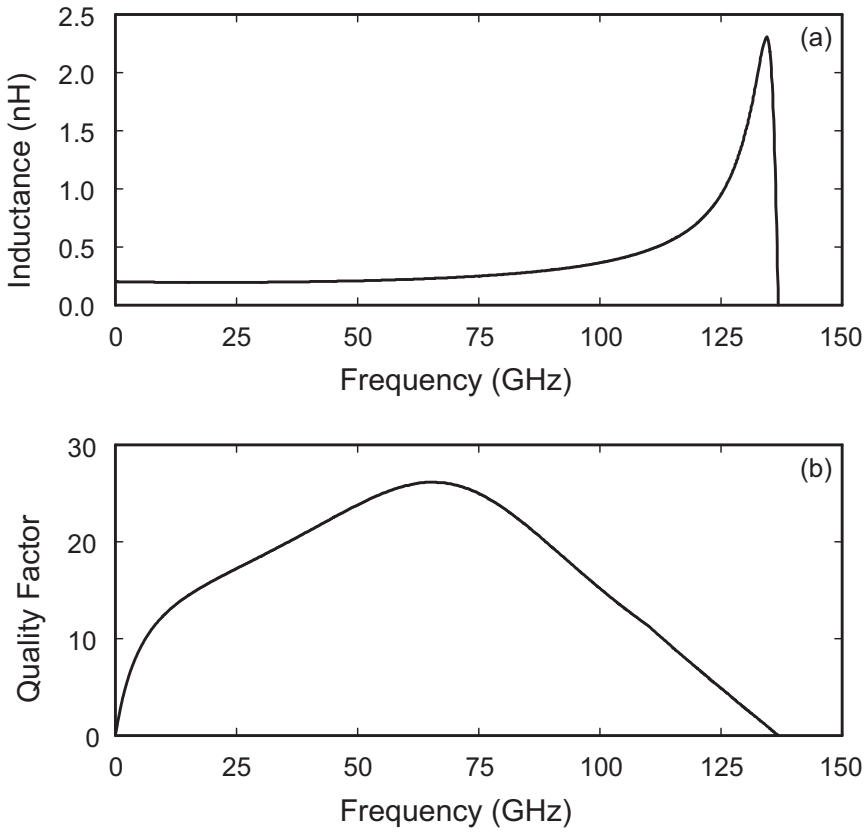



Figure 2.8: Simulated (a)inductance and (b) quality factor of differential, circular inductor ($L \approx 0.23$ nH).

## 2.7 Measured Results

The 24 GHz SiGe VCO was fabricated in Atmel's SiGe2-basic process, described in Chapter 1. Fig. 2.9 shows a micro-photograph of the circuit with dimensions of $230 \times 290\,\mu\text{m}^2$. The oscillator was measured on-wafer using a differential Picoprobe® from GGB Industries and the test setup of Fig. 2.10. The DC power and the tune voltage were supplied to the chip using RF probes to maintain good shielding of the DC voltages. The differential signal at the oscillator output was combined using a 0/180° hybrid as a balun. The single-ended output was then measured using a spectrum analyzer. Two back-to-back cable-coupler-probe assemblies were measured on a network analyzer to de-embed the loss in the power measurements with the spectrum analyzer.

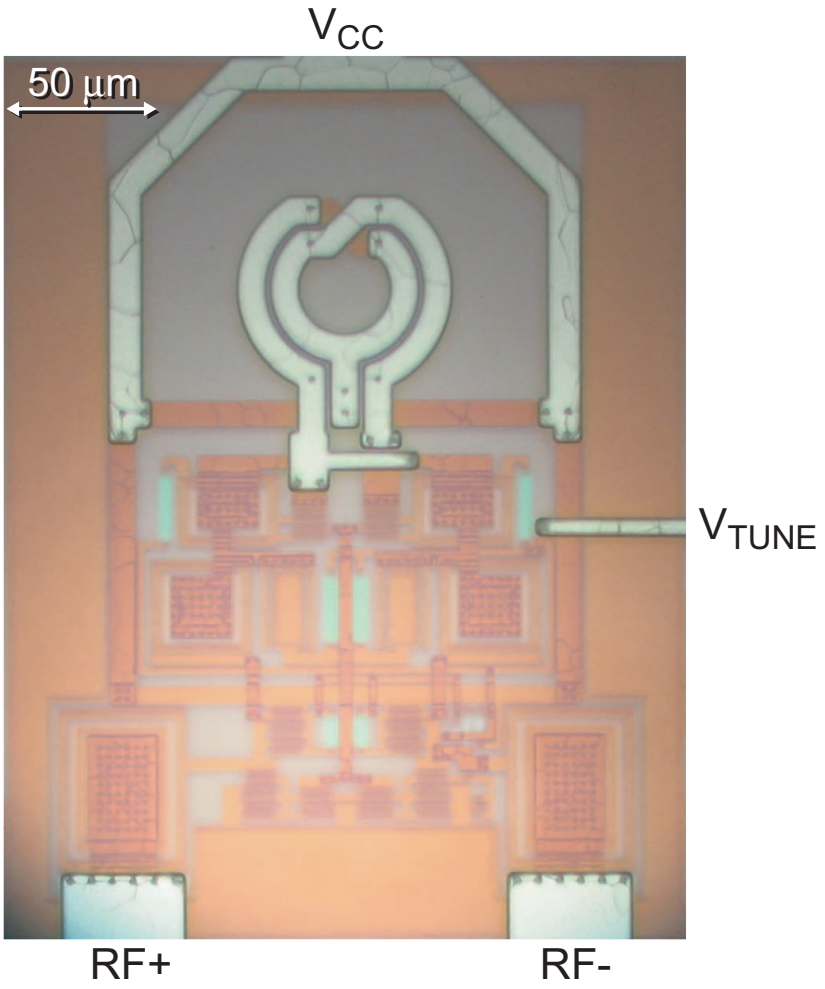



Figure 2.9: Micro-photograph of the differential VCO ($230 \times 290\,\mu\text{m}^2$).

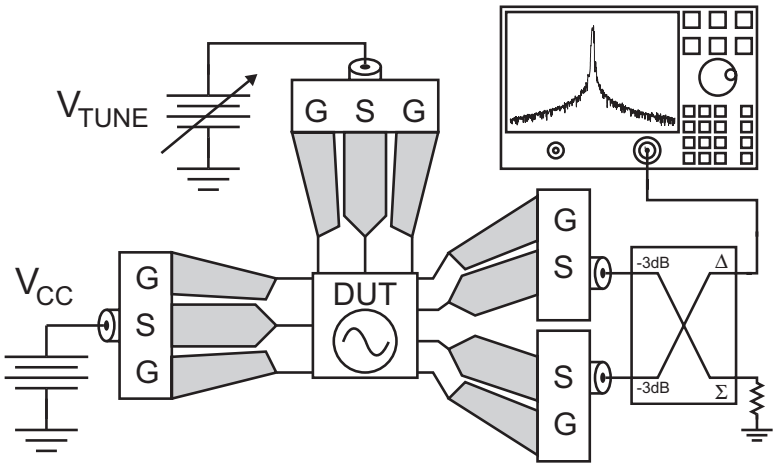



Figure 2.10: Test setup for on-wafer measurement of monolithic SiGe VCO.

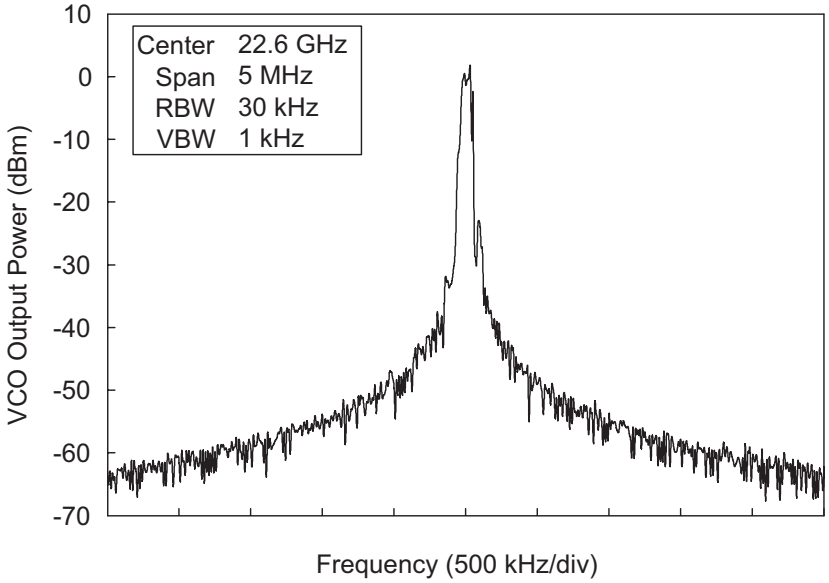



Figure 2.11: Measured output spectrum of 24 GHz differential VCO.

The VCO was designed for a 3.5 V supply voltage and the average measured current for three samples was 33.9 mA which is only 1.2% higher than the simulated results of 33.5 mA. Based on simulation results, this indicates that the oscillator core uses approximately 12 mA while the buffer amplifier uses 22 mA. Although the VCO was designed for 24 GHz, the SiGe2basic process was in development and the transistor and varactor models were still preliminary. This resulted in a 5.1% shift in the carrier frequency to 22.8 GHz, and can be easily fixed in the second design iteration.

The VCO was designed for a 3.5 V supply voltage because care must be taken not to exceed the collector-emitter breakdown voltage ($V_{CEBO}$) of 2.5 V, but the varactor can withstand a much higher reverse bias, in excess of 10 V. Because of this, the tuning characteristic was measured over a 5 V range, requiring a negative tune voltage for a portion of the tuning range since the cathode of the varactor diode is connected to the 3.5 V $V_{CC}$. Fig. 2.12 shows the tuning characteristics of three samples of the VCO. The tuning linearity is limited by the non-optimum grading coefficient of the varactor diode, however, there is more than 3 V of linear tune range with an approximate tune constant of 150 MHz/Volt. The average output power over the linear tune range, when corrected for cable and coupler loss, is 2.2 dBm with a variation of less than ±0.6 dBm over the tune range and a variation between samples of less than ±0.6 dBm.

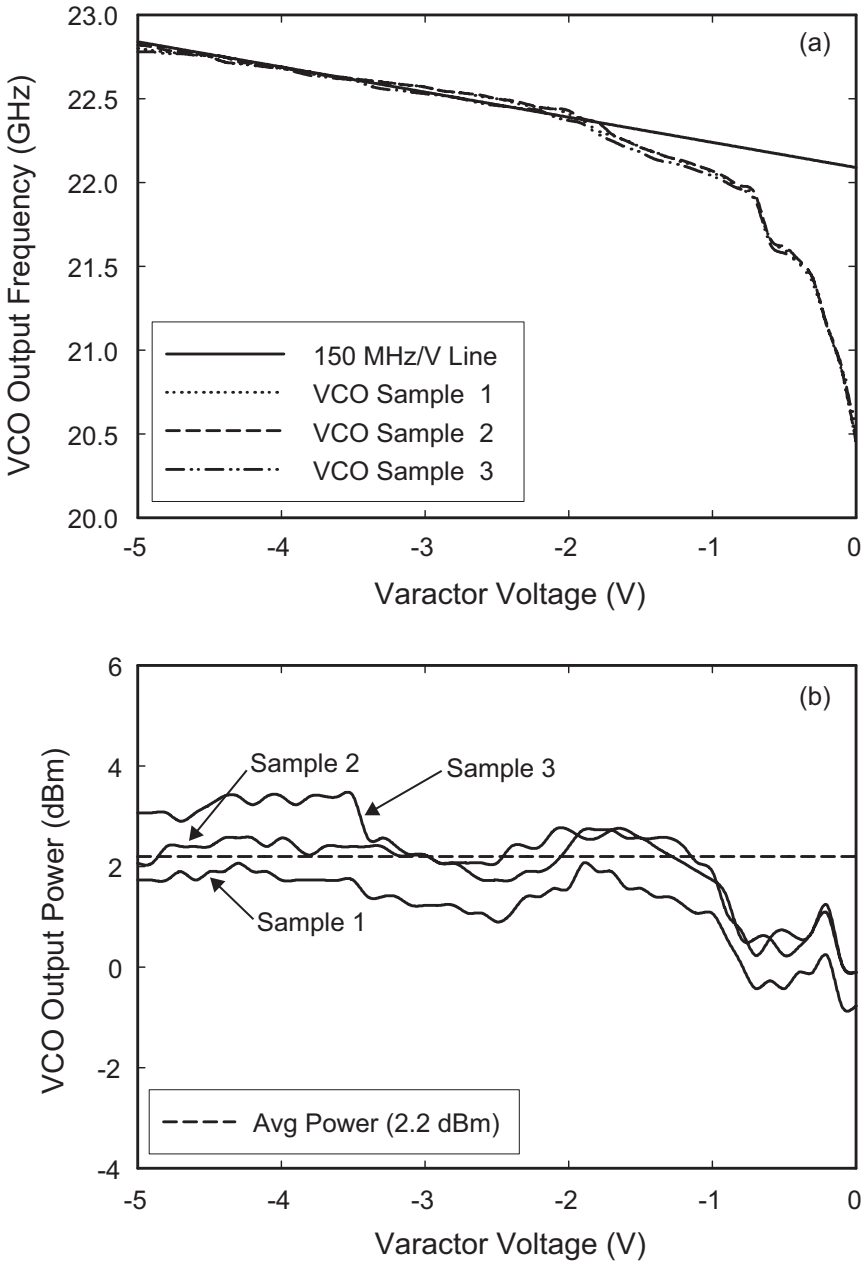



Figure 2.12: Measured tuning characteristic of the 24 GHz differential VCO for three samples: (a) frequency, (b) output power.

For this varactor-tuned resonator, as the tune voltage is increased, there is a decrease in the reverse bias of the varactor diode and the Q of the tank decreases ($V_{varactor} > -1.5$ V). This results in a degradation in the phase noise and output power, and this region of operation should be avoided. In addition to this, baseband noise from the current source may be undergoing AM-PM conversion as the varactor becomes more non-linear. The phase

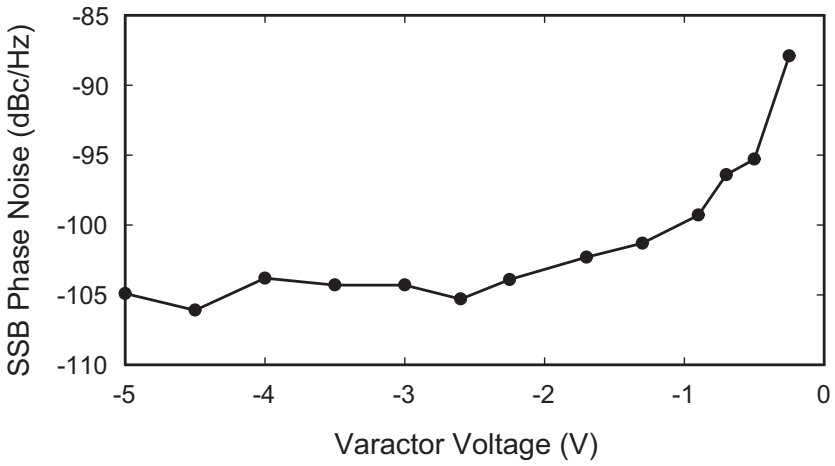



Figure 2.13: Measured SSB phase noise at 1 MHz offset for Sample 1.

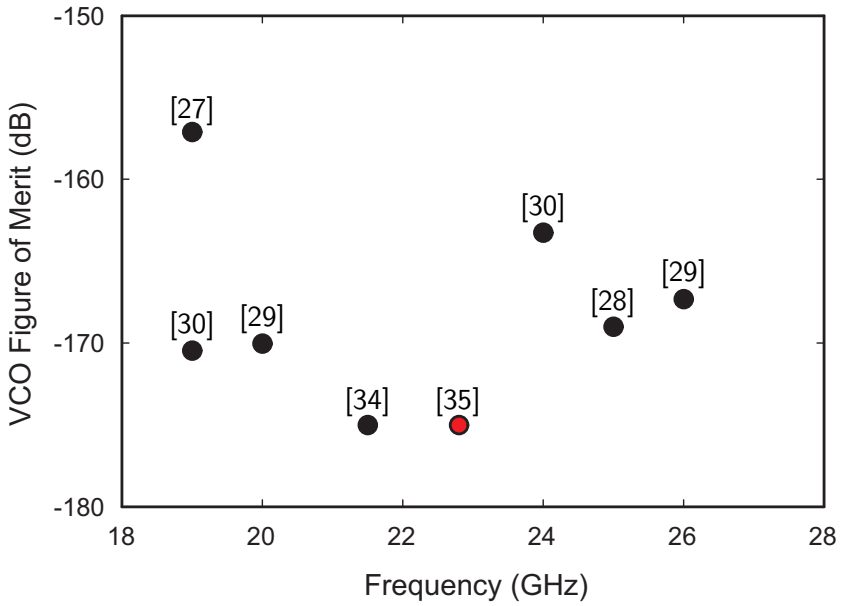



Figure 2.14: Comparison of K-band VCO figure of merits

noise was measured using an Agilent 8564E spectrum analyzer and has an average value over the linear tune range of -104 dBc/Hz at 1 MHz offset from the carrier. This agrees well with the simulated phase noise of -104 dBc/Hz in Spectre® RF for a 24 GHz carrier. Fig. 2.13 shows the variation in the phase noise as the tune voltage is adjusted. The figure of merit for the VCO is -175 dB and is calculated according to the expression [36]

$$FOM = 10\log\left(\left(\frac{f_c}{\Delta f}\right)^2 \frac{1}{\mathcal{L}(\Delta f)\, P_{core}}\right) \tag{2.6}$$

where $f_c$ is the frequency of oscillation, $\Delta f$ is the offset frequency and $P_{core}$ is the power

| | Year | $f_{max}$ [GHz] | $f_o$ [GHz] | $P_{out}$ [dBm] | $L_{SSB}$ at 1 MHz [dBc/Hz] | Size (no pads) [mm$^2$] | VCO Core DC Power [mW] | FOM [dB] |
|---|---|---|---|---|---|---|---|---|
| Ettinger [27] | 2000 | 75 | 19 | 0 | -85 | 0.230$^\dagger$ | 21 | -157 |
| Ettinger [30] | 2002 | 75 | 24 | 0 | -89 | 0.104$^\dagger$ | 22 | -163 |
| Voinigescu [29] | 2000 | 75 | 26 | 0 | -96 | 0.041$^\dagger$ | 50 | -167 |
| $^*$Kuhnert [28] | 2001 | 85 | 25 | 4.2 | -101 | 0.680$^\dagger$ | 90 | -169 |
| Voinigescu [29] | 2000 | 75 | 20 | 0 | -101 | 0.041$^\dagger$ | 50 | -170 |
| Ettinger [30] | 2002 | 75 | 19 | 0 | -100 | 0.054$^\dagger$ | 32 | -170 |
| Bao [34] | 2004 | 90 | 21.5 | -6 | -110 | 0.099$^\dagger$ | 130 | -175 |
| **This Work** [35] | **2003** | **90** | **23** | **2.2** | **-104** | **0.067** | **42** | **-175** |

$^*$not tunable $^\dagger$estimated from published micro-photograph

Table 2.2: Comparison of K-band monolithic SiGe VCOs.

dissipated in the oscillator core in milliwatts. This design has good output power, low phase noise and FOM. A comparison of recent results is listed in Table 2.2 and Fig. 2.14.

## 2.8 Improvements to Current Design

The biggest improvement to this design comes with the improvement of the process. The original MIM capacitors that were available used a polysilicon layer for the bottom plate of the capacitor (4 $\Omega/\square$). The new MIM capacitor described in Chapter 1 performs much better and preliminary simulations indicate that by simply substituting the new capacitors the output power is increased by 3-4 dB.

In this design the varactor diodes are DC coupled to the LC tank to avoid using the original MIM capacitors. This results in the cathodes of the varactors being directly connected to the tank. This in itself is not necessarily bad, but the cathode of the varactor is built in the sub-collector, therefore there is a parasitic substrate diode that is in parallel with the tank. This has several effects, 1) the tuning range is reduced by the fixed reverse biased substrate diode capacitance 2) the VCO could couple in to the substrate and pick up noise/interference and translate it into phase noise and 3) the full non-linearity of the C-V curve of the varactor is seen by the tank. Changing the polarity of the varactors and ca-

pacitively coupling them to the tank shorts out the parasitic substrate diode with a virtual ground reducing the oscillators coupling to the substrate at odd harmonics. The tuning range should also be improved since the substrate diode will no longer be in parallel with the tank. Finally, the capacitive coupling will help to linearize the tuning curve.

There are three sources of phase noise in the VCO, some of which may be able to be reduced. The prime contributor of phase noise is the noise of the core devices and finite tank Q at the fundamental frequency of oscillation. The noise from the core transistors will improve with emitter scaling. As emitter widths reduce due to lithography improvements, the base resistance of the devices will decrease. The base resistance is a significant component of the noise generated in the core will continue to decrease.

Next, there is the noise contributed by the bias circuitry through the tail current source. Earlier in this chapter a filtering technique was discussed that can be used to reduce the noise contribution of the tail current source at $2f_o \approx 50$ GHz. However, this technique would most likely have little or no effect on the phase noise. Any noise at 50 GHz that appears at the base of the tail current source transistor sees virtually no gain because the $f_t$ of the device is only 60-70 GHz. Similarly, the collector shot noise that is generated internal to the current source will also be filtered by the parasitic capacitance of the output of the current source. In effect the parasitics at the output of the collector provide some noise filtering at 50 GHz.

The final noise source is the baseband noise of the bias circuitry that can be up-converted to the frequency of oscillation and undergo AM-PM conversion to become phase noise. Reducing the baseband noise can only be accomplished with a baseband filter and for this to be effective the values of capacitance would need to be implemented off-chip and is only occasionally an option. However even without baseband filtering the baseband noise may not be of much concern. It has been shown in [20, 21] that AM-PM conversion of baseband noise can be controlled by ensuring that the single-ended waveforms have a symmetric swing. For microwave oscillators operating at $f_o/f_t < 5$ with reasonably high-Q tanks and properly biased devices in the current limited regime the voltage wave forms tend to have very good single-ended symmetry, indicating there there is mostly likely only a small amount of AM-PM conversion. This has also been seen in simulation where large ideal inductors and capacitors are used to filter the tail bias current. In this case the simulated phase noise is reduced by only 1-2 dB.

## 2.9 Conclusion

This chapter has given an overview of the design and optimization of Voltage Controlled Oscillators (VCOs) at microwave frequencies. First, background information was provided on the progression of integrated VCO designs, followed by a discussion of the cross-coupled differential pair and its use as a core oscillator topology. Next, two popular phase noise models were presented (Leeson and Hajimiri) to determine the sources of phase noise as well as some mitigating strategies. Finally, the design and measurement of a 24 GHz SiGe VCO was presented including the design of a circular differential inductor for use in the LC resonator. The compact differential VCO at 22.8 GHz has an average output power of 2.2 dBm, a SSB phase noise of -104 dBc/Hz at 1 MHz offset and a FOM of -175 dB while maintaining a small footprint of only $230 \times 290\,\mu\text{m}^2$.

# CHAPTER 3

# Design and Analysis of a SiGe Differential Absorptive 70 ps RF Switch at 24 GHz

## 3.1 Introduction

Ultrawideband (UWB) technology is emerging as a potential solution for high data rate, short-range communications and high-resolution pulsed radar systems. In recent years the FCC has opened two UWB frequency bands from 3.1-10.6 GHz and 22-29 GHz that are allowing designers to pursue UWB solutions for commercial applications. The 3.1-10.6 GHz band is intended to enable Gbit communications over short distances and several system architectures are being investigated, including a pulse modulated solution [37]. The 22-29 GHz band is intended exclusively for automotive radar applications that promises high resolution ($20 \pm 5$ cm) at short ranges ($< 30$ m) [11]. For both of these applications sub-nanosecond pulse formation is required to use the allocated bandwidth efficiently and conform to the FCC spectral mask requirements.

In pulsed radar applications, pulse formation is implemented in several ways. For very high power airborne radar systems the pulse may be formed directly by turning a magnetron based oscillator on and off. High power radars use pulse widths in the microseconds range to allow for detection at distances on the order of kilometers, thus there is no need for the magnetron to turn on quickly. For low to medium power applications, an oscillator is left on all of the time and a tranmit/receive (T/R) switch is used to switch the oscillator output to a power amplifier (PA) and antenna or to a the receiver to be used in correlating the radar return. The speed at which the T/R switch changes state will determine the minimum detectible range and the range resolution. The intent here is not to review pulsed

radar system operation, however it is sufficient to say that to achieve a range resolution of $< 20$ cm for automotive applications, the pulse width must be approximately 500 ps long, requiring RF envelope rise-times less than 100 ps.

Traditionally microwave switches are implemented with PIN diodes [38, 39, 40, 41], FETs in III-V technology [42, 43, 44] and recently CMOS FETs [45, 46]. With the exception of [42], these designs switch no faster than 1-2 ns. To achieve an order of magnitude decrease in the switching time an improvement in technology is not sufficient but rather revolutionary circuit design is needed. By taking a cue from the world of high speed digital circuits and using RF design techniques an RF switching topology is presented that achieves an RF switching time of 70 ps with $> 35$ dB on/off ratio.

## 3.2 Overview of Circuit Design

Typically RF switch design consists of using either a diode or FET to implement a small resistance when turned on and a small capacitance when turned off. In a bipolar process that offers neither a PIN diode nor a FET, an alternate design topology must be considered. One advantage that BJTs have over their CMOS counterparts is their high transconductance that allows for very fast current steering. With this in mind, a novel topology was designed to use current steering to control the RF switching operation. In addition, it is necessary that the RF ports maintain a constant impedance regardless of the state of the switch (absorptive). Fig. 3.1 shows a schematic of the proposed topology.

Transistor pairs A, B, C and D are differential common-base stages where transistor pairs B and C make up the core amplifying elements of the switch. A common-base stage was chosen because of the inherently good isolation between the collector and the emitter when the transistor is off. The switching function is achieved by steering the bias current of each common base pair. When the control voltage $V_C$ is high, the tail currents are steered through transistors B$'$ and D$'$ to bias the common-base stages B and D, thus allowing the signal to pass from Port 1 to Port 2. When $V_C$ is low, the bias current is steered toward transistor pairs A and C and the signal passes from Port 1 to Port 3.

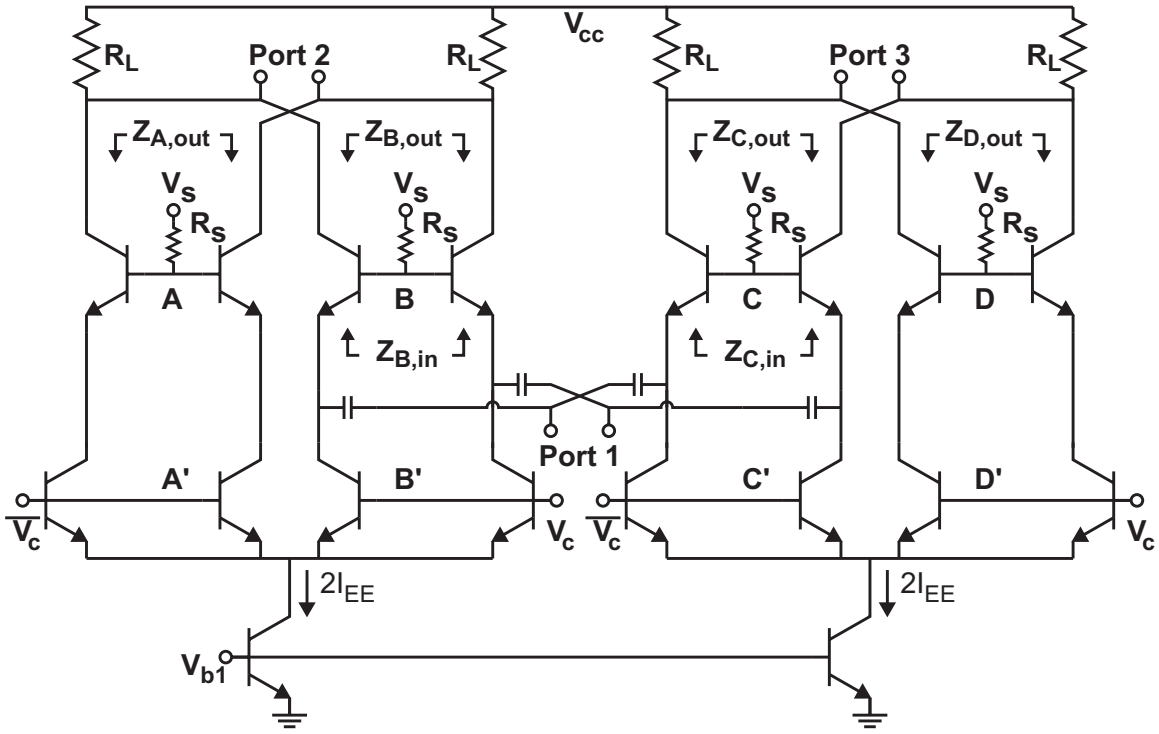



Figure 3.1: Schematic of proposed RF switching network to implement differential absorptive SPDT switch.

## 3.3 Analysis of Input and Output Port Impedances

In addition to switching very fast, this topology implements an inherently absorptive SPDT switch by maintaining a constant impedance at each of the ports regardless of the state of the switch. Assuming the DC blocking capacitors at the input are ideal RF shorts, the input impedance can be expressed as a function of bias current. When $V_C$ is high, the admittance looking into the emitters of each transistor pair B and C can be expressed as,

$$Y_{B,in} = \frac{I_{on}}{2V_T}(1 + j\omega\tau_F) + j\omega\frac{C_{je,on}}{2} \tag{3.1}$$

$$Y_{C,in} = \frac{I_{off}}{2V_T}(1 + j\omega\tau_F) + j\omega\frac{C_{je,off}}{2} \tag{3.2}$$

where $V_T$ is the thermal voltage, $\tau_F$ is the forward transit time of the transistor and $C_{je}$ is the base-emitter junction capacitance, $I_{on} \approx I_{EE}$ and $I_{off} \approx 0$. The input impedance is the parallel combination of these admittances and can be expressed as

$$Z_{in} = \left[\frac{I_{EE}}{2V_T}(1 + j\omega\tau_F) + j\omega C_{je}\right]^{-1} \tag{3.3}$$

where it has been assumed that $C_{je} \approx C_{je,off} \approx C_{je,on}$ because the difference between the $V_{BE}$ of the transistor when it is on and when it is off is small. Similarly, the output impedance of Port 2 is the parallel combination of $2R_L$, $Z_{A,out}$ and $Z_{B,out}$ such that,

$$Y_{out} = \frac{1}{2R_L} + Y_{A,out} + Y_{B,out}, \quad \text{where} \tag{3.4}$$

$$Y_{A,out} = \frac{1}{2r_{o,off}\left[1 + g_{m,off}\left(r_{\pi,off} \left\| \frac{1}{j\omega C_{\pi,off}} \right\| Z_{e,A}\right)\right]} + \frac{1}{2} j\omega \left(C_{\mu,off} + C_{cs,off}\right) \tag{3.5}$$

$$Y_{B,out} = \frac{1}{2r_{o,on}\left[1 + g_{m,on}\left(r_{\pi,on} \left\| \frac{1}{j\omega C_{\pi,on}} \right\| Z_{e,B}\right)\right]} + \frac{1}{2} j\omega \left(C_{\mu,on} + C_{cs,on}\right). \tag{3.6}$$

The impedances $Z_{e,A}$ and $Z_{e,B}$ are the impedances at the emitters of transistor pairs A and B respectively. These impedances include the parasitics associated with the collectors of transistors A′ and B′ and the impedance that the input matching network presents to transistor pair B. Transistor pair A does not have a matching network so $Z_{e,A}$ and $Z_{e,B}$ are not equal. However, the terms that contains $Z_{e,A}$ and $Z_{e,B}$ are multiplied by $r_o$ which is very large regardless of the state of the switch. This makes the first term of (3.5) and (3.6) negligible, such that the capacitances at the collectors and the load resistors dominate the overall port impedance.

Another advantage of this topology is the base and collector voltages of transistor pair A is the same as transistor pair B because of the current steering topology. This results in the parasitic capacitances at the collectors of the transistor pairs A and B being the same. Using these simplifications in (3.4)-(3.6), the output impedance of Port 2 is constant regardless of the state of the switch where,

$$Z_{out} = \left[\frac{1}{2R_L} + j\omega \left(C_{\mu} + C_{cs}\right)\right]^{-1}. \tag{3.7}$$

This transistor topology inherently implements a SPDT absorptive switch. It is absorptive at all three ports so the load or source impedance that an oscillator or power amplifier sees remains constant regardless of the state of the switch. The three ports can be matched to any characteristic impedance or if used as part of a larger monolithic system the matching can be removed and integrated with other circuits. In this design, a planar EM simulator was used to design matching networks to match all three ports to a 100 Ω differential characteristic impedance to facilitate measurement with 50 Ω test equipment.

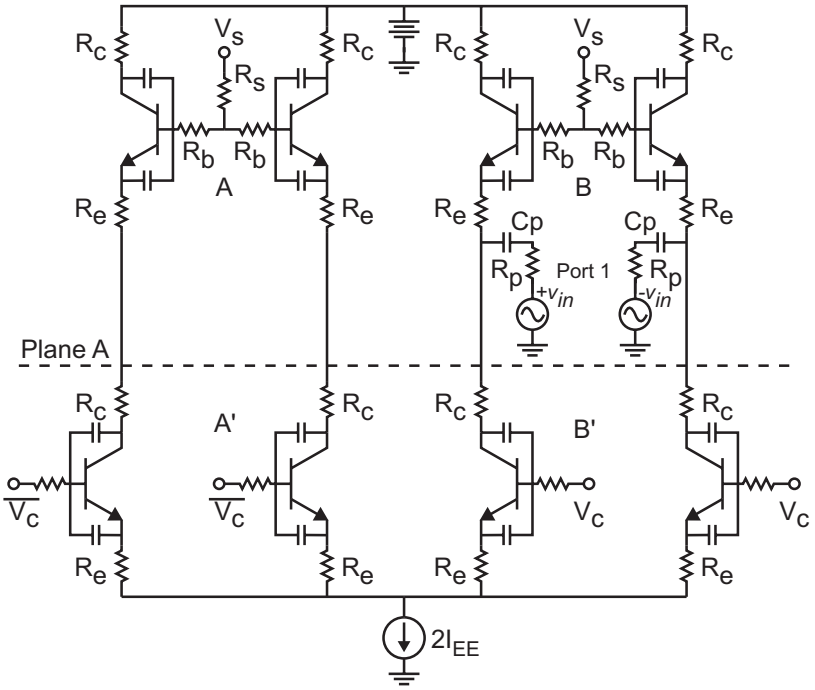



Figure 3.2: Schematic of the circuit to be analyzed with transistor parasitics.

In addition, a SPST switch was implemented by matching only two of the ports and leaving one of the output ports open and without a matching network for a more compact layout.

## 3.4 Analysis of Switching Time

The switching time of the RF envelope is limited by two mechanisms: 1) the inherent rise-time of the transistor core and 2) the bandwidth of the circuitry which follows the transistor core. The rise-time of the RF current envelope is first found in the presence of an infinite bandwidth output network which is implemented by a DC voltage source. Once this rise-time is determined, the impulse response of the finite bandwidth output network is used to determine the total rise-time at the output port (through convolution). The circuit in Fig. 3.1 is a SPDT switch where two SPST networks share a common input port. The sharing of Port 1 has virtually no effect on the transient performance of the circuit and therefore only one half of the circuit is analyzed. This is shown in Fig. 3.2 with the resistive and capacitive parasitics. The transistor symbol represents an Ebers-Moll or simplified hybrid-pi model as appropriate. For the simplified hybrid-pi model $r_\pi$, $C_D$ and $g_m$ are internal to the transistor symbol where $r_\pi$ are $C_D$ the small signal resistance and capacitance associated with the base-emitter junction.

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $R_b$ | 90 Ω | $\tau_F$ | 1.3 ps | $R_p$ | 50 Ω | $V_s$ | 0.5 V |
| $R_c$ | 25 Ω | $C_{je}$ | 30 fF | $C_p$ | 300 fF | $I_{EE}$ | 3.5 mA |
| $R_e$ | 13 Ω | $C_\mu$ | 8 fF | $R_s$ | 500 Ω | | |

Table 3.1: Circuit and transistor parameters for numerical evaluation.

The circuit of Fig. 3.2 can be broken in two distinct parts: Above plane A is the RF section with the RF input network represented by the series combination of $C_p$ and $R_p$, where $C_p$ is a DC blocking capacitor and $R_p$ is the RF port impedance. Below plane A, is the differential pair that steers the bias current to the appropriate RF transistors during switching. To further simplify the analysis, the circuits above and below the reference plane can be analyzed separately. The transistor and circuit parameters are listed in Table 3.1 where bias dependent variables such as base resistance and junction capacitances have been approximated to their (constant) values around the bias point.

### 3.4.1 Step Response of Differential Pair

The circuits below plane A in Fig. 3.2 are differential pairs used to steer the bias current to the appropriate RF stage. Fig. 3.3 shows a single differential pair with the associated transistor parasitics. The collectors of the the transistors have been shorted to a DC voltage source to determine the collector current response to an input voltage step. Determining the step response of the large signal current in a differential pair is similar to what is done when analyzing emitter-coupled logic (ECL) gates and has been done when the intrinsic transit time of the transistor is considered to be the dominant delay mechanism [47, 48]. In modern bipolar device technologies, the base width has decreased and the doping levels increased, resulting in a smaller transit time and larger junction capacitance making the base-emitter junction capacitance a significant portion of the delay associated with the base of the transistor.

In Fig. 3.3, at time $t < 0$, $Q_{A'}$ is on with nearly all of $I_{EE}$ flowing through it. At $t = 0$, $V_{b,B'}$ steps from $-V_s/2$ to $+V_s/2$ while $V_{b,A'}$ does the complement. For $Q_{B'}$ to turn on, its base-emitter junction capacitance, $C_{je}$, must be charged and this is done with the approximately constant current that is determined by the control voltage swing and the parasitic resistors,

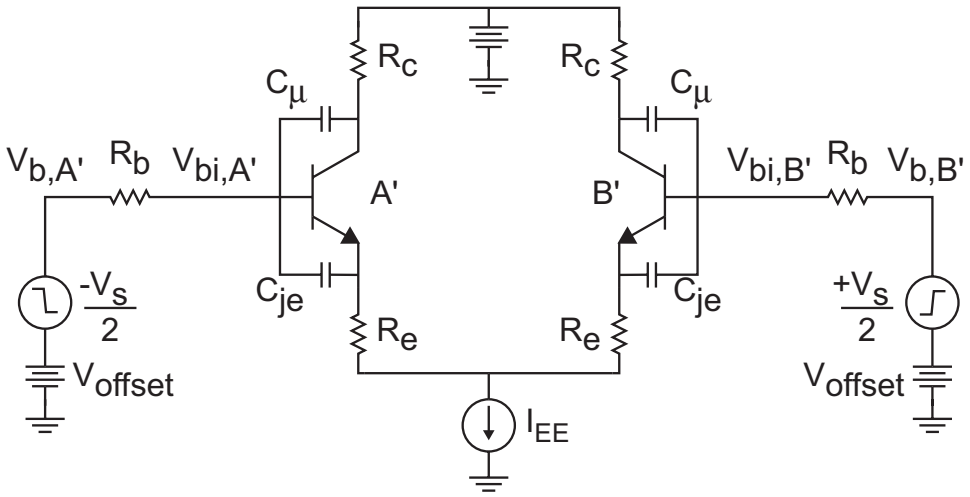



Figure 3.3: Schematic differential pair below plane A that is used to steer the bias current into the emitters of the RF transistors.

$$I_{C_{je},0} = \left[\frac{V_s}{R_b + R_e \| R_c}\right]\left[\frac{R_c}{R_e + R_c}\right] = 3.34 \text{ mA}. \tag{3.8}$$

The constant current $I_{C_{je},0}$ slews $C_{je}$ until a significant portion of intrinsic base current begins to populate the base of $Q_{B'}$ with charge. The current $I_{C_{je},0}$ represents the term $C_{je}\frac{dV_{BE}}{dt}$ in the base current of the charge control model of a bipolar transistor [49],

$$I_b = \frac{Q_F}{\beta\,\tau_F} + \frac{dQ_F}{dt} + C_{je}\frac{dV_{BE}}{dt} + C_{\mu}\frac{dV_{BC}}{dt}, \tag{3.9}$$

where $Q_F$ is the excess minority charge in the base-emitter region and $\tau_F$ is the forward transit time. The first term of (3.9) is the steady state bias current and is negligible when the DC current gain ($\beta$) is large and the last term ($C_{\mu}\frac{dV_{BC}}{dt}$) does not effect the flow of intrinsic collector current. The current $I_{C_{je},0}$ stays constant until $dV_{BE}/dt \approx 0$ and is approximated as when the intrinsic collector current of $Q_{B'}$ has reached 10% of its final value such that the $V_{BE}$ of $Q_{B'}$ has changed by the amount $V_{slew}$ where,

$$V_{slew} = V_s - V_t \ln(10) = 440 \text{ mV}. \tag{3.10}$$

The time at which the slewing of $C_{je}$ is approximately complete is,

$$t_1 = C_{je}\frac{V_{slew}}{I_{C_{je},0}} = 4.0 \text{ ps}. \tag{3.11}$$

The time $t_1$ is when $Q'_B$ begins to conduct collector current and $I_{C_{je}}$ decreases to zero such that the base current is dominated by $dQ_F/dt$. This transition happens quickly and

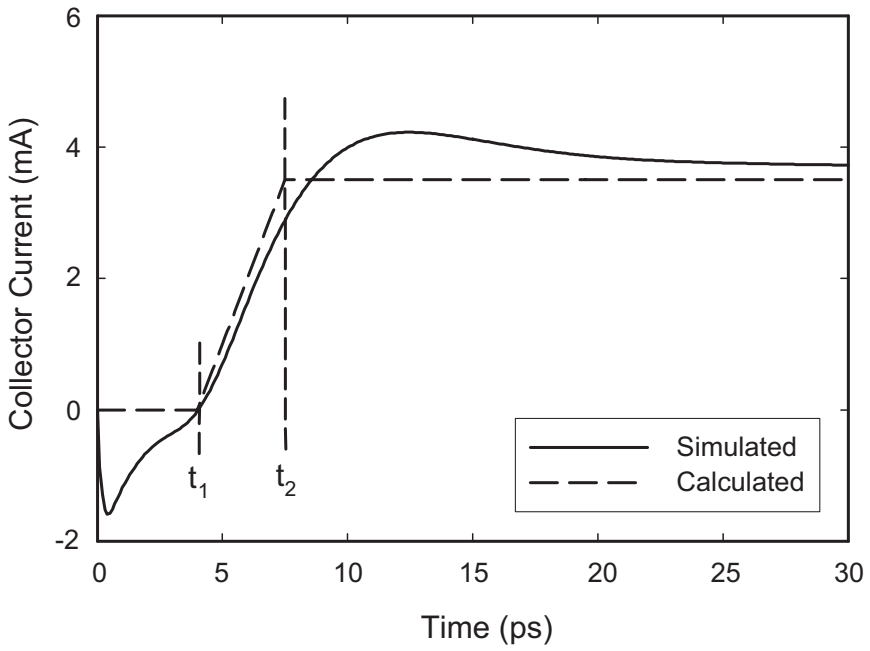



Figure 3.4: Comparison of simulated and calculated collector current of the differential pair in response to input voltage step at $t = 0$.

is approximated as instantaneous. Substituting $I_c\tau_F = Q_F$ into $dQ_F/dt$,

$$I_c = I_{EE}\left(1 - e^{-\frac{t-t_1}{\tau_1}}\right) \quad \text{and} \quad I_{b,i} = \tau_F \frac{dI_c}{dt}. \tag{3.12}$$

where $\tau_1$ is the time constant associated with the collector current. Evaluating $I_b$ at $t_1$, where to avoid a discontinuity in the base current, $I_b(t_1) = I_{C_{je},0}$,

$$\tau_1 = \tau_F \frac{I_{EE}}{I_{C_{je},0}} = 1.36 \text{ ps}. \tag{3.13}$$

The collector current can be approximated as a ramp with the same 90% rise-time as (3.12) where the ramp reaches its final value at $t_2$ where,

$$t_2 - t_1 = \tau_1 \frac{\ln(10)}{0.9} = 3.5 \text{ ps}. \tag{3.14}$$

Fig. 3.4 shows a comparison of the simulated collector current and the ramp approximation of (3.14). The simulated collector current shows a negative value for $t < t_1$ due to the forward current through $C_\mu$ whereas the approximate calculation is for the intrinsic collector current only. The delay and rise-time of the differential pair below reference plane A is very small and is virtually decoupled from the rise-time analysis. For the remainder of the analysis, the differential pair below plane A is approximated by an current step with a delay of $t_1 = 4.0$ ps, linear rise-time of $t_2 - t_1 = 3.5$ ps, and a final value of $I_{EE} = 3.5$ mA.

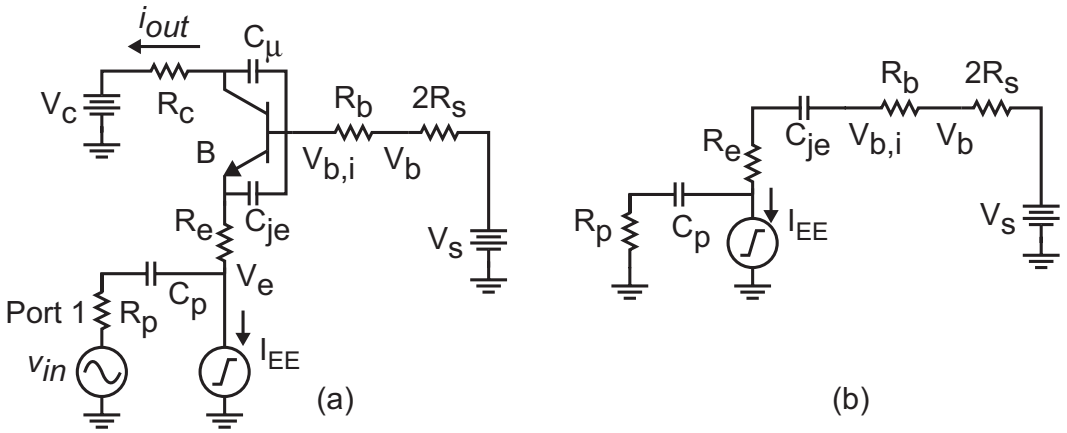



Figure 3.5: Simplified model of (a) RF stage and (b) passive parasitics.

### 3.4.2 Response of RF Transistors to an Emitter Current Step

In Fig. 3.2, the circuit above plane A is composed of two differential common-base stages. The stage to be analyzed is transistor pair B because their emitters are connected to the RF inputs, and the DC blocking capacitor ($C_p$) and RF port impedance ($R_p$) have a strong influence on the switching time. Although, transistor pair B is in a differential configuration, the bias is a common-mode signal and therefore only half of the transistor pair needs to be analyzed. Fig. 3.5a shows the simplified circuit to be analyzed where $v_{in}$ is the RF small signal input.

Once again, to analyze the transistor collector current in response to an emitter current step, the base current can be analyzed using the charge control model,

$$I_b = \frac{Q_F}{\beta\,\tau_F} + \frac{dQ_F}{dt} + C_{je}\frac{dV_{BE}}{dt} + C_{\mu}\frac{dV_{BC}}{dt}. \tag{3.15}$$

The first term of (3.15) is the negligible DC bias current and the last term is negligible because $V_{BC}$ is approximately constant due to the DC voltage sources $V_c$ and $V_s$. In reality $dV_{BC}/dt$ is not zero all of the time resulting in a small amount of base current flowing forward through $C_{\mu}$, but this has virtually no effect on the flow of intrinsic collector current.

The remaining two terms represent the current necessary to charge $C_{je}$ and populate the base-emitter region with excess minority carriers. In general, both of the these current components flow at the same time and require numerical simulation to evaluate them. However, as a first-order approximation, the time required to charge the base-emitter junction is broken into two portions of time, first when $Q_B$ is off and $dQ_F/dt \approx 0$ and second when $C_{je}$ is completely charged such that $dV_{BE}/dt \approx 0$.

When $Q_B$ is off, the circuit simplifies to Fig. 3.5b and is valid until the intrinsic collector and hence the emitter current becomes 10% of the current charging the base-emitter junction capacitance, $I_{C_{je}}$. For $t < t_1$, $I_{C_{je}} = 0$ and for $t_1 < t < t_2$, $I_{C_{je}}$ follows the linear ramp of the input current step with a final value at $t_2$ of

$$I_{C_{je}}(t_2) \simeq I_{EE} \frac{R_p + \frac{t_2 - t_1}{2C_p}}{R_T + \frac{t_2 - t_1}{2}\left(\frac{C_{je}+C_p}{C_{je}C_p}\right)} = 161 \ \mu\text{A} \tag{3.16}$$

where $R_T = R_p + R_e + R_b + 2R_s$, and the equivalent resistance of the capacitors have been taken as $\frac{\Delta t}{2C}$ from $t_1 < t < t_2$. For time $t > t_2$, $I_{C_{je}}$ is given by the solution to a first-order differential equation (Fig. 3.6):

$$I_{C_{je}} = I_{Cje}(\infty) + \left[I_{C_{je}}(t_2) - I_{Cje}(\infty)\right] e^{-\frac{t-t_2}{\tau_2}} \tag{3.17}$$

where

$$I_{Cje}(\infty) = I_{EE} \frac{C_{je}}{C_p + C_{je}} = 318 \ \mu\text{A} \tag{3.18}$$

and

$$\tau_2 = R_T \frac{C_p C_{je}}{C_p + C_{je}} = 31.4 \ \text{ps}. \tag{3.19}$$

The time $t_3$ is when $C_{je}$ becomes charged and $V_{BE}$ becomes large enough to support a significant flow of collector current. Integrating $I_{C_{je}}$ from $0 < t < t_3$ results in the total charge needed to charge $C_{je}$ and is equal to $\Delta V_{BE} C_{je}$. The transistors $Q_B$ and $Q_{B'}$ have the same area, so the total change in $V_{BE}$ is the control voltage swing $V_s$. However $V_{BE}$ only needs to change by a fraction of $V_s$ before a significant portion of the emitter current to begins to flow. This is approximated as 10% of $I_{Cje}(\infty)$ such that

$$\Delta V_{BE} = V_s - V_t \ln\left(10 \frac{I_{EE}}{I_{Cje}(\infty)}\right) - \Delta V_0 = 378 \ \text{mV}, \tag{3.20}$$

where $\Delta V_0$ is zero when the transistor switches from steady-state. However, after the initial pulse, node $V_e$ does not fully discharge because it is being discharged by the difference of two leakage currents. For very short pulse repetition intervals (PRI), $\Delta V_0$ could be as large as 300 mV, however for larger PRIs such as 100 ns (PRF=10 MHz), $\Delta V_0$ is as small as 150 mV and continues to decrease towards zero as the PRI approaches infinity. During the time interval between $t_2$ and $t_3$, the collector current is not flowing yet so the value of $\Delta V_0$ will only affect the delay of the pulse and not the rise-time.

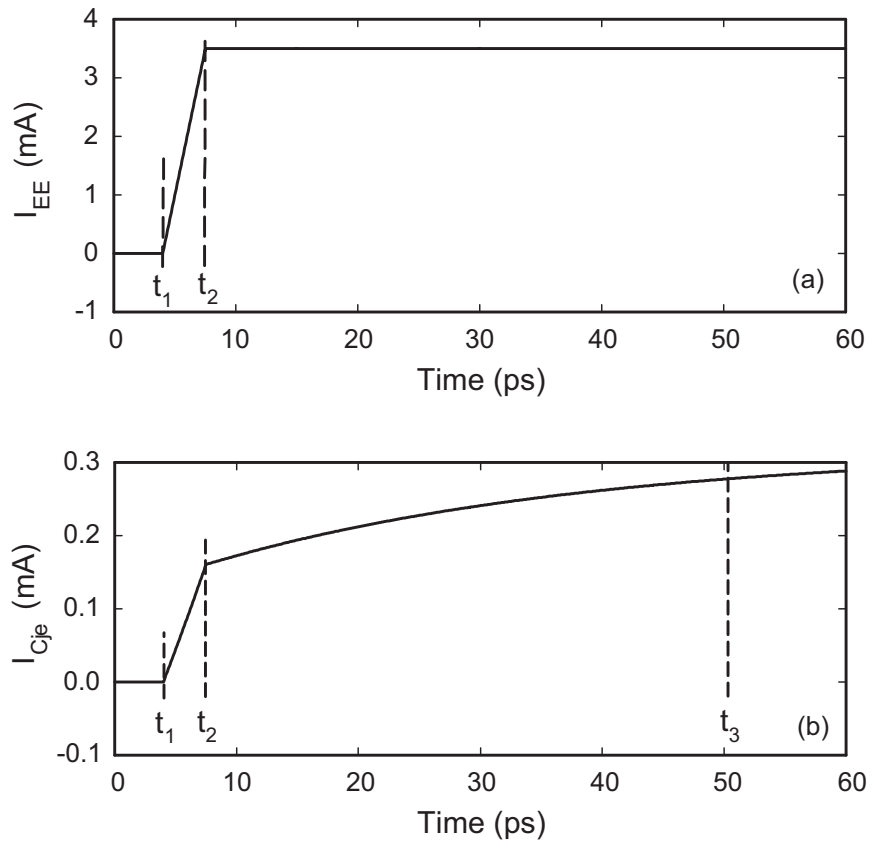



Figure 3.6: Plot of (a) driving current $I_{EE}$ and (b) current through $C_{je}$ while charging the base-emitter junction, using equations (3.16) and (3.17).

To determine the time $t_3$, $I_{C_{je}}$ must be integrated,

$$\begin{aligned}
\Delta V_{BE} C_{je} &= \int_0^{t_3} I_{C_{je}} \, \mathrm{d}t \\
\Delta V_{BE} C_{je} &= I_{C_{je}}(t_2) \frac{t_2 - t_1}{2} + I_{C_{je}}(\infty)(t_3 - t_2) \\
&\quad + \left[ I_{C_{je}}(\infty) - I_{C_{je}}(t_2) \right] \tau_2 \left[ e^{-\frac{t_3 - t_2}{\tau_2}} - 1 \right]
\end{aligned} \tag{3.21}$$

The expression in (3.21) can be solved numerically for $t_3$. However to determine an approximate closed-form expression, $I_{C_{je}}$ can be approximated as a linear function for $t_2 < t < t_3$ by replacing the exponential term with a linear ramp of the same 90% rise-time,

$$\left[ e^{-\frac{t_3 - t_2}{\tau_2}} - 1 \right] \approx -\frac{0.9}{\ln(10)} \frac{t_3 - t_2}{\tau_2}. \tag{3.22}$$

Substituting 3.22 into 3.21, the time $t_3$ is determined by,

$$t_3 - t_2 = \frac{\Delta V_{BE} C_{je} - I_{C_{je}}(t_2) \frac{t_2 - t_1}{2}}{I_{C_{je}}(\infty) - \left[ I_{C_{je}}(\infty) - I_{C_{je}}(t_2) \right] \frac{0.9}{\ln(10)}} = 43.1 \text{ ps}. \tag{3.23}$$

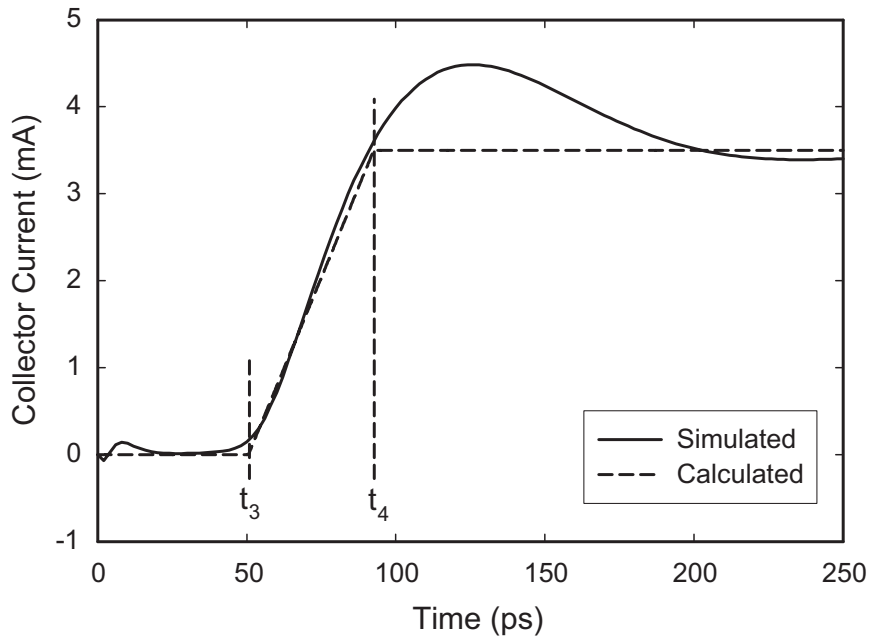



Figure 3.7: Comparison of simulated (using ADS) and calculated (using analytical equations) transient collector bias current through the RF stage, $Q_B$.

The time $t_3$ is when $Q_B$ begins to conduct collector current and $I_{C_{je}}$ decreases to zero such that the base current is dominated by $dQ_F/dt$. This transition happens quickly and is approximated as instantaneous. Substituting $I_c\tau_F = Q_F$ into $dQ_F/dt$,

$$I_c = I_{EE}\left(1 - e^{-\frac{t-t_3}{\tau_3}}\right) \quad \text{and} \quad I_b = \tau_F\frac{dI_c}{dt}, \tag{3.24}$$

where $\tau_3$ is the time constant associated with the collector current. Evaluating $I_b$ at $t_3$, where to avoid a discontinuity in the base current, $I_b(t_3) = I_{C_{je}}(t_3) = 278\ \mu$A, one gets

$$\tau_3 = \tau_F\frac{I_{EE}}{I_{C_{je}}(t_3)} = 16.4\ \text{ps}. \tag{3.25}$$

The collector current can be approximated as a ramp with the same 90% rise-time as (3.24). The ramp reaches its final value at $t_4$ where,

$$t_4 - t_3 = \tau_3\frac{\ln(10)}{0.9} = 42\ \text{ps}. \tag{3.26}$$

A comparison of the simulated and calculated collector current is shown in Fig. 3.7 where the simulated response using ADS exhibits some overshoot and ringing not captured by the first-order analysis.

### 3.4.3 Transient Response of the RF Transconductance

The RF envelope does not follow the bias current directly, but rather the magnitude of the transconductance of the RF stage. The transconductance can be determined using small-signal analysis that is linearized about the large-signal operating point. Referring to Fig. 3.5a, the transconductance of the RF stage in a common-base configuration ($i_{out}/v_{in}$) can be determined analytically when two simplifications are made. First, the effect of $C_p$ is ignored because of its use primarily as a DC blocking capacitor. Second, the effect of $r_\pi$ is ignored because $C_\pi$ dominates at microwave frequencies. The transconductance of the RF stage is therefore,

$$G_m(I_c) = \frac{I_c}{V_t + R_E I_c + j\omega(R_b + R_E)(V_t C_{je} + I_c \tau_F)} \tag{3.27}$$

where $V_t$ is the thermal voltage, $R_E = R_p + R_e$ and $I_c$ is the result of the large-signal analysis from the previous section and can be represented by the piecewise function

$$I_c(t) = \begin{cases} 0 & t < t_3 \\ \frac{t}{t_4 - t_3} I_{EE} & t_3 < t < t_4 \\ I_{EE} & t > t_4 \end{cases} . \tag{3.28}$$

Solving for the 90% rise-time of the magnitude of $G_m(t)$

$$|G_m(t)| = 0.9|G_m(\infty)| \quad \longrightarrow \quad \Delta t = 21.2 \text{ ps} \tag{3.29}$$

and approximating as a ramp, the transconductance reaches its final value at $t_5$ where,

$$t_5 - t_3 = \frac{\Delta t}{0.9} = 23.6 \text{ ps}. \tag{3.30}$$

It should be noted that the the RF envelope (3.30) has a faster rise-time than the collector bias current (3.26) (Fig. 3.8). This is due to the nonlinear (with respect to the collector current) transconductance of the RF stage caused by the emitter degeneration. This nonlinearity also makes the shape of the RF envelope very sensitive to the collector bias current when the collector bias current is small. Therefore, the small difference in the collector bias current around $t_3$ in Fig. 3.7 results in the error in the RF envelope around $t_3$ in Fig. 3.8. This error diminishes as the value the collector bias current increases as is evident from the simulated and calculated envelopes intersecting near their 90% values.

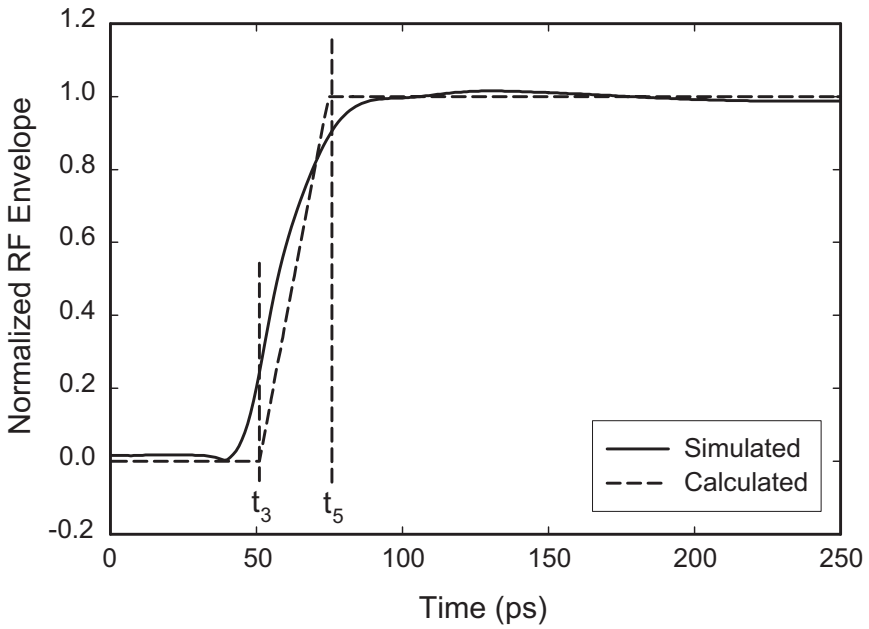



Figure 3.8: Comparison of the simulated (using ADS) and calculated (using Eq. 3.30) RF envelope into an infinite bandwidth network.

### 3.4.4 Effect of the Output Matching Network on the Rise-Time of the RF Envelope

The previous section addressed the rise-time of the RF envelope into an infinite bandwidth network. However, the output network limits the bandwidth of the signal, resulting in an increased rise-time. In this design, an LC match (L=0.87 nH, C=35 fF) is used to conjugately match the transistor output impedance to 100 Ω (differential). The center frequency is 24 GHz and the the 3-dB bandwidth is 17.5 GHz. The network was designed using full-wave EM simulation in Sonnet. Fig. 3.9a shows an approximate, singled-ended representation of the output network. For the output of transistors $Q_A$ and $Q_B$ the effect of $R_c$, $R_b$ and $r_o$ are ignored because the collector impedance is dominated by $C_\mu$ and $C_{cs}$, where $C_{cs}$ is the collector to substrate capacitance. $R_L$ provides the bias to the core and $R_{s1}$ increases the bandwidth by decreasing the Q of the network. Fig. 3.9b-c shows the frequency response and the impulse response, respectively.

To determine the rise-time of the RF envelope, it is straightforward to numerically convolve the impulse response with the input waveform which is taken as a 24 GHz RF signal whose envelope has a linear rise-time given by (3.30). Fig. 3.10 shows a comparison between the simulated RF envelope and the calculated RF envelope resulting from the

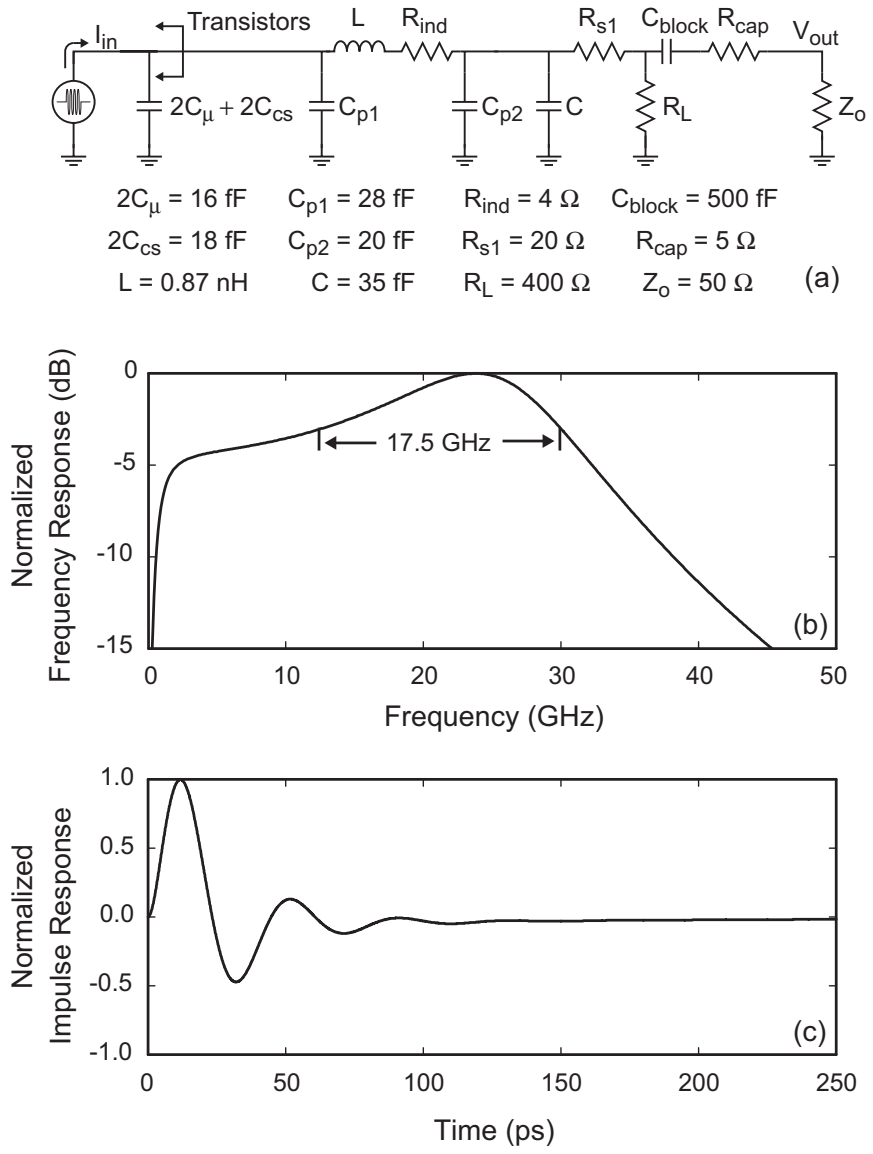



Figure 3.9: Single-ended, lumped-element approximation of output matching network (a) schematic, (b) frequency response,(c) impulse response.

convolution. Both envelopes reach 90% of their final value at $t_6$ where,

$$t_6 - t_3 = 69.3 \text{ ps.} \tag{3.31}$$

Notice that the switching time increased from 21.2 ps to 69.3 ps after the addition of the output matching network. This means that the output matching network completely dominates the switching time and one must have a very wideband matching network in order to result in a very short RF pulse. A simulation with an $L_1$-$C_1$-$L_2$-$C_2$ matching network with a 3-dB bandwidth of 25 GHz results in an output envelope rise-time of 57 ps.

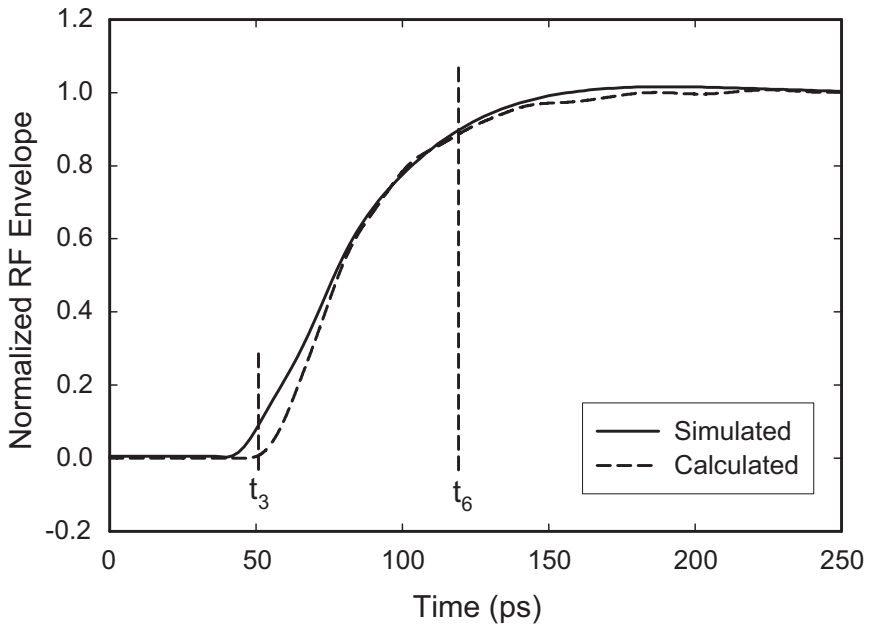



Figure 3.10: Comparison of the simulated (using ADS) and calculated RF envelope at the output of the matching network.

Although the rise-time of the RF envelope ($t_6 - t_3$) is approximately 70 ps, the absolute time of $t_6$ is 120 ps due to the delay, $t_3$. This delay is caused by the time that it takes to charge the DC blocking capacitor $C_p$ and was calculated assuming that $C_p$ started from a completely discharged state. In reality, when the the bias current is steered to change the state of the switch, there is some residual voltage that remains on the capacitor and is slowly discharged by small leakage currents. The initial condition of the capacitor voltage manifests itself in (3.20) as $\Delta V_0$ and is as function of the PRI and the leakage currents. For reasonable PRIs, $t_3$ is reduced to about 30 ps. The exact value of $t_3$ is of little concern because during the time from $t = 0$ until $t_3$ the bias current is flowing into the capacitor $C_p$ and not the transistor, therefore the transistor remains off until $t_3$. This means the delay caused by $t_3$ looks like a time delay for the entire RF wavelet, much the same way a transmission line would delay the signal. For a delay of 30 ps, this this is equivalent to about 6 mm of coaxial cable, or the delay through an SMA connector. This delay is of little consequence and for radar systems its effect would be removed through calibration.

### 3.4.5 Practical Considerations on the Rise-Time

The previous sections analyzed the rise-time of RF envelope with the assumption that the switch control was being driven by an ideal generator with zero rise-time and zero source impedance. In reality, for measurements the switching control was driven by an Agilent 8133A pulse generator with a typical 10-90% rise-time of 60 ps. In addition, there is an on-chip digital buffer and level-shifter which actually drives the switching control voltages. This has the net effect of changing the initial time ($t_1 = 3.5$ ps) and rise-time ($t_2 - t_1 = 4$ ps) of the collector current of $Q_{B'}$. However, the rise-time of the collector current of $Q_B$ ($t_4 - t_3$) is a weak function of the rise-time of the collector current of $Q_{B'}$ ($t_2 - t_1$). Therefore, the rise-time of the collector current of $Q_B$ ($t_4 - t_3$) is somewhat decoupled from the rise-time of the input control voltage.

### 3.4.6 Summary of Rise-Time Analysis

This analysis has illustrated several important concepts in determining and optimizing the rise-time of the RF envelope in a circuit which uses current steering to switch the RF signal path. In the absence of a band-limiting network, the envelope follows the transconductance of the RF stage, and the rise-time of the transconductance will always be faster than the rise-time of the bias current.

The current steering topology used for the RF switch is closely related to the ECL logic gate that has been extensively analyzed in the literature. Work done at IBM gives a figure of merit (FOM) that is directly proportional to ECL gate delay, $\sqrt{(R_b C_\mu)/(2\pi f_T)}$ [50]. Our circuit was implemented in a 0.5 $\mu$m emitter technology with a FOM of 1.2 ps whereas the FOM for IBM's 0.12 $\mu$m process is less than 0.4 ps showing a more than 3$\times$ improvement. As technology scales, switching speed will continue to decrease, but this poses a microwave design challenge: If the bandwidth of the microwave circuits that follow the RF pulse is not increased, then further improvement in the active device technology will have little effect on the pulsed RF rise-times.

## 3.5 Measured Results

Several circuits were fabricated in Atmel's SiGe2-RF process described in Chapter 1. The primary design is a differential SPDT switch, however a SPST design was also fab-

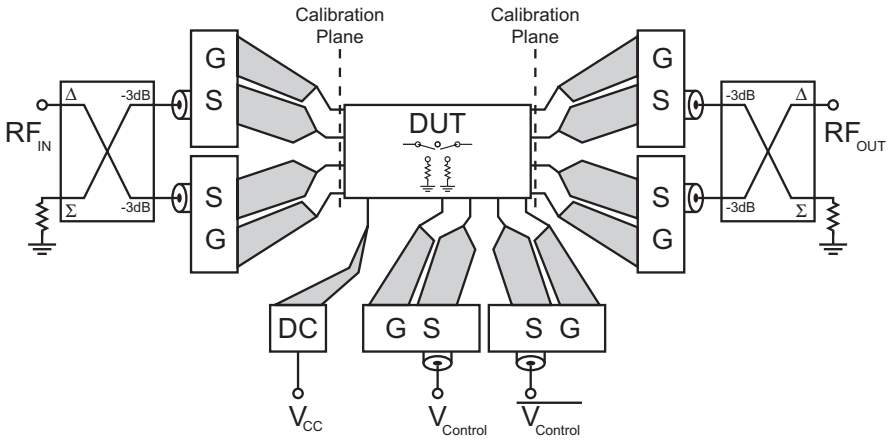



Figure 3.11: Differential test setup for on-chip measurement of SPST and SPDT switches.

ricated by taking a SPDT topology and eliminating the matching networks on one of the output ports for a more compact layout. These circuits performed virtually identically. For comparison, a single-end SPDT was also fabricated and measured.

All of the designs were measured on-chip. The single-ended design used G-S-G probes on the RF ports while the differential designs used G-S-S-G probes in conjunction with 0/180° hybrid used as a balun to convert the 100 Ω differential ports to single-ended 50 Ω ports. For S-parameter measurements, the network analyzer was calibrated to the probe tips using an LRRM calibration scheme and a calibration substrate from Cascade Microtech (Fig. 3.11).

### 3.5.1 Differential SPDT Measurements

Fig. 3.12 shows a micro-photograph of the differential SPDT ($1000 \times 550\,\mu\text{m}^2$) and SPST ($670 \times 340\,\mu\text{m}^2$). The measured and simulated S-parameters for the SPDT (Fig. 3.14) show a gain of 1.9 dB with a 35 dB on-off ratio. Also, both the input and output ports are absorptive so that it does not perturb the load or source impedances that an oscillator or power amplifier would see during switching. The 1 dB compression point, IIP3 and noise figure of the SPDT are similar to the SPST presented in [51] and were not re-measured because the circuits have the same core topology and nearly identical matching networks. The SPST has about 1 dB of additional gain due to a more compact output matching network. Table 4.1 presents a comparison between the simulated and measured results for the SPDT switch.

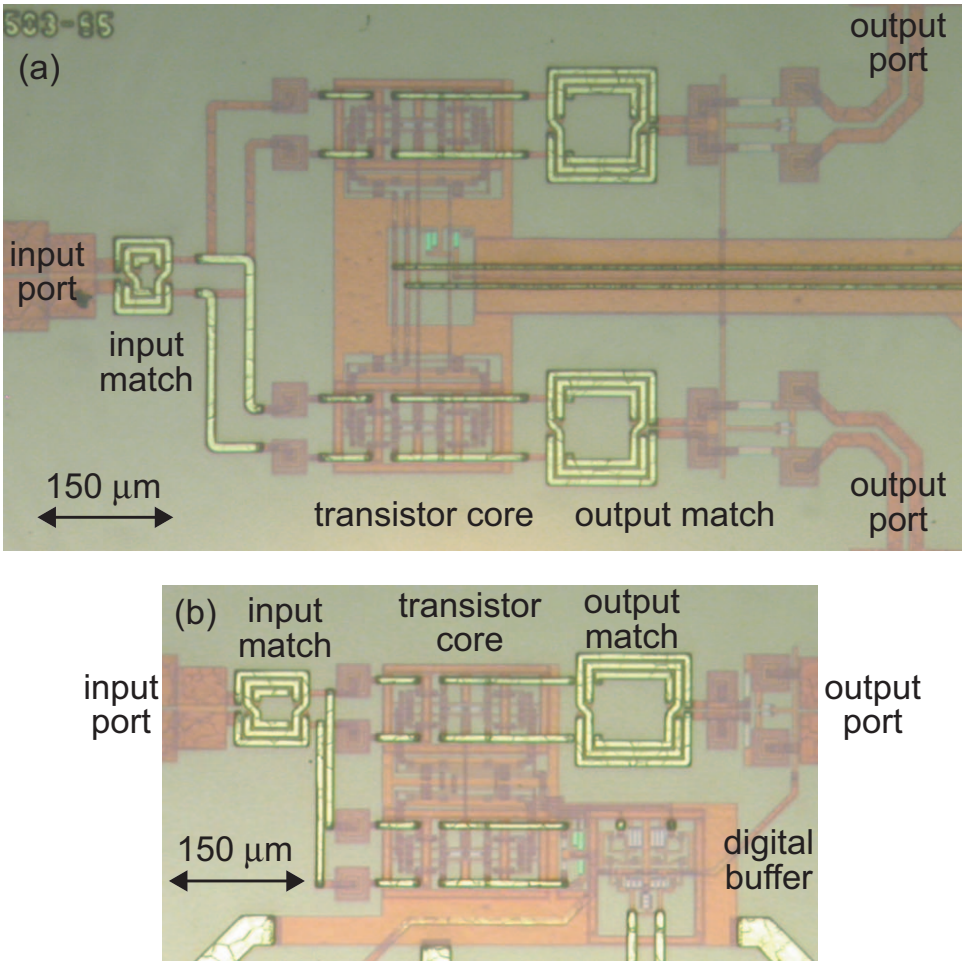



Figure 3.12: Microphotograph of sub-nanosecond differential absorptive (a) SPDT ($1000 \times 550\,\mu\text{m}^2$) and (b) SPST ($670 \times 340\,\mu\text{m}^2$).

The switching speed was measured by applying a 24 GHz CW signal to the input and a digitizing oscilloscope to the output. The switch control lines were driven by an Agilent 8133A 3 GHz differential pulse generator with a rise-time of approximately 60 ps. The 10 MHz reference of the microwave source was used to externally trigger the pulse generator and the pulse generator was used to trigger the oscilloscope (Fig. 3.13). This forces the 24 GHz RF sine wave to be coherent with the RF envelope for easy visualization of the RF wavelet.

A 500 ps pulse is shown in Fig. 3.15a. The differential topology suppresses the baseband feed-through because the control voltage is a common-mode signal. However, two 0/180° hybrid-couplers were used as single-ended to differential baluns at the input and output ports and have a bandwidth of 6-26.5 GHz. This results in common-mode signals below

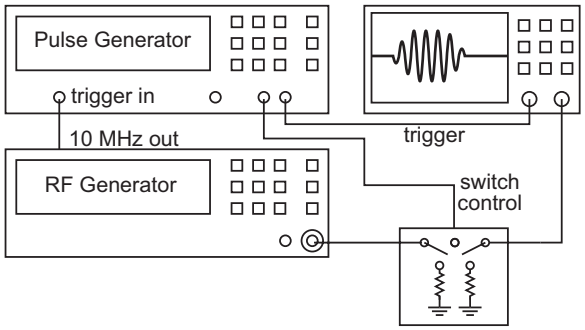



Figure 3.13: Test setup for coherent pulse formation, the reference of the RF source triggers the pulse generator and oscilloscope.

| | | Simulated | Measured |
|---|---|---|---|
| Center Frequency | [GHz] | 24.8 | 23.8 |
| Supply Voltage | [V] | 5 | 5 |
| Current (RF section) | [mA] | 16.8 | 16.1 |
| Current (digital buffer) | [mA] | 8.9 | 8.6 |
| Gain | [dB] | 2.3 | 1.9 |
| Noise Figure | [dB] | 13.2 | 13.1† |
| Isolation | [dB] | 38 | 35 |
| 1-dB compression | [dBm] | 1.7 | 0.5† |
| IIP3 | [dBm] | 10.3 | 9.0† |
| Switching Time | [ps] | 70 | 70 |

†from SPST measurement [51]

Table 3.2: Simulated and measured performance of the 24 GHz, 70 ps SPDT switch.

6 GHz experiencing mode conversion and being superimposed on the desired RF signal at the output of the coupler. The control voltage occupies the spectrum up to 3 GHz and can be removed by post-processing the data with a third order, 3.5 GHz butterworth high-pass filter as seen in Fig. 3.15b. This allows for more accurate characterization of the rise-time of the RF envelope. The envelope of the modulated signal is virtually impossible to measure directly when the envelope rise-time is the same order of magnitude as the period of the RF carrier. From Fig. 3.15b, it is clear that the waveform is not perfectly symmetric about the

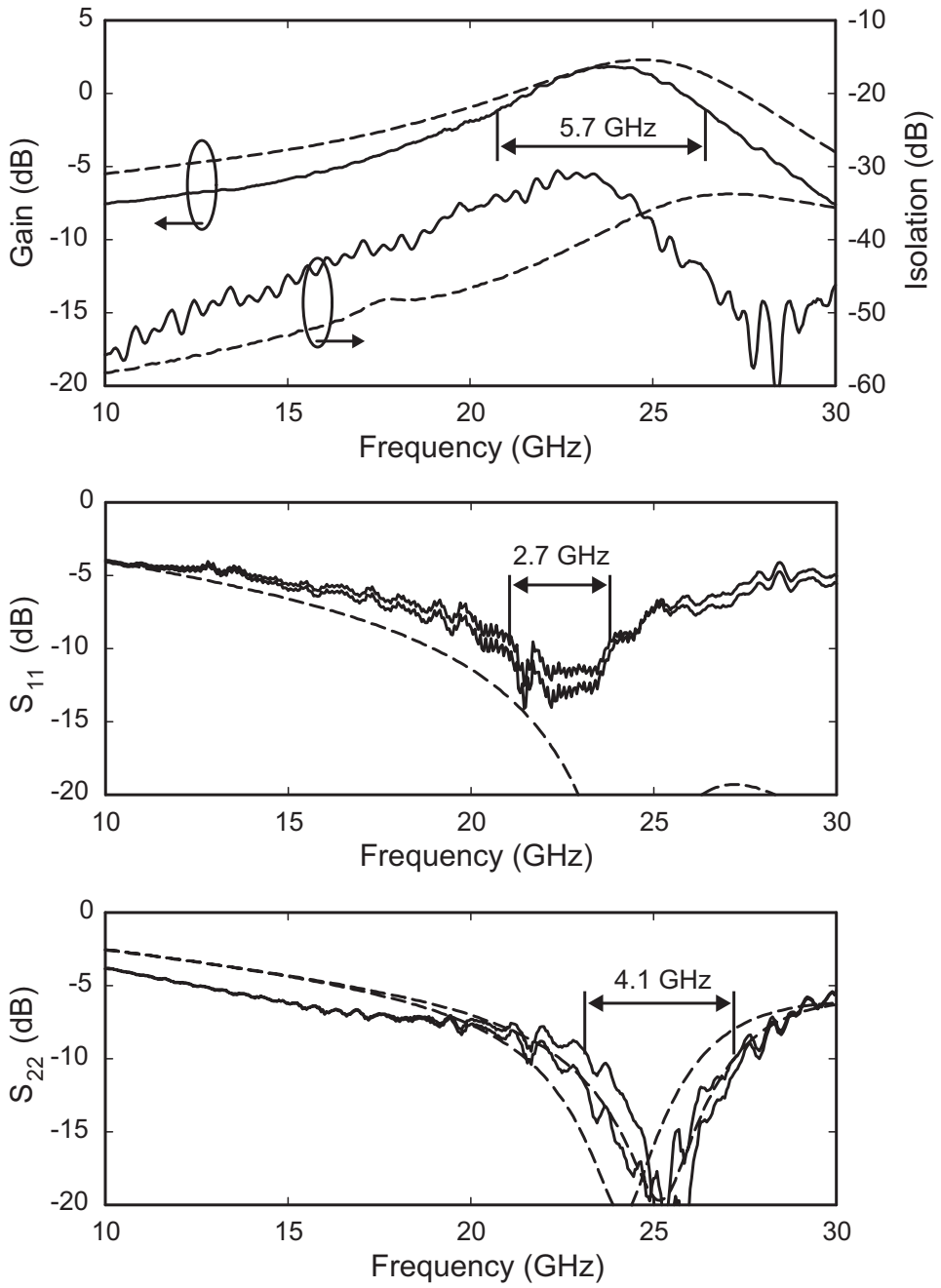



Figure 3.14: Measured (solid) and simulated using ADS (dashed) S-parameters of the sub-nanosecond SPDT absorptive switch.

x-axis, however the envelope can be approximately re-constructed with two polynomials (above and below the x-axis) resulting in two rise-times of 50 ps and 90 ps. Averaging these two values results in an estimated rise-time of 70 ps. A comparison of the measured, simulated and calculated waveforms are shown in Fig. 3.16.

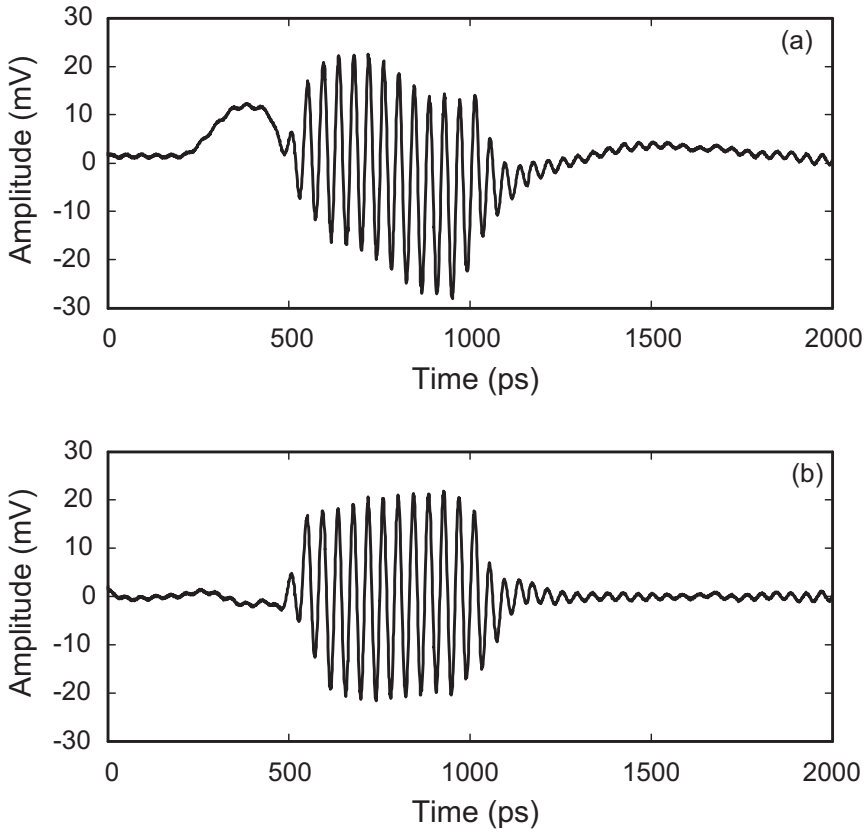



Figure 3.15: Measured (a) 500 ps pulse, (b) filtered to reduce baseband leakage.

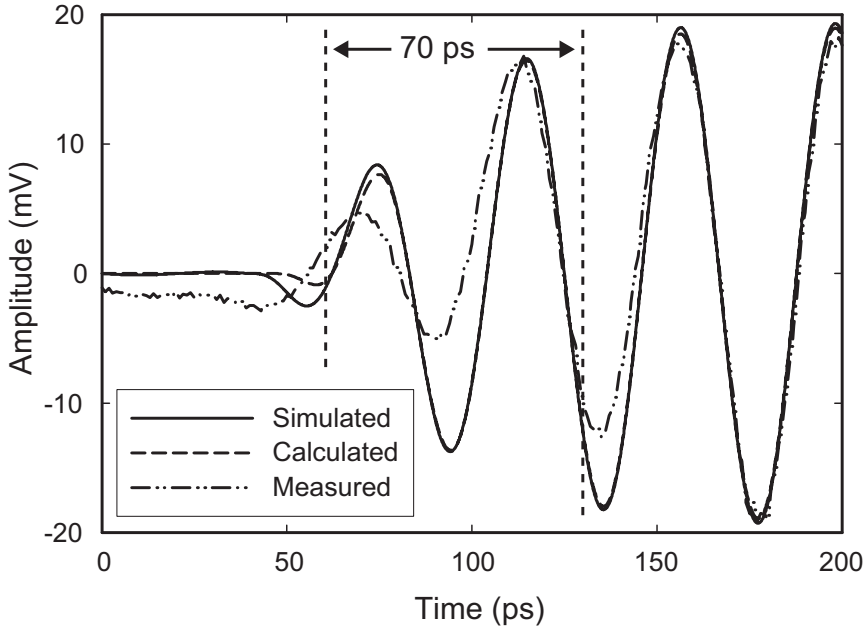



Figure 3.16: Comparison of measured, simulated (using ADS), and calculated RF envelope (using analytical equations).

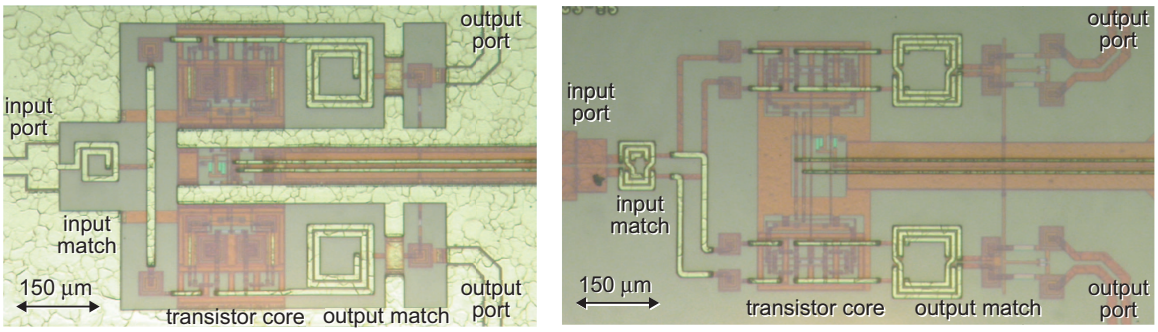



Figure 3.17: Micro-photograph of (a) single-ended SPDT ($900 \times 550\,\mu\text{m}^2$) and (b) differential SPDT ($1000 \times 550\,\mu\text{m}^2$).

### 3.5.2 Comparison of Single-Ended and Differential Design

The concept of using current steering to switch the RF signal path is not exclusive to a differential topology. The original circuit (Fig. 3.1) can be implemented in its single-ended form. The differential common-base stages become single-ended with the base of the transistors bypassed to ground with a capacitor. The challenge in this design is modeling the RF ground though careful EM simulation. The layouts of the single-ended and differential SPDT are virtually the same size and are shown in Fig. 3.17. Fig. 3.18 shows a comparison of the S-parameters of the two circuits as well as the measured switching performance in both the time domain and frequency domain.

The single-ended design exhibits about 3 dB more gain which is due to the absence of the additional loss in the differential pad launch which could not be removed through calibration. Notice that the single-ended and differential designs have very similar S-parameters and the primary difference in the performance of these two circuits is in their switching characteristics. While the single-ended design does switch very quickly, it does nothing to suppress the clock feed-through which occurs when the bias current is steered from one RF stage to another. This results in a significant amount of baseband leakage which is seen at the RF port but could be removed through the use of a high-pass filter.

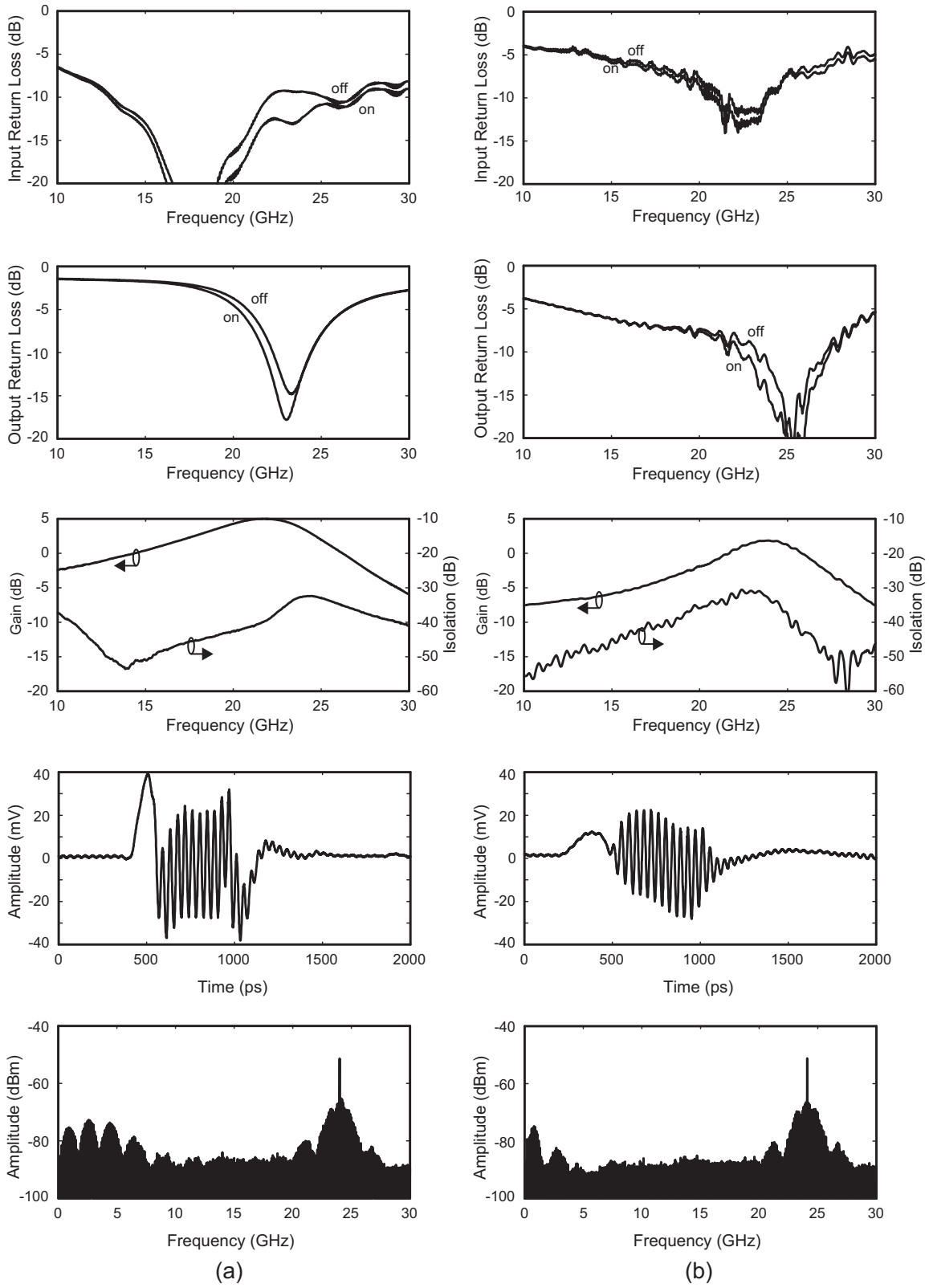



Figure 3.18: Measured S-parameters and switching performance of (a) single-ended SPDT and (b) differential SPDT.

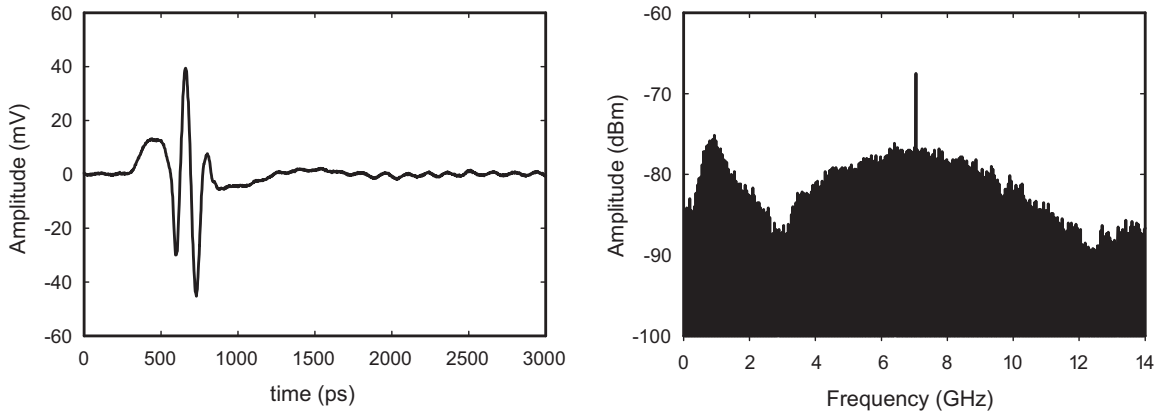



Figure 3.19: Measured UWB pulse in the 3.1-10.6 GHz band. A 7 GHz CW signal was pulsed with a 200 ps pulse width and 5 MHz PRF.

### 3.5.3 Use of the SPDT in the 3.1-10.6 GHz Band

There are several modulations schemes that have been proposed to efficiently make use of the 3.1 10.6 GHz band, some of which are a pulsed solution [37]. Whether pulse position modulation (PPM), pulse amplitude modulation (PAM) or bi-phase shift keying (BPSK) is used, sub-nanosecond pulse formation is required. Although the work in this chapter is designed for use in automotive radar applications at 24 GHz, the circuit topology is well suited for use in the UWB band at 3.1-10.6 GHz. The 24 GHz SPDT has reduced gain in the 3.1-10.6 GHz band but the performance is sufficient to demonstrate pulse formation. As an example, a 7 GHz CW signal was pulsed with a 200 ps pulse width and 5 MHz pulse repetition frequency (PRF). Fig. 3.19 shows both the time domain and frequency domain measurements of the signal. As mentioned before, there is some mode conversion that manifests itself as clock feed through due to the non-ideal 0/180° hybrids used as baluns. This is visible in the time domain at the beginning and end of the pulse as well as in the frequency domain where the clock feed-through is occupying spectrum from about 3 GHz to near DC. In addition, in the off state, the switch has an attenuation of about 60 dB that is evident by the CW leakage that is clearly visible at 7 GHz.

## 3.6 Conclusion

This chapter has presented the design and analysis of a SiGe differential absorptive SPDT switch topology at 24 GHz. An RF envelope switching time of 70 ps is achieved through the use of differential current steering to switch the RF path. The switching time of the RF envelope is analyzed analytically and agrees well with simulated and measured results. The SPDT switch achieves 1.9 dB of gain in the pass band and an isolation of 35 dB while remaining matched at its ports (absorptive). In addition, measured results for a single-ended SPDT were presented and compared to the differential design to illustrate that the differential topology suppresses clock feed through (baseband leakage). Finally, the switching performance of the differential SPDT was measured at 7 GHz to demonstrate the feasibility of using this topology in the 3.1-10.6 GHz UWB band for sub-nanosecond pulse formation.

# CHAPTER 4

# Design and Analysis of a SiGe Phase Shifter Using a Novel Constant-Impedance Topology

## 4.1 Introduction

Phase shifters are an invaluable component of microwave systems that have traditionally been limited to military applications or high-end commercial applications in which performance was the key design constraint and cost was of secondary importance. As the need for commercial smart antenna systems has grown, low cost electronically steerable phased arrays have become necessary. The dominating cost in a phased array system is associated with the electronics to control the phase of each antenna element. Phase shifters have been implemented with a variety of materials including ferrites and III-V planar integrated circuit technologies using a variety of techniques, but recently the performance of silicon has improved so that compact, low-cost, phase shifters can implemented.

In the past, phase shifters have been implemented using ferrites. While these offer high power handling capability they are large and difficult to integrate with planar circuits [52]. As planar microwave circuits have become more popular, many different circuit topologies have been developed. One technique is a reflective-type phase shifter (RTPS) that uses a 3 dB hybrid where two adjacent ports are terminated with identical reflective loads [53]. This design can provide a constant phase shift over a large bandwidth but at the expense of large size due to the layout of the 3 dB hybrid. The size of the phase shifter can be reduced, usually at the expense of bandwidth. The work presented in [54] miniaturizes the RTPS by implementing the 3 dB hybrid with lumped inductors and capacitors resulting in a 10% bandwidth.

A popular design for microwave and mm-wave phase shifters uses an electronic means to change the phase velocity along a section of transmission line. The concept was introduced in the 1950's at Bell Labs and and implemented using Schottky diodes by Nagra and York [55]. This technique was further explored by Barker and Rebeiz using MEMS varactors to load a transmission line with excellent results [56]. The same concept was used in [57] where the MEMS bridges were replaced with varactors fabricated using thin-film ferroelectric BST.

In commercial IC processes, phase shifters can be implemented using loaded-lines where the transmission line is synthesized with lumped inductors [58]. These can give good performance but there is trade-off between the matching performance and the amount of phase per section that can be obtained. Therefore a large number of inductors are required to maintain a good match while achieving the desired phase shift.

The remaining types of phase shifters in commercial IC processes are digital and require the use of a solid-state switch that is typically implemented with a PIN diode or FET. Large phase shifts (180°-bit) are usually implemented with a switched high-pass/low-pass topology where two single-pole-double-throw switches are used to toggle between two LC networks that each provide +90° and -90° for a net 180° digital phase shift. The LC networks are typically implemented with Π and T-networks. For the remainder of the bits (<90°) an embedded FET topology can be used [59, 60]. These designs offer good performance for their high level of integration but rely on the use of a FET as a low loss switching element.

To further reduce the cost of phase shifters it would be highly desirable to use silicon technology. A MMIC implementation similar to [59, 60] was implemented in silicon using a thick polyimide on top of the silicon chip so that a low-loss microstrip layer could be used for inductors and transmission lines [61]. The switching elements were implemented with PIN diodes that were available in the process, a 6-bit phase shifter was achieved with 12 dB of insertion loss. Recently using a SiGe BiCMOS process, the work in [62] has explored the possibility of phase shifting the LO signal rather than the RF signal. In this case the RF undergoes a phase shift when it is down converted to the IF frequency. The LO phases are generated directly using a tuned ring oscillator structure and an analog multiplexer chooses the correct phase for each mixer.

This work details the implementation of a phase shifter in SiGe with an integrated LNA without any post fabrication processing. A digital 180° phase shift is integrated into the LNA and is cascaded with an analog phase shifter using SiGe varactors that provides 180° of

continuously variable phase shift. The analog phase shifter uses a *constant-impedance* tuning technique that tunes the phase while simultaneously keeping a constant port impedance. The topology is analyzed and design equations are presented. The phase shifter with integrated LNA is designed using extensive electromagnetic simulation and implemented in SiGe. Finally, measured results are presented for the complete chip.

## 4.2 Analysis of Constant-Impedance Topology

Low-pass Π and T-networks can provide up to 90° of delay while remaining matched, conversely the dual high-pass network can provide up to a 90° phase advance. However the inductance and capacitance must be changed simultaneously to keep a constant port impedance. For the T-network in Fig. 4.1a, the required values of the inductance and capacitance can be derived for a given phase delay and the condition that the network is matched to a characteristic impedance $Z_o$. The $ABCD$ matrix for the network is:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1+Z_L Y_C & Z_L(2+Z_L Y_C) \\ Y_C & 1+Z_L Y_C \end{bmatrix} \tag{4.1}$$

where

$$Z_L = jX_L = j\frac{\omega L}{Z_o} \quad \text{and} \quad Y_C = jB_C = j\omega C Z_o \tag{4.2}$$

are the normalized values for $L$ and $C$. Neglecting any resistive parasitics, to remain matched, $S_{11} = 0$, therefore using (4.1), $A = D$ and $B = C$. An expression for $B_C$ can be determined,

$$B_C = \frac{2X_L}{1+X_L^2}. \tag{4.3}$$

The insertion phase of the network is:

$$\phi = \angle S_{21} = \tan^{-1}\left[\frac{X_L^2 B_C - 2X_L - B_C}{2 - 2X_L B_C}\right]. \tag{4.4}$$

Substituting (4.3) into (4.4)

$$\tan(\phi) = \frac{-2X_L}{1-X_L^2} \quad \rightarrow \quad X_L = -\tan\left(\frac{\phi}{2}\right). \tag{4.5}$$

Using (4.3) and (4.5), the value of inductance and capacitance can be calculated as:

$$L = -\frac{Z_o}{\omega}\tan\left(\frac{\phi}{2}\right) \quad \text{and} \quad C = -\frac{1}{\omega Z_o}\sin(\phi). \tag{4.6}$$

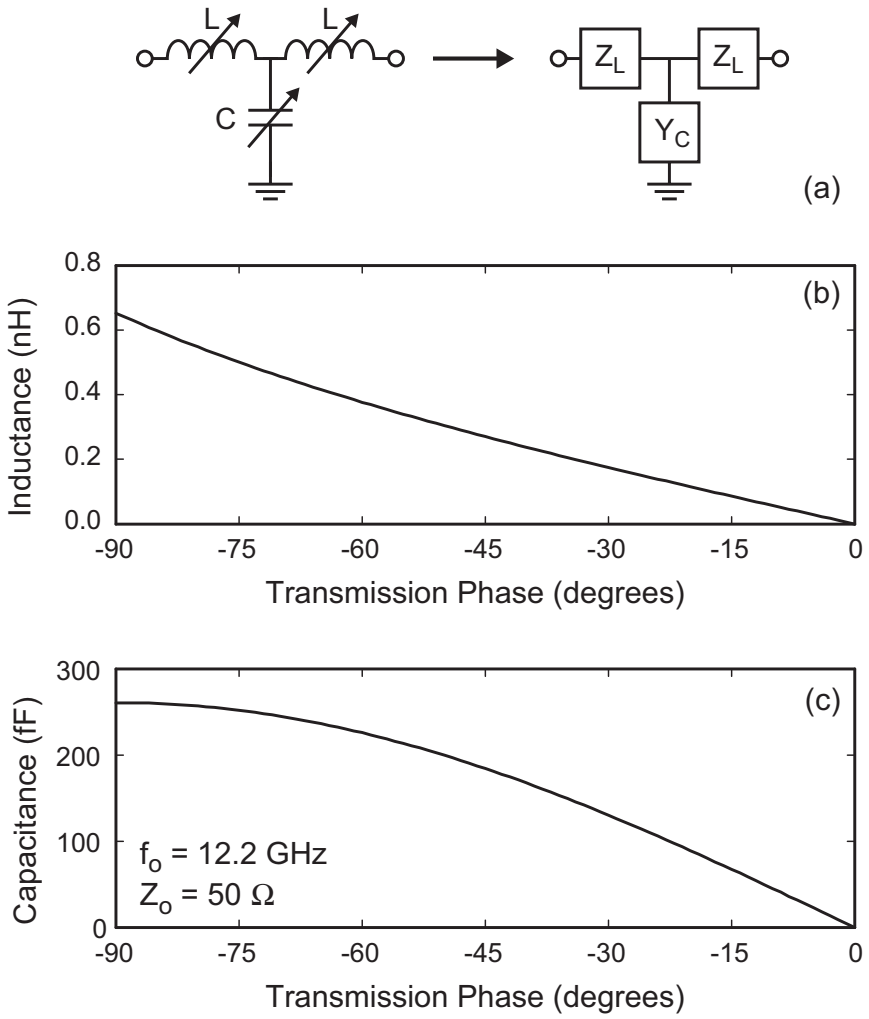



Figure 4.1: Ideal tunable T-network, (a) schematic and the values of (b) inductance and (c) capacitance to obtain different phase shifts while remaining matched to a constant impedance.

Plotting (4.6)in Fig. 4.1 shows that for a capacitance tuning range of 2:1 one can achieve a phase shift of 60°. This is only possible if the inductance can be simultaneously tuned over a 3.7:1 tuning ratio.

In an integrated circuit process, tunable inductors are not available, however over a small bandwidth (10-20%) a variable inductance can be approximated by a fixed inductor in series with a variable capacitance because the series capacitance subtracts reactance from the inductor. This leads to the proposed circuit of Fig. 4.2. Assuming that $C_s$ has the same capacitance ratio as $C$, $C_s$ can be designed to be $r$ times larger than $C$ to facilitate easy control of tuning.

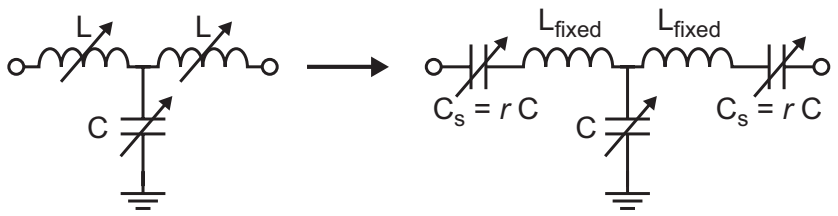



Figure 4.2: Schematic of proposed tunable T-network.

The reactance of the series combination of $L_{fixed}$ and $C_s$ can be written as

$$X_L = X_{L,fixed} - \frac{1}{\omega r C}. \tag{4.7}$$

The equivalent series inductance of this network is determined by dividing (4.7) by $\omega$. If the equivalent inductance is forced to equal the ideal inductance at the maximum and minimum values, two equations can be written.

$$L_{max} = L_{fixed} - \frac{1}{\omega^2 r C_{max}} \tag{4.8}$$

$$L_{min} = L_{fixed} - \frac{1}{\omega^2 r C_{min}} \tag{4.9}$$

Solving (4.8) and (4.9) for $L_{fixed}$ and $r$ results in:

$$r = \frac{1}{\omega^2 \left(L_{max} - L_{min}\right)} \left(\frac{1}{C_{min}} - \frac{1}{C_{max}}\right) \tag{4.10}$$

$$L_{fixed} = L_{max} + \frac{1}{\omega^2 r C_{max}}. \tag{4.11}$$

For a 50 Ω port impedance, 12.2 GHz center frequency and a capacitance ratio of 2:1, the phase shift network can be easily designed using (4.10) and (4.11). For $C_{max}$ and $C_{min}$ of 260 fF and 130 fF, given by the technology, $r$ and $L_{fixed}$ are found to be 1.36 and 1.13 nH respectively. Simulation shows that a capacitance ratio of 2:1 results in a phase shift of 60° and a return loss of better than −15 dB (Fig. 4.3). Notice that the network is perfectly matched when the capacitance equals $C_{max}$ and $C_{min}$ as per (4.8) and (4.9). In between these values, the equivalent inductance does not equal the ideal inductance but is close enough that the matching better than −15 dB.

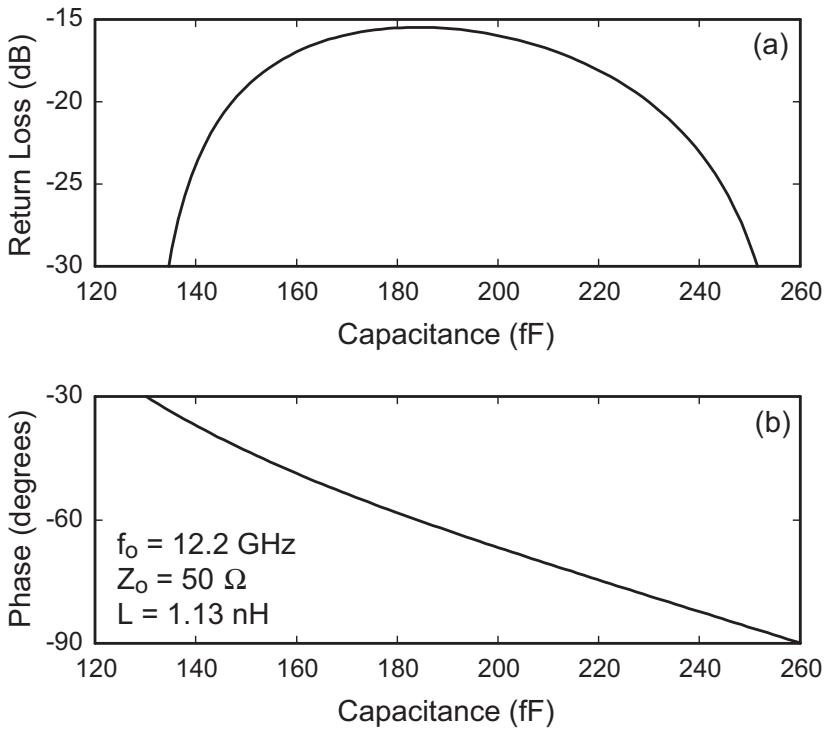
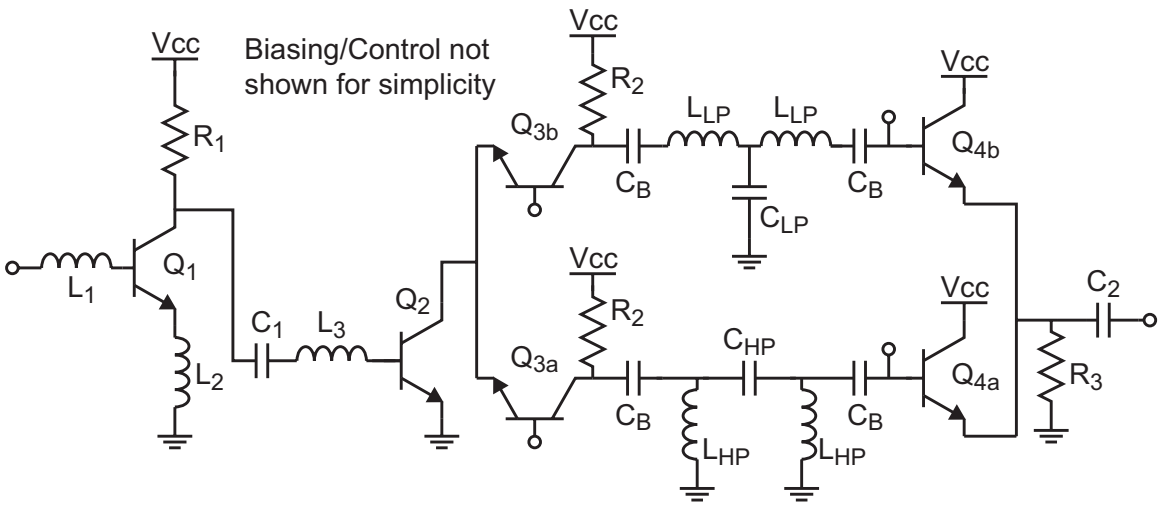



Figure 4.3: Simulated return loss (a) and insertion phase (b) of the proposed constant-impedance phase shift network over a 2:1 change in capacitance.

## 4.3 Design of LNA/180°-bit

The topology for the 1-bit digital phase shifter with integrated LNA is shown in Fig. 4.4. The first stage is simultaneously matched for noise and return loss by sizing the device properly and through the use of $L_2$ for inductive emitter degeneration [63]. Because a 5 V supply voltage was required, a resistive load of 1 kΩ was used instead of an RF choke. This saves area with only a small impact on the noise performance. The input transistor $Q_1$ has four emitter fingers ($5 \times 0.5\,\mu\text{m}^2$) and is biased at 3.6 mA for low noise. Using a cascode in the first stage was an option and would result in more gain, but with more noise. Between the first and second stage of the LNA, a DC blocking capacitor and interstage matching inductor is used for maximum power transfer.

The second stage in the LNA consists of $Q_2$ and is the same size as $Q_1$. It is also biased for low noise performance at 3.6 mA, but does not use inductive degeneration. It uses a cascode for increased gain and to implement a single-pole-double-throw (SPDT) switch in the signal path. The bias of $Q_{3a}/Q_{4a}$ and $Q_{3b}/Q_{4b}$ are controlled such that only one




| | |
|---|---|
| $L_{HP}$ | 1.3 nH |
| $L_{LP}$ | 1.3 nH |
| $C_{HP}$ | 130 fF |
| $C_{LP}$ | 130 fF |

| | |
|---|---|
| $L_1$ | 0.45 nH |
| $L_2$ | 0.2 nH |
| $L_3$ | 0.75 nH |

| | |
|---|---|
| $C_1$ | 0.45 nH |
| $C_2$ | 0.2 nH |
| $C_B$ | 0.75 nH |

| | |
|---|---|
| $R_1$ | 1 kΩ |
| $R_2$ | 320 Ω |
| $R_3$ | 1.5 kΩ |

Figure 4.4: Schematic of the digital 180° phase bit with integrated LNA.

transistor pair is turned on at a time and the signal is directed either through the high-pass (+90°) or low-pass (−90°) network to provide a net 180° phase shift ($Q_{4a}$ and $Q_{4a}$ are biased at 1.9 mA). The complete LNA/180° bit consumes 10.2 mA. The simulated gain is 14.5 dB with a noise figure of 3.4 dB at 12.2 GHz. The 1 dB input compression point and IIP3 is −25 dBm and −15 dBm respectively.

The high-pass and low-pass networks are designed to have a characteristic impedance of approximately 100 Ω. Using a high impedance improves the power transfer between $Q_3$ and $Q_4$ by providing some interstage matching. The values of the low-pass T-network can be chosen by using (4.6). For the high-pass Π-network the derivation is similar resulting in dual expressions,

$$L = \frac{Z_o}{\omega \tan\left(\frac{\phi}{2}\right)} \quad \text{and} \quad C = \frac{1}{\omega Z_o \sin(\phi)} \tag{4.12}$$

where $\phi$ is −90° in (4.6) for the low-pass network and $\phi$ is +90° in (4.12) for the high-pass network.

The shunt capacitor ($C_{LP}$) in the low-pass T-network was implemented as a parallel-plate structure in the oxide between metal 1 and metal 2 (metal-insulator-metal, MIM). The

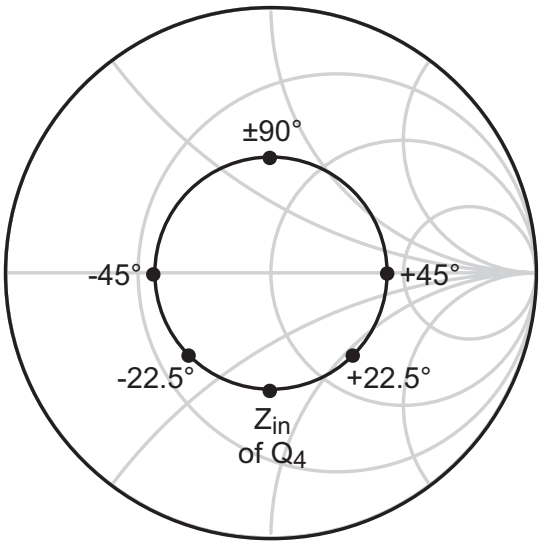



Figure 4.5: The input impedance of $Q_4$ is not matched to the characteristic impedance of the phase shift networks and introduces gain mismatch when the delay networks other than $\pm 90°$.

series capacitor ($C_{HP}$) in the high-pass Π-network was implemented as two series capacitors to maintain symmetry in the network. These two series capacitors were realized using the MIM capacitor layer in the process that uses silicon nitride as a dielectric. In both networks, the inductors are placed next to each other and simulated as a three-port element to take into account the mutual coupling. The high-pass/low-pass networks, including the blocking capacitors ($C_B$), are full-wave simulated and optimized to provide a net phase shift of 180° with a small amplitude imbalance when integrated between the transistors $Q_3$ and $Q_4$.

There is a subtlety that can be overlooked when designing the switched high-pass/low-pass networks. At first glance this topology could be used to create 90°, 45° and 22.5° bits, but these are not implemented as easily. The input impedance of $Q_4$ and the output impedance of $Q_3$ are not matched to the characteristic impedance of the high-pass and low-pass networks. When the input impedance of $Q_4$ does not equal $Z_o$, it will be transformed along a constant impedance circle and be rotated by $\pm 2\beta\ell$.

In the case of the 180°-bit where ±90° networks are used, the input impedance of both signal paths are rotated ±180° and both end up at the same point on the Smith chart. This is not the case if the other phase shifter bits are implemented in this manner (Fig. 4.5), and results in a gain imbalance because the gain of the two signal paths are proportional to the impedances presented to the outputs of $Q_{3a}$ and $Q_{3b}$. The gain imbalance can be corrected

by matching the output of $Q_3$ and the input of $Q_4$ to $Z_o$ before inserting the high-pass and low-pass networks, but this requires the use of four additional matching networks leading to an increased area and narrower bandwidth. For this reason, the remainder of the phase shifter is implemented with an analog constant-impedance phase-shift network.

## 4.4 Design of Constant-Impedance Phase Shifter

The first step in designing the analog constant-impedance phase shifter is to determine the sizing of the shunt and series varactors. Equation (4.6) is used to to determine the size of the shunt varactor. The value of $r$ and $L_{fixed}$ are then calculated using (4.10) and (4.11). In reality the cathodes of the series varactor diodes have a shunt substrate diode associated with them resulting in a parasitic junction capacitance. In addition there are also shunt parasitics at the two terminals of the inductors (Fig. 4.6a). The effect of these parasitics can be compensated by adjusting the values of value of $r$ and $L_{fixed}$ through simulation. The parasitics reduce the tuning range to about 45° requiring the complete analog phase shifter to use four sections to achieve the required 180° phase shift.

The varactors have a simulated Q in the range of 30-45 at 12 GHz and the inductors have a simulated of Q of approximately 15-18 at 12 GHz depending on how close they are to the CPW ground plane. This results in approximately 1.7 dB of insertion loss per 45° section. The full wave simulations of the four cascaded sections are shown in Fig. 4.6. The insertion loss is 6.8 dB and the RF ports are matched around the design frequency. Because of the lumped implementation, the the absolute phase is linear with frequency while the relative phase shift is constant with frequency in the center of the band of interest. The constant-impedance network is easily scalable to higher frequencies, but care must be taken to minimize and correctly model the substrate parasitics associated with the varactors and inductors. This task can be made somewhat easier by implementing the topology in a differential topology.

The power handling capability of the network was also simulated and the phase begins to deviate from the nominal value due to self-biasing of the varactors at high input powers. When the diodes are reverse biased at 2 V, the phase shifts from its nominal value by 2° for an input power of 20 dBm. Therefore, the overall linearity of the phase shifter is limited by the input LNA.

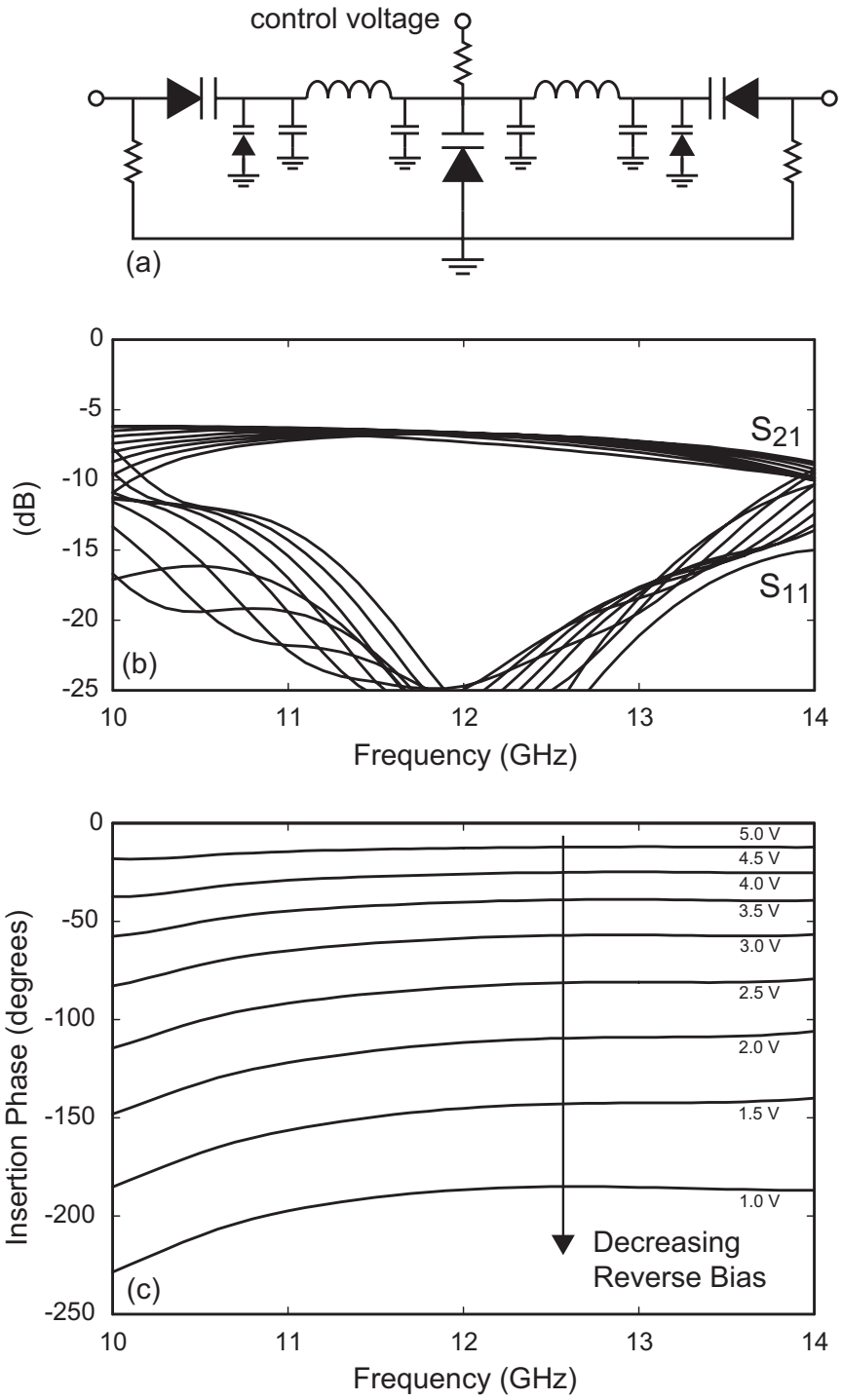



Figure 4.6: The (a) schematic of a single 45° cell of the passive varactor-tuned phase shift network. Simulated performance of four cascaded the constant-impedance phase shift networks (b) insertion/return loss and (c) relative phase shift at different control voltages.

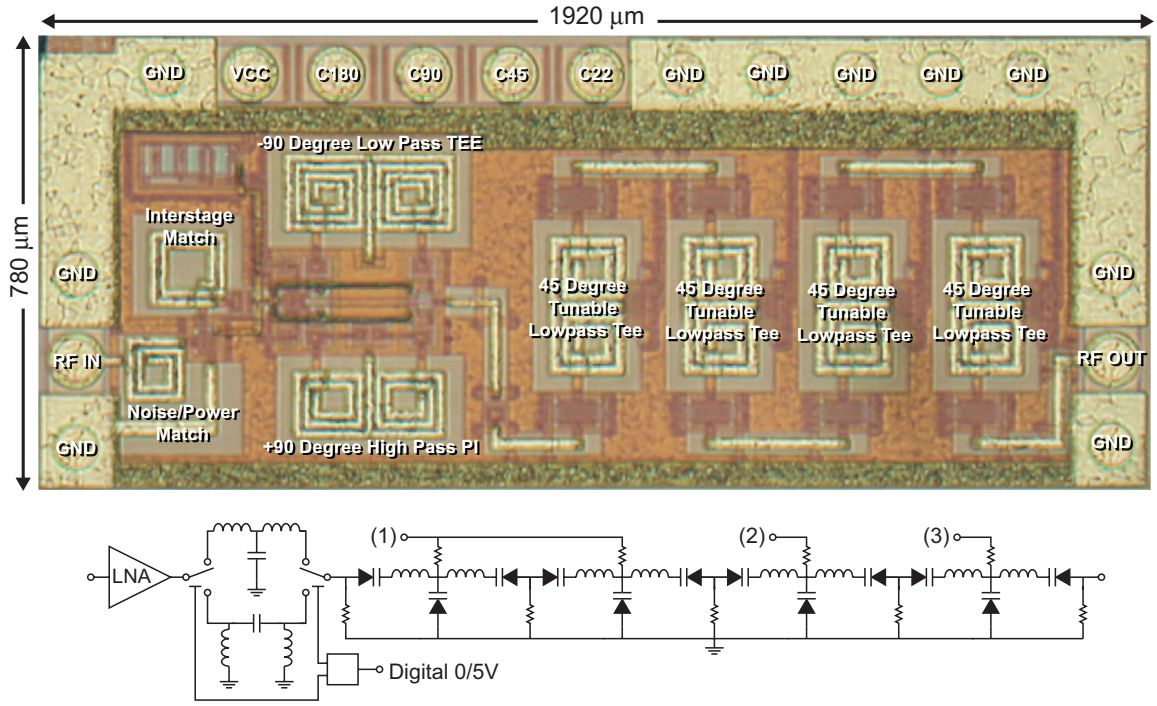



Figure 4.7: Micro-photograph and schematic of 12 GHz active phase shifter with integrated LNA.

## 4.5 Physical Design

The proposed phase shifter topology was fabricated in Atmel's SiGe2-RF process described in Chapter 1. The phase shifter was first designed in ADS with lumped components to determine the topology and bias points of the devices. The physical layout is then simulated in pieces using Sonnet for planar electromagnetic simulations to take into account the coupling between adjacent inductors and the interaction with the ground plane. The multi-port S-parameters are used in ADS in conjunction with the models of the active devices to simulate the phase shifter performance and iterate as necessary. Once completed, the final layout is done in Cadence using Virtuoso. Fig. 4.7 shows a micro-photograph of the phase shifter with integrated LNA. The dimensions of the total chip, including pads is $1920 \times 780\,\mu\text{m}^2$, however without pads the area of the active circuitry is $1680 \times 660\,\mu\text{m}^2$, an area of 1.1 $\text{mm}^2$.

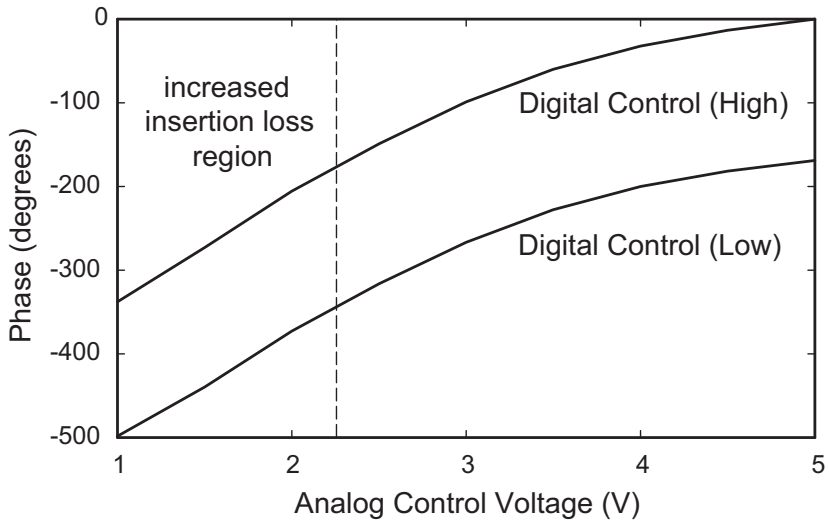



Figure 4.8: Measured phase at 11.5 GHz as a function of control voltage. The insertion loss is high and is not used at 1-2 V.

## 4.6 Measured Results

The phase shifter was measured on-chip using RF probes and an LRRM calibration to the probe tips to measure the S-parameters. There is one digital control and three analog phase controls. For most of the testing the three analog controls were shorted together to form a single analog control. The digital control introduces a 180° phase delay, while the analog control voltage provides continuous phase control over a 180° range.

Fig. 4.8 shows that a phase shift of $0° - 180°$ is achieved with the digital control high and the analog voltage swept from 5 V to 2.4 V. When the digital control is low and the analog voltage swept from 5 V to 2.4 V, the phase shift is $180° - 360°$. The constant-impedance network was designed based on the CV curve of the varactor model which indicated that a reverse bias from 5 V to 1 V would be needed. However, a reverse bias of only 5 V to 2.4 V is found to achieve the required phase shift and $S_{21}$ degrades quickly below 2 V. This is due to a combination of increased capacitance and a decrease in varactor Q, and indicates that the scalable varactor model from the foundry underestimates the tuning ratio and overestimates the Q. The absolute phase performance is shown in Fig. 4.9 and increases linearly with frequency as expected. Fig. 4.10 shows the same curves normalized to their relative phase values at 11.5 GHz. The relative phase shift is constant and flat to within $\pm 10°$ over more than 1 GHz of bandwidth.

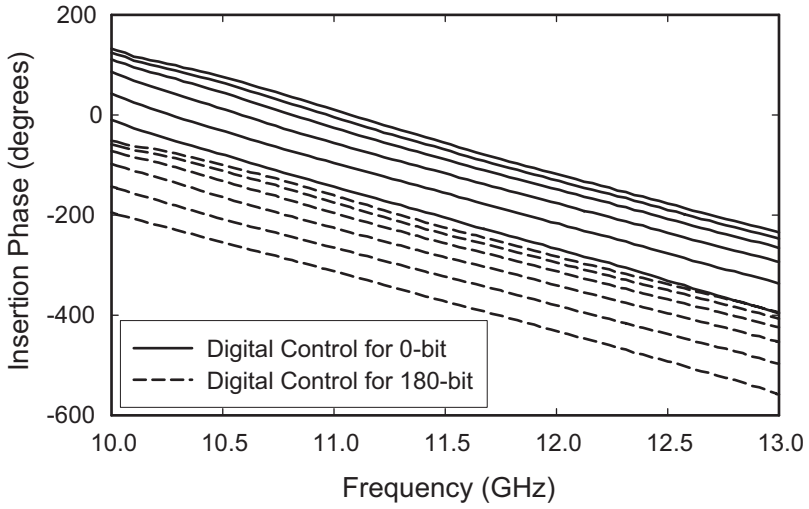



Figure 4.9: Measured absolute phase for analog control voltages from 5 V to 2.5 V (0.5 V steps).

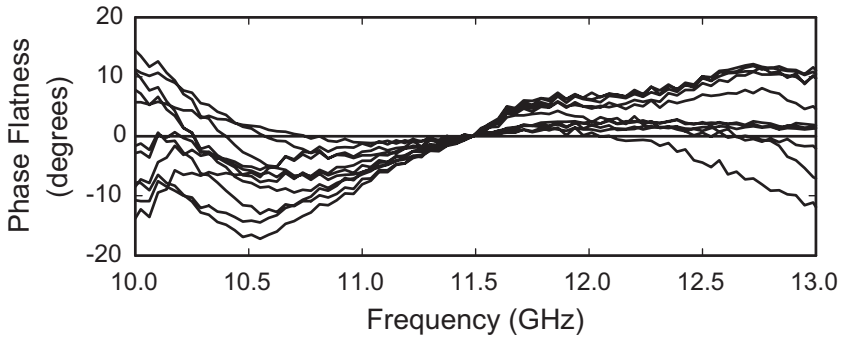



Figure 4.10: Measured phase difference flatness; the phase vs. frequency curves are normalized to their value at 11.5 GHz.

The measured gain and return loss are presented in Fig. 4.11. The overall gain of the phase shifter is simulated to be 7.2 dB at 12.2 GHz and measured to be 3.7±0.5 dB at 11.5 GHz. From 11-12 GHz the gain varies by less then ±1.2 dB. Both the input and output return loss are better than -10 dB over the band of interest. The $S_{22}$ was designed to be better than −15 dB and the difference is most likely due to the inaccuracies in the varactor model. However, the concept of using series varactors to implement a constant-impedance phase shift network is working properly. Fig. 4.12 shows the output return loss for different phase states from 11-12 GHz and the impedances are concentrated in a very small area.

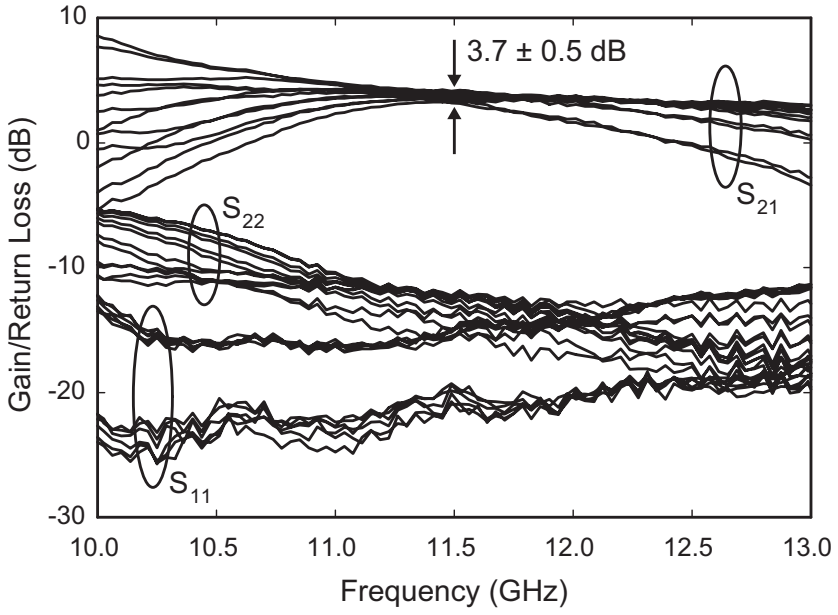



Figure 4.11: Measured gain and return loss of the phase shifter with integrated LNA in both digital states of the 180° bit and for analog control voltages from 5 V to 2.5 V (0.5 V steps).

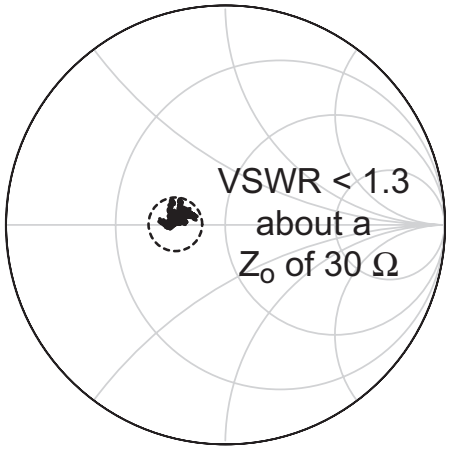



Figure 4.12: Measured output return loss ($S_{22}$) from 11-12 GHz showing that a constant impedance is maintained.

It is difficult to precisely determine the cause of the 3.5 dB decrease in gain from the simulated performance due to the cascaded nature of the system and the individual building blocks were not fabricated by themselves. The most likely culprit is the varactor diode

model. According to the process documentation[1], the C-V characteristics at 1 MHz were measured for different junction areas covering a 4:1 range and the model is in good agreement with the measured data. However, the S-parameters were also measured from 50 MHz to 23 GHz and the model begins to clearly deviate from the measured data as the frequency increases. This indicates that there clearly are parasitic effects that are not being taken into account by the foundry model of the varactor diode.

The measured noise figure is 4.4 dB at 11.5 GHz which agrees reasonably well with the simulated value of 3.7 dB at 12.2 GHz. The difference is most likely due to increased loss in the analog phase shifter that follows the 180° digital bit. In future designs the noise figure could be improved by increasing the Q of the inductors used in the LNA stage ($L_1$ and $L_2$) by using the parasitic inductance of a package (bondwires, etc.). This design was not intended for packaging and therefore this design approach was not an option. Beyond improving the Q of the passive devices in the LNA stage, the device would need to scale to improve the noise performance. This technology uses a $0.5\,\mu$m emitter width which can obtain a 1.5 dB noise figure with 14 dB of associated gain at 10 GHz. However in a state-of-the-art technology where the emitter width could be as small as $0.12\,\mu$m, the minimum noise figure is 0.45 dB with an associated gain of 14 dB at 10 GHz [64].

The measured input 1-dB compression point and IIP3 is $-27.3$ dBm and $-17.3$ dBm respectively. The linearity requirement is dependent on the application, and the input power could be as high as $-20$ dBm. The linearity of this design is dominated by the performance of the LNA and could be improved by replacing $R_1$ with an RF choke and using lower supply voltage to avoid transistor breakdown.

As designed, the phase shifter has a bandwidth of 1 GHz centered around 11.5 GHz. This is limited by the allowable amplitude and phase ripple over changes in the phase states and is determined by the phase shift per stage of the constant impedance network. Currently four stages are used with 45° per stage. The bandwidth could be increased by making the network more distributed and using eight stages with 22.5° per stage at the expense of more area. A summary of the simulated and measured results are shown in Table 4.1.

Although this phase shifter has an analog control function, individual control of the the phase shift cells can be done to synthesize a 4-bit digital phase shifter. Referring to Fig. 4.7, the analog control lines for two of the phase shift cells are tied together to implement a

[1] see Appendix B

| | Simulated | Measured |
|---|---|---|
| Supply Voltage [V] | 5 | 5 |
| Supply Current [mA] | 10.2 | 10.7 |
| Center Frequency [GHz] | 12.2 | 11.5 |
| Gain [dB] | 7.2 ± 0.6 | 3.7 ± 0.5 |
| Noise Figure [dB] | 3.7 | 4.4 |
| 1-dB compression [dBm] | -25.0 | -27.3 |
| IIP3 [dBm] | -15 | -17.3 |
| Area with Pads [$mm^2$] | – | 1.48 |
| Area without Pads [$mm^2$] | – | 1.1 |

Table 4.1: Comparison between simulated and measured performance of the phase shifter with integrated LNA.

| Bias Point | (1) | (2) | (3) |
|---|---|---|---|
| Phase [deg] | -90 | -45 | -22.5 |
| Voltage [V] | 2.15 | 2.3 | 3.0 |

Table 4.2: Analog voltages to produce digital-like behavior by controlling the phase shifter cells independently. All cells result in 0° relative phase when biased at 5 V.

90° bit. The other two cells can correspond to the 45° and 22.5° bits. The required bias voltages are presented in Table 4.2.

The voltages of Table 4.2 were applied manually to simulate a 4-bit phase shifter. The measured relative phase shift is shown in Fig. 4.13a. Fig. 4.13b shows the phase variation when the phases are normalized to their ideal digital values. This reveals that there is an 18° phase error on the 180° bit, and may be due to the fabrication tolerance of the MIM capacitance layer used for $C_{HP}$. If $C_{HP}$ is implemented as an oxide capacitor similar to $C_{LP}$, this error may be eliminated.

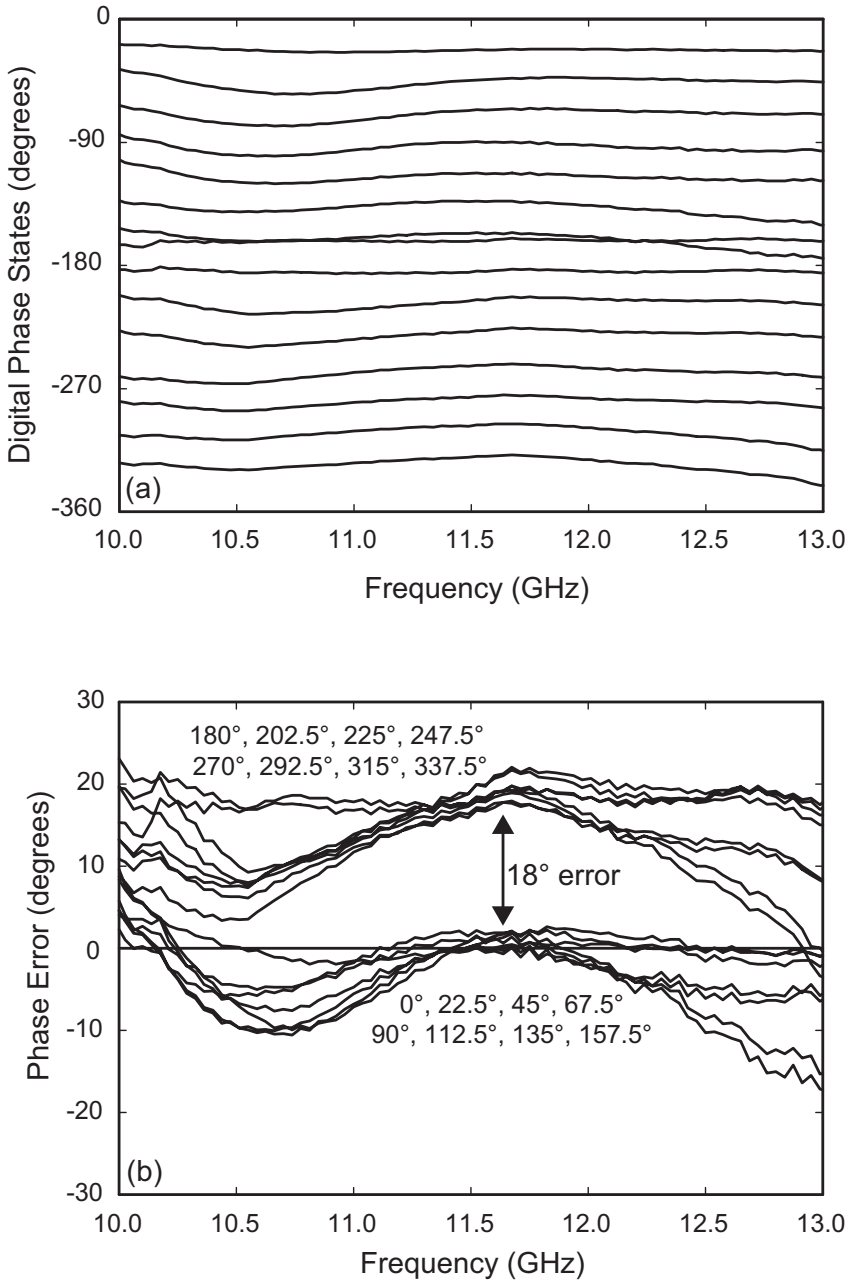



Figure 4.13: Measured relative phase (a) of the 16-states when the phase shifter is tested in a digital fashion, (b) normalized to the corresponding 4-bit digital values (0°, 22.5°, 45°, etc.).

## 4.7 Conclusion

This chapter has presented the design and measurement of a 12 GHz phase shifter with integrated LNA in SiGe. A digital 180° phase shift is integrated into the LNA using a switched high-pass/low-pass network. The remaining phase shift is achieved with an analog phase shifter using varactors that implements a novel *constant-impedance* tuning technique that tunes the phase while simultaneously compensating for mismatch introduced by the phase shift. The phase shifter has a measured gain of $3.7 \pm 0.5$ dB at 11.5 GHz with a noise figure of 4.4 dB. The phase shifter has more than 360° of phase shift and the relative phase shift is flat with frequency within ±10° over more than 1 GHz of bandwidth centered at 11.5 GHz. The analog control lines for individual phase shifter cells were also be adjusted independently to demonstrate that a 4-bit digital phase shifter could also be implemented with good performance.

# CHAPTER 5

# Conclusion

## 5.1 Summary of Work

This thesis has given design examples in the emerging field of *silicon MMIC design*. Voltage controlled oscillators and sub-100 ps RF switching networks at 24 GHz as well as a 12 GHz phase shifter have been demonstrated in a SiGe bipolar process. These designs draw upon both RFIC and MMIC techniques to meet the objective of demonstrating the design and analysis of high performance SiGe microwave components at frequencies in the range of 12-24 GHz

Chapter 2 provides an overview of the design and optimization of Voltage Controlled Oscillators (VCOs) at microwave frequencies followed by a design example. The VCO design uses the extensive body of work at low RF frequencies to optimized the VCO for K-band operation. In doing this, a novel differential circular inductor was designed for use in the LC resonator. The compact differential VCO at 22.8 GHz has an average output power of 2.2 dBm, a SSB phase-noise of -104 dBc/Hz at 1 MHz offset and a FOM of -175 dB while maintaining a small footprint of only $230 \times 290\,\mu\text{m}^2$.

A new quadrature oscillator topology is also presented in Appendix A. A novel super-harmonic bilateral coupling network is used to mutually injection lock two 6 GHz oscillators, forcing the two oscillator outputs into a quadrature phase state. The coupling network does not decrease the tuning range or increase the power consumption and the phase-noise is decreased by 3 dB as predicted by coupled-oscillator theory. The QVCO has a 24% tuning range with a maximum output frequency of 5.92 GHz and an average output power of -5.3 dBm.

Chapter 3 introduces a new RF switching network and presents its design, analysis and measurement. The proposed circuit topology implements a differential absorptive SPDT switching circuit at 24 GHz. An RF envelope switching time of 70 ps is achieved through the use of differential current steering of the RF signal path. The switching time of the RF envelope is analyzed analytically and agrees well with simulated and measured results. The SPDT switch achieves 1.9 dB of gain in the pass band and an isolation of 35 dB while remaining matched at its ports (absorptive).

Phase shifters are one of the most expensive microwave components in a phased array system due to the large number of elements required and their implementation in III-V technology. Chapter 4 presents the design and measurement of a 12 GHz phase shifter with integrated LNA in a SiGe bipolar process. Most phase shifter networks rely on a true switching element such as a FET or a quality diode, neither of which are available in a bipolar process. To achieve a solution to this problem, a digital 180° phase shift is integrated into the LNA using a switched high-pass/low-pass network. Two cascode stages in the LNA implement the SPDT function. The remaining phase shift is achieved with an analog phase shifter using varactors that implement a novel *constant-impedance* tuning technique which tunes the phase while simultaneously compensating for mismatch introduced by the variable load capacitance. The complete phase shifter chip has a measured gain of $3.7 \pm 0.5$ dB at 11.5 GHz with a noise figure of 4.4 dB. The phase shifter has more than 360° of phase shift and the relative phase shift is flat with frequency within $\pm 10°$ over more than 1 GHz of bandwidth centered at 11.5 GHz.

## 5.2 Future Work

Although the majority of the the work in this thesis is motivated by automotive radar applications at 24 GHz, it is applicable on a much broader scale. In the next decade military applications (and some commercial) at X and K-band will look to silicon technology to revamp the current microwave systems. The work in this thesis has focused on the use of SiGe bipolar transistors only, however there is a significant value added in using a SiGe BiCMOS process that allows the designer to use sub-micron CMOS transistors where needed.

### 5.2.1 Voltage Controlled Oscillators

At low RF frequencies the resonant frequency of a VCO is determined primarily by the passive components that make up the LC resonator. Inductance values are relatively constant over process and temperature variation and a thin film capacitor typically has a $\pm 10\%$ tolerance in its capacitance value. If this is the dominant capacitance in the resonator, the frequency will vary by about $\pm 5\%$. As the frequency of oscillation increases, the junction capacitances of the active device and any tuning elements (such as varactors) introduce more process and temperature variation. This pushes the variation of the oscillation frequency from $\pm 7\%$ to $\pm 9\%$ requiring that the VCO have a tuning range of at least 15% to 20% to cover process and temperature variation so that the yield is not degraded. A reduced yield may be acceptable for niche markets (military) where testing and sorting can be a solution. However in commercial applications, high yields are imperative to making a viable product. This leads to the need for work in the area of wideband VCO design. One approach that has been looked at is the use of digital tuning in BiCMOS VCOs. It is clear that the marriage of SiGe and CMOS can lead to new generation of *smart microwave circuits* that automatically detect and correct for degradations in performance due to changes in process, temperature, etc. without intervention from the outside user.

### 5.2.2 Ultrawideband RF Switching Circuits

It has yet to be determined that the use of a pulsed UWB system for communications is the right direction for the 3.1-10.6 GHz band opened by the FCC in 2002. However, it is clear that pulsed UWB systems lend themselves well to radar applications. This is no more evident than in the UWB automotive radar band (22-29 GHz). By 2006 there will be 24 GHz low-cost pulsed radar solutions on the market, fully integrated in silicon technology. Although the 24 GHz band is reserved for vehicular applications, the concept can be used at any frequency. There already exist through-the-wall radar imaging systems with limited resolution for police and military use. This can be improved upon and extended to other applications such as medical imaging, and perhaps even turned turned into a therapeutic modality such as microwave ablation of tumor sites. Some of the challenges in accomplishing these goals are at the circuit level as well as the system implementation. The speed of pulse formation will continue to scale with active device technology, however wideband passive

microwave circuitry is necessary. In addition, efficient power amplification of low duty cycle RF pulses with flat group delay may be a challenge to implement. As for system design, high levels of silicon integration should afford the use of more complex architectures that may improve processing gain such as the ability to dwell on multiple targets simultaneously.

### 5.2.3 Phase Shifters

There is an immense body of work on III-V MMIC phase shifter designs available in the literature as well as devices in production. Using some of these tested techniques in silicon will allow for increased yield and decreased cost. A CMOS FET can be used in a similar fashion to a MESFET or HEMT to implement numerous phase shifter and true-time delay designs, but the real value added to the system is the addition of the CMOS. As mentioned before this could lead to *smart microwave circuits* that operate in a more autonomous fashion. Currently, phase shifter MMICs have the required microwave circuits and a serial interface to load the desired phase state. With CMOS available on chip, it could be possible to add more functionality, such as memory to store phased-array calibration coefficients. Perhaps the level of integration can be pushed even further to add more signal processing such that eventually the signal is detected and sampled all on the same chip.

# APPENDICES

# APPENDIX A

# A Novel Superharmonic Coupling Topology for Quadrature Oscillator Design at 6 GHz

## A.1 Introduction

In today's complex radio architectures, it is often necessary for the local oscillator in a transceiver to produce two tones with a quadrature phase relationship. This can be done with a single oscillator and an RC-CR poly-phase filter but introduces loss and quadrature mismatch [65]. An alternative method is to use a VCO at twice the desired frequency and use frequency division to produce two outputs in quadrature [66]. Both of these techniques result in a need for additional power consumption as the frequency of oscillation increases.

A third technique for obtaining quadrature is to couple two oscillators such that their outputs are locked together in quadrature. One coupling method uses a parallel coupling scheme which tends to result in poor phase-noise performance [67]. This additional phase-noise has been addressed in [68] and [69] by using phase shift networks to optimize the coupling. In addition to the parallel coupling topology, several series coupling topologies have been implemented with good results [70, 71, 72]. All of these QVCOs use coupling at the fundamental frequency of operation and the added coupling transistors introduce unwanted parasitics, increase the power consumption and degrade the phase-noise.

Another type of coupled oscillator couples the second harmonic of two VCOs such that the fundamental frequencies are in quadrature. This coupling has been achieved using large passive networks. This paper presents a novel superharmonic coupling scheme that does not degrade the oscillator performance and is significantly smaller than the passive networks used in [73] and [74].

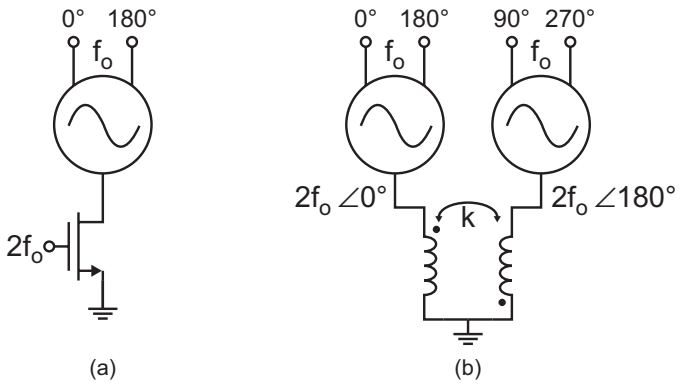



Figure A.1: Schematic of (a) the injection locking a differential oscillator at one of its common mode nodes and (b) the mutual injection locking of two differential oscillators with a large passive network.

## A.2 Injection Locked Oscillators

The phenomenon of injection locked oscillators is well known. In general, an oscillator with a natural frequency $f_o$ can be injected with an external stimulus at a frequency that is harmonically related to $f_o \pm \Delta f$ where $\Delta f$ is some locking bandwidth. The dynamics of this injection locking has been analyzed in the context of injecting a signal at $2f_o$ to lock an oscillator at its natural frequency for use as an analog frequency divider [75].

With the proliferation of differential oscillators in RFIC/MMIC design, it became apparent that the second harmonic circulating in the circuit appears at common mode points in the circuit. These common mode points make ideal nodes to inject a signal at twice the natural frequency of the oscillator (Fig. A.1a). The work published in [73] and [74] take advantage of this phenomenon and use a passive network to mutually injection lock two oscillators together. The passive network imposes a 180° phase shift between the second harmonics of the two oscillators, thus enforcing quadrature at the fundamental frequency (Fig. A.1b). Both [73] and [74] use large on-chip transformers wound in an anti-phase configuration to couple the two oscillators at the second harmonic.

## A.3 Circuit Design

This work presents a novel coupling topology that does not use a transformer, but rather makes use of transistors that are already present in many differential oscillators. Fig. A.2

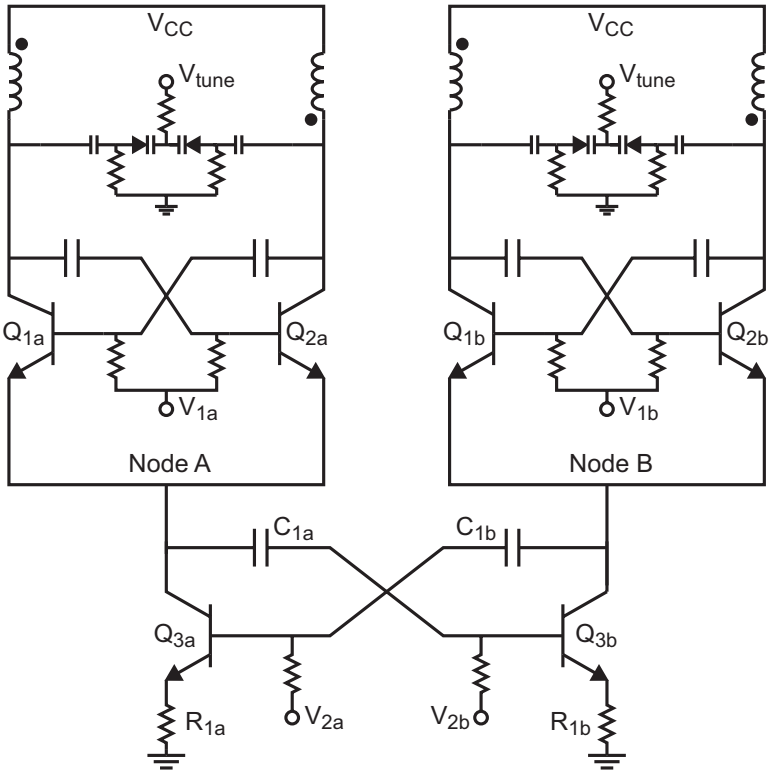



Figure A.2: Schematic of the new quadrature VCO topology using the current sources to bilateral injection lock two VCO cores.

shows the topology of the two coupled oscillators (output buffers omitted for simplicity). The oscillator design is a standard cross-coupled differential pair that uses a differential inductor that has a simulated differential value of 2 nH with a simulated Q of 27 at 6 GHz. The varactors have a minimum value of 520 fF at a reverse bias of 5 V. They have a tuning ratio of 3.3:1 from 0-5 volts and a Q based on device models that ranges from 45 to 60 at 6 GHz.

The two oscillators are mutually injection locked to each other at their second harmonic by connecting node A and node B with the proper coupling network. Rather than use a large on-chip transformer as done in [73] and [74], the two oscillators are capacitively coupled through their current sources. The current sources are implemented with transistors $Q_{3a}$ and $Q_{3b}$ and are degenerated by resistors $R_{1a}$ and $R_{1b}$.

The degeneration decreases the transconductance of $Q_3$ which serves two purposes. First, it decreases the noise contributed by $Q_{3a}$ and $Q_{3b}$ to a point that they do not affect the overall phase-noise performance of the oscillator. Second, the reduction in transconductance

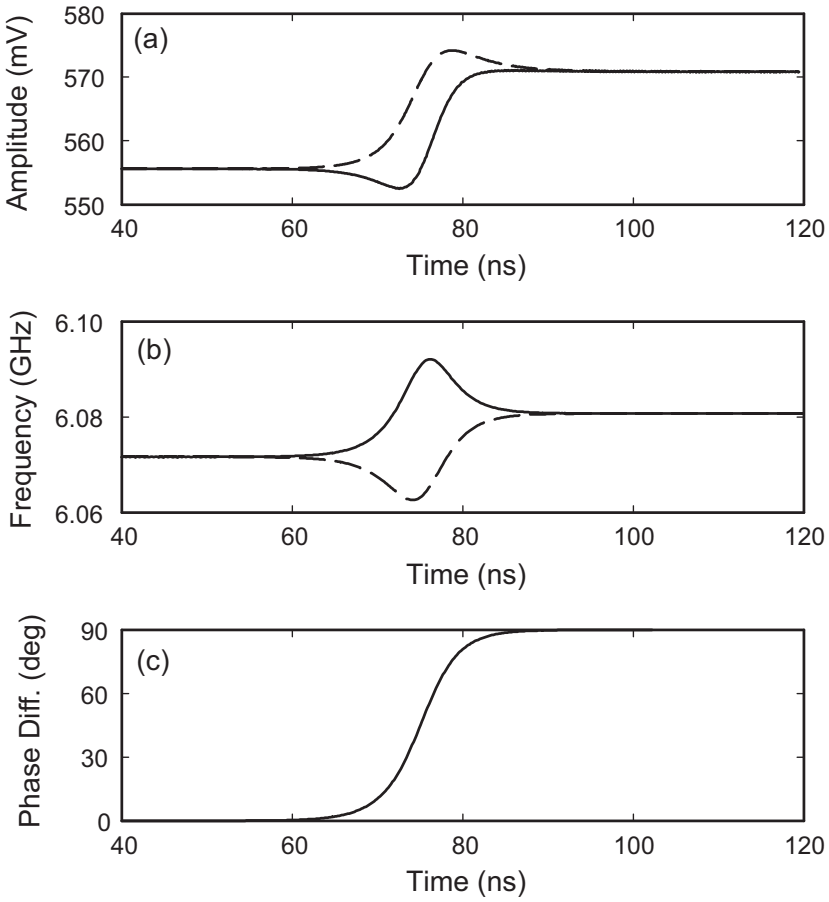



Figure A.3: Simulated start-up transients of the in-phase and quadrature differential outputs showing quadrature locking, (a) envelope amplitude, (b) frequency, (c) phase difference.

is necessary for stability. The transconductance must be reduced through the combination of base and emitter degeneration by $C_1$ and $R_1$ respectively such that the loop gain from the collector of $Q_{3a}$ through $C_{1a}$, $Q_{3b}$, $C_{1b}$ and back to the collector of $Q_{3a}$ is less than one. If the loop gain is greater than one, then a parasitic oscillation at nodes A and B occur resulting in an AM modulated output waveform.

When the tail current sources $Q_{3a}$ and $Q_{3b}$ are cross-coupled with capacitors $C_{1a}$ and $C_{1b}$, a bilateral coupling network is formed that forces the second harmonic at node A and node B to be 180° out of phase. In reality, the phase relationship between the base and collector of $Q_3$ is not exactly 180°. Nevertheless, because of the non-linear nature of injection locking, lock can still occur if the natural frequency of two oscillators are close to each other. This can be explained intuitively by considering the voltages at node A and

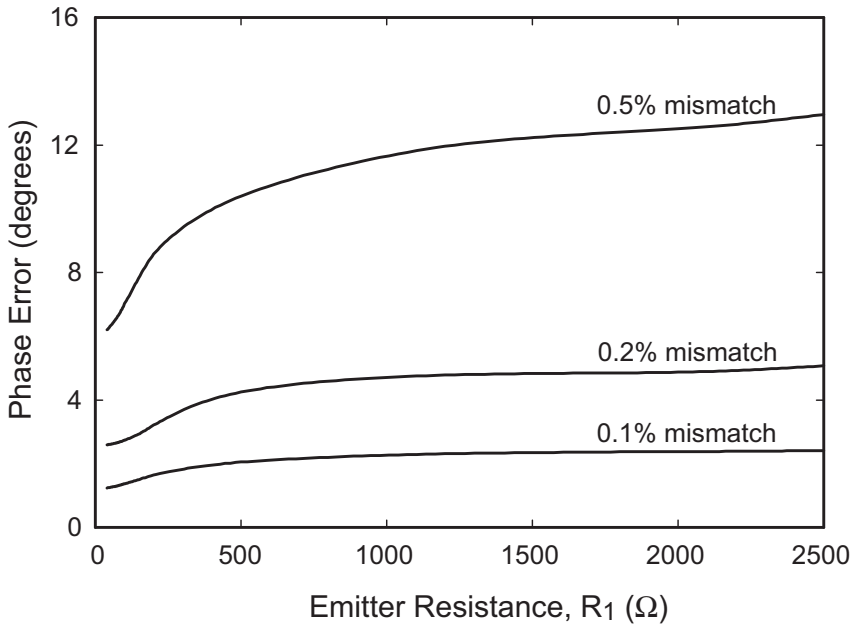



Figure A.4: Simulated phase error for different values of emitter resistance in the presence of oscillator resonator mismatch. The resonator mismatch was simulated as a small percentage change in the tank inductance, and would be the same for a small change in the tank capacitance.

node B. If initially nodes A and B were to start in-phase, the cross-coupling would try to force them to 180°, but in reality would achieve something less than 180° during the first period. During each successive period, there is less of a phase error and the cross coupling slowly forces the two nodes to be 180° out of phase. This can be verified with simulation by forcing the two oscillators to start in-phase as shown in Fig. A.3. As the simulator's numeric noise creates small perturbations in the waveforms, the coupling forces the two oscillators into quadrature. This happens when both oscillators adjust their amplitude and frequency until lock is achieved. These start-up transients are similar to those presented in [74] where a transformer is used for the superharmonic coupling.

Perfect quadrature can only be achieved if the two oscillators match identically. However, for small resonator mismatches, the cross-coupling will still lock the the two oscillators in quadrature with a small phase error. The phase error is related to the strength of the cross-coupling and is a function of the transconductance of $Q_3$ with $R_1$ in the emitter and $C_1$ in the base. The capacitance $C_1$ was chosen to be 1 pF because it is the largest capacitance that can be implemented with a self-resonant frequency greater than the $2f_o$ of

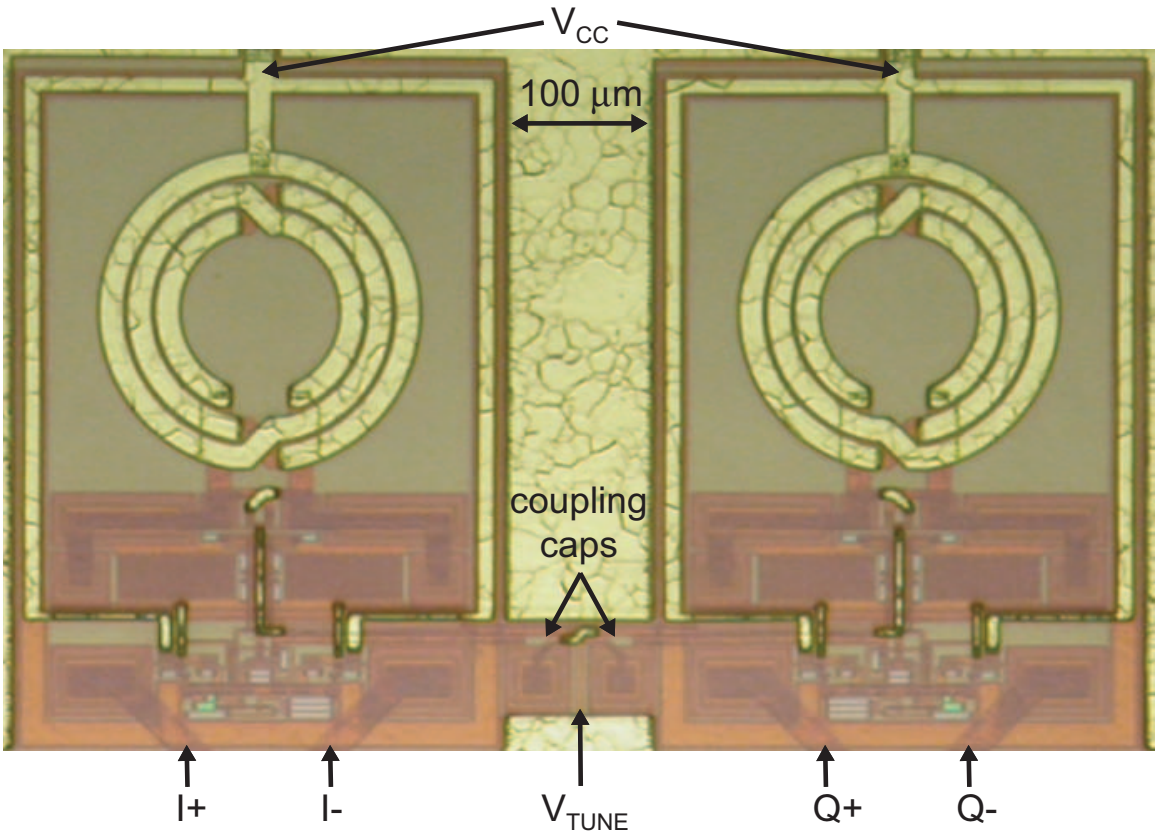



Figure A.5: Micro-photograph of differential QVCO without pads ($810\,\mu$m $\times$ $485\,\mu$m).

12 GHz. The value of $R_1$ can be adjusted to increase the transconductance and reduce the phase error. Fig. A.4 shows the simulated variation in the phase error for different values of $R_1$ for different tank mismatches. A value of 1.2 k$\Omega$ was chosen for $R_1$ because this was the value needed to obtain the desired bias point with a 5 V supply voltage.

## A.4 Measured Results

The QVCO was fabricated in Atmel's SiGe2-RF process, described in Chapter 1. Fig. A.5 shows a micro-photograph of the circuit without pads with dimensions $810\,\mu$m $\times$ $485\,\mu$m. The output power and frequency were measured on-chip using differential RF probes and a 0/180° hybrid was used as a balun. The output power was corrected for probe, coupler and cable loss. In addition, a single VCO was measured to see the effect of the superharmonic coupling on the output power and tuning characteristic (Fig. A.6). Both the VCO and QVCO have a tuning range of 24% with a maximum output frequency of 5.92 GHz

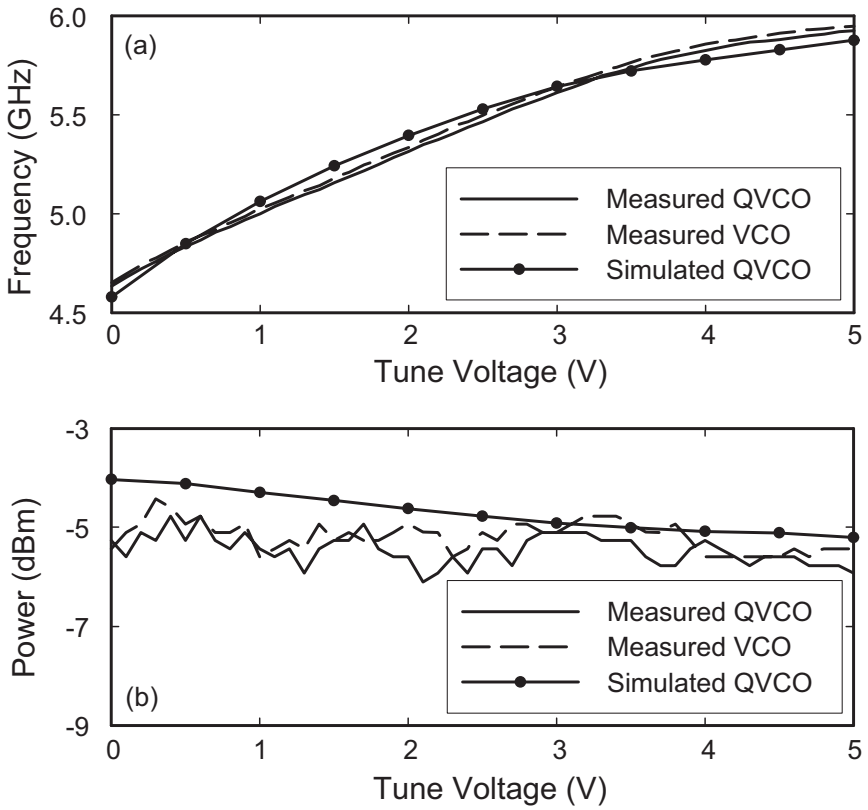



Figure A.6: Measured tuning range of the QVCO and VCO, (a) frequency, (b) power.

and an average output power of -5.3 dBm across the tuning range. This indicates that the superharmonic coupling does not effect the output power or the tuning range of the QVCO.

The QVCO was designed to have approximately 7 dB more output power, but at the time of design the model for the nitride capacitor in the design kit did not properly model the behavior at 6 GHz. The previous design kit modeled the substrate parasitics as a lossless capacitor and all of the loss was lumped into a resistor in series with the nitride capacitor. In the new design kit, the substrate is more accurately modeled as a lossy RC network. The capacitors are used in several places for DC blocking as well as to couple the varactors to the oscillator tank. Simulations using the previous design kit indicated that the complete oscillator tank would have a Q of 15.9 while simulations with the updated design kit indicate that the tank has a Q of 6.4 and could have been corrected by re-sizing some of the devices. Post-measurement simulations were run with the new design kit and show good agrement with the measured power and frequency (Fig. A.6).

Quadrature operation was verified by using a sampling oscilloscope to measure the quadrature outputs. The oscilloscope was calibrated to compensate for channel delay mis-

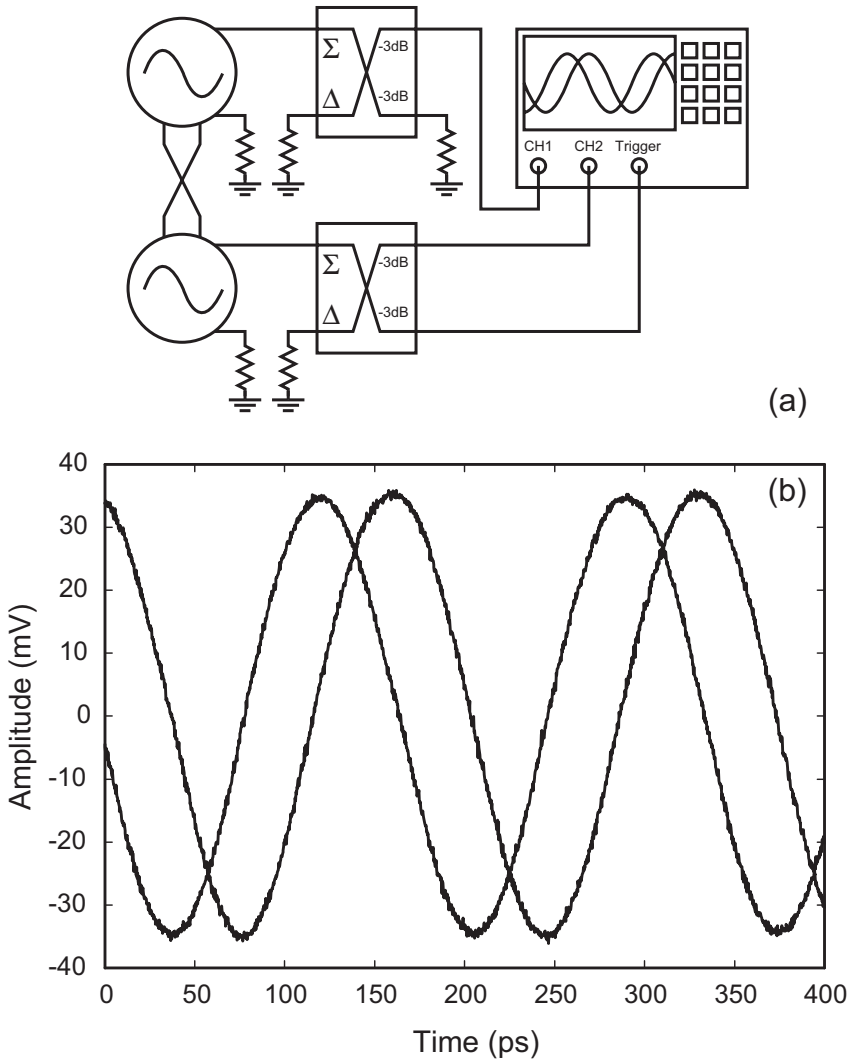



Figure A.7: Measurement of quadrature accuracy with digital sampling oscilloscope (a) test setup, (b) measured waveforms.

match and is accurate to 1 ps. At a frequency of 6 GHz this corresponds to a phase accuracy of approximately $\pm 2^{\circ}$. Fig. A.7a illustrates the test setup where a trigger signal was generated by placing identical 3 dB couplers in the signal paths where one of the coupled ports is used to trigger the oscilloscope. Fig. A.7b shows the measured waveforms where the deviation from quadrature is measured to be $4^{\circ}$ which corresponds to an image rejection ratio of 29 dB. To confirm this result, the image rejection was measured directly using matched off-chip mixers to up-convert a 10 MHz I and Q IF signals and measure the difference between the lower and upper sidebands (Fig. A.8). With this technique an image rejection of 28 dB was measured, and agrees well with the results obtained using the sampling oscilloscope.

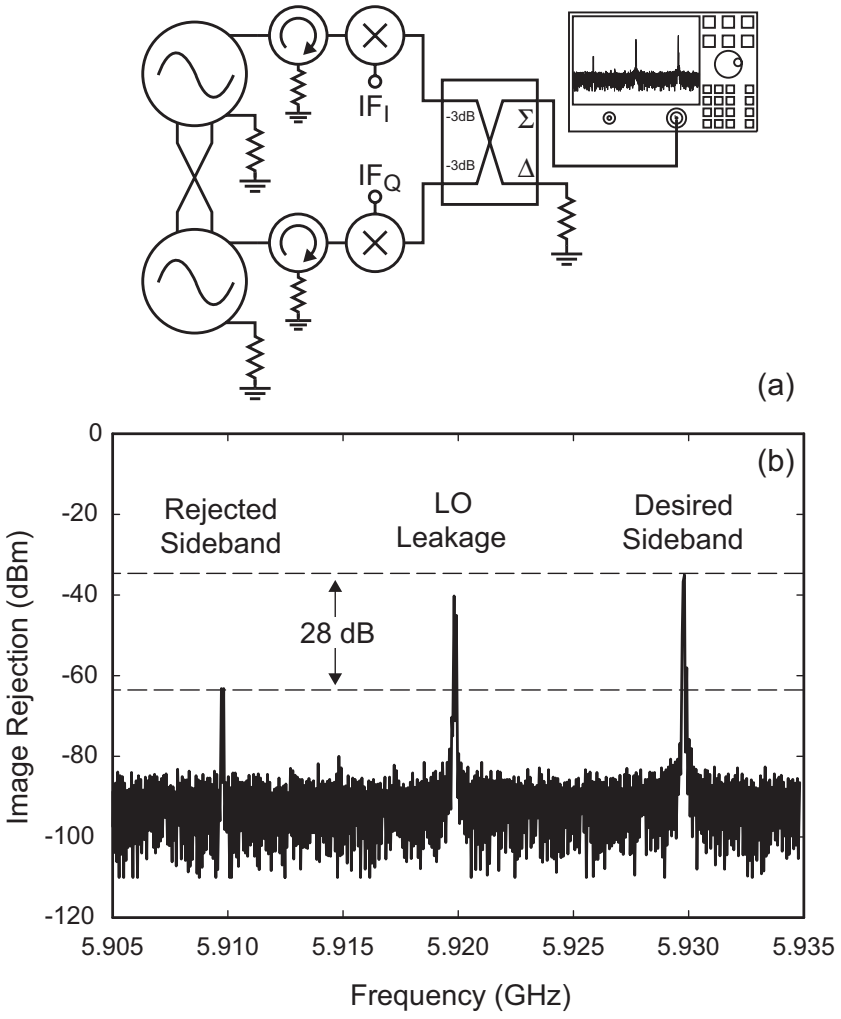



Figure A.8: Measured image rejection using two matched off-chip mixers, (a) test setup and (b) upper and lower sidebands.

The phase-noise of the QVCO and VCO were both measured, however as mentioned before, at the time of design the model for the nitride capacitor did not accurately represent its performance. For this reason, the measured phase-noise is worse than what was simulated at the time of design. The measured performance of the single VCO is -102.5 dBc/Hz at 1 MHz offset from the 5.92 GHz carrier. This is very close to the post-measurement simulation in ADS 2003a of -103.7 dBc/Hz. The total circuit consumed 11.8 mA from a 5 V supply, 4.8 mA was used for each buffer and the oscillator core only consumed 1.4 mA.

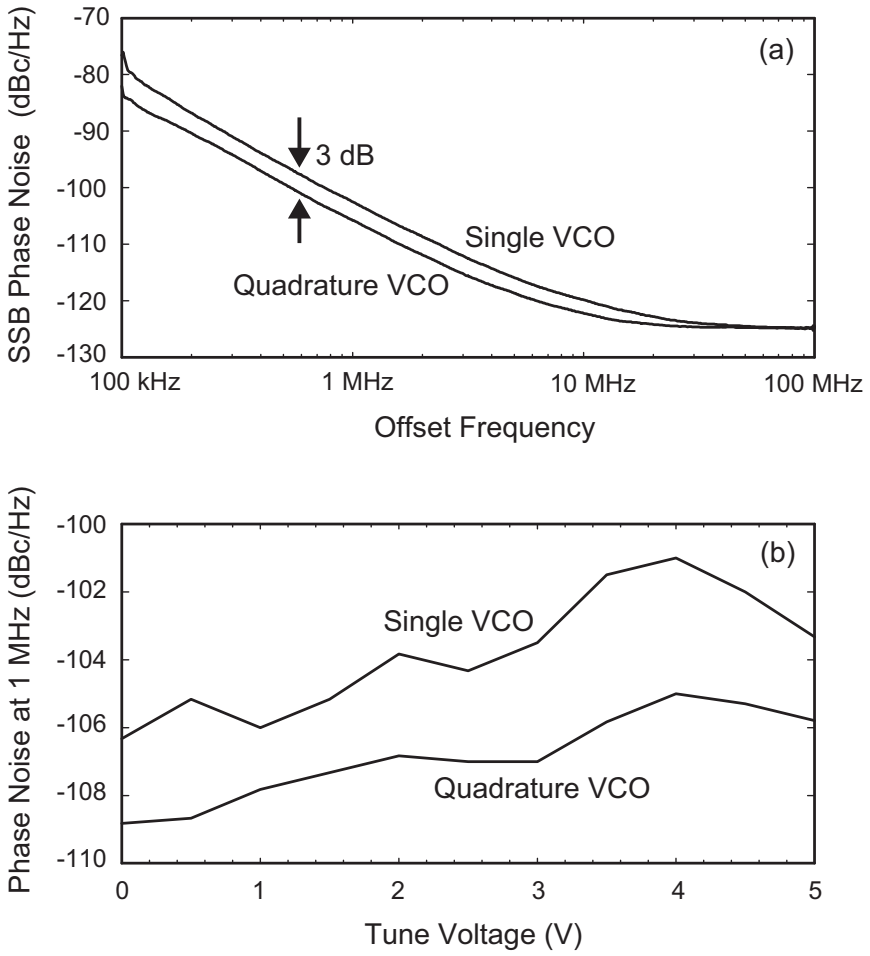



Figure A.9: Measured phase noise (a) as a function of offset frequency and (b) across the tuning range.

The figure of merit for the VCO is $-170$ dB calculated according to the expression [36]

$$FOM = 10\log\left(\left(\frac{f_c}{\Delta f}\right)^2 \frac{1}{\mathcal{L}(\Delta f)\, P_{core}}\right) \tag{A.1}$$

where $f_c$ is the frequency of oscillation, $\Delta f$ is the offset frequency and $P_{core}$ is the power dissipated in the oscillator core in milliwatts.

The phase-noise of the QVCO was measured to be -105.8 dBc/Hz at 1 MHz offset from a 5.92 GHz carrier (Fig. A.9a). This is 3 dB lower than the single VCO and is a consequence of the bilateral injection locking of the two identical oscillators and indicates that the superharmonic coupling does not increase the phase-noise over the performance of the single VCO [76]. The phase-noise of the QVCO at 1 MHz offset was measured across its tuning range and it is better than -105 dBc/Hz across the band (Fig. A.9b). The phase-

| | Technology | Tuning Range [%] | VCO Core DC Power [mW] | $L_{SSB}$ at 1 MHz [dBc/Hz] | FOM [dB] | Size (no pads) [mm$^2$] |
|---|---|---|---|---|---|---|
| van der Tang [69] | Si | 6 | 21.2 | -107 | -168 | 2.128 |
| Gierkink [74] | CMOS | 13 | 22.0 | -125 | -185 | – |
| Chang [71] | CMOS | 20 | 5.8 | -115 | -183 | 0.588 |
| **This work** | **SiGe** | **24** | **14.0** | **-106** | **-170** | **0.393** |
| Revised design | SiGe | 17 | 28.8 | -121 | -182 | – |

Table A.1: Comparison of 5-6 GHz monolithic QVCOs.

noise tends to decrease with tune voltage and frequency resulting in a nearly flat figure of merit over the tune range.

Had the new model for the nitride capacitor been available at the time of design, the oscillator could have been designed to provide better phase-noise performance. By decreasing the size of the coupling capacitor in series with the varactors from 2 pF to 1 pF and doubling the VCO core current, the VCO phase-noise is decreased by 15 dB in simulation. The decrease in the size of the coupling capacitor only reduces the tuning range from 24% to 17%. The FOM for this simulated result is comparable to the work presented in [71, 74]. A comparison of the recently published QVCOs in the 5-6 GHz range are shown in Table A.1.

## A.5 Conclusion

A novel superharmonic bilateral coupling topology has been presented to mutually injection lock two 6 GHz oscillators together forcing the two oscillator outputs into a quadrature phase state. The QVCO was implemented in a commercial SiGe process along with a single VCO for comparison. The QVCO layout is compact occupying an area of only $810\,\mu$m $\times$ $485\,\mu$m without pads. Based on measurements of the VCO and QVCO, the coupling does not decrease the tuning range or increase the power consumption and the phase-noise is decreased by 3 dB as predicted by coupled oscillator theory. The QVCO has a 24% tuning range with a maximum output frequency of 5.92 GHz and an average output power of -5.3 dBm.

# APPENDIX B

# Design of a Differential 24 GHz Phase Shifter

## B.1 Introduction

The differential design of RF circuits offers advantages over their single-ended counterparts such as reducing parasitic ground inductance/resistance and improving the immunity to common mode noise and interference from other circuits on the same chip. Chapter 4 discussed the importance of phase shifters in microwave systems, so it is a natural next step to implement a similar phase shifter topology in a differential fashion. This appendix will discuss the design and measurement of a differential 24 GHz phase shifter in SiGe.

## B.2 Circuit Design

Using the methodology presented in Chapter 4, a two tier approach was taken to implement a complete phase shifter. First an LNA with digital 180° phase shifter is designed followed by an analog phase shifter with 180° of variation over a 4 V tuning range (Fig. B.1). The digital phase shifter is implemented with a Gilbert cell to provide a precise phase shift in a small area. The complete circuit consumes 32 mA from a 5 V supply and the bias currents were chosen for an input P1-dB of −10 dBm. The input and output ports of the LNA/180°-bit are matched to 100 Ω differentially with $L_1$, $L_3$, $C_1$, $C_2$ and $C_3$ where all of the inductors have a simulated Q of approximately 15 at 24 GHz. The LNA and Gilbert cell are DC coupled together to avoid using a lossy blocking capacitor and interstage matching is provided by $L_2$. The LNA/180°-bit have a simulated gain of 14.3 dB and noise figure of 6.5 dB at 24 GHz.

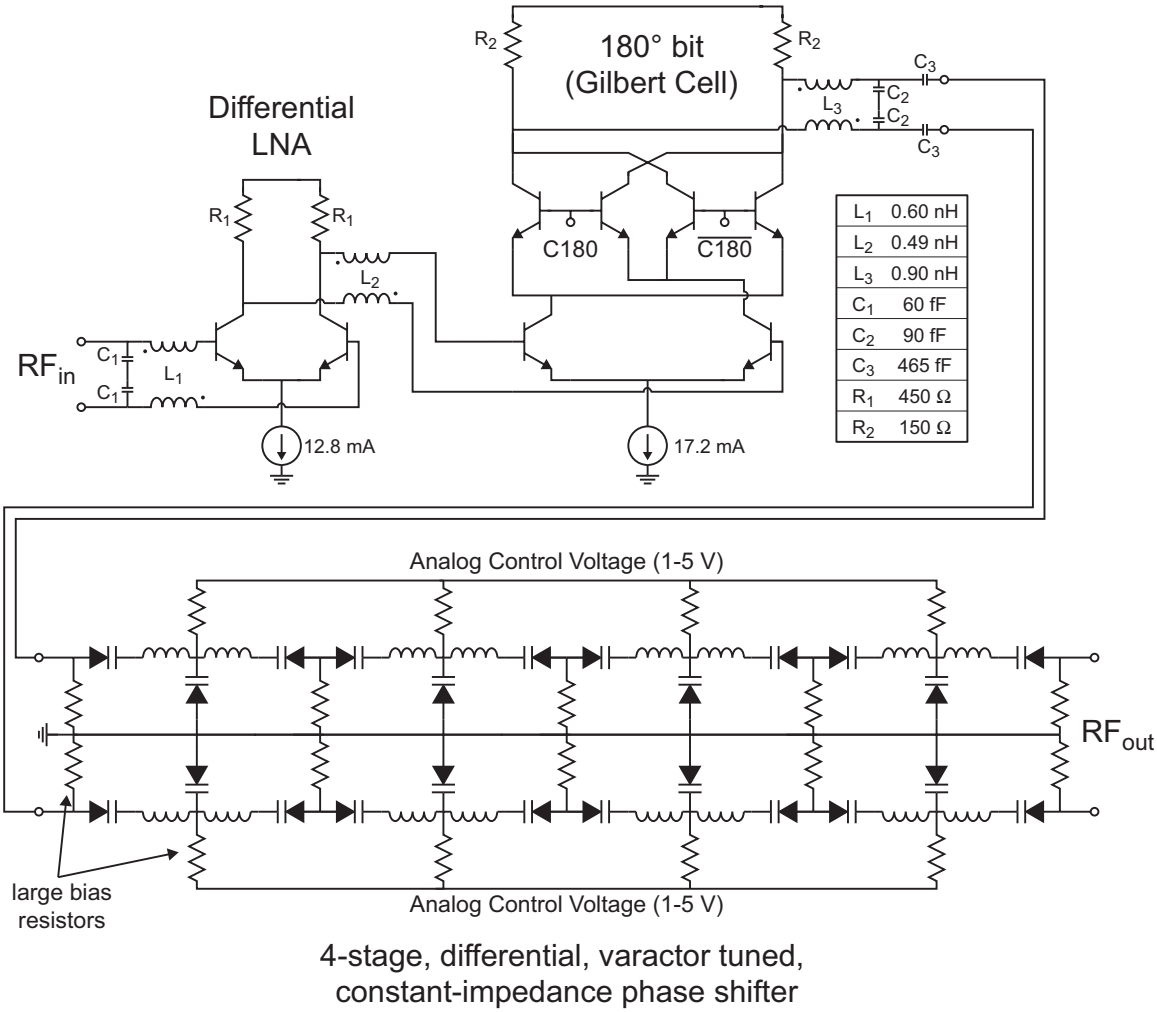



Figure B.1: Schematic of differential 24 GHz phase shifter in SiGe implemented with an LNA/180°-bit (Gilbert cell) followed by a 4-stage analog phase shifter.

Following the LNA/180°-bit are four analog phase shifter cells, each provide a relative phase shift of 45° over a 4 V tuning range. The differential series inductor in the analog phase shifter is 0.48 nH with a Q of 15 at 24 GHz. The shunt varactor is $2 \times 4\,\mu\text{m} \times 25\,\mu\text{m}$ providing a capacitance range of 125:220 with a Q of 10-20 at 24 GHz. The series varactor is twice the junction area of the shunt varactor. Each 45° cell has a simulated insertion of loss of 2 dB at 24 GHz. When the LNA/180°-bit is cascaded with the four analog phase shifter cells, the overall gain is $6.2 \pm 0.2$ dB with a noise figure of 6.7 dB and good input and output return loss (Fig. B.2). The insertion phase is linear with frequency and the relative phase shift is constant with frequency as expected for a lumped phase shifter design.

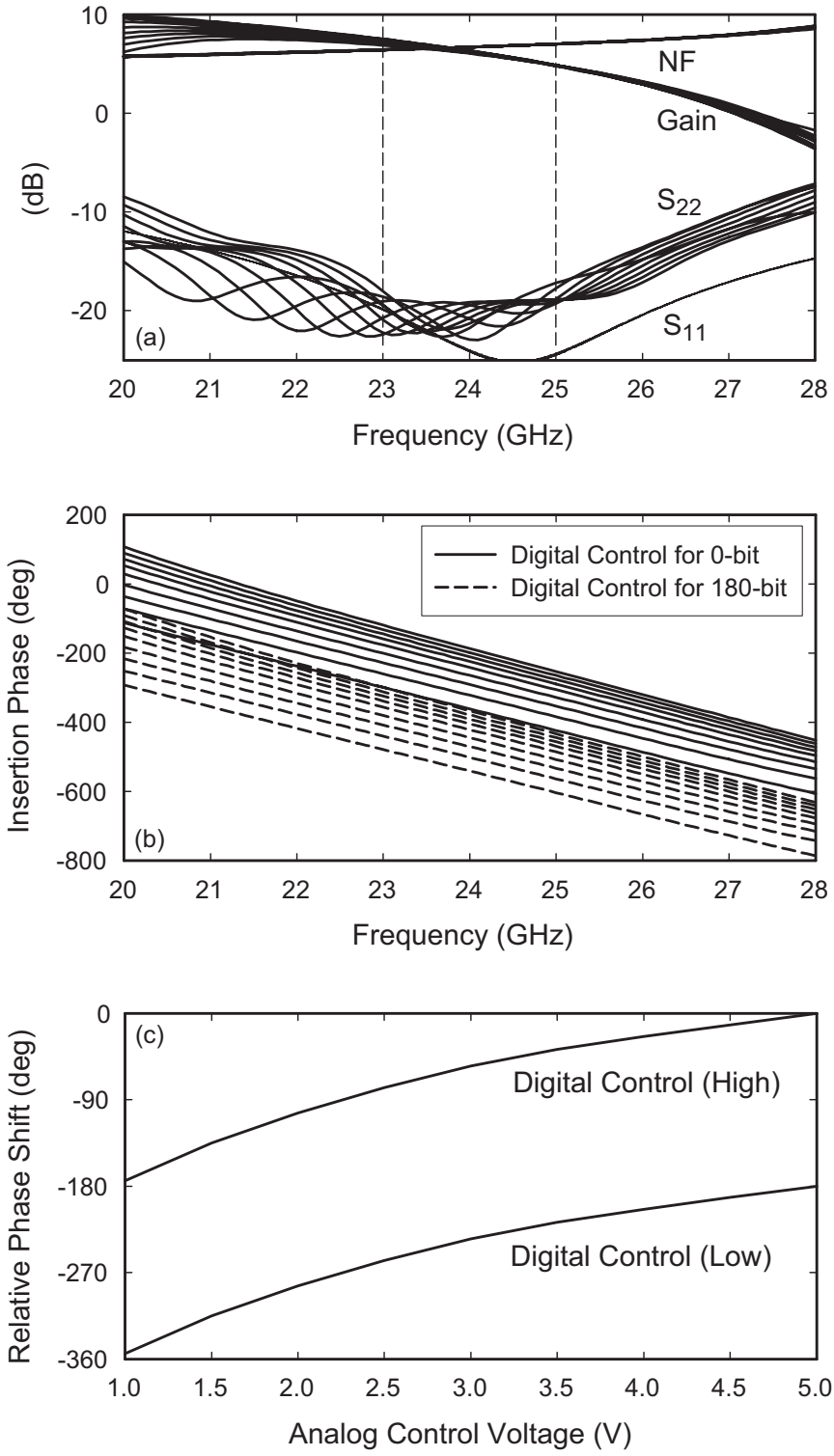



Figure B.2: Simulation results of 24 GHz phase shifter (a) gain, noise figure and return loss, (b) insertion phase and (c) relative phase shift at 24 GHz.

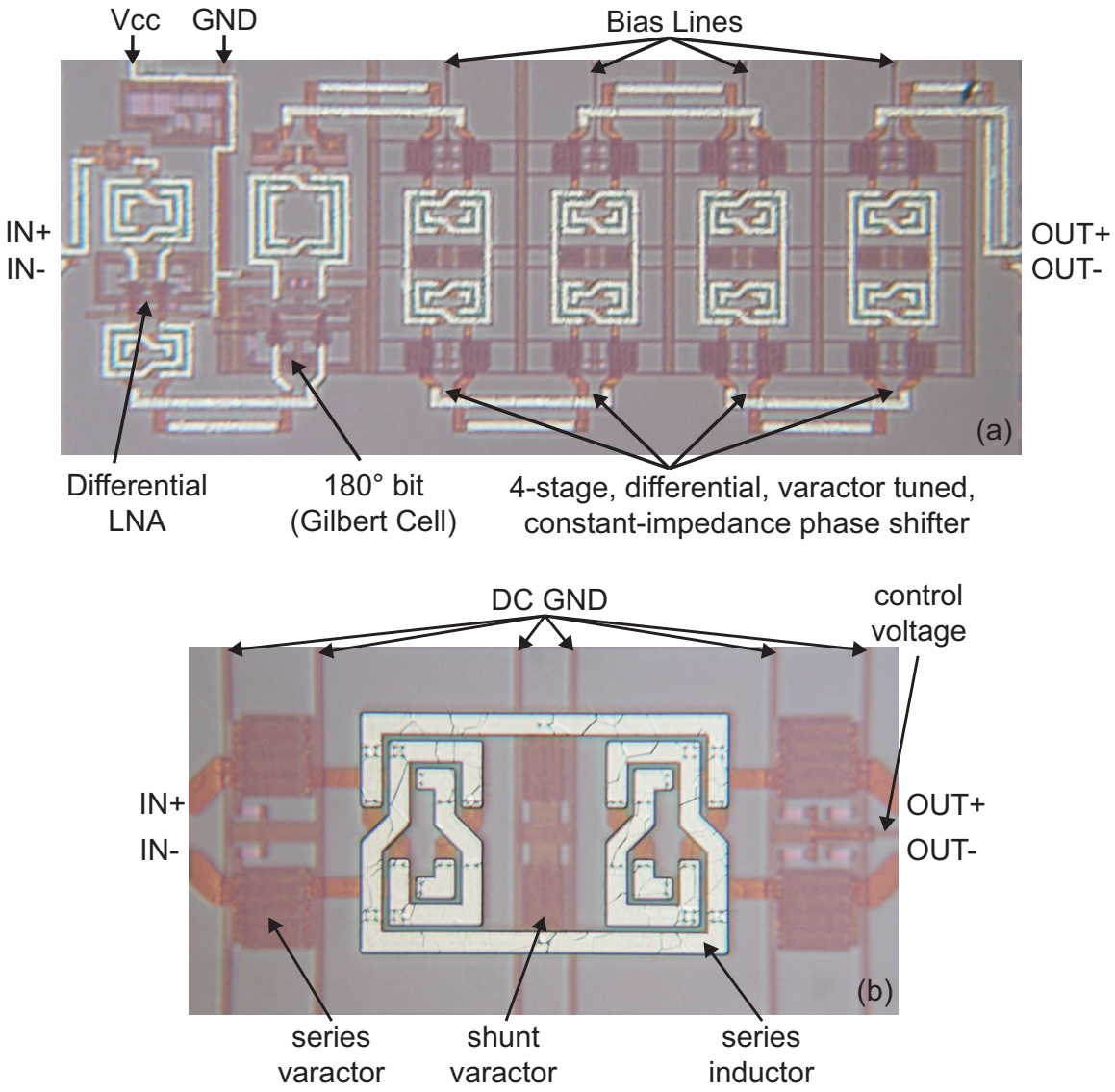



Figure B.3: Micro-photograph of (a) differential 24 GHz phase shifter ($1120 \times 415\,\mu\text{m}^2$) and (b) a single 45° analog phase shift cell ($310 \times 140\,\mu\text{m}^2$).

## B.3 Measured Results

The differential 24 GHz phase shifter was fabricated in Atmel's SiGe2-RF process described in Chapter 1. The area of the active circuitry (without pads) is $1120 \times 415\,\mu\text{m}^2$ (Fig B.3a). The phase shifter was designed using EM simulation in Sonnet to account for parasitic interactions associated with the differential inductors and the coplanar slotline (CPS) interconnect between stages. A close-up picture of a single 45° analog phase shift cell

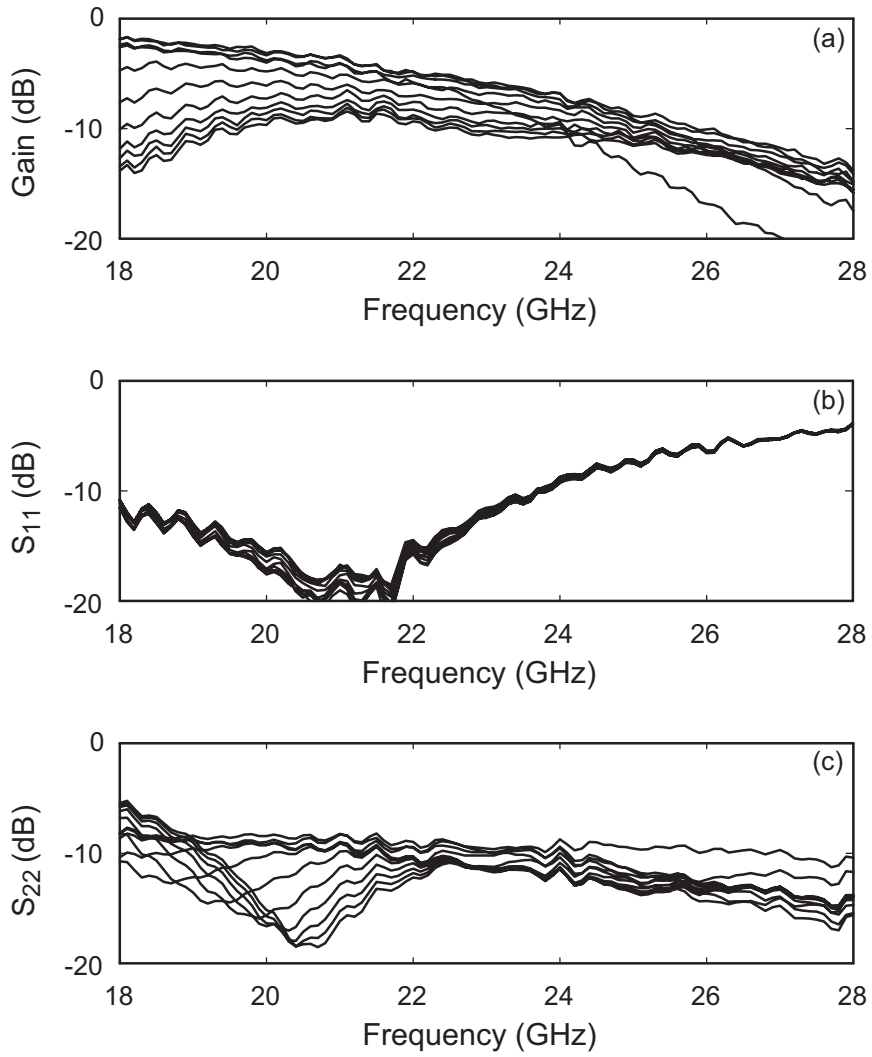



Figure B.4: Measured performance (a) gain, (b) $S_{11}$ and (c) $S_{22}$ of the differential 24 GHz phase shifter for analog control voltages 1-5 V in 0.5 V steps.

($310 \times 140\,\mu\text{m}^2$) clearly shows the differential inductor and the varactors (Fig. B.3b). The differential S-parameters were measured on-chip with G-S-S-G probes in conjunction with two 0/180° hybrids used as baluns to convert the 100 Ω differential ports to single-ended 50 Ω ports similar to the test setup used in Chapter 3 (Fig. 3.11). The network analyzer was calibrated to the probe tips using an LRRM calibration scheme and a calibration substrate from Cascade Microtech.

The gain, and return loss of the 24 GHz phase shifter is not as expected with a total of three issues contributing to problem (Fig. B.4). The first problem is the that the 180°-bit does not toggle the phase state. Upon careful investigation of the layout it was discovered

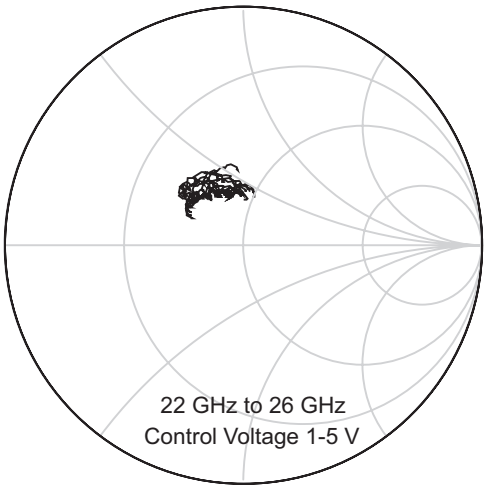



Figure B.5: Measured output return loss of the differential 24 GHz phase shifter from 22-26 GHz for analog control voltages 1-5 V in 0.5 V steps. The tight cluster demonstrates that the constant impedance topology is partially working.

that there is a layout error in the core of the Gilbert cell such that the quad of transistors are directly coupled rather than cross-coupled. This results in no wire inversion when the state of the Gilbert cell is toggled, however the Gilbert cell should continue to perform correctly as a cascode amplifier. This is a direct result of an LVS[1] error. Due to poor communication LVS was not run on this circuit before being placed on the mask.

The second problem is a design error in the biasing of the LNA. The LNA is biased by a tail current source that is implemented with a simple current mirror. Nominally this is fine, but the reference resistor has a $\pm 15\%$ tolerance [77]. If the value of the reference resistor is low, then the tail current of the LNA increases. Due to the resistive load of the differential pair ($R_1$ in Fig. B.1) the input transistor pair saturates eliminating the gain in the LNA/180°-bit. Due to the DC coupling between the LNA and Gilbert cell, the bias point of the Gilbert cell also shifts, saturating the Gilbert cell tail current source. This increases the tail current and reduces the $V_{CE}$ of some of the core transistors, however, none of them saturate. This design error could have been prevented by running a Monte Carlo simulation on the DC operating point to highlight the process variation.

The measured bias current for the complete circuit is 39 mA rather than the designed value of 32 mA. When the sheet resistance of the current mirror reference resistor and the load resistors of the differential pair ($R_1$) are varied in simulation within the specified

[1]LVS, layout verses schematic checker to automatically verify that the schematic and layout are identical.

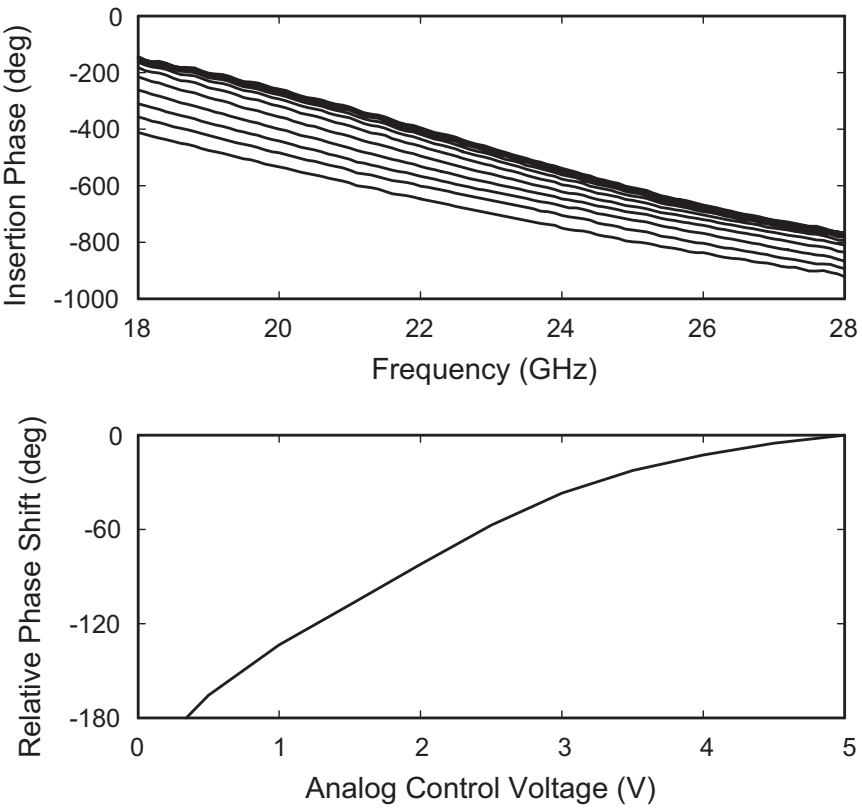



Figure B.6: Measured (a) insertion phase and (b) relative phase shift at 24 GHz for analog control voltages 1-5 V in 0.5 V steps.

tolerance, the bias current does increase to 39 mA and the gain of the complete circuit reduces to between $-5$ dB and $-10$ dB depending on the amount of saturation. Also the null in $S_{11}$ shifts down to 21 GHz due to the increased input capacitance of the saturated transistors. Both of these effects are seen in the measured S-parameters (Fig. B.4).

Despite the problems with the LNA/180°-bit, based on simulation, the 180° analog phase shifter should still work properly. The analog phase shifter provides slightly less phase shift over the 4 V tuning range than expected (Fig. B.6). The $S_{22}$ is relatively constant over frequency (22-26 GHz) and control voltage (1-5 V), however the port should be better matched at the design frequency verifying that the constant-impedance design is partially working (Fig. B.5). Also, there should be less variation in the gain. The simulated variation in the gain is $\pm 0.2$ dB at 24 GHz but the measured gain varies by $\pm 2.0$ dB at 24 GHz.

The degradation in the $S_{22}$ and the gain variation is most likely due to inaccuracies in the varactor model. The SiGe2-RF is a low-cost silicon process and most likely was

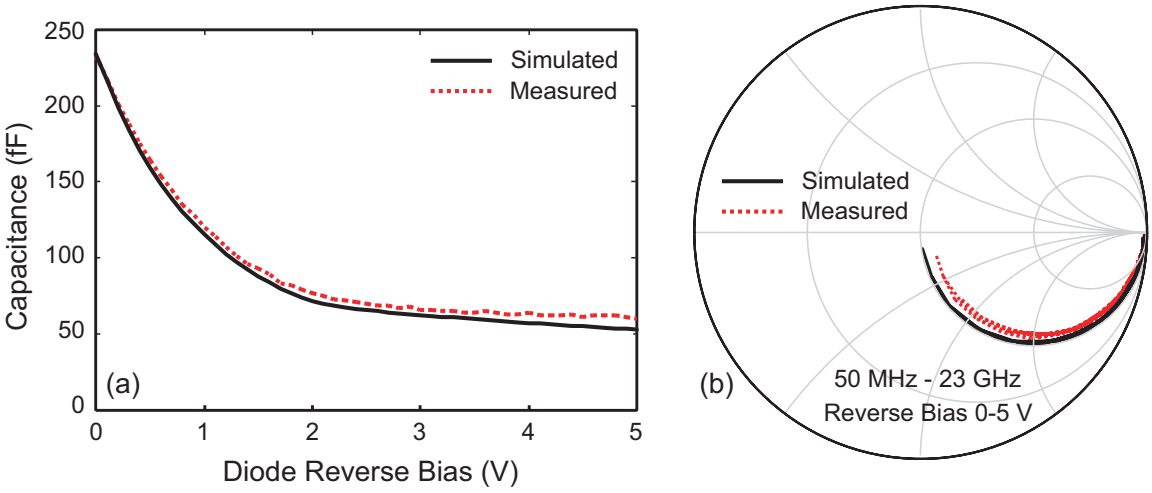



Figure B.7: Comparison between measured and simulated performance of varactor diode ($2 \times 5\,\mu\text{m} \times 21.2\,\mu\text{m}$), (a) C-V characteristic at 1 MHz and (b) $S_{11}$ in a series configuration.

not originally intended for use at 24 GHz. This can be seen by examining the process documentation from the foundry for the varactor model [78]. This documentation presents a comparison between measured data and the scalable model for different junction areas covering a 4:1 range. The smallest varactor measured is approximately the same size as the shunt varactor in the 24 GHz analog phase shifter, the results are repeated in Fig. B.7. The C-V characteristic at 1 MHz were measured and is in good agreement with the simulated performance. However, the $S_{11}$ of a series varactor was also measured from 50 MHz to 23 GHz and the measured data begins to clearly deviate from the model as the frequency increases. This indicates that there are parasitic effects that are not being taken into account by the foundry model of the varactor diode, most notably the quality factor.

## B.4 Conclusion

This appendix has outlined the design and measurement of a differential 24 GHz phase shifter with LNA. Following the LNA, a digital 180° phase shifter is implemented with Gilbert cell to provide gain and a precise phase shift in a small area. Following the LNA/180°-bit are four analog phase shifter cells, each provide a relative phase shift of 45° over a 4 V tuning range. Simulated gain of the circuit is 6.2 dB with a noise figure of

6.7 dB at 24 GHz. Measurement of the phase shifter revealed an LVS error in the Gilbert cell and a design error in the biasing of the LNA causing the LNA to saturate over process variation and severely reduce the gain. Despite this, the analog phase shifter still operates but with some degradation in its performance. This is attributed in the scalable varactor model that does not accurately represent the performance of the diode as the frequency of operation increases.

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