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High-Performance Digital X-Band and Ka-Band Distributed MEMS Phase Shifters

by

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A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
(Electrical Engineering)
in The University of Michigan
2002

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To my family, friends, and country.

ACKNOWLEDGEMENTS

I would like to thank everyone who allowed me to meet this important goal in my life. Above all, I would like to thank my advisor, Professor Gabriel Rebeiz, for discovering me as a first year graduate student, and providing the leadership and support I needed to complete this thesis. He has been a friend throughout and I think I will actually miss working by his side. I would also like to thank Research Scientist John Whitaker who gave me my first job at the University of Michigan in the Center for Ultrafast Optical Science, and also a good friend throughout. And to Professor Tony England and Associate Professor Kim Winick for their time and support by being on my committee.

Thank you to my family who was always there for me. My brother and I started and completed our graduate degrees together and it was just plain beautiful to have him around. My parents raised me with a love for discovery and creativity, leaving me with a feeling that with hard work, anything is possible. And to Charles Proteus Steinmetz, who would be glad to know after three generations of Joseph Steinmetz Hayden, there is finally one trained as an electrical engineer.

Thomas Edison once said he was friends with Steinmetz because "when they talked, they didn't talk about mathematics." Thank you to my best friends in Michigan and afar who interacted with me in the same way. There is a quote by Robert Louis Stevenson that a very close friend once said that has continued to resonate with me "... no man is useless while he has a friend." In those difficult and troubling times in my life, friends define us all and I have been truly been blessed with the best there is.

Thank you to my country which directly financed my undergraduate degree through the U.S. Army. The Army, along with my parents, not only supported me financially, but also taught me some of life's most important lessons. Thank you to the various government

contracts, most specifically those from DARPA and the Air Force Research Lab which supported me financially though graduate school.

Thank you to Raytheon Company and Chuck Goldsmith, which provided R&D funding and fabrication assistance which helped make the Ku-band microstrip phase shifters contained in this thesis possible.

Thank you to the students who served as my mentors: Sanjay Raman, Andy Brown, N. Scott Barker, and Leo DeDominico. And thank you to all my fellow graduate students who were always there to offer advice or just a good laugh: Jeremy Muldavin and his wife Katherine, Guan Leng Tan, Jad Rizk, Bernhard Schoenlinner, Lee Harle, Jim Becker, Dimitrios Peroulis, and Alex Margomenos.

Lastly, I would like to thank the entire clean room staff, especially Dennis Grimard, Keith Bowerman, Tim Brock, Phil Collica, and James Kulman for running what must be one of the best educational clean rooms today.

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CHAPTER 1

INTRODUCTION

1.1 The Field of MEMS

The field of MEMS (Micro-Electro-Mechanical-Systems) work has matured greatly since its introduction in the early 1980's. In 1982-1983 the first mass-produced MEMS devices, micromachined automotive MAP (Manifold Air Pressure) sensors and micromachined disposable blood pressure sensors, were sold on the commercial market. In 1982, only 5 Fortune 500 companies were in the field and in 1998 there were 25. Today, more and more companies are starting new MEMS research groups to design and manufacture accelerometers, gyroscopes, sensors, micro-valves, micro-motors, projection micro-mirrors, and possibly the greatest growing field, micromachined biosensors.

In a general sense, the terms MEMS and micromachining can be taken to mean the process of greatly reducing the scale of everyday devices, but in a true sense, MEMS devices are much more than that. MEMS devices provide a link between the physical and electrical world in an extremely small package. The techniques to process these devices go far beyond the simple lithography of integrated circuits because the MEMS process engineer must have a strong grasp of mechanical (stress, strain, etc.), chemical (fluidics, reactions, etc.), and electrical (noise. capacitance, etc.) systems on the micro-scale so as to create a novel MEMS device.

Indeed, the field of MEMS work is extremely diverse and what is presented in this thesis is just one aspect of MEMS, mainly RF (radio frequency) MEMS. By the use of

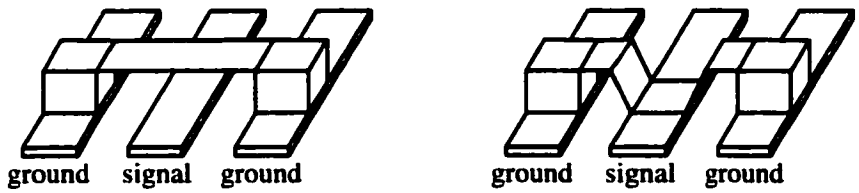


Figure 1.1: The RF MEMS switch implemented on a coplanar line in the up (a) and down (b) state positions.

one MEMS device, the MEMS RF switch, what is presented in this thesis is one of the lowest loss distributed phase shifters available to date at X-band (8-10 GHz) and Ka-band (26.5-40 GHz) frequencies.

1.2 The RF MEMS Switch

As the name may imply, a RF MEMS switch (Fig. 1.1) is simply a micro-scale switch. The MEMS switches presented in this work are, at their largest, only five human hair diameters long and two hair diameter wide ($300 \times 120\ \mu m^2$) and switches nearly one third this size were fabricated for millimeter-wave applications. And unlike its macro-scale equivalent in which the force required to turn it on or off is provided by an electromagnetic relay (or by the hand), MEMS switches require some other form of force such as electrostatic, magnetostatic, thermal, or piezoelectric force. Electrostatic force is widely accepted as one of the most simple and effective actuator systems for MEMS devices because when implemented, these systems are very small compared to other systems (such as thermal or magnetostatic) and use virtually no DC (direct current) power, which is important for applications such as airborne or satellite phased array antenna systems.

1.3 Phase Shifters

Phase shifters are used to delay the phase or timing of a sinusoidal RF wave (Fig. 1.2). Phase shifters have many applications in instrumentation systems and wireless communi-

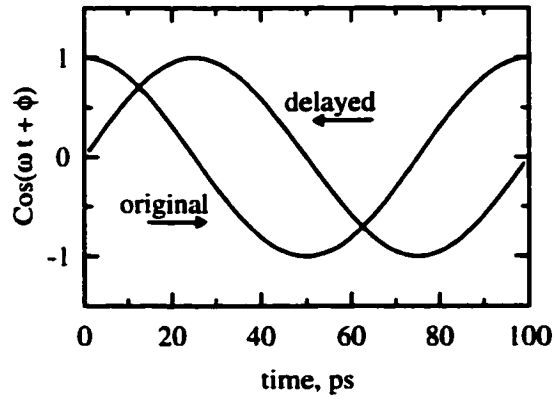


Figure 1.2: A 10 GHz wave and a 10 GHz wave delayed by 90°, or 25 ps.

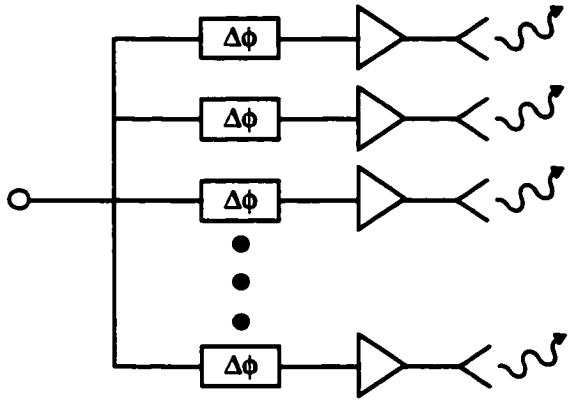


Figure 1.3: A standard phased array antenna system.

cation circuits [25] but are most significantly used in phased array antennas for telecommunications and radar applications. In this case, placing a phase shifter on each radiating element allows the antenna beam to be electronically steered without physically moving the antenna elements (Fig. 1.3).

Traditionally, commercially available phase shifters are based on ferrite materials, p-i-n diodes, or FET switches [39]. FET-based phase shifters are similar to MEMS switch based phase shifters in that the FET devices consume very little power, but unlike a MEMS system, have a large amount of loss, around 4-6 dB at 12-18 GHz [52],[10] and 8-9 dB at 35 GHz for 4-bit designs [44],[29]. Phase shifters based on p-i-n diodes consume more power (3-10 mW per diode) and have slightly better performance than FET based phase shifters but do not come close to the loss characteristics of a MEMS switch based system.

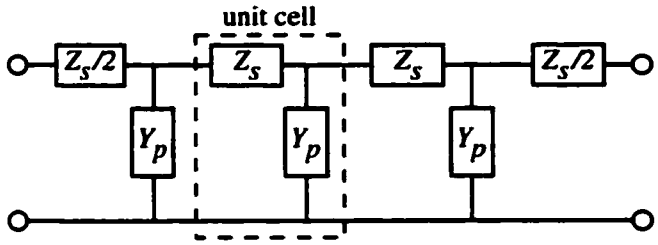


Figure 1.4: The unit cell of a distributed circuit.

Standard phase shifter designs, regardless if implemented with p-i-n diodes, FET switches, or MEMS switches, are based on three main techniques: 1) switched delay-line, 2) reflect-line, and 3) distributed loaded-line. The MEMS phase shifters presented in this thesis are based on the distributed technique which has been shown to result in excellent operation up to 20 GHz when based on Schottky-diode varactors (−4.2 dB of loss for an analog 360° phase shifter at 20 GHz) [33],[34], and up to 110 GHz when based on analog MEMS varactors (−2.5 dB of loss for an analog 180° phase shifter at 94 GHz) [3],[7],[5].

1.4 Distributed Circuits

Distributed techniques have been used as a solution to obtaining very wideband circuits. The idea is based on periodically loading a t-line (transmission line) with transistors, Schottky-diodes, or passive components such as capacitors or stubs, to obtain wideband amplifiers [8],[2],[48],[24], oscillators [48],[11],[54],[14],[55], mixers [50],[47],[46], multipliers, and pulse-shaping circuits. The concept is very useful because the parasitics of the discrete device, such as the gate-to-source capacitance of transistors in traveling-wave amplifiers, or the capacitance of the Schottky-diode in non-linear pulse shaping circuits, are included as part of the distributed model of the transmission line, thereby resulting in wideband operation. Furthermore, distributed circuits often result in a precise analytical model which greatly simplifies the design process. The distributed circuit model consists of a unit cell which is cascaded multiple times in a t-line circuit (Figure 1.4). In the case of a distributed phase shifter, each unit cell is capable of a certain amount of phase shift and by adding more cells, the total phase shift increases by a factor of the number of cells.

1.5 Contents of Thesis

The work in this thesis demonstrates that distributed phase shifters based on MEMS switches have vastly superior low-loss characteristics than the ones based on solid-state devices such as Schottky diodes, FETs, or p-i-n diodes. The reason is that MEMS switches have a very low series resistance, 0.1 to 0.3 Ω, as compared to solid state devices (2 to 6 Ω). MEMS devices also have lower power drive requirements (μW vs. mW in p-i-n devices). The first chapter contains the theory, design rules, and optimization of distributed circuits and distributed phase shifters. This chapter is followed by a discussion and measurements of loss in capacitors, which will be shown to be extremely important for low-loss distributed phase shifter design. Chapters 4, 5, and 6 contain the measurement and analysis of phase shifters at X-band, Ku-band, and Ka-band frequencies, respectively. The X-band CPW design has shown excellent performance, comparable to other non-distributed MEMS phase shifters. The Ku-band microstrip phase shifter is the first of its kind, that is, a novel topology which includes MEMS switches and electrically short microstrip radial stubs. The Ka-band distributed phase shifters are contained in Chapter 6 and are the lowest loss measured phase shifters to date for all types (switched line, reflect, etc.) of phase shifters. This chapter concludes with Chapter 7, where a W-band design and some final conclusions are presented.

CHAPTER 2

DESIGN, LAYOUT, AND OPTIMIZATION OF LOW-LOSS DMTL PHASE SHIFTERS

2.1 Introduction

The DMTL (Distributed MEMS Transmission Line) phase shifter consists of a CPW or microstrip line and a periodic set of electrostatic force actuated MEMS switches. By using a single control voltage to vary the height of the MEMS switches, the distributed capacitance loading on the transmission line, and therefore its propagation characteristics, can be varied. This results in a voltage controlled transmission line with variable phase velocity and therefore a true time delay (TTD) phase shifter.

2.2 Modeling the Wave Equation

First consider that all the characteristics of a distributed transmission line, and in a more general sense, a transmission line, stem from Maxwell's equations. These equations, as will be shown, predict lumped model approximations of phase velocity and impedance of the distributed line and these lumped equations, in turn, will be used to develop closed-form expressions for the design of distributed phase shifters.

Take Maxwell's first two equations in time domain form for a source-free medium:

$$\begin{aligned} \nabla \times \overline{E} &= -j\omega\mu\overline{H} \\ \nabla \times \overline{H} &= j\omega\epsilon\overline{E} + \sigma\overline{E} \end{aligned} \tag{2.1}$$

By taking the curl of the first equation, substituting the second for $\nabla \times \overline{H}$, and using the vector identity $\nabla \times \nabla \times \overline{A} = \nabla(\nabla \cdot \overline{A}) - \nabla^2 \overline{A}$, the following is obtained:

$$\begin{aligned} \nabla \times (\nabla \times \overline{E}) &= -j\omega\mu(\nabla \times \overline{H}) = -j\omega\mu(j\omega\epsilon\overline{E} + \sigma\overline{E}) \\ &= (\omega^2\mu\epsilon - j\omega\sigma\mu)\overline{E} \\ \nabla(\nabla \cdot \overline{E}) - \nabla^2\overline{E} &= (\omega^2\mu\epsilon - j\omega\sigma\mu)\overline{E} \end{aligned} \tag{2.2}$$

where $\nabla \cdot \overline{E} = 0$ in a source-free region leading to:

$$\begin{aligned} \nabla^2\overline{E} + (\omega^2\mu\epsilon - j\omega\sigma\mu)\overline{E} &= 0 \\ \nabla^2\overline{E} + \omega^2\mu\epsilon\left(1 - j\frac{\sigma}{\omega\epsilon}\right)\overline{E} &= 0 \end{aligned} \tag{2.3}$$

Equation (2.3) is in the form of Helmholtz's equation:

$$\nabla^2\overline{E} + k_o^2\overline{E} = 0 \tag{2.4}$$

where k_o is the wavenumber of the propagating wave and jk_o is the complex propagation constant:

$$jk_o = \gamma = \alpha + j\beta = j\sqrt{\omega^2\mu\epsilon\left(1 - j\frac{\sigma}{\omega\epsilon}\right)} = j\omega\sqrt{\mu\epsilon}\sqrt{1 - j\frac{\sigma}{\omega\epsilon}} \tag{2.5}$$

Equation (2.5) describes the propagation of the wave where the propagation velocity, v_p, is ω/β and the rate of decay of the wave with distance due to loss is equal to α. Consider, for example, a wave traveling in free space ($\epsilon_r = \mu_r = 1$ where $\epsilon = \epsilon_r\epsilon_o$ and $\mu = \mu_r\mu_o$) travels at the speed of light assuming propagation is lossless ($\sigma = 0$).

$$\alpha + j\beta = j\omega\sqrt{\mu_o\epsilon_o} \tag{2.6}$$

$$v_p = \frac{\omega}{\beta} = \frac{1}{\sqrt{\mu_o\epsilon_o}} = \mathrm{c} \quad \mathrm{m/s} \tag{2.7}$$

The wave impedance is defined as the relation between electric and magnetic fields. To obtain the wave impedance, assume an electric field has only an $\hat{x}$ component, then the Helmholtz (2.4) equation can be written as:

$$E_x(z) = E^+e^{-\gamma z} + E^-e^{+\gamma z} \tag{2.8}$$

and using Maxwell's first equation (2.1):

$$H_y(z) = \frac{-j\gamma}{\omega\mu}\left(E^+e^{-\gamma z} + E^-e^{+\gamma z}\right) \tag{2.9}$$

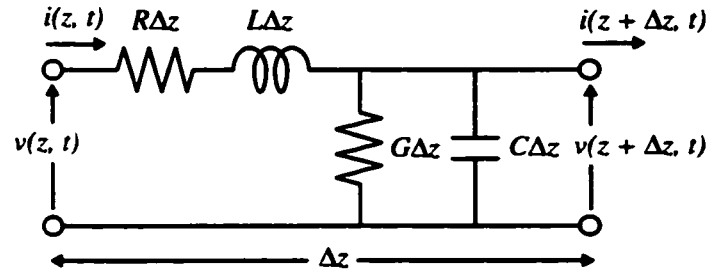


Figure 2.1: Lumped element equivalent circuit of a transmission line.

The wave impedance, η, is therefore defined as:

$$\begin{aligned}\eta &= \frac{E_x(z)}{H_y(z)} = \frac{j\omega\mu}{\gamma} = \frac{j\omega\mu}{j\omega\sqrt{\mu\epsilon}}\left(\sqrt{1-j\frac{\sigma}{\omega\epsilon}}\right)^{-1} \\ &= \sqrt{\frac{\mu}{\epsilon}}\left(\sqrt{1-j\frac{\sigma}{\omega\epsilon}}\right)^{-1}\end{aligned} \tag{2.10}$$

The free space impedance is a well known quantity and it can be obtained from (2.10) assuming propagation is lossless:

$$\eta = \frac{\sqrt{\mu_o}}{\sqrt{\epsilon_o}} = 377\ \Omega \tag{2.11}$$

2.3 Transmission Line Lumped Model

The lumped element equivalent to the derivation obtained from Maxwell's equations in the previous section will be obtained next. A short section (Δz) of two conductor transmission line is often represented as a lumped circuit [38] as shown in Figure 2.1 where R, L, G, and C are the per unit length resistance (due to transmission line conductivity), inductance (self inductance of the two conductors), conductance (due to dielectric loss of the substrate on which the transmission line is patterned), and capacitance (due to the proximity of the two conductors), respectively. In a distributed sense, a long length of transmission line can be simply thought of as a cascade of the unit cell shown in Figure 2.1, and the accuracy of representing a transmission line with this lumped distributed model will increase as Δz approaches zero. Obtaining this unit cell will lead to a determination of the closed form expressions used for design of the distributed phase shifter.

To obtain closed-form expressions for the impedance and propagation velocity of the

transmission line in terms of the lumped components, apply Kirchhoff's voltage and current laws to the lumped model:

$$\begin{aligned} v(z,t) - R\Delta z\, i(z,t) - L\Delta z\frac{\partial i(z,t)}{\partial t} - v(z+\Delta z,t) = 0 \\ i(z,t) - G\Delta z\, v(z+\Delta z,t) - C\Delta z\frac{\partial v(z+\Delta z,t)}{\partial t} - i(z+\Delta z,t) = 0 \end{aligned} \tag{2.12}$$

Dividing each equation by Δz and taking the limit $\Delta z \to 0$ to (2.12) yields the following:

$$\begin{aligned} \frac{v(z,t) - v(z+\Delta z,t)}{\Delta z} &= R\, i(z,t) + L\frac{\partial i(z,t)}{\partial t} \\ \frac{\partial v(z,t)}{\partial z} &= R\, i(z,t) + L\frac{\partial i(z,t)}{\partial t} \end{aligned} \tag{2.13}$$

$$\begin{aligned} \frac{i(z,t) - i(z+\Delta z,t)}{\Delta z} &= G\, v(z+\Delta z,t) + C\frac{\partial v(z+\Delta z,t)}{\partial t} \\ \frac{\partial i(z,t)}{\partial z} &= G\, v(z,t) + C\frac{\partial v(z,t)}{\partial t} \end{aligned} \tag{2.14}$$

And assuming a sinusoidal system,

$$\begin{aligned} \frac{dV(z)}{dz} &= (R + j\omega L)\, I(z) \\ \frac{dI(z)}{dz} &= (G + j\omega C)\, V(z) \end{aligned} \tag{2.15}$$

These equations (2.15) can be solved simultaneously to yield the following equations in the form of Helmholtz's (2.4) equation:

$$\begin{aligned} \frac{dV^2(z)}{dz^2} - [(G + j\omega C)(R + j\omega L)]\ V(z) = 0 \\ \frac{dI^2(z)}{dz^2} - [(G + j\omega C)(R + j\omega L)]\ I(z) = 0 \end{aligned} \tag{2.16}$$

Therefore the complex propagation constant, in terms of lumped element components is:

$$\gamma = \alpha + j\beta = \sqrt{(G + j\omega C)(R + j\omega L)} \tag{2.17}$$

where the propagation velocity of the wave, v_p, is ω/β and the rate of decay of the wave with distance due to loss is equal to α. By approximation, this equation can be put into a corollary form derived from Maxwell's equations (2.5) by taking $R = 0$. This is not a bad assumption since R represents transmission line conductivity, and the transmission lines used for the majority of work in this thesis have very low loss.

$$\begin{aligned} \gamma = \sqrt{(G + j\omega C)(j\omega L)} &= \sqrt{j\omega LG + j^2\omega^2 LC} \\ &= j\omega\sqrt{LC}\sqrt{1 - j\frac{G}{\omega C}} \end{aligned} \tag{2.18}$$

To obtain the impedance of the transmission line in terms of the lumped components, start with the traveling forward and reverse wave solutions on a transmission line using the propagation constant of (2.17):

$$\begin{aligned} V(z) &= V_o^+ e^{-\gamma z} + V_o^- e^{+\gamma z} \\ I(z) &= I_o^+ e^{-\gamma z} + I_o^- e^{+\gamma z} \end{aligned} \tag{2.19}$$

Applying (2.19) to (2.15) gives the current on the line in terms of V_o:

$$I(z) = \frac{\gamma}{R + j\omega L}\left(V_o^+ e^{-\gamma z} + V_o^- e^{+\gamma z}\right) \tag{2.20}$$

and the characteristic impedance of the line, Z_o, is defined as:

$$Z_o = \frac{V(z)}{I(z)} = \frac{R + j\omega L}{\gamma} = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{2.21}$$

As before, by assuming $R = 0$, this equation represents the corollary form of the equation derived by Maxwell's equations (2.10):

$$Z_o = \sqrt{\frac{L}{C}}\left(\sqrt{1 - j\frac{G}{\omega C}}\right)^{-1} \tag{2.22}$$

2.4 Theory of Transmission Line Loading

For a typical microwave transmission line, the series resistance term, R, has little effect on the characteristic impedance (2.21) and propagation velocity derived from (2.17) as long as the conductance term, G, which dominates the equations, is minimal. The majority of transmission lines built for the work in this thesis are made on a quartz substrate which is an extremely good insulator, meaning that the G term may be considered equal to zero. A typical 50 Ω coplanar transmission line on a quartz substrate at 30 GHz has a loss of 50 dB/m or an equivalent series resistance term of $R = 575$ Ω/m.

Including this term in the impedance (2.21) equation and the equation used to derive the propagation velocity (2.17) reveal that they are increased by only 0.02%. Therefore, by assuming $R = G = 0$, the following equations can be used to approximate transmission line characteristics with great accuracy.

$$Z_o = \sqrt{\frac{L}{C}} \tag{2.23}$$

$$v_p = \frac{1}{\sqrt{L\,C}} \tag{2.24}$$

These two equations serve as the basis for all closed-form expressions of the distributed MEMS transmission line and it will be shown that, by increasing the per unit length capacitance, while keeping the per unit length inductance constant, the propagation velocity, v_p, and characteristic impedance will decrease, thus slowing down the wave, and providing the true time delay (TTD) required for a phase shifter. Changing this capacitance will be done by loading the transmission line at a periodic separation, s, with a varactor, as shown in Figure 2.2. The unit cell contained in this figure shows the transmission line split into 4 parts and the varactor is represented by C_b. For accurate model representation over all frequencies of interest, the transmission line should be split into more parts than 4 because as discussed previously, the lumped model of a transmission line is accurate as $\Delta z \rightarrow 0$, so in order to accurately represent the effect of loading, the transmission line must be split into several small parts. But, as it turns out, s will be less than 5% of the design frequency wavelength for frequencies at and below the design frequency, and the unit cell for the DMTL can be accurately represented by a single inductor and two capacitors as shown in Figure 2.3. Using (2.23) and (2.24), the impedance and propagation velocity of this loaded unit cell is:

$$Z_o = \sqrt{\frac{sL_t}{sC_t + C_b}} \tag{2.25}$$

$$v_p = \frac{s}{\sqrt{sL_t\,(sC_t + C_b)}} \tag{2.26}$$

2.5 Bragg Frequency

As discussed, Equations (2.25) and (2.26) only hold true when the length of the unit cell, s, is a small fraction of a wavelength. At higher frequencies (frequencies above the design frequency) this model is inaccurate and a new method to determine the characteristic impedance and propagation velocity must be used. The general model for a distributed transmission line is shown in Figure 2.4. Taking the complex propagation constant $\gamma = \alpha + j\beta$ as in (2.5) then the forward and reverse traveling waves are represented by:

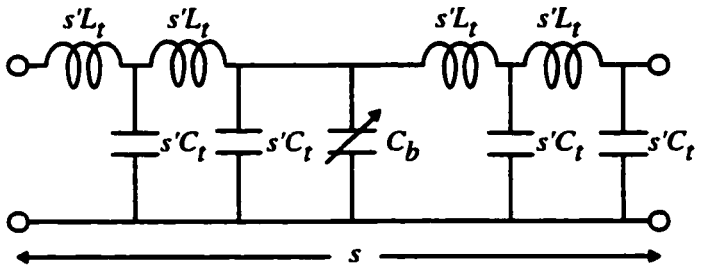


Figure 2.2: The unit cell lumped model of a distributed phase shifter. The transmission line is represented in parts by $s'L_t$ and $s'C_t$, where $s' \ll s$. The varactor is represented by C_b.

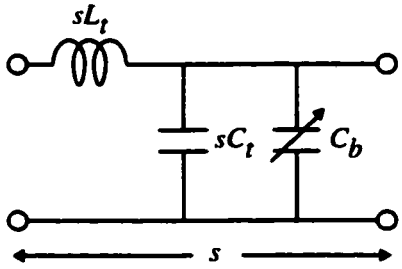


Figure 2.3: The simplified unit cell lumped model of a distributed phase shifter for frequencies at and below the design frequency.

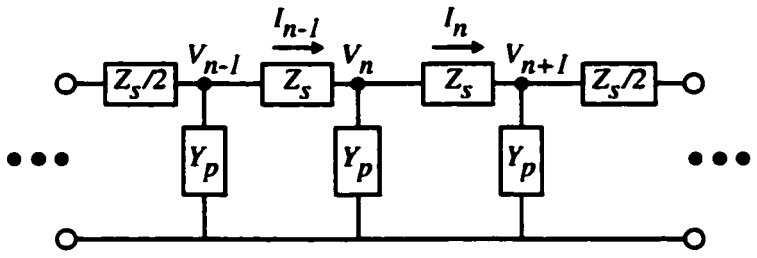


Figure 2.4: The general model for a distributed transmission line.

$$V_{n+1} = V_n e^{-\gamma}$$
$$V_{n-1} = V_n e^{+\gamma} \tag{2.27}$$

The voltages and currents on the line are:

$$V_n = \frac{I_{n-1} - I_n}{Y_p}$$
$$I_{n-1} = \frac{V_{n-1} - V_n}{Z_s} \tag{2.28}$$
$$I_n = \frac{V_n - V_{n+1}}{Z_s}$$

and using (2.27) along with the hyperbolic cosine identity yields the following

$$1 + \frac{Z_s Y_p}{2} = \frac{V_{n-1} + V_{n+1}}{2V_n} = \frac{e^{+\gamma} + e^{-\gamma}}{2} = \cosh\gamma \tag{2.29}$$

The DMTL is a symmetric line and it is important to define the impedance at the middle. Using $Z = V_{in}/I_{in}$ and the voltage at the middle of the line, $V_{n+1/2} = V_n - I_n Z_s/2$ then

$$Z = \frac{V_{n+1/2}}{I_n} = \left(\frac{V_{n-1} - 2V_n + Vn + 1}{V_n - V_{n+1}}\right)\frac{1}{Y_p} - \frac{Z_s}{2} = \frac{Z_s e^{+\gamma/2}}{2\sinh(\gamma/2)} - \frac{Z_s}{2} \tag{2.30}$$

Using the half angle formula for the hyperbolic sine (2.30) the characteristic impedance of the distributed line is

$$Z_s = \sqrt{\frac{Z_s}{Y_p}}\sqrt{1 + \frac{Z_s Y_p}{4}} \tag{2.31}$$

The per unit length inductance and capacitance of a transmission line are determined from (2.5) (2.24) and (2.23) and are determined to be:

$$L_t = \frac{\sqrt{\epsilon_{eff}}\, Z_o}{\mathrm{c}}$$
$$C_t = \frac{\sqrt{\epsilon_{eff}}}{Z_o\, \mathrm{c}} \tag{2.32}$$

where Z_o is the characteristic impedance of the line before loading and $\mathrm{c}/\sqrt{\epsilon_{eff}}$ is the guided velocity of the transmission line. Using the models of Figure 2.3 and 2.4 along with equation (2.31) gives the characteristic impedance, Z_L, of the loaded unit cell of length s. Since $Z_s = j\omega s L_t$ and $Y_p = j\omega\,(sC_t + C_b)$, the loaded impedance is:

$$Z_L = \sqrt{\frac{sL_t}{(sC_t + C_b)}}\sqrt{1 - \frac{\omega^2 s L_t\,(sC_t + C_b)}{4}} \tag{2.33}$$

It is apparent from the second term of the equation (2.33) that as the frequency increases, provided L_t, C_t, C_b, and s are constant, then there is a frequency point at which the periodic filter structure of the distributed loaded line causes the line impedance to become zero and thus there will be no power transfer from one port to the other. The frequency at which this occurs is called the Bragg frequency, f_B as will be shown later. The Bragg frequency is a very important design parameter and is calculated using Equation (2.33):

$$\begin{aligned} \omega_B^2 s L_t \left(sC_t + C_b\right) &= 4 \\ \omega_B = 2\pi f_B &= \frac{2}{\sqrt{sL_t\left(sC_t + C_b\right)}} \end{aligned} \tag{2.34}$$

2.6 Loading Impedances

As previously shown, the DMTL phase shifter consists of a transmission line loaded with the periodic placement of varactors to slow propagation velocity (2.26). The impedance of this distributed structure (2.25) also decreases, and therefore the next natural question to answer is: what are the optimal DMTL impedances?

Consider the DMTL is placed within a 50 Ω system as shown in Figure 2.5. The impedance seen at the input of the DMTL will depend on the distance between generator and load at the frequency of interest:

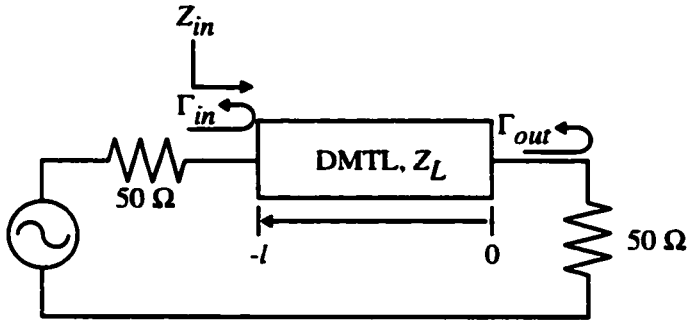


Figure 2.5: A DMTL transmission line of arbitrary length placed in a 50 Ω system.

$$Z_{in} = Z_L \frac{1 + \Gamma_{out} e^{-2j\beta l}}{1 - \Gamma_{out} e^{-2j\beta l}} \tag{2.35}$$

This equation (2.35) may be put into a more useful form by using trig identities and by recognizing that $\Gamma_{out} = (50 - Z_L) / (50 + Z_L)$.

$$Z_{in} = Z_L \frac{50 + jZ_L \tan(\beta l)}{Z_L + j50 \tan(\beta l)} \tag{2.36}$$

It is easily seen from (2.36) that if βl is $\pi/4$ then $Z_{in} = 50\ \Omega$, meaning that the impedance seen at the input of the DMTL in this system will pass through 50 ohms at frequencies where the transmission line is an odd multiple of a quarter wavelength. If however, both sides of (2.36) are divided by $\tan(\beta l)$ and the limit $\beta l \rightarrow \pi/2$ is taken, then the quarter wavelength transformer condition exists and:

$$Z_{in} = \frac{Z_L^2}{50} \tag{2.37}$$

The resulting reflection coefficient seen at the input of the DMTL is shown by (2.38) and to maximize power transfer through the DMTL, the reflected power loss due to the impedance mismatch between ports and the DMTL must be minimized. If the maximum reflection loss at the input of the DMTL is taken to be RL_{max} in dB, then the maximum input reflection coefficient is shown by (2.39).

$$\Gamma_{in} = \frac{Z_{in} - 50}{Z_{in} + 50} \tag{2.38}$$

$$\Gamma_{in} = 10^{RL_{max}/20} \tag{2.39}$$

Substituting (2.38) into (2.37) gives the desired DMTL loaded impedances in terms of the maximum desired reflection coefficient (2.39):

$$Z_L = 50\sqrt{\frac{1 \pm \Gamma_{in}}{1 \mp \Gamma_{in}}} \tag{2.40}$$

The solutions to this equation for $RL_{max} = -20$ dB, -15 dB, and -10 dB are given in Table 2.1. These are the optimal load impedances at the design frequency to maximize phase shift while keeping the reflected power loss at the input of the DMTL to a design specified minimum. These loaded impedances are not labeled arbitrarily as Z_u and Z_d; they represent the maximum (Z_u) and minimum (Z_d) impedances of the DMTL in the up and down-states of the MEMS switch, respectively as will be explained later (see Section 2.7). For the condition when $\beta l = \pi/4$, the impedance of the DMTL will pass through 50 Ω.

RL_{max}, dB	Z_u, Ω	Z_d, Ω
-20	55.3	45.2
-15	59.8	41.8
-10	69.4	36.0

Table 2.1: Optimal loaded impedances for various maximum reflection losses at the input of the DMTL.

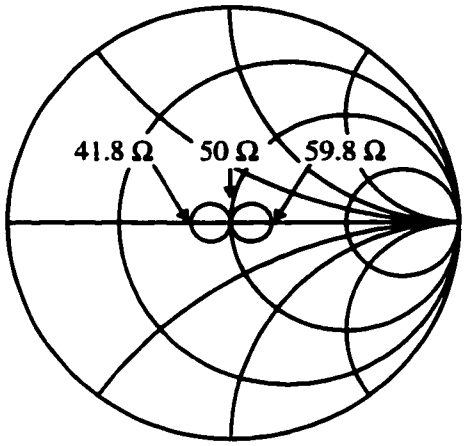


Figure 2.6: The two frequency-dependent solutions to (2.40) assuming $RL_{max} = -15$ dB.

This is demonstrated on the Smith chart of Figure 2.6 which shows the -15 dB reflection coefficient high and low impedances (Z_L) assuming no loss and half wavelength lines which are not loaded. At the frequency where the line is a quarter wavelength, $Z_u^{in} = 59.8\ \Omega$ and $Z_d^{in} = 41.8\ \Omega$ and at a half wavelength, the impedance returns to the center of the Smith chart (50 Ω).

Now that the optimum loaded impedances are known which maximize power transfer through the DMTL in a 50 Ω system, one must determine the impedance of the transmission line before it is loaded. This impedance will be referred to as the unloaded impedance and will be labeled as Z_o. This impedance obviously must be greater than or equal to the highest loaded impedance, Z_u, since the varactor can only serve to lower the impedance. It will be shown in Section 2.12 that the unloaded impedance, Z_o, is chosen to minimize the power loss per degree of phase shift as well as to meet some dimensional layout concerns of the

MEMS switch in the distributed line.

2.7 MEMS Switch Implementation

The MEMS switch may be implemented in distributed phase shifters in one of two ways. The first way uses a series DC-contact switch as shown in Figure 2.7. Here, the MEMS switch in the up-state position has very low series capacitance and therefore the series combination of this switch in the up-state with a fixed capacitance to ground will be dominated by the MEMS switch up-state capacitance. Because this capacitance and therefore loading on the line is minimal, the unloaded impedance, Z_o, will be very close to the highest loaded impedance, Z_u (59.8 Ω for $RL_{max} = -15$ dB). When the MEMS switch is in the down-state position, the capacitance of the MEMS switch (the down-state capacitance of a DC-contact series switch is infinite) becomes much greater than that of the fixed series capacitor to ground and the loading is dominated by the fixed capacitor. Thus, the value of the fixed capacitor is chosen such that when the MEMS switch is down, the loaded impedance will be at its lowest, Z_d (41.8 Ω for $RL_{max} = -15$ dB). This topology was not explored in this thesis for one major reason: although a very good design for low frequencies, it would not work well for high frequency designs because the MEMS series switch would be quite large in relation to the size of the unloaded line. Thus, the physical size of a MEMS switch would make this design approach simply unreasonable at W-band (75-110 GHz) or K/Ka-band (18-40 GHz) frequencies.

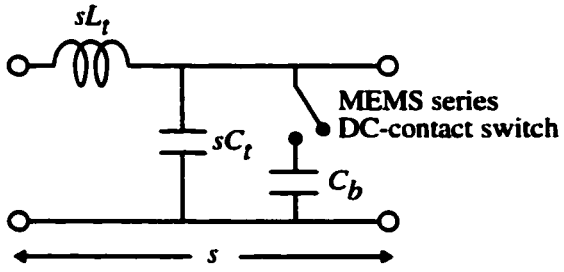


Figure 2.7: The DMTL phase shifter with the MEMS switch in a series topology.

The second way to implement a MEMS switch into the distributed transmission line is to use a MEMS switch which acts as a varactor (since it does not make DC-contact) as shown in Figure 2.8 for a coplanar line design and in Figure 2.9 for a microstrip line design. "Switch" is an accurate term because although it does not make DC-contact, its capacitance is so high that it is essentially a short at high frequencies. The MEMS switch is sometimes referred to as a MEMS bridge because it spans over the signal line. Capacitance loading to the unloaded line is a result of fields contained between the bottom of the MEMS switch and the signal conductor of the transmission line. When the height of this switch (or bridge) is lowered by an electrostatic force, the capacitance loading will increase and thus the impedance and propagation velocity of the DMTL will decrease. Thus, the MEMS switch will have a maximum height when no electrostatic force is applied and the corresponding impedance will be labeled Z_u (the up-state impedance). Likewise, the MEMS switch will have a minimum height when electrostatic force is applied and the corresponding impedance will be labeled Z_d (the down-state impedance). These MEMS switches have a width w, a thickness t, are suspended at a height h above the signal line, and are periodically spaced by a distance s. The number of switches vary depending upon the design and more switches will result in more phase shift.

2.8 Closed Form Design Equations

There is now sufficient information to develop closed form design equations for a DMTL phase shifter. The design proceeds as follows:

1. As shown in section 2.6, the loaded impedances of the DMTL with the MEMS switches in the up and down-state positions are selected to correspond to the maximum desired reflection loss. Referring to Table 2.1, if $RL_{max} = -15$ dB then these impedances are $Z_u = 59.8$ and $Z_d = 41.8\ \Omega$.

2. The impedance of the unloaded line is picked arbitrarily for now but will be optimized later for the lowest loss per degree of phase shift (see Section 2.12). A coplanar line on a quartz substrate ($\epsilon_r = 3.6$-3.8) with equal signal conductor width (W) and gap

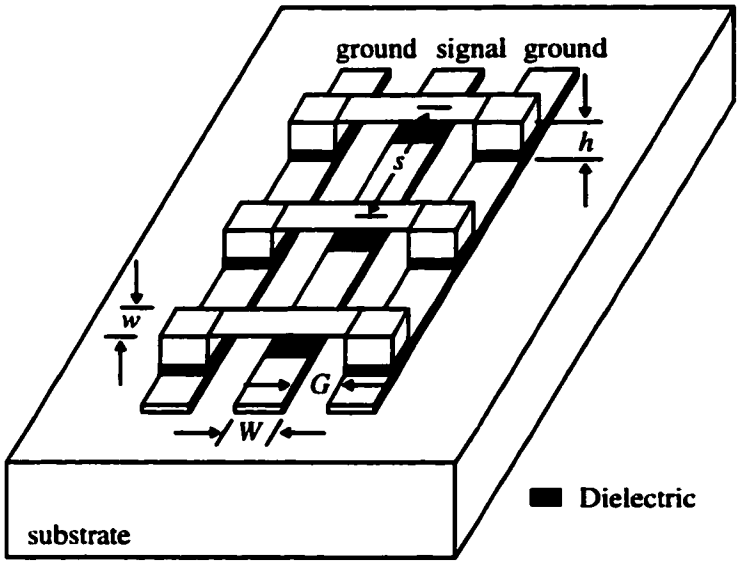


Figure 2.8: The DMTL phase shifter built on a coplanar line topology with MEMS varactors.

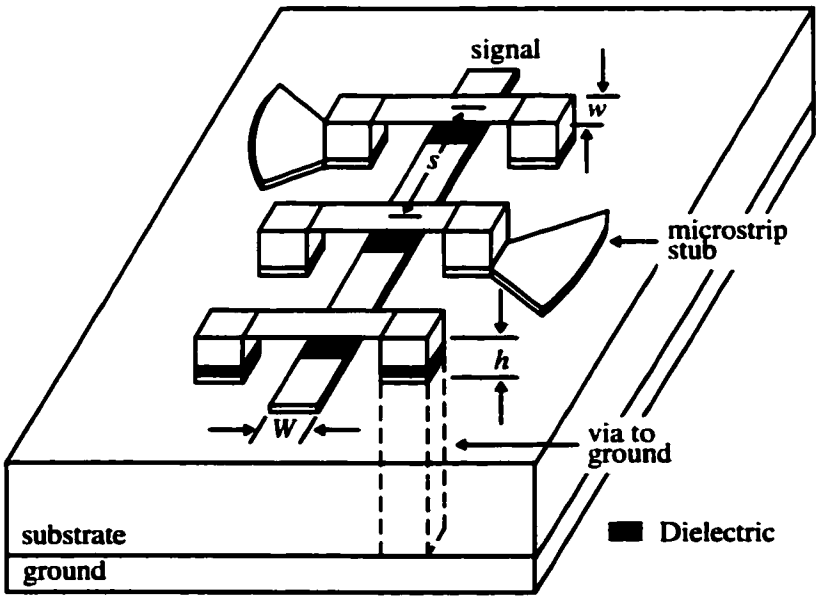


Figure 2.9: The DMTL phase shifter built on a microstrip line topology with MEMS varactors. The switches may either be coupled to ground through a via or through a microstrip stub.

(G) separation (see Figure 2.8) is a good first choice for dimensional layout concerns. It will also have a near optimal impedance (Z_o) of 98 Ω.

3. Design values for the MEMS switch capacitance (C_b) and the separation, s, between MEMS switches are dependent on simultaneous equations (2.34) and (2.25). The Bragg frequency, f_B, is selected by the designer. Solving these two equations for the separation, s, assuming the Bragg frequency is defined at the lowest impedance of interest (Z_d) results in:

$$s = \frac{Z_d \, \mathrm{c}}{\pi f_B Z_o \sqrt{\epsilon_{eff}}} \tag{2.41}$$

4. Substituting (2.41) into (2.25) gives the switch (bridge) capacitance values in the up (C_{bu}) and down (C_{bd}) states:

$$C_{bu} = \frac{(Z_o^2 - Z_u^2)\, Z_d}{Z_o^2 Z_u^2 \pi f_B} \tag{2.42}$$

$$C_{bd} = \frac{(Z_o^2 - Z_d^2)}{Z_o^2 Z_d \pi f_B} \tag{2.43}$$

and the capacitance ratio between the up and down states:

$$C_r = \frac{C_{bd}}{C_{bu}} = \frac{Z_u^2}{Z_d^2} \frac{(Z_o^2 - Z_d^2)}{(Z_o^2 - Z_u^2)} \tag{2.44}$$

5. The velocity of propagation on the DMTL with MEMS switches in the up or down states is derived from (2.26), (2.41), (2.42), and (2.43). Note that this solution is valid only at a frequency much less than the Bragg frequency because as the frequency approaches the Bragg frequency, the loaded impedance will approach zero and will not meet the original design goals for loaded impedances set forth in step 1.

$$v_L = \frac{\mathrm{c}\ Z_L}{Z_o \sqrt{\epsilon_{eff}}} \tag{2.45}$$

where Z_L is the loaded impedances for the DMTL with MEMS switches in the up or down states.

6. Using (2.45), the phase shift for frequencies much less than the Bragg frequency is obtained. It is seen that the addition of more sections will increase the total phase shift by a factor equal to the number of sections added.

$$\Delta\phi = \frac{360\ s f Z_o \sqrt{\epsilon_{eff}}}{\mathrm{c}} \left(\frac{1}{Z_u} - \frac{1}{Z_d} \right) \frac{\text{degrees}}{\text{section}} \tag{2.46}$$

2.8.1 Design Concepts

These equations serve as the basis for design of the DMTL phase shifter. Some important design concepts are determined from these equations:

1. As expected from (2.25), Equation (2.46) shows the phase shift per section increases as the loaded line impedances are symmetrically moved further away from the center impedance of 50 Ω. The loaded impedances are selected by the designer to meet a maximum reflection loss at the input of the DMTL. In fact, $RL_{max} = -10$ ($Z_u = 69.4$, $Z_d = 36.0$ Ω) dB will provide twice as much phase shift per section than $RL_{max} = -15$ dB ($Z_u = 59.8$, $Z_d = 41.8$ Ω), but at the expense of more reflected power loss at the input of the DMTL.

2. The unloaded impedance is selected to meet dimensional layout concerns and to minimize loss (see Section 2.12). The effective dielectric constant, $\sqrt{\epsilon_{eff}}$, is dependent on the type of substrate and transmission line used. Equations (2.46) and (2.41) show phase shift per section is independent of the dielectric constant because s is inversely proportional to $\sqrt{\epsilon_{eff}}$. However due to (2.41), higher dielectric constant materials such as silicon ($\epsilon_r = 11.8$, $\epsilon_{eff} \approx 6.4$) will produce a physically smaller phase shifter than one built on quartz ($\epsilon_r = 3.6$-3.8, $\epsilon_{eff} \approx 2.3$-$2.4$). The balancing factor is loss; losses in silicon are much higher than those in quartz and the loss per degree of phase shift becomes equivalent on quartz and silicon substrates (see Section 2.13.1).

3. Increasing the separation, s, between MEMS switches will increase the phase shift per section, however, this parameter (along with choices for Z_L) controls the Bragg frequency and therefore is not an independent variable. The Bragg frequency is a very important design parameter and increasing it will:

   - Decrease the spacing required (2.41) between the MEMS switches. The spacing becomes quite small at W-band (70-110 GHz) frequencies and a lower Bragg frequency can be used to design a DMTL phase shifter with a reasonable separation between switches.
   - Increase the range of linear phase shift (2.46) as shown in Figure 2.10a. Phase

shift quickly becomes non-linear because the optimal loaded impedances determined by Table 2.1 drop off quickly to zero near the Bragg frequency according to (2.33) and as shown in Figure 2.10b. To increase the range of linearity, the Bragg frequency must be increased.

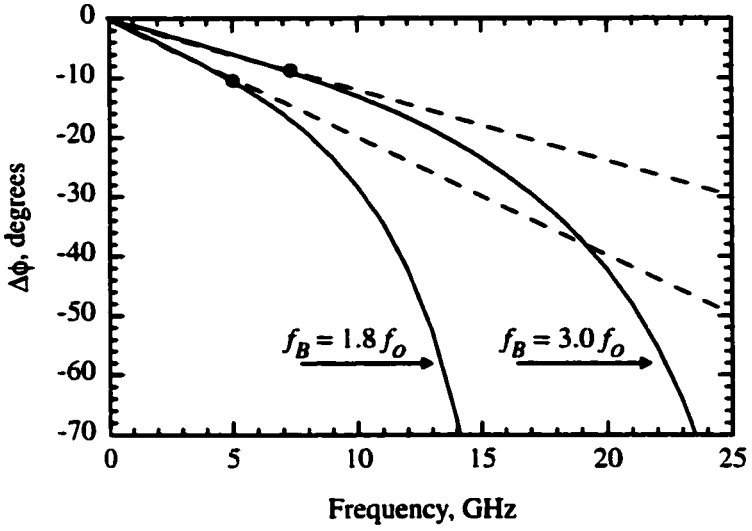
- Lower the required loading capacitors C_{bu} (2.42) and C_{bd} (2.43). For example, following the design parameters of Figure 2.10, the loading capacitors will be $C_{bu} = 79.4$ fF, $C_{bd} = 209.7$ fF if $f_B = 3f_o$, and $C_{bu} = 132.4$ fF, $C_{bd} = 349.4$ fF if $f_B = 1.8f_o$. Since the loading capacitance is quite small at W-band frequencies, a low Bragg frequency may be desirable; plus, separation between the MEMS sections will increase (first bullet) resulting in a design which is easier to fabricate at the expense of decreased bandwidth (second bullet).

4. Referring to Figure 2.11, the capacitance ratio between the MEMS switch in the down and up states will decrease along with an increase in the unloaded impedance regardless of the choice of RL_{max} and nears an asymptotic value at high impedances. Thus for stable designs, a higher unloaded impedance is desired. The maximum reflected power will have a large effect on the required capacitance ratio and thus again, for a rugged design, a RL_{max} on the order of -15 dB is preferable over -10 dB.

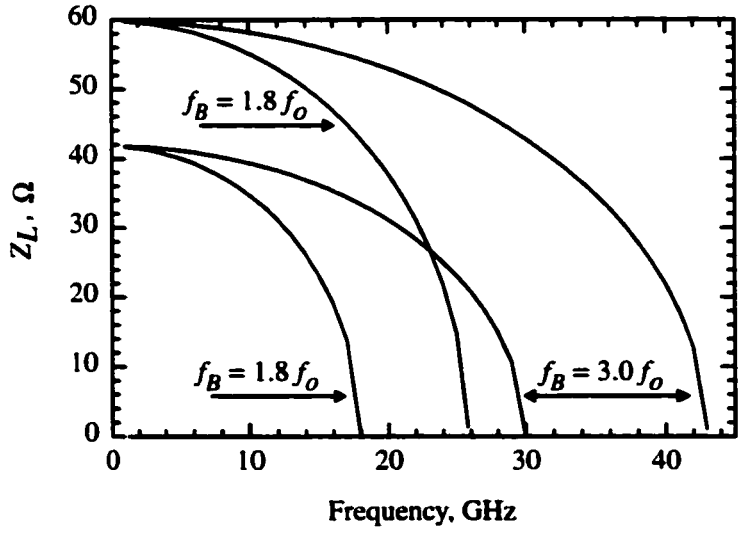
5. Figure 2.12 shows the corresponding MEMS switch capacitance values for the capacitance ratio values shown in Figure 2.11. All these values can be physically constructed but certainly values above 40 fF would be desirable. Depending on the range of switch membrane heights, widths, and signal line widths available, certain values for the unloaded impedance and RL_{max} may become limited.

2.9 Bridge Inductance and Resistance Effect on the Bragg Frequency

The lumped model of Figure 2.3 is a very rough approximation but this section will show why it does serve as a good model to derive closed-form design equations for the DMTL



(a)



(b)

Figure 2.10: The effect of Bragg frequency on the range of linear phase shift (a) and the loaded DMTL impedances (b). $Z_o = 100\ \Omega$, $f_o = 10$ GHz, $\epsilon_{eff} = 2.39$, and $RL_{max} = -15$ dB.

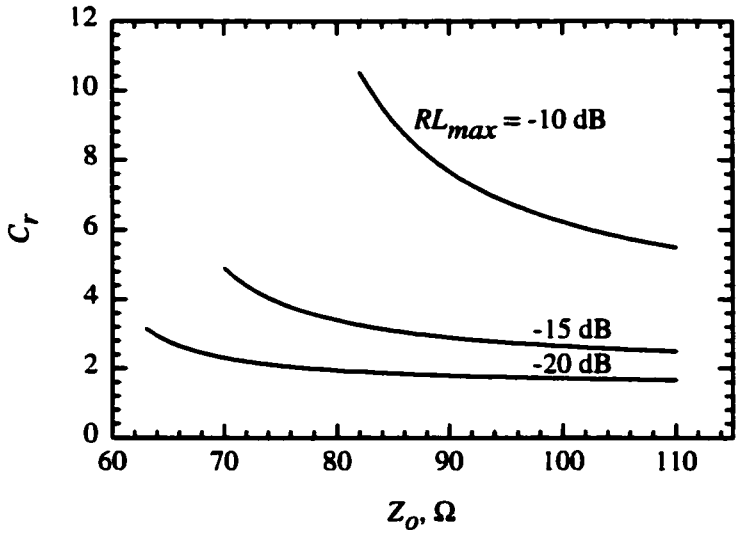


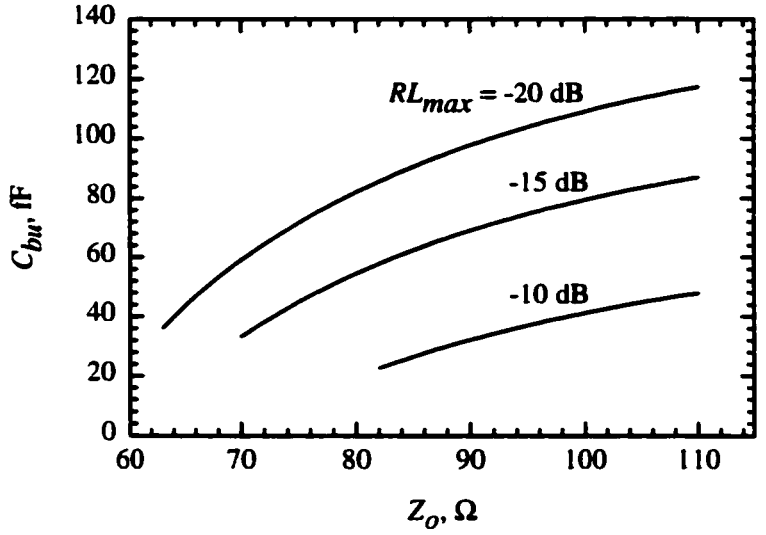
Figure 2.11: The effect of RL_{max} and unloaded impedance on the MEMS capacitance ratio. Stable designs have high unloaded impedance and RL_{max} near -15 dB. $f_b = 30$ GHz, $f_o = 10$ GHz, and $\epsilon_{eff} = 2.39$.

phase shifter. The true model of the MEMS switch consists, in addition to the capacitance of the MEMS switch, some inductance (L_b) and resistance (R_b) as shown in Figure 2.13.

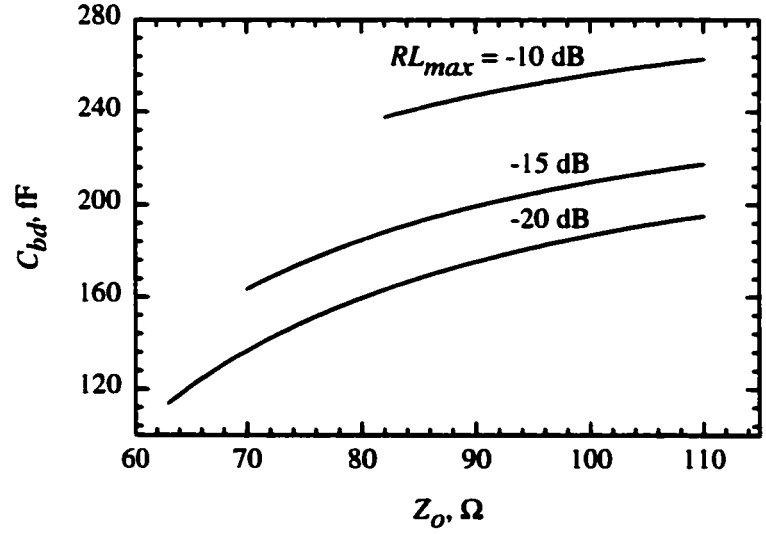
The inductance of a typical MEMS switch has been approximated to be 5-20 pH in typical circuits by fitting various measurements to modeled data [31]. In a similar way, the resistance is found to be 0.1-0.3 Ω. Using (2.31) and the technique used to obtain (2.33), the effect of the MEMS switch inductance and resistance on the loaded impedance and Bragg frequency can be found. The series resistance and shunt admittance is as follows:

$$\begin{aligned} Z_s &= j\omega s L_t \\ Y_s &= j\omega s C_t + \left(\frac{1}{j\omega C_b} + j\omega L_b + R_b\right)^{-1} \end{aligned} \tag{2.47}$$

By solving the full analytical function for Z_L and f_B (2.31), it is seen that a MEMS switch resistance of 0.1-0.3 Ω has little effect on both quantities. In fact, even resistances more than an order of magnitude higher, which would equate to a switch Q of 50, has little effect. By setting the second term of the impedance equation (2.31) equal to zero and by setting $R = 0$, the new Bragg frequency which accounts for switch inductance is found to



(a)



(b)

Figure 2.12: The effect of RL_{max} and unloaded impedance on required MEMS switch loading capacitances. f_b = 30 GHz, f_o = 10 GHz, and ϵ_{eff} = 2.39.

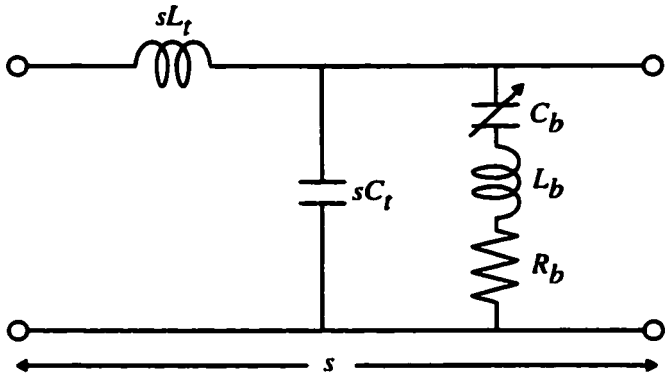


Figure 2.13: The unit cell lumped model of a distributed phase shifter for all frequencies.

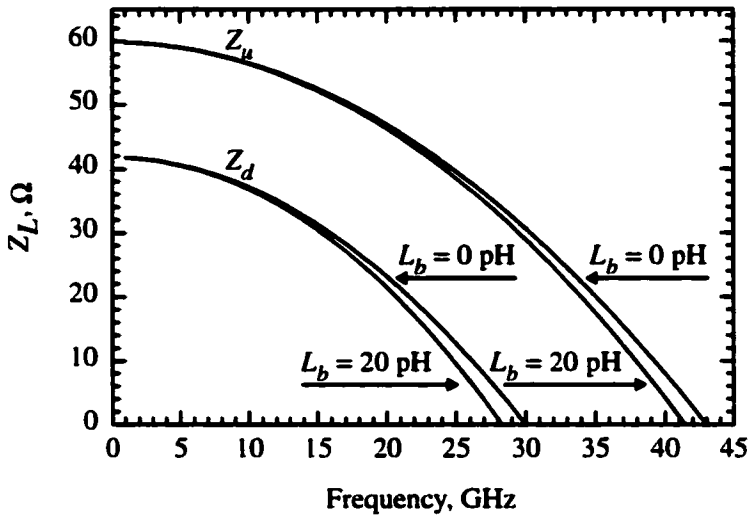
be:

$$\begin{aligned} \omega_B &= \sqrt{\frac{b - \sqrt{b^2 - 4ac}}{2a}} \\ a &= s^2 L_t C_t L_b C_b \\ b &= s^2 L_t C_t + s L_t C_b + 4 L_b C_b \\ c &= 4 \end{aligned} \tag{2.48}$$

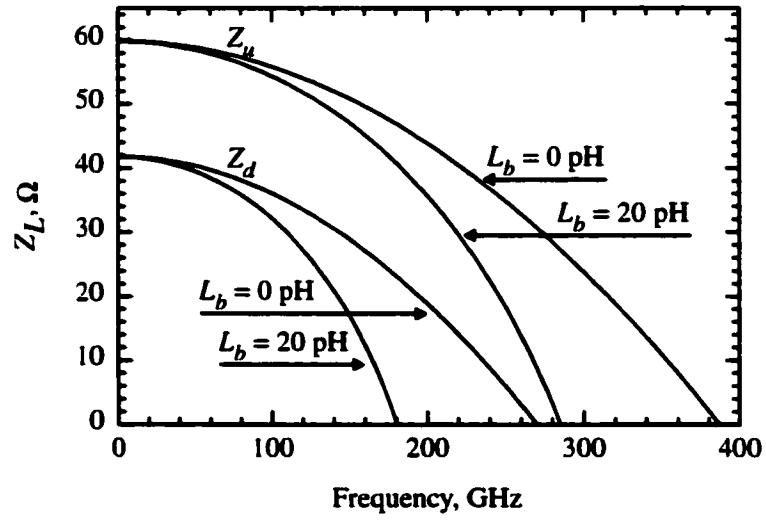
The switch inductance has a much smaller effect at low design frequencies (f_o = 10 GHz, as shown in Figure 2.14a) than high frequencies (f_o = 90 GHz, as shown in Figure 2.14b). Yet for either design frequency, the inductance has a very small effect on the loaded impedances in the 0-f_o range meaning that the closed form design equations derived in Section 2.8, which were developed by assuming that $L_b = 0$, still serve as a very good approximation for design.

2.10 Analog Versus Digital

The actuator system used to move the MEMS switches in this work is the electrostatic force. The electrostatic force between the MEMS switch and the signal conductor of the transmission line is the result of a simple voltage potential between them, as exists between the plates of a capacitor under voltage [26]. This force is found by evaluating the power



(a)



(b)

Figure 2.14: The effect of MEMS switch inductance on loaded impedances for the $f_o = 10$ GHz design (a) and $f_o = 90$ GHz design (b). $Z_o = 100\ \Omega$, $f_b = 3f_o$, $\epsilon_{eff} = 2.39$, and $RL_{max} = -15$ dB.

delivered to the time dependent capacitance of the MEMS switch [56].

The capacitance of the MEMS switch is

$$C = C_{pp} + C_f = \frac{\epsilon_o W w}{h} + C_f \tag{2.49}$$

where W is the width of the signal conductor, w is the width of the MEMS switch, and h is the suspended height as shown in Figures 2.8 and 2.9. The capacitance of the MEMS switch to the signal conductor also has a component, C_f, which accounts for the fringing field components. Typically, C_f ranges anywhere from 20% to 30% of C_{pp}, but for a particular set of parallel plate dimensions, C_f is constant.

The applied force to the MEMS switch is shown below and can be written in terms of the switch's physical dimensions using the capacitance equation above.

$$F = \frac{1}{2} V^2 \frac{dC(h)}{dh} = -\frac{1}{2} V^2 \frac{\epsilon_o W w}{h^2} \tag{2.50}$$

By setting this applied force equal to the mechanical restoring force of the switch at a height h, a closed form solution for the switch height versus the applied voltage up to an instability point can be found:

$$\frac{1}{2} \frac{\epsilon_o W w V^2}{h^2} = k\left(h_o - h\right) \tag{2.51}$$

$$V = \sqrt{\frac{2kh^2}{f_r \epsilon_o W w}\left(h_o - h\right)} \tag{2.52}$$

In the equation above, the original switch height is h_o and the spring constant [5] of the MEMS bridge (switch) is k. The general expression for the spring constant of a fixed-fixed beam is:

$$k = \frac{32 E w t^3}{L^3}\left(\frac{1}{2 - (2 - x)\, x^2}\right) + \frac{8\sigma\left(1 - \nu\right) w t}{L}\left(\frac{1}{2 - x}\right) \tag{2.53}$$

where $x = W/L$, E is the Young's modulus of the MEMS switch membrane, σ is the biaxial residual stress on the switch membrane, t is the thickness, ν is the Poisson's ratio, and L is the length of the switch. The solution to (2.52) is drawn in Figure 2.15 which demonstrates an instability at 2/3 h_o due to the positive feedback resulting from the constant voltage effect on charge in the moving switch membrane. This instability point may also be found by taking the derivative of (2.51) with respect to h. Because the switch membrane quickly

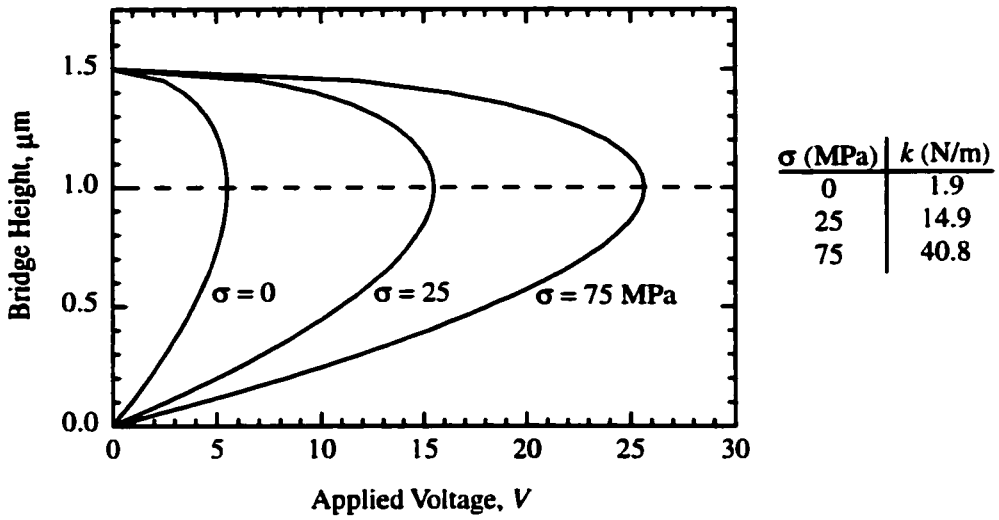


Figure 2.15: Switch height versus applied voltage with a zero voltage switch height of 1.5 μm. (L = 300 μm, W = 100 μm, w = 70 μm, E = 80 GPa, t = 8000 Å, ν = 0.42).

snaps to the signal conductor at this instability point, it is called the pull-in voltage, V_p. The data contained in Figure 2.15 below the instability point is of little practical value and may be confusing. This data represents the new pull down voltage if, after pulling the switch all the way to the signal conductor, a mechanical stop is placed at a height below the instability point.

$$V_p = V\left(\frac{2}{3}h_o\right) = \sqrt{\frac{8k}{27\epsilon_o W w}h_o^3} \tag{2.54}$$

The pull-in voltage represents an important limitation for "analog" DMTL phase shifter design. Due to this instability, it is clear that a switching ratio, C_r (2.44), is limited to 1.5 because beyond that voltage, the switch membrane snaps down and a very high (20-80) switching ratio results. Optimal designs require typical switching ratios (Figure 2.11) of 2-3. In practice and due to the fringing capacitance which does not change with height, the practical capacitance ratio is around 1.3.

An "analog" design consists of any DMTL phase shifter designed for a maximum capacitance ratio of $C_r \approx 1.3$. Because the capacitance ratio can be adjusted to be anywhere from 0-1.3 based on the voltage applied, the phase shift which results can be considered analog due to the infinite number of states obtainable.

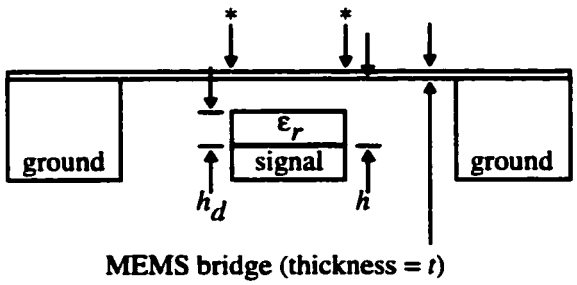


Figure 2.16: Cross section drawing showing the implementation of a thick dielectric to limit switch membrane travel.

The DMTL phase shifter can be made "digital" in several ways; two are mentioned here. In the first method, a very thick dielectric (Figure 2.16) is used to limit the travel of the MEMS switch. The capacitance of the MEMS switch in the up and down state is (ignoring the effect of fringing capacitance):

$$C_u^{-1} = \left(\frac{\epsilon_o W w}{h - h_d}\right)^{-1} + \left(\frac{\epsilon_o \epsilon_r W w}{h_d}\right)^{-1}$$
$$C_u = \frac{\epsilon_o \epsilon_r W w}{(h - h_d)\,\epsilon_r + h_d} \tag{2.55}$$

$$C_d = \frac{\epsilon_o \epsilon_r W w}{h_d} \tag{2.56}$$

and the capacitance ratio is:

$$C_r = \frac{C_d}{C_u} = \epsilon_r \left(\frac{h}{h_d} - 1\right) + 1 \tag{2.57}$$

which is drawn in Figure 2.16 for PECVD SiO_2 ($\epsilon_r = 3.5$) and PECVD Si_3N_4 ($\epsilon_r = 7.5$). This method presents a couple of challenges, the first of which is the required thickness. A typical design will have a switching ratio of $C_r = 2.5$ and a suspended switch height, h, of 1.5 to 2.0 μm for low-voltage electrostatic actuation. Using the equation above, oxide dielectric must be 1.0-1.3 μm and the nitride dielectric must be 1.2-1.6 μm, which are unrealistically thick for the deposition and etching tools available at the University of Michigan.

Furthermore, thick layers underneath the MEMS switch present a challenge to good MEMS switch fabrication. Because the sacrificial layer follows the contours of the materials below it, a large step height change will result at the points marked by an asterisk on

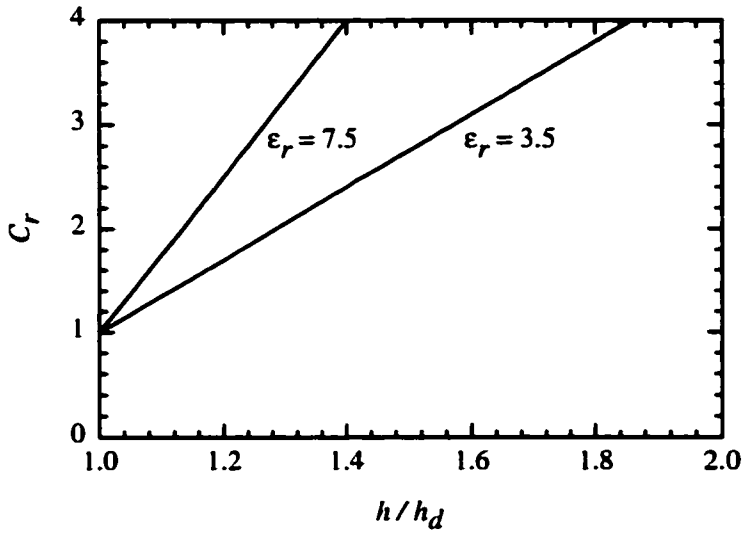


Figure 2.17: The MEMS switching ratio obtainable when a thick dielectric is used to limit membrane travel.

Figure 2.16. Since the MEMS membrane is less than a micron thick and the step height change is much greater than a micron, this change in step height will require reinforcement by a plating step on the switch membrane itself, which can create stress issues and bowing of the membrane.

Perhaps the biggest challenge to using thick dielectrics is the switching ratio instability introduced. If the switch membrane and dielectric layer below it are not perfectly smooth, the capacitance measured will be quite lower than the capacitance expected from the equation $C = \epsilon_r \epsilon_o A/d$. Charge buildup in the dielectric can exasperate this condition because moving charges in the dielectric will cause the membrane to "wiggle" on top of the dielectric, causing the capacitance to change with time. Since a stable down-state capacitance is required for a "digital" design, it may be argued that the thick dielectric method is not digital at all unless an extremely mature MEMS switch fabrication process is available.

The second "digital" implementation method uses a static stabilization capacitor, C_s, in series between the MEMS switch and the ground conductor (Figure 2.18). The total load

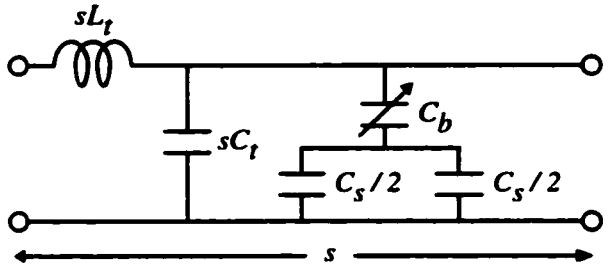


Figure 2.18: The simplified unit cell lumped model of a distributed phase shifter with static stabilization capacitance to ground. The model is accurate for $\omega \ll \omega_B$.

capacitance, C_L, on the transmission line is the series combination of the two capacitors:

$$C_L = \frac{C_b C_s}{C_b + C_s} \tag{2.58}$$

There are two states for the MEMS switch: up and down (pulled down completely by the electrostatic force). When the switch is pulled down, its capacitance is on the order of 1-3 pF whereas in the up state it is on the order of 30-100 fF. So, when the MEMS switch is in the down-state position, the load capacitance, C_L, seen by the line is dominated by the static capacitor, C_s, and $C_L \rightarrow C_{bd} \approx C_s$. When the MEMS switch is in the up-state position, the capacitance seen by the line is C_{bu} in series with C_s. The distributed capacitance can therefore be "discretely" controlled by the independent choice of the MEMS switch up-state capacitance, C_{bu} and the static capacitance, C_s and tends towards C_{bu}. Since the desirable switching ratio is on the order of 2-3, the MEMS switch capacitance is designed to be equal to 1-0.5 times that of the static capacitor. The ruggedness of this design is twofold. First, as a result of adding the static capacitor, the required MEMS switch loading capacitance becomes larger and thus easier to fabricate. Second, in comparison to the thick dielectric method, the stability of down state capacitance is greatly improved. Without a very mature MEMS switch fabrication procedure, as could only be obtained in industry, the MEMS switching capacitance ratio could be anywhere between 20-80. The stabilization capacitor makes this factor unimportant because the static capacitance, C_s, dominates in

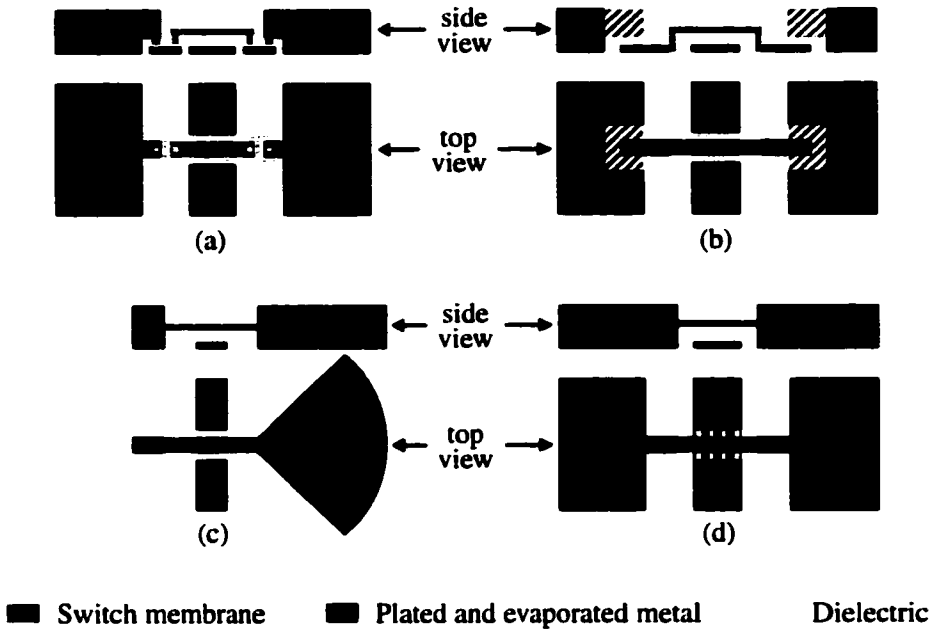


Figure 2.19: Implementations of a single-section of a DMTL using (a) metal-insulator-metal (MIM), (b) metal-air-metal (MAM), (c) microstrip-stub, and (d) two-state MEMS varactors.

the down-state position and this capacitance can be consistently fabricated. Therefore, the first "digital" method mentioned above (thick dielectric which limits switch membrane travel) is undesirable. Because of its great stability, the second method (series stabilization capacitor) is used for the work contained in this thesis. The second method also allows for a via-free microstrip design since a short electrical stub acts as a wideband capacitance to ground. This will allow for the first demonstration of not only a distributed microstrip phase shifter, but also a via-free one.

When discrete static capacitors are required, their loss is of paramount importance, as will be described in Chapter 3, but suffice it to say that for CPW designs, discrete capacitors can be implemented using standard metal-insulator-metal (MIM) capacitors, or for higher Q, the MIM capacitors can be replaced with metal-air-metal (MAM) capacitors, as seen in Figure 2.19.

2.11 Transmission Line Loss and Impedance

Closed form equations for transmission line characteristics (ex. loss, impedance, guided wavelength) are the first step to good design and optimization. Software packages such as Linecalc [1] which give transmission line characteristics at a single frequency and a single set of physical dimensions are suitable for a good design, but closed form expressions [38],[13],[51] are needed for optimization because they provide solution over a variety of physical dimensions and frequencies. However, often these equations have accuracy constraining limitations on them. For example the loss equations are often terribly inaccurate if they are used for thin metallizations since many equations assume several skin depths of conductor thickness, and if characterizing this loss is important, full-wave analysis may be required. Alternatively, one could use the equations such as those contained in [20] which accurately determine the R, L, C, and G of a transmission line, but these equations are quite extensive and are not used here. Generally, the loss equations used here are inaccurate and are scaled by a constant factor so that they correspond with either full-wave analysis or measurements. Even if the design equations are not absolutely accurate, they still serve an important role in identifying general design trends.

2.11.1 Coplanar Waveguide Transmission Line

Design equations for the impedance of a CPW line is determined using the conformal mapping technique assuming an infinitely thick substrate [13]. This technique uses the Elliptical function described in Equation (2.61):

$$Z_o = \frac{30\pi}{\sqrt{\epsilon_{eff}}} \frac{K'(k)}{K(k)} \tag{2.59}$$

where the effective dielectric constant is approximated by assuming half of the fields are present in the air above the metallization and the other half is in the substrate.

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} \tag{2.60}$$

The elliptic function, $K(k)$, can be approximated as follows:

$$K(k) = \frac{\pi}{2}\left(1 + \left(\frac{1}{2}\right)^2 k^2 + \left(\frac{1\cdot 3}{2\cdot 4}\right)^2 k^4 + \left(\frac{1\cdot 3\cdot 5}{2\cdot 4\cdot 6}\right)^2 k^6 + \cdots\right) \tag{2.61}$$

$$k = \frac{W}{W + 2\,G} \tag{2.62}$$

$$K'(k) = K(k') = K(\sqrt{1-k^2}) \tag{2.63}$$

where W is the width of the center conductor and G is the CPW gap, as shown in Figure 2.8.

An important design parameter of CPW lines is the total distance from ground conductor to ground conductor, $S = W + 2\,G$. For an equivalent impedance line, as S increases, W will widen, which will result in a lower loss transmission line. So, typically a CPW line is made (assuming layout space doesn't prevent it) as wide as possible for low loss performance. Practically, the high limit for S is $S < \lambda_g/10$ where λ_g is the guided wavelength $(c/f\sqrt{\epsilon_r})$. For example, for a CPW line on a quartz substrate at 10 GHz, $S < 1,550$ μm before the line begins to radiate substantially into the substrate.

The conductor loss of a CPW line, accounting for the effect of metallization thickness, assuming it is greater than four skin depths is [13]:

$$\begin{aligned}\alpha_c = F_f \frac{8.686 R_s \sqrt{eff}}{4\eta S K(k) K(k')\,(1-k^2)} \\ \times \left[\frac{2S}{W}\left(\pi + \ln\left[\frac{4\pi W(1-k)}{t(1+k)}\right]\right) + 2\left(\pi + \ln\left[\frac{4\pi S(1-k)}{t(1+k)}\right]\right)\right] \text{ (db/m)}\end{aligned} \tag{2.64}$$

where F_f is a fudge factor since Equation 2.64 follows the correct trend for loss vs. impedance but underestimates the loss. The sheet resistance, R_s of the conductor is:

$$R_s = \sqrt{\frac{\pi f \mu_o}{\sigma}} \tag{2.65}$$

Dielectric loss is minimal, especially on quartz substrates ($\tan\delta = 0.0009$):

$$\alpha_d = 2.73 \frac{\tan\delta}{\lambda_o} \text{ (dB/m)} \tag{2.66}$$

Radiation loss is also present in an unloaded CPW line on a thick dielectric substrate because the wave velocity of the transmission line is greater than the phase velocity of the waves in the dielectric [43]. This loss is given by:

$$\begin{aligned}\alpha_{rad} &= \left(\frac{\pi}{2}\right)^5 \frac{1}{\sqrt{2}} \frac{(1-\epsilon_r)^2}{\sqrt{1+\epsilon_r}} \frac{f^3 S^2}{c^3 K(k) K(k')} \\ k &= \frac{W}{S} \\ k'^2 &= 1 - k^2\end{aligned} \tag{2.67}$$

Physical parameters μm	f GHz	eqn. ϵ_{eff}	meas. ϵ_{eff}	eqn. $Z_o\ \Omega$	meas. $Z_o\ \Omega$	eqn. loss dB/m	meas. loss dB/m
W=200, G=350	10	2.30	2.33	113.9	114.8	11.1	11.0
W=300, G=300	10	2.30	2.34	97.2	98.0	9.9	10.0
W=400, G=250	10	2.30	2.34	84.8	85.4	9.8	9.8
W=500, G=200	10	2.30	2.34	74.6	75.2	10.2	10.2
W=100, G=175	30	2.30	2.38	113.9	114.8	39.7	39.3
W=150, G=150	30	2.30	2.38	97.2	97.9	35.6	35.6
W=200, G=125	30	2.30	2.38	84.8	85.5	34.8	34.9
W=250, G=100	30	2.30	2.39	74.6	75.2	36.5	36.3

Table 2.2: CPW line parameter comparison on quartz. The scaling factor $F_f = 1.32$ for the 10 GHz calculation and $F_f = 1.47$ for 30 GHz.

where $S = W+2G$ and $K(k)$ is the complete elliptic integral of the first kind. This radiation into the substrate occurs primarily around the angle:

$$\cos\psi = k_z/k_d \tag{2.68}$$

where k_z is the propagation constant of the line and k_d is the propagation constant in the dielectric. However, a very interesting characteristic of DMTLs built on low dielectric constant substrates is that the wave velocity of the transmission line is *slower* than the phase velocity of the dielectric. Therefore the angle necessary to phase match the wave on the transmission line to the wave in the dielectric, ψ, becomes imaginary indicating that radiation, and therefore radiation loss, cannot occur for DMTL transmission lines. Total loss of the coplanar line, therefore, is approximated by the conductor loss equation (2.64). This is not to say that radiation loss does not exist in a distributed phase shifter. Certainly, there is radiation at any discontinuity in the structure, especially where the MIM or MAM capacitors are. But in general, this loss is not quantifiable through closed form equations.

Table 2.2 demonstrates the accuracy of these design equations compared to test structures fabricated and measured. As mentioned, the equations are not absolutely accurate but still have been proven to be useful in choosing an optimal design [7].

Physical parameters μm	f GHz	eqn. ϵ_{eff}	meas. ϵ_{eff}	eqn. $Z_o\ \Omega$	meas. $Z_o\ \Omega$	eqn. loss dB/m	meas. loss dB/m
W=400, h=900	10	2.61	2.71	110.3	109.9	5.54	5.66
W=600, h=900	10	2.67	2.77	94.9	94.1	4.75	4.74
W=800, h=900	10	2.71	2.82	83.8	83.1	4.33	4.25
W=1,000, h=900	10	2.75	2.88	75.5	74.7	4.07	3.93

Table 2.3: Microstrip line parameter comparison on quartz.

2.11.2 Microstrip Transmission Line

The closed form expression for microstrip transmission lines are quite extensive and they are presented in Appendix A. Table 2.3 compares results from the equations to method of moments simulations [49] which have demonstrated to very well fit test structure measurements.

2.12 Optimization

2.12.1 The Effect of Conductor Loss

As discussed in Section 2.8, phase shift is inexorably tied to the DMTL reflection loss. The further away loading impedances are placed from 50 Ω, the more the phase shift per section increases with corresponding increase in reflection loss. The phase shift per section is also dependent on the unloaded impedance, Z_o. Up to this point in the chapter, Z_o was arbitrarily chosen to be around 100 Ω for a design with reasonable physical dimensions. Now, Z_o will be optimized because not only does it impact phase shift per section, but also the total loss of the DMTL phase shifter. The unloaded impedance Z_o is optimized to obtain the maximum amount of phase shift for the smallest amount of loss given a particular design frequency, substrate, and type of transmission line.

It is important to recognize that when a transmission line is loaded such that the impedance is changed (for example, from 100 Ω to 41.8 Ω), the loss of the line is increased due to a change in the amount of current on the line for the same amount of transmitted power. Consider a transmission line which is represented by a series inductance and resistance per unit length, L_t and R_t, and by a shunt capacitance and admittance per unit

length, C_t and G_t, respectively, the attenuation constant α is given by [38]:

$$\alpha = \frac{R_t}{2Z} + \frac{G_t Z}{2} \quad \frac{\text{Np}}{\text{unit length}} \tag{2.69}$$

In a planar transmission line such as microstrip or CPW, R_t represents the conductor loss while G_t represents the dielectric loss. For the lines considered in this work (on low loss substrates at mm wave frequencies), the conductor loss dominates and the attenuation constant can be approximated as $\alpha = R_t/(2Z)$. For example, take a CPW line on a quartz substrate having an impedance of 100 Ω at 10 GHz. If the loss of this line is 20 dB/m then $R_t = 460$ Ω/m. By loading this 100 Ω line to 50 Ω, the conductor loss, R_t, remains constant. Thus, a change in the characteristic impedance from a high impedance to a low impedance will increase the loss by a factor of the ratio of the high to low impedances. This factor of increased loss must be included in the optimization.

The unloaded impedance is optimized in the following manner: the phase shift per centimeter ($\Delta\phi/s$) versus the unloaded impedance is determined using Equation (2.46) and is shown in Figure 2.20 for quartz and silicon substrates. The length of each section (the separation between MEMS switches, s) is taken out of consideration and therefore the result of optimization here is independent of the DMTL Bragg frequency. Loading impedances are selected such that $RL_{max} = -15$ dB (Table 2.1) and the design frequency (f_o) is selected to be 10 GHz arbitrarily to demonstrate the optimization procedure.

The corresponding loss per centimeter for a CPW line (Figure 2.21) and microstrip line (Figure 2.22) are determined by (2.64) and Appendix (A.16). Both graphs show that the loaded line loss increases for a high unloaded impedance, Z_o, due to the narrow signal conductor of the unloaded line and the multiplicative factor of Z_o/Z_d.

The optimal unloaded impedance is obtained by dividing the phase shift per centimeter (Figure 2.20) by the transmission line loss per centimeter (Figures 2.21 and 2.22), which results in the optimization graph of phase shift per dB of loss (Figures 2.23 and 2.24 for CPW and microstrip, respectively).

For a CPW design, the figure shows that a maximum occurs around an unloaded impedance of Z_o = 90-100 Ω for quartz substrates. For silicon substrates, the best performance occurs at $Z_o < 60$ Ω, which is not possible since the unloaded impedance must be

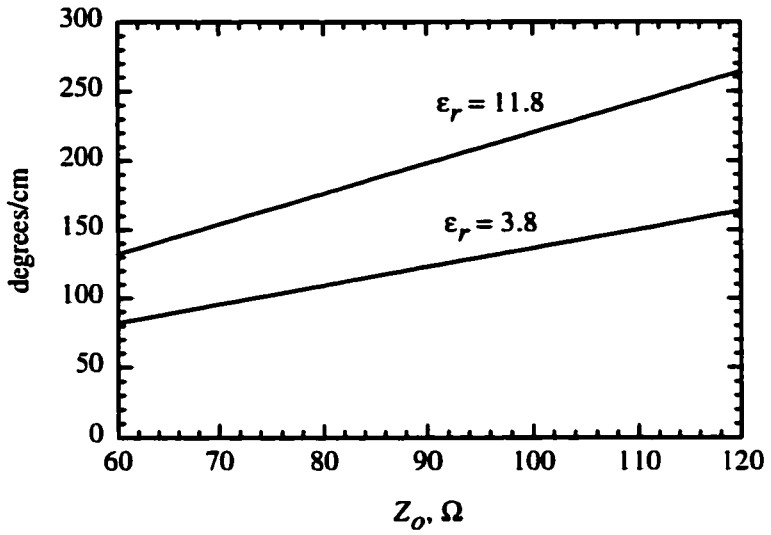


Figure 2.20: Phase shift versus unloaded impedance on quartz and silicon substrates. Results are independent of transmission line type. $f_o = 10$ GHz, $RL_{max} = -15$ dB.

significantly greater than the loaded impedance, Z_u.

For a microstrip design, the figure shows that a maximum occurs at an unloaded impedance less than 60 Ω. Again, this choice would not be possible and an unloaded impedance around 70-80 Ω is appropriate for a reasonable switching ratio (C_r).

For CPW and microstrip designs, the phase shift per dB of loss for the DMTL phase shifter improves with frequency since the phase shift increases linearly (2.46) with frequency while the loss, if dominated by conductor loss, increases as $\sqrt{f}$ with frequency. There is, however, an upper frequency limit of operation determined by the allowable reflection coefficient, which in turn, is dependent on the Bragg frequency selected.

2.12.2 Effect of the Loading Capacitor

Using conductor loss (as outlined in the previous section) is a good first cut approach to demonstrating a procedure for optimization, but the DMTL phase shifter does not just consist of conductor loss; Q loss in the static loading capacitor, C_s, often has the same order of magnitude loss as conductor loss.

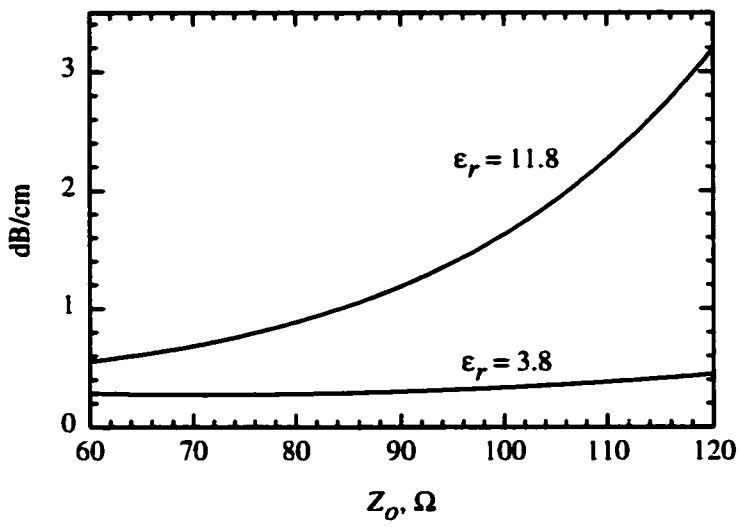


Figure 2.21: Coplanar waveguide loaded transmission line loss versus unloaded impedance. $f_o = 10$ GHz, $W + 2G = 900$ μm for quartz, and $W + 2G = 500$ μm for silicon.

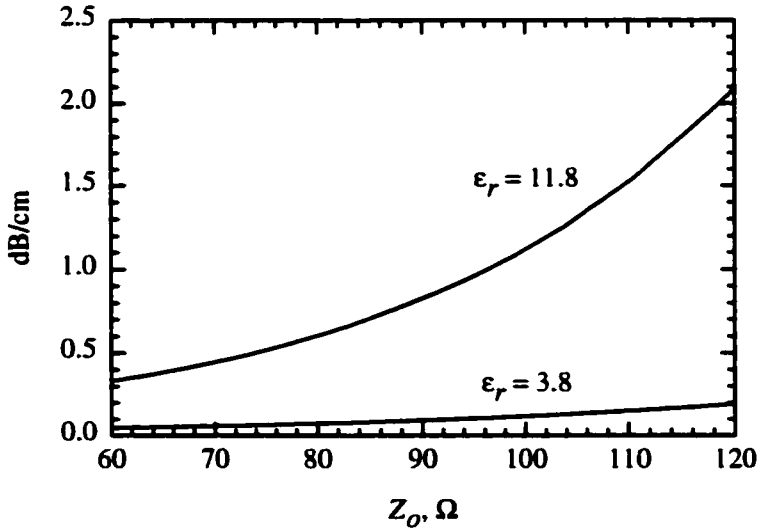


Figure 2.22: Microstrip line loaded transmission line loss versus unloaded impedance. $f_o = 10$ GHz, substrate height $d = 500$ μm for silicon, and $d = 900$ μm for quartz.

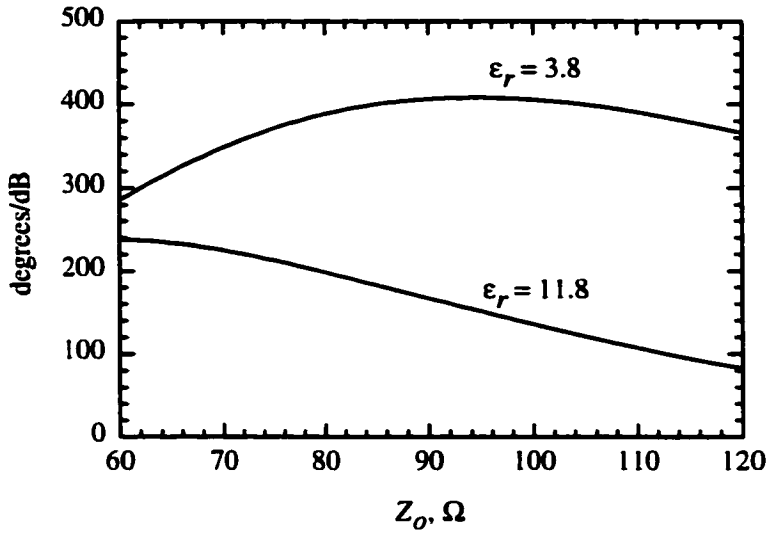


Figure 2.23: Coplanar waveguide phase shift per dB of loss versus unloaded impedance. Optimal designs are at the maximum (90-100 Ω for quartz). $f_o = 10$ GHz.

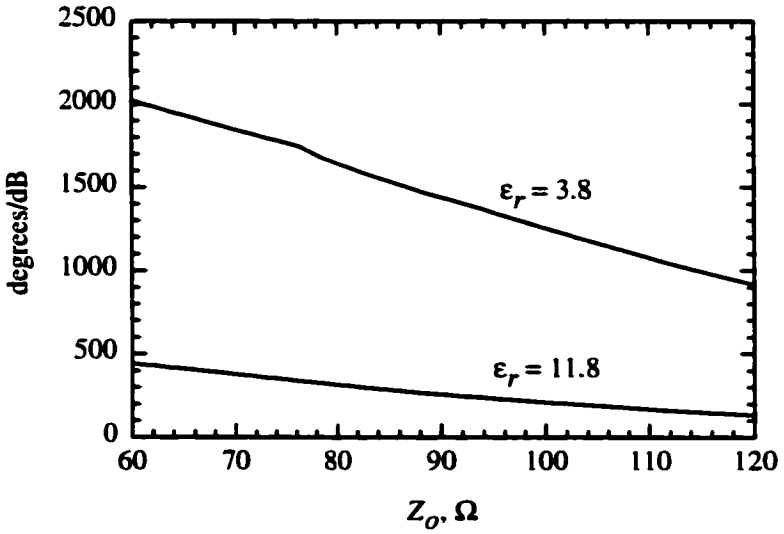


Figure 2.24: Microstrip line phase shift per dB of loss versus unloaded impedance. $f_o = 10$ GHz.

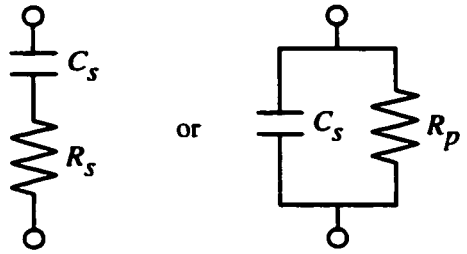


Figure 2.25: The lumped model of a lossy static capacitor.

Total Q loss actually consists of loss due to series resistance loss in the MEMS switch and the static capacitor and, in addition, loss due to bias lines if they are directly connected to the MEMS switches for electrostatic actuation. The resistance of the MEMS switch itself, which is typically a 80 μm wide by 300 μm long, 8000 $\AA$ thick piece of gold is typically 0.1 to 0.3 Ω [32]. The loss due to resistance in the static capacitor, C_s, is typically much larger than that of the MEMS switch, but both are included in the following analysis.

The lossy static capacitor is modeled as a resistance, R_p, in parallel with C_s (or a resistance, R_s, in series with C_s). See Figure 2.25. The capacitor Q can be written as:

$$Q = \omega C_s R_p = \frac{1}{\omega C_s R_s} \tag{2.70}$$

where

$$R_s = \frac{1}{\omega^2 C_s^2 R_p} \tag{2.71}$$

The total resistance to ground is equal to the switch resistance, R_b, plus two parallel resistances, R_s, due to the Q of the static capacitors:

$$R_q = R_b + R_s = R_b + \frac{1}{\omega Q C_s} \tag{2.72}$$

Keep in mind that for a typical CPW layout, the total static capacitance is split into two equal parts (one in each gap) to keep guided fields in the transmission line balanced (see Figure 2.26). This effectively means there are two Q losses, $2R_s$, in parallel for each capacitor $C_s/2$. Both means of modeling result in the same result.

For microstrip designs, the loading capacitors may either be in parallel (butterfly stub) or loaded on a single alternating side (radial stub) depending on the amount of space available between the MEMS switches. For convenience of notation, C_s will always represent the total loading required for each design regardless of how such a capacitance is implemented.

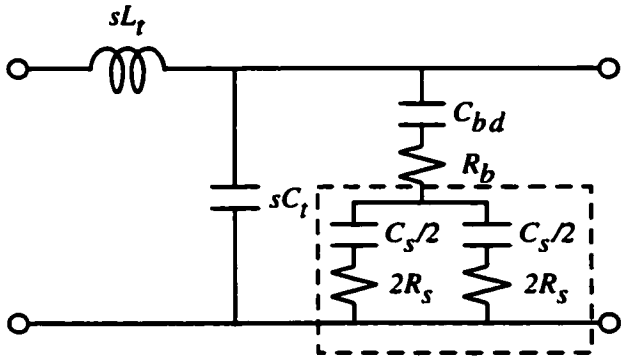


Figure 2.26: Lumped model of the DMTL phase shifter. A box is drawn around the lossy static capacitor, C_s.

The total loss, therefore, is the sum of loaded transmission line loss (2.69) plus Q loss:

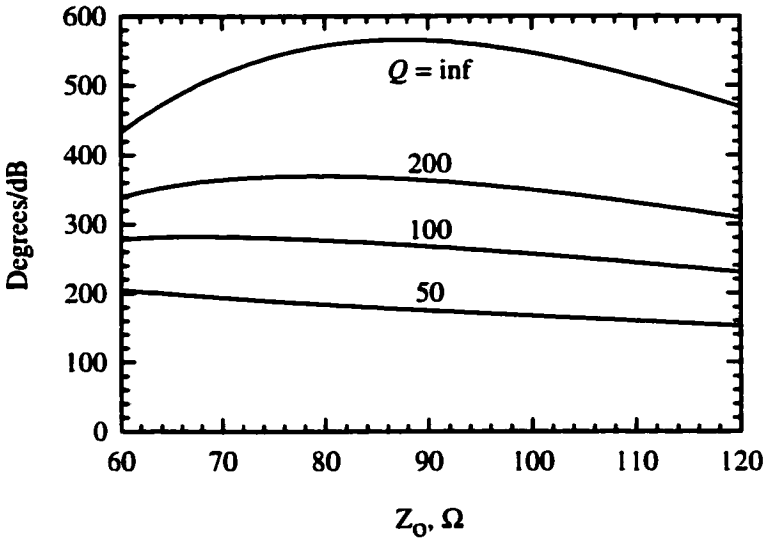
$$\alpha \cong 8.686 \left(\frac{R_t}{2Z_L} + \frac{R_q Z_L \omega^2 C_L^2}{2} \right) \quad \text{dB/section} \tag{2.73}$$

where Z_L and C_L are the loaded impedances and loading capacitances, respectively.

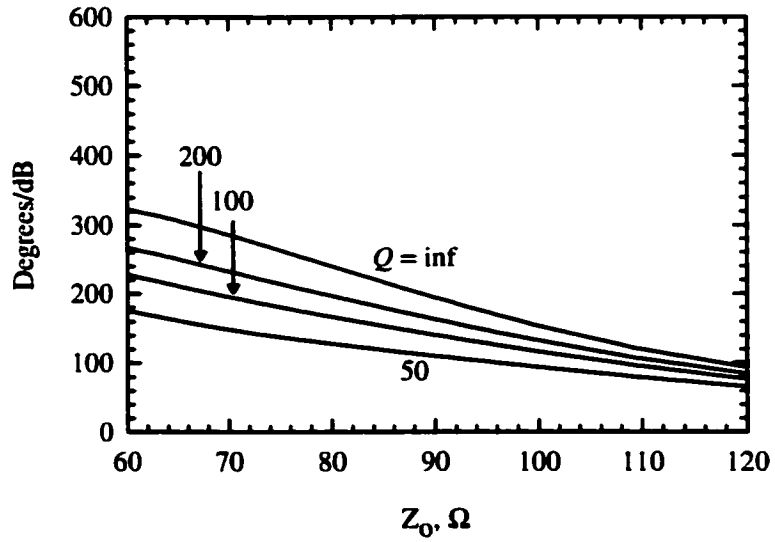
This expression can be simplified by ignoring the minor effect of switch resistance on performance, since the capacitor Q loss usually dominates:

$$\begin{aligned} \alpha &\cong 8.686 \left(\frac{R_t}{2Z_L} + \frac{Z_L}{2R_p} \right) \\ &= 8.686 \left(\frac{R_t}{2Z_L} + \frac{Z_L \omega C_L}{2Q} \right) \quad \text{dB/section} \end{aligned} \tag{2.74}$$

The Q of the static capacitors can range from 10-600 depending on the fabrication techniques used and the presence of other loss factors such as bias lines (discussed in the next chapter). Loss calculations (both conductor and Q loss) are made for the down state impedance because in both cases, the down state loss is much larger than the up state loss. In the previous section, while considering the conductor loss alone, the separation between the MEMS switches, and therefore the Bragg frequency, is taken out of consideration. But now that the capacitor Q loss is included, the number of switches and the separation between them must be known. To demonstrate the optimization procedure here, the Bragg frequency is selected to be three times the design frequency ($f_B = 30$ GHz).

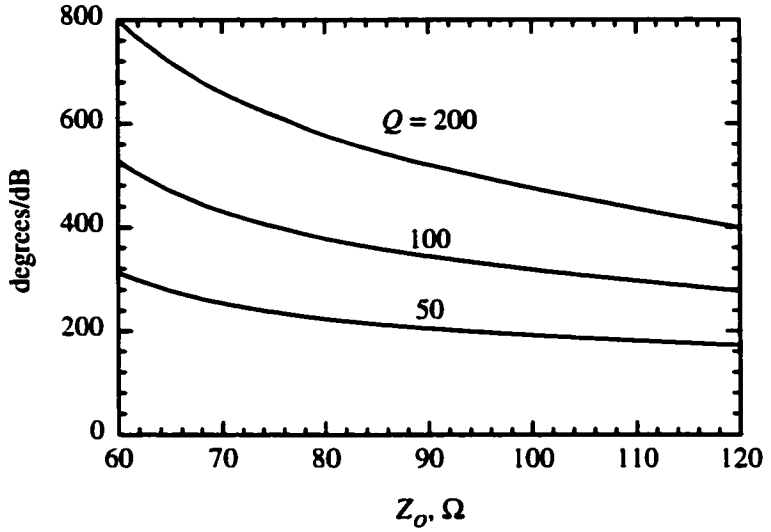


(a)

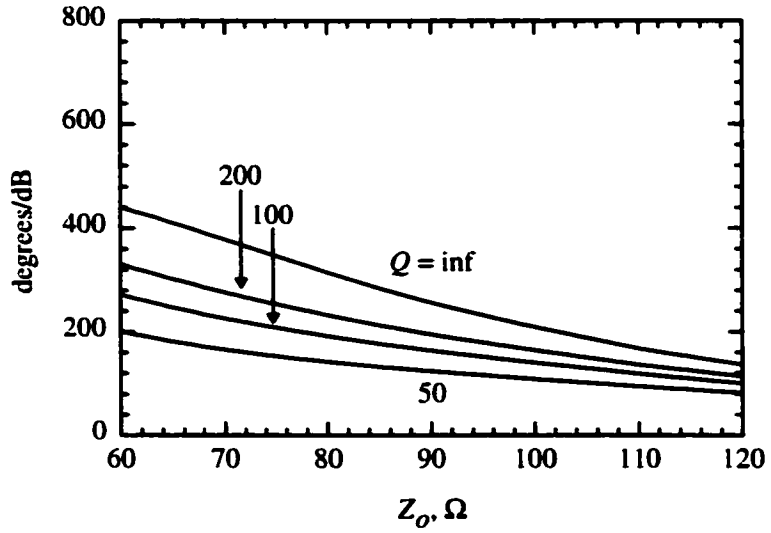


(b)

Figure 2.27: Coplanar waveguide phase shift per dB of loss versus unloaded impedance for (a) quartz and (b) silicon substrates. $f_o = 10$ GHz, $f_b = 30$ GHz.



(a)



(b)

Figure 2.28: Microstrip line phase shift per dB of loss versus unloaded impedance for (a) quartz and (b) silicon substrates. f_o = 10 GHz, f_b = 30 GHz.

2.12.3 CPW Optimization

Figure 2.27 shows the coplanar waveguide topology optimization curves for quartz and silicon substrates. As figure (a) shows, the choice of the unloaded impedance is not particularly important on a quartz substrate. Also, there is little improvement between $Z_o = 60$ and 120 Ω for Q = 50-200 and therefore on a quartz substrate, the CPW line dimensions should be chosen to result primarily in a reasonable MEMS pull down voltage, and an acceptable CPW gap so as to allow the easy integration of loading capacitors.

On a silicon substrate using a coplanar waveguide topology (Figure 2.27b), performance significantly improves with a lower unloaded impedance. Low impedance CPW lines, however, have a small gap between center conductor and ground conductor , especially on silicon substrates. Eventually, the gap becomes too small to anchor the MEMS switch to the substrate and fit in a series capacitor. As with coplanar designs on quartz, the choice of unloaded impedance is dominated mostly by layout considerations.

2.12.4 Microstrip Optimization

Figure 2.28 shows the microstrip topology optimization curves for quartz and silicon substrates. As seen in the figure, microstrip designs on both substrates tend to become more optimal as the unloaded impedance approaches the loaded impedance, Z_u, as shown in the Section 2.12.1 where the switch and series capacitor loss was ignored. Therefore, as mentioned in that section, the choice of the unloaded impedance is selected to be anywhere between 70-80 Ω to result primarily in an acceptable (i.e., narrow) microstrip line width so that the MEMS switch does not become too long and unstable.

2.13 Typical Optimized Designs

2.13.1 Designs on Different Substrates

Equation (2.46) shows that the phase shift is directly dependent on $\sqrt{\epsilon_{eff}}$, and therefore, a DMTL on a silicon substrate results in more phase shift per unit length than a DMTL on a quartz substrate. However, the line loss per unit length on silicon is much higher than

that on quartz, and therefore, the best substrate choice is not immediately clear.

Table 2.4 shows the design parameters for a 10 GHz DMTL phase shifter with $S_{11} \leq -15$ dB and $f_B = 2.3\ f_o$ on several substrates. Reasonable choices for unloaded impedance are $Z_o = 110,\ 90,\ 70\ \Omega$ for air, quartz, and silicon substrates, respectively. The MEMS switch is assumed to be ideal, and the loss is solely determined by the fixed lumped capacitor and the transmission line. It is seen from the table that the Q of the lumped capacitor must be higher than 150 at 10 GHz in order to result in excellent performance. For this reason, low loss air dielectric capacitors were designed and implemented in the improved designs contained in this thesis.

It is also seen from the table that for best performance, low loss substrates should be used. Here, a quartz design outperforms silicon by 58% for $Q = 200$. This assumes, of course, that such a high Q capacitor can be implemented, but notice that for a $Q = 50$, loss is dominated by the capacitor and the difference in line loss for the two substrates has little effect on the overall performance. Still, $Q = 50$ is excellent and results in 2 dB loss per 360° of phase shift on a quartz substrate. Since most processes result in a Q between 100-200, it is seen that quartz is the best substrate for DMTL phase shifters, since air substrates are not practical for MEMS circuits [9].

2.13.2 Microstrip vs. CPW Implementations

Microstrip lines inherently have lower loss than CPW lines so it is natural to ask what the performance of DMTL phase shifters are on microstrip vs. CPW, using the optimization procedure in Section 2.12.2 which accounts for both conductor and Q loss. As discussed previously, the static lumped capacitors used in CPW topologies could be used for microstrip designs at low frequencies if via holes are used. However, designs with via holes at higher frequencies would not be practical because of inductive parasitics (40-150 pH) which will pull the Bragg frequency down. Practically, via holes limit the upper frequency of operation to around 20 GHz. Besides, it is much easier to fabricate without via holes and as it turns out, there is a very practical way of implementing capacitors in a microstrip DMTL phase shifter without using via holes. In microstrip designs, static lumped capacitors are replaced

Substrate (ϵ_r)	Air (1.0)	Quartz (3.8)	Silicon (11.8)
S (μm)	1500	900	500
W (μm)	890	370	120
G (μm)	305	265	190
Z_o (Ω)	110	90	70
s (μm)	1575	1245	975
C_{lu} (fF)	114	90	44
C_r	2.5	2.9	4.8
C_{ld} (fF)	285	261	211
sections per 180°	12.0	12.0	12.0
length per 180° (mm)	18.9	14.9	11.7
loss (dB), $Q = inf$	0.23	0.34	0.67
loss (dB), $Q = 200$	0.42	0.52	0.82
loss (dB), $Q = 100$	0.62	0.70	0.96
loss (dB), $Q = 50$	1.00	1.05	1.25

Table 2.4: DMTL phase shifter with 180° of phase shift: design parameters on air, quartz and silicon substrates (f_o = 10 GHz, $f_B = 2.3\ f_o$).

with open ended stubs which have a Q of 50-150 in the frequency range of 10 to 30 GHz.

These radial stubs are much shorter than a quarter wavelength at the design frequency and act as a capacitor referenced to RF ground. They may either be placed on both anchors of the MEMS switch (butterfly stubs) or may be placed on a single side (radial stub or simple square stub). For the designs contained in this work, often a single radial stub is used on alternating sides of the MEMS switch (Figure 2.29) so that the required small separation between the switches does not lead to stub overlap or RF coupling.

There is a disadvantage to using radial stubs. Since their capacitance to ground is not constant with frequency (Figure 2.30), the loaded impedances will change with frequency as a result of the Bragg frequency *and* the non-constant loading of a radial stub. Figure 2.10 shows an example of how phase shift linearity is degraded by the Bragg frequency alone. Figure 2.31 shows that non-constant capacitance loading also degrades phase shift linearity.

Ultimately, the performance of microstrip vs. CPW designs depend on line loss *and* Q. Although line loss is lower in microstrip, the Q of a microstrip stub may be lower than that of a MAM capacitor used in a CPW design. This topic will be explored more in Chapter 3.

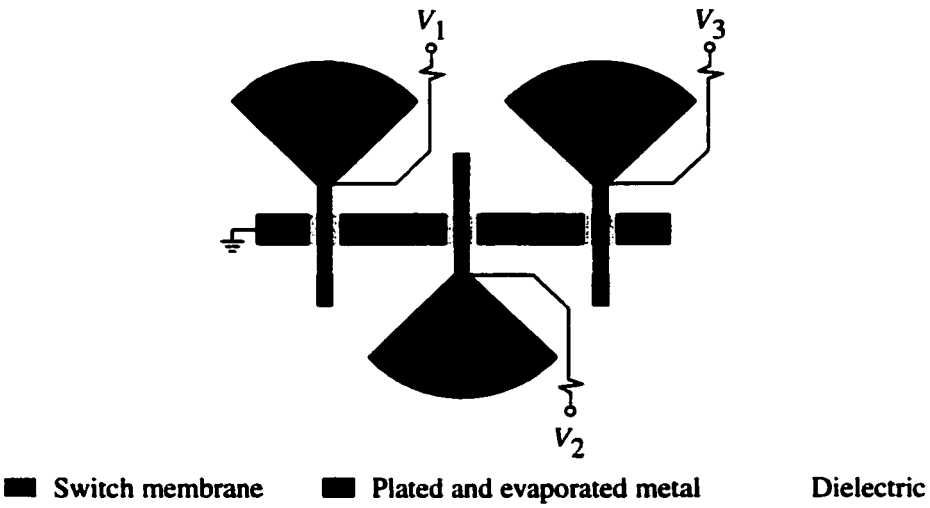


Figure 2.29: Implementation of radial stubs in a DMTL phase shifter when the space between switches is small.

2.14 MEMS Switch Failure

Assume a single MEMS switch on a DMTL phase shifter fails, then two things will happen:

1. Since each section of the DMTL is responsible for a portion of the total phase shift (2.46), a switch failure will reduce phase by the ratio $(N-1)$ / N where N is the total number of MEMS sections:

$$N = \frac{D\,\mathrm{c}}{360 s f_o Z_o \sqrt{\epsilon_{eff}}} \frac{Z_d Z_u}{Z_d - Z_u} \tag{2.75}$$

where D is the desired phase shift in degrees at the design frequency f_o. The separation, s (which is dependent on the Bragg frequency, f_B), between the MEMS switches can be eliminated from the expression using (2.41):

$$N = \frac{D\pi f_B}{360 f_o} \frac{Z_u}{Z_d - Z_u} \tag{2.76}$$

Lower Bragg frequency designs have less sections and therefore the effect on the reduction in phase shift $(N-1)$ / N will be larger.

2. A switch failure will change the DMTL measured S-parameters as a result of the impedance change of the MEMS DMTL. The total effect depends on the placement

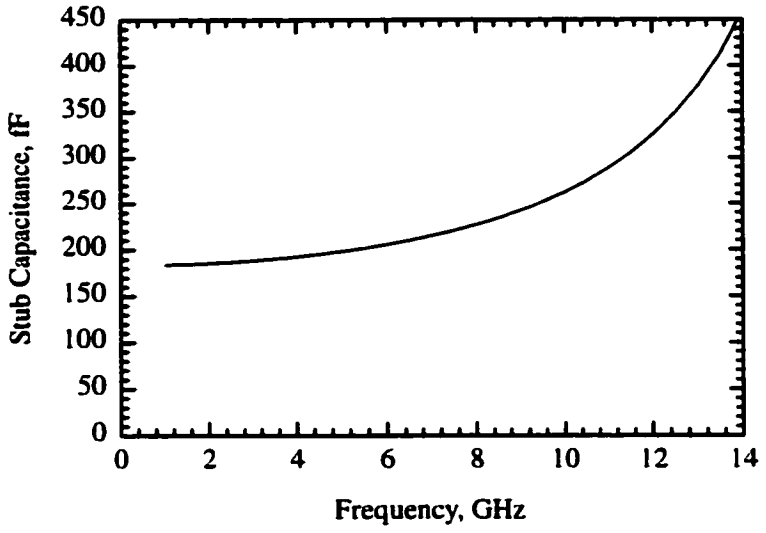


Figure 2.30: Capacitance of a microstrip radial stub versus frequency. $h = 900\ \mu m$, $e_r = 3.8$.

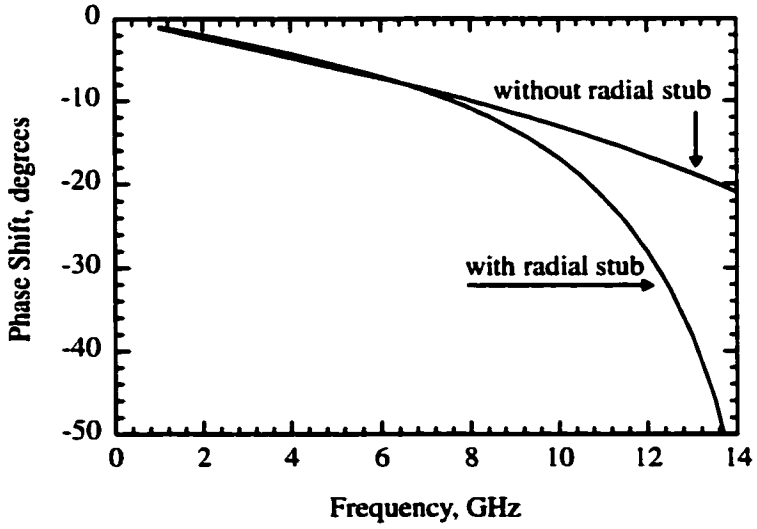


Figure 2.31: The non-constant capacitance effect of a microstrip radial stub on phase shift linearity.

$f_o\ (GHz)$	30	90
S (μm)	450	200
W (μm)	185	80
G (μm)	133	60
s (μm)	415	135
C_{lu} (fF)	30	10
C_r	2.9	2.9
C_{ld} (fF)	87	29
sections per 180°	12.0	12.0
length per 180° (mm)	5.0	1.6
loss (dB), $Q = inf$	0.37	0.44
loss (dB), $Q = 200$	0.55	0.61
loss (dB), $Q = 100$	0.72	0.79
loss (dB), $Q = 50$	1.08	1.15

Table 2.5: Scaled quartz CPW designs ($\epsilon_r = 3.8$, $Z_o = 90\ \Omega$, $f_B = 2.3\ f_o$).

of the failure in the DMTL and therefore, the worst case scenario is best found by comparing simulated results of reflection and transmission from a single port. The worst case effect of a single MEMS switch failure is often negligible on insertion and return loss.

2.15 Scaling to Other Frequencies

The 10 GHz designs in the previous sections can be easily scaled to 30 GHz or 90 GHz. The up and down state impedances (2.40) and the capacitance ratio (2.44) are not affected by the design frequency. The only design change is the spacing between MEMS switches, s, and the up state capacitance value, C_{bu} (2.42), which are dependent on the higher Bragg frequencies required at 30 and 90 GHz. Ground to ground spacing, $S = W + 2G$, in a CPW implementation must be reduced at higher frequencies as described in Section 2.11.1 to reduce radiation loss. For microstrip designs, the substrate must be thinner to reduce this radiation loss as described in Section 2.11.2. Table 2.5 presents scaled CPW designs at 30 and 90 GHz ($f_B = 2.3 f_o$) on a quartz substrate.

2.16 Multiple Bit Digital Designs

Finally, having obtained "discrete-type" distributed MEMS phase shifters, one can cascade several sections with predetermined phase shifts (180°, 90°, 45°, ...) to result in an N-bit phase shifter. Typically, a maximum reflection coefficient of -15 dB per section is required since the overall cascaded performance is expected to remain lower than -10 dB for any state of the phase shifter.

The bias arrangement in a microstrip implementation is easy: each MEMS switch is connected to high resistivity bias lines (Fig 2.29) and the microstrip conductor is connected to DC ground. Individual MEMS switches can therefore be uniquely actuated. For example, if turning on 7 out of 21 switches results in 90° of phase shift, 14 out of 21 will result in 180° and all 21 will result in 270° of phase shift.

For a CPW design, the bias voltage is connected to the center conductor using high resistivity bias lines and very large capacitors are used to isolate the different bits (Figure 2.32). In a 2-bit design, bias lines are not required because a single DC blocking capacitor can be used in the CPW center conductor, and the bias voltage can be applied from the input and output ports of the phase shifter (Figure 2.32). In this case, two bias-T circuits are required at the input and output ports to isolate the applied DC voltage from the network analyzer.

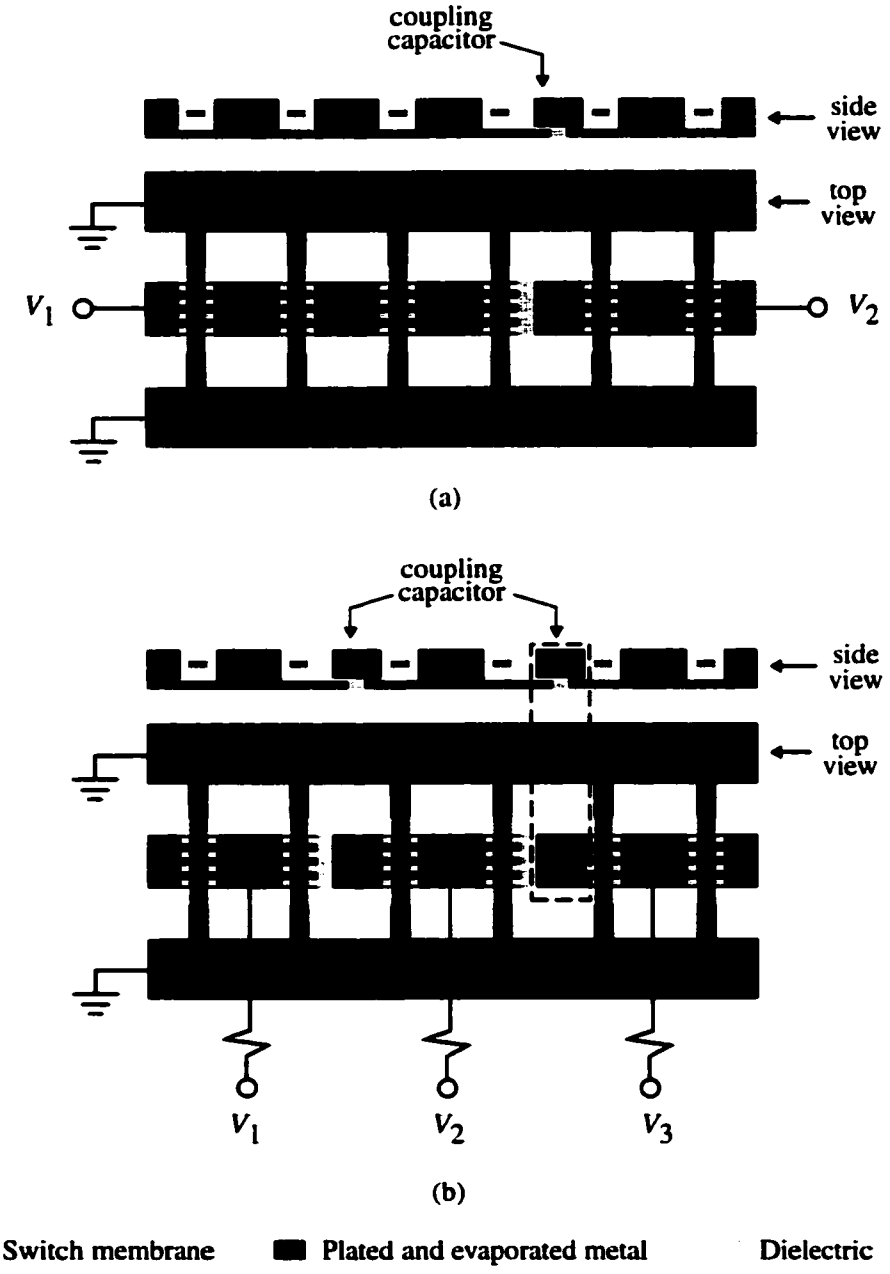


Figure 2.32: Biasing configurations for two or more bit DMTL phase shifters.

CHAPTER 3

ACCURATE CAPACITOR Q MEASUREMENT

3.1 Introduction

A high Q capacitor, along with the MEMS switch, is an essential component of a low-loss distributed phase shifter. The effect of Q, detailed in Section 2.12, shows that a $Q > 100$ is required for optimal design. This chapter will describe the techniques used to measure Q loss in MIM (Metal-Insulator-Metal) or MAM (Metal-Air-Metal) capacitors, and their corresponding test structures. The first technique described is based on a reflection coefficient measurement and it will be shown that the method is valid only for measuring relatively low Q (< 60) values. The second technique described is based on a full S-parameter, distributed structure measurement, which can be used to measure much higher Q (> 100) values. Also contained in this chapter are X-band measurements of MIM and MAM capacitors and K-band measurements of MAM capacitors using the distributed technique.

3.2 Reflection Coefficient Technique

Section 2.12.2 presented that a lossy capacitor, C_s, modeled as a capacitance in series with a resistor, R_s, results in:

$$Q = \frac{1}{\omega C_s R_s} = \frac{|X|}{R_s} \tag{3.1}$$

where the impedance of the capacitor is defined in (3.2) and the capacitance, $C_s = 1/(\omega|X|)$.

$$Z_c = R_s + jX \tag{3.2}$$

The reflection coefficient of this impedance is defined as in (3.3) in a measurement system which has a port impedance Z_p. Assuming $S_{11} = a + jb$, the complex impedance of the lossy capacitor can be determined in terms of a and b as follows:

$$S_{11} = \frac{Z_c - Z_p}{Z_c + Z_p} \tag{3.3}$$

$$\begin{aligned} Z_c = R_s + jX &= Z_p\left(\frac{1+S_{11}}{1-S_{11}}\right) = Z_p\left[\frac{(1+a)+jb}{(1-a)-jb}\right] \\ &= Z_p\left[\frac{(1+a)+jb}{(1-a)-jb}\cdot\frac{(1-a)+jb}{(1-a)+jb}\right] = Z_p\left[\frac{1-a^2-b^2+j2b}{(1-a)^2+b^2}\right] \end{aligned} \tag{3.4}$$

therefore,

$$\begin{aligned} R_s &= Z_p\left[\frac{1-a^2-b^2}{(1-a)^2+b^2}\right] \\ X &= Z_p\left[\frac{2b}{(1-a)^2+b^2}\right] \end{aligned} \tag{3.5}$$

From these equations, the Q of the capacitor can be calculated directly from the reflection coefficient:

$$Q = \frac{|X|}{R_s} = \frac{2b}{1-a^2-b^2} = \frac{2\ \mathrm{Im}\,(S_{11})}{1-|S_{11}|^2} \tag{3.6}$$

In practice, measuring this reflection coefficient is quite simple using the de-embedding technique of a TRL calibration for MIM capacitors placed in the gap of a CPW transmission line (Fig. 3.1). The transmission line is kept short, so that the capacitance of the MIM capacitor dominates the additional capacitance introduced by the transmission line itself. For an even more accurate capacitance measurement, an additional structure is also measured, which does not have capacitors in the gap, as shown in Figure 3.1b. This reference capacitance, which is that of the transmission line alone, is typically $\sim$ 15 fF for an X-band test structure.

There is a limit to how far this technique can be used to accurately extract the capacitor Q. As seen in Equation 3.6, the Q measurement becomes extremely sensitive as the magnitude of the reflection coefficient approaches unity, since at this point, the denominator approaches zero. The limit to which this reflection coefficient technique can be used is determined from the capacitance values in a typical design and from the instability caused by the denominator of Equation 3.6. Define the constant, M, to represent this instability

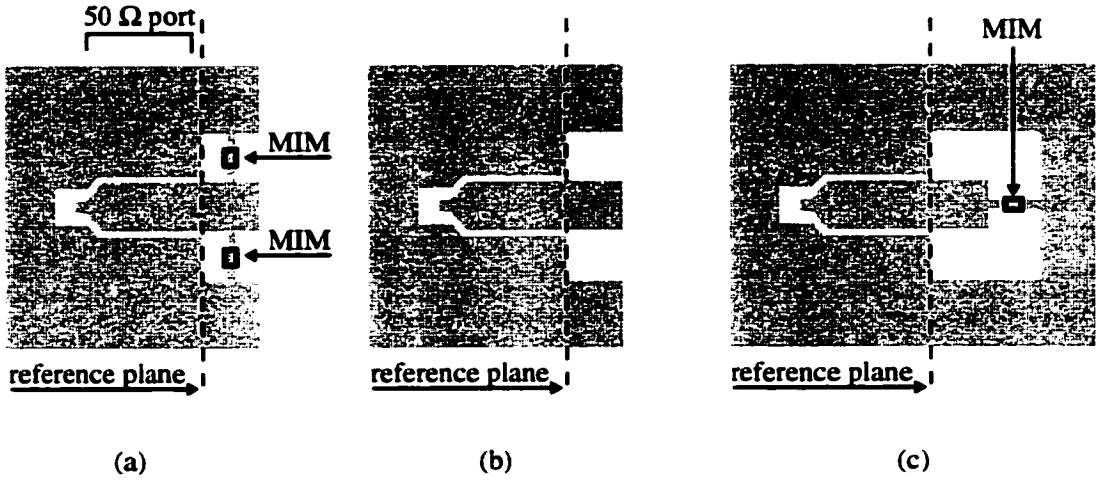


Figure 3.1: Typical test structures used with the reflection coefficient technique to determine capacitor Q.

point such that:

$$M = |S_{11}|^2 = a^2 + b^2 \tag{3.7}$$

The Q of a measured capacitor, in terms of M is:

$$Q = \frac{2\ \mathrm{Im}\,(\mathrm{S}_{11})}{1 - M} = \frac{2b}{1 - M} \tag{3.8}$$

where

$$\begin{aligned} S_{11} = a + jb &= \frac{Z_c - Z_p}{Z_c + Z_p} = \frac{(R_s - Z_p) + jX}{(R_s + Z_p) + jX} \\ &= \frac{(R_s - Z_p) + jX}{(R_s + Z_p) + jX} \cdot \frac{(R_s + Z_p) - jX}{(R_s + Z_p) - jX} \end{aligned} \tag{3.9}$$

$$b = \frac{2XZ_p}{(R_s + Z_p)^2 + X^2} \tag{3.10}$$

The maximum capacitance is the down-state loading capacitance assuming that the MEMS switching ratio is very high. The down-state capacitance, C_{Ld}, defined in Equation 2.43, is dependent on the unloaded impedance, Z_o, the down-state loaded impedance, Z_d, and the Bragg frequency, f_B. From this loading capacitance, the minimum reactance is determined to be $|X| = 1/(\omega C_{Ld})$.

All which remains is to calculate R_s such that it satisfies the limit M placed on the magnitude of the reflection coefficient and the maximum capacitance (minimum reactance),

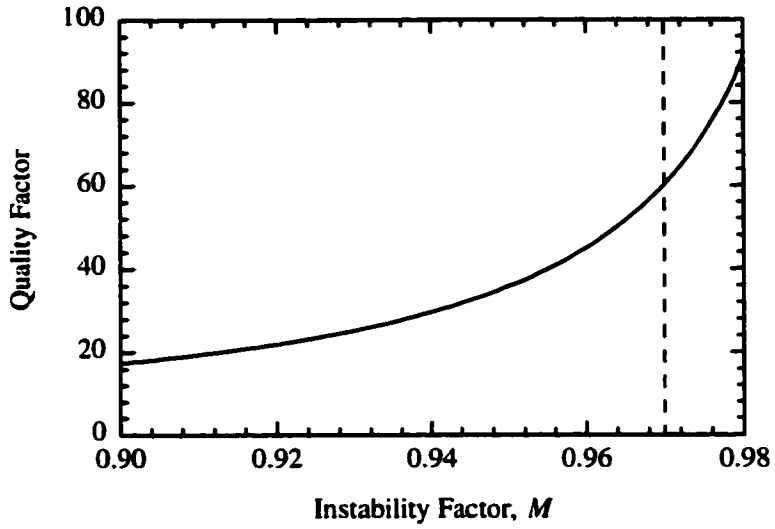


Figure 3.2: Maximum measurable Q of DMTL phase shifter capacitors vs. the instability factor M for the reflection coefficient type measurement.

using Equations 3.1, 3.9, and 3.10.

$$R_s = \frac{Z_p(1+M) - \sqrt{4MZ_p^2 - |X|^2(M-1)^2}}{1-M} \tag{3.11}$$

This analysis condenses down into one clear graph. Figure 3.2 shows a plot of measurable Q versus the instability factor M assuming an unloaded impedance $Z_o = 100\ \Omega$, port impedance $Z_p = 50\ \Omega$, down-state loaded impedance $Z_{Ld} = 41.8\ \Omega$, design frequency $f_o = 10$ GHz, and Bragg frequency $f_B = 3f_o$. It is seen that the calculation of Q from measured results becomes quite unstable at $M = 0.97$, which corresponds to a maximum Q of 60. The term "unstable" is defined loosely here. For $M = |S_{11}|^2 = 0.97$, a change of ± 0.01 in M will result in a Q change of 68 ± 25. Therefore, any result obtained higher than 60 using this technique should not be considered valid. Since much higher Q values are required for a distributed phase shifter, the reflection coefficient technique is not used to test the Q value of MIM or MAM capacitors.

Figure 3.3: Typical test structure used in conjunction with the distributed technique.

3.3 Distributed Structure Technique

The distributed structure technique is much better suited for measuring high-Q values because instead of measuring the complex impedance of a single set of capacitors, the technique measures the total effect of several sets of capacitors. A typical test structure consists of 8 or more MEMS sections, as shown in Figure 3.3. The design of this structure, including the length of each unit cell, impedances, etc., is exactly that of a typical DMTL phase shifter. For a quartz substrate design, $Z_o \sim 100\ \Omega$, $Z_d \sim 42\ \Omega$, and $f_B \sim 2\text{-}3f_o$. In practice, a high Bragg frequency is desired since more capacitors per unit length are used which minimizes the t-line loss influence on the measurement. MEMS switches are not used in the structure and the entire CPW line is plated to reduce the effect of transmission line loss.

There are two components of insertion loss through the test structure 1) t-line conductor loss and 2) capacitor Q loss, described in Section 2.12, and is:

$$\alpha \simeq 8.686N\left[\frac{R_t}{2Z_d} + \frac{Z_d\omega C_{Ld}}{2Q}\right] \quad \text{dB} \tag{3.12}$$

where N is the number of unit cells, R_t represents conductor loss of the unloaded t-line, and Z_d is the loaded impedance (corresponding to C_{Ld}).

A circuit simulator such as ADS with an optimization test bench is the easiest and most accurate way to extract Q from a distributed test structure since Equation 3.12 is only an approximation and does not account for the effect of Bragg frequency. Measured

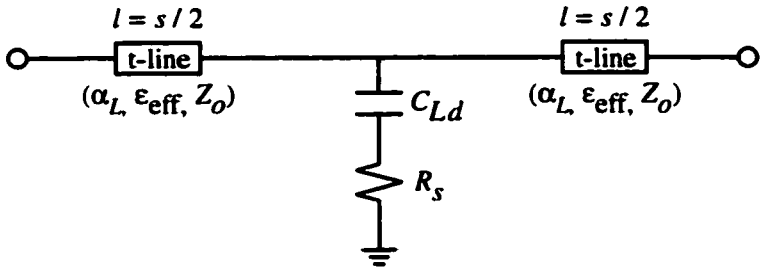


Figure 3.4: Circuit simulator model for a single unit cell used in conjunction with the distributed technique for measuring Q.

S-parameters are matched to a loaded t-line model such as the one shown in Figure 3.4 for a single unit cell. The characteristics of the unloaded t-line, such as Z_o, ϵ_{eff}, and α_L are determined either from equations (as described in Section 2.11) or from separate test structures which do not contain capacitors in the gaps. Loading capacitance C_{Ld} and series resistance R_s are obtained by matching transmission phase and transmission loss, respectively, to the measured results and finally, the capacitor Q is determined from $Q = 1/(\omega R_s C_{Ld})$.

3.3.1 Capacitor Q Measurements

Figure 3.5 shows a cross sectional drawing of the MIM capacitor structure which was measured using the distributed technique. It consists of two MIM capacitors in series and it is fabricated by first evaporating a base metal which forms the bottom metallization of the MIM, over which a 2,000 Å thick dielectric layer is deposited. Next, a sacrificial layer is placed over the dielectric and two square holes are etched into it using a plasma RIE etch. These holes (30×30 μm^2) provide the contact areas required for the MIM capacitors. Next, metal is sputtered into the holes and portions are electroplated with gold to more than 3 μm thick. Finally, the sacrificial layer is removed. The MAM capacitor, as shown in Figure 3.6 is fabricated in a very similar manner except there is no dielectric and the separation between the 125×125 μm^2 capacitor plates is 1.5 μm.

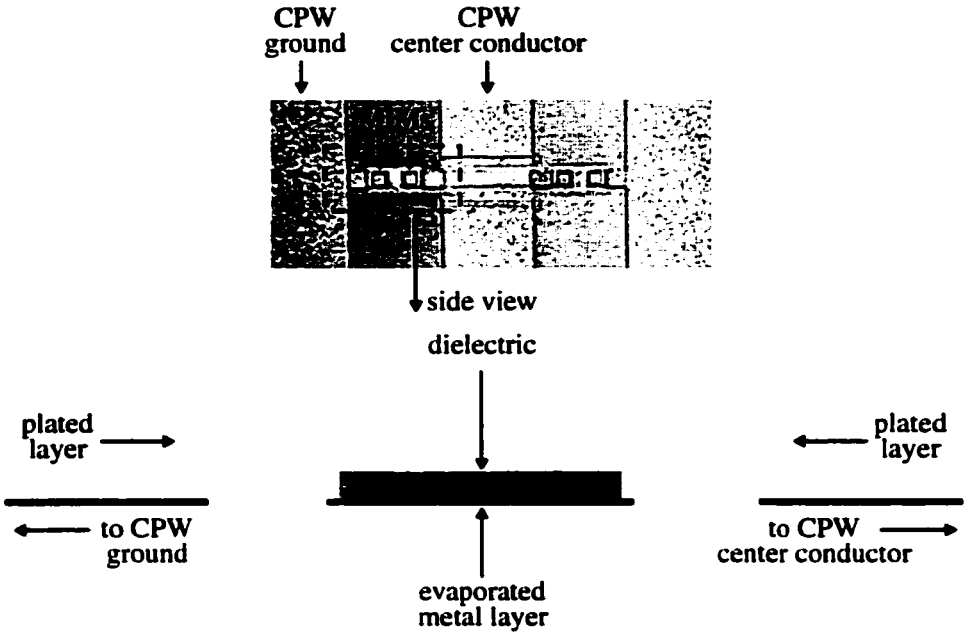


Figure 3.5: Photograph and cross sectional drawing of the electroplated MIM capacitor measured at X-band.

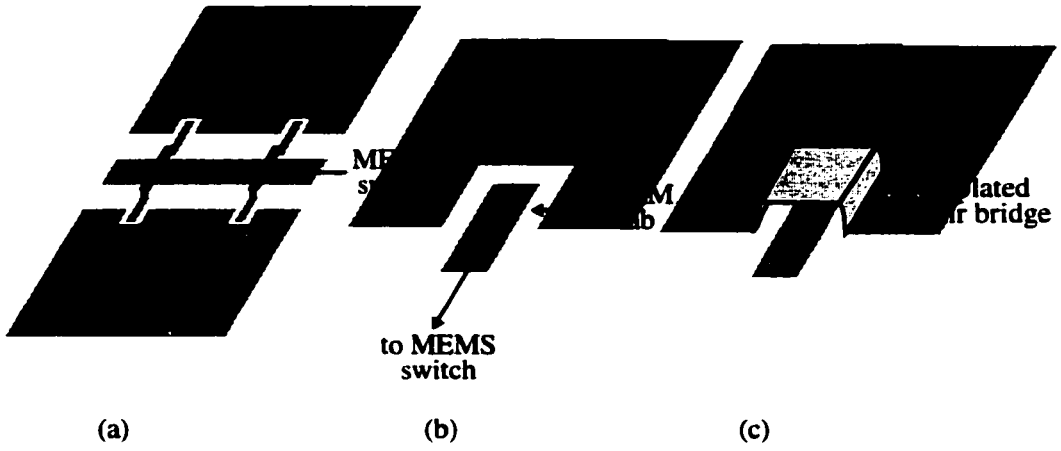


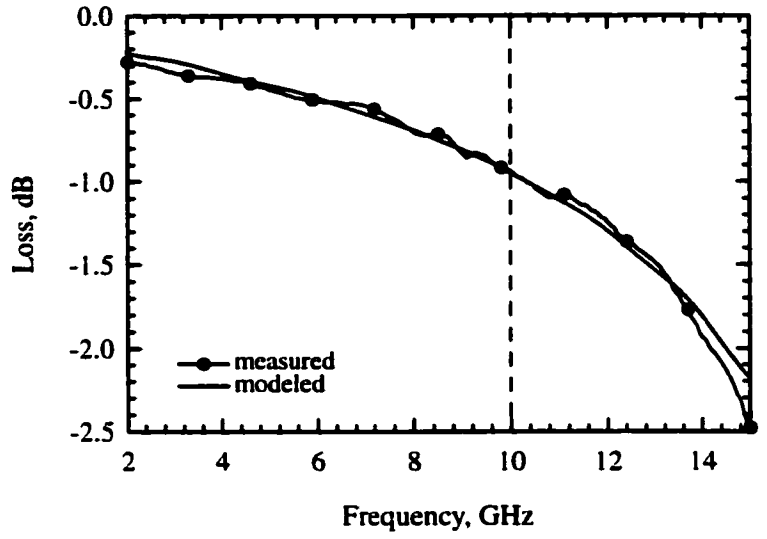
Figure 3.6: Drawing of the MAM capacitor (a) and detail drawings before (b) and after (c) electroplating gold, thus forming the MAM capacitor under the air bridge.

Measurement vs. model of the X-band MIM distributed test structure, which consists of 12 sections, each 1,130 μm long is contained in Figure 3.7. The unloaded t-line is fabricated on a 500 μm thick quartz wafer ($W = 300$, $G = 300$ μm) which has the following characteristics at 10 GHz: $Z_o = 98\ \Omega$, $\epsilon_{eff} = 2.34$, and $\alpha = 10$ dB/m. A short length of t-line in the middle of each section (150 μm) is taken to have a slightly higher loss ($\alpha = 17$ dB/m) because it is not electroplated. The capacitance value extracted from this model shows $C_{Ld} = 407$ fF with a corresponding $R_s = 0.29\ \Omega$ and Q of 135 at 10 GHz, which is a fairly good Q for a DMTL phase shifter, but a much higher value can be obtained with MAM capacitors. For better clarity, the ripple in the insertion loss (S_{21}) due to return loss (S_{11}) is removed from measured data in Figures 3.7-3.9 according to:

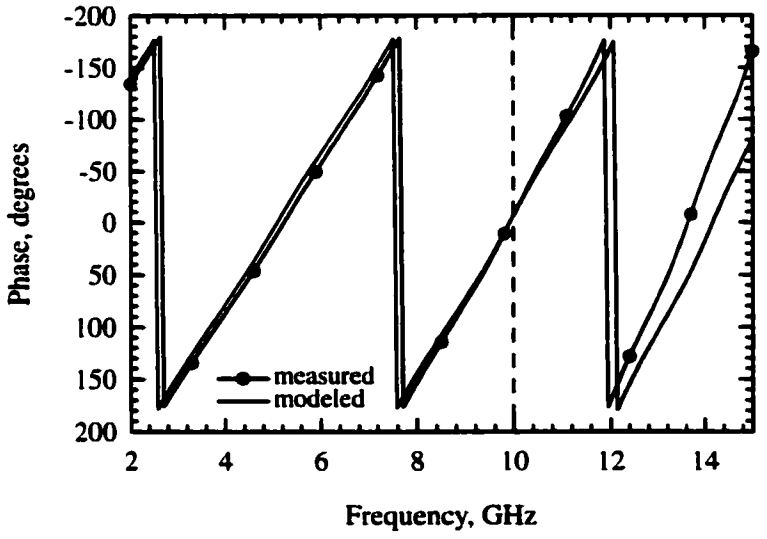
$$\text{Loss} = 10\log|S_{21}|^2 - 10\log\left[1 - |S_{11}|^2\right] \quad \text{dB} \tag{3.13}$$

Measurement and model of the X-band MAM capacitor is shown in Figure 3.8. Once again, the test structure is based on a CPW line with the same dimensions and characteristics, except that it is slightly longer (s = 1,130 μm) and has 14 sections. A short length of t-line in the middle of each section (240 μm) is taken to have a slightly higher loss ($\alpha = 17$ dB/m) because it is not electroplated. The capacitance value extracted from this model shows $C_{Ld} = 250$ fF with a corresponding $R_s = 0.13\ \Omega$ and Q of 500 at 10 GHz. This Q is so high that it is arguable the limit of measurement accuracy for Q is reached using 14 sections. To accurately measure higher Q values, more sections should be used. But ultimately, for DMTL phase shifter work, a Q anywhere in this range is all that is required, and more exact measurements would not be significant.

Measurement vs. model of the K-band MIM distributed test structure, which consists of 14 sections, each 400 μm long is contained in Figure 3.9. The unloaded t-line is fabricated on a 500 μm thick quartz wafer ($W = 150$, $G = 150$ μm) which has the following characteristics at 30 GHz: $Z_o = 98\ \Omega$, $\epsilon_{eff} = 2.38$, and $\alpha = 35.6$ dB/m. A length of t-line in the middle of each section (150 μm) is taken to have a slightly higher loss ($\alpha = 42.1$ dB/m). The capacitance value extracted from this model shows $C_{Ld} = 75$ fF with a corresponding $R_s = 0.18\ \Omega$ and Q of 400 at 30 GHz, which is shows the MAM capacitor has excellent low-loss characteristics at K-band and above.

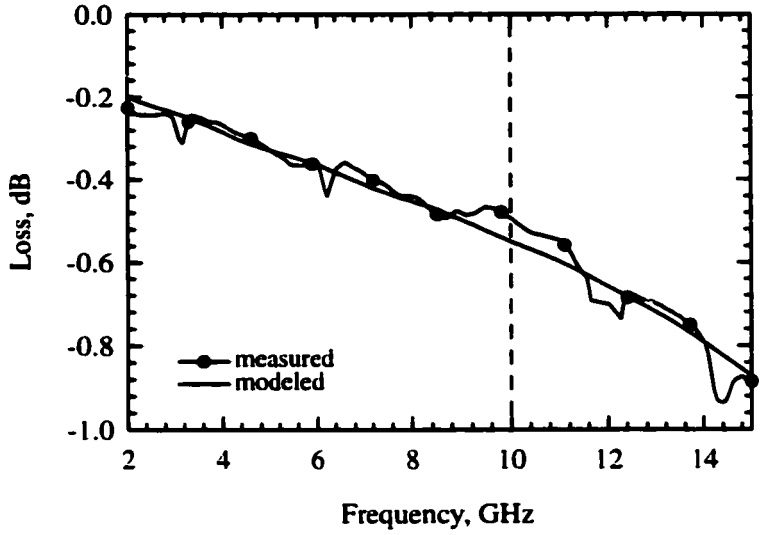


(a)

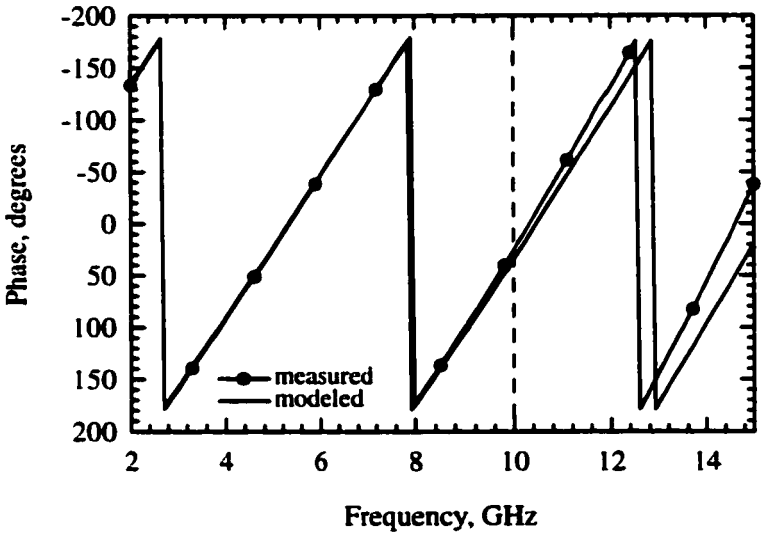


(b)

Figure 3.7: Measurement vs. simulation of a 12 section X-band test structure containing MIM capacitors. Modeled values for C_{Ld} = 407 fF and Q = 135 at 10 GHz.

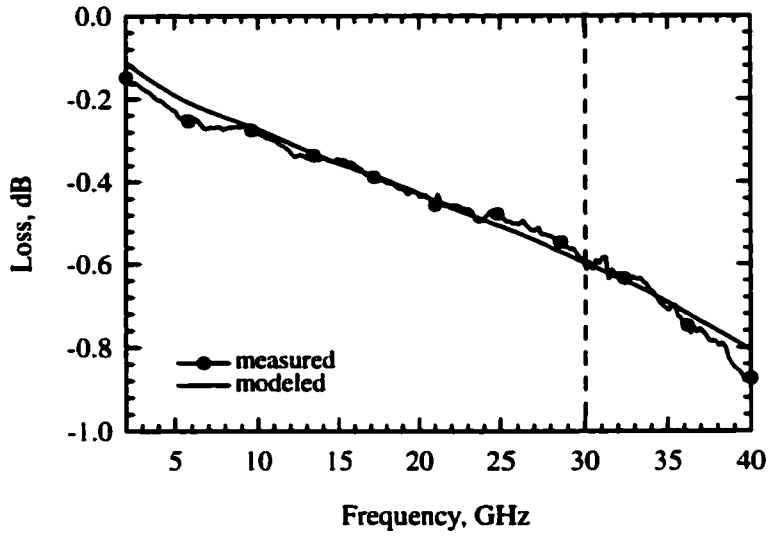


(a)

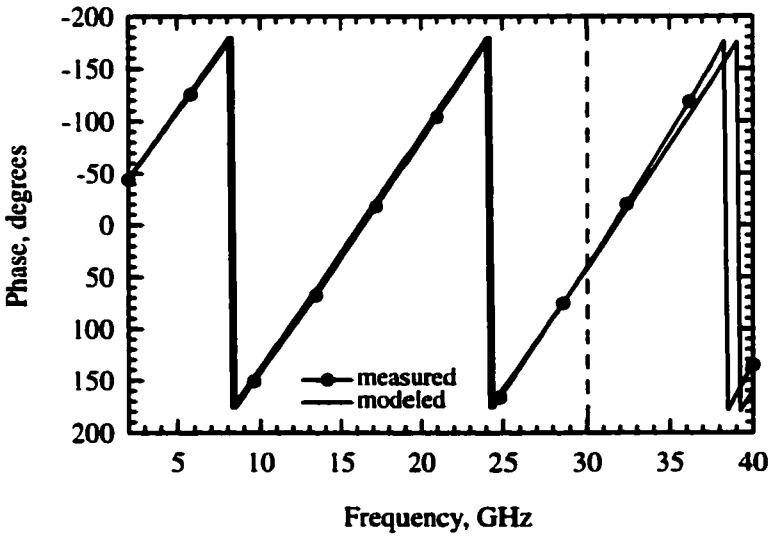


(b)

Figure 3.8: Measurement vs. simulation of a 14 section X-band test structure containing MAM capacitors. Modeled values for C_{Ld} = 250 fF and $Q = 500$ at 10 GHz.



(a)



(b)

Figure 3.9: Measurement vs. simulation of a 14 section K-band test structure containing MAM capacitors. Modeled values for C_{Ld} = 75 fF and $Q = 400$ at 30 GHz.

	change $1.10\alpha_L$	change $1.05\alpha_L$	nominal value	change $0.95\alpha_L$	change $0.90\alpha_L$
X-band MIM	+17	+8	135	−6	−14
X-band MAM	+523	+172	500	−102	−170
K-band MAM	+343	+120	400	−75	−127

Table 3.1: Effect of ±10% inaccuracy in the unloaded line loss on the error of the extracted Q using the distributed technique (14 sections).

	change $1.10C_{Ld}$	change $1.05C_{Ld}$	nominal value	change $0.95C_{Ld}$	change $0.90C_{Ld}$
X-band MIM	+29	+13	135	−11	−24
X-band MAM	+248	+106	500	−81	−145
K-band MAM	+167	+73	400	−58	−104

Table 3.2: Effect of ±10% inaccuracy in the loading capacitance on the error of the extracted Q using the distributed technique (14 sections).

3.3.2 Measurement Error

The distributed technique is based on two assumptions: 1) that the characteristics of the unloaded line (α_L, Z_o, ϵ_{eff}) are well known using separate test structures, and 2) the loading capacitance C_{Ld} is correctly extracted from the measured data by matching the phases of the measured DMTL and fitted model. The effect of changing the modeled parameters for unloaded line loss and loading capacitance by ±10% is shown in Tables 3.1 and 3.2, respectively. The tables demonstrate that lower Q measurements ($Q < 200$) are accurate to within about ±10%. However, high-Q measurements are accurate to within about 30% on the negative side only. The positive side is ignored because Q measurements above 500 are difficult to extract with a low number of distributed sections.

CHAPTER 4

X-BAND CPW DMTL PHASE SHIFTERS

4.1 Introduction

The X-band wideband DMTL phase shifters are presented in this chapter. All of the designs are built on a quartz substrate using a CPW topology. Contained here is the progression of designs, starting from the initial one-bit design and ending with a two-bit design which, at the time of writing, is one of the most competitive distributed MEMS phase shifters at this frequency band. The improvement of these designs is due primarily to two factors: 1) advances in MEMS switch fabrication, which lead to more reliable and predictable on/off switch states, and 2) static capacitor Q loss reduction, which leads to a lower loss phase shifter.

4.2 Prior Work

The distributed phase shifter consists of a high impedance line ($> 50\ \Omega$) capacitively loaded by the periodic placement of discrete varactors [42]. By applying a single bias voltage on the line, the distributed capacitance can be changed, which in turn changes the phase velocity of the line and creates a true-time delay phase shift. This technique has been recently optimized by Nagra et al. with Schottky diode varactors [33],[34], and have shown good performance with 86°/dB insertion loss at 20 GHz. However, the millimeter wave performance of these devices is limited by the series resistance of the diodes which is typically 2-5 Ω. This problem was solved by Barker et al. [3],[4] with the use of suspended MEMS

varactors over a CPW line. The MEMS varactors have a series resistance of 0.15 Ω and result in excellent performance at mm-wave frequencies with 90°/dB and 72°/dB insertion loss at 60 GHz and 90 GHz, respectively.

In Barker's "analog" design, the performance of the DMTL was limited by the MEMS capacitance ratio of 1.2. Mechanical instability of the MEMS switch under a constant DC bias voltage limits the theoretical usable capacitance ratio of 1.5 and a practical limit of 1.2-1.3 [3]. A further limitation of the designs by Nagra and Barker is based on an analog bias voltage which will produce phase noise at the output of the device due to electrical noise on the bias line.

The purpose of work contained here is twofold: First, to turn the distributed MEMS phase shifter into a "digital" design which is not sensitive to electrical noise, and second, to develop a distributed MEMS phase shifter which has a large capacitance ratio (1.5-2.5) resulting in a large phase shift with minimal insertion loss.

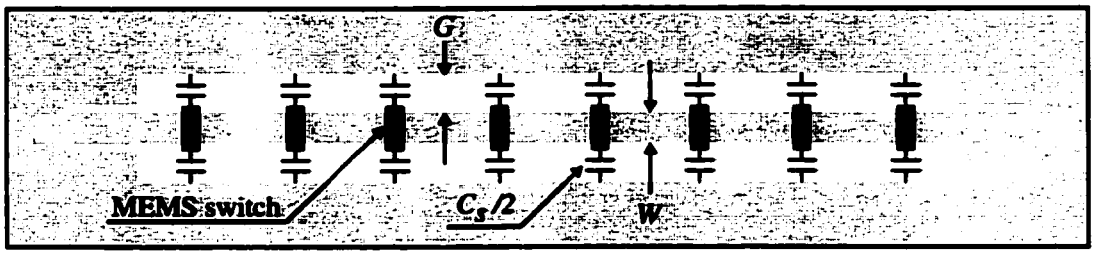
4.3 Initial Design: One-bit MIM CPW

4.3.1 Design and Fabrication

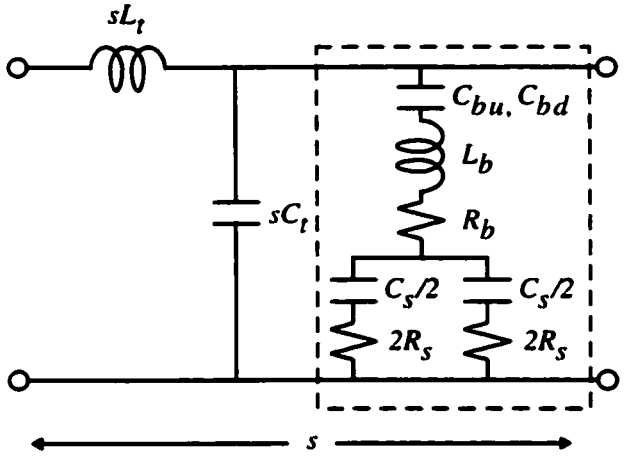
The first generation one-bit DMTL phase shifter is fabricated on a 500 μm thick quartz ($\epsilon_r = 3.6$) substrate. Figure 4.1 shows the "digital" distributed design together with the equivalent circuit model of a single period, s. As represented in the lumped model, the design is composed of an unloaded line periodically loaded with MEMS switches in series with lumped element capacitors (the portion within the box in the figure). The total load capacitance seen by the line is the series combination of the switch capacitance (C_b) and the total lumped capacitance (C_s) and is:

$$C_L = C_s C_b / (C_b + C_s) \tag{4.1}$$

Designed for 10 GHz operation and composed of a 900 μm wide ($W + 2G$) CPW line with 284 μm center (G) conductor, the CPW line is wide for reduced ohmic loss and has an unloaded impedance of $Z_o = 100$ Ω. The DMTL is composed of 17 MEMS switches at



(a)



(b)

Figure 4.1: First generation, one-bit CPW phase shifter with MEMS switches and MIM capacitors (a) and distributed lumped model for one unit cell of the DMTL (b).

a spacing of 884 μm for approximately 169° of phase shift at 10 GHz when loading on the transmission line in the up and down-state positions is C_{Lu} = 81 fF and C_{Ld} = 190 fF, respectively (C_{Ld}/C_{Lu} = 2.35). Using Equation 2.46 and ϵ_{eff} = 2.39, the equivalent loaded impedances are Z_u = 60 Ω and Z_d = 44 Ω. Assuming the down-state MEMS switch capacitance is 20 times that of the up-state position, design values for the static capacitance C_s = 204 fF, and the up-state MEMS switch capacitance C_{bu} = 134 fF.

The MEMS switch membranes are 350 μm long, 60 μm wide, and suspended at a height of 1.5 μm above the nitride layer covering the CPW center conductor underneath it. A 2,500 Å thick nitride layer is used as the insulating dielectric between the 6,000 Å thick CPW center conductor and the MEMS switch bottom, preventing high resistance DC-switching as well as preventing the switch membrane from sticking in the down-state position. This nitride layer is also used in the fabrication of the MIM (Metal-Insulator-Metal) static capacitor. The CPW center conductor and ground plane are electroplated to > 1 μm high except underneath the MEMS switch for reduced transmission line loss.

The fabrication process is shown in Figure 4.2. Unloaded CPW line metal is first defined by evaporating a 500/5,000 Å thick layer of Ti/Au (Fig. 4.2a) using a liftoff process in which photoresist protects areas of the substrate where metallization is not desired and a thin titanium layer is used to promote adhesion of the gold layer to the substrate. Metal is blanket evaporated onto the wafer and undesired metal is "lifted off" the wafer when the protective photoresist is dissolved in a solvent. Next, a 2,500 Å thick Si_3N_4 silicon nitride PECVD layer is grown on top of the metal and substrate at 400 °C. Photoresist patterns the silicon nitride and it is etched in a RIE plasma (Fig. 4.2b). Once this masking layer is removed in solvent, a sacrificial photoresist layer is spun to 1.5 μm thick and patterned (Fig. 4.2c) over which, the MEMS switch layer will be formed. The MEMS switch layer, consists of two parts: 500/1,000/500 Å thick layers of Ti/Au/Ti, evaporated onto the wafer to act as a seed layer for electroplating, and a 8,000 Å thick layer of electroplated gold. The CPW ground plane and center conductor are also electroplated in this step to reduce line loss (Fig. 4.2d). Excess seed layer metal (any metal in the gaps) is removed using a wet etch. The MEMS switch is released by removing the sacrificial layer in a solvent such as acetone. Finally, the wafer is dried in a critical point CO_2 dryer, which prevents

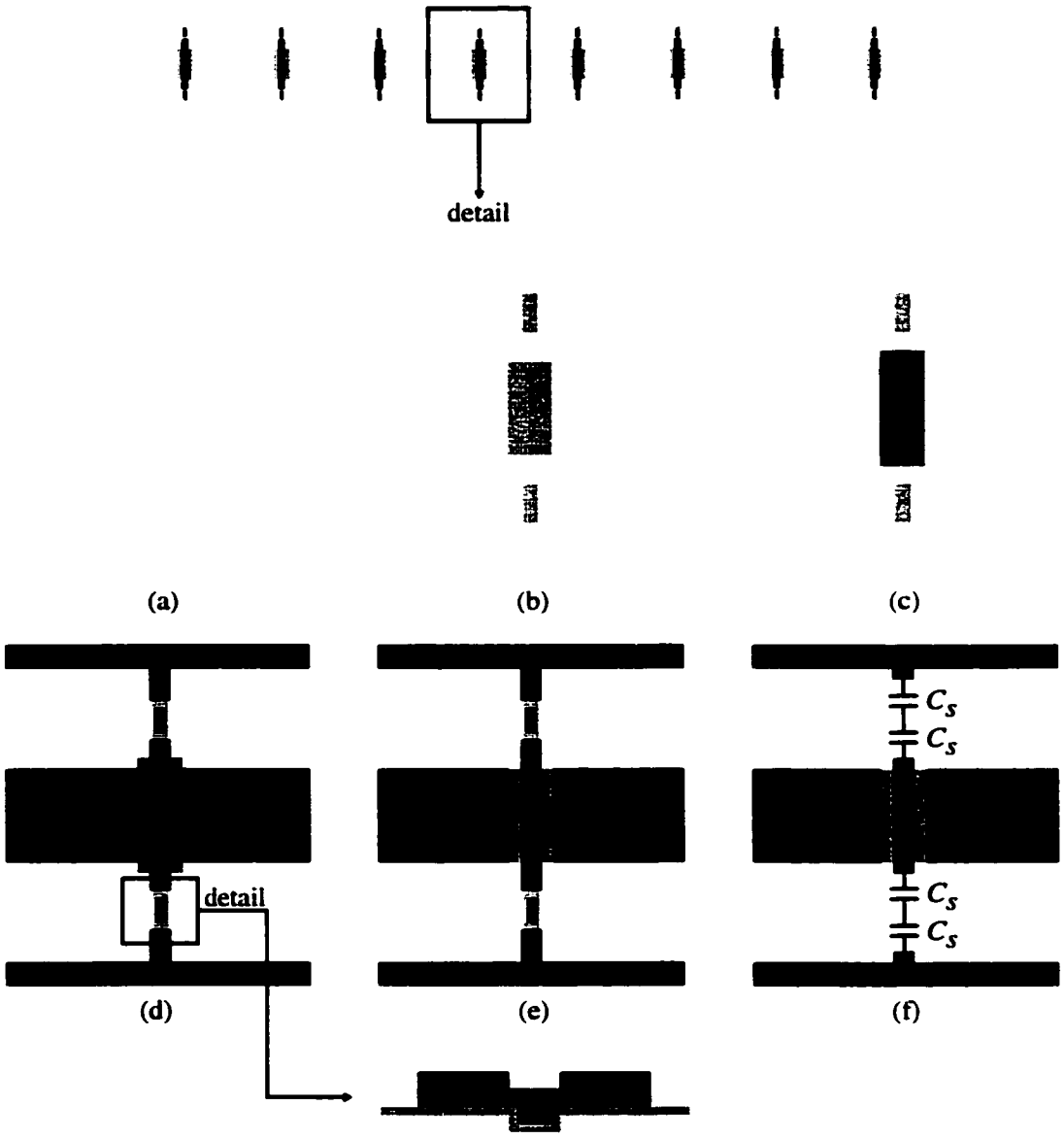


Figure 4.2: Fabrication detail drawing of the first generation DMTL phase shifter. After liftoff (a), after nitride patterning (b), after sacrificial layer patterning (c), after plating (d), after sacrificial layer removal (e), and lumped equivalent of MIM capacitors (f).

liquid surface tension from permanently pulling down the MEMS switches during drying (Fig. 4.2e).

Along with the MEMS switch membrane, the top metal of the MIM capacitor is formed in the electroplating step. The total static loading capacitance consists of 4 capacitors as seen in Figure 4.2e, where each of the 4 capacitors has a contact area of 41 $\times$ 35 μm^2, and given a 2,500 Å thick layer of Si_3N_4 ($\epsilon_r = 7.5$), the total static loading capacitance is approximately 381 fF. For this initial design, the static capacitance is built much larger than designed (204 fF) because at this early stage of fabrication, the MEMS switch height could not be well controlled. Often, the switch membranes had to be plated thick so that they were relatively flat to result in a consistent up-state capacitance. As a result of making these membranes thick, the switch membrane becomes too stiff to conformally pull down to the conductor beneath it and therefore the capacitance switching ratio is not high when the membranes are electrostatically actuated. Thus, the MIM capacitance is made larger to compensate for the low change in MEMS switching capacitance.

Use of plated metal for the MIM capacitor fabrication is also less than ideal. MIM capacitor test structures measured to be 465, 327, 429, and 184 fF. The average, 351 fF, has a great deal of variability. This variability is partially due to using an electroplated MIM top layer. The edges of the top MIM metallization grow beyond the masking layer, and stress in the plated layer causes the edges of the MIM to pull up off the dielectric, which is further aided by undercutting the seed layer in the wet etch step. In addition to the plating step, it is believed the nitride deposition step itself is counterproductive to good capacitor fabrication. This high temperature step (400 °C) creates bumps in the gold layer underneath the nitride, thus creating a random separation between the MIM metal layers. The yield of construction for the MIM capacitors is quite poor and its improvement is addressed in the next design.

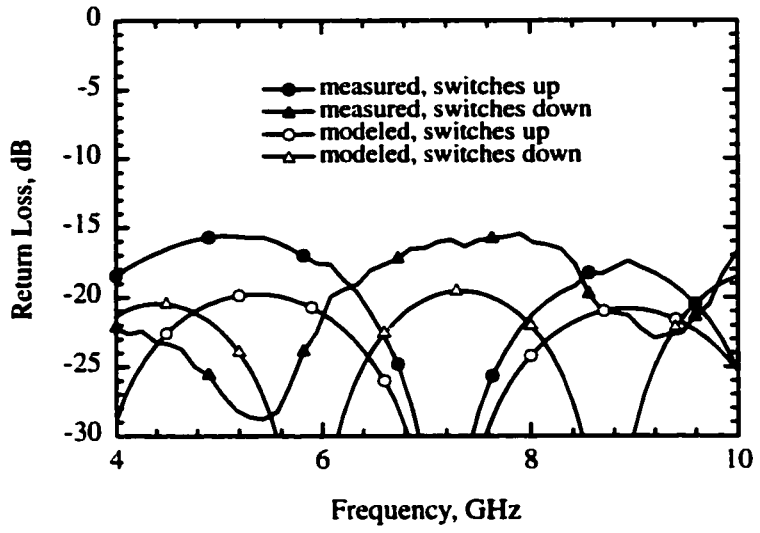
The pull-down voltage of these MEMS switches is 40 V. This is larger than usual (15-20 V) due to the series division of the applied voltage between the MEMS switch and the static MIM capacitance, C_s.

4.3.2 Measurement

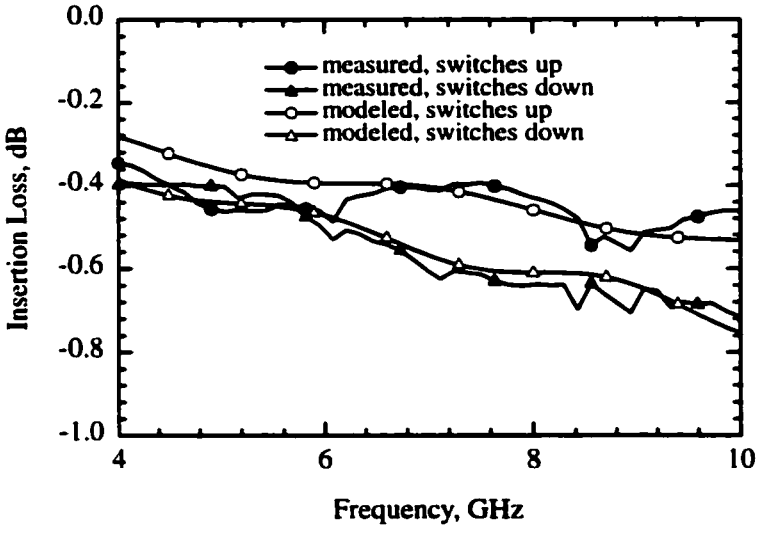
The simulated and measured performance of the DMTL phase shifter is shown in Figures 4.3 and 4.4. Average loading on the high impedance transmission line is found using measurement data by matching a loaded transmission line model to the measured phase in the up and down-state positions. The simulated results are obtained from ADS [1] using a model consisting of an ideal TEM lossy transmission line periodically loaded by the MEMS switch capacitance along with a series inductance of 20 pH (which does not have an effect at X-band) as shown in Figure 4.1. Using this technique, $C_{Lu} = 100$ fF and $C_{Ld} = 174$ fF. Assuming the average static loading $C_s = 351$ fF, then the MEMS switch capacitance in the up and down-state positions is 140 and 345 fF, respectively ($Z_u = 56$ and $Z_d = 45.5\ \Omega$). The expected up-state capacitance of the MEMS switch is 134 fF, calculated using a 3-D electrostatic simulator [30], thus, the average up-state MEMS capacitance is quite close to design.

The simulation model also consists of two lossy capacitors, $C_s/2$, (see Fig. 4.1) connected in series between the switch capacitance (C_b) and ground. Fitting the measured insertion loss to this lossy model, it is determined the combined Q of the MEMS switch and MIM capacitors is ~ 125 at 10 GHz. The Q is constant at 4-10 GHz and the series resistance R_s follows Equation 2.70.

The DMTL phase shifter results (Figure 4.3) in excellent return loss from 4-10 GHz (< -15 dB) in both the up-state and down-state positions. It is seen that the measured data agrees quite well with the simulations. The measured phase shift (Figure 4.4) at 8-10 GHz is 95-123° with an insertion loss of 0.62-0.66 dB. This results in a 153-186°/dB of insertion loss at 8-10 GHz, and is excellent for wideband cascadable phase shifters. As usual of distributed phase shifters, the performance is best in the upper frequency range since the loss increases as $\sqrt{f}$ while the phase shift increases as f. The measured performance is comparable to state-of-the-art X-band MEMS phase shifters based on Lange couplers and resulting in a performance of 240°/dB [28].



(a)



(b)

Figure 4.3: Measured and modeled return loss (a) and insertion loss (b) of the first generation, one-bit MEMS phase shifter.

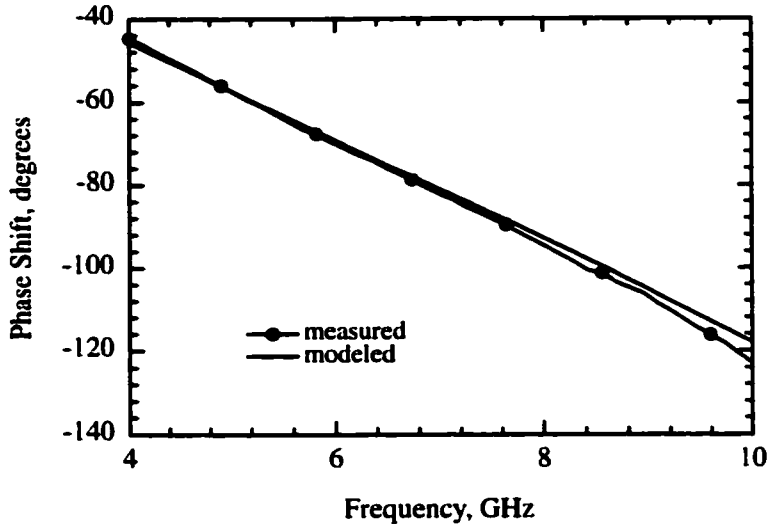


Figure 4.4: Measured and modeled phase response of the first generation, one-bit MEMS phase shifter.

4.3.3 Conclusion and Future Improvement

This first generation one-bit design of a distributed phase shifter is a novel topology for a "digital" MEMS design, and is relatively insensitive to the MEMS switch capacitance ratio, as is desired in "digital" designs, but there is room for improvement. One easy improvement addressed in the next generation design involves cascading two sections, separated by a large DC bias-isolating capacitor, to result in a 2-bit phase shifter. But, the most important changes include improvement of the fabrication process for the MEMS switch, and secondhand, improvement of fabrication for the MIM static capacitor. It is clear from several attempts at building this design that electroplated thin membrane switches and MIM capacitors are not ideal because controlling stress and thickness is very hard to do for this processing step. The research from this point forward focuses on using a variety of sputtered layers to form the MEMS switch membrane in various ambient environments, as well as investigation for an optimal sacrificial layer which can be used in conjunction with high temperature annealing.

(a) (b)

Figure 4.5: Comparison of thin layer depositions of evaporated (a) and sputtered (b) material on a step height.

4.4 Next Generation Design: Two-bit MIM CPW

4.4.1 MEMS Switch Improvement

MEMS switches built in the original design are composed of an evaporated seed layer of Ti/Au/Ti and electroplated gold. The electroplating process is as follows: a wafer is immersed in an arsenic or cyanide solution containing gold and current is passed from anode to cathode where the anode is a platinum electrode and the circuit to be plated acts as the cathode. More current and more time in solution results in a thicker plating layer. The process is best suited for very thick gold layers ($> 2 \pm 0.5$ μm) and not for depositing layers within $\pm$1,000 Å. Stress is difficult to control because it dependent on the gold solution chemistry which changes after each use of the solution, plating area of the wafer, current, time, and temperature. The process has so many variables that it became immediately evident from the initial design that electroplated MEMS switches must be abandoned.

The second generation MEMS switches are fabricated using a sputtering process. Sputtering (Fig. 4.5b) is an ideal process for thin layers because unlike evaporation (Fig. 4.5a), the metal to be deposited is contained in a plasma, thus sputtered material is deposited onto edges as well as surfaces. Also, in a sputtering tool, several ambient environmental conditions can be controlled, including plasma gases, pressure, and in some cases temperature, all of which have an effect on the mechanical properties of the membrane deposited.

The first step in producing these new sputtered membranes is to qualify how these parameters effect stress. Before any suspended structures are fabricated, the conditions for

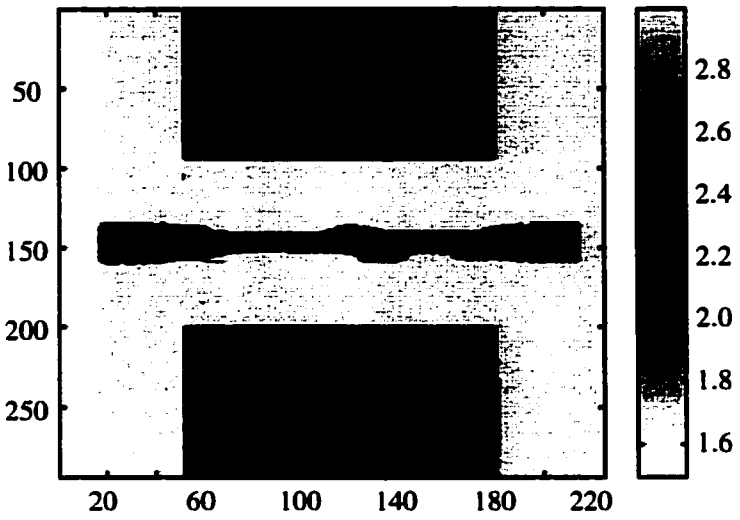


Figure 4.6: Light interferometer measurement of an early aluminum sputtered MEMS switch. Dimensions are in microns.

low stress are found by measuring the curvature of blank wafers before and after blanket depositions [21]. In this sputtering tool, aluminum membranes are slightly tensile and gold membranes are highly compressive using the normal N_2 deposition environment and pressure of 7 mT. The stress of the gold membrane turns from highly compressive to slightly tensile by increasing the sputtering pressure from 7 to 10 mT.

This period of research focused on perfecting the aluminum and gold MEMS switches concurrently, for it was not known if an aluminum or gold membrane would be possible. Aluminum showed the most promising early results (Fig. 4.6), but using it would greatly complicate the steps required for circuit fabrication for the following reasons: although aluminum is nearly as conductive as gold ($\sigma = 3.8 \times 10^7$ vs. 4.5×10^7 S/m), aluminum reacts with gold over a long period of time, forming a green-black film. Furthermore, introducing aluminum into a standard Au/Ti processing flow greatly complicates fabrication because aluminum is easily etched by hydrofluoric acid, which is used to etch titanium in the standard Au/Ti process flow. Another metal, such as tungsten (etched by H_2O_2), must be introduced to protect certain aluminum layers during processing. It might seem using only aluminum in the circuit may be a perfect solution, but it is not realistic for two reasons: first,

aluminum melts at a much lower temperature than gold (660 vs. 1065 °C) and when placed in the PECVD for Si_3N_4 deposition at 400 °C, forms bumps (the process of "hillocking") of more than ±500 Å on the surface. Second, it is not easy to plate aluminum layers, and thus loss of the unloaded line would be too high for a good X-band design. Both aluminum and gold MEMS switch fabrication processes were perfected concurrently, and in the end, both produced very flat MEMS switches.

The early gold membranes were anything but flat. Once released, it would not be unusual for the membrane to arch more than 6-10 μm over a 300 μm fixed-fixed suspended span. One of the approaches used to flatten the membrane was to anneal them prior to release. This technique had limited success with photoresist sacrificial layers because photoresist does not tolerate temperatures > 130 °C. SiO_2 sacrificial layers worked well, but were difficult to remove without destroying other structures on the wafer because the adhesion layer used on the wafer is titanium, which etches in the same chemicals as silicon dioxide. PMMA [37] proved to be the best sacrificial layer. It is spun on in layers and cured at 200 °C, which allows for a bit of reflow at step heights. It is easily defined by a metal mask, which acts as a protective layer during an oxygen plasma etch. Best of all, PMMA is removable in solvent.

The final process steps include using PMMA as the sacrificial layer, sputtering gold as slowly as possible in a 10 mT N_2 environment, reinforcing the anchors of the MEMS switch with the plated gold, and "annealing" the membrane at 170 °C prior to release. Minimizing the percentage of other metals (such as titanium, which would be used to promote adhesion) is also very important because even a small amount can greatly change the residual stress. A light interferometer measurement of the final gold switch membrane is in Figure 4.7. The membrane bows by only 2000 Å over a 300 μm length and curls by only 1000 Å over a 80 μm width. Interestingly enough, although gold switches are preferable because their use does not complicate the processing flow, aluminum switches were used in the next generation two-bit design because the gold sputter target was not available for several months.

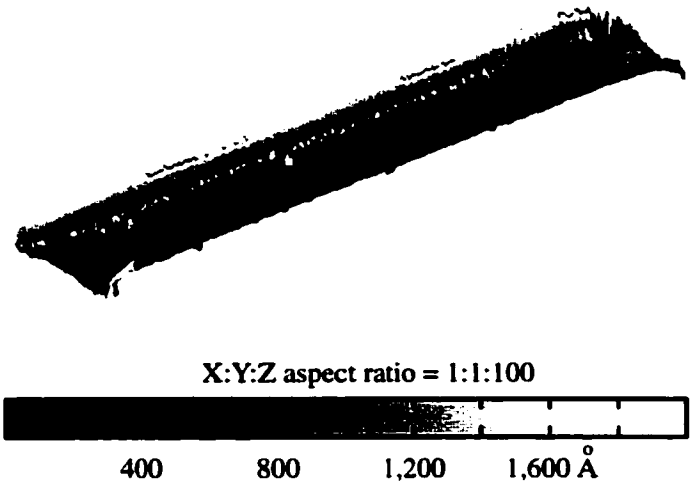


Figure 4.7: Light interferometer measurement of a gold MEMS switch. The Z scale is greatly expanded to emphasize membrane flatness.

4.4.2 MIM Capacitor Improvement

The largest challenges to good small value (< 250 fF) MIM capacitor fabrication is adhesion and surface flatness. In the original design, the small metal tab (the top layer drawn in the detail drawing of Fig. 4.2d) was undercut in the final processing steps, which effectively reduced the capacitor contact area. A solution to this problem is to simply protect the MIM with the MEMS switch sacrificial layer which is not removed until the final process step. But unfortunately, this step is not enough, as hillocking formed in the bottom MIM gold metallization during the nitride deposition later produces capacitors with a great deal of variability. Another solution is to use a much higher melting point metal, such as tungsten, which does not hillock in the PECVD. And to improve the MEMS switching ratio, tungsten is also used under the MEMS switch, as seen in Figure 4.8a. Test structures prove the approach works: MIM capacitance values of 214, 210, 217, and 218 fF are obtained. Unfortunately, analysis shows tungsten, with its high sheet resistance, is the source of high insertion loss in the measured circuit, as is discussed in detail in Section 4.4.4. It was later found that tungsten was not required to minimize hillocking, and simply keeping a thin layer of titanium on top of gold layers greatly reduces hillocking and probably produces the

same excellent MIM capacitors as can be fabricated with tungsten.

4.4.3 Design and Fabrication

Two-bit and one-bit (180°) DMTL phase shifters are fabricated on a 500 μm thick quartz substrate. They are designed for 11.3 GHz operation and are based on a 900 μm wide (W+2G) CPW line with 300 μm center (W) conductor. The CPW line is wide for reduced unloaded line loss and has an impedance of 98 Ω. The complete 2-bit (0°, 90°, 180°, and 270°) phase shifter is composed of 24 MEMS switches; the 90°-bit section has 8 switches and it is cascaded with the 16 switch 180°-bit section using a very large MIM capacitor in the CPW center conductor which isolates the bias voltage between the two sections. Each MEMS switch is separated by s = 906 μm, is 350 μm long, 60 μm wide, and is suspended at a height of 1.5 μm above the substrate. A 2,000 Å nitride layer is used as the insulating dielectric between the 1,500 Å thick tungsten CPW center conductor and the MEMS switch. To reduce transmission line loss, the CPW center conductor and ground plane are electroplated to 4.5 μm thick except underneath the MEMS switch.

The design values for loading capacitance are C_{Lu} = 83 fF (60 Ω) and C_{Ld} = 182 fF (44 Ω). Assuming the down-state MEMS switch capacitance is 10 times that of the up-state position, the design values for the static capacitance C_s = 210 fF, and the up-state MEMS switch capacitance C_{bu} = 138 fF. Using Equation 2.46, 16 sections result in 180° of phase shift at 11.3 GHz.

A remarkably flat MEMS switch was fabricated using a 6,000 Å thick aluminum metal suspended 1.5 μm above the insulating nitride. A light interferometer measurement of the released switch shows bowing over the long dimension (350 μm) of the switch membrane is less than 2,000 Å and curling over the narrow dimension (60 μm) is less than 1,000 Å. Fabrication yield of these switches with these height, curling, and bowing tolerances is 97-100 percent. The pull-down voltage of the MEMS switch alone is 13 V (extracted values: spring constant, k = 73 N/m, residual stress, σ = 72 MPa [5]), and around 60 V with the series MIM capacitor to ground. The MEMS switches pull down conformally with bias and snap back to their original height without deformation over numerous actuations, as can be

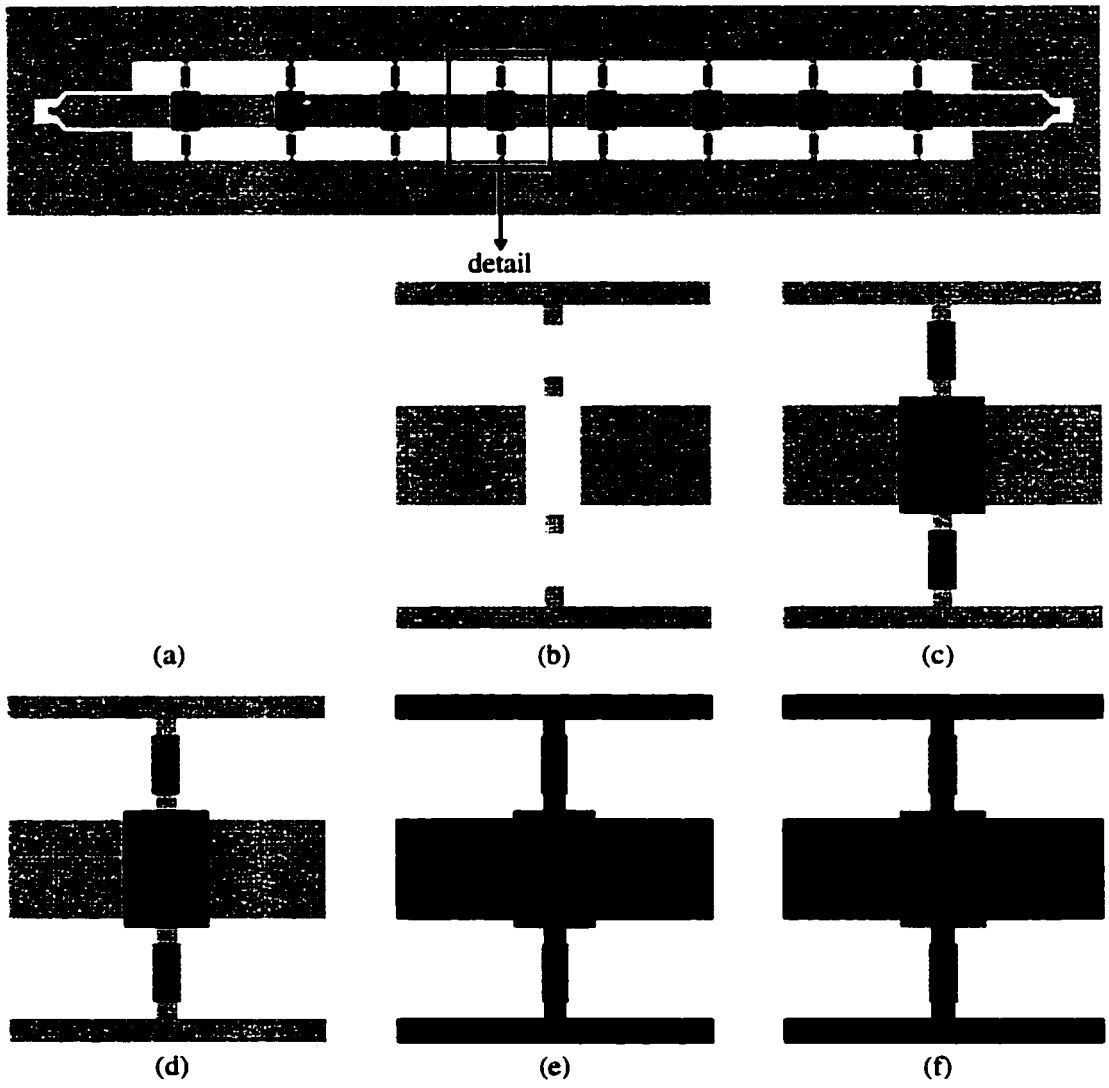


Figure 4.8: Fabrication detail drawing of the next generation phase shifter. After tungsten wet etch (a), after Ti/Au/Ti evaporation and liftoff (b), after Si_3N_4 patterning and MIM top metal liftoff (c), after PMMA sacrificial layer RIE etch (d), after MIM membrane aluminum sputter, etch and gold plating(e), and after sacrificial layer removal (f).

observed in phase measurements.

A summary of this wafer's particular fabrication flow is as follows: First, tungsten metal is blanket sputtered onto the quartz wafer. It is wet etched in H_2O_2 using a photoresist mask to leave metal underneath the MEMS switch and in the gaps where the MIM capacitors will be placed (Fig 4.8a). Next, the remainder of the CPW line Ti/Au/Ti metal layers are blanket evaporated onto the wafer and undesired metal is removed using the liftoff process described in Section 4.3.1 (Fig 4.8b). Following this step, Si_3N_4 is deposited and defined, also as described in Section 4.3.1. Once the nitride is defined, the top metal of the MIM is made using a liftoff process (Fig 4.8c), after which PMMA is spun onto the wafer and defined using an oxygen plasma to protect the MIM capacitors until the final steps, and of course, to remain underneath the MEMS switch (Fig 4.8d). An aluminum layer is sputtered (which will later be the MEMS switch), a Ti/Au/Ti seed layer is evaporated, and the circuit is electroplated with gold, after which the MEMS switch is defined by wet etching the aluminum layer (Fig 4.8e). The plated gold is used to reduce the unloaded line loss as well as to reinforce the point where the MEMS switch meets its post. Finally, the sacrificial layer is removed and the circuit is dried in a critical point CO_2 dryer (Fig. 4.8f).

4.4.4 Measurement

The two-bit phase shifter is biased through the left and right ports using bias T's and DC blocks to protect the VNA. For 0° of phase shift, the left and right ports are unbiased, for 90°, the left port is biased, for 180°, the right port is biased, and finally, for 270°, both ports are biased. To reduce charging of the nitride layer and to promote a maximum switching ratio, the bias voltage used is a low frequency (3 kHz) ±70V square wave.

The simulated and measured performance of the 180°-bit section is shown in Figures 4.9 and 4.10a. The phase shifter nearly meets the design criteria for return loss, which is < -14 dB over the 2-20 GHz band. The simulated and measured performance of the two-bit phase shifter is shown in Figures 4.11 and 4.10b. The phase shifter results in excellent return loss (< -11 dB) from 2-20 GHz for all four states. The measured phase shift of the 180°-bit section is 0 at 11.4 GHz and the two-bit phase shifter has states of 0°, 87°, 182°,

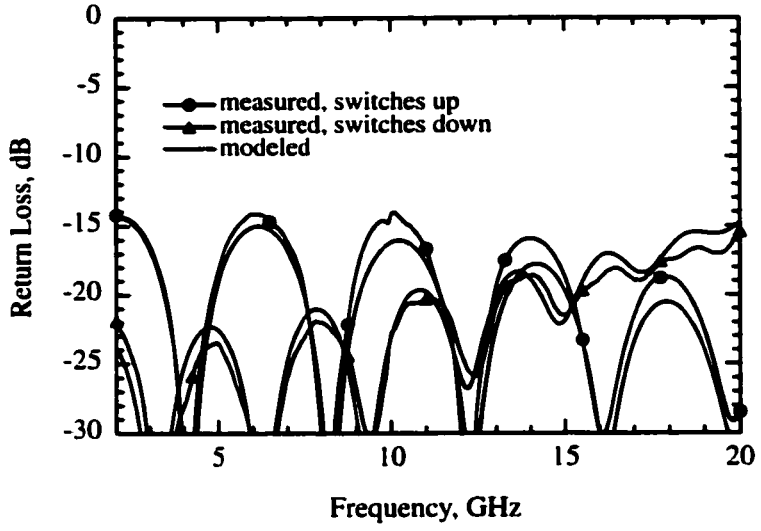
and 270° at 11.4 GHz (±3° error). Both simulations confirm the MEMS switch loading capacitance is exactly as designed in the up state (measured: C_{bu} = 140 fF vs. designed: 138 fF).

The non-linear phase response of Figure 4.10 for the 180°-bit and two-bit phase shifters clearly indicates the static MIM capacitors are frequency dependent since the effect of Bragg frequency alone does not account for this response. This degree of non-linearity as well as the very high insertion loss are quite unexpected, so the measured insertion loss and phase response of the 180°-bit phase shifter in the up and down-state positions were matched to an ADS [1] model (Fig. 4.12) at 2,4, ..., 20 GHz. A closed-form equation for C_{Ld}, R_s, and Q was fit using the ADS model (Fig. 4.13). The equations are used in conjunction with ADS to obtain the simulated results in Figures 4.9-4.11.

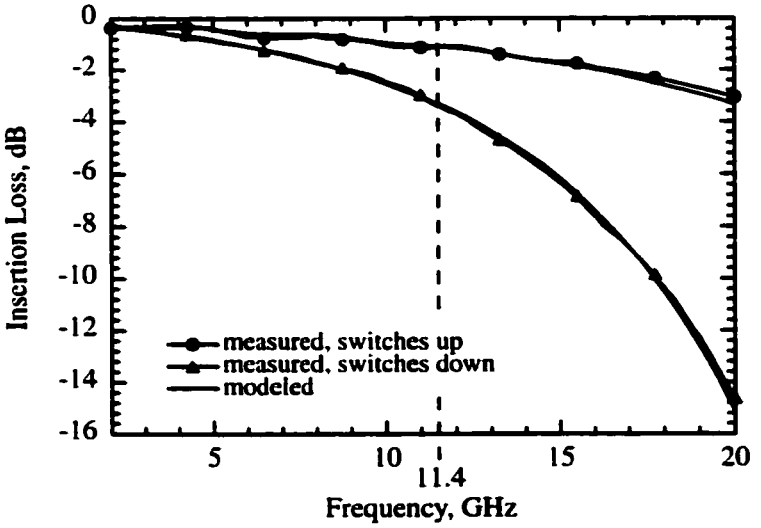
The non-linear capacitance of the MIM capacitor is most probably due to an increase in fringing capacitance between the two bottom metals of the MIM capacitors in each gap, as generally confirmed by a method of moments simulation. Q loss of the MIM capacitor, as measured by test structures and as confirmed by the fitted model is quite low, and since the metallizations are much less than a skin depth, R_s is nearly constant. Method of moments simulations show that although the metallizations used for the MIM capacitor are quite thin, that alone does not account for the high degree of loss. What does account for the loss is low conductivity metal, that is, a conductivity much lower than would be expected from the bulk properties of tungsten. But the tungsten target used in the sputtering machine is not composed of 100% tungsten. It is mixed with titanium (a very low conductivity metal) to promote adhesion. A method of moments simulation performed on the MIM capacitors using a conductivity close to titanium confirms the first metal placed on the wafer, the tungsten-titanium layer, which was used to reduce hillocking and improve variability from one capacitance value to another, is responsible for high insertion loss of the phase shifter.

4.4.5 Conclusion and Future Improvement

MIM losses dominate the insertion loss of these second generation phase shifters, and much better performance can be achieved by simply increasing the MIM Q, which can be

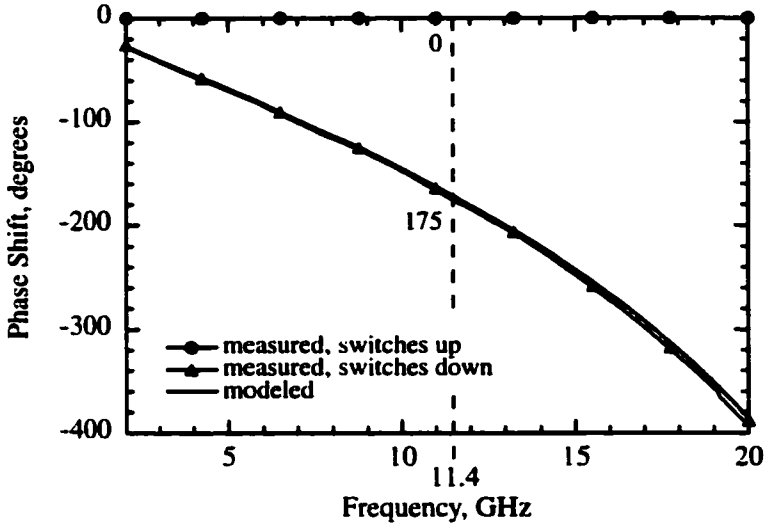


(a)

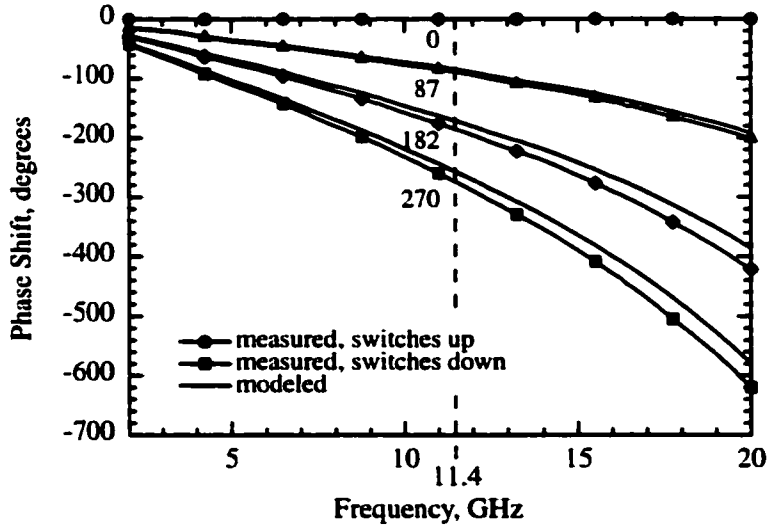


(b)

Figure 4.9: Return loss (a) and insertion loss (b) measurements of a second generation, single-bit phase shifter.

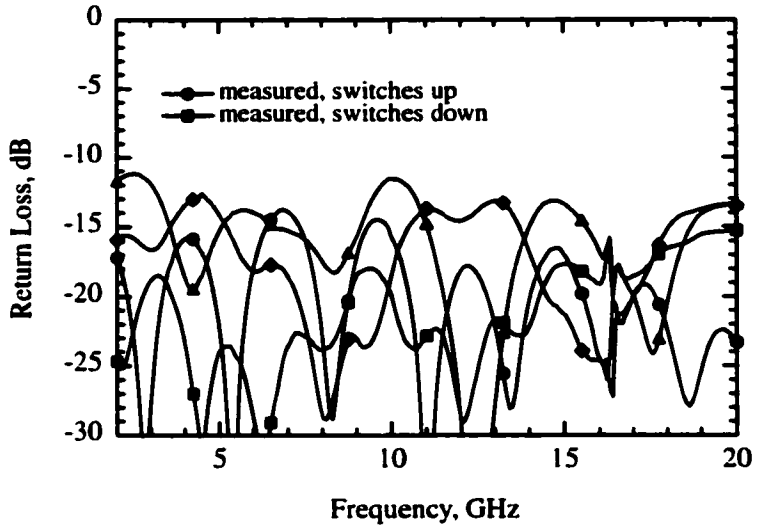


(a)

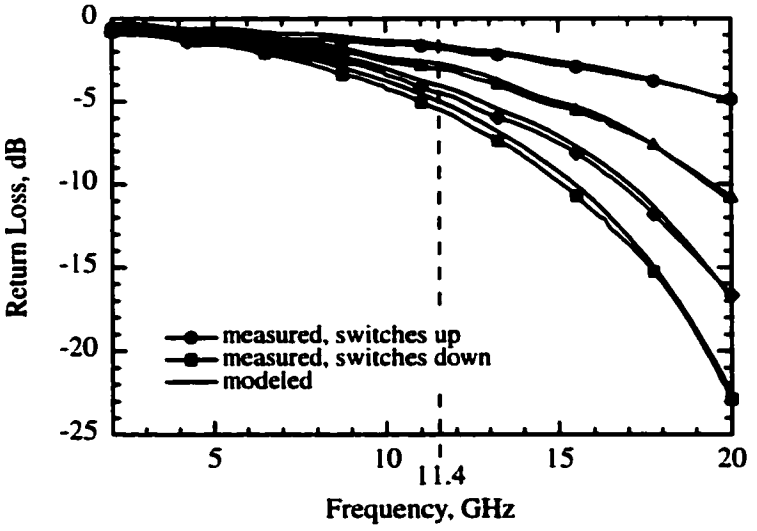


(b)

Figure 4.10: Phase response measurements of the second generation phase shifters. Results for the 180°-bit phase shifter (a) and two-bit phase shifter (b).



(a)



(b)

Figure 4.11: Return loss (a) and insertion loss (b) measurements of the second generation two-bit phase shifter.

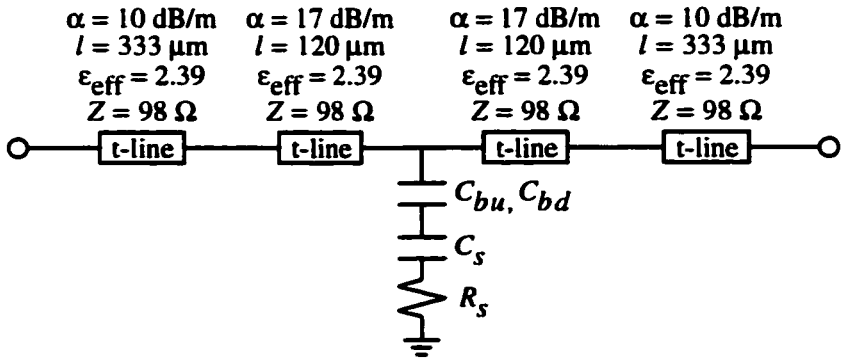


Figure 4.12: Single unit cell ADS model for the 180°-bit second generation phase shifter.

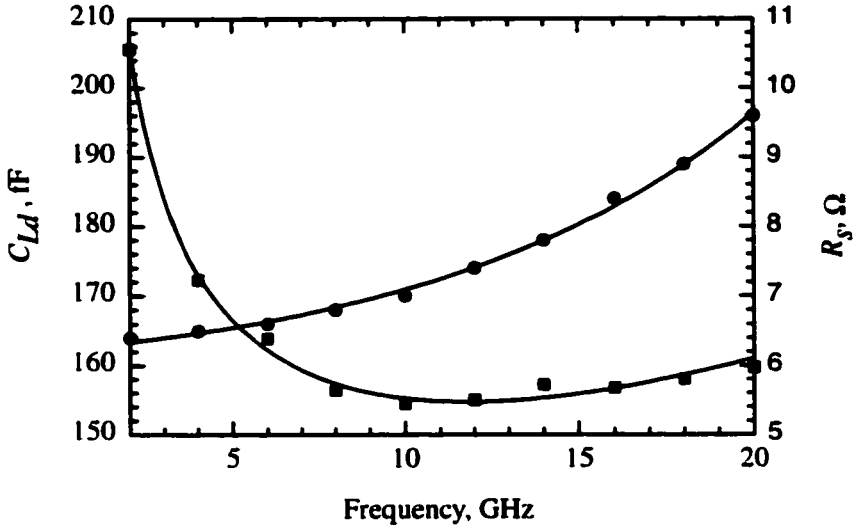
done by increasing the MIM metallization thickness and/or by using a higher conductivity base metal such as gold topped with a thin tungsten or titanium layer, which will prevent hillocking in the PECVD nitride deposition. The expected insertion loss at 11.4 GHz is -0.9 dB for a 180° phase shifter with a MIM capacitor $Q = 60$.

The fabricated MEMS switches were nearly ideal. Their capacitance in the up-state position is exactly as designed, they switch to a > 20 capacitance ratio, and return to their original position after millions of cycles of actuation. What remains in the final aspect of design is to improve the insertion loss by decreasing the influence of static capacitor Q loss as much as possible. This could be done with MIM capacitors as described in the previous paragraph, but since they do have limitations, a much higher Q design will be used: the MAM (Metal-Air-Metal) capacitor.

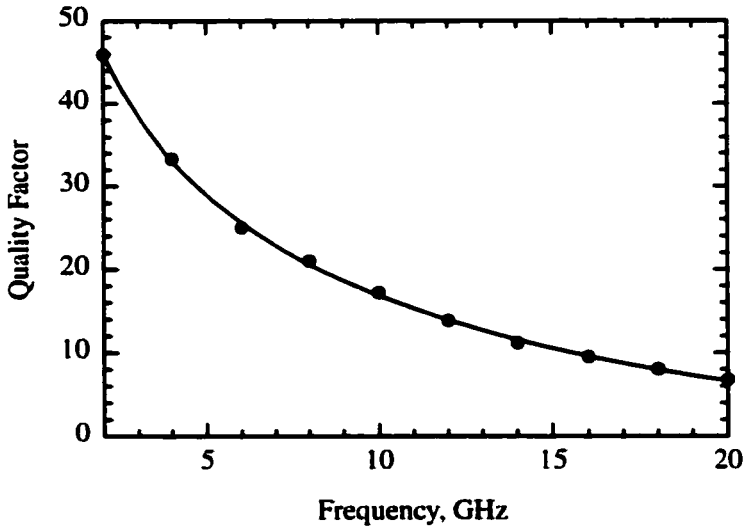
4.5 Final Design: Two-bit MAM CPW

4.5.1 Introduction

The two-bit X-Band design described here the first demonstration utilizing high-Q MAM (Metal-Air-Metal) capacitors instead of the standard MIM (Metal-Insulator-Metal) capacitors. The high-Q MAM capacitors are responsible for a drastic improvement in the performance of the DMTL phase shifter. Also, high-resistivity bias lines have been introduced



(a)



(b)

Figure 4.13: Representations of closed-form expressions used to obtain modeled results for the 180°-bit and two-bit second generation phase shifter. Symbols indicate the values to which the curves were fit.

for lower-voltage actuation of the MEMS switches. The effect of the bias lines is discussed in Section 4.5.5.

The design starts with the closed-form expressions for phase shift, MEMS separation, and loading capacitors, but true modeling was best achieved by the software package Sonnet [49], a method of moments simulator which is found to produce accurate simulations of these distributed circuits. The Sonnet simulation is performed on only one unit cell and a multiple cell simulation is obtained by cascading the unit-cell S-parameters in a circuit simulator such as Agilent-ADS [1].

4.5.2 Effect of the Loading Capacitor Q

The loss of the loading capacitor is modeled as a resistance, R_p, in parallel with C_s (or a resistance, R_s, in series with C_s). The capacitor Q can be written as:

$$Q = \frac{1}{\omega C_s R_s} = \omega C_s R_p \tag{4.2}$$

and

$$R_p = \frac{1}{\omega^2 C_s^2 R_s} \tag{4.3}$$

The other component of phase shifter loss, the transmission line loss, α, was derived in Section 2.12.2. The effect of this unloaded line performance is determined from the unloaded t-line series resistance is R_t, and the impedance Z, which is taken as the down-state loaded impedance when the static capacitor is connected to the t-line. The total loss can be written as:

$$\alpha \cong 8.686 \, (\frac{R_t}{2Z_d} + \frac{Z_d}{2R_p}) \quad \text{dB/section} \tag{4.4}$$

Consider for example a X-band (f_o = 10 GHz, f_B = 23 GHz) design with loaded impedances of $Z_u = 60\ \Omega$ and $Z_d = 42\ \Omega$. The CPW line dimensions are 300/300/300 μm ($Z_o = 98\ \Omega$, $\epsilon_{eff} = 2.36$) with a measured unloaded line loss of 11.2 dB/m at 10 GHz ($R_t = 250\ \Omega$/m). The corresponding spacing and loading capacitances are s = 1,500 μm and $C_s = 267$ fF.

Table 4.1 shows the effect of the capacitor Q loss in relation to the other major contributor of DMTL loss, the loaded-line loss. It is clear from the table that one needs $Q \geq 150$ for

Q	R_p kΩ	Q loss dB/m	Loaded-line loss dB/m
inf	inf	0	28.7
250	14.9	11.8	28.7
150	8.9	19.7	28.7
100	6.0	29.5	28.7
50	3.0	59.0	28.7

Table 4.1: Effect of capacitor Q on the loss performance assuming C_s = 267 fF and unloaded line loss is 11.2 dB/m at 10 GHz.

low loss performance. For this reason, MAM capacitors, which have an inherently higher Q than MIM capacitors, were designed and implemented in this work.

The effect of the capacitor Q vs. frequency is presented in Fig. 4.14 for the designs mentioned above. Again, it is seen that for $Q \sim 150$, there is a broad maximum around the design frequency, especially at higher frequencies. In theory, for Q = inf, the performance improves monotonically with frequency since the t-line loss increases as $\sqrt{f}$ while the phase shift increases as f.

There is another advantage to using MAM capacitors: physical size. Whereas a single MIM capacitor for X-band may be 25 × 25 μm^2, the MAM capacitor is around 120 × 120 μm^2. The capacitance requirements are very small at Ku and Ka-band frequencies, making the MIM capacitors almost too small to fabricate, but MAM capacitors are quite easy to fabricate up to W-band and above since they are much larger.

4.5.3 Design and Fabrication

Figure 4.15 shows a unit cell of the X-band phase shifter (s = 1,150 μm) on a 500 μm thick quartz substrate (ϵ_r = 3.6). The MEMS switch is suspended over the center conductor, is anchored in the CPW gap, and is attached to a thin-film bias-line resistor. The MEMS switch is also connected to a short t-line, which ultimately forms the bottom metal of the MAM (Metal-Air-Metal capacitor). The MAM capacitor is plated on three sides thus providing a very high Q, rigid and stable capacitor (Fig. 4.16). The sacrificial layer underneath the MAM capacitor is PMMA, and is defined using an oxygen plasma in a reactive ion etcher, as described in Section 4.4.3.

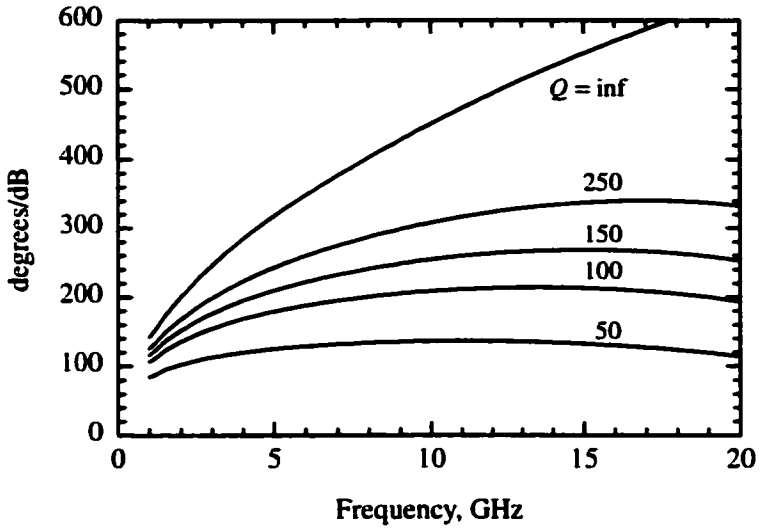
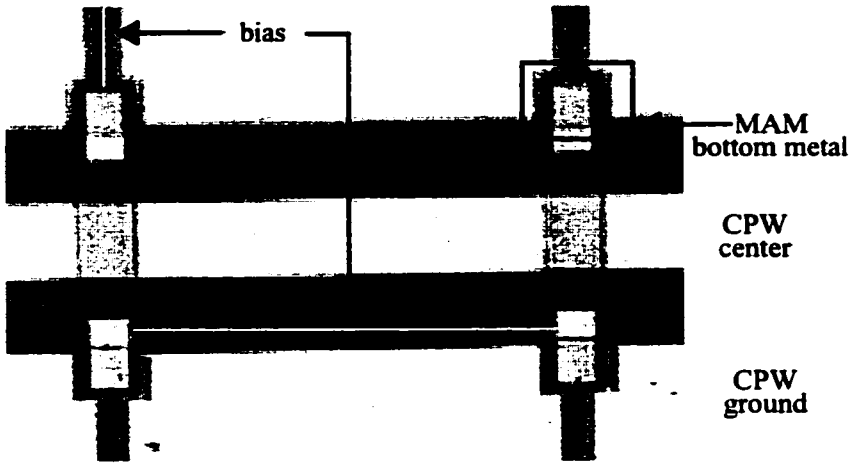


Figure 4.14: Effect of the capacitor Q vs. frequency for a typical X-band design.

The impedance of the CPW unloaded line without the MAM cuts in the ground plane is approximately 98 Ω. However, fringing capacitance (2 × 25 fF) due to the ground-plane cuts lowers the t-line impedance to around 72 Ω. Test structures show that the combined Q of the fringing and MAM capacitance to be ≥ 250. Each MAM capacitor is approximately 81.5 fF, and the fringing capacitance due to the ground-plane cuts is 25 fF, resulting in a total loading capacitance of 213 fF. When the MEMS switches are activated, this loading lowers the CPW line impedance from 98 Ω to 46 Ω.

A photograph of the entire X-band two-bit phase shifter is shown in Figure 4.17. It consists of two sections, and each is connected to its own bias line. The first section has 7 switches and is designed to have $\Delta\phi = 90°$ at 10 GHz. The second section has 14 switches and is designed to have $\Delta\phi = 180°$ at 10 GHz. Differential phase shifts of 90°, 180°, and 270° result from applying a ±20 V AC bias voltage to the individual sections. The AC bias voltage is needed to eliminate dielectric charging and to increase the lifetime of the MEMS switch to billions of cycles.

The fabrication of the phase shifters follows that described in Section 4.4.3 except for a couple of changes (the complete fabrication process is detailed in Appendix B). First, the



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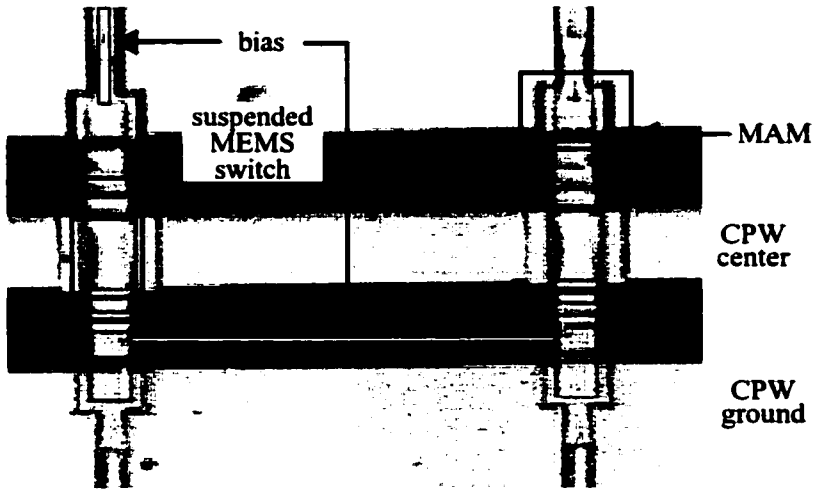


(b)

Figure 4.15: Photograph of the final generation X-band DMTL phase shifter showing a unit cell before electro-plating (a) and after (b), thus forming the MAM capacitor.

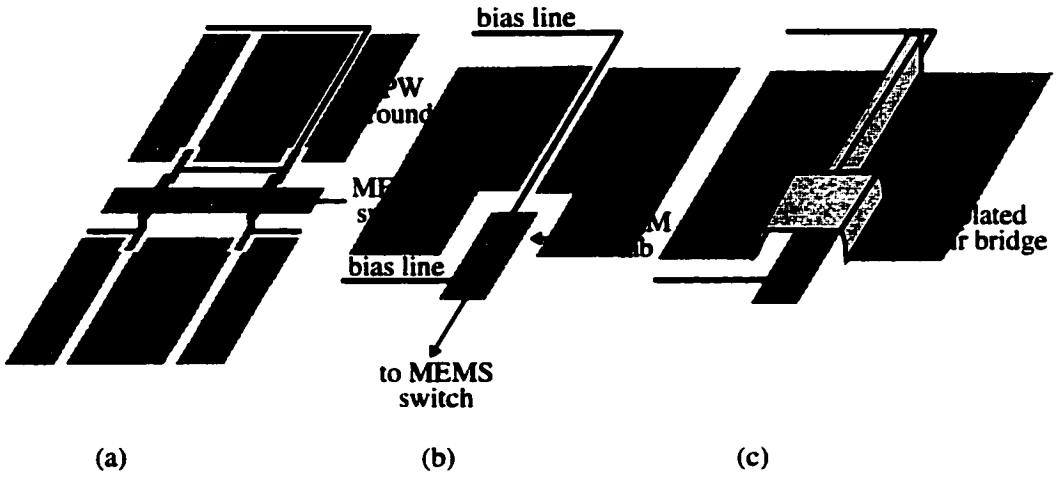


Figure 4.16: Fabrication drawing of the MAM (Metal-Air-Metal) capacitor. (a) The bias line is run in a gap of the CPW ground at one point per bit and from there, runs in the CPW gap from switch to switch. (b) Detail drawing. (c) The complete MAM capacitor after a sacrificial layer over the MAM tab is removed, over which an air bridge was formed by electroplated gold.

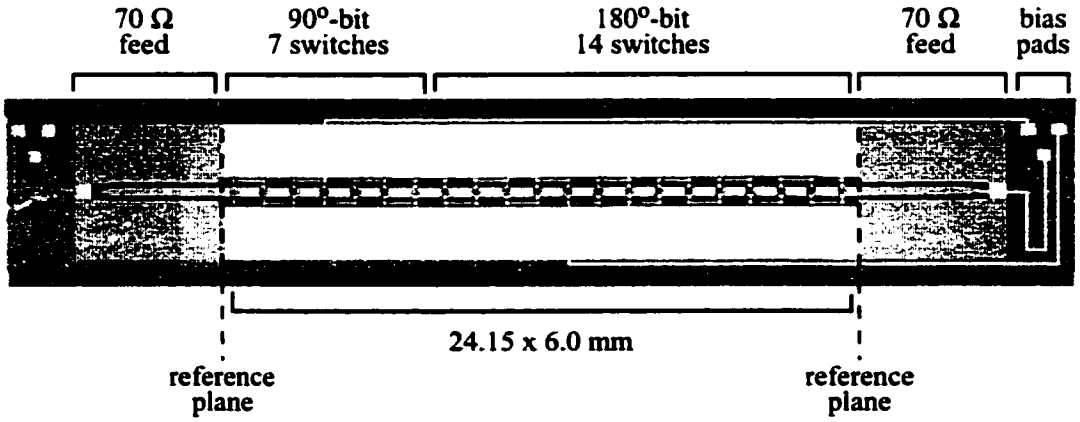
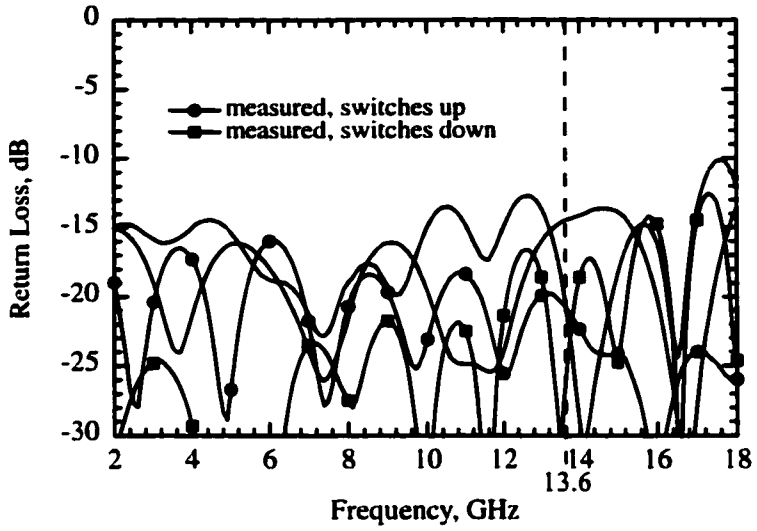
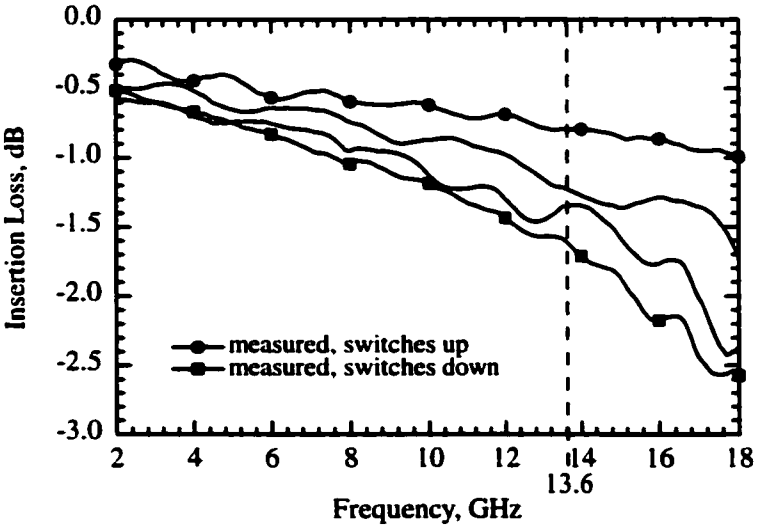


Figure 4.17: Photograph of the final generation X-band, two-bit, 21-section DMTL phase shifter.



(a)



(b)

Figure 4.18: Measurement of the final generation X-band, two-bit, DMTL phase shifter. Return loss is better than −12.5 dB, and the average insertion loss is −1.2 dB at 13.6 GHz.

bias layer is sputtered onto the blank quartz wafer and wet etched in buffered hydrofluoric acid using a photoresist mask. Tungsten metallizations are completely removed from the process flow and replaced by 500/8,000/500 Å thick layers of evaporated Ti/Au/Ti. The evaporator used has an administrative limit of 8,000 Å thick for gold, but this is sufficient since this thickness is nearly one skin depth at 10 GHz, which means loss under the MEMS switch is minimized. The following process steps, including the nitride and sacrificial layer steps are as before. The aluminum switch membrane is replaced by a mostly gold, 8,000 Å thick layer sputtered in a nitrogen environment at 9.5 mT. Electroplating is as before except now the switch membrane is reinforced (in addition to the posts) at the step height change where the CPW center conductor edges meet the substrate (20 μm on either side of points marked by "*" in Figure 2.16). These points must be reinforced since the membrane and underlying layer are nearly the same thickness and are quite weak here. Release and wafer drying steps are performed as before.

4.5.4 Measurement and Simulation

The X-band design was developed for a MEMS switch and a MAM capacitor with a height of 1.5 μm. The fabrication procedure used for the MEMS switch was changed in hopes of producing a lower stress switch and this was accomplished by removing most of the titanium metals from the sputtered gold switch and leaving out the annealing step. However, as a result of changing the fabrication procedure, the switch lowered to 1.2 μm after release, while the MAM capacitor remained at 2.1 μm, the PMMA sacrificial height used. The movement is consistent over all 21 switches, and was measured by a light-interferometer microscope. This measurement also shows that bowing and curling of the metal membrane to be less than 2,000 Å over its span and width. The MEMS switch up-state capacitance with a height of 1.2 μm is 232 fF. As a result, the loaded impedances are shifted from the ideal 60-42 Ω to 60-46 Ω. The resulting spring constant is 30 N/m with pull-in voltage of V_p = 13-14 V. The switching time is calculated to be 9 μs for a switching voltage of $V_s = 20$ V [5].

The measured phase shifter therefore does not operate at 10 GHz, but the distributed de-

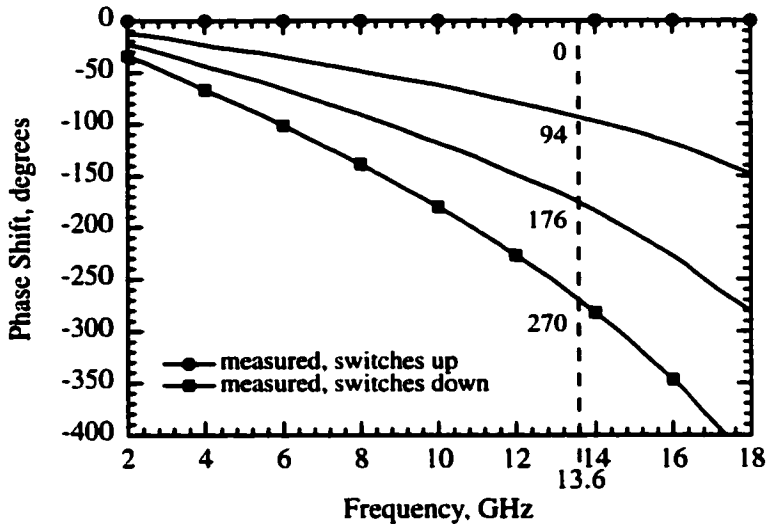


Figure 4.19: Phase shift measurement of the final generation X-band, two-bit, DMTL phase shifter.

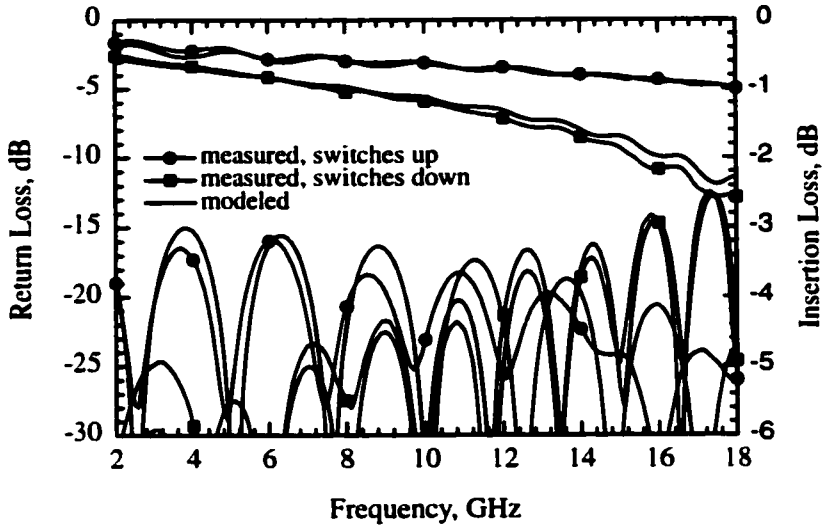
sign is so wideband, that proper operation was achieved around 14 GHz. Figures 4.18 and 4.19 show the measured two-bit performance with differential phase shifts of 94°, 176°, and 270° at 13.6 GHz. All states have a return loss of better than −12.5 dB, with a worst-case insertion loss of −1.6 dB. The average insertion loss is −1.2 dB.

Simulation using a combined Sonnet/ADS method and using the new suspended heights agree quite well with measurements, as seen in Figure 4.20. Also modeled by the full EM simulation is the loss due to the thin film Si-Cr bias resistor, whose effect is discussed next.

4.5.5 Effect of the Bias Lines

Sonnet/ADS X-band simulations demonstrate that the two-bit phase shifter would have a *maximum* insertion loss of −1.0 dB at 13.6 GHz if no bias lines were present, or if the resistances linking the switches are increased significantly from 45 kΩ. This loss should be compared to the measured *maximum* insertion loss of −1.6 dB at 13.6 GHz. This large influence on loss is caused by the bias lines and is explained below.

The biasing of each bit is achieved using a single high-resistance line which is attached to one of the switches in the bit, and then moving the bias from switch to switch using a thin-



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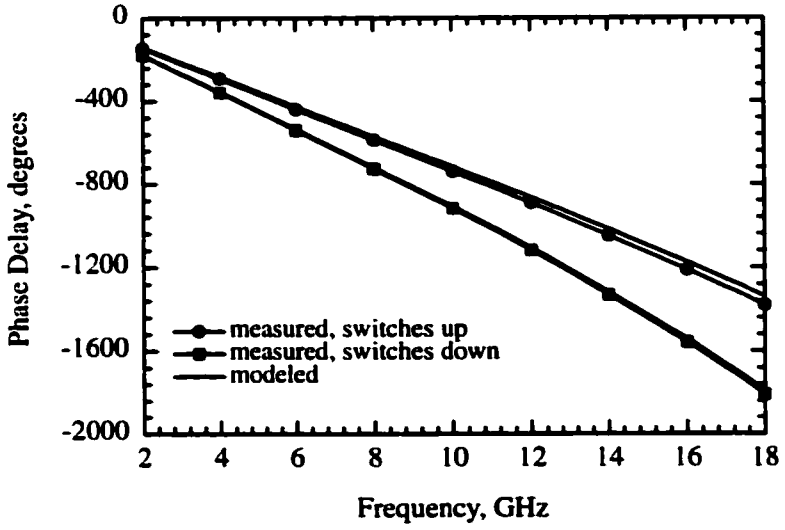


(b)

Figure 4.20: Measurement (with symbols) vs. simulation of the final generation, two-bit DMTL phase shifter with all switches either up or down.

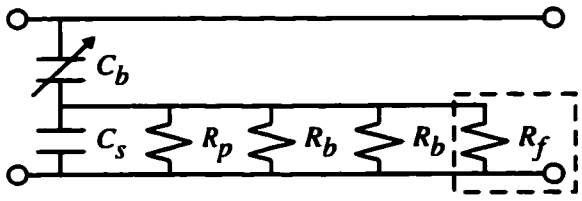


Figure 4.21: Lumped model of unit cell loading showing how the MAM Q is effectively reduced by bias lines. R_p is the loss due to the MAM Q itself. R_b is the effective resistance of the long bias line connecting the switches and R_f is the effective resistance of the bias line feed, which is present at only 2 out of 21 sections of the two-bit phase shifter.

film high-resistance line (Fig. 4.15 and 4.16) placed in the gap. Although the layout is near optimal, the bias lines still have a significant effect on the overall insertion loss performance of the phase shifter because they decrease the effective Q of the MAM capacitors.

The bias lines are sputtered from a silicon-chrome target, defined using wet etching (BHF), and are 20 μm wide, 1,500 Å thick, and approximately 1,150 μm long. The conductivity of the material is 2,150 S/m, thus resulting in a resistance of 44.6 kΩ from switch to switch. Effectively, the MAM capacitors "see" two of these resistances in parallel because there are two bias lines attached to each switch (Fig. 4.21). Additionally, where the bias lines feed underneath the CPW ground and contact the first switch in a phase bit, the capacitor Q is further reduced by another resistance in parallel with the two mentioned above. This small resistor is modeled as a 30 μm long section of resistive line because the Si-Cr line strongly couples to the ground plane by means of the air bridge over it. The effective resistance of this short section is 1.16 kΩ.

The X-band design has a static MAM capacitance, C_s of 213 fF and using a Q of 400 at 13.6 GHz, $R_p = 33$ kΩ. By adding the resistance (R_b) of two parallel bias lines in parallel with R_p, the Q is effectively reduced from 400 to 160. The reduction in Q is most dramatic in the two sections of the phase shifter (out of 21) where the bias lines feed the MEMS switches. In this case, the Q is effectively reduced to around 15 (for a single section per phase bit). This reduction in the capacitor Q increases the maximum measured loss (when

Loss component	X-band design
Plated line loss	0.76 dB
Evaporated line loss	0.24 dB
19 Section Q loss	0.20 dB
2 Section Q loss	0.43 dB
Total max. loss	1.63 dB
Measured max. loss	1.60 dB

Table 4.2: Loss contributions (all switches down) in the final generation DMTL phase shifter.

all switches are down) from an ideal value of -1.0 dB to the measured value of -1.6 dB at 13.6 GHz.

4.5.6 Loss Components

There are three contributors to the insertion loss of the DMTL phase shifter: 1) line loss of the plated high-impedance line $R_t = 255\ \Omega$/m at 13.6 GHz), 2) line loss of the thin high-impedance line underneath the MEMS switch ($R_t = 435\ \Omega$/m at 13.6 GHz), and 3) Q loss of the MAM capacitors. The influence of each of these contributors on the measured design is summarized in Table 4.2. The plated and evaporated line losses are obtained from measured test structures. Each section of the X-band ($s = 1{,}150\ \mu$m) DMTL includes a 200 μm-long evaporated section underneath each MEMS switch. The capacitor Q loss is all encompassing, including the reduction in MAM Q due to the bias lines. The loss in Table 4.2 is split into two parts: the first part details loss in the 19 sections where there is a reduction in Q to 100-200 due to the bias lines. The second part details the loss in the remaining two sections where the Q is greatly reduced by the bias line feeds under the CPW ground plane. It should be noted that without bias lines, the loss of the DMTL phase shifter is essentially that of the plated and evaporated sections alone, as confirmed by simulations, because the Q of the MAM capacitors is quite high.

4.5.7 Conclusion

This section presents very low-loss X-band distributed phase shifters improved by the use of high Q MAM capacitors. The switch height was incorrect, and this moved the design frequencies from 10 GHz to 13.6 GHz. Still, the concept of using a very high Q MAM capacitor in series with a low-loss MEMS switch is proven to work very well, especially if the influence of bias lines is removed from the design. The results present state-of-the-art performance for true-time delay phase shifters at Ka-Band frequencies. The design can be easily scaled to 30-40 GHz, and this is presented in Chapter 6.

CHAPTER 5

Ku-BAND MICROSTRIP DMTL PHASE SHIFTERS

5.1 Introduction

Two and four-bit wideband distributed microstrip phase shifters were developed on a 21 mils (533 μm) silicon substrate ($\epsilon_r = 11.8$) for DC-18 GHz operation. Presented here is the first demonstration of a microstrip distributed MEMS transmission line (DMTL) phase shifter design, periodically loaded by MEMS varactors in series with fixed value microstrip radial stubs, as described in Section 2.13.2, and as shown in Figure 2.9.

The design was developed at the University of Michigan and fabricated by Raytheon Company, Dallas, Texas as a joint collaboration to compare their microstrip switched-line phase shifters on the same silicon substrate to the distributed design. Under the agreement, no significant changes would be made to their mature fabrication process for the MEMS switch so that no uncertainties would be introduced into the fabrication, since the majority of the wafer would be used for other Raytheon MEMS circuits.

5.2 Phase Shifter Design

The microstrip DMTL phase shifter design consists of a high impedance line ($> 50\ \Omega$) loaded by MEMS switches and microstrip radial stubs as shown in Figure 5.1. When a bias voltage is applied between the MEMS switch and the high impedance line using a 120 kΩ resistor, the MEMS switch capacitance increases by a factor of 80 and the loading to the line therefore becomes dominated by the microstrip stub alone. The microstrip stubs are

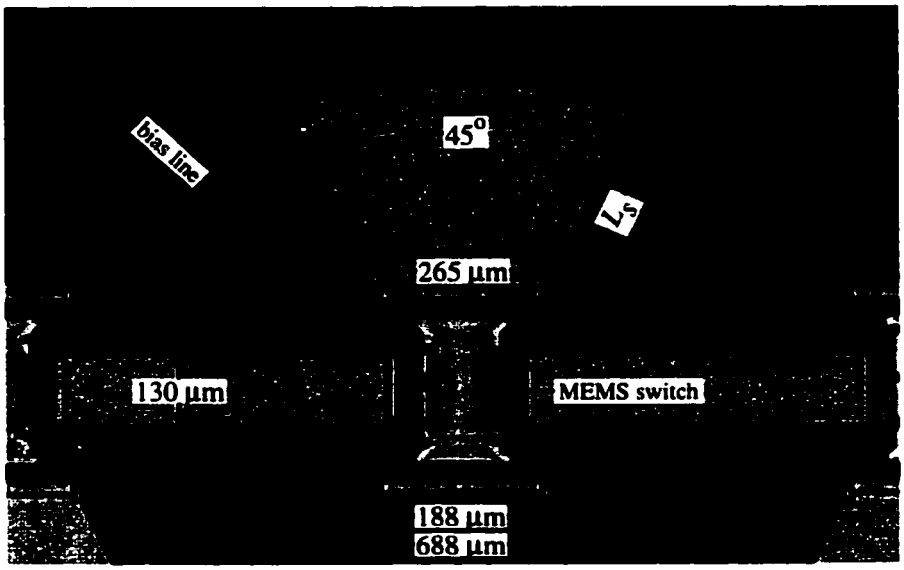


Figure 5.1: Photograph of a single MEMS section. The radial stub is fed by a 120 kΩ bias line. The MEMS bridge lays over the high impedance line, which runs from left to right in the photograph.

a particularly beautiful aspect of these designs as the fabrication process for the stubs is extremely simple compared to a typical MIM or MAM capacitor process. In addition, the stubs provide a virtual ground connection and therefore a complicated via hole process is not required, as described in Section 2.12.2.

The high-impedance t-line is 130 μm wide on a 21 mils silicon substrate which results in an impedance of 78 Ω. The Bragg frequency is placed at approximately 3 times the design frequency (10 GHz) for maximum phase shift linearity [16]. The Bragg frequency can be chosen to be 1.8 times the design frequency for a longer phase shifter, because MEMS separation will increase with Bragg frequency, but at the expense of less phase linearity up to 18 GHz, as detailed in Section 2.8.1.

A larger separation between switches may be desirable because if the separation is too small, the microstrip radial stubs can RF couple to one another or even overlap. For the 16 GHz silicon substrate design presented here, where the radial stubs are positioned on alternating sides of the high impedance line (Fig. 5.2), the Bragg frequency is appropriately selected since the stubs are quite short. However, higher frequency designs which require

a smaller separation between the MEMS switches and lower dielectric constant substrates generally need longer stubs, unless the substrate is made quite thin, which would be counter-productive since unloaded line loss would increase significantly. In such cases, the Bragg frequency must be carefully selected.

Closed-form expressions for phase shift, MEMS separation, and loading capacitance result in the design parameters contained in Table 5.1. Modeling of the phase shifter is performed on HP Series IV [45], which includes the high-impedance t-line microstrip model, the MEMS switch model, and the radial stub microstrip model.

A photograph or the two-bit and four-bit phase shifters are contained in Figures 5.2 and 5.3, respectively. Each bit of the phase shifter is linked to a bias pad for electrostatic actuation. The two-bit phase shifter consists of two sections. The 180°-bit section has 15 MEMS switches and the 90°-bit section has 8 MEMS sections. Normally, the number of MEMS switches contained in each section would equal an even multiple of the number of switches in the lowest order bit (8 and 16 switches in this case). However, these phase shifters are to be measured in a special nitrogen environment, temperature controlled, hermetic chamber which limits how far the RF probes can be separated. The original design had to be shortened by one MEMS section as a result. For this reason, the 180°-bit section has 15 MEMS switches instead of 16, and the radial stubs were tuned to be slightly longer to compensate for the phase shift lost by the removal of the MEMS switch.

The four-bit phase shifter consists of 4 sections, each having 15, 8, 4, and 2 MEMS switches, respectively. The unloaded line is meandered so that the circuit can fit in the measurement chamber. The radial stubs lengths are also tuned as described for the two-bit phase shifter.

5.3 Calibration and Measurements

The DMTL microstrip phase shifters are connected using a 6 mils-long, 5 mils-wide, 0.5 mils-thick gold ribbon to off-chip alumina substrate microstrip to CPW transitions, so that the circuit can be measured with CPW probes, and calibrated with CPW standards. Calibration is performed up to the probe tip ends using a load, reflect, match (LRM)

	180°	90°	45°	22.5°
Sections	15	8	4	2
s, MEMS separation (μm)	688	688	688	688
Z_o (Ω)	78	78	78	78
ϵ_{eff}	7.3	7.3	7.3	7.3
Z_{lu} (Ω)	63	64	64	64
Z_{ld} (Ω)	49	51	51	51
f_b (GHz)	33	35	35	35
C_{bu} (fF)	70	70	70	70
Radial stub capacitance (fF)	120	108	108	108
L_s, stub length (μm)	395	360	360	360

Table 5.1: Design parameters for the cascaded sections of the 2 and 4-bit microstrip MEMS DMTL phase shifters.

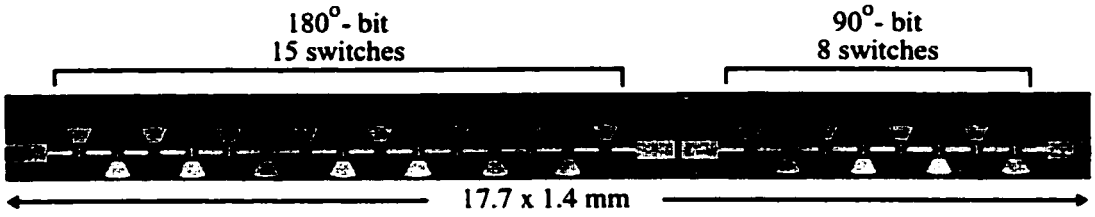


Figure 5.2: Photograph of the complete 2-bit phase shifter.

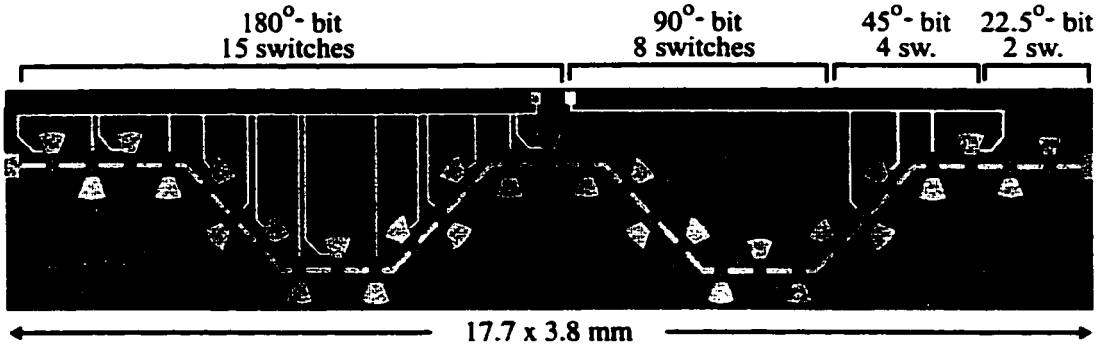


Figure 5.3: Photograph of the complete 4-bit phase shifter.

standard on an alumina substrate. Measurements of the DMTL phase shifter therefore include the input and output transitions and ribbons. The effect of the transitions and ribbons are de-embedded by a linear model which removes a total (back-to-back) loss of -0.05 dB of insertion loss at 10 GHz and -0.2 dB at 16 GHz as well as phase shift of these transitions. The effect of the CPW to microstrip transitions on the return loss cannot be easily de-embedded and thus these measurements are presented raw.

The MEMS structure is measured in a nitrogen environment following a dehydration bake cycle to reduce humidity induced sticking of the MEMS switch to the nitride covered microstrip high impedance line underneath. Pulldown of the MEMS bridges is 40-46 V and the MEMS switch can be maintained in the down-state position using a 15 V bias voltage.

5.4 Two-bit and Four-bit Measurements

The measured performance of the two-bit phase shifter is shown in Figures 5.4 and 5.5a. Return loss for the four states is < -10 dB, and average insertion loss is -2.5 dB at 16 GHz. Table 5.2 lists the measured phase shift for the four states, and as can be seen in the Table, the 2-bit phase response is accurate within +0.5/-0.5° of the ideal at 16 GHz, when a linear fit of measured phase shift data is made from DC-18 GHz.

The measured performance of the four-bit phase shifter is shown in Figures 5.6 and 5.5b. Return loss for the 16 states is < -9 dB, and the average insertion loss is -2.9 dB at 16 GHz. Table 5.3 lists the measured phase shift for the 16 states. The 4-bit phase response is accurate within +4.1/-4.9° of the ideal at 16 GHz.

Simulations vs. measurements of insertion loss for both the two and four-bit cases show a much larger than expected loss for the measured case. As mentioned before, simulations are modeled on Series IV [45], which has very accurate models of microstrip components. Modeling demonstrates that only t-line loss under the MEMS switch can explain the majority of the insertion loss. If loss was dominated by a low Q radial stub capacitance, which may be caused by the bias lines (see Section 4.5.5), there would be four or 16 distinct cases of insertion loss (Figs. 5.4b and 5.6b, respectively). And if loss was dominated by a high MEMS switch resistance, the insertion loss at high frequencies would be much higher than

State	Measured	Design	Error
1	0.0°	0.0°	0.0°
2	−90.5°	−90.0°	−0.5°
3	−180.0°	−180.0°	0.0°
4	−269.5°	−270.0°	+0.5°

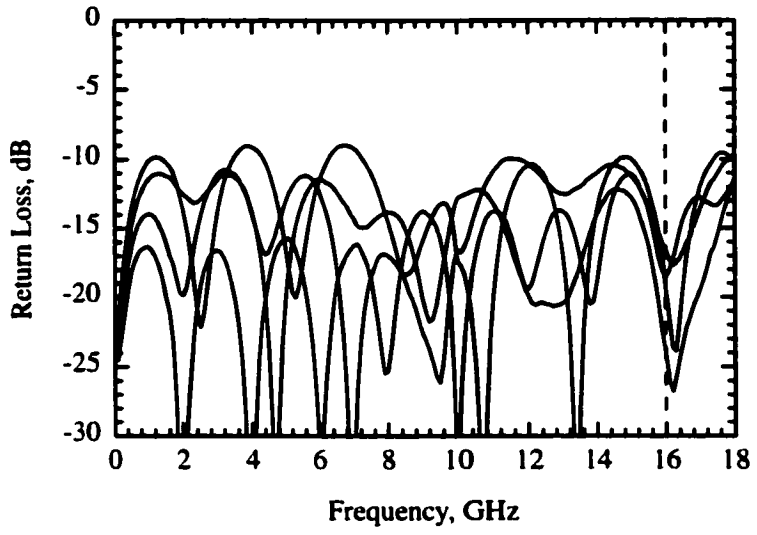
Table 5.2: Measured phase shift of the microstrip 2-bit MEMS DMTL phase shifter at 16 GHz.

State	Measured	Design	Error
1	0.0°	0.0°	0.0°
2	−22.1°	−22.5°	+0.4°
3	−49.9°	−45.0°	−4.9°
4	−69.6°	−67.5°	−2.1°
5	−88.2°	−90.0°	+1.8°
6	−109.4°	−112.5°	+3.1°
7	−136.9°	−135.0°	−1.9°
8	−157.0°	−157.5°	+0.5°
9	−180.3°	−180.0°	−0.3°
10	−201.8°	−202.5°	+0.7°
11	−228.9°	−225.0°	−3.9°
12	−248.9°	−247.5°	−1.4°
13	−267.1°	−270.0°	+2.9°
14	−288.4°	−292.5°	+4.1°
15	−316.0°	−315.0°	−1.0°
16	−335.7°	−337.5°	+1.8°

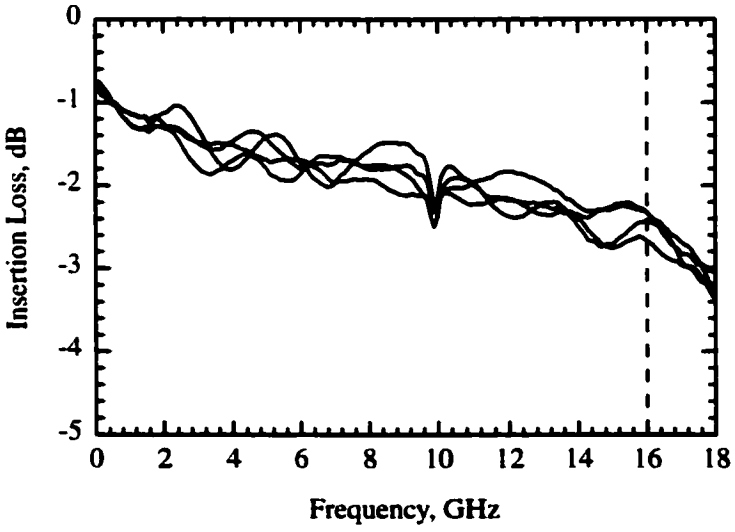
Table 5.3: Measured phase shift of the microstrip 4-bit MEMS DMTL phase shifter at 16 GHz.

those at low frequencies.

As described in section 5.1, it was not possible to redesign any significant aspect of the Raytheon MEMS switch, which is suspected to contain a very thin metallization under the MEMS switch. The phase shifters presented here provide an excellent proof-of-concept, but the reader should be aware much lower insertion losses are possible in future designs.

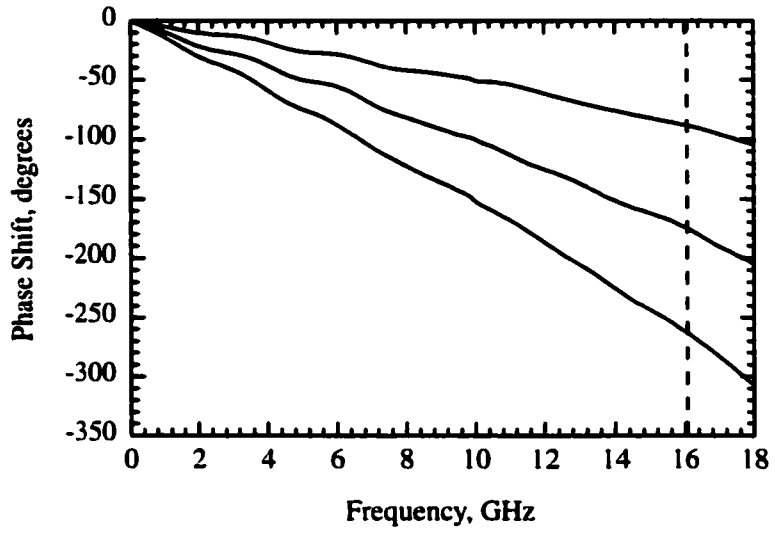


(a)

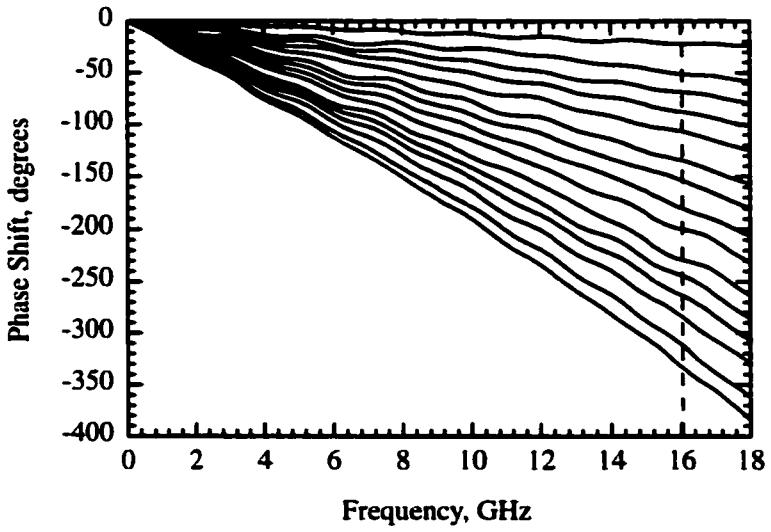


(b)

Figure 5.4: Measured return loss (a) and insertion loss (b) results of the microstrip 2-bit MEMS DMTL phase shifter.

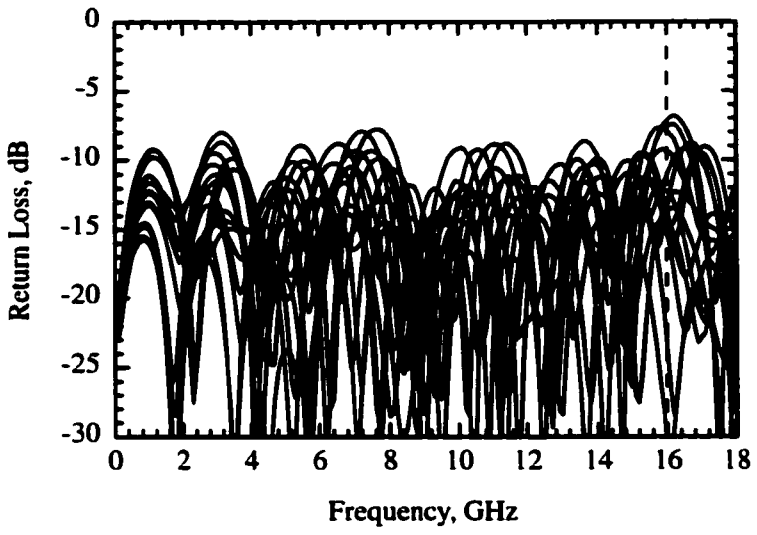


(a)

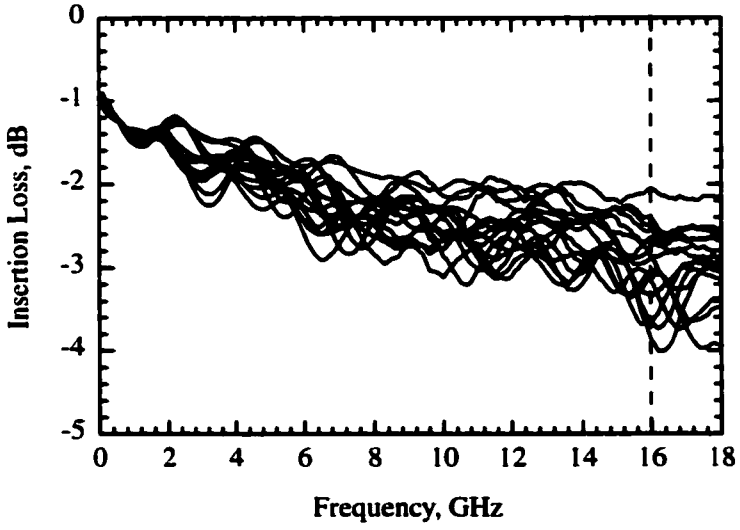


(b)

Figure 5.5: Measured phase shifts of the microstrip 2-bit (a) and 4-bit (b) MEMS DMTL phase shifters.



(a)



(b)

Figure 5.6: Measured return loss (a) and insertion loss (b) results of the microstrip 4-bit MEMS DMTL phase shifter.

Loss contribution	16 GHz
Plated line sections	−0.7
Thin line sections	−1.9
MEMS switches	−0.2
Microstrip stubs	−1.0
Total max. loss	−3.7
Measured average loss	−2.9

Table 5.4: Insertion loss contributions to the microstrip 4-bit MEMS DMTL phase shifter.

5.5 Loss Contributions

There are four main contributions to the insertion loss in the DMTL phase shifter. Table 5.4 contains the estimates of losses for the 4-bit phase shifter which are attributable to each of these factors:

1. Line loss of the plated high impedance t-line (500 μm long out of each 688 μm section).
2. Line loss of the thin high impedance t-line under the MEMS bridge (188 μm long out of each 688 μm section).
3. Bridge loss (0.5 Ω per MEMS bridge).
4. Q loss in the microstrip radial stub (Q=100).

5.6 Conclusions

The microstrip DMTL MEMS phase shifters presented here are very wideband. In fact, the phase shift remains linear up to 20 GHz. This first-cut design can be optimized by lengthening the radial stubs so that the DMTL is loaded to more optimal impedances (60 and 42 Ω) for maximum phase shift and minimum reflection loss. Also, a large part of the insertion loss is due to the thin metal layer underneath the MEMS switches. The insertion loss will improve to −1.8 dB if a thicker metal layer is used underneath the MEMS switches. Phase error will further improve if a single radial stub length is used in conjunction with sections containing even multiple MEMS sections (Section 5.2).

CHAPTER 6

Ka-BAND CPW DMTL PHASE SHIFTERS

6.1 Introduction

The Ka-Band design described here is the first demonstration of a DMTL phase shifter at 30-40 GHz, and the first demonstration utilizing high-Q MAM (Metal-Air-Metal) capacitors instead of the standard MIM (Metal-Insulator-Metal) capacitors. The high-Q MAM capacitors are responsible for a drastic improvement in the performance of the DMTL phase shifter. Also, high-resistivity bias lines have been introduced for lower-voltage actuation of the MEMS switches. The effect of the bias lines is discussed in Section 6.5.

The design started with the closed-form expressions for phase shift, MEMS separation, and loading capacitors, but true modeling was best achieved by the software package Sonnet [49], a method of moments simulator which is found to produce accurate simulations of these distributed circuits. The Sonnet simulation is performed on only one unit cell and a multiple cell simulation is obtained by cascading the unit-cell S-parameters in a circuit simulator such as Agilent-ADS [1]. These results are very competitive with switched transmission-line and reflection-based phase shifters, and the distributed design can be easily scaled to V-band and W-band frequencies for wideband low-loss performance.

6.2 Effect of the Loading Capacitor Q

The loss of the loading capacitor is modeled as a resistance, R_p, in parallel with C_s (or a resistance, R_s, in series with C_s, as shown in Fig. 6.1). The capacitor Q can be written

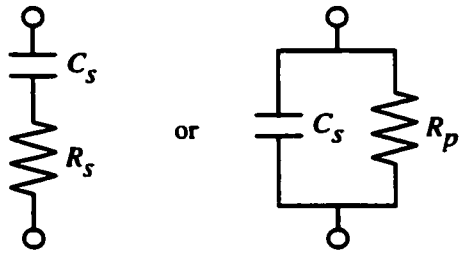


Figure 6.1: Lumped model of a lossy capacitor.

as:

$$Q = \frac{1}{\omega C_s R_s} = \omega C_s R_p$$
$$R_p = \frac{1}{\omega^2 C_s^2 R_s} \tag{6.1}$$

The corresponding t-line loss, α, was derived in Section 2.12.2. The unloaded t-line series resistance is R_t, and the impedance is taken as the down-state loaded impedance when the static capacitor is connected to the t-line. The total loss can be written as:

$$\alpha \cong 8.686\ (\frac{R_t}{2Z_d} + \frac{Z_d}{2R_p})\ \text{ dB/section} \tag{6.2}$$

Consider for example a Ka-band (f_o = 30 GHz, f_B = 67 GHz) design with loaded impedances of $Z_u = 60\ \Omega$ and $Z_d = 42\ \Omega$. The CPW line dimensions are 150/150/150 μm ($Z_o = 98\ \Omega$, $\epsilon_{r,eff} = 2.36$) with a measured unloaded line loss of 38.9 dB/m at 30 GHz ($R_t = 860\ \Omega$/m). The corresponding spacing and loading capacitances are $s = 400\ \mu$m and $C_s = 93$ fF. Table 6.1 shows the effect of the capacitor Q loss in relation to the other major contributor of DMTL loss, the loaded-line loss. It is clear that one needs $Q \geq 150$ for low loss performance. For this reason, MAM capacitors, which have an inherently higher Q than MIM capacitors, were designed and implemented in this work.

The effect of the capacitor Q vs. frequency is presented in Fig. 6.2 for the design mentioned above. Again, it is seen that for $Q \sim 150$, there is a broad maximum around the design frequency, especially at higher frequencies. In theory, for Q = inf, the performance improves monotonically with frequency since the t-line loss increases as $\sqrt{f}$ while the phase shift increases as f.

Q	R_p kΩ	Q loss dB/m	Loaded-line loss dB/m
inf	inf	0	99.7
250	14.6	35.8	99.7
150	8.7	59.7	99.7
100	5.8	89.5	99.7
50	2.9	179.0	99.7

Table 6.1: Ka-band design. Effect of capacitor Q on loss performance (C_s = 93 fF).

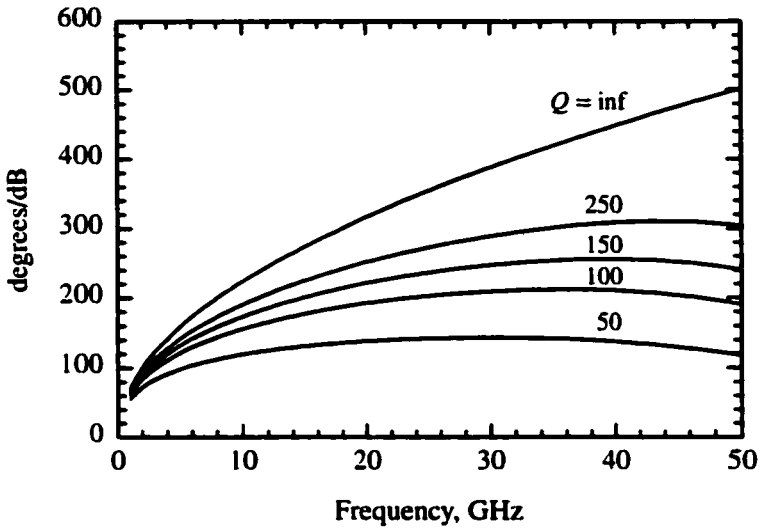
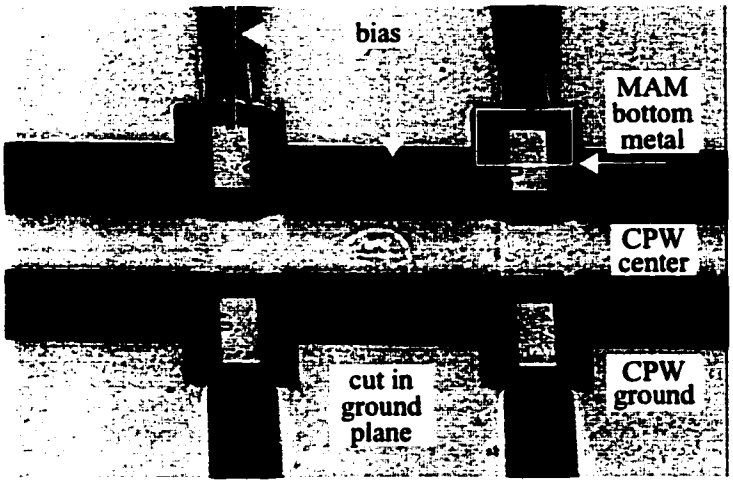


Figure 6.2: Effect of the capacitor Q vs. frequency for Ka-band design.

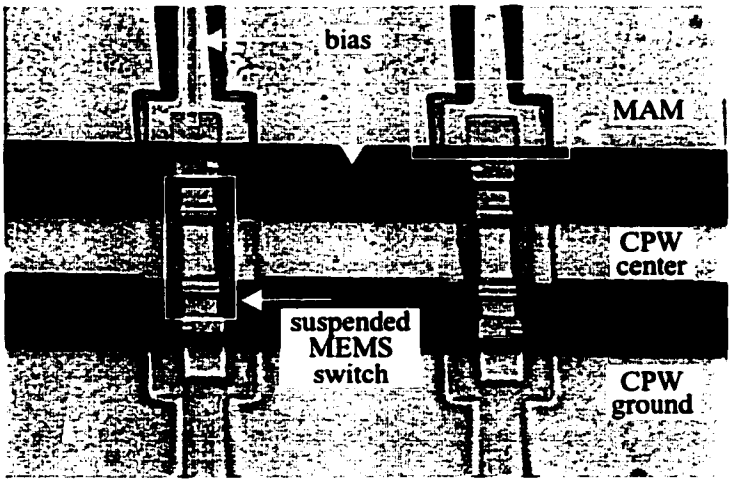
There is another advantage to using MAM capacitors: physical size. Whereas a single MIM capacitor for Ka-band may be 14 × 14 μm^2, the MAM capacitor is around 65 × 65 μm^2. The capacitance requirements are very small at Ku and Ka-band frequencies, making the MIM capacitors almost too small to fabricate, but MAM capacitors are quite easy to fabricate up to W-band and above.

6.3 Phase Shifter Design

Figure 6.3 shows two unit cells of the Ka-band phase shifter (s = 400 μm) on a 500 μm thick quartz substrate (ϵ_r = 3.6). The MEMS switch is suspended over the center con-



(a)



(b)

Figure 6.3: Photograph of the Ka-band DMTL phase shifter showing two unit cells (a) before electroplating and (b) after, thus forming the MAM capacitor.

ductor, is anchored in the CPW gap, and is attached to a thin-film bias-line resistor. The MEMS switch is also connected to a short t-line, which ultimately forms the bottom metal of the MAM (Metal-Air-Metal capacitor). The MAM capacitor is plated on three sides thus providing a very high Q, rigid and stable capacitor (Fig. 6.4). The sacrificial layer underneath the MAM capacitor is PMMA, and is defined using an oxygen plasma in a reactive ion etcher.

The impedance of the CPW unloaded line without the MAM cuts in the ground plane is approximately 98 Ω. However, fringing capacitance (2×9 fF) due to the ground-plane cuts lowers the t-line impedance to around 72 Ω. Test structures show that the combined Q of the fringing and MAM capacitance to be $\geq$ 250. Each MAM capacitor is approximately 24 fF, and the fringing capacitance due to the ground-plane cuts is 9 fF, resulting in a total loading capacitance of 66 fF. When the MEMS switches are activated, this loading lowers the CPW line impedance from 98 Ω to 48 Ω.

A photograph of the entire Ka-band two-bit phase shifter is shown in Figure 6.5. It consists of two sections, and each is connected to its own bias line. The first section has 7 switches and is designed to have $\Delta\phi = 90°$ at 30 GHz. The second section has 14 switches and is designed to have $\Delta\phi = 180°$ at 30 GHz. Differential phase shifts of 90°, 180°, and 270° result from applying a $\pm$20 V AC bias voltage to the individual sections. The AC bias voltage is needed to eliminate dielectric charging and to increase the lifetime of the MEMS switch to billions of cycles.

6.4 2-bit Measurements and Simulations

The Ka-band design was developed for a MEMS switch and a MAM capacitor with a height of 1.5 μm. As in the X-band MAM phase shifter design, which was fabricated on the same wafer as this design, the fabrication procedure used for the MEMS switch was changed in hopes of producing a lower stress switch and this was accomplished by removing most of the titanium metals from the sputtered gold switch and leaving out the annealing step. The resulting spring constant is 30 N/m with pull-in voltage of V_p = 13-14 V. The switching time is calculated to be 9 μs for a switching voltage of $V_s = 20$ V [5]. However,

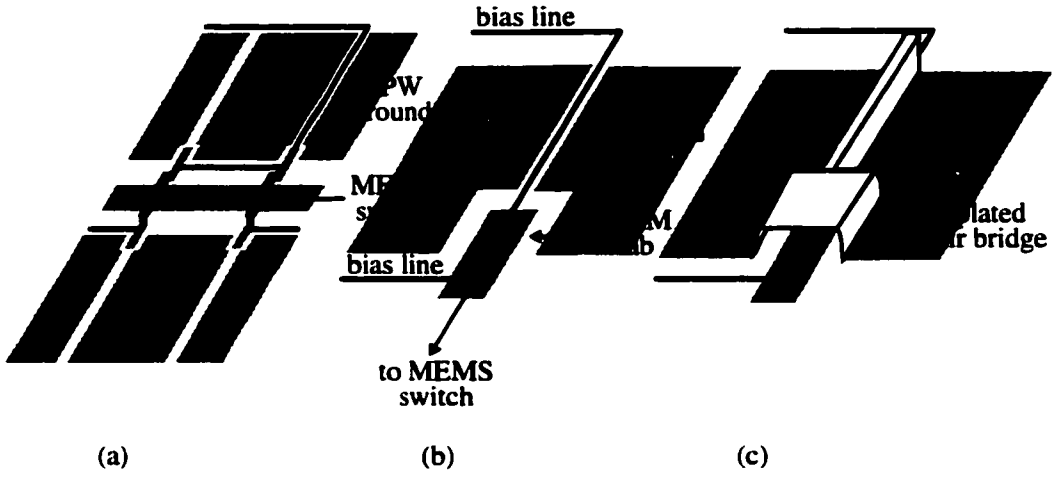


Figure 6.4: Fabrication drawing of the MAM (Metal-Air-Metal) capacitor. (a) The bias line is run in a gap of the CPW ground at one point per bit and from there, runs in the CPW gap from switch to switch. (b) Detail drawing. (c) The complete MAM capacitor after a sacrificial layer over the MAM tab is removed, over which an air bridge was formed by electroplated gold.

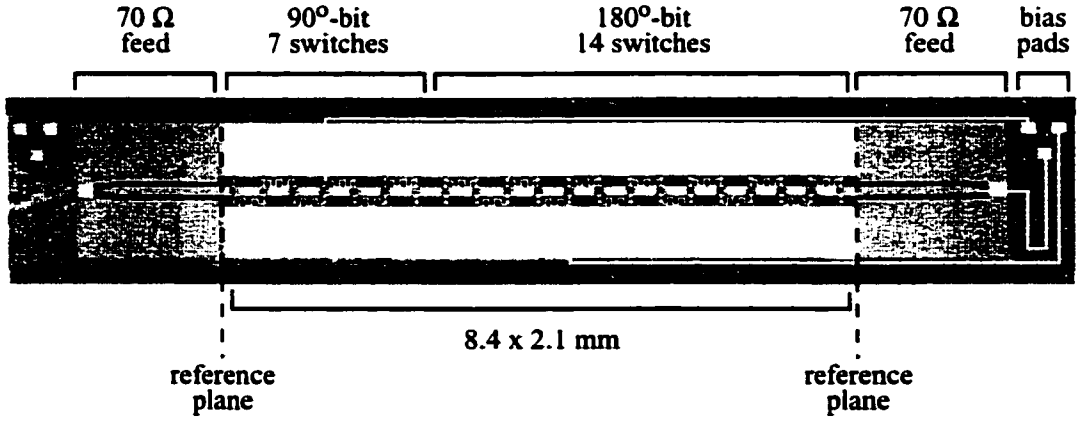
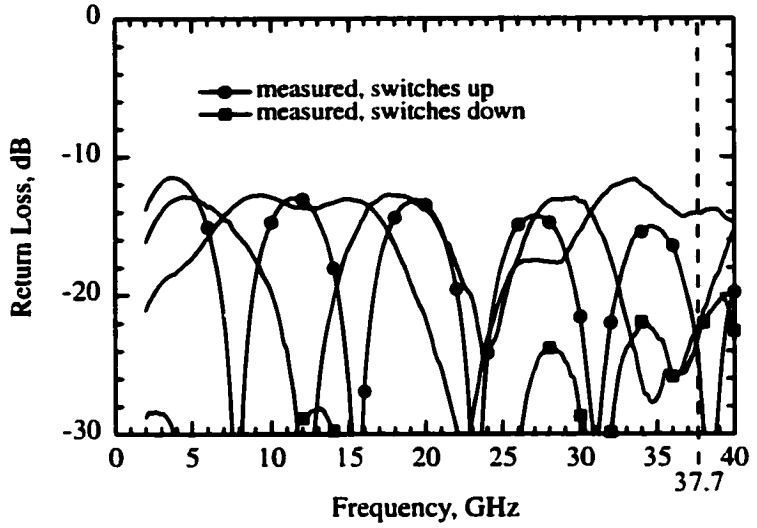
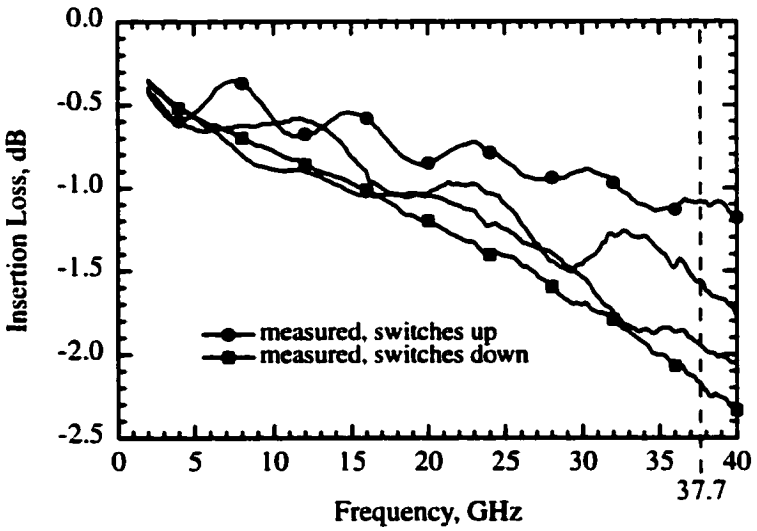


Figure 6.5: Photograph of the Ka-band 2-bit, 21-section DMTL phase shifter.



(a)



(b)

Figure 6.6: Measurement of the Ka-band, 2-bit, DMTL phase shifter. Return loss is better than −11.5 dB, and the average insertion loss is −1.5 dB at 37.7 GHz.

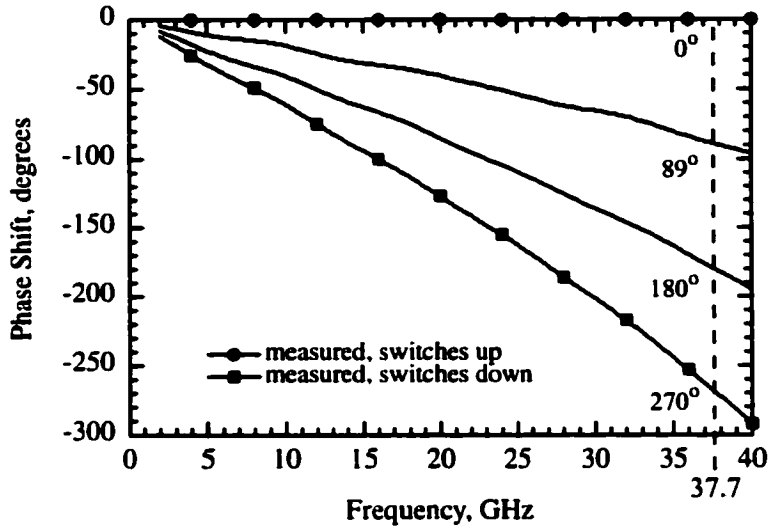
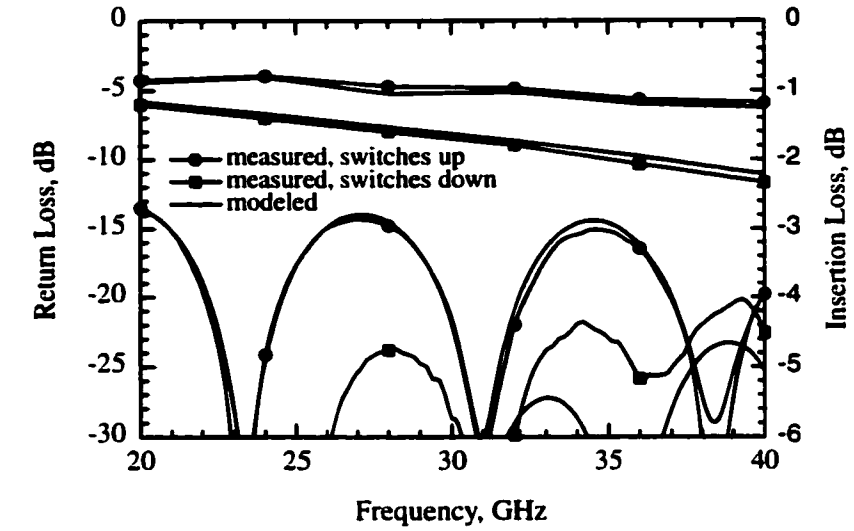


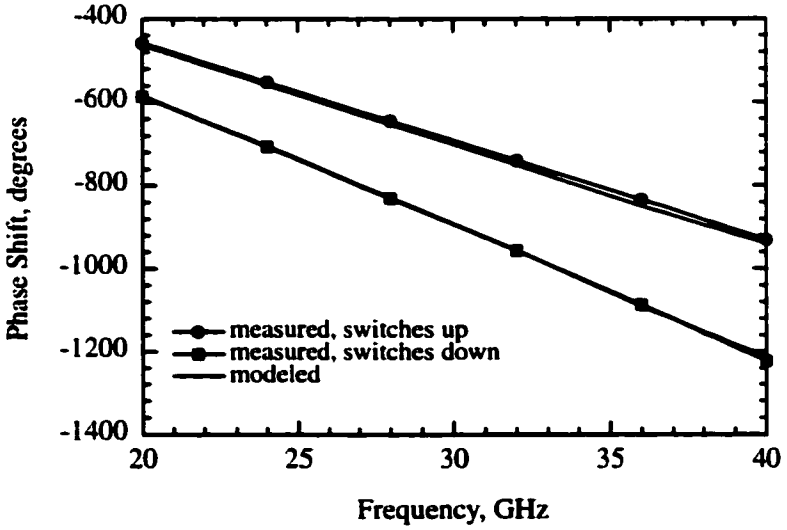
Figure 6.7: Phase shift measurement of the Ka-band, 2-bit, DMTL phase shifter.

as a result of changing the fabrication procedure, the switch lowered to 1.2 μm after release, while the MAM capacitor remained at 2.1 μm, the PMMA sacrificial height. The movement is consistent over all 21 switches, and was measured by a light-interferometer microscope. This measurement also shows that bowing and curling of the metal membrane to be less than 2,000 Å over its span and width. The MEMS switch up-state capacitance with a height of 1.2 μm is 58 fF. As a result, the loaded impedances are shifted from the ideal 60-42 Ω to 62-48 Ω.

The measured phase shifter therefore does not operate at 30 GHz, but the distributed design is so wideband, that proper operation was achieved around 38 GHz. Figures 6.6 and 6.7 show the measured two-bit performance with differential phase shifts of 89°, 180°, and 270° at 37.7 GHz. All states have a return loss of better than -11.5 dB, with a worst-case insertion loss of -2.1 dB. The average insertion loss is -1.5 dB. Simulation using a combined Sonnet/ADS method and using the new suspended heights agree quite well with measurements, as seen in Figure 6.8. Also modeled by the full EM simulation is the loss due to the thin film Si-Cr bias resistor, whose effect is discussed next.



(a)



(b)

Figure 6.8: Ka-band design measurement (with symbols) and simulation of the 21 switch DMTL phase shifter with all switches either on or off.

6.5 Effect of the Bias Lines

Sonnet/ADS X-band simulations demonstrate that the two-bit phase shifter would have a *maximum* insertion loss of -1.1 dB at 37.7 GHz if no bias lines were present, or if the resistances linking the switches are increased significantly from 24 kΩ. This loss should be compared to the measured *maximum* insertion loss of -2.1 dB at 37.7 GHz. This large influence on loss is caused by the bias lines and is explained below.

The biasing of each bit is achieved using a single high-resistance line which is attached to one of the switches in the bit, and then moving the bias from switch to switch using a meandering thin-film high-resistance line (Fig. 6.3 and 6.4). Although the layout is near optimal, the bias lines still have a significant effect on the overall insertion loss performance of the phase shifter because they decrease the effective Q of the MAM capacitors.

The bias lines are sputtered from a silicon-chrome target, defined using wet etching (BHF), and are 20 μm wide, 1,500 Åthick, and approximately 610 μm long. The conductivity of the material is 2,150 S/m, thus resulting in a resistance of 23.7 kΩ from switch to switch. Effectively, the MAM capacitors "see" two of these resistances in parallel because there are two bias lines attached to each switch (Fig. 6.9). Additionally, where the bias lines feed underneath the CPW ground and contact the first switch in a phase bit, the capacitor Q is further reduced by another resistance in parallel with the two mentioned above. This small resistor is modeled as a 30 μm long section of resistive line because the Si-Cr line strongly couples to the ground plane by means of the air bridge over it. The effective resistance of this short section is 1.16 kΩ.

The Ka-band design has a static MAM capacitance, C_s of 66 fF and using a Q of 300 at 37.7 GHz, R_p = 19.2 kΩ. By adding the resistance (R_b) of two parallel bias lines in parallel with R_p, the Q is effectively reduced from 300 to 110. The reduction in Q is most dramatic in the 2 sections of the phase shifter (out of 21) where the bias lines feed the MEMS switches. In this case, the Q is effectively reduced to around 15 (for a single section per phase bit). This reduction in the capacitor Q increases the maximum measured loss (when all switches are down) from an ideal value of -1.1 dB to the measured value of -2.1 dB at 37.7 GHz.

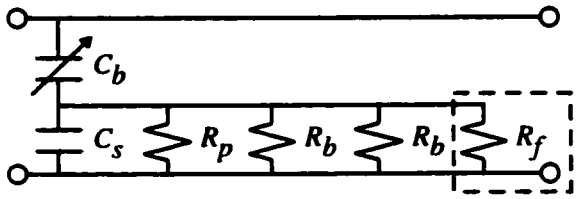


Figure 6.9: Lumped model of DMTL section showing points where MAM Q is effectively reduced by bias lines. R_p is the loss due to the MAM Q. R_b is the effective resistance of the long bias line connecting the switches and R_f is the effective resistance of the bias line feed, which is present at only 2 out of 21 sections of the 2-bit phase shifter.

6.6 Loss Components

There are three contributors to the insertion loss of the DMTL phase shifter: 1) line loss of the plated high-impedance line $R_t = 875\ \Omega$/m at 37.7 GHz), 2) line loss of the thin high-impedance line underneath the MEMS switch ($R_t = 1{,}035\ \Omega$/m at 37.7 GHz), and 3) Q loss of the MAM capacitors. The influence of each of these contributors on the measured design is summarized in Table 6.2. The plated and evaporated line losses are obtained from measured test structures. Each section of the Ka-band ($s = 400\ \mu$m) DMTL includes a 200 μm-long evaporated section underneath each MEMS switch. The capacitor Q loss is all encompassing, including the reduction in MAM Q due to the bias lines. The loss in Table 6.2 is split into two parts: the first part details loss in the 19 sections where there is a reduction in Q to 100-200 due to the bias lines. The second part details the loss in the remaining 2 sections where the Q is greatly reduced by the bias line feeds under the CPW ground plane. It should be noted that without bias lines, the loss of the DMTL phase shifter is essentially that of the plated and evaporated sections alone, as confirmed by simulations, because the Q of the MAM capacitors is quite high.

Loss Component	Ka-band design
Plated line loss	−0.51 dB
Evaporated line loss	−0.58 dB
19 Section Q loss	−0.39 dB
2 Section Q loss	−0.45 dB
Total max. loss	−1.93 dB
Measured max. loss	−2.10 dB

Table 6.2: Loss contributions (all switches down).

6.7 Conclusion

This chapter presents very low-loss Ka-band distributed phase shifters. The switch height was incorrect, and this moved the design frequencies from 30 GHz to 37.7 GHz. Still, the concept of using a very high Q MAM capacitor in series with a low-loss MEMS switch is proven to work very well, especially if the influence of bias lines is removed from the design. The results present state-of-the-art performance for true-time delay phase shifters at Ka-Band frequencies. The design can be easily scaled to 45 GHz, 60 GHz, or 77 GHz for satellite and covert communications, and radar systems.

CHAPTER 7

CONCLUSION AND FUTURE WORK

This thesis presented a detailed analysis and measurements of distributed MEMS phase shifters at X-band, Ku-band, and Ka-band, as summarized in Table 7.1. The measured results show that distributed MEMS phase shifters have state-of-the-art performance which is 3-4 times better than the best currently obtainable from solid-state phase shifters. It also proves that unlike solid-state designs, distributed phase shifters are quite wideband. The measured X-band CPW design has excellent performance, comparable to other non-distributed MEMS phase shifters and the measured Ka-band distributed phase shifter is the lowest loss measured phase shifter at this frequency band to date for all types of phase shifters.

The success of obtaining such low-loss phase shifters is attributable to two factors: 1) advances in MEMS switch fabrication and 2) static capacitor Q loss reduction. The MEMS switch fabrication advancement ultimately resulted in extremely flat membranes ($\pm$2,000 Å bowing over a 300 μm span) which have predictable up/down capacitance states and have a lifetime of millions of cycles. The metal-air-metal capacitors fabricated for these phase shifters have measured Q values of > 400 from 10-40 GHz which is a vast improvement over the originally built metal-insulator-metal capacitors having a Q of < 150 at 10 GHz. The major factor limiting even better performance of these phase shifters is the MEMS switch biasing lines, which have been shown to effectively lower the Q of the MAM capacitors greater than 400 to less than 200. By simply changing the layout of these bias resistors, or by using a higher resistivity material, the average insertion loss of the 2-bit

Freq. (GHz)	Bits	Design	Substrate	Average Loss (dB)	Return Loss (dB)	Accuracy (degrees)	Ref.
13.6	2	CPW	Quartz	−1.2	−12.5	±4	[19]
16.0	4	Microstrip	Silicon	−3.0	−9.5	±0.5	[18]
37.7	2	CPW	Quartz	−1.5	−11.5	±0.5	[19]

Table 7.1: Summary of the MEMS phase shifters contained in this thesis.

CPW phase shifters can improve to −0.75 dB at X-band and −0.85 dB at Ka-band.

The MEMS switches built today are capable of operating on the order of several billion cycles, have switching times of 1-10 μs, and handle 10-50 mW of RF power. The advantage to using MEMS switches in phase shifters is clear: there is a 6-8 dB system improvement at X-band over solid-state phase shifters in telecommunication and radar applications, and even greater improvements at millimeter-wave frequencies. These low-loss characteristics and low-power characteristics offer a clear advantage for modern low-power portable devices or for space-born applications. Future work in distributed phase shifters includes lowering the effect of bias lines on performance, which was discussed at length in this thesis, and the development of digital phase shifters at higher frequencies, such as 80-100 GHz. An example of such a design is presented in the next section.

7.1 A W-band Distributed MEMS Phase Shifter

Higher frequency distributed phase shifter designs require less spacing between the MEMS switches, but it is quite conceivable to build W-band (f_o = 80 GHz) designs with reasonably wide (35 μm) MEMS switch membranes and still have enough separation between the elements. Two examples of such designs, one based on a microstrip t-line and the other on a CPW t-line are presented here.

The microstrip design and the unit cell are shown in Figure 7.1. It is based on a 100 μm thick quartz substrate with an 83 Ω unloaded microstrip line and a MEMS switch membrane height of 1.5 μm (C_{bu} = 24 fF). The loaded impedance in the up and down-state positions is approximately 60 and 42 Ω, respectively. Twelve MEMS sections, each 195 μm long ($f_B \sim$ 150 GHz), results in approximately 186° of phase shift at 80 GHz.

The substrate is kept thin, and the Bragg frequency designed low to minimize coupling between the microstrip stubs, which are 160 μm apart (edge-to-edge). The performance of this design, obtained from Sonnet and ADS, is shown in Figure 7.2. As seen, the simulated phase shifter results in excellent performance. Considering that the electrical lengths of mm-wave lines are so short in comparison to the size of MEMS switches, this microstrip distributed design and the CPW design which follows may represent the only type (versus reflection or switched-line phase shifters) of MEMS phase shifter which results in a reliable mm-wave design.

Another example, based on a 98 Ω CPW t-line is shown in Figure 7.3. The MEMS switch membrane height is again 1.5 μm (C_{bu} = 27 fF) and loaded impedance in the up and down-state positions is approximately 60 and 42 Ω. Ten MEMS sections, each 195 μm long ($f_B \sim$ 150 GHz), results in approximately 175° of phase shift at 80 GHz. There are two less sections than the microstrip design because the unloaded impedance changed from 83 to 98 Ω. The MAM capacitor (C_s = 20 fF) is reasonably large enough to fabricate. It consists of a bottom metal tab which cuts into the ground plane and is 40 $\times$ 35 μm^2, surrounded by 10 μm gaps. The top MAM metal fills in the break of the ground plane, and can be fabricated from the same sputtered material used for the MEMS switch membrane. The performance of this design is shown in Figure 7.4. As seen, the performance is quite comparable to the microstrip design and is also excellent.

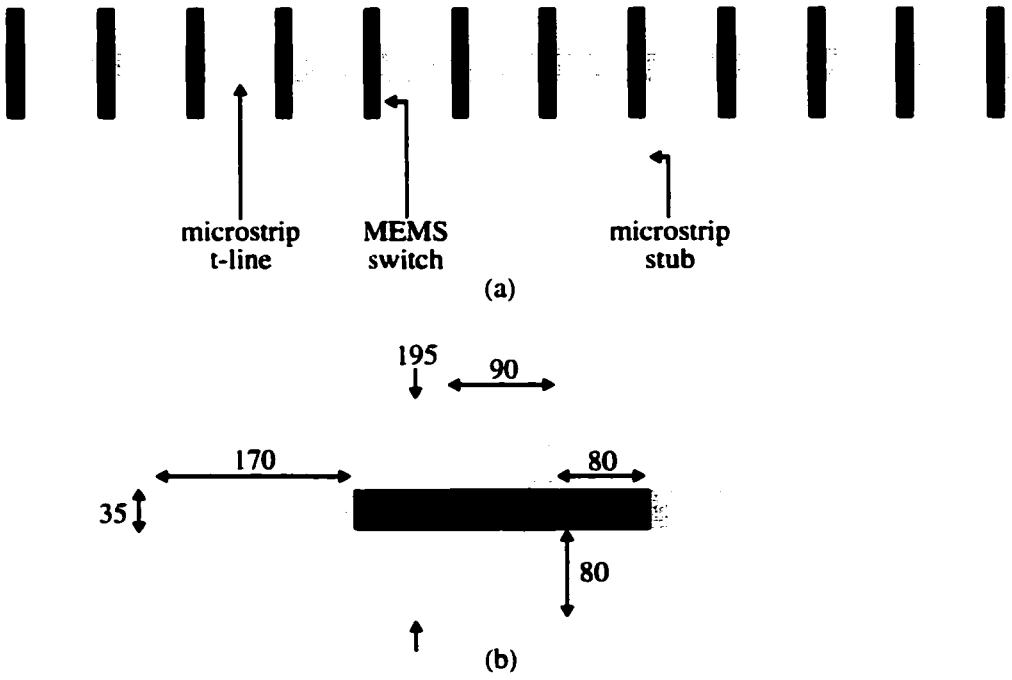
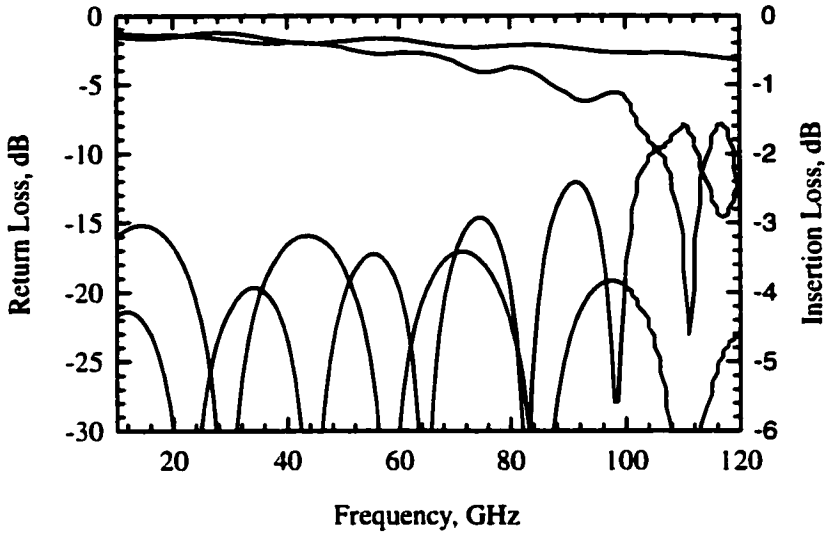
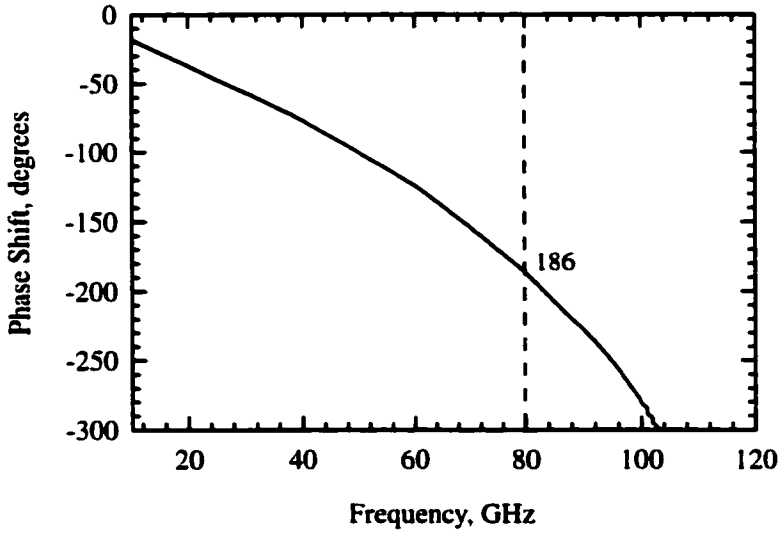


Figure 7.1: Drawing of a W-band, quartz substrate, microstrip t-line (W = 90 μm, h = 100 μm) based distributed MEMS phase shifter (a) and unit cell details (b). All dimensions in microns. Not shown is a dielectric layer which covers the microstrip line.



(a)



(b)

Figure 7.2: Simulated performance of a 12 section W-band microstrip distributed MEMS phase shifter.

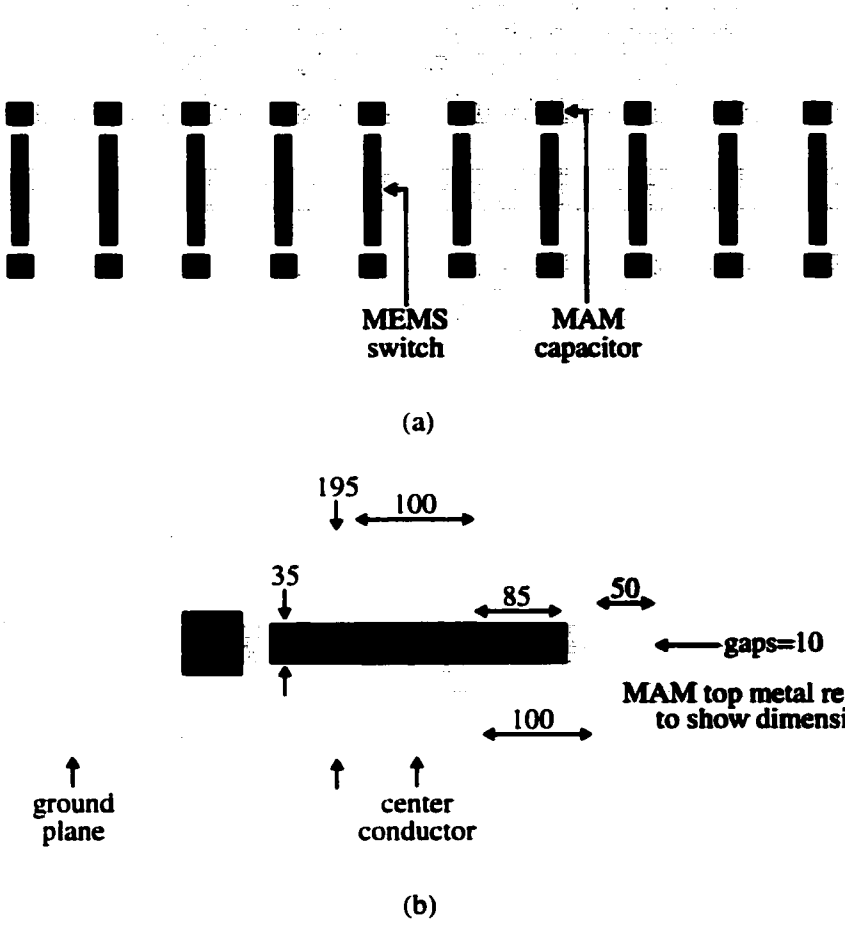
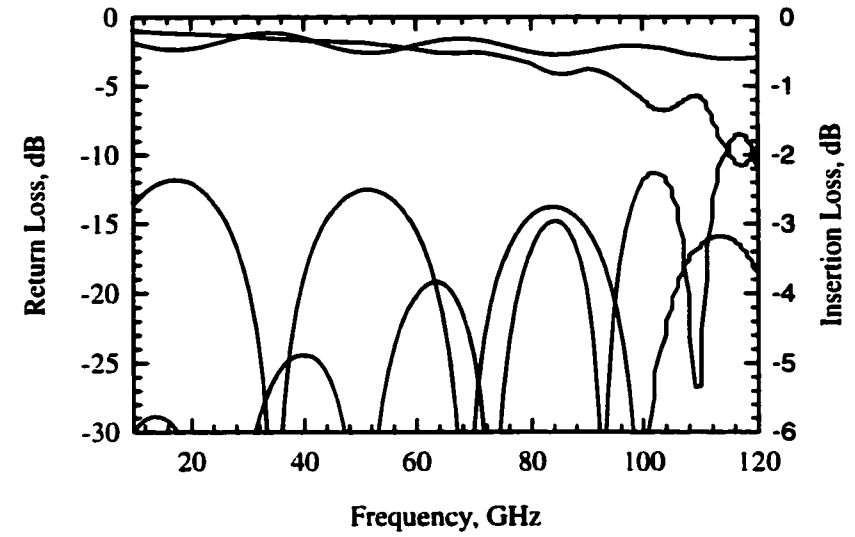
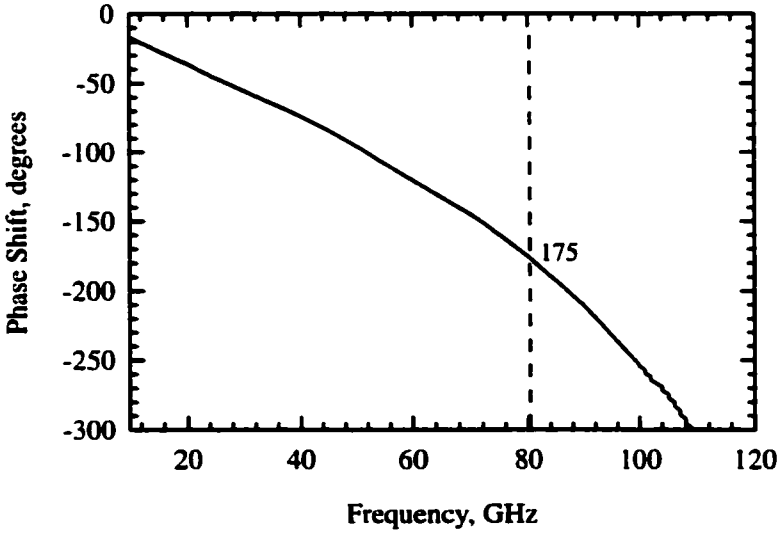


Figure 7.3: Drawing of a W-band, quartz substrate, CPW t-line (W = 100 μm, G = 100 μm) based distributed MEMS phase shifter (a) and unit cell details (b). All dimensions in microns. Not shown is a dielectric layer which covers the CPW center conductor.



(a)



(b)

Figure 7.4: Simulated performance of a 10 section W-band CPW distributed MEMS phase shifter.

APPENDICES

APPENDIX A

MICROSTRIP DESIGN EQUATIONS

$$Z_o = \begin{cases} \frac{\eta}{2\pi\sqrt{\epsilon_{re}}} \ln\left(\frac{8d}{W_e} + 0.25\frac{W_e}{d}\right) & (\mathrm{W_e/d} < 1) \\ \frac{\eta}{\sqrt{\epsilon_{re}}}\left[\frac{W_e}{d} + 1.393 + 0.667\ln\left(\frac{W_e}{d} + 1.444\right)\right]^{-1} & (\mathrm{W_e/d} > 1) \end{cases} \tag{A.1}$$

$$\frac{W_e}{d} = \begin{cases} \frac{W}{d} + \frac{1.25}{\pi}\frac{t}{d}\left(1 + \ln\frac{4\pi W}{t}\right) & (\mathrm{W/d} < \frac{1}{2\pi}) \\ \frac{W}{d} + \frac{1.25}{\pi}\frac{t}{d}\left(1 + \ln\frac{2d}{t}\right) & (\mathrm{W/d} > \frac{1}{2\pi}) \end{cases} \tag{A.2}$$

$$F(W/d) = \begin{cases} (1 + 12d/W)^{-0.5} + 0.04(1 - W/d)^2 & (\mathrm{W/d} < 1) \\ (1 + 12d/W)^{-0.5} & (\mathrm{W/d} > 1) \end{cases} \tag{A.3}$$

$$\epsilon_{re} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2}F(W/d) - \frac{\epsilon_r - 1}{4.6}\frac{t/d}{\sqrt{W/d}} \tag{A.4}$$

$$\epsilon_{re}(f) = \epsilon_r - \frac{\epsilon_r - \epsilon_{re}}{1 + (f/f_{50})^m} \tag{A.5}$$

$$f_{50} = \frac{f_k}{0.75 + [0.75 - (0.332/\epsilon_r^{1.73})]\,W/d} \tag{A.6}$$

$$f_k = \frac{c\,\tan^{-1}\left(\epsilon_r\sqrt{\frac{\epsilon_{re}-1}{\epsilon_r-\epsilon_{re}}}\right)}{2\pi d\sqrt{\epsilon_r - \epsilon_{re}}} \tag{A.7}$$

$$m = m_o m_c \tag{A.8}$$

$$m_o = 1 + \frac{1}{1+\sqrt{W/d}} + 0.32\left(\frac{1}{1+\sqrt{W/d}}\right)^3 \tag{A.9}$$

$$m_c = \begin{cases} 1 + \frac{1.4}{1+W/d}\left[0.15 - 0.235\exp\left(\frac{-0.45f}{f_{50}}\right)\right] & (\mathrm{W/d} < 0.7) \\ 1 & (\mathrm{W/d} > 0.7) \end{cases} \tag{A.10}$$

$$\alpha_c = \begin{cases} 1.38\ A\frac{R_s}{dZ_o}\frac{32-(W_e/d)^2}{32+(W_e/d)^2} & (\mathrm{dB/m})\ (\mathrm{W/d} < 1) \\ 6.1\times10^{-5}\ A\frac{R_s Z_o \epsilon_{re}(f)}{d}\left[W_e/d + \frac{0.667\ W_e/d}{W_e/d+1.444}\right] & (\mathrm{dB/m})\ (\mathrm{W/d} > 1) \end{cases} \tag{A.11}$$

$$\alpha_d = \begin{cases} 4.34\ \eta\sigma_d\frac{\epsilon_{re}(f)-1}{\sqrt{\epsilon_{re}(f)}(\epsilon_r-1)} & (\mathrm{dB/m})\ (\mathrm{W/d} < 1) \\ 27.3\frac{\epsilon_r}{\epsilon_r-1}\frac{\epsilon_{re}(f)-1}{\sqrt{\epsilon_{re}(f)}}\frac{\tan\delta}{\lambda_o} & (\mathrm{dB/m})\ (\mathrm{W/d} > 1) \end{cases} \tag{A.12}$$

$$A = 1 + \frac{d}{W_e}\left(1 + \frac{1.25}{\pi}\ln\frac{2B}{t}\right) \tag{A.13}$$

$$\sigma_d = \omega\epsilon_o\epsilon_r\tan\delta \tag{A.14}$$

$$B = \begin{cases} d & (\mathrm{W/d} > \frac{1}{2\pi}) \\ 2\pi W & (\mathrm{W/d} < \frac{1}{2\pi}) \end{cases} \tag{A.15}$$

$$\alpha_{total} = \alpha_c + \alpha_d \tag{A.16}$$

APPENDIX B

FABRICATION DETAILS

Listed here are the specific process steps used to fabricate the X-band and Ka-band MEMS phase shifters with MAM capacitors. Wafers are 3 inch in diameter, 500 μm thick, Dynasil 2000 double-side polished quartz wafers. The processing is done in a class 100 clean room at the University of Michigan.

B.1 Definition of Terms

The following definition of processing terms are taken from the thesis of Jeremy Muldavin [32] with minor changes.

1. Photo-lithographic patterning:

   (a) **Mask maker**: a device which selectively exposes small apertures on to the surface of photosensitive masking plate.

   (b) **Photomask**: a patterned layer of material that is opaque to light and is used to pattern photo-sensitive material on the surface of a wafer. A typical photomask consists of a glass plate with an opaque reflective chrome surface.

   (c) **Photoresist**: a light sensitive material that is spun on to the surface of a wafer. Depending on the polarity of the photoresist, when an area of the photoresist is exposed to UV light, it can either be removed or preserved while the unexposed areas are either preserved or removed, respectively, during the developing process.

Positive photoresist is removed after exposure and negative photoresist remains after exposure.

(d) **Image reversal photoresist**: a special type of negative photoresist that reverses its polarity after a second exposure. This process creates a special profile or lip at the edge of the resist pattern that is advantage for use in lift-off techniques.

(e) **Mask aligner**: a device used to align a photomask to an existing pattern on a wafer. After the wafer and mask are aligned, UV light transfers the pattern from the mask to the photoresist. The mask aligners used for this work are contact, meaning the mask and wafer are in direct contact.

(f) **Developer**: a chemical solution that will selectively remove exposed or unexposed areas of photoresist, depending on the polarity of the resist. These developers are often matched to a specific type and brand of photoresist.

(g) **Soft bake**: heating step to partially remove solvent from photoresist before aligning and exposing a wafer. It reduces stickiness of the photoresist layer, which is necessary for contact alignment.

(h) **Hard bake**: heating step to solidify photoresist after the it has been developed. This process makes the photoresist more resistant to chemical etchants.

2. Material deposition:

(a) **Electron beam evaporator**: a device which uses a high energy beam to evaporate materials form a source crucible. The evaporated materials are ejected from the surface of the crucible and deposited in a thin film of the surface of a wafer. Common source materials include: Au, Al, Ti, Cr, Ag, Pt, NiCr, and Cu. Theses materials are often deposited in a lift-off process where photoresist protects areas of the wafer from direct deposition. The undesired metal deposited on the photoresist is then removed when the photoresist is stripped from the wafer in acetone.

(b) **Sputtering tool**: a device which uses a high energy plasma to etch particles

from a source target and then redeposit the particles on to the surface of a wafer. The source particles are ejected from the plasma in random directions, ensuring a conformal coating of a surface. The plasma, a mixture of charged particles and electrons, can be excited using a direct current (DC) or a radio frequency (RF) source. DC plasmas are often used to deposit metals such as Au, Al, Ti, Cr, and Cu. RF plasmas are sued to deposit metal and dielectric materials such as Si, SiO_2, SiN, SiCr, and TaN.

(c) **PECVD**: (plasma enhanced chemical vapor deposition) a technique that uses an RF plasma with specific gaseous mixtures to deposit materials on the surface of a wafer. This process is often used to deposit dielectric films such as SiO_2 and Si_3N_4.

3. Etching techniques:

(a) **Wet chemical etching**: wet chemical agents used to selectively etch a material from the surface of a wafer. Common etchants include Au etchant, Ti etchant, Al etchant, HF and BHF to etch oxide and Ti films.

(b) **Plasma etching (RIE etching)**: a technique that uses an RF plasma and chemical etching to remove materials from the surface of a wafer. This technique is often used to etch SiO_2, Si_3N_4, or organic (such as PMMA) layers.

4. Release:

(a) **Sacrificial layer**: a layer of material that separates a top layer from an underlying layer. The sacrificial layer is removed later to create an air gap between the layers.

(b) **CPD**: (critical point dryer) a system which allows the drying of wet released MEMS membranes without collapse due to surface tension. The critical point system consists of a cooled chamber that fills with liquid CO_2, mixing with other wet chemicals which are purged from around the MEMS devices. The liquid CO_2 filled chamber is then pressurized and heated to the critical point of CO_2, in which CO_2 exists as a liquid and a vapor state simultaneously. Pressure

is released slowly from the chamber, drying the MEMS wafer without passing through a liquid phase.

5. Chemicals used:

   (a) **Acetone**: a strong chemical solvent capable of completely removing or stripping most photoresist materials from a wafer or mask.

   (b) **IPA**: (isopropoyl alcohol) is a solvent used to clean the surface of a wafer. It is often used to remove traces of acetone and photoresist after stripping the resist in acetone.

   (c) **PMMA**: an organic photoresist from MicroChem Corporation for e-beam lithography.

   (d) **PG remover**: a proprietary solvent from MicroChem Corporation for removing PMMA.

   (e) **PRS2000**: a proprietary photoresist solvent.

   (f) **HF**: Hydrofluoric acid.

   (g) **BHF**: Buffered hydrofluoric acid.

B.2 Specific Processes Steps

B.2.1 Wafer Clean

1. Soak in chomerge for 1 minute.
2. Rinse in DI water for 2 minutes.
3. Spray with acetone and IPA.
4. Dry with nitrogen (N_2) air gun.
5. Dry 2 minutes on a 130 °C hot plate.

B.2.2 SiCr Bias Layer Deposition and Etch

1. RF sputter from SiCr target, argon environment with 10% nitrogen, 7 mT, 700 W, 20 minutes, for a 1,500 Å thick layer.
2. Spin photoresist 1827 for 30 seconds at 3 krpm.
3. Soft bake 1.5 minutes on a 105 °C hot plate.
4. Align mask and expose for 15 seconds at 20 mW/cm^2..
5. Develop in MF 351 for 1 minute.
6. Rinse in DI water for 2 minutes.
7. Dry with (N_2) air gun.
8. Hard bake 1.5 minutes on a 130 °C hot plate.
9. Wet etch SiCr in BHF for 3.5 minutes, swirling the etchant.
10. Rinse in DI water for 2 minutes.
11. Strip photoresist in hot PRS2000.
12. Rinse in DI water and spray with IPA.
13. Dry with nitrogen (N_2) air gun.

B.2.3 First Metallization Layer (Lift-Off)

1. Spin image reversal photoresist AZ 5214 for 30 seconds at 2 krpm.
2. Soft bake 1.5 minutes on a 105 °C hot plate.
3. Align mask and expose for 2.5 seconds at 20 mW/cm^2.
4. Hard bake 1.5 minutes on a 130 °C hot plate.
5. Flood expose for 30 seconds at 20 mW/cm^2.
6. Develop in AZ 327 developer for 1 minute.

7. Rinse in DI water for 2 minutes.
8. Dry with nitrogen (N_2) air gun.
9. Examine edge profile under microscope.
10. Evaporate Ti/Au/Ti 1,000/8,000/1,000 Å thick.
11. Soak in acetone overnight for metallization liftoff.
12. Spray with IPA
13. Lightly swab with hot PRS2000.
14. Rinse in DI, spray with IPA, and dry with nitrogen (N_2) air gun.

B.2.4 Nitride Deposition and Etch

1. PECVD deposit Si_3N_4 for 12 minutes for 2,000 Å thick layer. SiH_4 (100 sccm) NH_3 (10 sccm) He (900 sccm) N_2 (990 sccm) 400 °C 700 mT 100 W.
2. Spray with acetone and IPA.
3. Dry with nitrogen (N_2) air gun.
4. Dry for 2 minutes on a 130 °C hot plate.
5. Spin photoresist 1827 for 30 seconds at 3 krpm.
6. Soft bake 1.5 minutes on a 105 °C hot plate.
7. Align mask and expose for 15 seconds at 20 mW/cm^2..
8. Develop in MF 351 for 1 minute.
9. Rinse in DI water for 2 minutes.
10. Dry with (N_2) air gun.
11. Hard bake 1.5 minutes on a 130 °C hot plate.

12. RIE etch dielectric in CF_4 (40 sccm) and O_2 (1 sccm) plasma at 100 mT and 100 W for 6 minutes.

13. Strip photoresist in hot PRS2000, lightly swabbing.

14. Rinse in DI water and spray with IPA.

15. Dry with nitrogen (N_2) air gun.

B.2.5 Sacrificial Layer Deposition

1. Spin adhesion promoter HMDS for 45 seconds at 1.5 krpm.

2. Spin PMMA (950K, 6% in anisole solvent) for 45 seconds at 1.5 krpm.

3. Bake PMMA for 7 minutes in a 170 °C oven.

4. Spin another layer of PMMA for 45 seconds at 1.5 krpm (2 layers = 1.5 μm).

5. Bake PMMA for 23 minutes in a 170 °C oven.

6. Evaporate 2,500 Å Ti.

7. Spin photoresist 1827 for 30 seconds at 3 krpm.

8. Soft bake 1.5 minutes on a 105 °C hot plate.

9. Align mask and expose for 15 seconds at 20 mW/cm^2..

10. Develop in MF 351 for 1 minute.

11. Rinse in DI water for 2 minutes.

12. Dry with (N_2) air gun.

13. Skip hard bake.

14. Etch Ti in 1:10 HF:DI (a quick dip etch).

15. Rinse in DI water for 2 minutes.

16. Dry with nitrogen (N_2) air gun.

17. Flood expose for 30 seconds at 20 mW/cm^2.

18. Develop in MF 351 for 1 minute.

19. Rinse in DI water for 2 minutes.

20. Dry with (N_2) air gun.

21. Preclean RIE for 20 minutes.

22. Etch PMMA in 50 mT 100 SCCM O_2 250 W plasma for 14 minutes, turning plasma RF power on and off in 1.5 and 1 minute cycles, respectively.

23. Etch Ti in 1:10 HF:DI (a quick dip etch).

24. Rinse in DI water for 2 minutes.

25. Dry with nitrogen (N_2) air gun.

B.2.6 MEMS Membrane Sputtering

1. DC sputter from Ti target, argon environment, 7mT, 550 W, 1 minute, for a 100 Å thick layer.

2. DC sputter from Au target, argon environment, 9.5mT, 0.5 A, 30 minutes, for a 8,500 Å thick layer.

B.2.7 Electroplating

1. Spin photoresist 1827 for 30 seconds at 3 krpm.

2. Soft bake 1.5 minutes on a 105 °C hot plate.

3. Align mask and expose for 15 seconds at 20 mW/cm^2..

4. Develop in MF 351 for 1 minute.

5. Rinse in DI water for 2 minutes.

6. Dry with (N_2) air gun.

7. Skip hard bake.

8. Electroplate gold on exposed 1.5 cm^2 area of wafer at 19 mA for 30 minutes, resulting in 4 μm thick layer.

B.2.8 MEMS Membrane Etch

1. Flood expose for 30 seconds at 20 mW/cm^2.

2. Develop in MF 351 for 1 minute.

3. Rinse in DI water for 2 minutes.

4. Dry with (N_2) air gun.

5. Anneal 2 minutes on a 105 °C hot plate.

6. Anneal 2 minutes on a 130 °C hot plate.

7. Anneal 2 minutes on a 150 °C hot plate.

8. Anneal 3 minutes in a 170 °C oven.

9. Cool.

10. Spin photoresist 1827 for 30 seconds at 3 krpm.

11. Soft bake 1.5 minutes on a 105 °C hot plate.

12. Align mask and expose for 15 seconds at 20 mW/cm^2..

13. Develop in MF 351 for 1 minute.

14. Rinse in DI water for 2 minutes.

15. Hard bake 1.5 minutes on a 130 °C hot plate.

16. Wet etch Au in gold etchant for 6 minutes.

17. Wet etch Ti in 1:10 HF:DI (a quick dip etch).

18. Rinse in DI water for 2 minutes.

19. Release membranes in hot PG remover, overnight.

20. Rinse in DI water 5 minutes.

21. Rinse in IPA 5 minutes.

22. Dry wafer in CPD.

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