Fully Micromachined Power Combining Module for Millimeter-Wave Applications

by

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To my family.....

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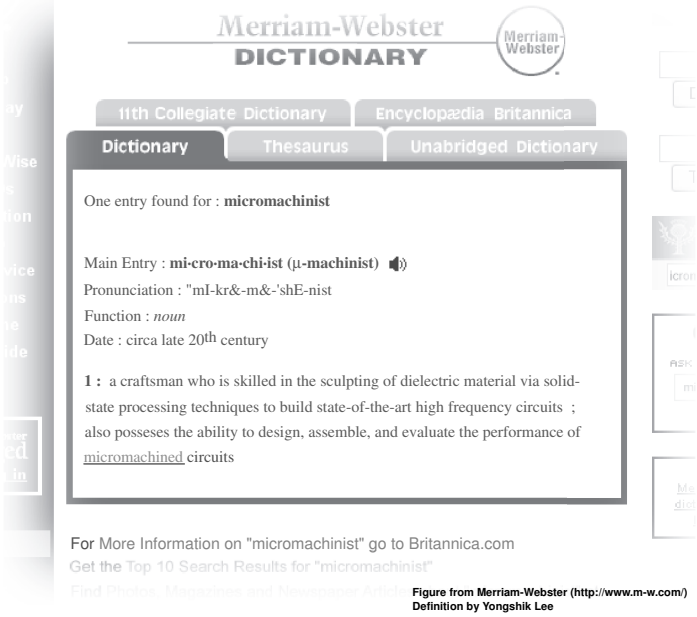

Figure from Merriam-Webster (http://www.m-w.com/)
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CHAPTER 1

Introduction

1.1 Motivation

THE THZ spectrum, loosely defined as the frequency range from 0.1 THz to 10 THz [1], holds a great deal of promise for many applications including high-resolution environmental sensing, high-resolution biological imaging, wide-bandwidth satellite communications, and is widening to the military and commercial fields. However, while advanced technologies in its neighboring bands, microwave and optical bands, have been well-developed, research in the THz region has been limited. This is mainly due to the fact that compact, economical, reliable, and high-power sources in the THz region are lacking.

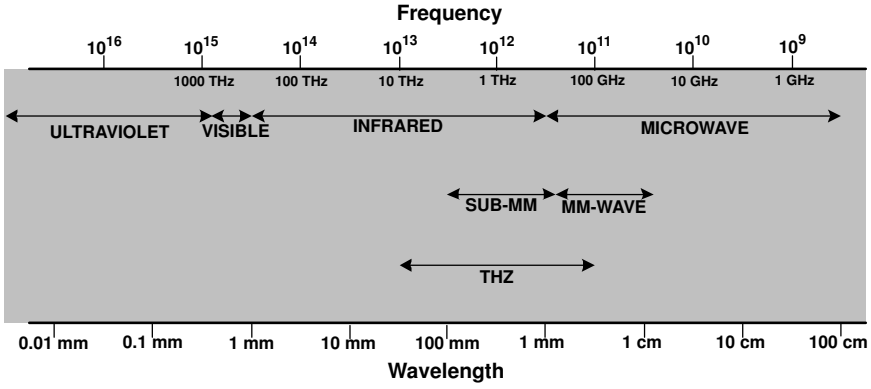


Figure 1.1: Electromagnetic spectrum.

1.1.1 Millimeter-wave, Submillimeter-wave, and THz Sources

At present, the most commonly used RF sources for the microwave and THz spectrum are solid-state sources and microwave tube sources. Compared with the microwave tube sources, solid-state sources have the advantages of small size, low cost, and compatibility with microwave integrated circuits [2], and so are more preferred. However, as the operating frequency of semiconductor solid-state devices increases, their power-handling capacity is reduced due to the reduction in the size of the devices. Hence, although there has been an extensive effort to develop solid-state sources for the millimeter and submillimeter regime, vacuum tube-type sources such as klystrons and gyrotrons have been the mainstay of microwave power sources at frequencies above 100 GHz, especially for high-power applications. Unfortunately, these vacuum-type sources are large in size and weight, require high-voltage supplies for operation, and have low reliability and short life time.

A considerable amount of effort has been carried out to improve the power and frequency performances of semiconductor solid-state oscillators based either on three-terminal devices or two-terminal devices to serve as sources at frequencies above 100 GHz. An output power of 1 μW for a DC to RF efficiency of 0.014 % was demonstrated at 213 GHz with a Microwave Monolithic Integrated Circuit (MMIC) High Electron Mobility Transistor (HEMT) oscillator based on AlInAs/GaInAs/InP technology [3]. Currently, two-terminal devices are more promising candidates than the three-terminal devices for RF power generation in the THz spectrum. For instance, an output power of 34 mW was delivered at 193 GHz [4], 1.1 mW at 315 GHz using state-of-the-art InP Gunn devices [5], and over 9 mW of output power at 202GHz with an outstanding phase noise of -94dBc/Hz with GaAs Tunnel Injection Transit-time (TUNNET) diodes [6].

An alternate approach, rather than depending on all-solid-state local oscillators for high-power and high-frequency signal generation, is to use a frequency multiplier or a chain of multiplier stages driven by RF frequency oscillators at medium millimeter-wave frequencies. This is the most common approach to RF power generation above *D*-band

(110 GHz - 170 GHz) since it has the advantage of using lower frequency oscillators or amplifiers which, compared with currently available high-frequency oscillators, have superior frequency stability, accuracy, and phase noise performances [7]. For instance, a high-performance InGaAs/InAlAs/AlAs heterostructure barrier varactor (HBV's) tripler has been reported that produces an output power 9.55 mW with a conversion efficiency of 10.7 % at 247.5 GHz [8]. A demonstration of a 1.126 THz monolithic GaAs Schottky diode membrane tripler, driven by a 400 GHz solid-state chain composed of power amplifiers followed by two tunerless frequency doublers, with an output power of 80 μW at room temperature, 195 μW at the ambient temperature of 120 K, and as high as 250 μW at the ambient temperature of 50 K has been reported [9].

Although these are excellent results, they still suffers from low power levels and thus are not suitable for medium to high-power applications, such as radar systems. One possible solution to overcome this limitation of solid-state sources is to combine the output power of numerous solid-state oscillators, amplifiers, or frequency multipliers. Theoretically, a large amount of RF power can be generated by combining a number of sources. However, the amount of power that can be combined is limited due to factors such as loss in the combining circuit, isolation between each sources [2], combining efficiencies, and circuit size limitations.

There are various techniques of power combining. Device level combining, which is to design circuits with multiple devices in a series or parallel configuration rather than a single configuration, is generally limited in the number of devices that can be efficiently combined. Power combining can also be realized at the circuit level. The Wilkinson power combiner is an example of a nonresonant circuit level power combining scheme, which offers better frequency performance compared with resonant circuit level power combining schemes such as those utilizing rectangular or circular resonant cavities. Multiple power combining schemes can be used, both device level combining and circuit level combining, to achieve higher efficiency and higher output power levels. However, the efficiency of

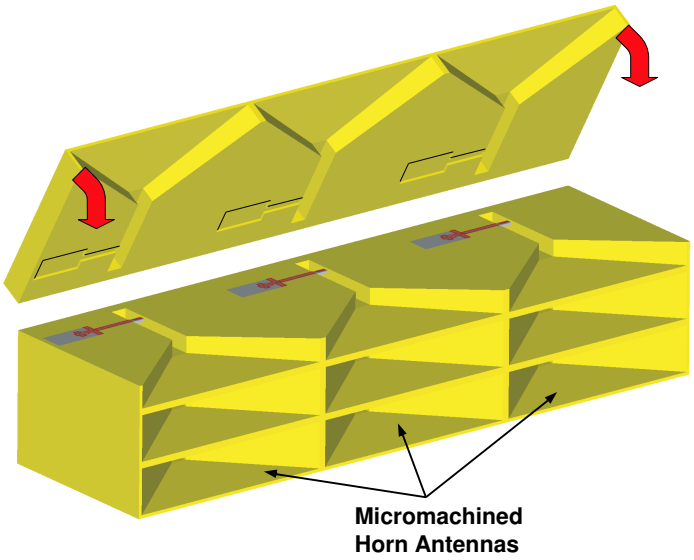
circuit level combining decreases dramatically and eventually becomes impractical as the number of components increases, since then most of the semiconductor area will be used for the passive matching and combining circuitry.

Spatial or quasi-optical power combining provides enhanced combining efficiency by coupling the output powers of each component in a single stage to large-diameter guided beams or waveguide modes [10]. In this approach, complicated lossy network can be eliminated, which provides the ability to achieve higher combining efficiencies. Moreover, quasi-optical power combining schemes become more attractive at higher frequencies since denser device integration is feasible due to the shorter wavelengths [10], and thus higher efficiency and output power level can be achieved. For instance, using a quasi-optical power combining scheme, 24 mW of power was delivered at the output frequency of 1 THz from a 144-element grid of GaAs varactor-diode frequency doublers with bow-tie antennas [11].

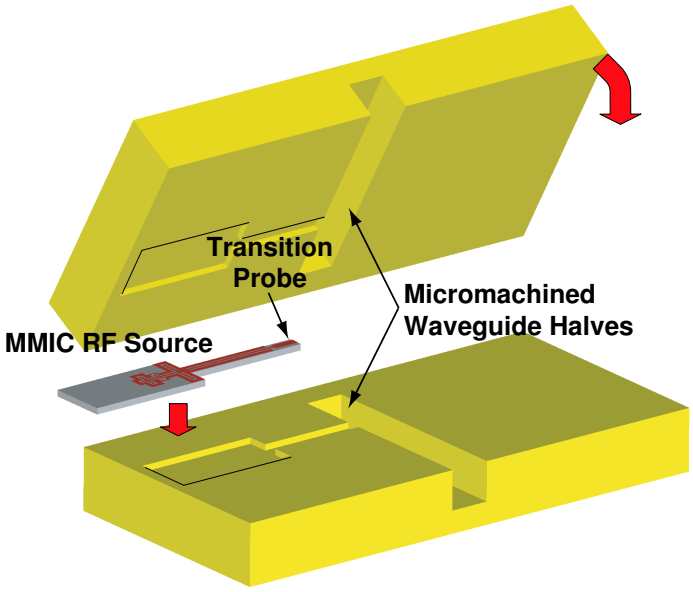
1.1.2 Micromachined Power Combining Module

The proposed waveguide-based quasi-optical power combining system [12] is shown in Figure 1.2. Each module that constitutes the power combining system consists of 3 components - a solid-state Microwave Monolithic Integrated Circuit (MMIC) RF source such as frequency multipliers or oscillators, a transition circuit between the output of this planar circuit and a micromachined waveguide, and a section of micromachined waveguide. The output signal of the planar solid-state component is coupled to the waveguide via the transition circuit, which is then delivered to the output of the waveguide. The waveguide can then be used to feed a highly directive micromachined horn antenna. A number of these modules can be simply combined together in an effort to deliver combined, therefore higher power levels into free space.

The advantage of the proposed power combining system is that output powers of Finite Ground Coplanar (FGC) line-based MMIC's are combined using a waveguide system. Compared with microstrip lines, FGC lines are easy to fabricate since the necessity to met-



(a) Micromachined power combining system.



(b) Power combining module.

Figure 1.2: Proposed fully micromachined power combining system (a) and module that constitutes the power combining system (b). An example of a 3×3 array power combining modules is shown in this figure. Each module consists of a finite ground coplanar line-based MMIC RF source, a transition probe, and a silicon micromachined waveguide section. The waveguide can then be used to feed a highly directive micromachined horn antenna.

allize backside of the wafer is eliminated and that the electrical characteristics are relatively insensitive to substrate thickness. Moreover, its uniplanar nature allows straightforward integration of series and shunt elements, diodes for example, without the need for via holes which can provide additional parasitics as well as fabrication complexity. All of these are a strong advantage over microstrip lines especially for MMIC's. MMIC's have the advantages of small size, and modern integrated circuit (IC) techniques allow fabrication of such circuits in large quantities at low cost.

Waveguides are bulky and difficult to integrate other circuitry, especially at lower frequencies where the dimensions of waveguides are on the order of centimeters. However, the loss in waveguides is significantly lower than the loss in planar transmission lines, and its power handling capacity is well beyond that of FGC lines, microstrip lines, and other types of planar transmission lines. In addition, waveguides can optimize the circuit performance with incorporated tuners such as backshorts and can be used to directly feed highly directive horn antennas. The proposed power combining system takes such advantages of waveguides to combine the output power of individual modules at the low-loss waveguide system level, rather than at the lossy planar transmission line level. The difficulty and high cost of conventionally machining waveguides for submillimeter and THz spectrum due to their small size and therefore small dimensional tolerance can be considerably reduced by means of silicon micromachining technology. The waveguides can be fabricated in a "split-block"manner, using various cost-effective silicon micromachining techniques, and still provide excellent performance.

The transition from the output of the MMIC to the waveguide is another critical element of the proposed power combining system. The transition utilizes a novel micromachined *E*-plane probe that is fed by extending the center conductor of an FGC line and inserted into the waveguide. Effective transition between the FGC line and the micromachined waveguide is important since it has a substantial effect on the overall efficiency of the power combining system.

The biggest challenge in realizing the proposed power combining system lies in the difficulty of 2D-integration of individual modules and also in phase locking MMIC output signals with suitable power dividing circuits. In addition, the design of a micromachined horn antenna array is another key factor for the overall performance of the power combining system.

1.2 Dissertation Overview

The main object of this dissertation is development of the proposed fully micromachined power combining module. Module components - GaAs monolithic frequency multipliers and fully micromachined FGC line to waveguide transitions - are first investigated. A complete power combining module can be developed by integrating the two heterogeneous components.

Chapter 2 presents millimeter-wave high efficiency monolithic GaAs frequency multipliers. A relatively simple yet effective means to reduce the loss in the passive circuitry of monolithic circuits and therefore to improve the frequency multiplier efficiencies is demonstrated. Simulated as well as experimental results are provided. The frequency multipliers developed in this chapter are used as the RF source in the power combining module presented later in this dissertation.

Chapter 3 describes the development of transitions between 50 Ω finite ground coplanar lines and micromachined waveguides. A simple yet promising technique to develop micromachined waveguides via dry etching silicon is introduced and utilized to fabricate waveguides. A free-standing transition probe that provides the potential of such transitions to be applicable well into the submillimeter-wave and THz range, is also presented. The transition and the micromachined waveguide is the passive part of the power combining module presented later in this dissertation. Thus, development of effective transition is an essential part for successful demonstration of the module.

Chapter 4 demonstrates the fully micromachined power combining module. It integrates, in a unique micromachined arrangement, the high efficiency monolithic GaAs frequency multipliers developed in Chapter 2 and the FGC line to micromachined diamond waveguide developed in Chapter 3. A number of the demonstrated modules can be simply combined together to produce higher output power levels. Therefore demonstrated power combining module will seek as a promising candidate of an efficient power source for high-frequency high-power application sources.

Chapter 5 summarizes the accomplishments in this dissertation and introduces other high-frequency applications that the multi-functionality of the demonstrated power combining scheme can be utilized in.

CHAPTER 2

High Efficiency *W*-band GaAs Monolithic Frequency Multipliers

2.1 Introduction

HIGH-FREQUENCY signals can be generated either by using high frequency oscillators, or by multiplying signals from lower frequency sources. The performance of oscillators, in terms of stability, accuracy, and phase noise, becomes worse as the operating frequency is increased [7]. This makes frequency multiplication a preferred method for generating high frequency signals. As a result, frequency multipliers are one of the critical components in millimeter and submillimeter wireless communication systems.

Traditionally, frequency multipliers have been based on Schottky barrier diodes. Frequency multipliers utilizing novel diodes such as SBV (Single-Barrier-Varactor) have been reported [13], yet the results are only promising. Recently, frequency multipliers utilizing various types of transistors such as pHEMT's and FET's also have shown high efficiency performance in millimeter and submillimeter region with their potential to amplify the output signals [7, 14, 15]. However, due to the advantages of Schottky diode-based multipliers over transistor-based multipliers such as higher power handling capacity, improved stability, and better frequency response [16], Schottky diodes still remain as preferred nonlinear

devices for frequency multipliers in millimeter and submillimeter systems.

The most popular type of millimeter-wave and submillimeter-wave frequency multipliers have been of waveguide-based [17–19]. Waveguide circuits have low loss, high Q, and the ability to optimize the performance with incorporated tuners such as backshorts. However, as the operating frequency is increased, conventional machining of metal rectangular waveguides becomes more difficult and thus costly. Specifically for the waveguide-based multipliers, the mount structures become more complex to design and fabricate as the operating frequency increases [20].

An alternate but still competitive approach is monolithic microwave integrated circuits (MMIC's). MMIC frequency multipliers have more loss and lower Q than waveguide-based frequency multipliers, and it is nearly impossible to include tuning elements. However, MMIC's are often preferable to bulky-waveguide circuits due to their small sizes and the possibility of low-cost fabrication in large quantities using integrated circuit (IC) fabrication techniques. In addition, MMIC's allow much better reproducibility of performance than waveguide-based frequency multipliers.

Useful diode-based MMIC multipliers have been reported recently. Chen *et al*. successfully demonstrated a diode-based MMIC multiplier with an output power of 65 mW and an efficiency of 25 % at 94 GHz using microstrip lines [21]. Brauchler *et al*. demonstrated output power of 93 mW at 80 GHz [20] and Papapolymerou *et al*. demonstrated an output power of 115 mW at 74 GHz with 4 diodes [22], both based on finite ground coplanar(FGC) lines. However, MMIC frequency multipliers have suffered from relatively low efficiencies compared to their waveguide-based counterpart.

One of the major limiting factors for achieving high efficiencies in MMIC's is the loss in the passive circuitry. For instance, transmission lines are used extensively not only to transfer the input and output signals but also to match the impedances of active devices to those of the input and output ports, with open/short stubs. Therefore, the efficiency of a multiplier can benefit from reducing the loss in the transmission lines.

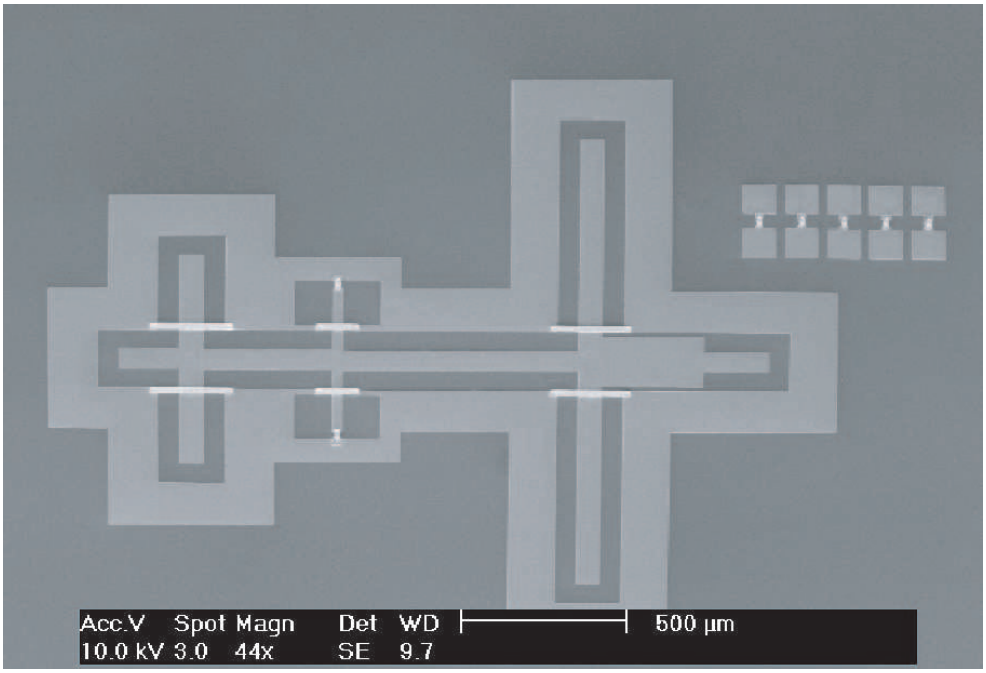


Figure 2.1: Scanning electron micrograph of a fabricated MMIC frequency multiplier with GaAs Schottky barrier planar diodes of input Q=2. Shown in the top right corner are test diodes.

This chapter presents high efficiency diode-based MMIC frequency multipliers that have comparable performance to the waveguide-based counterpart in *W*-band. Passive circuitry with lower loss has been adopted to improve the multiplier efficiencies. First, Section 2.2 will discuss basic Schottky barrier diode theory. Extracting diode DC parameters from experimental *C/V* and *I/V* curve is also shown for a Schottky barrier diode used as the nonlinear device for the frequency multipliers presented. In section 2.3, a practical method of reducing the loss in FGC lines is provided and its experimental results are discussed. Then the design and fabrication of two types of MMIC frequency multipliers are described in Sections 2.4 and 2.5. Section 2.6 is devoted to the measurement setup and procedures. In Section 2.7, the evaluated performance of the fabricated frequency multipliers is presented. Finally, conclusion will follow in Section 2.8. The frequency multipliers discussed in this chapter will be used as the MMIC RF source in the power combining module presented in Chapter 4.

2.2 Schottky Barrier Diode Theory

Signal generation plays an important role in high frequency communications systems. A variety of stable, low noise sources are available below 100 GHz, but most higher frequency systems require harmonic multipliers in order to obtain the required output power and frequency [23]. Due to their advantages such as higher power handling capacity, improved stability, low noise characteristics, and superior frequency response especially at high frequencies, Schottky (metal-to-semiconductor) barrier diodes have been the most common nonlinear device for millimeter and submillimeter-wave frequency multipliers. Reactive multipliers can be realized when the Schottky barrier diodes are used as varactors, nonlinear voltage-controlled capacitors. Compared to resistive multipliers where Schottky barrier diodes are used as resistive diodes, reactive multipliers have a strong advantage of theoretical efficiency of 100%, restricted only by the losses in the diodes.

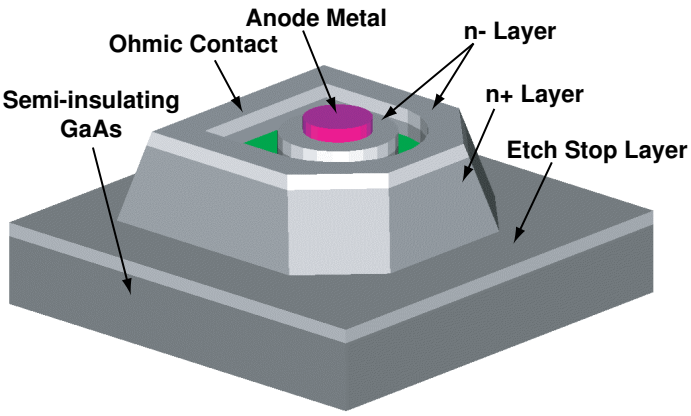


Figure 2.2: Schottky barrier diode used for the *W*-band frequency multipliers in this chapter.

2.2.1 Junction Capacitance

A diagram of the Schottky barrier diode used for the multipliers in this chapter and in Chapter 4 is shown in Fig. 2.2. The diode shown in this figure is a planar disk type commonly used in MMIC applications. The n^- layer had a doping level (N_d) of 1×10^{17} /cm^3 and a thickness of 4700 Å. The n^+ layer had a doping level of 5×10^{18} /cm^3 and a thickness of 2.5 μm. The ohmic contact is formed on top of the n^+ layer with GaAs alloyed nickel-germanium-gold layers. The size and shape of the anode are selected to give the appropriate combination of junction capacitance and series resistance for the intended application. Due to the difference in work functions of anode metal and *n*-type semiconductor (GaAs), a Schottky barrier type junction is formed when the anode that consists of Ti/Pt/Au metal layers is placed on the semiconductor surface. Electrons are transferred from the semiconductor to the anode until equilibrium is obtained and a single Fermi level characterizes both the metal and the semiconductor [24]. Hence, a depletion region is formed within the semiconductor at the metal interface, which is depleted of mobile carriers (electrons). Having lost electrons, the *n*-type semiconductor will be charged positively with respect to the anode at thermal equilibrium.

The depth of the depletion region (x_d) can be controlled with an external bias voltage

and is obtained by solving Poisson's equation :

$$x_d = \sqrt{\frac{2\varepsilon_r}{qN_d}(\phi_i - V_a)} \quad \text{[cm]}, \tag{2.1}$$

where ε_r is the permittivity of the semiconductor, q is the electron charge (1 eV=1.6×10^{-19} J), N_d is donor density (doping level) of the n^- layer, ϕ_i is the built-in voltage or the voltage drop across the depletion region (space charge region) at equilibrium, and V_a is the bias voltage applied to the anode with the semiconductor grounded [24]. The built-in voltage ϕ_i is simply the difference between the metal work function and the electron affinity of the semiconductor.

The space charge Q_s per unit area in the semiconductor is

$$Q_s = qN_d x_d = \sqrt{2q\varepsilon_r N_d(\phi_i - N_d)} \quad \text{[C/cm}^2\text{]} \tag{2.2}$$

and the capacitance per unit area under small-signal ac conditions can be calculated by using Equation 2.2:

$$C = \left|\frac{\partial Q_s}{\partial V_a}\right| = \sqrt{\frac{q\varepsilon_r N_d}{2(\phi_i - V_a)}} = \frac{\varepsilon_r}{x_d} \quad \text{[F/cm}^2\text{]}. \tag{2.3}$$

If this equation is solved for the total voltage across the junction, we obtain :

$$(\phi_i - V_a) = \frac{q\varepsilon_r N_d}{2C^2}. \tag{2.4}$$

Equations 2.4 indicates that a plot of the square of the reciprocal of the small-signal capacitance ($1/C^2$) versus the reverse bias voltage should be a straight line. The slope of the straight line can be used to obtain the doping level (N_d) in the semiconductor, and the intercept of the straight line with the abscissa should equal to the built-in potential, ϕ_i [24],

$$N_d = \frac{-2}{q\varepsilon_r} \times \frac{1}{\text{slope}}. \tag{2.5}$$

Shown in Fig. 2.3 is a plot of a $1/C^2$ as a function of DC bias for a test diode with an anode area of 0.389 mm^2. This diode was fabricated on the same wafer as the multipliers, presented later in this chapter, for the purpose of calculating the doping level. The multiplier diodes can be used for such a measurement. However, considering the fabrication tolerances and that the value of the anode area squared (capacitance per unit area, [F/cm^2]) is considered in the calculation, the results are more consistent when obtained using a test diode with relatively large anode area. The measurements were taken with an HP 4285A Precision LCR Meter for the bias levels from -9 V up to -1 V with an increment of 1 V. Also shown is a fitted curve used to find the exact slope and to extract the built-in potential ϕ_i from the intercept of this line with the positive V_a axis where no measurements were taken. The doping level was calculated to be 1.08 $\times 10^{17}/\text{cm}^3$ which agrees well with the value (1×10^{17} /cm^3) provided by the vendor. The calculated built-in potential ϕ_i was 0.71 V.

The capacitance per unit area (Equation 2.3) can also be expressed as [24, 25]

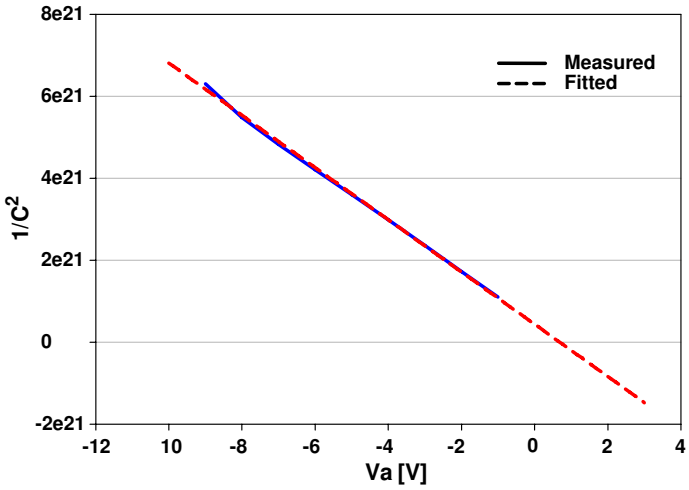


Figure 2.3: Plot of $1/C^2$ versus applied bias for a test diode with an anode area of 0.389 mm^2.

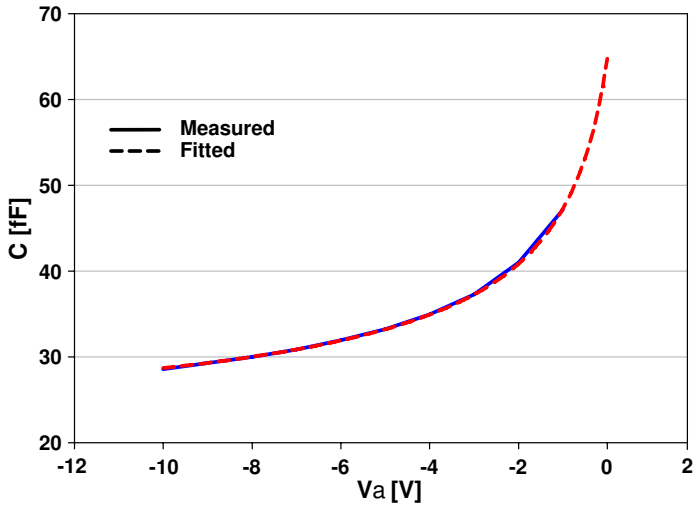


Figure 2.4: Plot of measured capacitance versus applied bias for a Q=3 diode with an anode area of 65.3 μm^2.

$$C = \frac{C_o}{\sqrt{1 - \frac{V_a}{\phi_i}}} \quad [\text{F/cm}^2], \tag{2.6}$$

where C_o is the zero bias capacitance and can be obtained from Equation 2.2,

$$C_o = C|_{V_a=0} = \sqrt{\frac{q\varepsilon_r N_d}{2\phi_i}}. \tag{2.7}$$

Taking into account the parasitic capacitances from diode fingers and probing pads, the total capacitance of a Schottky barrier diode can be expressed as :

$$C_t = C_p + \frac{C_o}{\sqrt{1 - \frac{V_a}{\phi_i}}} \quad [\text{F/cm}^2], \tag{2.8}$$

where C_p is the parasitic capacitance.

Shown in Fig. 2.4 is a plot of measured capacitance versus applied bias for a Q=3 diode used for the multipliers presented later in the chapter. The diode had an anode area of 65.3

μm^2 and was fabricated on the same wafer as the large test diode in Fig. 2.3. The built-in potential ϕ_i of 0.71 V obtained from Fig. 2.3 was used to obtain the zero-bias capacitance of 48.3 fF and and the parasitic capacitance of 16.5 fF.

2.2.2 *I/V* Characteristics

The dependence of current on applied bias voltage (V_a) of a Schottky barrier metal-semiconductor junction can be obtained by the thermionic emission-diffusion theory. The total current density can be approximated by [24, 25]

$$J = J_{sat}\left[\exp\left(\frac{qV_a}{\eta kT}\right) - 1\right] \quad [\text{A/cm}^2], \tag{2.9}$$

where J_{sat} is the reverse-saturation current density, η is the diode ideality factor, k is Boltzmann's constant (1.37×10^{-23} J/K), and T is the temperature in Kelvin. J_{sat} can be obtained by extrapolating the current density from the log-linear region to V_a=0. An expression for J_{sat} is [25]

$$J_{sat} = A^{**}T^2\exp\left(\frac{q\phi_i}{kT}\right), \tag{2.10}$$

where A^{**} is the modified Richardson constant and is approximately 4.4 A/cm$^2\cdot$K^2 for GaAs. ϕ_i is the the barrier height, or the built-in potential.

The diode ideality factor η in Equation 2.9 can be obtained by taking the logarithm of the same equation :

$$\eta = \frac{q}{kT}\frac{\partial V_a}{\partial(\ln J)}, \qquad \text{for} \quad V_a \gg \frac{kT}{q}. \tag{2.11}$$

The diode ideality factor accounts for unavoidable imperfections in the junction and for other secondary phenomena that thermionic emission theory cannot predict [25]. The value of η represents departures from an ideal Schottky junction (η=1) and actual Schottky

barriers on moderately doped *n*-type GaAs usually have η values within the range of 1.0 to 1.25. However, it can depart substantially from unity when the doping is increased or the temperature is lowered [26].

The reverse-saturation current density J_{sat} and the diode ideality factor η of the q=3 diode are calculated from the its *I/V* curve in the next section.

2.2.3 Parasitic Series Resistance

It should be noted that Equation 2.9 is an approximated *I*/*V* characteristic of the junction of a Schottky barrier diode and does not include the voltage drop across other parts of the diode. In Schottky barrier diodes, the epitaxial layer is never fully depleted of charge in normal operation even at the highest reverse voltages [25]. Consequently, there is always some undepleted epitaxial material between the depletion and the layers below. This represents a parasitic resistance in series with the diode junction. High electron mobility in GaAs allows lower series resistance to be achieved with relatively lighter doping. However, this series resistance is an important loss mechanism in diodes for mixers and frequency multipliers and thus must be considered.

Shown in Fig. 2.5 is the high frequency equivalent circuit of a Schottky barrier diode.

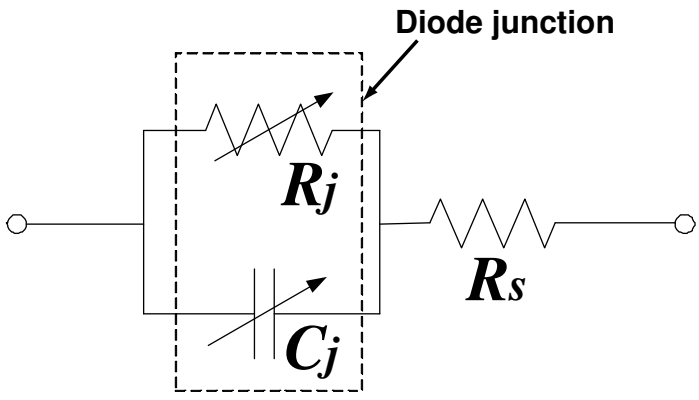


Figure 2.5: Equivalent circuit for a Schottky barrier diode. The components in the dotted box represents the diode junction.

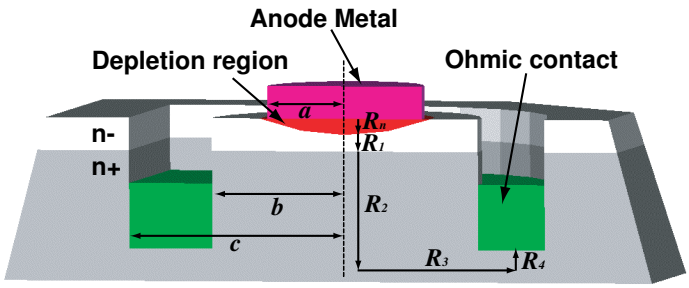


Figure 2.6: Profile of the Schottky barrier diode shown in Fig. 2.2

It consists of three nonlinear elements : the junction capacitance (C_j) in parallel with the junction resistance (R_j) associated with the generation-recombination current, diffusion current, and surface leakage current, and the parasitic series resistance (R_s). However, R_s is usually approximated as a linear element even when the diode is operated as a varactor with a reverse bias, in which case the series resistance shows nonlinearity and varies somewhat more with applied bias [25].

Fig. 2.6 shows the profile of the Schottky barrier diode shown in Fig. 2.2. In such a mesa-type diode where both contacts (anode and cathode) are on the top surface of the chip, the current through the device flows down from the anode and spreads laterally around the base of the mesa before flowing out of the cathode [21]. The current flow path is shown by the arrows in the right half of the figure. Assuming that the anode metal has an infinite conductivity and that the current density is confined within a skin depth (δ), total series resistance (R_s) of a Schottky barrier diode can be broken into the components, R_n, R_1, R_2, R_3, R_4. R_n is the spreading resistance of the undepleted n^- layer, and R_4 is the contact resistance. $R_1 \sim R_3$ are the spreading resistance of the n^+ layer and are divided based on the current path shown in Fig. 2.6. The analytical equations for each series resistance component are as follows [21, 27, 28]

$$R_n = \frac{t - x_d}{\sigma_n \pi a^2}, \tag{2.12}$$

$$R_1 = \frac{\delta_s}{2\pi\sigma_s a^2}, \tag{2.13}$$

$$R_2 = \frac{1}{4\pi\sigma_s\delta_s}, \tag{2.14}$$

$$R_3 = \frac{1}{2\pi\sigma_s\delta_s}\ln\left(\frac{b}{a}\right), \tag{2.15}$$

$$R_4 = \frac{\rho_m\rho_s}{\rho_m\delta_s+\rho_s\delta_m}\left[\frac{1}{2\pi}\ln\left(\frac{c}{b}\right)+\frac{\delta_s}{\rho_s}\left(AI_o(\beta c)+BK_o(\beta c)\right)+\frac{\delta_m}{\sigma_m}\left(AI_o(\beta b)+BK_o(\beta b)\right)\right], \tag{2.16}$$

where

$$A = \frac{1}{2\pi\beta\Delta}\left[\frac{\rho_m K_1(\beta b)}{\delta_m c}+\frac{\rho_s K_1(\beta c)}{\delta_s b}\right],$$

$$B = \frac{1}{2\pi\beta\Delta}\left[\frac{\rho_m I_1(\beta b)}{\delta_m c}+\frac{\rho_s I_1(\beta c)}{\delta_s b}\right],$$

$$\Delta = I_1(\beta c)K_1(\beta b) - I_1(\beta b)K_1(\beta c),$$

$$\beta = \sqrt{\frac{1}{\rho_c}\left(\frac{\rho_m}{\delta_m}+\frac{\rho_s}{\delta_s}\right)},$$

and t is the thickness of the n^- epitaxial layer, x_d is the depth of the depletion region, ρ_c is the ohmic contact resistance. δ_s and δ_m are the skin depths, ρ_s and ρ_m are resistivities, σ_s and σ_m are conductivities, in the substrate and metal regions, respectively. The a, b, and c dimensions can be found in Fig. 2.6. $I_n(\cdot)$ and $K_n(\cdot)$ are modified Bessel functions of the first and second kind, respectively. The total series resistance of the Schottky diode is then

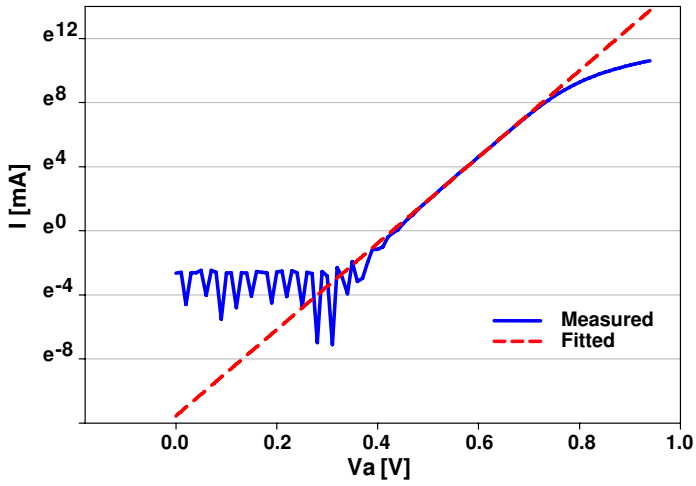


Figure 2.7: Measured *I/V* curve for a Q=3 diode with an anode area of 65.3 μm^2.

$$R_s = R_n + R_1 + R_2 + R_3 + R_4. \tag{2.17}$$

Thus, the series resistance of a Schottky barrier diode can be calculated using the above equations. For a Q=3 Schottky barrier diode with a=4.56 μm, b=8.7 μm, c=12 μm, t=4700 Å, and $N_d = 1.08 \times 10^{17}$, the estimated series resistance is approximately 1.6 Ω.

Fig. 2.7 shows a measured *I/V* characteristic for the same Q=3 diode, plotted on semilogarithmic axes. The diode *I/V* curve was measured using an HP 4155A Semiconductor parameter analyzer and a pair of Cascade Microtech tungsten probes with 2.4 μm radius tips. The reverse-saturation current I_s and the diode ideality factor η can be found from the slope of the fitted line and Equations 2.10 and 2.11 : $I_s = J_s \times$ (Anode area)=615 fA and η=1.19. The parasitic series resistance R_s can also be found from the measured and fitted curves in Fig. 2.7. As is seen from this figure, the curve deviates from a straight line at the high voltage end because of the voltage drop across the R_s. The series resistance value can be obtained from the difference (ΔV) between the actual bias voltage and the expected bias voltage (found from the fitted curve) for a certain current level (I_1) beyond the deviating point

$$R_s = \frac{\Delta V}{I_1}. \tag{2.18}$$

The R_s of the q=3 diode is found to be 5.6 Ω, which is higher than the value calculated from Equation 2.17. The measured R_s of 5.6 Ω includes the contact resistance between the probe tip and the on-wafer gold pad. This resistance can be obtained from the *I/V* measurements of a back to back probe tip to gold pad contact, and the average contact resistance is found to be 0.9 Ω per contact. Thus, it is reasonable expectation that the actual R_s of the Schottky barrier diode is 3.8 Ω. This series resistance value is still higher than the value (1.6 Ω) calculated using Equation 2.17. The difference of about 2 Ω between the theoretical experimental values of the series resistance is largely due to the resistance coming from other diode components such as anode metal, ohmic contact, and ohmic metal. The Equation 2.17 assumes that the anode metal has an infinite conductivity (zero resistivity) and the contacts between the metal and semiconductor are ideal. In addition, the employed ohmic contact (325/250/640 Å of Ni/Ge/Au annealed at 405°C for 40 sec.) is known to have an average contact resistivity of $5.0 \pm 2.5 \times 10^{-7}$ Ω · cm^2 [29]. Thus, it can be said that the measured series resistance of 3.8 Ω is in reasonable agreement with the theoretical value of 1.6 Ω.

When a Schottky barrier diode is operated as a varactor under a reverse bias condition, a large capacitance variation can be achieved. From Equation 2.3, this implies that the depletion region depth (x_d) varies considerably over the voltage applied across the junction. Since the series resistance R_s consists largely of the undepleted epitaxial layer (R_1 in Fig. 2.6), it is expected that there is also a great variation of R_s. Therefore, the assumption that the series resistance is linear may not be valid for varactors [25].

When the junction capacitance C_j in Fig. 2.5 and the series resistance R_s are obtained, the quality factor of the diode can be calculated. The quality factor, Q, of a diode is the ratio of energy stored to energy dissipated within the diode and is a measure of the efficiency of a varactor [26]

$$Q = \frac{\omega C_j R_j}{1 + \omega^2 C_j^2 R_j R_s}. \tag{2.19}$$

Since the junction resistance R_j is on the order of kΩ range and is much larger than series resistance R_s, the above equation can be simplified at high frequencies as :

$$Q \approx \frac{1}{\omega C_j R_s} = \frac{X_{in}}{R_{in}}, \tag{2.20}$$

where R_{in} and X_{in} are the real and imaginary parts of the diode input impedance at a frequency ω.

For a given bias, Q varies as $\omega C_j R_j$ at low frequencies and as $1/\omega C_j R_s$ at high frequencies [26]. This is due to the fact that C_j is fixed when the bias is fixed, and to the fact that there is a great difference between the values of R_j and R_s. Diodes operating at high frequencies are subject to additional phenomena that can affect their performance [25]. For example, the skin depth (δ) effects will have an effect on parasitic series resistance R_s.

A Schottky barrier diode can be modelled as a one-sided step junction which is a highly asymmetrical (abrupt) junction [24]. The dopant concentration on one side of the junction (metal) is much higher than on the other side (semiconductor), and thus the depth (x_d in Fig. 2.6) of the depletion region on the heavily doped region (metal) is negligible when compared to that of the lightly doped region (semiconductor). The breakdown voltage of a Schottky barrier diode can therefore be expressed as [26]:

$$V_B \cong 60(E_g/1.1)^{3/2}(N_d/10^{16})^{-3/4}, \tag{2.21}$$

where E_g is the bandgap of the semiconductor material at room-temperature, which is 1.12 eV for silicon and 1.424 eV for GaAs at 300K.

The cutoff frequency f_c is a figure of merit for a diode, and is traditionally calculated from its DC parameters [25] :

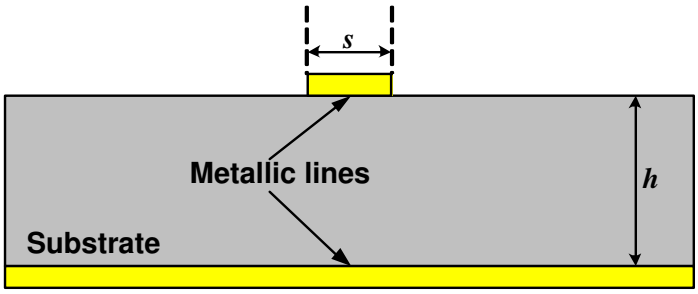
$$f_c = \frac{1}{2\pi\left(R_s + R_j\right)C_{jo}} \approx \frac{1}{2\pi R_s C_{jo}} \tag{2.22}$$

2.3 Loss Control in Finite Ground Coplanar Lines

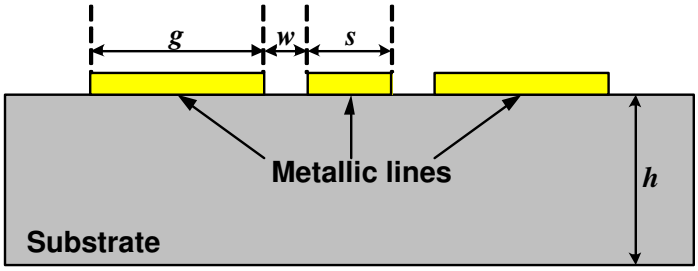
Geometries of the two most popular planar transmission lines used in MMICs are shown in Fig.2.8. Owing to several advantages over the conventional microstrip lines, finite ground coplanar (FGC) lines have become one of the most widely used transmission lines in today's millimeter and submillimeter applications. Among the advantages is a better control of loss in the transmission lines. One way to reduce the loss in a microstrip line is to reduce the current density on the conductor by making the conductor width (s in Fig. 2.8(a)) wider. This reduces the ohmic loss in the microstrip line, therefore the overall loss. However, in order to account for the decrease in the characteristic impedance (Z_o) due to a wider conductor width, the thickness of the substrate (h in Fig. 2.8(a)) has to be increased accordingly. This may not be feasible, especially at very high frequencies where thin substrates are required to prevent higher order modes.

In FGC lines, most of the electromagnetic field is concentrated in the aperture between conductors (w in Fig. 2.8(b)). Thus, dielectric loss in FGC lines can be reduced by removing the dielectric in these apertures [30]. However, removing the dielectric from the slots also affects other transmission line characteristics such as effective permittivity(ε_{eff}) and thus its characteristic impedance and electrical length. Therefore the relationship between the amount of dielectric removed from the slots and the transmission line characteristics needs to be explored when designing such FGC lines. In addition, micromachining grooves in the slots requires an additional process step which may not be compatible with the other process steps, or which may be feasible only for certain substrate materials.

On the other hand, reducing the ohmic loss can be a more practical way to reduce the overall loss of FGC lines. Ohmic loss can be reduced by widening the center conductor



(a) Microstrip line geometry.



(b) Finite Ground Coplanar(FGC) line geometry.

Figure 2.8: Geometries of the two most popular planar transmission lines used in MMICs.

width (s in Fig. 2.8(b)) thereby reducing the current density. In fact, this is a more effective method for reducing the loss of FGC lines, since ohmic loss is the dominant factor of FGC line loss [31, 32]. The changes in transmission line parameters such as the characteristic impedance due to a wider center conductor width can be compensated simply. Provided that the ground plane width (g in Fig. 2.8(b)) and the dielectric thickness (h in Fig. 2.8(b)) can be considered to be infinite, the characteristic impedance (Z_o) of an FGC line, found by a quasi-static analysis using conformal mapping, is expressed as [33]

$$Z_o = \frac{30\pi}{\sqrt{\varepsilon_{eff}}} \frac{K'(k)}{K(k)} \quad [\Omega], \tag{2.23}$$

where

$$\varepsilon_{eff} = 1 + \frac{\varepsilon_r + 1}{2},$$

$$k = \frac{s}{s+2w},$$

and $K(\cdot)$ and $K'(\cdot)$ are the complete elliptic integrals of the first kind and its complement, respectively. Thus for FGC lines, k=s/(s+2w) is the dominant factor that determines the characteristic impedances. Therefore, if the w/s ratio is kept the same by increasing the widths of the slots at the same time and by the same ratio that the center conductor width is increased, the characteristic impedance will remain nearly the same. Thus, it can be said that controlling the loss in FGC lines is relatively easier compared to microstrip lines.

There are limitations. As mentioned above, as the center conductor is widened to reduce the ohmic loss, the slot widths needs to be widened in order to maintain the w/s ratio constant, therefore the characteristic impedance constant. At the same time, to ensure a single mode of operation, the entire width of an FGC line has to be less than half a wavelength in the dielectric at the highest frequency of operation [34]. This condition sets an upper limit on center conductor and slot dimensions. This upper limit, in turn, sets a threshold on how much line loss can be improved from increased dimensions. In addition, due to the wider center conductor slot widths, the circuit size may become too large to implement. Reducing the ground plane widths maybe a solution to such a problem, but such truncation can reduce the characteristic impedance of the lines [33, 35], and/or introduce additional loss [32].

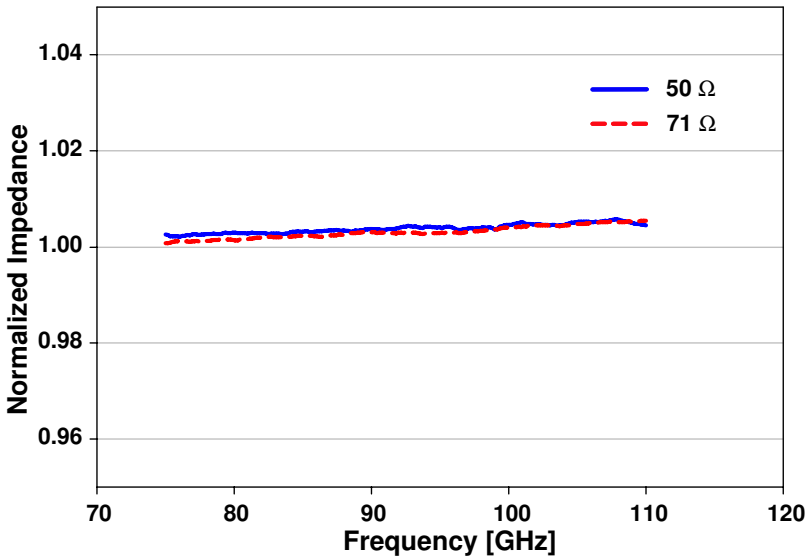
The relationship between FGC line dimensions and the loss was experimentally verified. Two FGC lines with characteristic impedances of 50 Ω are used for this experiment. The FGC line with narrower dimensions are the FGC lines that have been used extensively by our group at University of Michigan for high frequency circuits. The FGC line with wider dimensions are scaled versions of these. In an effort to reduce the ohmic loss, the width of the center conductor was widened by 40%. At the same time, width of the slots was widened also by 40% so as to maintain the same w/s ratio and thus the characteristic impedance of the line. Additional two FGC lines with characteristic impedances of 71 Ω

were also investigated in this experiment. The ground plane widths of scaled FGC lines were carefully chosen to minimize the effect on characteristic impedances, and to ensure single mode of propagation. The dimensions of FGC lines used in this experiment are summarized in Table 2.1. Thru-reflect-line(TRL) calibration standards of the four FGC lines were fabricated on a 625 μm semi-insulating GaAs wafer and tested in *W*-band. The lines were patterned with 500 Å of titanium and 1 μm of gold via standard lift-off process. Measurements were performed with an HP8510C vector network analyzer and a set of ground-signal-ground model 120 GGB Picoprobes. On-wafer calibration was achieved through the use of MultiCal [36], a TRL protocol. In Fig. 2.9(a), the measured characteristic impedance of the wider 50 Ω FGC line, normalized to the measured characteristic impedance of the narrower 50 Ω line, is plotted in the solid line. The measured characteristic impedance of the wider 71 Ω FGC line, normalized to the measured characteristic impedance of the narrower 71 Ω line is plotted in the dotted line. The results show that the changes in impedances due to the changes in dimensions were less than 1% over the entire *W*-band, for both 50 Ω and 71 Ω FGC lines.

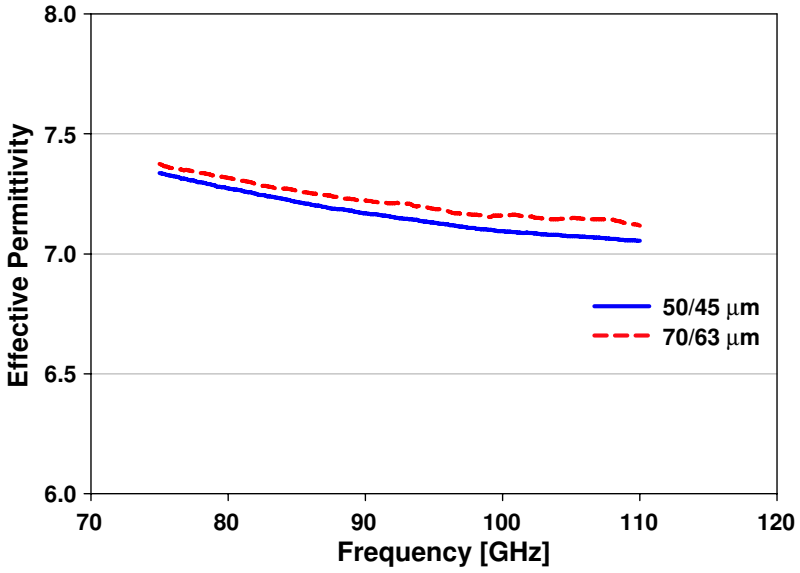
Shown in Fig. 2.9(b) are the real parts of the effective permittivity of the two 50 Ω FGC lines tested. The fact that the effective permittivity is nearly constant indicates that the propagation along both lines are quasi-TEM modes and are nearly dispersionless. As can be seen from this figure, the effective permittivities of the two lines show little difference

Table 2.1: Dimensions of 50 Ω and 71 Ω FGC lines on semi-insulating GaAs substrate used to experimentally verify the relationship between FGC line dimensions and the associated loss.

Z_o	Center [μm]	Slot [μm]	Ground [μm]
50 Ω	50	45	160
	70	63	140
71 Ω	20	80	260
	28	112	230

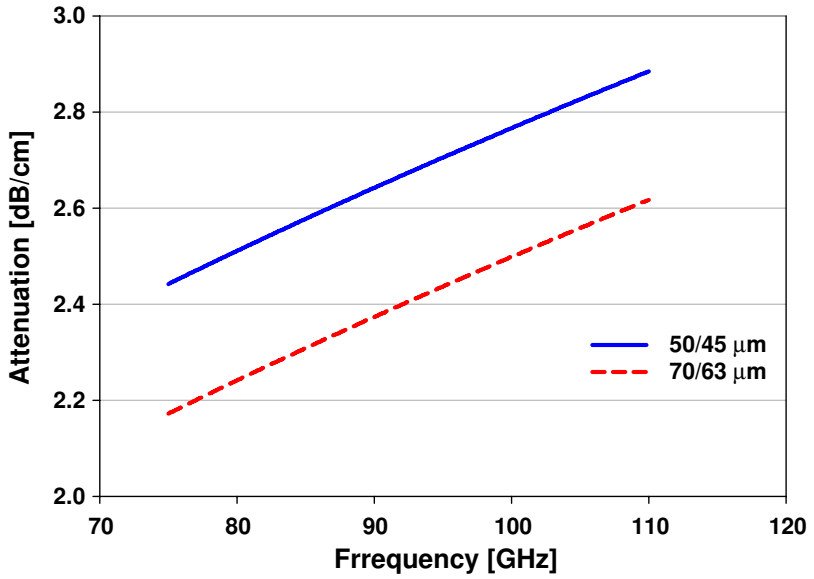


(a) Normalized Impedances

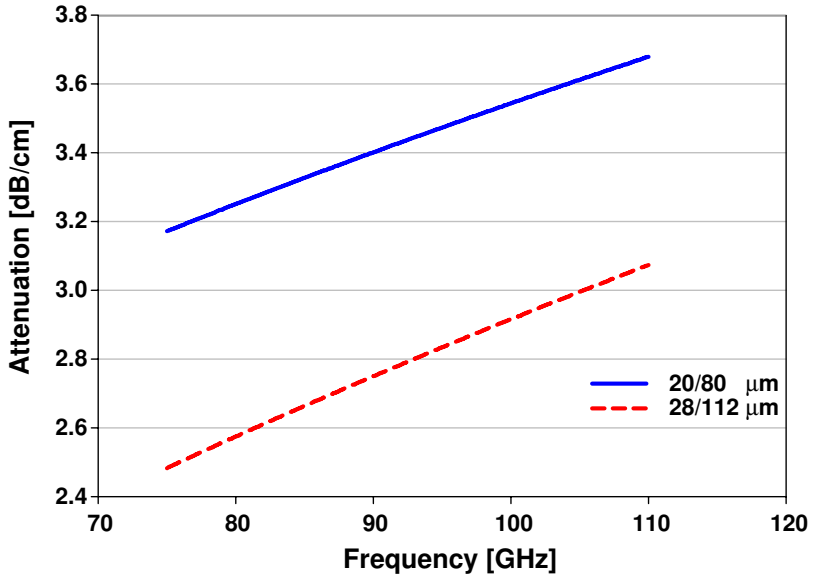


(b) Effective Permittivity

Figure 2.9: Experimental results for comparison of FGC lines in Table 2.1. (a) Impedances of 50 Ω and 71 Ω FGC lines with 40 % wider center conductor and slot widths, normalized to the impedances of original FGC lines. (b) Effective permittivity of the two 50 Ω lines tested.



(a) 50 Ω FGC lines



(b) 71 Ω FGC lines

Figure 2.10: Attenuation [dB/cm] curves of the 50 Ω and 71 Ω FGC lines. The curves were fitted to $\sqrt{f}$ functions to provide clearer illustration.

in *W*-band.

These results, together with the fact that no mode other than the dominant mode is excited over the entire *W*-band, implies that the tested FGC line pairs are electrically indistinguishable in this frequency range.

Shown in Fig. 2.10 are the attenuation curves of the tested FGC lines, obtained from MultiCal. Since loss in FGC lines are mainly ohmic, the curves were fitted to $\sqrt{f}$ functions, to illustrate the differences in loss more clearly. As can be seen in this figure, 40% wider center conductor width reduces the overall loss by about 0.3 dB/cm for the 50 Ω FGC line and about 0.7 dB/cm for the 71 Ω FGC line across the whole *W*-band. For example, for the 50 Ω line, the loss was reduced from 2.5 dB/cm to 2.2 dB/cm at 80 GHz. For the 71 Ω line, the loss was reduced from 3.3 dB/cm to 2.6 dB/cm at 80 GHz.

Since FGC lines with various impedances are used extensively in MMIC designs not only to transfer the input and output signals but also to match the impedances of active devices to those of the input and output ports, the efficiencies of MMIC's can benefit from reducing the loss in these FGC lines.

2.4 Multiplier Design

Monolithic frequency multipliers were designed with a pair of GaAs Schottky barrier planar diodes as the nonlinear devices. Shown in Fig. 2.11 is a block diagram of the designed monolithic frequency doublers. The planar diode pair is connected from the signal lines to the ground planes of FGC lines, in a shunt configuration, which is not an easily available configuration in circuits based on microstrip lines. The two matching and isolation networks should be designed so that the maximum power of the fundamental frequency is delivered to the diodes and at the same time, the maximum second harmonic power output from the diodes is delivered to the output ports.

A nonlinear multiple-reflection program that includes velocity saturation, doping, ava-

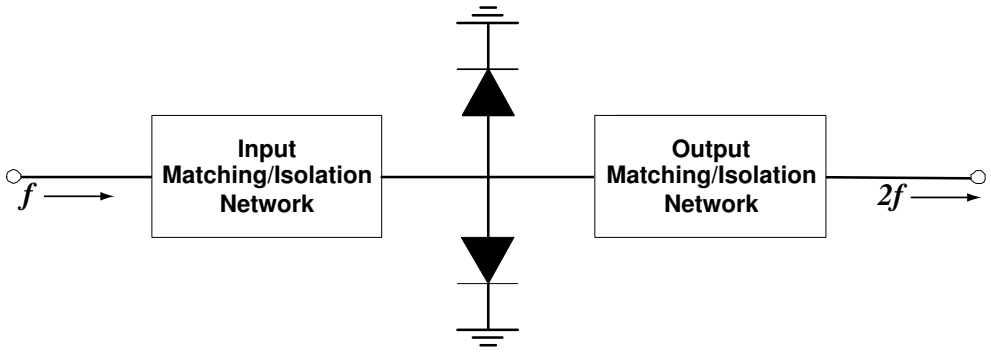


Figure 2.11: Block diagram of the investigated MMIC frequency doublers of shunt diode configuration.

lanche breakdown voltage, and mode of operation, based on the code described by East *et al.* [37,38] was used to design the circuit so that the diodes have input *Q*'s of two and three. The input *Q* of a diode determines the operating mode. Multipliers with lower *Q* diodes are more resistive and thus have relatively lower efficiencies and wider bandwidths. Those with higher *Q* diodes are more reactive and the multipliers with such diodes (varactors) have relatively higher efficiencies and narrower bandwidths. As the *Q* of a diode increases, the circuit design becomes more sensitive to small changes in the actual circuit [38]. For example, variation in the passive circuitry dimensions due to fabrication tolerances can degrade the actual multiplier performance. This degradation can be greater for multipliers operating with higher *Q* diodes.

The *Q* of a diode is inversely proportional to the product of $C_j R_S$ (where C_j is the junction capacitance and R_s is the parasitic series resistance, Equation 2.19), and higher diode *Q* can be achieved with lower junction capacitance (C_j). Higher reverse bias voltage (more negative) increases the depth of the depletion region (x_d in Fig. 2.6), which in turn reduces the junction capacitance. Therefore, smaller anode area and/or higher bias voltage is required to operate a diode with a higher *Q*. The designed *Q*=2 diode has an epitaxial layer doping of $1\times10^{17}/\text{cm}^3$, a thickness of 4700 Å, an anode area of 73.6 μm^2 per diode, and a tuning bias voltage of -3 V. The *Q*=3 diode has an epitaxial layer thickness with

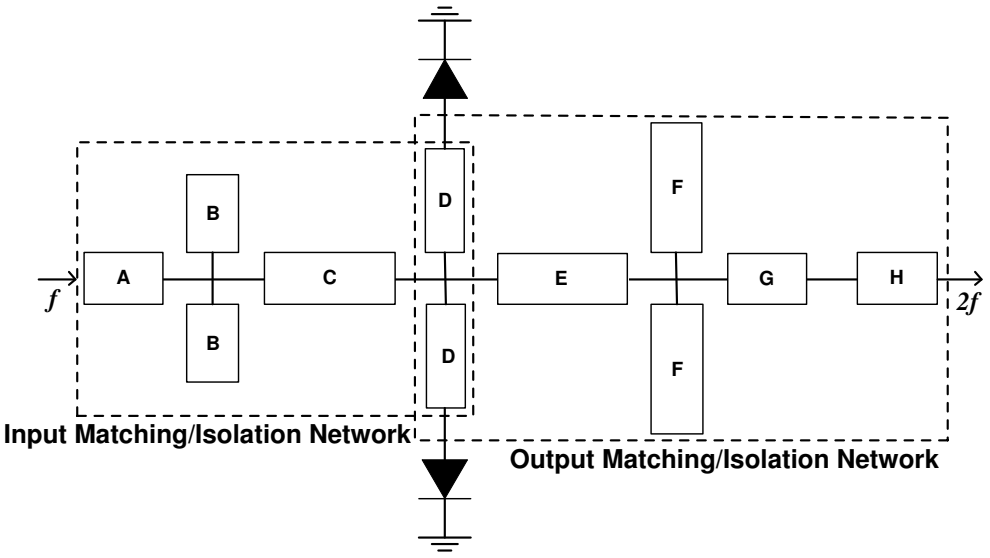


Figure 2.12: Schematic of the designed MMIC frequency doublers.

the same doping and the same thickness, an anode area of 65.3 μm^2, and a tuning bias voltage of -6 V. As is expected, the difference between the two designed diodes are in the anode area and bias voltage that is used to control the *Q* of the diodes. At the fundamental frequency (40 GHz), the impedances of the diodes were calculated to be 52.3-*j*100 Ω and 52.4-*j*160.8 Ω for the *Q*=2 and *Q*=3 diodes, respectively. At the second harmonic (80 GHz), the impedances of the *Q*=2 diode was calculated to be 41.2-*j*56 Ω and that of the *Q*=3 diode was calculated to be 50.4-*j*96 Ω. The peak efficiencies predicted by the nonlinear multiple-reflection program was 34% and 39% for the *Q*=2 and *Q*=3 diode multiplier, respectively.

The passive circuitry was designed in Agilent ADS with FGC lines optimized for lower loss, using the calculated diode impedances at the fundamental frequency and at the second harmonic. The ground plane widths of the FGC lines were carefully chosen in an effort to ensure a single mode of propagation. A schematic of a designed multiplier is shown in Fig. 2.12. The lengths of the open-ended balanced stub pair at the input are $\lambda_g/4$ at the second harmonic and the lengths of the open-ended balanced stub pair at the output are $\lambda_g/4$ at the fundamental frequency. The 50 Ω standard sections C and E are also $\lambda_g/4$

Table 2.2: Passive circuitry dimensions for the Q=2 diode multiplier.

Section	**Description**	***w*** [μm]	***s*** [μm]	**Length** [μm]
A	50 Ω signal launch section	70	63	200
B	49 Ω open-end balanced stubs	70	65	318
C	50 Ω standard section	70	63	374
D	71 Ω diode feed lines	28	112	213
E	50 Ω standard section	70	63	694
F	49 Ω open-end balanced stubs	70	65	710
G	21.5 Ω low impedance section	168	14	300
H	50 Ω signal launch section	70	63	200

Table 2.3: Passive circuitry dimensions for the Q=3 diode multiplier.

Section	**Description**	***w*** [μm]	***s*** [μm]	**Length** [μm]
A	50 Ω signal launch section	70	63	200
B	42 Ω open-end balanced stubs	70	26.6	346
C	50 Ω standard section	70	63	360
D	71 Ω diode feed lines	28	112	273
E	50 Ω standard section	70	63	702
F	49 Ω open-end balanced stubs	70	65	682
G	21.5 Ω low impedance section	168	14	307
H	50 Ω signal launch section	70	63	200

long at the second harmonic and at the fundamental frequency, respectively. Thus the output isolation network appears to be an open circuit at the fundamental frequency, and similarly, the input isolation network appears to be an open circuit at the second harmonic, providing appropriate isolations. At the same time, the impedances of these stubs and the high impedance FGC lines (Section D in Fig. 2.12) that are used at the diode input to resonate the average capacitances of the diodes, are chosen to match the diode impedances to the input and output port impedances of 50 Ω, at the input frequency of 40 GHz and at the output frequency of 80 GHz, respectively. The input and output matching/isolation networks were optimized using Agilent ADS where the diodes were modelled as a resistor in series with a capacitor. The goal was to match the diode impedances to the embedding impedances, while the harmonic trap at the input and pump trap at the output provide appropriate RF blockings. The designed passive circuitry dimensions are summarized in Table 2.2 and 2.3.

The measured DC characteristics of fabricated Q=2 and Q=3 diodes are in Table 2.4. The measurement was taken with HP 4155A Semiconductor Parameter Analyzer and a pair of Cascade Microtech tungsten probes with 2.4 μm radius tips. As is mentioned in Section 2.2.3, included in the measured parasitic series resistances (R_s) in Table 2.4 are contact resistance between the probe and the gold probing pad on the wafer. This was found to be 0.9 Ω/contact. Considering the fact that measurements require two probe-to-gold contacts, the actual parasitic series resistances are expected to be 3.6 Ω and 3.8 Ω for the Q=2 and Q=3 diode, respectively. Finally, the measured DC parameters are used to model the diodes

Table 2.4: Measured DC characteristics of the Q=2 and Q=3 Schottky barrier diodes.

	R_s [Ω]	C_{jo} [fF]	C_p [fF]	I_o [fA]	V_{BR} [V]	η	f_c [GHz]
Q=2	5.4	59	18.2	278	12.8	1.16	750
Q=3	5.6	48	16.5	615	13.0	1.19	873

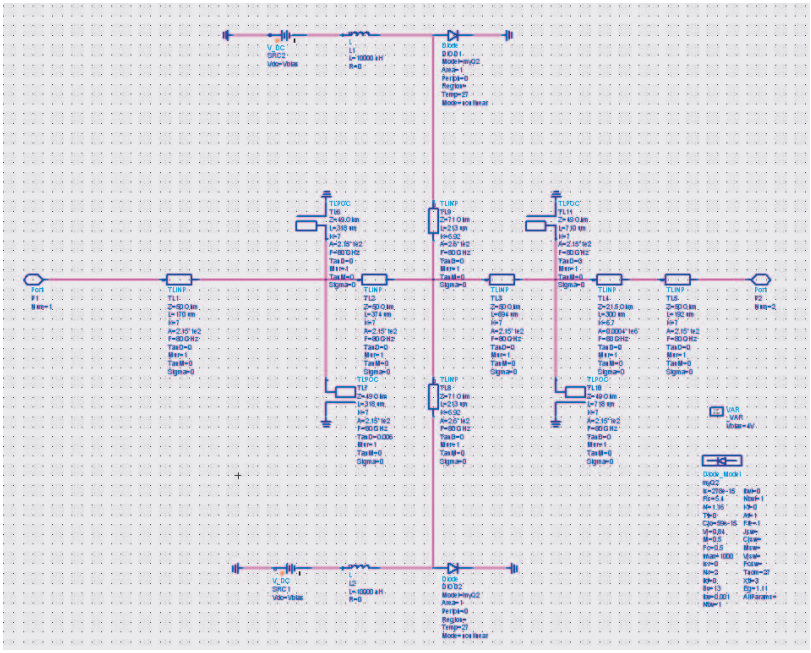
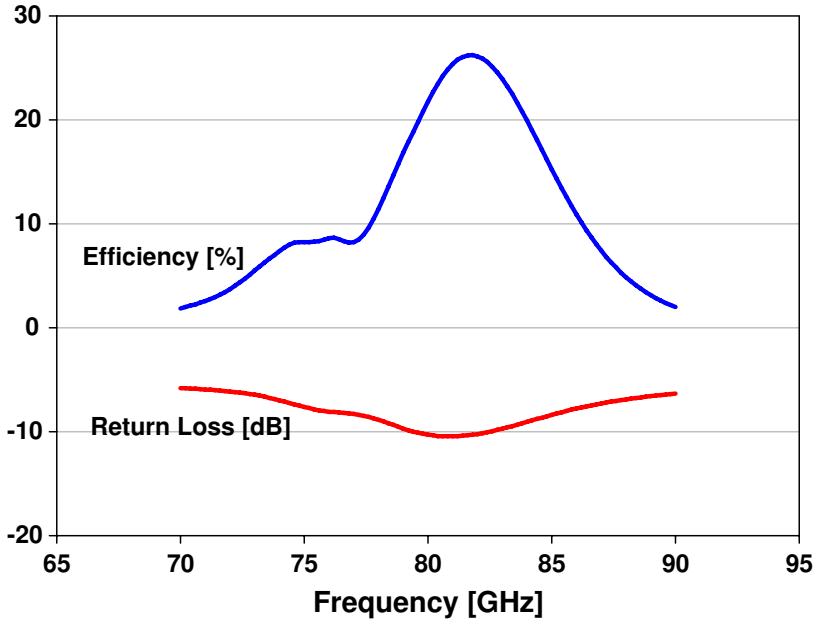


Figure 2.13: Schematic of a frequency multiplier circuit for simulations in Agilent ADS.

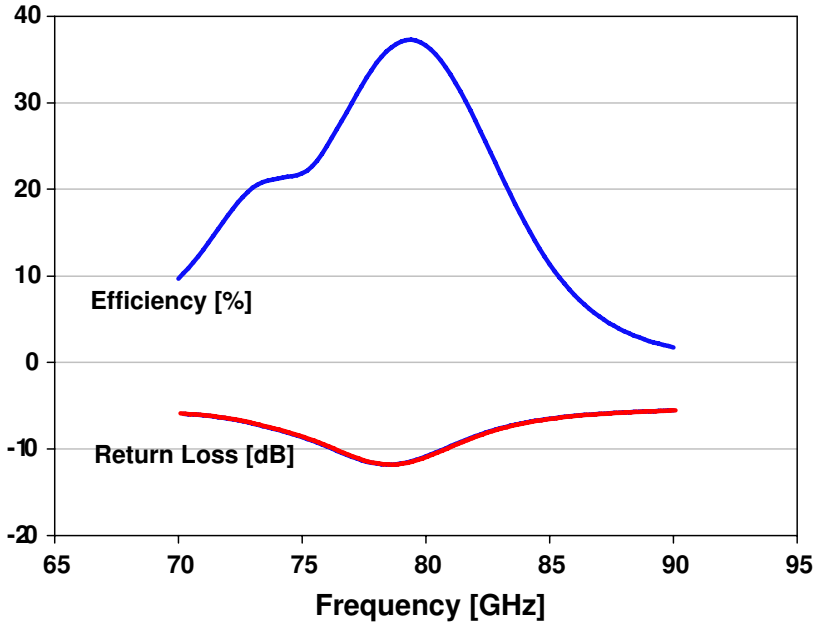
used in the frequency multiplier simulations in Agilent ADS (Fig. 2.13). The simulated peak efficiency for the Q=2 diode multiplier was 26.2% at an output frequency of 81.8 GHz with an input power level of 18 dBm, biased at -4 V. The simulated peak efficiency for the Q=3 diode multiplier was 37.3% at an output frequency of 79.4 GHz with an input power level of 17 dBm and biased at -4.4 V. Simulated efficiencies and return loss for both multipliers with fixed bias is plotted in Fig. 2.14. Shown in Fig. 2.15 are the simulated output power as a function of the input power at the output frequency of 81.8 GHz and 79.4 GHz, for the Q=2 and Q=3 diode multipliers, respectively, biased at -4 V and -4.4 V.

2.5 Multiplier Fabrication

The designed frequency multipliers were fabricated on GaAs wafer with a thickness of 625 μm. The silicon-doped active layers were grown on a 3 inch (100)-oriented GaAs substrate. The n^- layer was 4700 Å thick with a doping level (N_d) of 1×10^{17}/cm^3 and



(a)



(b)

Figure 2.14: Simulated efficiency and return loss vs. output frequency for the GaAs multipliers. Diodes were modelled in Agilent ADS using the DC parameters in Table 2.4: (a) Q=2 diode multiplier with an input power of 18 dBm and bias level of -4 V. (b) Q=3 diode multiplier with an input power of 17 dBm and bias level of -4.4 V.

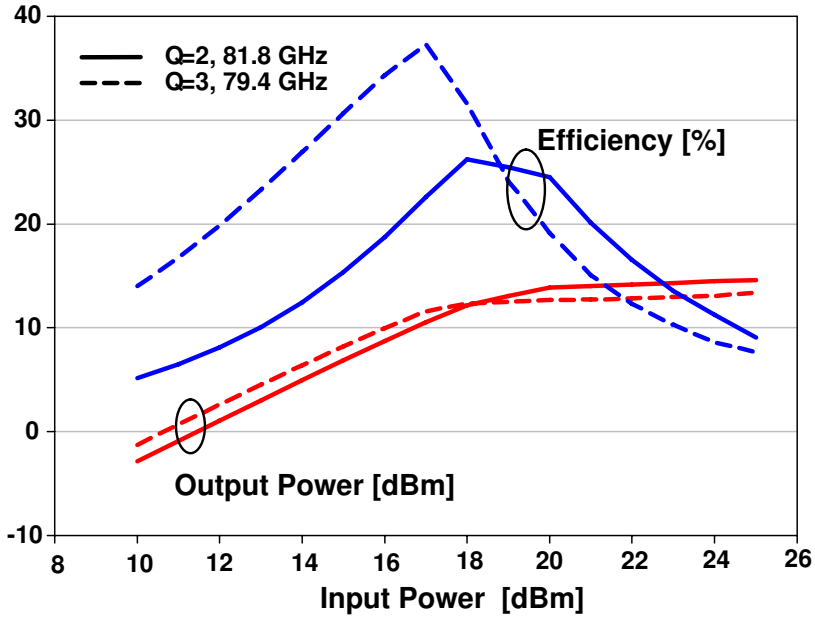


Figure 2.15: Simulated output power vs. input power at 81.8 GHz and 79.4 GHz for the Q=2 and Q=3 diode multipliers, respectively. Each diode was biased at -4 V and -4.4V.

the n^+ layer was 2.5 μm thick with a doping level of 5×10^{18}/cm^3. Between these epitaxial layers was a 500 Å thick etch stop layer of $Al_{.6}Ga_{.4}As$.

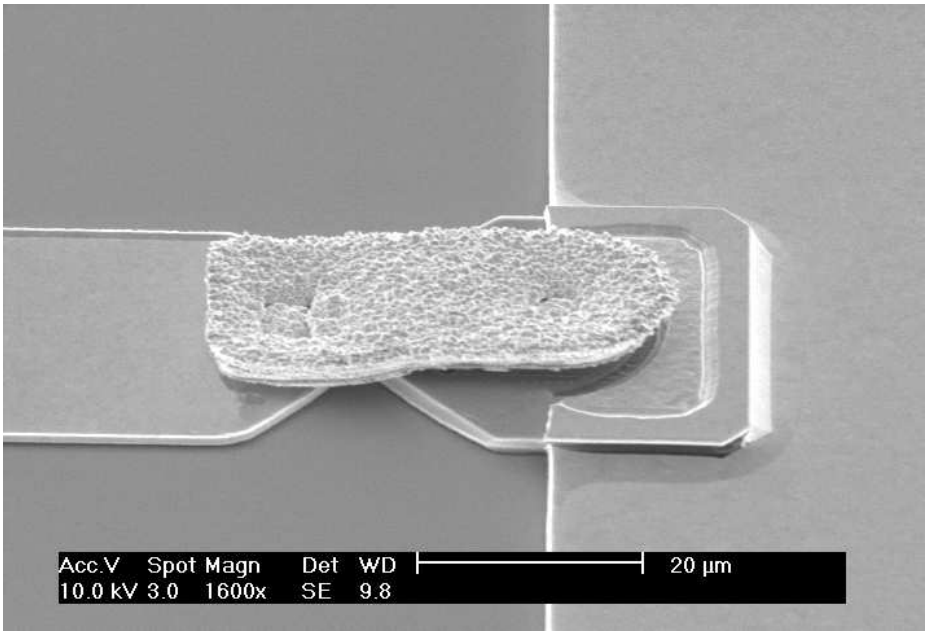
First, ohmic contacts were formed through standard lift-off process after the n^- layer was etched through with H_3PO_4:H_2O_2:H_2O (1:1:8) and the native oxide was removed in buffered-HF (BHF). The ohmic metal consisting of 250/325/650/450/2500 Å of Ni/Ge/Au/ Ti/Au layers was then annealed for 40 seconds at 405° C. Second, the Schottky anodes that consisted of 500/500/3000 Å of Ti/Pt/Au layers were formed through standard lift-off process. The native oxide on the anode patterns were etched in BHF before the wafer was metallized. After the planar diodes were formed, the doped active layers were etched away in NH_4OH:H_2O_2 (1:24) followed by an oxide etch in NH_4OH:H_2O (1:15), forming mesas to isolate the diodes from the passive circuitry. Then the passive circuitry was printed with 500 Å/1 μm of Ti/Au via standard lift-off process. Finally, air bridges were added by gold electroplating to equalize the the ground planes of FGC lines and at the same time, diode

fingers were added to connect the Schottky anodes to the passive circuitry. An SEM picture of a fabricated Q=2 diode frequency multiplier is shown in Fig. 2.1. Shown in Fig. 2.16 is a fabricated planar GaAs Schottky barrier diode.

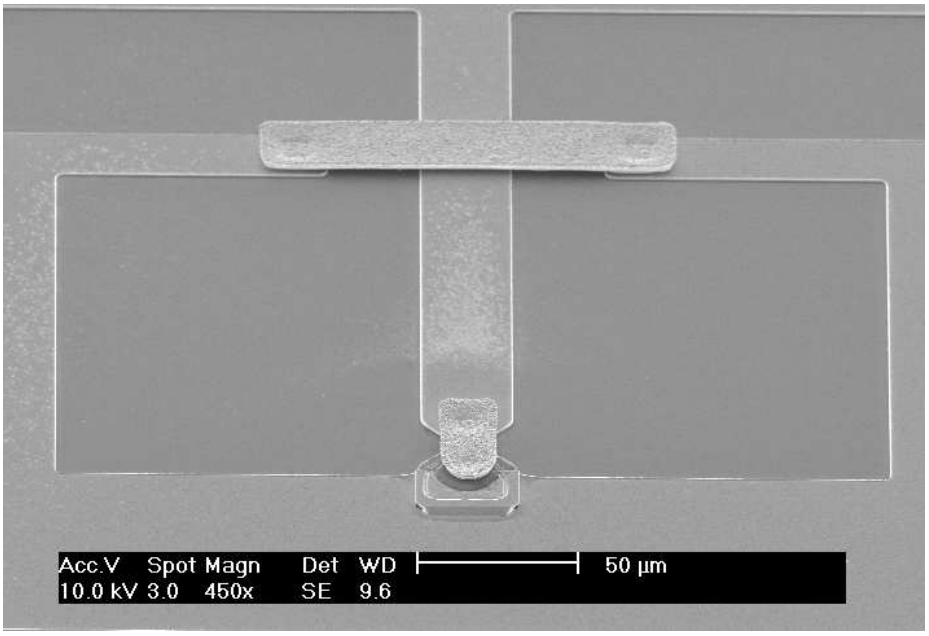
2.6 Measurements

The performance of the fabricated *W*-band frequency multipliers was evaluated using the measurement system in Fig. 2.17. The system consisted of two subsystems, input and output. A single tone signal from the HP 8510C Vector Network Analyzer system is multiplied to a *Ka*-band (26-40 GHz) signal by an HP 83554A mm-Wave Source Module. This signal drives a Hughes 800IH TWT (Travelling Wave Tube) amplifier via an HP R382A variable attenuator. The output power level of the TWT amplifier is controlled by the the variable attenuator so that the measurements can be taken at various multiplier input power levels. The output of the TWT amplifier is connected to a *Ka*-band waveguide (WR-28) system consisted of a pair of HP R752D 20 dB Directional Couplers, HP 11970A Harmonic Mixers (26.5-40 GHz), and HP R365A Isolators. The WR-28 waveguide system mixes the sampled forward and reverse signals from the directional couplers with an LO signal provided by the network analyzer system and the resulting IF is fed back to the network analyzer system to calculate the return loss.

The WR-28 waveguide system is followed by an HP R752D 20 dB Directional Coupler. An HP R4886A Power Sensor (26.5-40 GHz) followed by an HP 437B Power Meter is connected at the coupled port of this coupler to monitor the power levels at the output of the thru port. Using an HP R281A coax-to-WR28 adapter, the thru port of the 20 dB coupler was connected to a 2.4 mm Micro-Coax coaxial cable, which is connected to an HP 11612B 45 MHz-50 GHz Bias Network (tee). Bias is provided from an HP E3631A DC Power Supply, and the output of this bias tee is connected to a 150 μm pitch Picoprobe (Model 40A) by GGB Industries using a 2.4 mm-to 2.9 mm adapter and a 2.9 mm Micro-

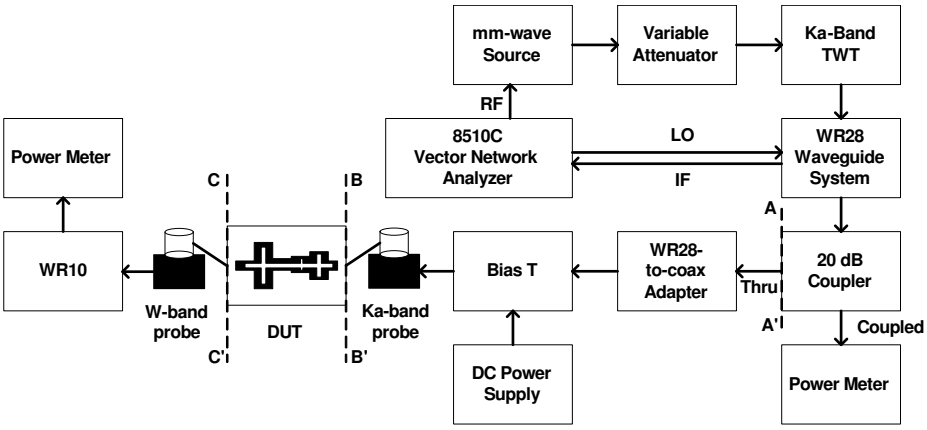


(a)

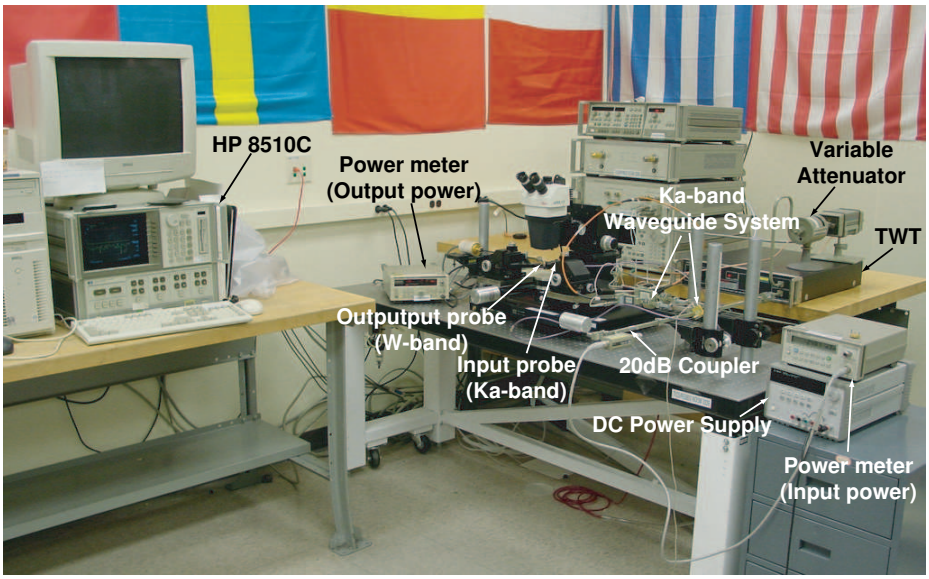


(b)

Figure 2.16: (a) Scanning electron micrograph of a fabricated planar GaAs Schottky barrier diode. (b) The diode finger connects the anode to the 71 Ω FGC line that cancels out the average capacitance of the diode. Air bridges are added to equalize the potentials of FGC line ground planes.



(a) Block diagram of the measurement setup



(b) Digital still image of the measurement setup

Figure 2.17: Block diagram and image of the frequency multiplier measurement setup system. A *Ka*-band TWT amplifier and a variable attenuator was used to vary the power delivered to the multipliers.

Coax coaxial cable.

The output measurement subsystem consisted of a 150 μm pitch Picoprobe (Model 120) that has a WR-10 waveguide input, a 30 cm long WR-10 waveguide section, and an Anritsu MP717A Power Sensor (60-90 GHz) followed by an Anritsu MA402B Sensor Adapter and an Anritsu ML4803A Power Meter. With the described measurement system, the highest input frequency is limited to 40 GHz whereas the lowest output frequency is limited to 70 GHz. Therefore, the frequency multiplier performance measurement is limited to the input frequency range of 35-40 GHz, which corresponds to the output frequency range of 70-80 GHz.

In order to accurately measure the frequency multiplier efficiencies, loss introduced by the input and output measurement subsystems needs to be accounted for. To measure the loss associated with the input measurement subsystem, the system was first calibrated at the output flange of the 20 dB coupler connected to the WR-28 waveguide system, denoted by the dotted line AA' in Fig. 2.17(a). Calibration was achieved using WR-28 load, short, and offset short calibration standards (HP R11644A WR-28 Calibration Kit), and a WR-28 load was at the coupled port during calibration. The loss introduced by the components between this reference plane and the end of the *Ka*-band probe tips can be obtained from the *S*-parameters of the system consisting of the components. The system can be treated as a two-port network with unknown *S*-parameters, S_{11}, S_{21}, S_{12}, and S_{22}. The *S*-parameters can be calculated by measuring the input reflection coefficient of this two-port network (Γ_{in} in Fig. 2.18) when a load with a known reflection coefficient (Γ_L in Fig. 2.18) is connected to the output of this two-port network [39]:

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}. \tag{2.24}$$

Once the input reflection coefficients (Γ_{in}) of the input measurement subsystem with three standard planar short, open, and 50 Ω load connected at the output port is measured, the *S*-parameters of the two-port network yields a system of three equations with three

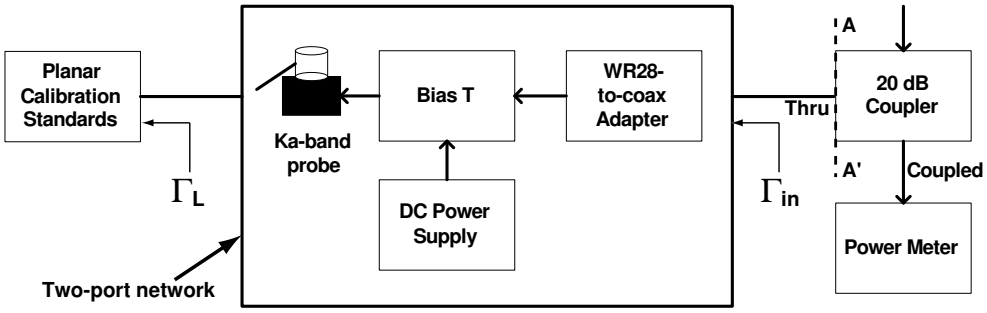


Figure 2.18: Block diagram of the input measurement subsystem beyond the waveguide-calibrated reference plane (AA'). The components between this component and the end of the *Ka*-band probe tips can be considered as a two-port network with unknown *S*-parameters. A WR-28 waveguide load was connected at the coupled port of the 20 dB coupler for the input reflection coefficient measurements.

unknowns :

$$S_{11} = \Gamma_{load}, \tag{2.25}$$

$$S_{22} = \frac{2\Gamma_{load} - \Gamma_{short} - \Gamma_{open}}{\Gamma_{short} - \Gamma_{open}}, \tag{2.26}$$

$$S_{21} = S_{12} = \sqrt{(S_{22} - 1)(\Gamma_{load} - \Gamma_{open})}, \tag{2.27}$$

The *S*-parameters of the output measurement subsystem (an output probe and a WR-10 waveguide section) can be calculated in a similar way using HP 8510C in a *W*-band configuration. The calculated *S*-parameters of, for example, the output measurement subsystems are plotted in Fig. 2.19

The S_{11} of the input and output measurement subsystems remained below -15 dB in the measured range, i.e. 35-40 GHz for the input and 70-80 GHz for the output. Therefore, the loss introduced by each subsystem can be approximated by its insertion loss ($|S_{21}|$). The loss in the input measurement subsystem is found to be 9.2 ± 0.2 dB. The loss in the output

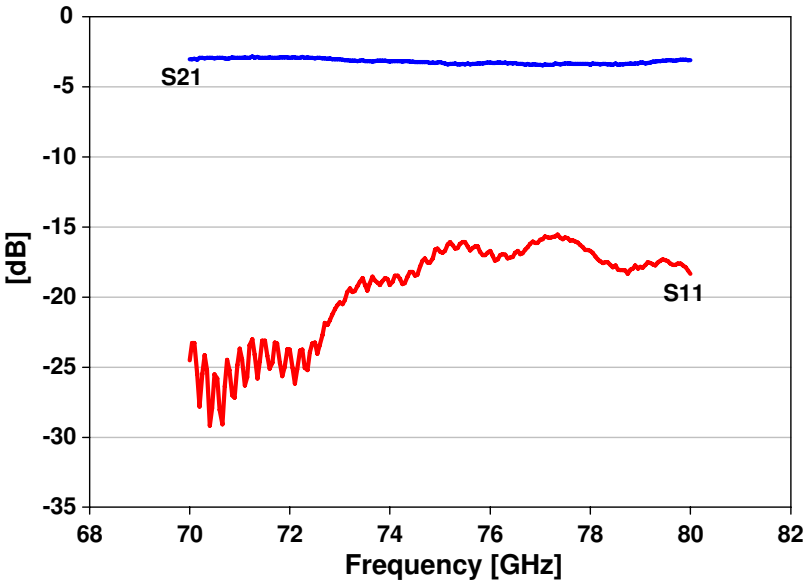


Figure 2.19: Calculated return loss and insertion loss of the output measurement subsystem. The subsystem consists of a ground-signal-ground Picoprobe and a section of WR-10 waveguide.

measurement subsystem is found to be 2.7$\pm$0.17 dB. Using the obtained loss, the input and output power level reference planes can be set to the corresponding ports of the frequency multipliers, as shown by the dotted line BB' (input) and the dotted line CC' (output) in Fig. 2.17(a). For accurate monitoring of the input power, *S*-parameters of the 20 dB coupler of the input measurement subsystem were also measured.

Frequency multiplier efficiency measurements were taken for the input frequency range of 35 GHz to 40 GHz, with 100 MHz steps. For each frequency points, the input power was varied from 10 dBm, with increments of 1 dBm, up to as high as 22 dBm. Input power was varied by controlling the power driving the TWT amplifier with the variable attenuator. The power levels at the input port of the frequency multipliers were monitored using the power meter at the coupled port of the 20 dB coupler, measured *S*-parameters of this 20 dB coupler, and the loss of the input subsystem obtained from its *S*-parameters. Finally, the DC bias was varied at every test points to maximize the performance for the given conditions, i.e. input frequency and input power. The loss associated with the output measurement

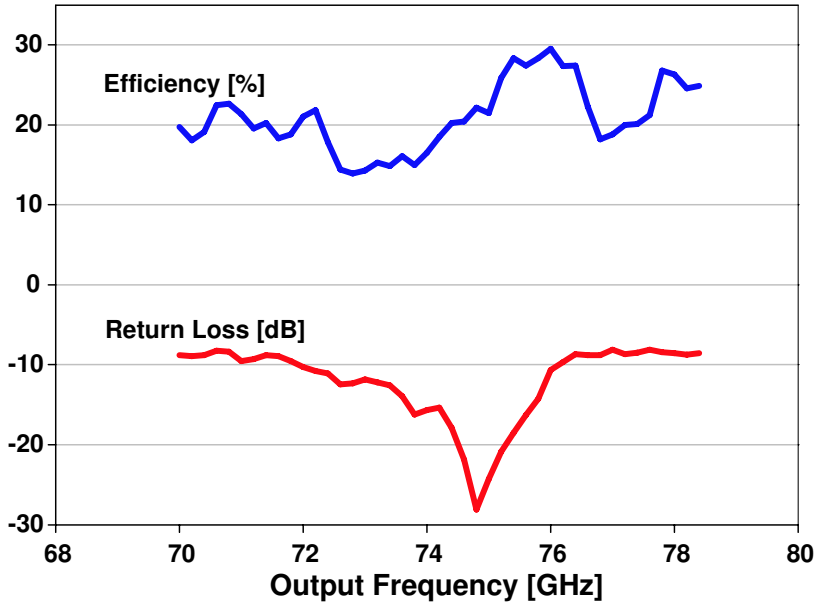


Figure 2.20: Measured efficiency and return loss versus output frequency for a Q=2 diode frequency multiplier at an input power level of 100 mW (20 dBm).

subsystem was calibrated out for the multiplier efficiency calculations.

2.7 Experimental Results

Measured RF power efficiency and return loss versus output frequency of a Q=2 diode multiplier is shown in Fig. 2.20. The multiplier shows a peak efficiency of 29.5% at the output frequency of 76.2 GHz with an input power of 20 dBm, showing a very close performance to the simulated peak efficiency of 26.2%. It is also close to the peak efficiency of 34% predicted by the multiple-reflection program. The corresponding experimental output power level is 14.7 dBm (29.5 mW). The efficiency remains above 20% in the majority of the measured frequency range. For an input power level of 20 dBm, the minimum efficiency is 13.9% at the output frequency of 72.8 GHz, where the output power level is 3.3 dB below the peak level.

As can be seen in this figure, the Q=2 diode frequency multiplier is well matched,

the return loss exhibiting better than 10 dB in the majority of the measured frequency range for the input power level of 20 dBm. For example, the return loss is 10.4 dB at the output frequency of 76.2 GHz where the multiplier shows maximum efficiency of 29.5%. The return loss at the output frequency of 72.8 GHz where the multiplier shows minimum measured efficiency of 13.9% is 12.4 dB, which indicates that less than 6% of the input power is being rejected. This implies that the actual diode impedances reasonably matches the predicted impedances and that the input matching network is efficiently delivering the input power to the diodes, therefore showing a good impedance match at the input port. The difference in the efficiencies at the two frequency points is largely due to the output matching network. The output matching network consists of a 50 Ω standard section, a pair of balanced 49 Ω open-ended stubs, and a 21.5 Ω quarter wavelength (at 80GHz) transformer. At the second harmonic frequency, this network is designed to match the Q=2 diode impedance of $41.2 - j56$ Ω to the output port impedance of 50 Ω so that maximum second harmonic power coming out from the diodes is delivered to the output port. The 50 Ω standard section and the open-ended stubs are quarter wavelengths at the fundamental frequency, or half wavelengths at the second harmonic. Therefore, greater variation in the impedances of the output matching network than the input matching network are expected with respect to frequency. All the passive circuitry sections of the multipliers are equal to or shorter than quarter wavelengths in the input frequency range (35-40 GHz) where as all the sections are close to being half wavelengths in the output frequency range (70-80 GHz). Therefore, it is expected that the input and output matching networks exhibit greater performance variations with respect to the input frequency than to the output frequency.

Experimental results of RF power efficiency and return loss versus output frequency for a Q=3 diode multiplier is shown in Fig. 2.21. The peak efficiency is 36.1% at the output frequency of 76.0 GHz with an input power of 20 dBm, again showing very close performance to the simulated peak efficiency of 37.3%. It is also very close to the peak efficiency of 39% predicted by the multiple-reflection program. The corresponding output

power level is 15.6 dBm, or 36.1 mW. As is the case with the Q=2 diode multiplier, the efficiency remains better than 20% in the majority of the measured frequency range for the Q=3 diode multiplier. For the input power level of 20 dBm, the minimum efficiency is 18.6% at the output frequency of 70.2 GHz, where the output power level was 2.9 dB below the peak level. The return loss of the Q=3 diode multiplier is also better than 10 dB in the majority of the measured frequency range. For example, the return loss is -10.4 dB at the output frequency of 76.0 GHz where maximum efficiency is achieved, indicating that less than 10% of the input power is being rejected at the input port of the circuit.

Although the experimental results show peak efficiency levels that are very close to the simulated results, there are still discrepancies between the two. For example, Agilent ADS expected the peak efficiency of the Q=3 diode multiplier at the output frequency of 79.4 GHz whereas in the experiment, the peak efficiency is at the output frequency of 76.2 GHz. The shift in the peak efficiency frequency point is mostly due to the reduced zero-bias capacitances. Using Equation 2.3, the zero-bias capacitances are calculated to be 79 fF for a Q=2 diode and 69 fF for a Q=3 diode. The zero-bias capacitances obtained from the measured *C/V* curve are 25-30 % smaller, 59 fF and 48 fF. The reduction in the zero-bias capacitances are due to the dimensional tolerances in the mask generation especially for circular patterns. The shift in the peak efficiency frequency point is also in part due to parasitic capacitances of the multiplier diodes, that had not be accounted for in the simulations. From the measured *C/V* curve, the parasitic capacitances (C_p) were calculated to be 18.2 fF and 16.5 fF for the Q=2 and Q=3 diodes, respectively. A 2D electrostatic simulation calculates the capacitance between the anode finger metal and anode/ohmic metal to be over 10 fF.

The measured efficiencies and the output power versus the input power at the output frequency of 76.2 GHz and 76.0 GHz for Q=2 and Q=3 diode multipliers, respectively, are shown in Fig. 2.22. Due to relatively high loss associated with the input measurement subsystem (9.2 ± 0.2 dB), the input power delivered to the frequency multipliers was limited

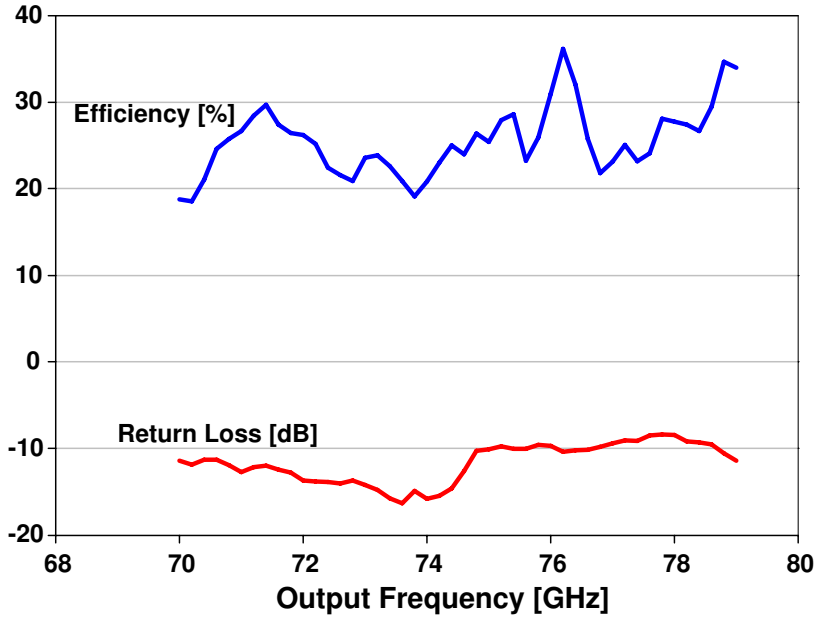
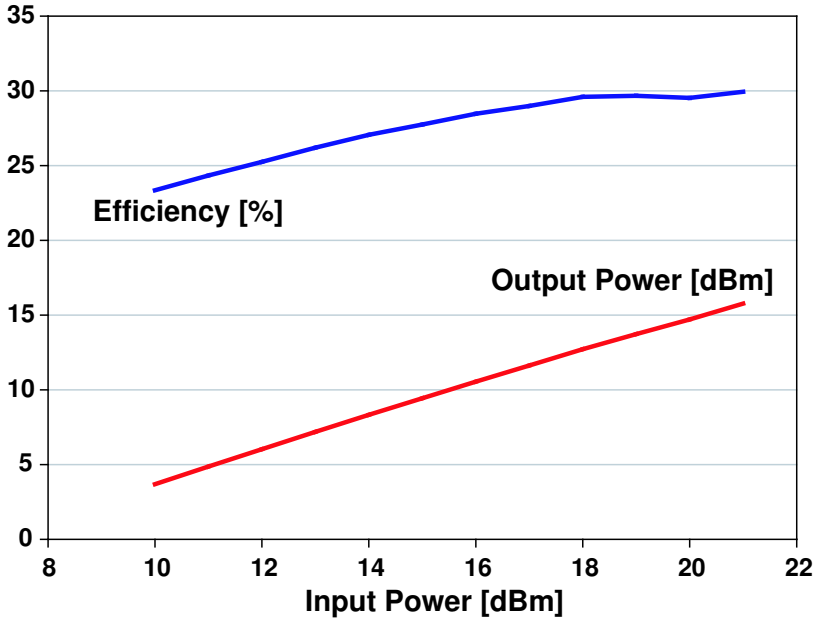
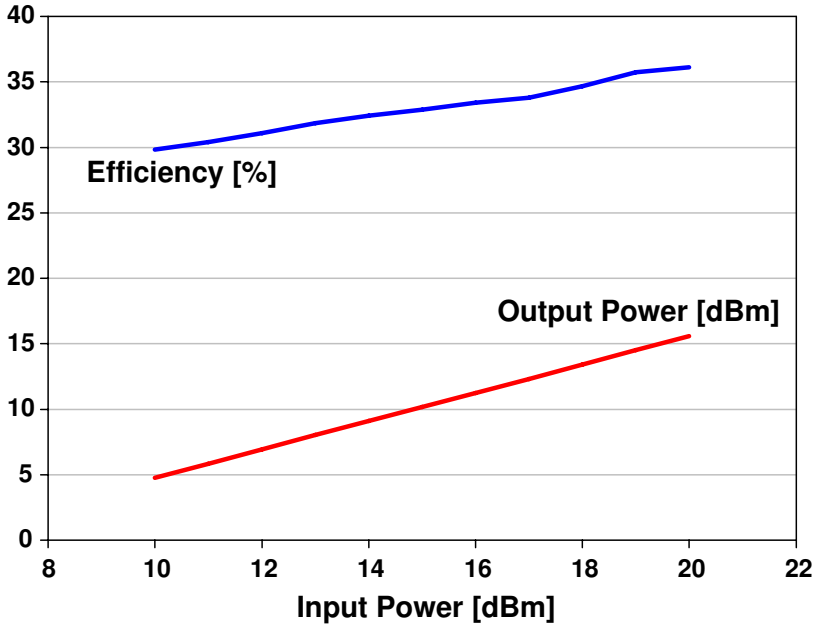


Figure 2.21: Measured efficiency and return loss versus output frequency for a Q=3 diode frequency multiplier at an input power level of 100 mW (20 dBm).

to 20-21 dBm at the frequencies where maximum efficiencies are achieved. Therefore, no measurements were taken with higher input power levels at these frequency points. However, as can be seen in the figure, the output power levels were still not saturated at the input power of 21 dBm and 20 dBm for Q=2 and Q=3 diode multipliers, respectively. Due to current saturation within the diodes, the efficiency of the Q=2 diode multiplier started to saturate at the input power level of 18 dBm, whereas the efficiency of the Q=3 diode multiplier starts to saturate at the input power level of 19 dBm, which are in reasonable agreements with the simulated results (Fig. 2.15). Throughout the whole experiment, the maximum output power for the Q=2 diode multiplier was 16.6 dBm (46 mW) at the output frequency of 75.6 GHz with an input power level of 22 dBm (158 mW). For the Q=3 diode multiplier, the maximum output power was 16.5 dBm (45 mW) at the output frequency of 75.6 GHz with an input power level of 22 dBm (158 mW). However, from previous results with similar diodes [40], it is a reasonable expectation that both multipliers would be able to produce higher output power levels given higher input power levels.



(a) Q=2 diode multiplier at the output frequency of 76.0 GHz



(b) Q=3 diode multiplier at the output frequency of 76.2 GHz

Figure 2.22: Measured efficiencies and output power levels versus input power of a Q=2 diode multiplier and a Q=3 diode multiplier.

2.8 Conclusions

GaAs Schottky barrier diode-based MMIC frequency multipliers were designed with finite ground coplanar (FGC) lines, fabricated, and tested in *W*-band. In an effort to increase the efficiency, the FGC line geometries were optimized to reduce the ohmic loss, therefore the overall loss, while still maintaining a single mode of propagation.

The relationship between the loss in the FGC lines and the dimensions were experimentally verified. Four different thru-reflect-line (TRL) calibration standard sets were printed with 500 Å of titanium and 1 μm of gold on semi-insulating GaAs of 625 μm thickness, two of which have the characteristic impedances of 50 Ω and the other two have the characteristic impedances of 71 Ω. A 50 Ω and a 71 Ω FGC lines were those that have been used extensively at The University of Michigan for high frequency circuits while the other two FGC lines have wider center conductor and slot dimensions. Both the center conductor and the slots are widened by 40 % so as to maintain the same *w*/*s* ratio and thus the characteristic impedances of the lines. The ground plane widths of scaled FGC lines were carefully chosen to minimize the effect on characteristic impedances, and to ensure single mode propagation. Experimental results reveal that by having 40 % wider center conductor and slot widths, the loss can be improved by 0.3 dB/cm for a 50 Ω line and by 0.7 dB/cm for a 71 Ω line over the entire *W*-band with nearly the same characteristic impedances and effective permittivities (ε_{eff}).

Based on the FGC lines with optimized dimensions, monolithic frequency multipliers with GaAs Schottky barrier diodes were investigated. The frequency multipliers were designed so that the diodes have input *Q*'s of two and three. The peak efficiencies achieved were 29.5% at the output frequency of 76.0 GHz with an input power of 20 dBm for a *Q*=2 diode multiplier, and 36.1% for a *Q*=3 diode multiplier at the output frequency of 76.2 GHz with an input power level of 20 dBm. The efficiency of 36.1% is the highest efficiency reported for a diode-based MMIC frequency multiplier in *W*-band. The experimental results imply that MMIC frequency multipliers, with the advantages of low cost fabrication, small

size, and better reproducibility of their performance, can very well compete conventional waveguide-based multipliers for millimeter-wave frequency sources.

CHAPTER 3

Finite Ground Coplanar (FGC) Line to Waveguide Transitions

RECTANGULAR waveguides, coaxial cables, and planar transmission lines such as finite ground coplanar (FGC) lines and microstrip lines are used extensively in microwave circuits to transfer input and output signals. An effective transition between two types of transmission lines, for example a coax-to-microstrip transition, is required in applications where two or more of such transmission means are used.

Since its introduction in 1969 [41], the finite-ground coplanar (FGC) line has become one of the most widely used transmission lines in Monolithic Microwave Integrated Circuits (MMIC's), owing to the simplicity of fabrication and its ability to easily integrate series and shunt elements without via holes . However, conventionally machined rectangular waveguides still play an important role, especially in very high frequency systems where the loss of such waveguides is significantly less than that of popular planar transmission lines. Besides its low loss and high-Q characteristics, rectangular waveguides have the ability to incorporate tuners to optimize their performance, and are capable of handling signals at much higher power levels than planar transmission lines. Therefore, effective transitions between FGC lines and rectangular waveguides are required in many applications.

While considerable amount of work has been done on microstrip- to-waveguide transitions [42–48], comparatively fewer efforts have been made to establish suitable transitions from FGC lines to waveguides [49–52]. In this chapter, transitions between FGC lines on silicon and various waveguides are presented. The transition is realized with a micromachined rectangular probe inserted into the broad sidewall of a waveguide.

First, loss characteristics of a *W*-band waveguide (WR-10) are investigated in Section 3.1. Measured attenuation as well as theoretical attenuation of the waveguide are presented and compared with the attenuation of a typical 50 Ω FGC line. Then a transitions from an FGC line to a conventional *X*-band (WR-90) and *Ka*-band (WR-28) rectangular waveguide are presented in Section 3.2. The *Ka*-band measurement results demonstrate the ability of such a transition to operate efficiently across the entire band of a WR-28.

Prior to presenting the *W*-band performance of fully micromachined transitions in Section 3.4, a simple yet promising micromachining technique, deep reactive ion etching (DRIE), that is used to develop micromachined waveguides is presented in Section 3.3. Although waveguides have many advantages over planar transmission lines especially at very high frequencies, the small dimensions make it difficult thus costly to conventionally machine to tight tolerances. If the high frequency waveguides can be micromachined, the cost can be reduced by taking advantage of the batch fabrication ability of micromachining, while maintaining equal or better dimensional tolerances. In Section 3.4 and 3.5, transitions between FGC lines and waveguides micromachined in silicon are presented. Micromachined waveguides developed via the DRIE technique have sidewall profiles that are nearly identical to those of conventionally machined waveguide. When bulk, anisotropically etched, waveguide with diamond shaped profiles are formed. The novel free-standing probe presented in Section 3.5 proves the ability of such transitions to be applicable well into the submillimeter-wave and THz range. The presented transition and micromachined waveguides will be the passive part of the power combining module demonstrated in Chapter 4.

3.1 Loss in Rectangular Waveguides

The largest advantage of rectangular waveguides over popular planar transmission lines, such as finite ground coplanar (FGC) lines and microstrip lines, is its loss performance and power handling capacity.

Although the strengths of most dielectrics used as the planar transmission line substrates are greater than that of air, the power handling capacity of a planar transmission line is limited primarily by the heating of the substrate due to ohmic loss [2]. The power handling capacity can be increased by increasing overall dimensions of a planar transmission line. In microstrip lines, for example, as the substrate becomes thicker, the breakdown voltage increases, thus its peak power handling capacity is improved. However, this may not be feasible at high frequencies where thin substrates are required to suppress excitations of higher order modes. In FGC lines, larger slot widths not only improves its power handling capacity, but also leads to excess radiation loss and higher order mode excitations. Assuming maximum operating temperature of 100°C, the average power handling capacity of a 50 Ω microstrip line on silicon is calculated to be 1.6 kW at 20 GHz [33]. On the other hand, the power handling capacity of a rectangular waveguide is limited mostly by the breakdown of air that fills up the waveguide. Air breaks down at a field strength of about $E_d = 3 \times 10^6$ V/m at room temperature while silicon and GaAs breaks down at a field strength that is 10 times higher or more. However, waveguides have much larger cross sectional area and the metal sidewall thickness is by far thicker than the metal strips of planar transmission lines. This enables rectangular waveguides to be suitable for high power applications. For example, a WR-10 rectangular waveguide has a cross sectional area of 2.54×1.27 mm^2 where as the typical width of a 50 Ω FGC line center conductor is below 100 μm for operation in *W*-band (75 GHz-110 GHz). The sidewall thickness of a standard WR-10 waveguide is around 1 mm while the planar transmission line metal strip thicknesses are on the order of μm's. At the time of this writing, a *K*-band (18-26.5 GHz) rectangular waveguide (WR-42) section with a peak power handling capacity of 170 kW is

commercially available from Advanced Technical Materials, Inc., Patchogue, NY [53].

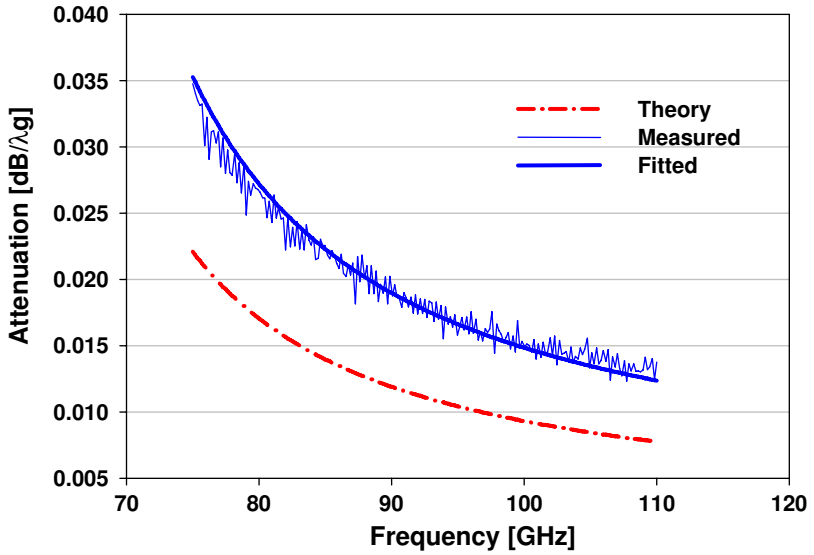
The other major advantage of a rectangular waveguide over planar transmission lines is its superior loss performance. As is seen in Section 2.3, loss performance of planar transmission lines can be improved, to some degree, by enlarging the dimensions. However, there are limiting factors in such schemes and also due to the limitation on the realizable minimum circuit size, the loss performance is especially critical for higher frequency applications, where the wavelengths become very small. For rectangular waveguides, the surface roughness of the sidewalls and finite conductivity of the sidewalls are the two main sources of loss. Due to the low loss characteristic of air, waveguides exhibit negligible dielectric loss. If the sidewall roughness is negligible compared to the wavelengths, the attenuation (α) of a waveguide is solely ohmic loss and thus can be expressed in a closed form [54] :

$$\alpha = \frac{20}{\ln 10}\sqrt{\frac{\varepsilon_o}{\mu_o}}\frac{1}{\sigma\delta_c}\left(\frac{C}{2A}\right)\sqrt{\frac{\frac{f}{f_c}}{1-\left(\frac{f_c}{f}\right)^2}}\left\{\xi_{mn}+\eta_{mn}\left(\frac{f_c}{f}\right)^2\right\} \quad \text{[dB/m]}, \tag{3.1}$$

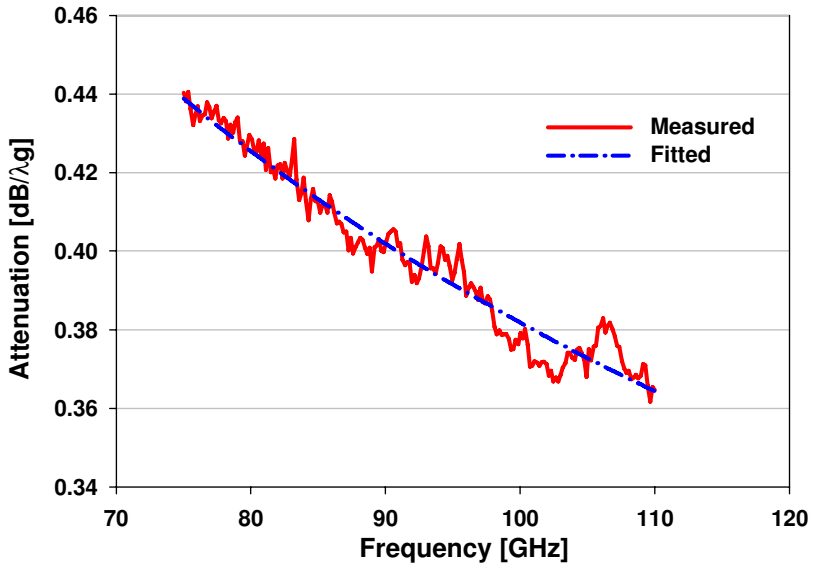
where the dimensionless geometrical parameters $\xi_{mn} = \eta_{mn} = 2/3$ for the TE_{10} mode, σ is the conductivity of the sidewall metal, δ_c is the skin depth at the cutoff frequency, A is the waveguide cross sectional area, and C is the waveguide circumference. The guided wavelength of a signal travelling inside a waveguide can be expressed as :

$$\lambda_g = \frac{\lambda_o}{\sqrt{1-\left(\frac{f_c}{f}\right)^2}}, \tag{3.2}$$

where λ_o is the free-space wavelength, f is the frequency, f_c is the cutoff frequency of the specific mode. Using these two equations, theoretical loss per guided wavelength (λ_g) for the TE_{10} mode of a WR-10 is plotted in Fig. 3.1(a). Also plotted is the measured attenuation of a WR-10 waveguide. The experimental results are obtained by measuring



(a) Attenuation in WR-10 rectangular waveguide. Copper ($\sigma = 5.8 \times 10^7$ $(\Omega \cdot \mathrm{m})^{-1}$) sidewalls are assumed for the theoretical data.



(b) Attenuation in a typical 50 Ω finite ground coplanar line on silicon.

Figure 3.1: Attenuation per guided wavelength (λ_g) for the TE_{10} mode of a WR-10 rectangular waveguide and a 50 Ω finite ground coplanar line on silicon with typical dimensions (50/45/160 μm).

the S_{11} of a 30 cm WR-10 thru section with a waveguide short connected at the other port. The measurement was taken with an HP 8510C vector network analyzer and standard one port waveguide calibration was performed with short, offset short, and load calibration standards. Another important source of loss for waveguides in practice is the connections of two waveguide sections or elements. Improper tightening of the screws can lead to radiation loss, or introduce reactance, therefore affect the signal transfer. In order to compensate for this affect, the S_{11} of the waveguide short was measured and twice the magnitude is subtracted from the magnitude of shorted 30 cm WR-10 section S_{11}. Indeed, although not shown here, the S_{11} of the waveguide short was somewhat different from that expected from an ideal waveguide short. This is mostly due to screwing that cannot be perfect in practice. Also plotted is a curve that is fitted to the experimental data in the form of :

$$\alpha = \nu \times \sqrt{\frac{\frac{f}{f_c}}{1-\left(\frac{f_c}{f}\right)^2}\left\{1+\left(\frac{f_c}{f}\right)^2\right\}} \quad \text{[dB/m]}, \tag{3.3}$$

where ν is a fitting parameter.

For comparison, an example of planar transmission line attenuation is plotted in Fig. 3.1(b). The plot shows the loss per guided wavelength (λ_g) of a 50 Ω FGC line with gap/slot/ground widths of 50/45/160 μm. The line was printed on a high resistivity ($\rho >$ 2000 Ω·cm) silicon wafer with 1 μm of gold via standard lift-off process. The curve was plotted using the attenuation (dB/cm) and effective permittivity (ε_{eff}) data provided by MultiCAL [36] after performing a thru-reflect-line (TRL) calibration. Since loss in FGC lines are mainly ohmic, a$\sqrt{f}$ curve fitted to the experimental data is also plotted.

Fig. 3.1(a) shows that measured attenuation for a WR-10 is 0.035 dB/λ_g at 75 GHz and drops down to 0.013 dB/λ_g at the high frequency end of the measured range. Throughout the *W*-band, the experimental data was approximately 1.6 times higher than the theoretical data. This is expected since theoretical data only accounted for the ohmic loss, whereas in practice more loss is expected due to dielectric (air) loss, surface roughness, and minute

surface irregularities [55]. Also, as mentioned previously, improper connections of waveguides sections and/or elements can introduce additional loss. However, as is evidenced from the figure, the frequency dependence of the experimental attenuation values agrees very well with the theory. Fig. 3.1(b) shows that attenuation per guided wavelength for a typical 50 Ω FGC line is 0.44 dB/λ_g at 75 GHz and drops down to 0.37 dB/λ_g at the high frequency end. As can be seen, the experimental attenuation value is in an excellent agreement with a $\sqrt{f}$ curve, showing that loss in FGC lines are mostly ohmic. The attenuation per guided wavelength of an FGC line is more than 10 times higher than that of a rectangular waveguide, approaching 30 times higher values than waveguide attenuation at the high frequency end of *W*-band. Although the loss in FGC lines can be reduced by the methods in [30] and in Section 2.3, rectangular waveguides still exhibit superior loss performance. Typical loss for commercially available WR-10 is 2.0 dB/foot at 75 GHz and 1.4 dB/foot at 110 GHz [56], which is approximately 0.043 dB/λ_g and 0.015 dB/λ_g at 75 GHz and 110 GHz, respectively.

3.2 Transition to Conventional Waveguides

3.2.1 Transition Design

A sketch of the FGC line to waveguide transition first proposed by Tentzeris *et al*. [52] is depicted in Fig. 3.2. A micromachined rectangular *E*-plane probe and FGC line are printed on a substrate. The probe is fed by extending the center conductor of the shielded FGC line, and is inserted into the waveguide through a slot on the broad sidewall of the waveguide, aligned with the electric field of the waveguide's dominant mode. By choosing appropriate probe size (l and w in Fig. 3.2), probe position within the waveguide (x and h_1), probe-supporting substrate material (therefore the dielectric constant ε_r), and the thickness of this substrate (h_2), the characteristic impedance (Z_o) of the FGC line can be directly matched to that of the rectangular waveguide, eliminating the necessity of impedance matching cir-

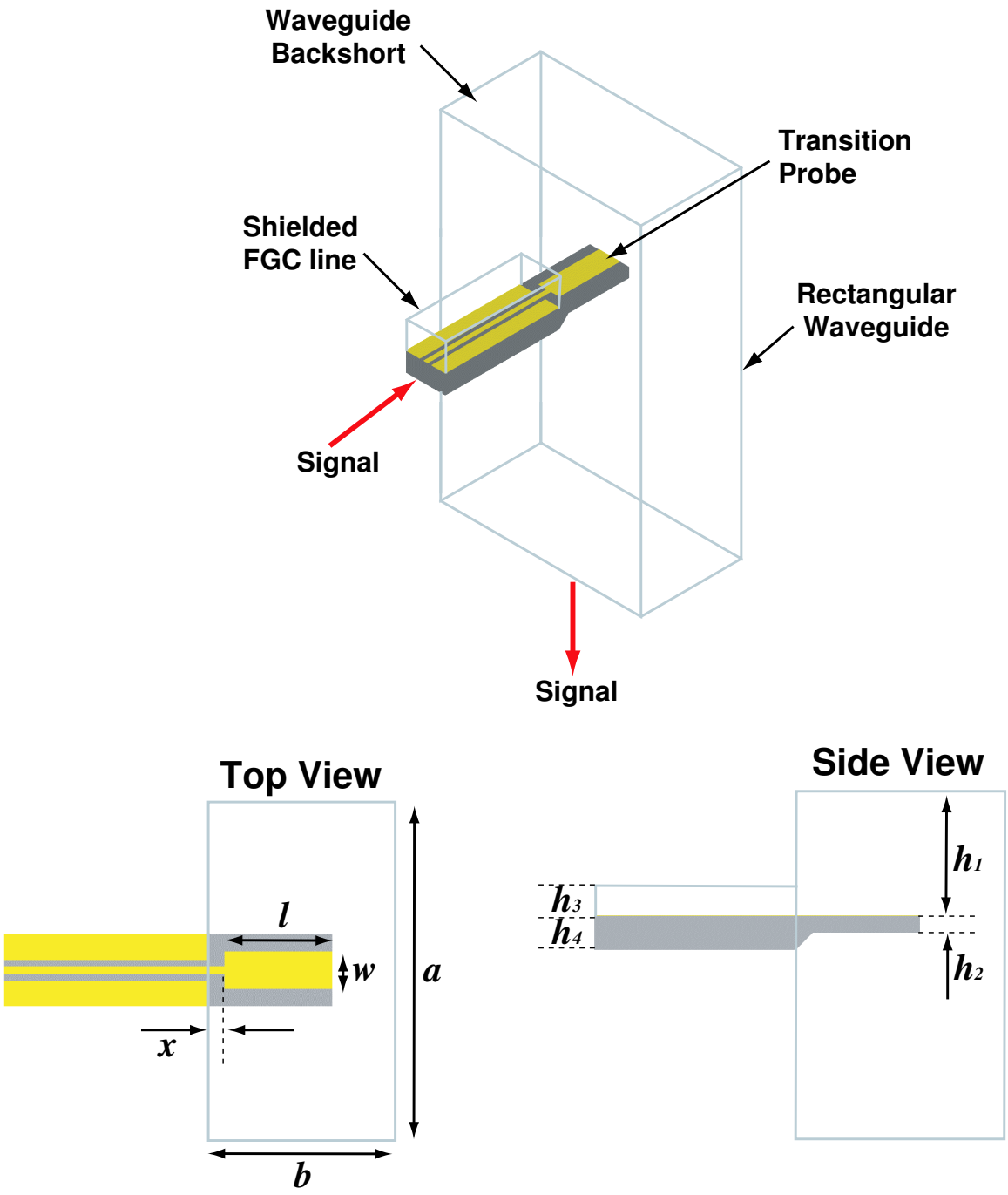


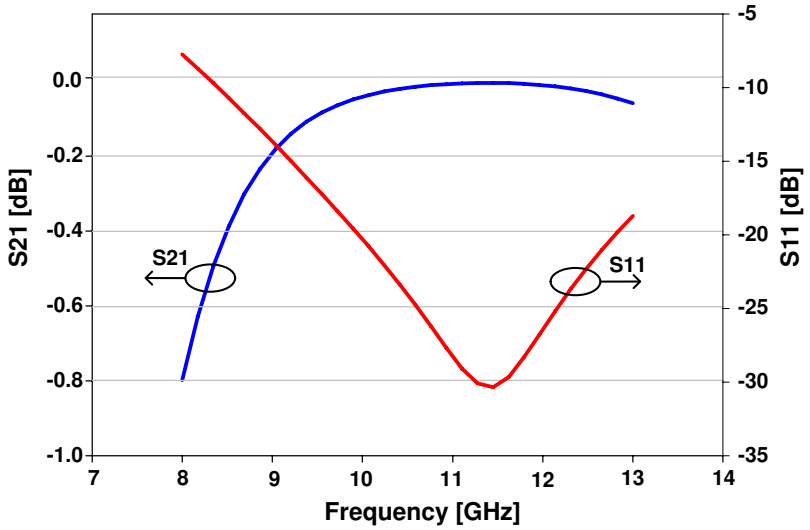
Figure 3.2: Sketch of the finite ground coplanar (FGC) line to rectangular waveguide transition via a micromachined *E*-plane probe. Dimensions are summarized in Table 3.1 and 3.2.

cuits. Transitions utilizing such probes provide wideband characteristics to operate across the entire waveguide band. Moreover, the simple structure makes such transitions more attractive for high frequency systems.

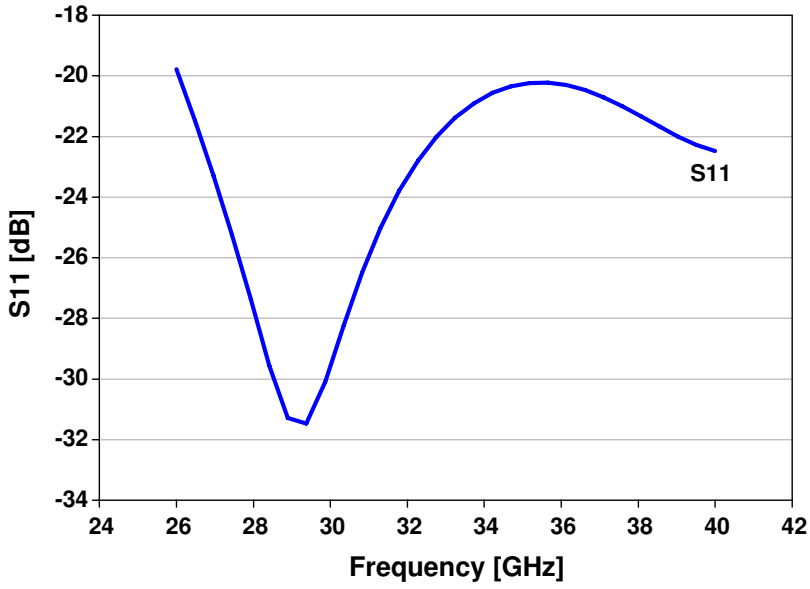
The original transition design in [52] was to couple from a 50 Ω FGC line to a *G*-band rectangular waveguide WR-187, the dominant mode of which is to operate in the frequency range of 3.95 GHz to 5.85 GHz. For an initial experiment to verify the performance of such a transition, an *X*-band (WR-90, 8.2-12.4 GHz) and a *Ka*-band (WR-28, 26.5 GHz-40 GHz) transition were designed by scaling the *G*-band design. The dimensions of a WR-187 (*a* and *b* in Fig. 3.2) are 4.755 cm × 2.215 cm, whereas the dimensions of a WR-90 are 2.286 cm × 1.016 cm and those of a WR-28 are 0.711 cm × 0.356 cm. Since the ratios of width (*a* in Fig. 3.2) to height (*b*) of the three standard waveguides were different, tuning of matching parameters (*x*, h_1, and h_2 in Fig. 3.2) other than the scaled probe dimensions (*l* and *w*) was required for an effective operation in *X*-band and *Ka*-band. Optimization was achieved with the help of Ansoft HFSS and the dimensions are summarized in Table 3.1 and 3.2. Full-wave simulation results for single transitions in *X*-band and *Ka*-band are shown in Fig. 3.3. The return loss is better than 15 dB from 9 GHz for the designed *X*-band transition, and is better than 20 dB across the entire waveguide band for the *Ka*-band transition. For both simulations, the dielectric (silicon) and metals were assumed to be lossless.

Table 3.1: Dimensions for *G*-band [52], *X*-band and *Ka*-band transition designs. Standard rectangular waveguides are used for all designs (WR-187, WR-90, and WR-28). All dimensions are in mm.

	a	b	w	l	x	h_1	h_2	h_3	h_4
***G*-band**	47.55	22.15	3.8	10.8	0.8	13.2	2.0	1.2	2.0
***X*-band**	22.86	10.16	1.58	4.67	0.54	6.06	0.875	0.79	0.875
***Ka*-band**	7.11	3.65	0.544	1.595	0.244	2.337	0.25	0.215	0.5



(a) *X*-band, WR-90



(b) *Ka*-band, WR-28

Figure 3.3: Simulated results for FGC line to rectangular waveguide transitions in *X*-band and *Ka*-band assuming lossless.

Table 3.2: Dimensions of the FGC lines in the *G*-band [52], *X*-band and *Ka*-band transition designs. All dimensions are in mm.

	Center	**Slot**	**Ground**
***G*-band**	0.8	0.5	5.8
***X*-band**	0.42	0.375	1.335
***Ka*-band**	0.112	0.99	0.365

3.2.2 Fabrication

Transition Probes

For experimental verifications, designed *X*-band and *Ka*-band transitions were fabricated and tested. For measurement purposes, the transitions were fabricated in a back-to-back configuration with an FGC line section between the two probes. The *X*-band probe structure that consists of two back-to-back transition probes with a 3.15 cm long FGC line section between the two probes was fabricated from 50 mils thick RT/Duroid 6010 M/W Laminate substrate with dielectric constant (ε_r) of 10.8 and foil (Copper) thickness of 0.67 mils. A milling machine was used to pattern the metal layer on top of the substrate, and also to mill around the probe structure so that they can be released.

The *Ka*-band probe structure consisted of two back-to-back transition probes with 1.65 cm long FGC line section between the two probes and was fabricated out of 500 μm thick silicon. First, metal alignment patterns were formed on the top of the wafer by standard lift-off process. 500 Å of titanium and 2500 Å of gold were evaporated to print verniers and crosses that could be used to align patterns on both sides of the wafer. Then the wafer was flipped over to thin down the silicon that would later serve as the probe-supporting substrate to approximately the half of its original thickness. This is for the purpose of improving the transition performance. As mentioned previously, the thickness of the probe-supporting substrate is one of the critical factors that determines the transition performance. Lithogra-

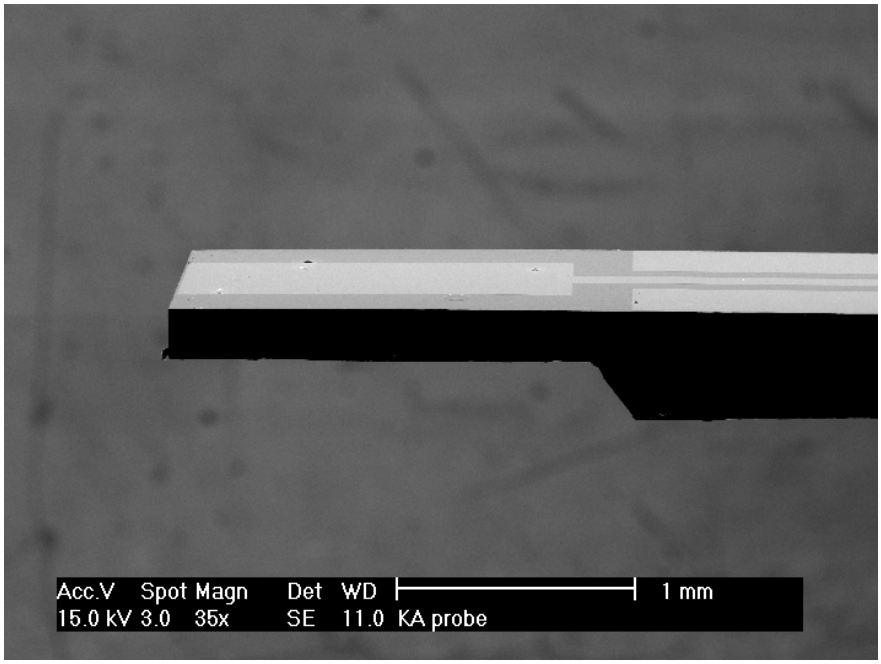
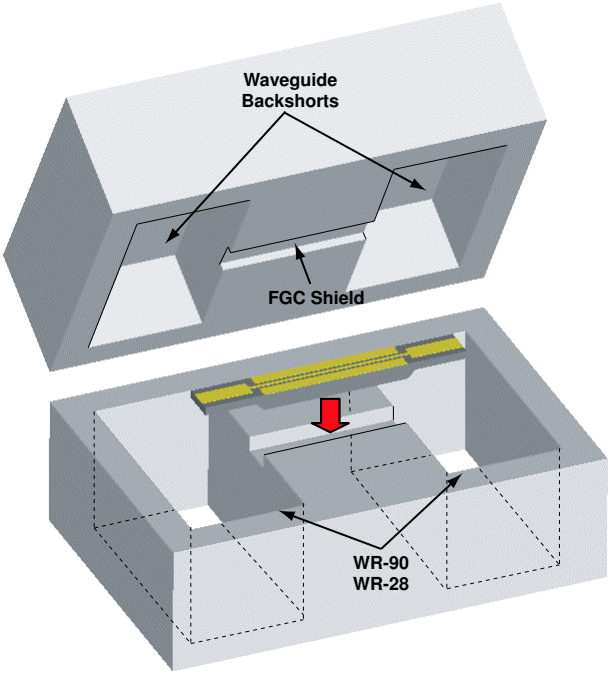
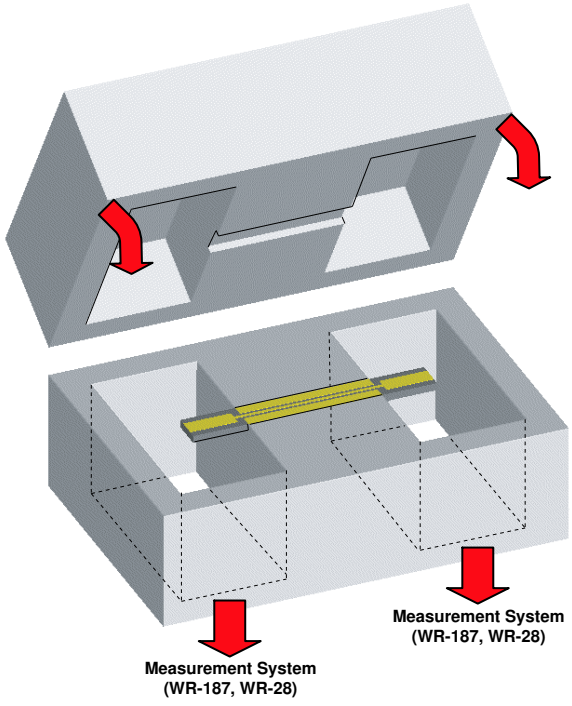


Figure 3.4: Scanning electron micrograph of a fabricated *Ka*-band transition probe structure. To improve performance of the transition, the silicon substrate under the probe was thinned down to half of its original thickness.

phy was done using an infrared (IR) alignment technique for backside processing, the patterns on which are aligned to the alignment marks on the front side. Rectangular apertures were opened in approximately 7000 Å thermally grown oxide by chemical wet etching in 49% buffered hydrofluoric acid (BHF) at an etch rate of roughly 1000 Å/min. The oxide on the front side was protected with another silicon wafer bonded with photoresist. With the remaining oxide serving as the mask, the silicon was anisotropically etched in 25% tetramethyl ammonium hydroxide (TMAH) at 80 °C. The average etch rate was roughly 20 μm/min, and the etch depth was measured using an optical microscope (Nikon Optiphot-2) by changing the focus from the etched surface to the top surface. After the oxide was stripped, probe and FGC line patterns on the front side were formed by gold electroplating. Taking into account the theoretical skin depth of 0.49 μm for gold ($\sigma = 4.1 \times 10^7\ (\Omega \cdot \mathrm{m})^{-1}$) at 26 GHz, approximately 3 μm of gold was electroplated on top of Ti/Au (500/1500 Å)



(a)



(b)

Figure 3.5: Illustration of *X*-band and *Ka*-band test structure assembly. Conventionally machined waveguide blocks were designed to accommodate back-to-back transition probes and introduce waveguide backshorts.

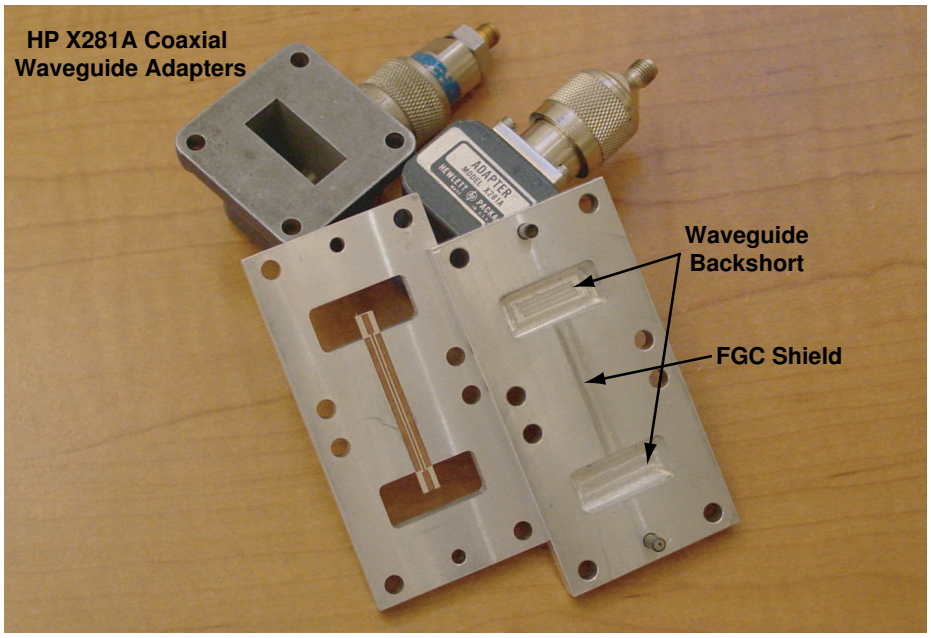


Figure 3.6: Digital still image of the *X*-band test structure with a probe structure placed in the groove. Screw holes for UG-135 standard waveguide flanges are incorporated on the aluminum block to accept *X*-band standard waveguides (WR-187). Also shown are HP X281A coaxial waveguide adapter used for *S*-parameter measurements.

seed layers. Finally, the probe structure was released from the silicon wafer with a dicing saw tool. A scanning electron micrograph of a fabricated *Ka*-band transition probe structure is shown in Fig. 3.4.

Waveguide Blocks

The *X*-band and *Ka*-band rectangular waveguides were conventionally machined out of 1/8 in. thick aluminum. The waveguide blocks were designed so that the back-to-back transition probe structures could be mounted. As suggested in Fig. 3.5, the probe structure rests in a shallow groove machined in the metal block, the depth of which is same as the thickness of the FGC line substrate. The groove above the transmission line serves as a shield and thus its height is chosen to ensure single-mode propagation along the line and maintain an impedance of 50 Ω. Each probe faces what becomes the waveguides backshort in the assembled system. For measurement purposes, the metal blocks also serve as

flanges, designed to accept *X*-band or *Ka*-band standard rectangular waveguides or suitable adapters. The test structure for *X*-band transition measurements is shown in Fig. 3.6. A similar metal block set as shown in this figure is also machined conventionally to accommodate *Ka*-band transition probe structures and to accept WR-28 with the incorporated screw holes for UG-599 standard waveguide flanges.

3.2.3 Experimental Results

The *X*-band transition structure was measured using HP 8722D vector network analyzer. Standard 2-port short-open-load-thru (SOLT) calibration was performed from 8 GHz to 12 GHz with 3.5 mm coaxial calibration standards. Using the HP X281A coaxial waveguide adapters shown in Fig. 3.6, the *S*-parameters of the transition structure were measured and are shown in Fig. 3.7. The results include loss due to the coaxial waveguide adapters and also the loss in the 3.15 cm long FGC line section. As is seen from this figure, the return loss is better than 10 dB from 9 GHz with reasonable insertion loss for a back-to-back transition up to the highest frequency end. The insertion loss, for example, is 0.56 dB per transition at 11.0 GHz, and is getting better as the operating frequency is increased.

The measured insertion loss is expected to be much smoother over the frequency range if the transition probe and the coaxial waveguide adapter were separated further. The distance between the two was decided by the thickness of the bottom metal block, 3.175 mm (1/8 in.). Thus in this experiment, the distance is less than 1/20 of the guided wavelength (λ_g) at 8 GHz, and about 1/10 of the guided wavelength at 12 GHz. This distance should be at least quarter wavelength in order to minimize the effect due to higher-order propagation modes generated at discontinuities.

The *Ka*-band transition structure was measured using HP 8510C vector network analyzer. Standard 2-port short-open-load-thru (SOLT) calibration was performed from 26 GHz to 40 GHz with HP 85056A 2.4 mm coaxial calibration standards. Using a pair of HP R281A coax-to-WR28 adapters connected to the metal blocks, the *S*-parameters of the

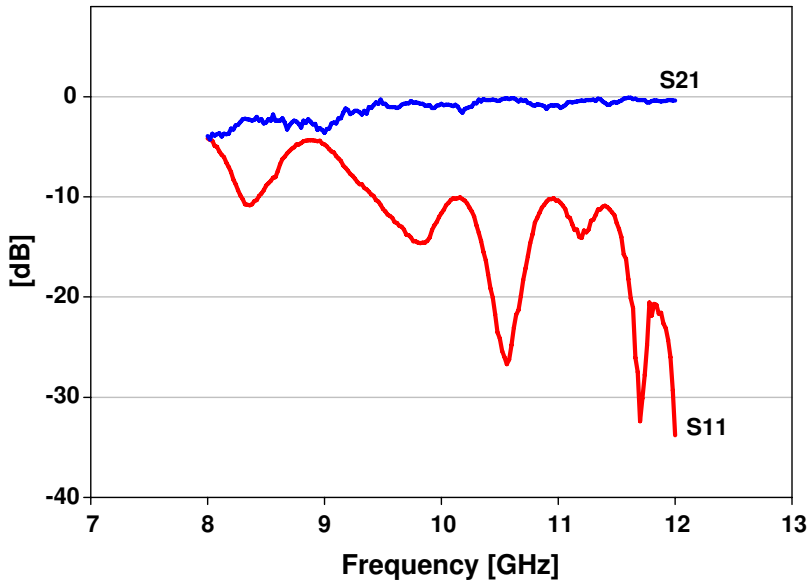


Figure 3.7: Measured *S*-parameters of a back-to-back *X*-band FGC line to rectangular waveguide transition.

back-to-back transition structure was measured and is shown in Fig. 3.8. The loss due to the coaxial waveguide adapters and also the loss in the 1.65 cm long FGC line section were de-embedded out in the insertion loss shown in this figure. The measured insertion ($|S_{21}|$) loss of back-to-back coaxial waveguide adapters is considered to be the loss introduces by the adapters. This is reasonable since the return loss of the adapters are better than 20 dB, in the entire *Ka*-band. Loss in the FGC line section between the two probes is measured by on-wafer calibration protocol using MultiCAL [36]. As is evidenced from the figure, the return loss of the back-to-back transition is better than 10 dB throughout the entire waveguide band, with the majority of the band exhibiting better than 20 dB. Also, the measured return loss shows a reasonable agreement with the simulated return loss of a lossless case.

Measured results show that the insertion loss is better than 0.5 dB per transition throughout the entire *Ka*-band. Due to the defective wafers provided by the vendor, the resistivity (ρ) of the silicon wafer that the probe structures were fabricated from was lower than 150 Ω·cm while the expected resistivity was greater than 1000 Ω·cm. This results in a greater

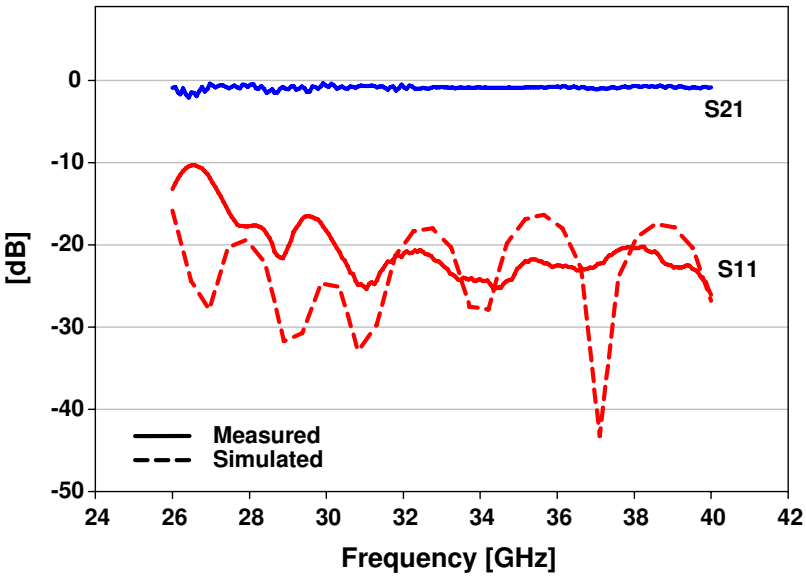


Figure 3.8: Measured *S*-parameters of a back-to-back *Ka*-band FGC line to rectangular waveguide transition. Simulated return loss for a lossless case is also shown.

loss due to increased current in the FGC line substrate as well as in the probe-supporting substrate. Indeed the FGC line attenuation, obtained from MultiCAL [36], was around 3.5 dB/cm which is more than twice as high as the attenuation of a 50 Ω FGC line on high resistivity ($\rho > 2000$ Ω·cm) silicon with similar dimensions [30]. Shown in Fig. 3.9 is simulated insertion loss results for *Ka*-band transitions with substrate different resistivities. Loss tangent ($\tan\delta$) of 0.004 was assumed for the substrate and conductivity (σ) of 4.1×10^{7} $(\Omega\cdot\mathrm{m})^{-1}$ was assumed for the metal layers. FGC lines feeding the probes were assumed to be lossless. According to the simulation results, the transition performance is degraded by approximately 0.2 dB when the resistivity is 100 Ω·cm, whereas the insertion loss for substrate resistivity of 2000 Ω·cm shows little difference from the infinite resistivity case. Thus, it is expected that the insertion loss in Fig. 3.8 improve by 0.2 dB per transition when the probes are fabricated out of silicon with resistivity of 2000 Ω·cm or higher.

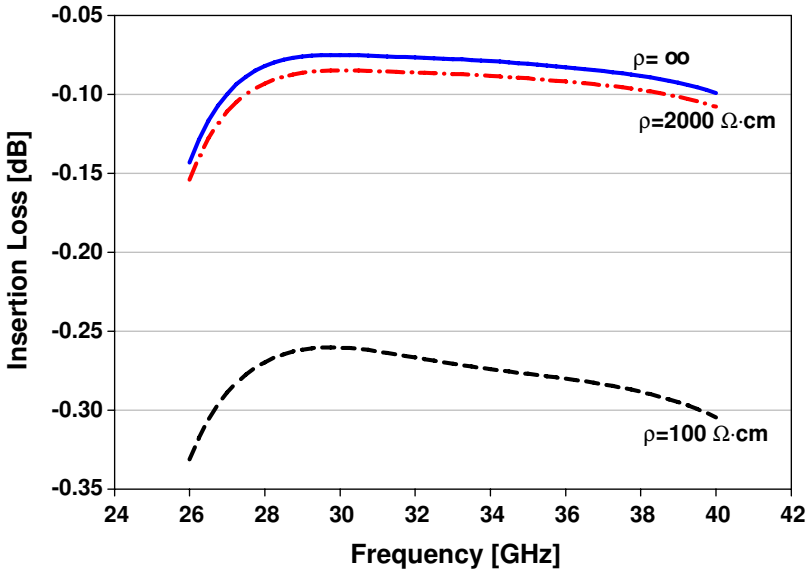


Figure 3.9: Simulated insertion loss for silicon ($\varepsilon_r = 11.9$ and $\tan\delta = 0.004$) substrates with different resistivities.

3.3 Deep Reactive Ion Etching (DRIE)

Silicon remains the substrate of choice for highly integrate circuits (IC's) and micromachined circuits owing to its advantages such as high quality thermal oxide, high stability during thermal processing, low defect densities, superior mechanical properties as well as good electrical properties and a well-established process technology. Etching is an essential process in developing micromachined circuits and structures. Deep reactive ion etching (DRIE) is a simple yet cost-effective technique that enables microfabrication of high-aspect ratio structures. The advantage of DRIE over wet anisotropic etching (Fig. 3.10) is that DRIE exhibits little crystal plane dependence, therefore reducing the geometric restrictions [57]. As evidenced in Fig. 3.11, DRIE enables fabrication of trenches that are independent of crystal planes thus making it possible to develop micromachined waveguides with vertical sidewall profiles.

The DRIE system by Surface Technology System (STS [59]), utilizing the "Bosch process" [60], typically achieves high aspect ratios of 20 to 30:1 with etch rates up to 6 μm/min.

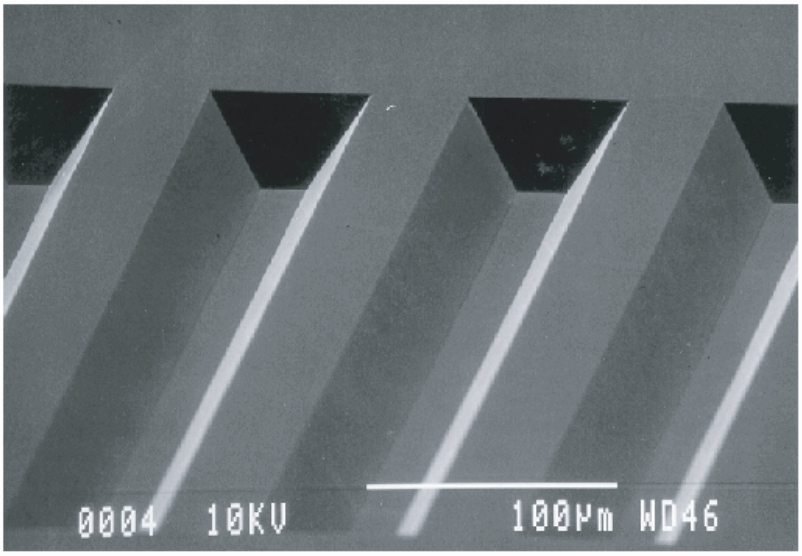


Figure 3.10: Scanning electron micrograph of micromachined grooves in (001)-oriented silicon, etched with 25% TMAH [57]. The crystal orientation dependence of etch profile can be clearly seen.

Etch uniformity is better than $\pm 5\%$ and Si:SiO_2 selectivity of more than 150:1 [61] is achievable. Typical silicon to photoresist selectivity is 50:1. A picture of the DRIE system of the Solid-State Electronics Lab, University of Michigan, Ann Arbor is shown in Fig. 3.12(a), and its schematic is shown in Fig. 3.12(b) [62, 63]. The wafer is loaded into the process chamber through a load station chamber. The loaded wafer (4 in. diameter) is mechanically clamped to the electrode using 8 alumina finger clamps, and the process chamber is pumped down to the preset base pressure (0.2 mT for all the work presented in this dissertation). High-density, low-pressure, and low-energy plasma is driven inductively with an RF power source operating at 13.56 MHz, and is accelerated by another RF source connected to the electrode. The wafer chuck is cooled to liquid nitrogen temperatures (77 K). Using helium gas under the wafer to transfer heat, the wafer's temperature is maintained at cryogenic temperatures throughout the process [64]. The cryogenic cooling enhances condensation of reactant gases and as a result, protects sidewalls from etching to achieve anisotropy [61].

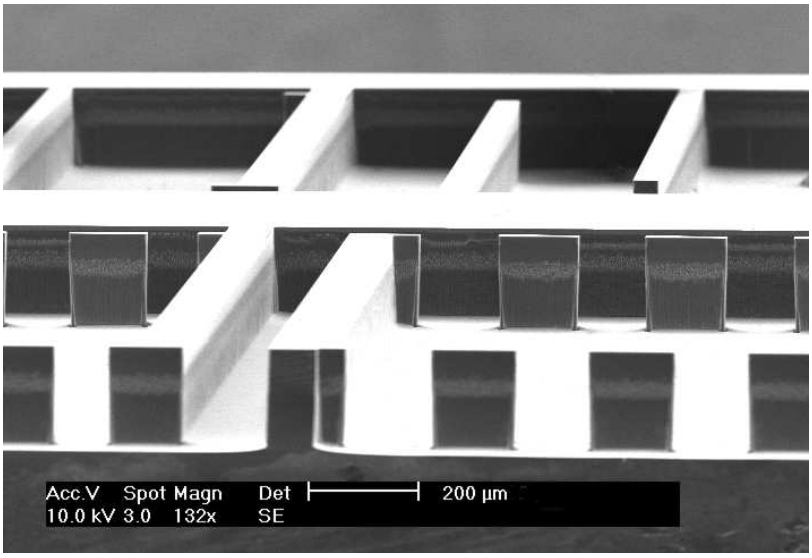
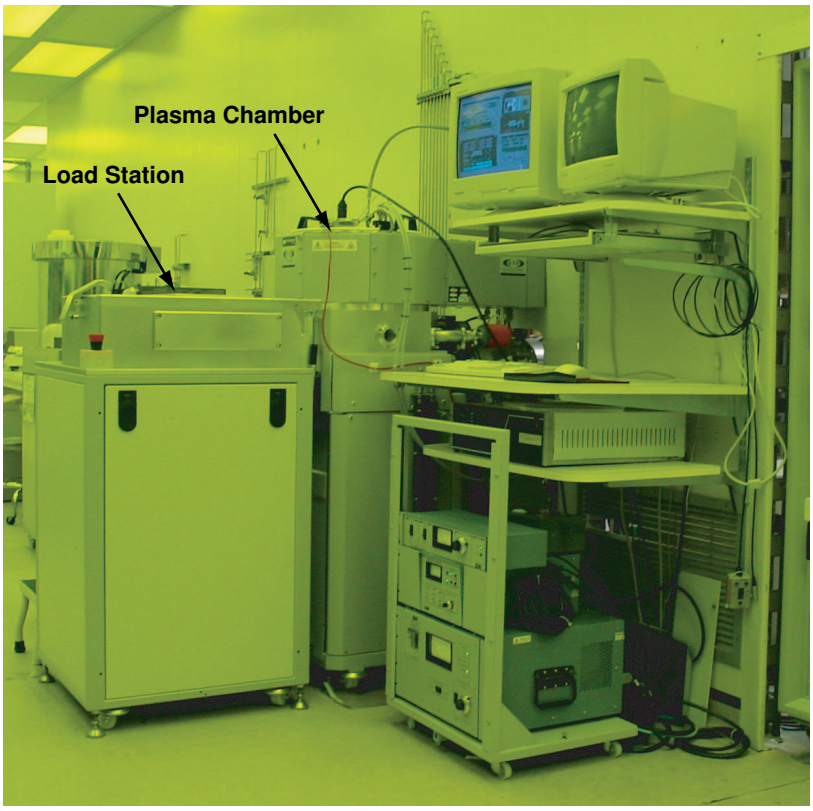
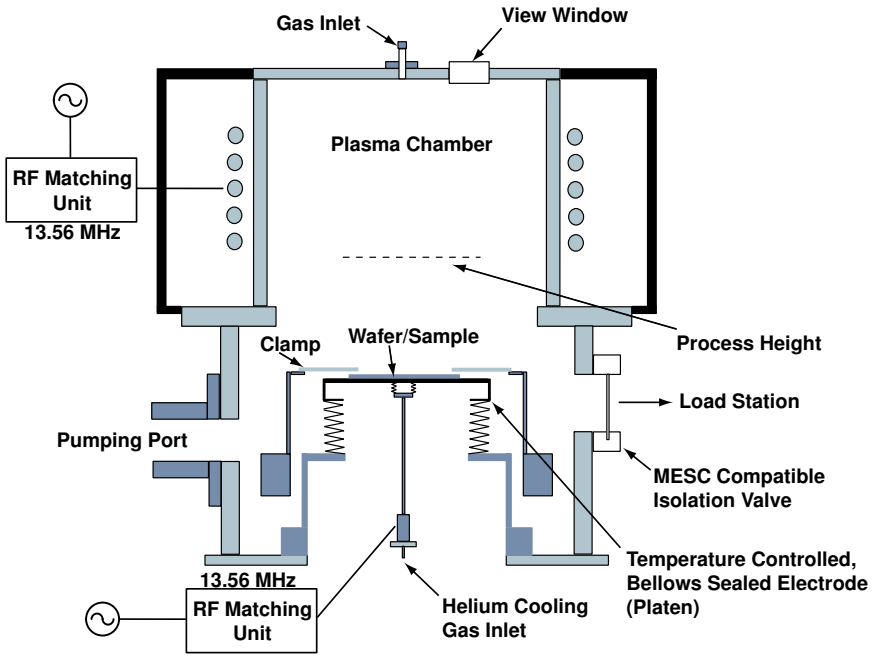


Figure 3.11: Scanning electron micrograph of micromachined silicon feature via deep reactive ion etching (DRIE) [58]. DRIE is capable of developing features in silicon with vertical sidewalls.

The silicon etching process in the DRIE technique consists of an etching cycle flowing only SF_6 and a sidewall passivating cycle flowing only C_4F_8, known as the "Bosch process" [60] or time multiplexed deep etching (TMDE) [65]. High etch rate is achieved by the fluorine-rich gas (SF_6) during the etching cycle, and anisotropy is achieved by the deposition of Teflon-like inhibiting films during the passivating cycle. During the etching cycle, bombardment of the accelerated ions removes passivating film preferably from the wafer surfaces, and further etches silicon by breaking the bond between silicon atoms. The DRIE tool can either be operated with a predetermined pressure levels for both cycles, or with the automatic pressure control (APC) valve fixed at an angular position. In the first case, the position of the APC valve position will vary in each cycles to maintain the preset pressure level whereas in the latter case, the pressure levels are determined by the gas flow rates. Higher APC valve angles correspond to higher chamber pressures for the same gas flow rates. The etch mechanism is a combination of physical sputtering of silicon and thermal reaction between silicon and the reactive fluorine radicals. The etch characteristics



(a)



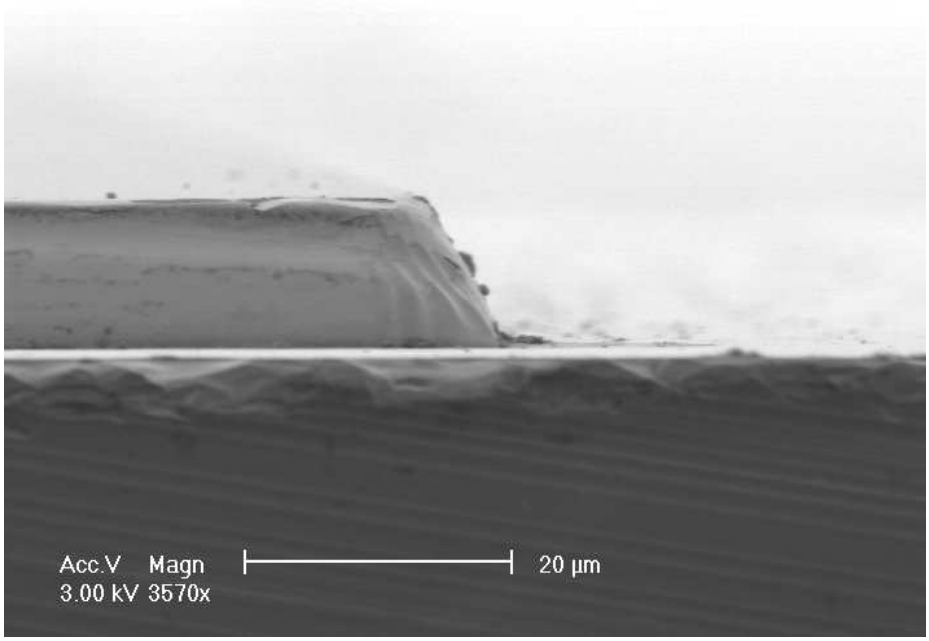
(b)

Figure 3.12: Deep reactive ion etching (DRIE) system by Surface Technology System (STS).

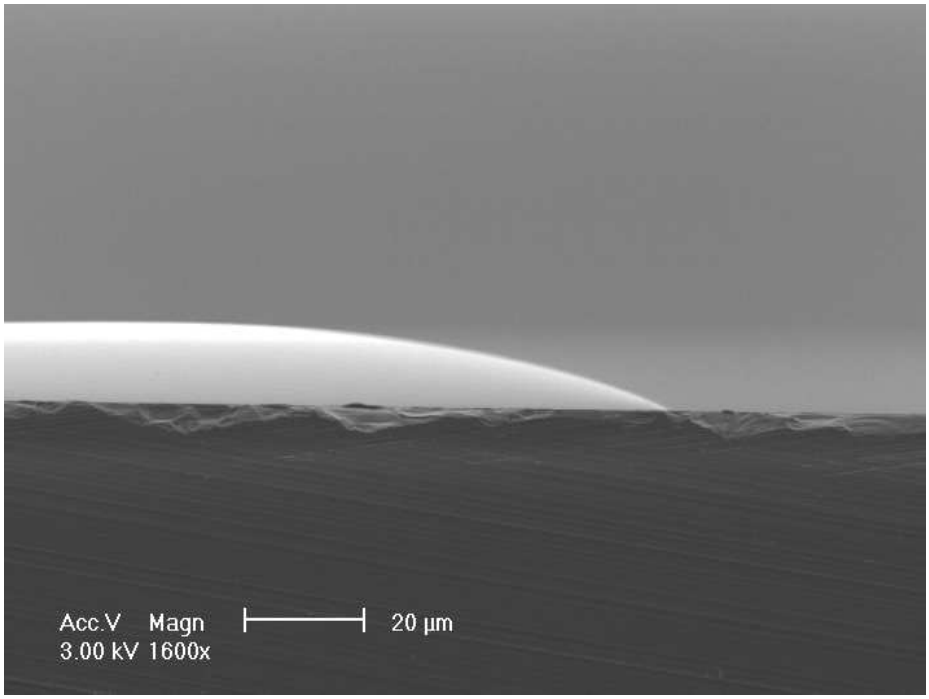
such as etch rate, sidewall profile (anionotropy), undercut, uniformity, selectivity, surface roughness, and critical dimension control depend on various conditions : gas flow rates, pressure levels, etching cycle duration, passivating cycle duration, switching time between the two cycles, platen power, coil power, mask type, exposed silicon area, platen temperature, etc. In general, by tailoring such conditions, the ion bombardment as well as the formation and preservation of protective films on the sidewalls can be controlled, thus the etch characteristics.

Due to the alternation of etching and passivating cycles in time multiplexed deep etching systems and to the spontaneous nature of the etch in fluorinated chemistries, resulting structures of DRIE exhibit horizontal scalloping on the sidewalls. It has been reported that the depths of such scallop range from 50 nm up to 300 nm [65]. Also, since physical sputtering of the substrate is the primary etch mechanism in all plasma-assisted etching systems, the surface of etched features exhibit roughness that is usually worse than that of a wet chemically etched surface. Although DRIE surface roughness can be improved to some degree, the surface roughness for the recipe utilized in this dissertation is known to be approximately twice the roughness of wet etched (tetramethyl ammonium hydroxide, TMAH) surface [57]. Certainly, the surface roughness is one of the most critical issues when developing micromachined waveguides via DRIE, the loss of which largely depends on surface roughness of the walls. This becomes especially important at very high frequencies when the wavelengths become very small.

In addition to the scalloping due to the inherent characteristics of time multiplexed deep etching systems, vertical striations known as “roughening bands”on the sidewalls of DRIE trenches also contribute to the sidewall roughness. This is caused by the plasma damage to the etch mask (photoresist) during the etching cycle which then leads to the uneven receding of photoresist as the etch proceeds. As a result, the uneven patterns at the photoresist edges are transferred to the sidewall of the etched feature. This becomes worse when the photoresist is hard baked prior to the etching process. Historically, researchers of



(a) No hard bake.



(b) Hard baked for 8 min. in a 120°C oven.

Figure 3.13: Profile of Clariant AZ9260 photoresist spun at 2k rpm.

Radiation Lab have been using quarter pieces of 4 in. silicon wafers. Since the STS DRIE system only accepts 4 in. full wafers, the wafer has to be bonded to a 4 in. carrier wafer prior to loading. This has been done by bonding the two wafers using photoresist followed by a hard bake. Thus, the patterning photoresist is also hard baked during wafer mounting process. Hard baking is used to further remove solvents inside the photoresist, to improve adhesion of the photoresist to the substrate, and to increase both chemical and physical etch resistance of the photoresist. However, the edge profile of the patterned photoresist profile deteriorates when it is hard baked, as shown in Fig. 3.13. AZ9260 photoresist by Clariant was spun at 2000 rpm, and soft baked for 4.5 min on a 110°C hot plate. The resist was exposed for 2 min. at an UV intensity of 20 mW/cm^2 and was developed in AZ400K:H_2O (1:3). Fig. 3.13(a) show the photoresist profile when the resist was not hard baked and Fig. 3.13(b) show when the resist was hard baked for 8 min. in a 120°C oven. Although not shown, the photoresist profile remain almost the same as in Fig. 3.13(b) even for a longer hard baking time, 40 min. for example. The vertical striations can be clearly seen in Fig. 3.14 that displays the sidewall of a micromachined WR-10 waveguide half, developed via DRIE. As is evidenced in Fig. 3.14, the vertical striations are usually worse near the photoresist interface.

This sidewall roughness can be improved by introducing a secondary hard mask, such as a thermal SiO_2 layer [65]. Also, it has been the author's experience that by tailoring

Table 3.3: Investigated deep reactive ion etching recipes.

	Recipe 1		**Recipe 2** [66]	
Parameters	**Passivating**	**Etching**	**Passivating**	**Etching**
Time	7 sec.	13 sec.	11 sec.	14 sec.
Overlap	0	0	0	0.5 sec.
Gas Flow	85 sccm	160 sccm	40 sccm	105 sccm
Electrode Power	0 W	25 W	6 W	12 W
Coil Power	600 W	800 W	600 W	750 W
APC Angle	67%	67%	65%	65%

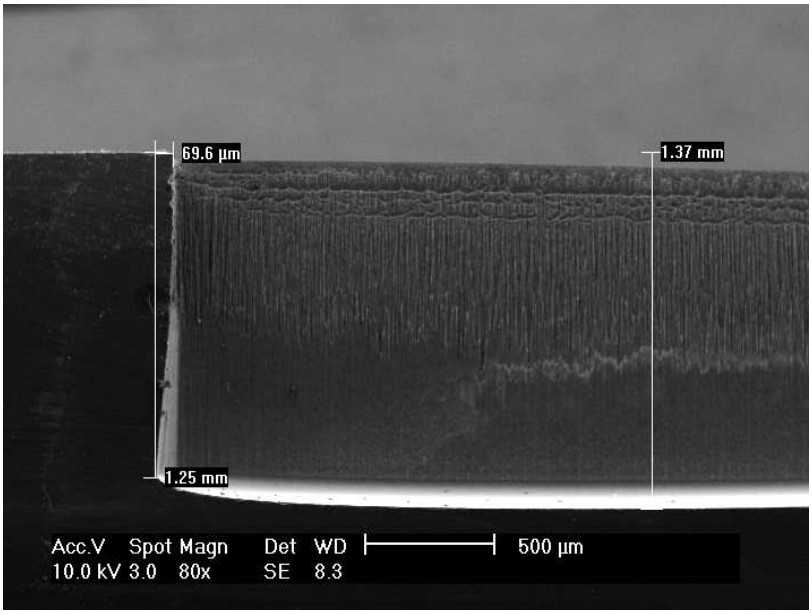


Figure 3.14: Scanning electron micrograph of sidewall of a DRIE feature. Approximately 20 μm of hard baked photoresist was used as a masking layer.

the etch conditions for a lower etch rate, the sidewall roughness can further be improved. Table 3.3 summarizes two DRIE recipes that have been investigated. Recipe 1 is utilized in all the DRIE work presented in this dissertation. Recipe 2 [66] has been investigated to improve sidewall roughness and to achieve more vertical sidewall profiles. The recipe can be used to develop micromachined WR-3 waveguides (220-325 GHz), which remain as a future work. The major differences between the two recipes are in cycle durations, gas flow rates, and electrode power for both cycles.

Compared with Recipe 1, the passivating cycle is longer in Recipe 2 although the etching cycle durations of the two are approximately the same. As the etch proceeds and the trenches become deeper, the reactive species tend to stay longer at the bottom of the trenches. Thus, DRIE profiles tend to be somewhat negative, or reentrant. Longer passivating cycles provide lower etch rates and less negative (reentrant) etch profiles since thicker passivating films are deposited on the sidewalls to prevent from etching. Obviously, longer passivating cycles will give lower etch rates, since the passivating films will be thicker not

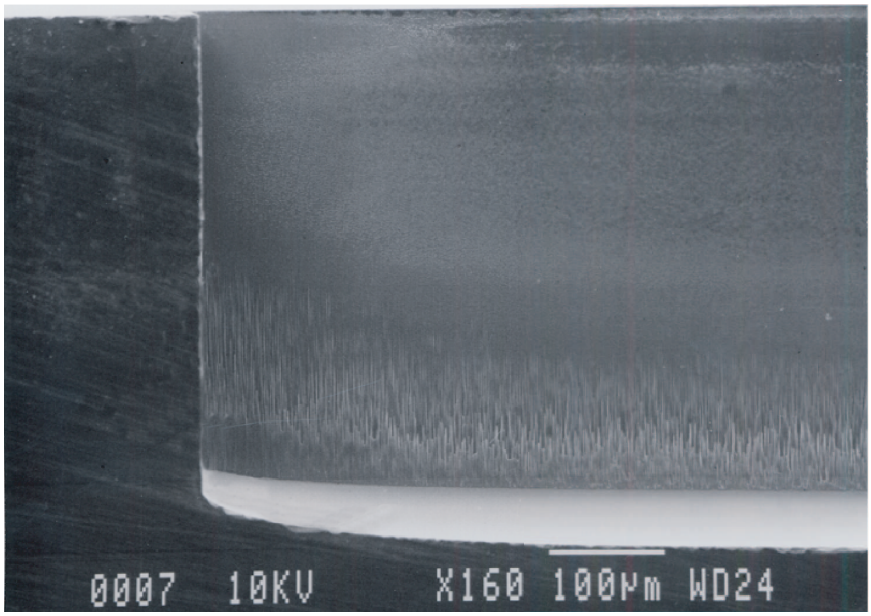
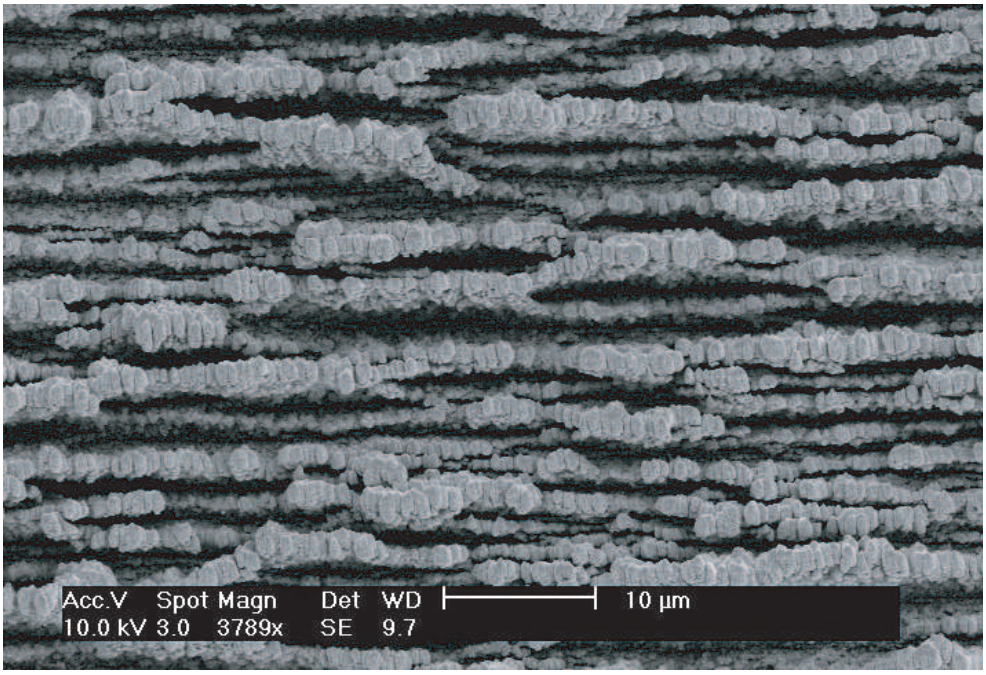


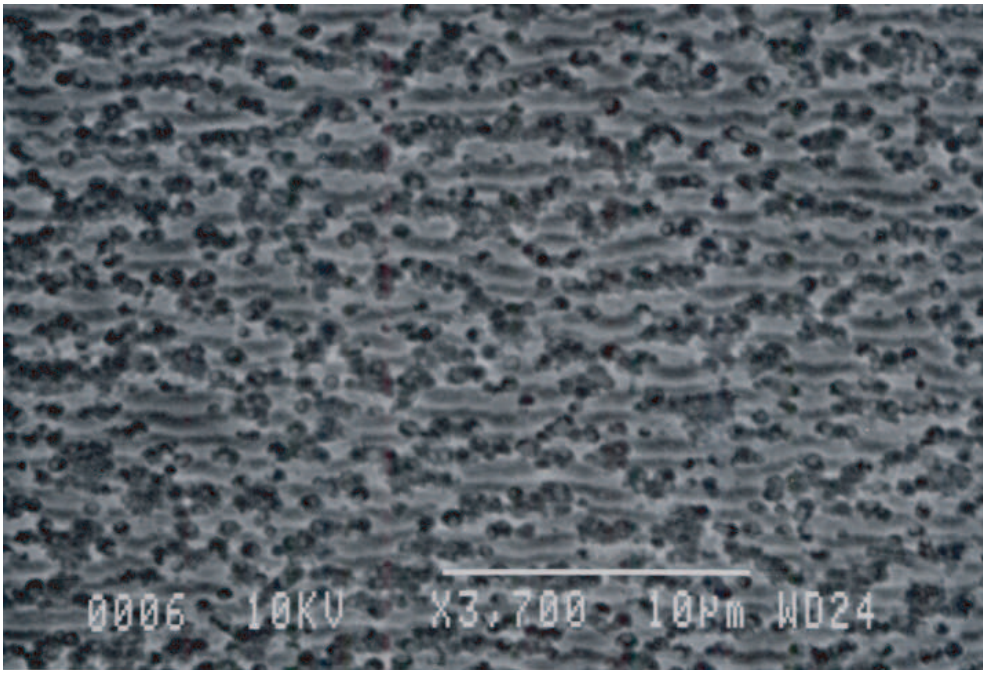
Figure 3.15: Scanning electron micrograph of sidewall of a DRIE feature with Recipe 2 in Table 3.3. 8000 Å of thermal oxide was used as a making layer in addition to photoresist.

only on the sidewalls but also on the etch surface. The gas flow rates are reduced substantially in both passivating and etching cycles of Recipe 2, as well as the electrode power of the etching cycle, which also reduces the etch rate. The plasma densities are expected to be roughly the same since the coil power are almost the same. For the investigated recipes, the APC valve was fixed at a preset angular position thus the chamber pressures were determined by the gas flow rates. Since the gas flow rates are substantially lower in Recipe 2 for both cycles, and the APC valves are set at approximately the same positions, chamber pressure levels of Recipe 2 are expected to be lower.

Shown in Fig. 3.15 is a scanning electron micrograph of the sidewall of a silicon micromachined WR-3 waveguide developed via DRIE using Recipe 2. Rectangular apertures were opened in 8000 Å thick thermal oxide by standard lithography and conventional reactive ion etching (RIE) during which approximately 12 μm of photoresist serving as the etch masking layer. The 2 mm silicon wafer was then mounted on a 4 in. carrier wafer,



(a) After 5.5 hours of etching with Recipe 1 in Table 3.3.



(b) After 3.7 hours of etching with Recipe 2 in Table 3.3.

Figure 3.16: Close up of the sidewalls of DRIE features of recipes in Table 3.3.

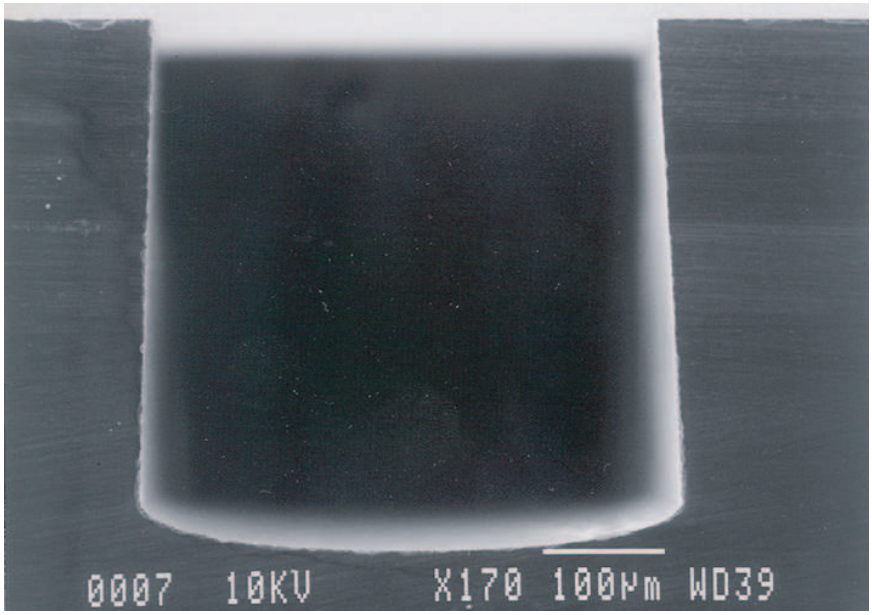
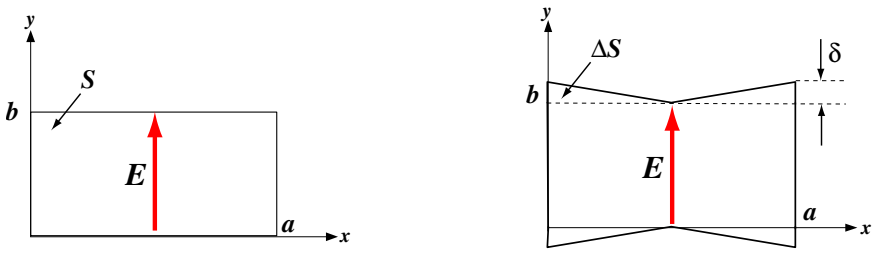


Figure 3.17: Scanning electron micrograph of sidewall of a WR-3 waveguide half developed via DRIE with Recipe 2 in Table 3.3. 8000 Å of thermal oxide was used as a making layer in addition to photoresist.

bonded with photoresist and hard baked. Top and bottom halves were etched down 430 μm at an average etch rate of 2 μm/min, which is roughly half the etch rate of Recipe 1. Finally, the wafer was diced to examine the sidewall roughness. Compared with Fig. 3.14, the sidewalls show less roughness, especially near the photoresist interface. The amount of vertical striations are reduced substantially, although they still appear near the bottom. Visually examining the micrographs in Fig. 3.16, there was a great improvement on the sidewall roughness of Recipe 2. As was done in [57], thorough investigations on the sidewall roughness of such DRIE features, taking into account the etching time, remain as a future work. Shown in Fig. 3.17 is a scanning electron micrograph of a WR-3 waveguide half developed via DRIE using Recipe 2, the depth of which is 430 μm. Compared with a WR-10 waveguide half developed via DRIE using Recipe 1 in Fig. 3.23, Recipe 2 results in a less negative and much more straight sidewall profiles. However, the slow etch rate of Recipe 2 makes it suitable for developing waveguides that require etch depths of about 400



(a) Rectangular waveguides. (b) DRIE waveguides.

Figure 3.18: Cross sections of rectangular waveguide and DRIE waveguide.

μm of less.

DRIE Waveguides

Shown in Fig. 3.18(a) is the cross section of a conventionally machined rectangular waveguide with the *E*-field vector of the dominant waveguide mode suggested by the arrow. Such waveguides can propagate transverse electric (TE) and transverse magnetic (TM) modes and have a unique characteristic that below cutoff frequencies, propagation is not possible. For a rectangular waveguide with such dimensions as in Fig. 3.18(a), the cutoff frequencies of the TE_{mn} or TM_{mn} mode for vacuum-filled waveguides are given as follows :

$$f_c = \frac{1}{2\pi\sqrt{\mu_o \varepsilon_o}} \sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2}, \tag{3.4}$$

where ε_o and μ_o are the permittivity and permeability of free space.

The propagation constant (β), guided wavelength (λ_g), and TE_{mn} mode characteristic impedance (Z_{TE}) of a waveguide are given as follows :

$$\beta = k_o \times \sqrt{1 - \left(\frac{f_c}{f}\right)^2}, \tag{3.5}$$

$$\lambda_g = \frac{\lambda_o}{\sqrt{1-\left(\frac{f_c}{f}\right)^2}}, \tag{3.6}$$

$$Z_{\mathrm{TE}} = \frac{\eta_o}{\sqrt{1-\left(\frac{f_c}{f}\right)^2}}, \tag{3.7}$$

where $k_o = \omega\sqrt{\mu_o\varepsilon_o}$, λ_o, $\eta_o = \sqrt{\frac{\mu_o}{\varepsilon_o}}$ are the free-space propagation constant, wavelength, and wave impedance.

As will be shown in later sections, the trenches formed with the DRIE recipe utilized in this work show somewhat negative or reentrant profiles. This is due to a relatively long etching cycle duration (13 sec.) compared with the passivating cycle (7 sec.). The trench slopes have dependence on several etch conditions, especially on coil and electrode power, the ratio of etching cycle duration to passivating cycle duration, and chamber pressure [67]. By controlling such conditions, the trench slopes can be made nearly vertical.

Assuming that DRIE gives reentrant profiles (see Fig. 3.23), flaring out by δ for an etch depth of $a/2$. The cross section of a resulting DRIE waveguide is shown in Fig. 3.18(b). The cutoff frequency of such "perturbed" geometry (DRIE waveguide) can be approximated by the cutoff frequency (f_c) of "unperturbed" geometry (rectangular waveguide) using perturbation method, and can be expressed as [68]:

$$\frac{\Delta f_c}{f_c} \approx \frac{\iint_{\Delta S}\left(\mu_o|H_o|^2 - \varepsilon_o|E_o|^2\right)dS}{\iint_S\left(\mu_o|H_o|^2 + \varepsilon_o|E_o|^2\right)dS}, \tag{3.8}$$

where E_o and H_o represent the fields of the original geometry.

When $\delta \ll b$, then the change in the geometry (ΔS) is negligible compared with the original geometry (S). Assuming that the field in ΔS can be considered as constant, Equation 3.8 can be simplified as (see Appendix B) :

$$\frac{\Delta f_c}{f_c} \approx \frac{\delta}{2b} \cdot \frac{\lambda_o^2\beta^2 - 4\pi^2}{\lambda_o^2\beta^2 + 4\pi^2} \cdot \sin^2\left(\frac{3m\pi}{4}\right), \tag{3.9}$$

where λ_o is the free-space wavelength.

Using the above equation, the first two cutoff frequencies of a WR-10 rectangular waveguide and a DRIE WR-10 waveguide, with a=2.54 mm, b=1.27 mm, and $\delta = 80\mu m$ have been calculated. The cutoff frequencies of both waveguides are calculated with Ansoft HFSS and summarized in Table 3.4. As can be noticed, the perturbation method results reasonably agrees with Ansoft HFSS results. However, the perturbation method result starts to deviate as the variation of the field in ΔS becomes larger for the TE_{20} mode.

As is noticed from Table 3.4, the cutoff frequencies of a DRIE waveguide are nearly the same as those of a rectangular waveguide, exhibiting a single-mode bandwidth that is close to 2:1 single-mode bandwidth of a rectangular waveguide. Although not shown here, the propagation constant (β, Equation 3.5) and the TE_{10} mode impedance (Z_{TE}, Equation 3.7) of a DRIE WR-10, obtained using the cutoff frequency in Table 3.4, are also in good agreement with those of a conventional WR-10.

3.4 Transition to a Micromachined Waveguide

In Section 3.1, the advantages of rectangular waveguides over popular planar transmission lines have been discussed. The advantages are especially important for very high frequency circuits where the loss of planar transmission lines become excessively large.

Table 3.4: The first two cutoff frequencies ([GHz]) of a WR-10 rectangular waveguide and a DRIE WR-10 waveguide.

	Analytic		**HFSS**	
Mode	**Rectangular**	**DRIE**	**Rectangular**	**DRIE**
TE_{10}	59.02	58.08	59.01	57.57
TE_{20}	118.03	116.17	118.03	110.75

Unfortunately, as the operating frequency is pushed toward the THz region, small waveguide dimensions make it difficult and costly to conventionally machine rectangular waveguides to tight dimensional tolerances. There has been an ongoing effort to develop waveguides using various low-cost micromachining techniques including those described in [69] and [70]. However, in these works, the waveguide heights were determined by the limited thickness of photoresist, resulting in reduced-height waveguides at *W*-band which suffer from higher attenuation and mismatch loss. This limitation on achievable waveguide dimensions through micromachining can be overcome by adapting the "snap-together" technique [71–74], which is to fabricate micromachined waveguides in two halves and put the two halves together to form a complete waveguide block. Therefore the depth/height that needs to be achieved by micromachining is reduced to the half of the standard waveguide dimensions thus making it possible to develop micromachined waveguides even at relatively lower frequencies, *W*-band for example [75, 76].

An alternate technique that has the potential to satisfy the needs for fabrication of low-cost high-performance micromachined waveguides is deep reactive ion etching (DRIE) introduced in the previous section. DRIE is capable of etching trenches with vertical sidewall profiles. Hence, micromachined waveguides developed via DRIE have cross sections that are identical to those of conventionally machined waveguides. this circumvents the bandwidth compatibility issue that the diamond shaped waveguides [75] have. Also, the relatively fast etch rate and high selectivity of DRIE provide the ability to develop full-height waveguides which overcomes the high attenuation and mismatch loss issues. Therefore, DRIE is a promising technique for fabrication of high-performance micromachined rectangular waveguides.

The FGC line to waveguide transitions presented in the previous section is converted to a fully micromachined version in this section. Waveguides are developed via DRIE, the cross section of which resembles that of a conventionally machined waveguide.

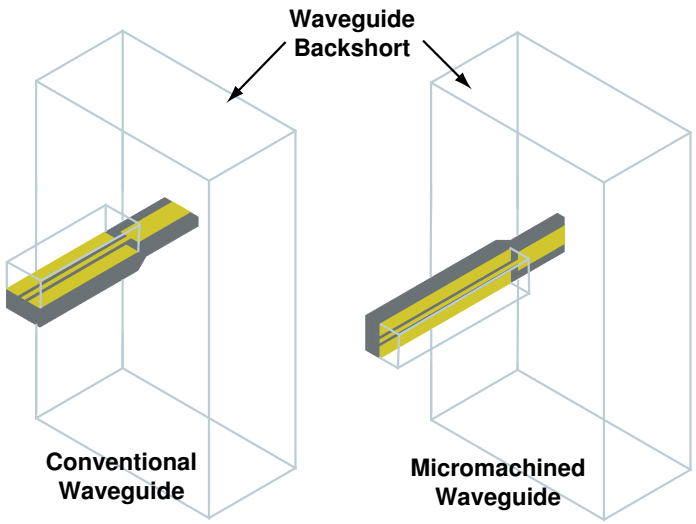


Figure 3.19: Drawing of transition to a conventional waveguide (left) and to a micromachined waveguide (right). For a fully micromachined transition, the rectangular probe is rotated 90°.

3.4.1 Motivation

To develop a fully micromachined version of the FGC line to waveguide transitions investigated in Section 3.2, the transition was designed with probe rotated 90°. As shown in Fig. 3.19, the transition probe to conventionally machined waveguides was facing the waveguide backshort. 90° rotated probes are preferred to fully micromachine such a transition since, from a fabrication standpoint, then the length (channel) of a waveguide is compliant in the plane of the wafer. Full-wave simulation results of FGC line to conventional waveguide transition via 90° rotated probe, although it requires different matching parameters, nevertheless show excellent transition performance across the entire waveguide band.

A fully micromachined transition has been demonstrated by Becker *et al*. [77] where the waveguide halves were micromachined in (001)-oriented silicon via wet anisotropic etching, resulting in a waveguide with a diamond-shaped cross section. Such waveguides have several advantages. They are simple to fabricate and can be easily fashioned into microma-

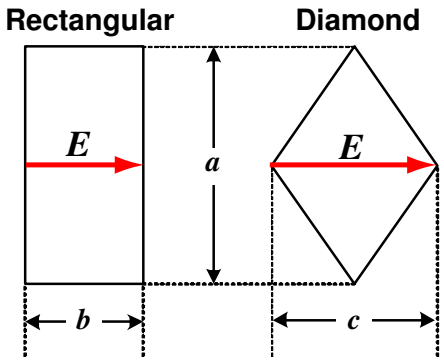
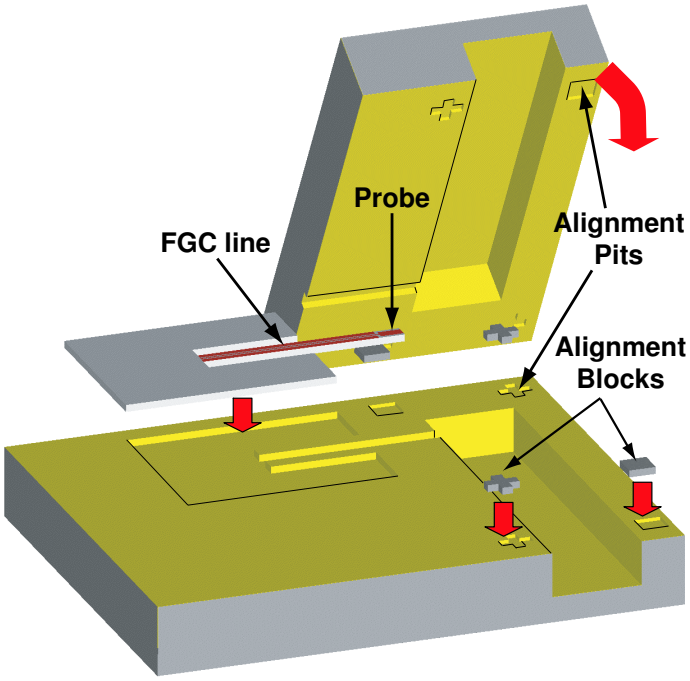


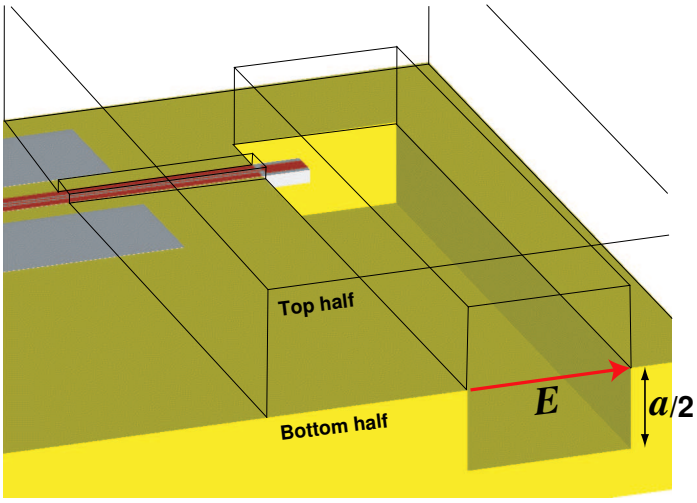
Figure 3.20: Cross sections of conventional rectangular waveguide and diamond-shaped micromachined waveguide. The *E*-field vector of the dominant waveguide mode is suggested by the arrow for each type.

chined horn antennas. In addition, the sidewalls in the etched feature are very smooth since wet chemical etching relies on the selectivity of the etchant to crystal orientation. This is of critical importance since the loss in a waveguide is dominated by the surface roughness of its sidewalls [55].

However, due to the fact that its height (the *c* dimension in Fig. 3.20) is determined by the width (*a* in Fig. 3.20), the diamond-shaped waveguide has a limited single-mode bandwidth of approximately 1.33:1. This can be problematic as the bandwidth is significantly less than that of a standard waveguide, especially in applications that operate across an entire waveguide band. In rectangular waveguides, the height of the narrow wall (*b* in Fig. 3.20) is chosen to establish a 2:1 frequency range of single-mode operation. For the fully micromachined transition version investigated in this section, waveguides are micromachined using a deep reactive ion etching (DRIE) technique, which does not depend on the crystal plane orientation. Therefore, micromachined waveguides that maintain a single-mode bandwidth of 2:1 can be developed, providing a better compatibility with conventional waveguide systems.



(a)



(b)

Figure 3.21: Schematic of the *W*-band fully micromachined transition structure utilizing DRIE waveguides. The top half is suggested in outline in (b).

3.4.2 Transition Design

The *W*-band FGC line to silicon micromachined waveguide transition module, utilizing only DRIE as a micromachining technique, is depicted in Fig. 3.21. A printed rectangular probe is fed by extending the center conductor of a shielded 50 Ω FGC line inserted into the DRIE WR-10 waveguide through its broadside wall, facing the narrow sidewall. The design of such a transition is based on matching the impedance of the FGC line to that of the waveguide. This can be done by by carefully choosing the size of the probe, the position of the probe within the waveguide, the distance between the probe and the waveguide backshort, and the dielectric constant and the thickness of the substrate supporting the probe.

Optimization of the transition design with a center frequency around 76 GHz was achieved with the help of Ansoft HFSS, the results of which with a 0.5 cm section of DRIE waveguide are shown in Fig. 3.22. The silicon under the probe was assumed to have a resistivity (ρ) of 2000 Ω·cm and loss tangent ($\tan\delta$) of 0.004. All metals were assumed to be gold(σ=4.1×10^7 $(\Omega\cdot\mathrm{m})^{-1}$, μ_r=0.99996) whereas the shielded FGC line was assumed to be lossless. Simulation results predict that the return loss of a single transition is better than 20 dB across the entire *W*-band, from 75 GHz to 110 GHz, with insertion loss better than 0.5 dB in the same frequency range. The size of the designed probe is 545 μm $\times$ 185 μm on a silicon substrate with a thickness of 100 μm, and the distance between the center of the probe and the backshort is 835 μm. The FGC line has center, slot, and ground strip widths of 50, 45, and 160 μm, respectively, and the height of the FGC line shield is chosen to be 100 μm in order to ensure single-mode propagation along the FGC line and maintain a 50 Ω impedance. The length of the extended center conductor of the FGC line feeding the probe is 95 μm. Arm-like appendages, as shown in Fig. 3.21(a), are developed on the probe structures for handling purposes as well as for proper placement of the structure in the probe cradle.

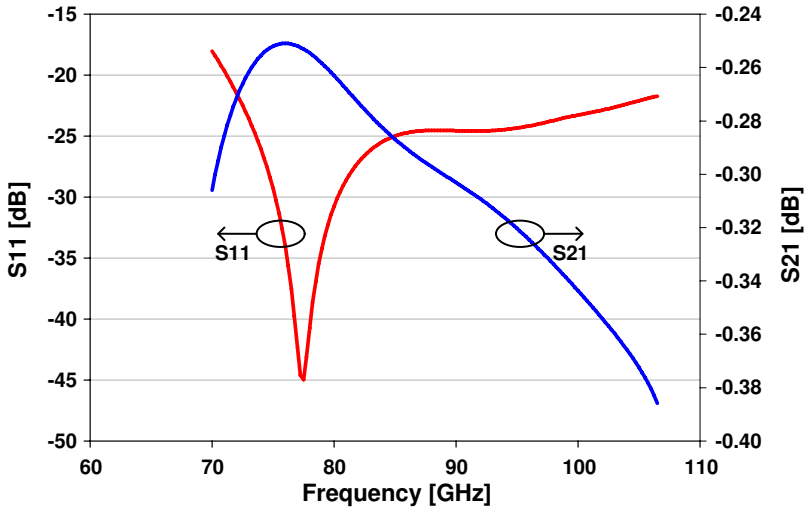


Figure 3.22: Simulated S_{11} and S_{21} of a single FGC line to DRIE waveguide transition with a 0.5 cm section of DRIE waveguide assuming gold metallization.

3.4.3 Fabrication

DRIE Waveguides

A back-to-back transition consisting of input and output FGC lines with a 1 cm section of micromachined waveguide in between the two transition probes was fabricated for measurement purposes. The top and bottom halves of the waveguide were etched via DRIE, at an etch rate of approximately 3.7 μm/min. The utilized DRIE recipe is Recipe 1 in Table 3.3. The etch depth for each waveguide half was 1.27 mm, which is one half of a standard *W*-band waveguide (WR-10) width. A high resistivity ($\rho > 1000\ \Omega\cdot$cm) silicon wafer with a thickness of 2 mm was used for the fabrication of these waveguide halves. Photoresist with a thickness of approximately 20 μm was used as a masking layer for the deep etch. A scanning electron micrograph of a micromachined DRIE waveguide half is shown in Fig. 3.23. As evidenced by this figure, deep etching with the utilized recipe (Recipe 1 in Table 3.3) shows a negative-sloped profile, flaring out approximately 80 μm on each side for an etch depth of 1.27 mm. However, it has been seen in Section 3.3 that such waveguides have characteristics that are nearly same as those of rectangular waveguides. Also, this negative

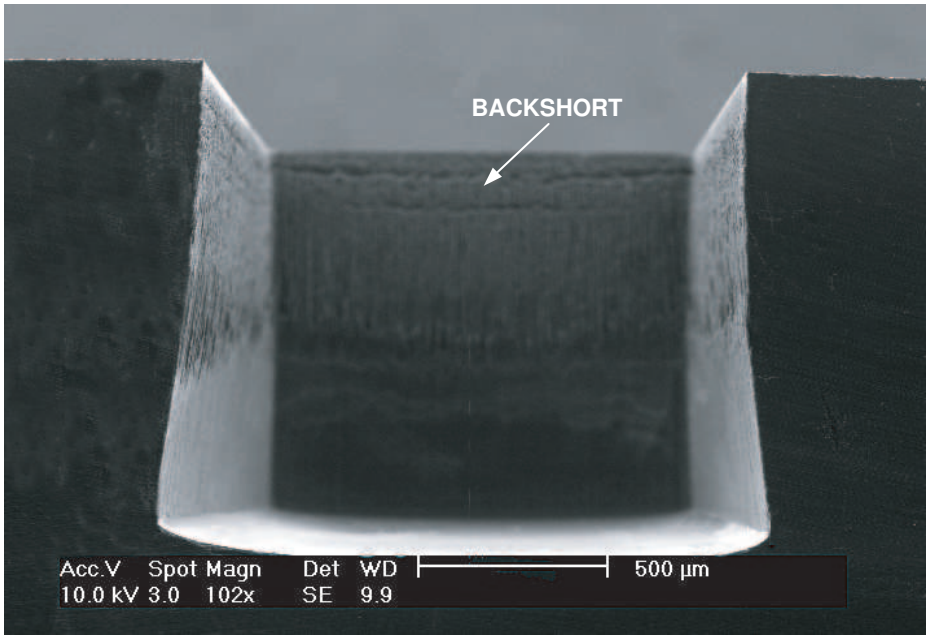


Figure 3.23: Scanning electron micrograph of a micromachined waveguide(WR-10) before metallization. Only the half is shown here. As can be seen, DRIE shows a negative-sloped profile with the utilized recipe.

etch profile was taken into account in the transition design and simulation.

Additional grooves were etched 100 μm deep by DRIE, for which photoresist with a thickness of 7 μm on top of a 3000 Å thick sputtered titanium layer served as masking layers. The grooves in the bottom waveguide half serve as the cradle where the fabricated probes are placed in, and the grooves in the top waveguide half serve as the shield for the FGC lines. At the same time that these grooves were formed, pits in forms of crosses and squares were etched on both top and bottom halves. For proper alignment of the two waveguide halves, 200 μm thick alignment blocks that have exactly the same cross sections as these pits will be placed in these pits that are half as deep, 100 μm. The alignment blocks were fabricated out of 200 μm thick silicon by deep etching around the pattern. By placing the alignment blocks in the correct pits on the top and bottom halves that are half as deep, both halves can be precisely aligned, thus forming a complete waveguide block. Shown in Fig. 3.24 is an alignment block placed in its pit that is half as deep as the thickness of the

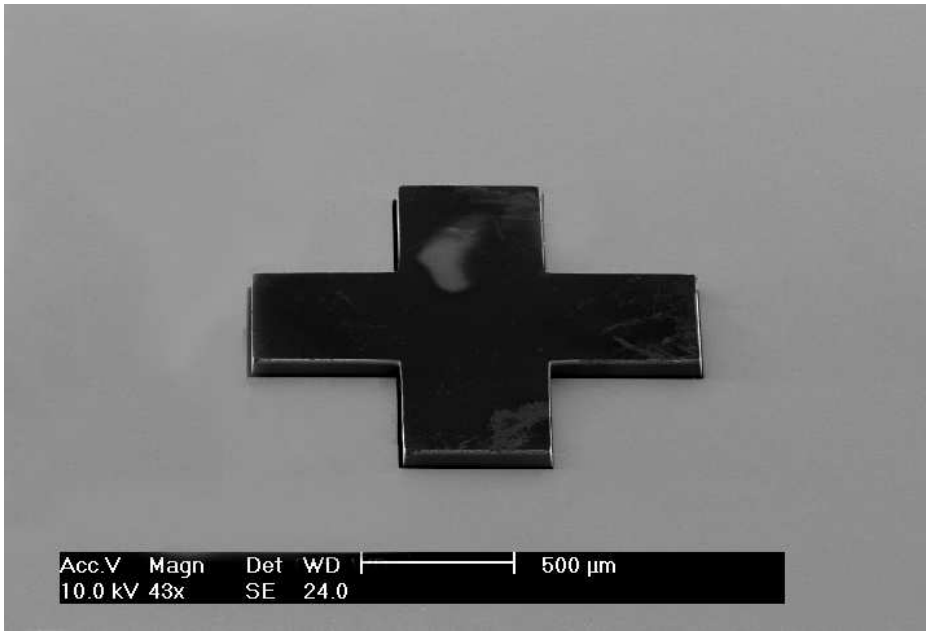


Figure 3.24: Alignment block placed in its cradle that is half as deep as the thickness of the block.

block.

The waveguide halves were then diced and finally, the waveguide walls and the grooves were sputtered with 500 Å of titanium and 1.6 μm of gold for metallization. Though not carried out in the reported effort, an additional step of bonding may be completed to ensure intimate contact between the two waveguide halves.

Transition Probes

The probes were fabricated on a high resistivity (ρ >2000 Ω·cm) silicon wafer with a thickness of 100 μm. To avoid the possibility of exposing gold inside the DRIE chamber, double side processing is required. Therefore, the alignment marks were first etched through by DRIE. Then on the top side of the wafer, the FGC line and the probe were patterned via standard lift-off process with 500 Å of titanium and 1 μm of gold. Then the wafer was flipped over for backside processing. Using the etched-through vernier and cross alignment marks, the substrate around the probe was etched through from the backside us-

ing DRIE. 100 μm thick silicon wafer pieces that have roughly the same size as the etching apertures are used to monitor deep etching and to obtain the desired depth of 100 μm. Finally, the remaining photoresist was removed in PRS2000 so that the probes are released from the wafer. For each process steps, the 100 μm thick silicon wafer was mounted on a 400 μm carrier wafer using photoresist.

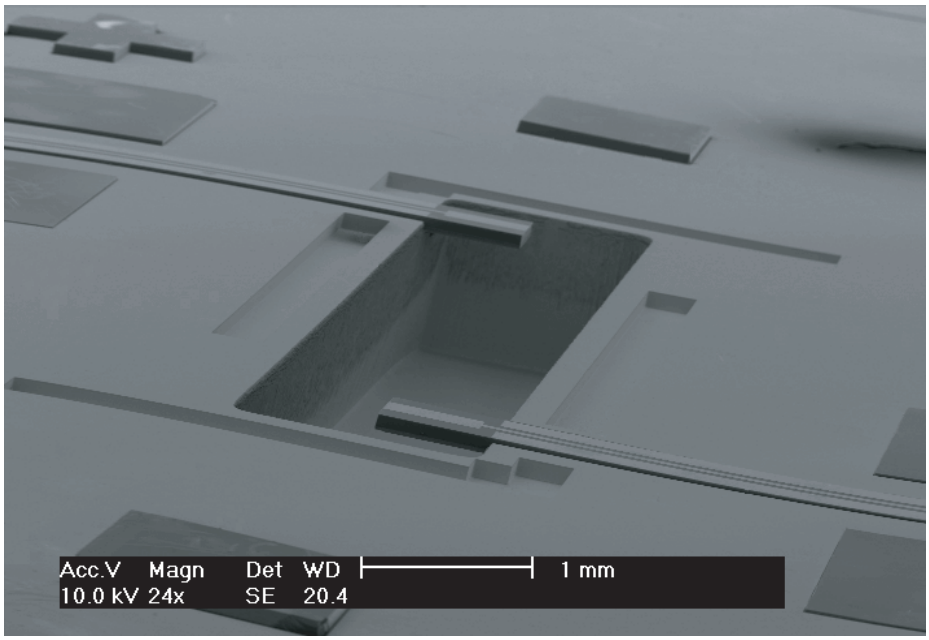
Shown in Fig. 3.25 is a scanning electron micrograph of a bottom half of a micromachined waveguide with fabricated probes placed in their cradles. Also displayed in Fig. 3.25 are alignment blocks in their alignment pits. Since the 200 μm-thick alignment blocks are placed in pits that are 100 μm deep, the upper half of these alignment blocks come up above the wafer surface by 100 μm. This can be clearly seen in this figure. The upper halves of these alignment blocks will fit in the 100 μm-deep alignment pits on the top waveguide half, enabling both waveguide halves to be aligned accurately.

3.4.4 Experimental Results

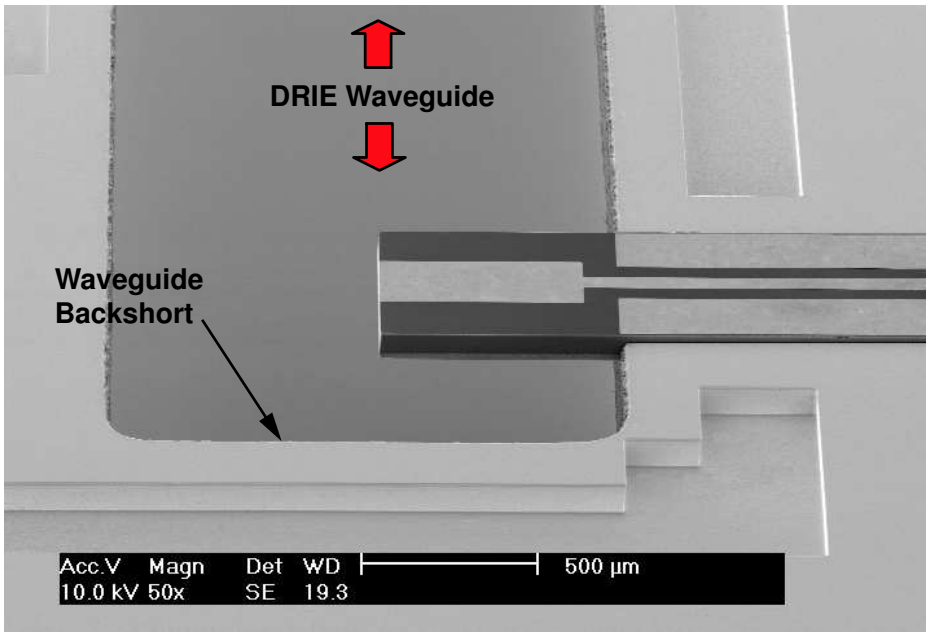
A fabricated transition in a back-to-back configuration (probe-to-probe) with a 1 cm section of DRIE waveguide between the two probes was measured in *W*-band using an HP8510C network analyzer and a set of ground-signal-ground model 120 GGB probes. Calibration was achieved with MultiCal [36], a thru-reflect-line (TRL) protocol, using on-wafer thru, short, and delay lines. The measured results are shown in Fig. 3.26. Loss in the FGC lines are calibrated out using the attenuation data provided by MultiCal, but the loss in the 1 cm section of DRIE waveguide is included in the results.

As can be seen from this figure, the back-to-back transitions show excellent performance across the entire waveguide band. The return loss is better than 10 dB in over 90 % of the *W*-band, with the insertion loss exhibiting better than 1.5 dB/transition (including the loss in 0.5 cm long DRIE waveguide) across the entire waveguide band, and better than 1 dB/transition in about 30 % of this band.

Compared with the performance of the similar transitions in Section 3.2 and in [77]



(a)



(b)

Figure 3.25: Scanning electron micrograph of a bottom half of a micromachined waveguide with probes placed in the cradles.

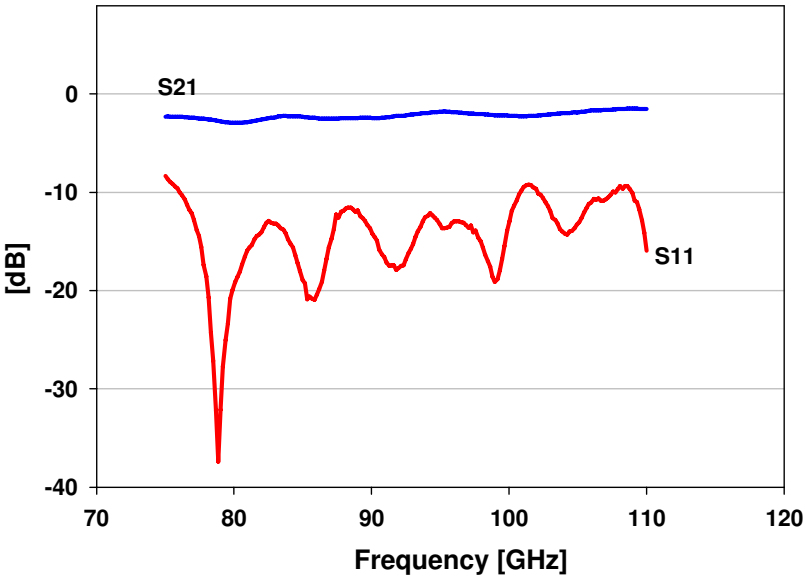


Figure 3.26: Measured results of a fully micromachined back-to-back FGC line to silicon DRIE waveguide transition.

where waveguides formed via wet anisotropic etching were employed, the insertion loss per transition of the investigated transition is somewhat higher. This is mainly due to the difference in the loss of waveguides. As can be seen from Fig. 3.23 and Fig. 3.25(a), the sidewalls of DRIE waveguides show some roughness, especially near the photoresist interface. As mentioned in Section 3.3, the roughness is caused by the imperfect side wall passivation throughout the DRIE process for the required high etch rate, and also by the plasma damage to the etch mask (photoresist) during the etching cycle which then leads to the uneven receding of photoresist as the etch proceeds. In addition, the alternating etching and passivating cycles of DRIE process forms scallops on the sidewalls [67], which also contribute to the sidewall roughness. Since the loss in waveguides is dominated by the surface roughness of the sidewalls, it is a reasonable expectation that the performance of the investigated transition will be significantly improved with the improvement of DRIE waveguide sidewall roughness through selection of the appropriate etch recipe and etch masks. Moreover, the transition performance can further be improved using wafer bonding

of the waveguide halves.

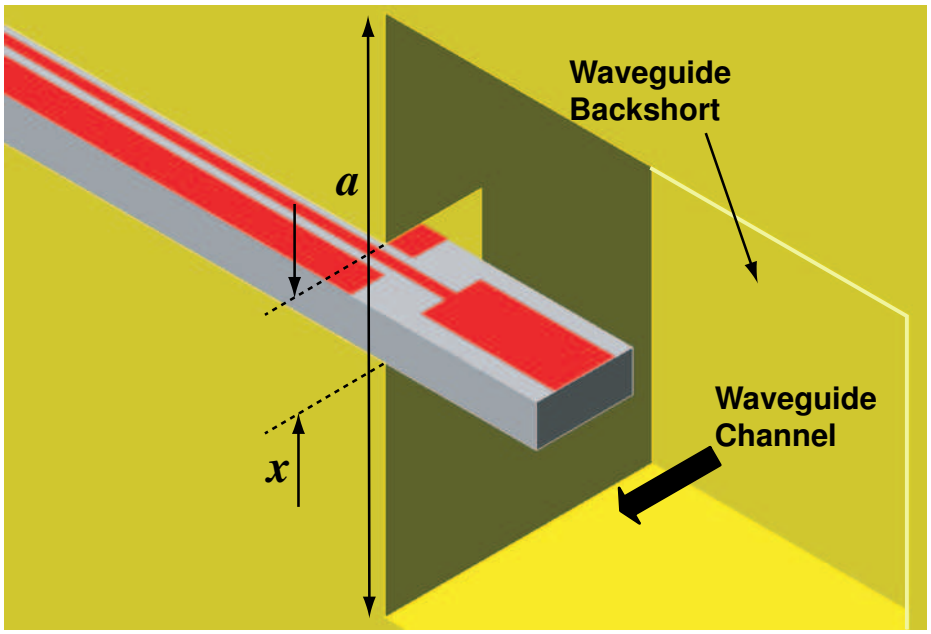
The performance of the transition to a diamond-shaped waveguide [77], in terms of bandwidth, is limited to the single-mode bandwidth(1:1.33) of the diamond-shaped waveguide itself. On the other hand, waveguides micromachined via DRIE enable the single-mode bandwidth to be the same as that of a standard rectangular waveguide. As a result, the investigated transition shows excellent performance across the entire waveguide band, from 75 GHz to 110 GHz.

The presented work also suggests that, along with other micromachining techniques including photolithographic techniques [69–72,74], wet silicon processing [73,75,76], X-ray lithography [78], and laser milling [79], DRIE is a relatively simple, yet another promising technique to develop low-cost high-performance micromachined waveguides especially at submillimeter and THz frequencies where the required etch depth is about 400 μm or less.

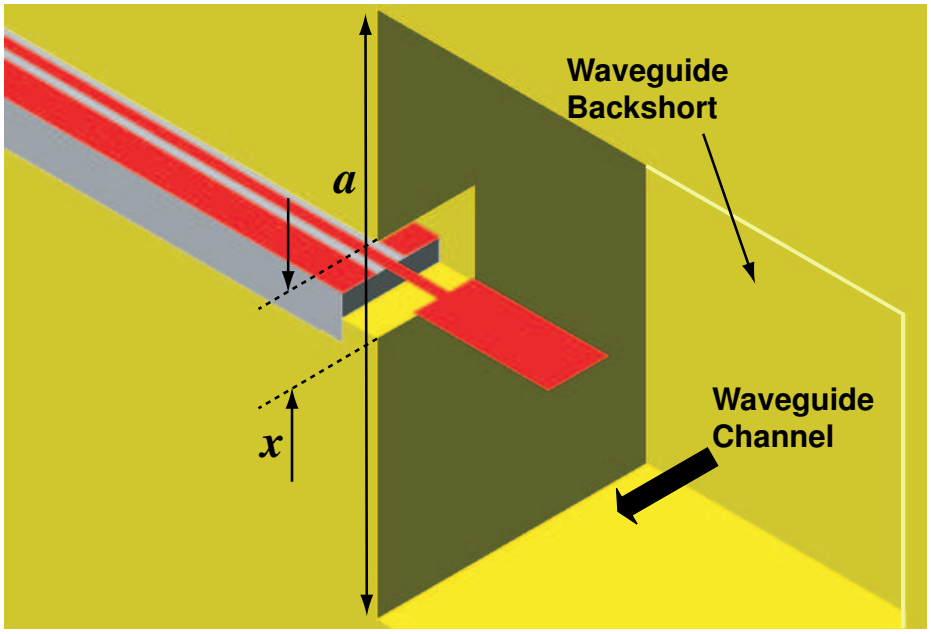
3.5 Transition for THz applications

3.5.1 Motivation

While the initial results of fully micromachined FGC line to waveguide transitions are encouraging, additional fabrication challenges exist for extending the transition to submillimeter and true terahertz frequencies. A major difficulty in the investigated transition is the required thinning of silicon wafer in order to achieve demonstrated transition performance. In Section 3.2, *Ka*-band probes were fabricated from 500 μm thick silicon and the silicon substrate under the probe was etched to half of the original thickness in order to improve the performance of the transition. As the *Ka*-band design was scaled down for operation in *W*-band in Section 3.4, the substrate under the probe had to be etched down to 100 μm, to provide a comparable level of performance. The thinned silicon substrates were difficult to fabricate from thicker wafers. In order to overcome this problem, the *W*-band probes were fabricated on a 100 μm, which made it unnecessary to thin down any part of the wafer. If



(a)



(b)

Figure 3.27: Drawing of close-up views of FGC line to waveguide transitions. Depicted in (b) is the case when free-standing probe is realized by completely removing the probe-supporting substrate.

the substrate supporting the probe is made even thinner as required at higher frequencies, it is expected that the transition performance will improve due to a reduction of the loss associated with the substrate. As we go higher in frequency, the substrate thickness under the probe has to be thinner in order to retain the same-scaled dimension. Also, as the operating frequency is increased, the substrate thickness under the probe must be thinner for the probe structure to properly fit within the waveguide whose dimensions must likewise shrink in accordance with the increased operating frequency. Eventually, complete removal of the substrate beneath the probe may in fact become necessary.

Another limitation of realizing such transitions at higher frequency lies on the size of the slot on a waveguide sidewall that is required to insert the probe. As conceived in Fig. 3.27(a), the width of this opening is the overall width of the FGC lines, whereas the height of this opening (x dimension in Fig. 3.27(a) is the thickness of the FGC line substrate and the height of the FGC line shield. For example, the width (a dimension in Fig. 3.27) of a WR-1, the dominant mode of which is to be operated 750 GHz up to 1.1 THz (1 THz=1000 GHz) is 254 μm. If the transition probe in Section 3.4 is designed for a WR-1 using, for example, 25 μm thick silicon substrate and 25 μm shield, the height of the slot will be 50μm. Practically, this is roughly the smallest possible slot height since from a fabrication standpoint, the substrate of the probe structure has to have a certain thickness to be properly handled. This implies that the height of the slot is larger than 1/10 of the waveguide width, which can lead to substantial amount of leakage loss through such a slot. Also, the waveguide will be partially filled up with probe-supporting dielectric, which result in excitation of spurious modes due to inhomogeneity and eventually impede effective transitions.

If the probe-supporting substrate is completely removed, as depicted in Fig. 3.27(b), the height of the slot can be reduced down to the height of the FGC line shield and the height required for the probe metal. Thus, by complete removal of the substrate, the height of the opening on a waveguide wall can be reduced to nearly half the height required for

a probe with supporting dielectric underneath. In addition, when the substrate under the probe is completely removed, the probe may have better mechanical strength than when it is etched locally and partially since the remaining substrate is of a single thickness. In this case, the metal probe has to have mechanical strength in order to be suspended in air. Also, control of the stress in the metal layers comprising the probe becomes crucial in preventing the suspended probe from warping.

In this section, the design, fabrication, and experimental results of a fully micromachined transition via a free-standing probe is demonstrated. By completely removing the substrate under the probe, the associated dielectric loss will be minimized, thus maximizing the transition performance. Such a structure is demonstrated to maintain its mechanical integrity. Moreover, the utilized free-standing probe proves the potential of such transitions to be applicable well into the submillimeter-wave and THz range.

3.5.2 Transition Design

A schematic diagram of the FGC line to silicon diamond waveguide transition is depicted in Fig. 3.28. The *E*-field vector of the dominant waveguide mode is suggested by the arrow. A free-standing rectangular probe is fed by extending the center conductor of a 50 Ω FGC line into the waveguide. The waveguide halves are micromachined in silicon via wet anisotropic etching, resulting in a waveguide with a diamond-shaped cross section. As mentioned in Section 3.4.1, such waveguides have reduced single mode bandwidth of approximately 1:1.33 due to the restrictions in the realizable geometry. However, this type of micromachined waveguides have several advantages over DRIE waveguides. They are simple to fabricate and can be easily fashioned into micromachined horn antennas. In addition, the sidewalls in the etched feature are very smooth. This is of critical importance since the loss in a waveguide is dominated by the surface roughness of its sidewalls [55].

The dimensions of diamond waveguide utilized in this section is chosen so that its width (*a* in Fig. 3.28) matches that of a standard WR-10 waveguide, 2.54 mm. This in turn de-

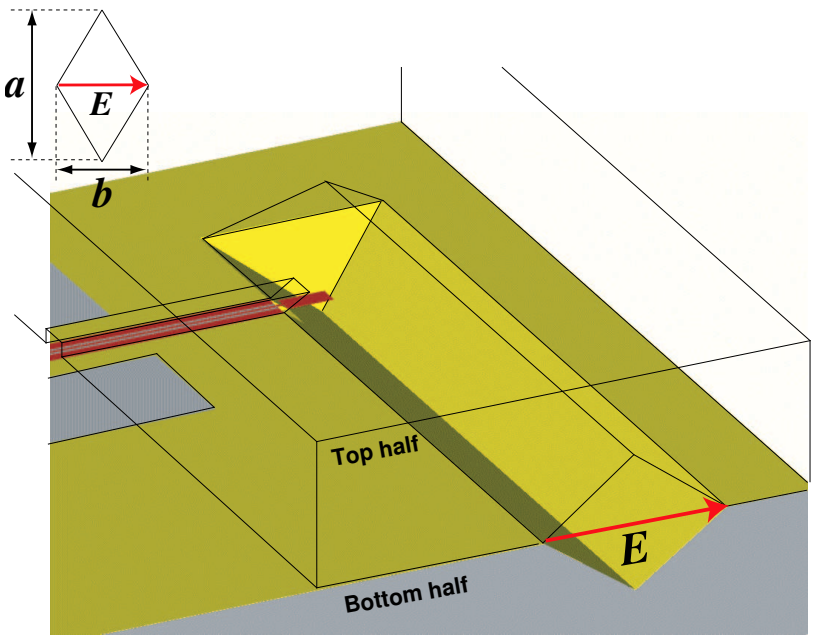


Figure 3.28: Schematic of the FGC line to diamond waveguide transition utilizing free-standing probe. The top half is depicted in outline. The waveguide halves are micromachined in 2 mm silicon via wet anisotropic etching.

termines its height (b in Fig. 3.28) to be 1.796 mm. The first two cutoff frequencies of a diamond waveguide with such dimensions, calculated by Ansoft HFSS, are 85.9 GHz and 113.8 GHz. Shown in Fig. 3.29 are the dominant mode impedances (Z_{pv}) of rectangular WR-10 waveguide, diamond waveguide (a=2.54 mm), and DRIE WR-10 waveguide with 80 μm of undercut (δ in Fig. 3.18(b)), calculated with Ansoft HFSS. The results show that the diamond waveguide exhibit a greater variation in the impedance with respect to frequency in its single mode band, than the rectangular waveguide and the DRIE waveguide. It is also evidenced from the figure that DRIE waveguides and rectangular waveguides have nearly the same dominant mode impedances, and that the impedance of a diamond waveguide is about 3 times higher than that of a rectangular waveguide .

Among the critical factors that affect the transition performance are the dielectric constant and the thickness of the substrate supporting the probe. If the substrate under the probe is thinned, or if a substrate material with a lower permittivity is used, less field will

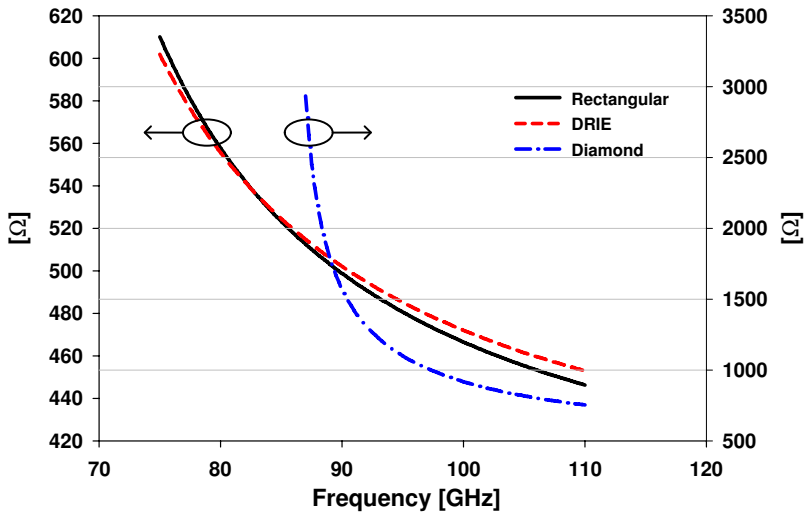


Figure 3.29: Calculated dominant mode impedances of rectangular WR-10 waveguide, diamond waveguide, and DRIE WR-10 waveguide.

be confined in the dielectric under the probe and thus the associated dielectric loss is reduced. As a result, the transition performance will improve.

In an effort to maximize the transition performance, the substrate under the probe was completely removed. An optimum transition design with the free-standing probe was achieved with Ansoft HFSS. The FGC lines have center/slot/ground widths of 50/45/160 μm and the designed probe size is 608 μm $\times$ 202 μm. The distance between the center of the probe and the backshort is 2.101 mm. The length of the extended center conductor of the FGC line feeding the probe is 170 μm, and the width of the micromachined waveguide (the *a* dimension in Fig. 3.28) is chosen to match that of a standard *W*-band waveguide (WR-10), 2.54 mm. The height of the waveguide (the *b* dimension in Fig. 3.28), 1.8 mm, is chosen by the height. The lowest two cut-off frequencies of a diamond waveguide with such dimensions, calculated with Ansoft HFSS, are 85.9 GHz and 113.8 GHz.

Simulated results of a single transition via a substrateless probe and 0.4 cm of diamond waveguide section are shown in Fig. 3.30. The shielded FGC lines were assumed to be lossless, where as the probe metal was assumed to be nickel with a conductivity of

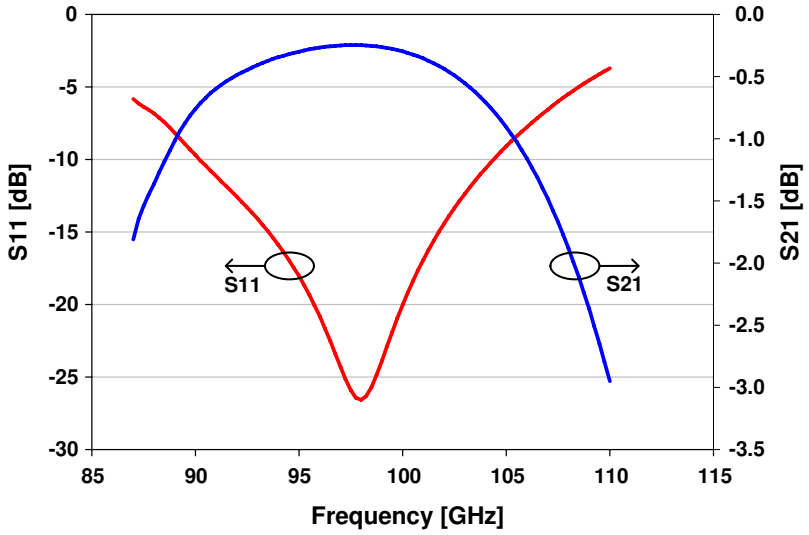


Figure 3.30: Simulated S_{11} and S_{21} of a single substrateless probe transition and 0.4 cm of diamond waveguide section.

1.45×10^{7} $(\Omega\cdot\mathrm{m})^{-1}$. The diamond waveguide surfaces were assumed to have a conductivity of 5×10^{6} $(\Omega\cdot\mathrm{m})^{-1}$, since such a conductivity gives the approximate loss of such a waveguide in its dominant mode bandwidth [75]. The simulation results predict that the transition performance be at its peak at around 97.5 GHz with an insertion loss of 0.25 dB and a return loss of better than 25 dB. As expected, the transition performance is degrading, as the frequency of operation is reaching the upper and lower cut-off frequencies.

3.5.3 Fabrication

For measurement purposes, back-to-back substrateless probe transition structures were fabricated with a 0.8 cm section of a diamond waveguide.

Free-standing Probes

The free-standing probes are fabricated out of (001)-oriented high resistivity ($\rho >$ 2000 $\Omega\cdot$cm) silicon wafer with a thickness of 100 μm, in a similar manner as in Section 3.4.3. To minimize the possibility of the mechanical deflection of the suspended probe,

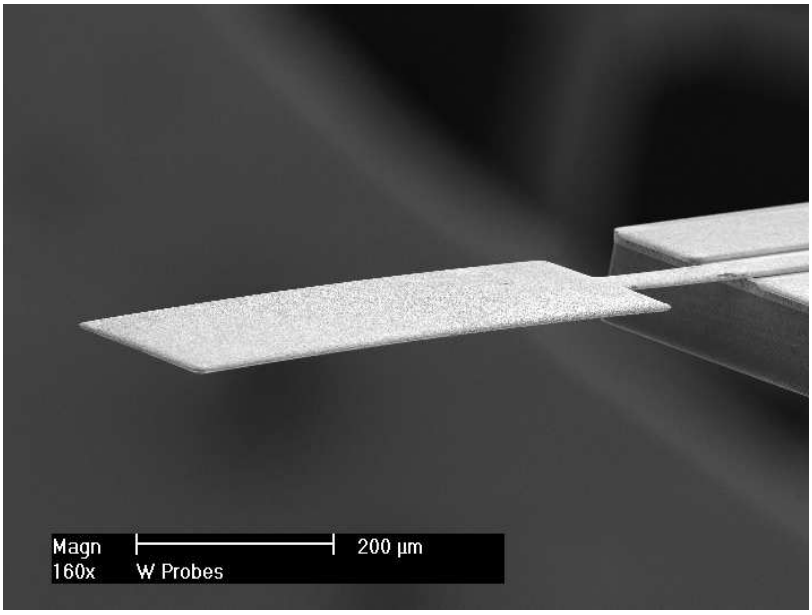


Figure 3.31: Scanning electron micrograph of a suspended metal probe formed by deep reactive ion etching of the underlying silicon substrate.

a relatively thick metallization is desired and realized through nickel plating. Approximately 8 μm of nickel was electroplated on top of 2000/500 Å titanium/nickel seed layers, at an electroplating rate of 0.13 μm/min. From an electrical loss standpoint gold is clearly preferred due to its higher conductivity. However, due to compatibility issues with the fabrication processes of other researchers in our shared facility, gold was not allowed to be used in the deep reactive ion system. In addition, stresses in the metal layers of the metal pattern are a critical issue in fabricating these air-suspended probes. Also, due to the degree of inherent stress, plated gold may in fact be more difficult to utilize for the free-standing structure than nickel. Further investigation is needed to investigate the potential of utilizing gold in the reported transition structure.

After the metal layers are formed, the silicon around the probe structure was etched through via DRIE from the backside so that they could be released from the wafer. At the same time, substrate under the probe was also etched away. Prior to releasing the probe structures from the wafer, the 2000 Å titanium seed layer of the probe metal, now

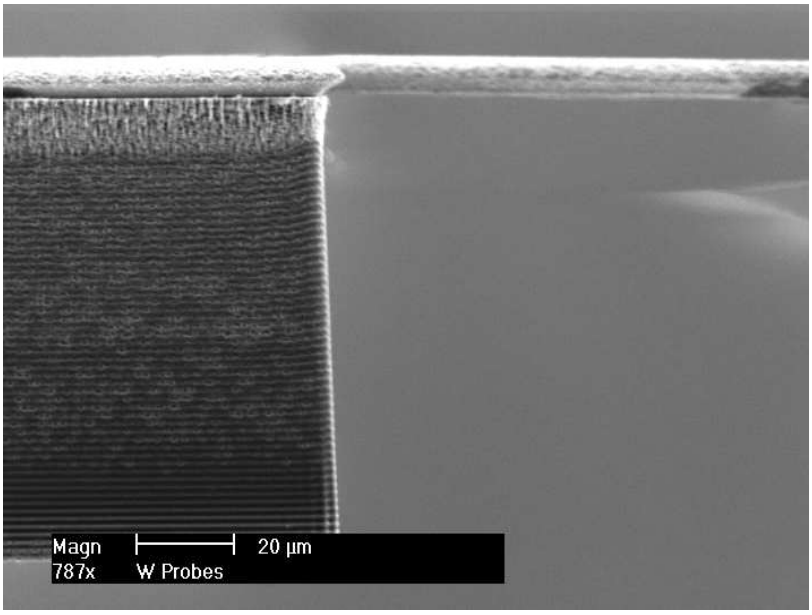


Figure 3.32: Cross sectional view of a free-standing probe. The silicon wafer is 100 μm thick.

exposed after complete removal of the silicon under the probe, is etched in hydrofluoric acid:deionized water (1:10). This was done to relieve the stress coming from the interface between the titanium and the nickel. Finally, the remaining photoresist is stripped in PRS2000 and the probes are cleaned in acetone and isopropyl alcohol (IPA).

A scanning electron micrograph of a fabricated free-standing probe is shown in Fig. 3.31. As can be seen, about 8 μm of electroplated nickel is thick enough to provide mechanical strength to the probe to keep it suspended in air. Also, the warping effect of the probe due to stress is negligible. A cross sectional view of the edge of the probe is given in Fig. 3.32. The deep etching recipe utilized (Recipe 1 in Table 3.3) results in a nearly vertical sidewall, as evidenced by the figure.

Diamond Waveguides

The silicon diamond waveguide are fabricated in a similar manner as in [77]. A (001)-oriented high resistivity ($\rho > 1000\ \Omega \cdot \mathrm{cm}$) silicon wafer with a thickness of 2 mm has been

etched in 25% tetramethyl ammonium hydroxide (TMAH) to form top and bottom halves of a diamond waveguide. 8000 Å of thermal oxide was used as the etch masking layer and the temperature of TMAH was held at 80°C. The etch rate was roughly 25 μm/min. The etch depth is 1270 μm, which is one half of the *W*-band standard waveguide (WR-10) width. At the same time, pits for 596 μm diameter glass microspheres for aligning the two halves of a waveguide are also etched.

The next step is to etch 100 μm deep grooves by deep reactive ion etching (DRIE). Grooves in the bottom waveguide half serve as the cradle for the fabricated probes, and grooves in the top waveguide half serve as the shields over the FGC lines. Before applying photoresist, 5000 Å of titanium is sputtered over the entire wafer. This titanium layer is used as another masking layer, in addition 8 μm of photoresist, when etching the grooves. This is especially important for the immediate edges of the waveguide where the resist becomes too thin to mask deep etching. Insufficient masking of the waveguide edges may result in etching damage along the waveguide edges, which in turn may degrade overall transition performance through signal leakage. 100 μm thick silicon wafer pieces that have roughly the same size as the etching apertures are used to monitor etching and to obtain the desired depth of 100 μm. The waveguide halves are then diced and 500 Å of titanium and 1.6 μm of gold are sputtered to metallize the waveguide walls and the grooves. A scanning electron micrograph of a bottom half of a silicon diamond waveguide with two probes placed in their cradles is shown in Fig. 3.33 and Fig. 3.34.

3.5.4 Experimental Results

The fabricated back-to-back transition module was measured using an HP 8510C vector network analyzer and GGB picoprobes of 120 μm pitch. Calibration was achieved using thru-reflect-line (TRL) protocol with on-wafer FGC thru, short, and delay lines of the same geometry as that used to feed the probe. From TRL calibration, it was calculated that the nickel-plated FGC line has loss of about 4.4 dB/cm at 85 GHz and about 4.8 dB/cm at 105

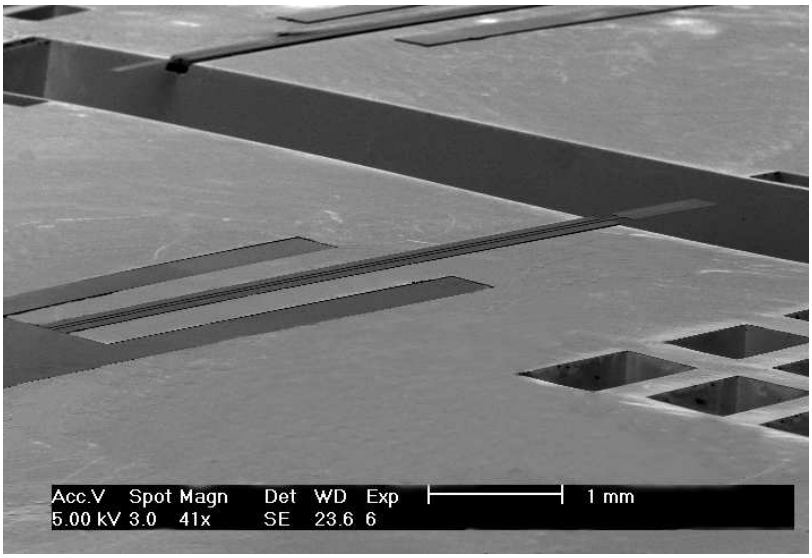


Figure 3.33: Scanning electron micrograph of a bottom half of silicon diamond waveguide with probes placed in the cradle. Pits for aligning the top and bottom waveguide pieces are shown in lower-right corner.

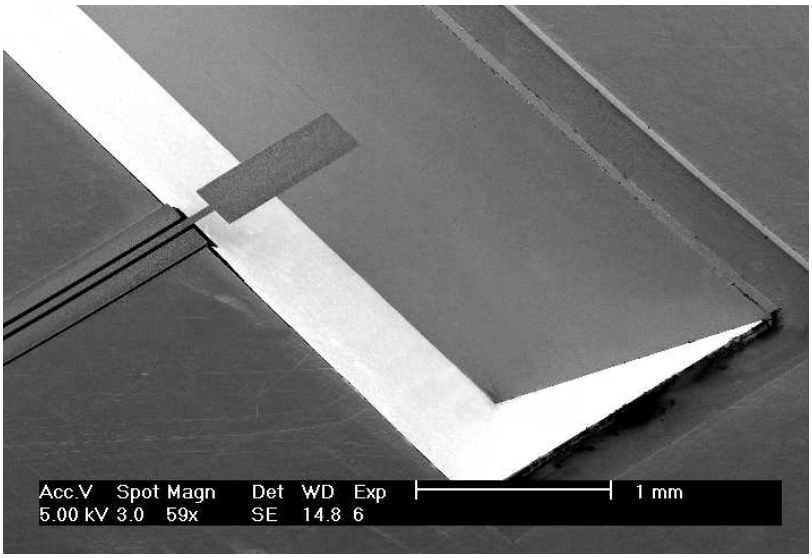


Figure 3.34: A closer look at a free-standing probe placed in its cradle.

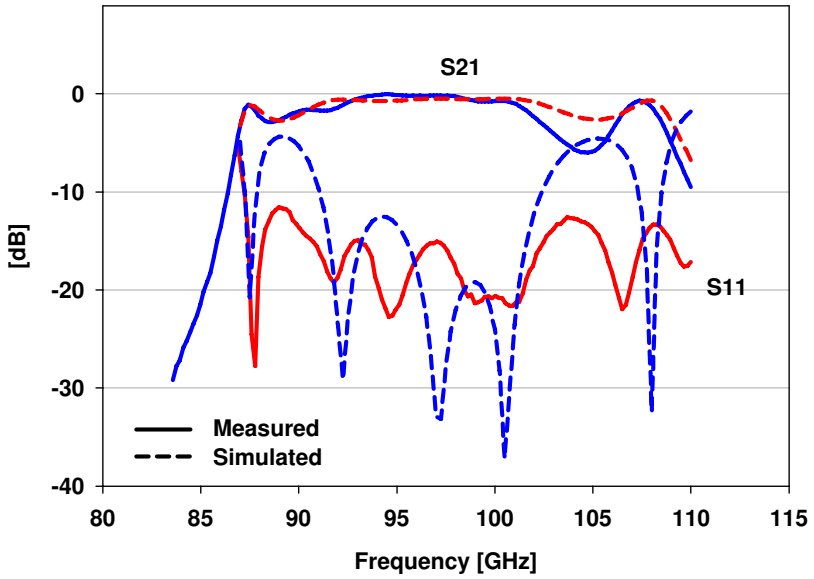


Figure 3.35: Measured and simulated results of back-to-back FGC line to silicon micromachined diamond waveguide transition.

GHz. which is somewhat higher than FGC lines with the same dimensions and patterned with gold (Fig. 3.1(b)).

Fig. 3.35 displays the measured results of a back-to-back transition after the FGC line and waveguide loss have been de-embedded out. For comparison, Ansoft HFSS simulation results for assuming waveguide wall conductivity of 5×10^6 Ω·cm are plotted in dashed lines. The measured results and simulated results are in good agreement, but is somewhat different around 105 GHz, where the measured insertion loss is roughly 3 dB below the simulated insertion loss, while exhibiting an excellent match with a measured return loss of 12 dB. The greatest cause for the difference between the two results rests in the fact that the two waveguide halves are simply clipped together. Imperfect bonding introduces gaps between the two halves. It is believed that in this experiment, the effect of the gap was negligible in the measured band except around 105 GHz.

Measured results show that the waveguide is cutoff below 86 GHz. Above the cutoff frequency, the return loss of the back-to-back transition is better than 10 dB throughout the

entire *W*-band, up to 110 GHz. The insertion loss is less than 0.5 dB per transition from $\sim$92 GHz to $\sim$101 GHz, and less than 0.25 dB per transition from $\sim$93 GHz to $\sim$98.5 GHz. When compared with the results of [77] where there was a 100 μm thick probe-supporting substrate, the experimental results suggest that complete removal of the dielectric may indeed improve the performance of such an FGC line to waveguide transition. As expected, the transition performance, in terms of bandwidth, is limited by the narrow dominant mode bandwidth of the diamond waveguide. However, the measured insertion loss and return loss are in good agreement with the simulated results within the single-mode bandwidth of the waveguide. It is certainly expected that when the top and the bottom waveguide halves are thermo-compression bonded (the waveguide halves were simply clipped together in this study), the transition performance will be further improved.

In addition to exhibiting improved performance over an earlier micromachined version [77], the novel free-standing probe structure provides a viable means to effect broadband FGC line to waveguide transitions applicable well into the submillimeter-wave and THz range.

3.6 Conclusions

The uniplanar geometrical characteristic of finite ground coplanar (FGC) lines provides ability to easily integrate both active and passive elements. Thus, FGC lines have become one of the most popular transmission lines for current monolithic microwave integrated circuits (MMIC's). However, owing to its superior loss performance as well as power handling capacity, there is still need for hollow rectangular waveguides. Thus, effective transitions between FGC lines and waveguides are required in many applications.

Such transitions have been demonstrated with conventionally machined waveguides in *X*-band (8.2-12.4 GHz) and *Ka*-band(26.5-40 GHz). Although the transition showed excellent performance across the entire waveguide band, the feasibility of such transitions is

limited due to the difficulty and high cost of conventionally machining rectangular waveguides at very high frequencies.

This has led to developing micromachined waveguides. Micromachining has the ability to cost-effectively manufacture to better, if not the same, tolerances. Among various micromachining techniques, deep reactive ion etching (DRIE) is a promising technique since it is a relatively simple and has a potential to fabricate micromachined waveguides that have the same cross sections as conventional waveguides.

The fully micromachined transition employing micromachined waveguides developed via DRIE showed not only the bandwidth but also the insertion loss performance that is comparable to the transition employing conventionally machined waveguides. One concern with developing waveguides via DRIE is the reproducibility of the process. It has been to the author's experience that the DRIE etch rate varies by as much as 10% depending on various conditions. One important factor is wafer mounting process. The STS DRIE system is capable of only handling full 4 in. wafers. Thus, quarter-piece wafers are bonded to a 4 in. carrier wafer using photoresist. This inevitably introduces air gaps between the two. Together with the wafer-bonding photoresist that has a low thermal conductivity, the air gaps impede efficient cooling during deep etching. Since the formation of air gaps is not always the same, wafer cooling is not the same and thus results in different etch rates. This can be circumvented by processing full 4 in. wafers. Since the process wafer can be directly cooled with helium from the backside, the results are expected to be far more consistent.

Finally, the free-standing probe presented in this chapter, with a reduced single-mode bandwidth of the diamond waveguide, not only maximizes the transition performance, but also proves the ability of such transitions to be applicable well into submillimeter-wave and THz range.

CHAPTER 4

Micromachined Power Combining Module

4.1 Introduction

SOLID-STATE sources have advantages over vacuum tube-type sources because of their small size, low cost, and compatibility with monolithic microwave integrated circuits (MMIC) [2]. However, as the operating frequency increases, their power-handling capacity is reduced due to the reduction in the size of the solid-state devices. As a result, vacuum-based sources have been widely used as microwave power sources at frequencies above 100 GHz. Unfortunately, these vacuum-based sources are large in size and weight, require high voltage supplies for operation, and have low reliability and a short life time.

A considerable amount of effort has been carried out to improve the power and frequency performances of solid-state oscillators and frequency multipliers that can be used as millimeter-wave sources [4, 14]. Although these are excellent results, they still suffer from low power levels and thus are not suitable for medium to high power applications, such as radar systems. One possible solution to overcome the limitations of solid-state sources is to combine the output power of numerous solid-state oscillators, amplifiers, or multipliers [10, 11].

The proposed waveguide-based power combining system is shown in Fig. 4.1. An example of a 3×3 array of power combining modules is shown in this figure. In each module

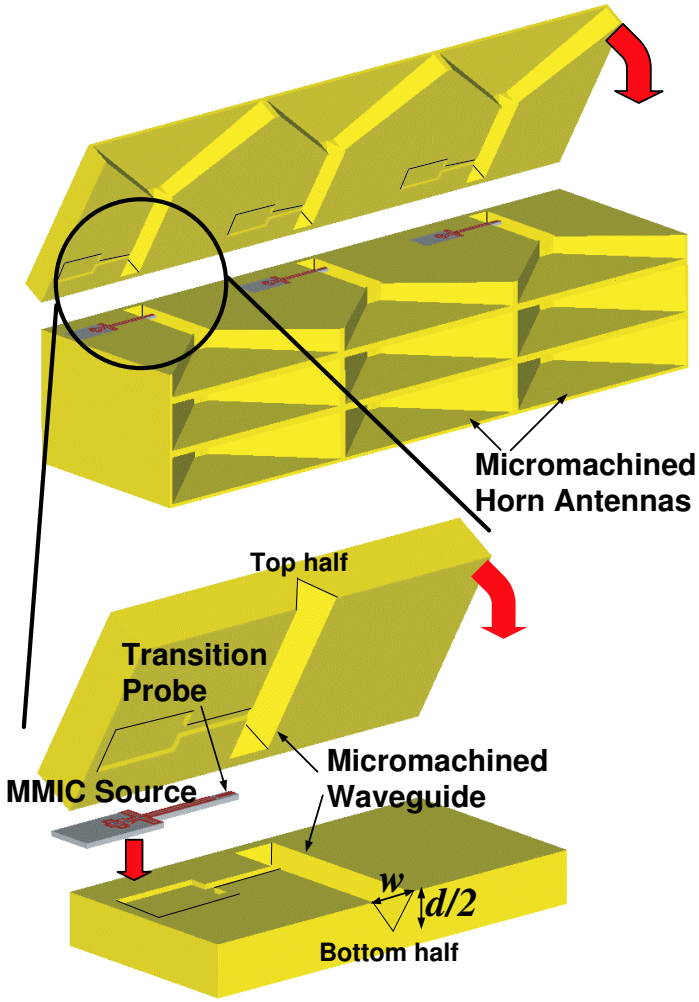


Figure 4.1: Proposed waveguide-based fully micromachined power combining system composed of modules. Each module consists of a finite ground coplanar (FGC) line-based MMIC source, a transition probe, and a silicon micromachined waveguide section. The waveguide can then be used to feed a highly directive micromachined horn antenna. A number of these modules can be combined together to produce higher output power.

that constitutes the power combining system, the output of an MMIC source is coupled to the micromachined waveguide via a rectangular transition probe. The waveguide then can be used to feed a highly directive micromachined horn antenna. A number of these modules can be combined together to constitute a fully micromachined power combining system for high-power millimeter-wave applications.

This chapter presents a fully micromachined power combining module that operates at an output frequency of 72 GHz. The module has the unique characteristic that it integrates, for the first time, micromachined components fabricated out of GaAs and silicon. GaAs monolithic circuits provide optimum high frequency performance while silicon micromachined components allow low cost fabrication. State-of-the-art high efficiency GaAs monolithic frequency doublers and all silicon-based finite ground coplanar (FGC) line to silicon micromachined waveguide transitions have been successfully demonstrated in Chapter 2 and Chapter 3, respectively. A successful integration of the two heterogeneous components through a unique micromachined arrangement is demonstrated in this chapter.

4.2 GaAs Micromachining

GaAs is notoriously fragile, thus is not well suited to be micromachined, to be chemically sculpted on a very fine scale [25, 57]. On the other hand, the high electron mobility and high saturated drift velocity characteristics make GaAs material of choice for high speed or high frequency circuits. Another strong advantage of GaAs over other materials is the availability of semi-insulating substrates [80]. High resistivity substrates are required to construct monolithic circuits since it greatly reduces parasitic capacitances. However, a well-established process technology is available and thus lost-cost fabrication of micromachined structures is viable with silicon that provides superior mechanical properties.

In order to integrate GaAs monolithic high frequency circuits with silicon micromachined structures, for example in the power combining module presented later in this chap-

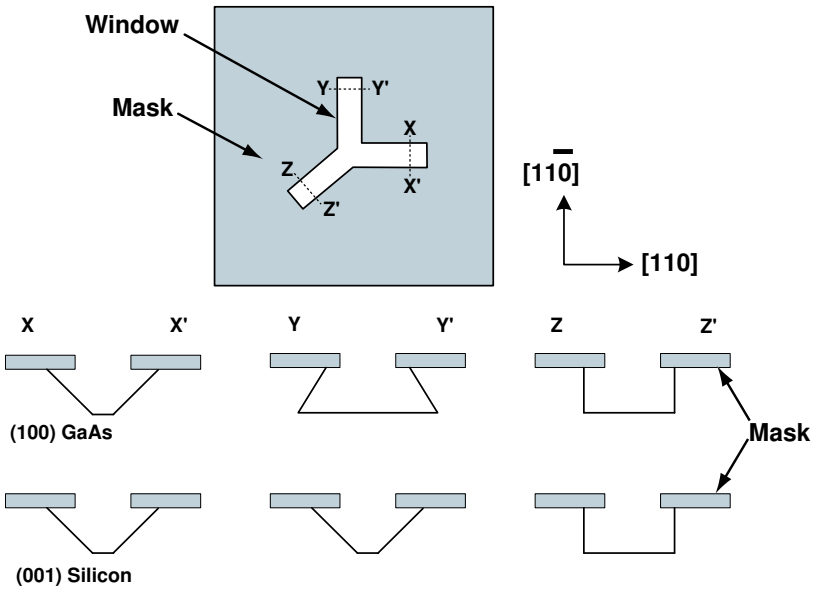


Figure 4.2: Typical wet chemical etching profiles of GaAs and silicon with most common slice orientations.

ter, process technology other than standard GaAs IC fabrication technology is also required. In this section, several GaAs micromachining techniques are discussed.

4.2.1 Wet Chemical Etching

GaAs and silicon wet chemical etching are anisotropic due to the nature of etching behavior that is dependent on crystal orientations. Etchants will attack different crystal planes at different etch rates, thus resulting in anisotropic etch profiles. However, the difference in the crystal structures of GaAs (zinc blende) and silicon (diamond) leads to other wet etching characteristics that differ from each other, as shown in Fig. 4.2. This is because the (111) crystal planes in GaAs are either of all gallium (Ga) atom planes (111*A* planes) or all arsenide (As) atom planes (111*B* planes) that have very different chemical properties thus different etch rates, whereas all crystal planes in silicon are of only silicon atoms.

There are various purposes for wet etching GaAs : to remove damaged material, to form mesa structures for device isolation, to recess gates prior to metallization in FET's, to

aid in polishing, as part of of cleaning procedures, etc. Most etchants for GaAs contain an oxidizing agent, a dissolving agent, and a dilutant, such as water [81]. The etchants first oxidize the surface and then dissolve the oxide, thereby removing gallium and arsenide atoms. The popular GaAs etchant $H_2SO_4/H_2O_2/H_2O$, for example, has hydrogen peroxide that oxidizes the surface, and sulfuric acid that dissolves the resulting oxide. However, GaAs will not etch in either H_2O_2 or H_2SO_4 alone. For example, the etch rate was reduced to roughly 0.5 μm/min from roughly 10 μm/min by diluting $H_2SO_4/H_2O_2/H_2O$ from 1:1:10 to 1:1:40. The etch rate depends strongly on proportions of each chemicals, especially the dilutant. Other conditions such as etchant temperature and agitation, as well as etchant type also have effects on various etch characteristics, $\{100\}/\{111\}$ selectivity for example. Most GaAs wet etchants have poor $\{100\}/\{111\}$ selectivity, and generally the amount of undercutting for GaAs wet etching is about the same as the etch depth. The undercutting of masking patterns for silicon wet etchants is small or negligible, and thus is better suited than GaAs for micromachining structures that require tighter dimensional tolerances. Typical $\{001\}/\{111\}$ selectivity for silicon wet etching is 10/1 in TMAH, 400/1 in KOH, and 40/1 in EDP.

Other popular GaAs etchants include $C_6H_8O_7$ (Citric acid)$/H_2O_2/H_2O$, $H_3PO_4/H_2O_2/H_2O$, $HCl/H_2O_2/H_2O$, and $NH_4OH/H_2O_2/H_2O$ systems. For frequency multipliers in Chapter 2 and in this chapter, $H_3PO_4/H_2O_2/H_2O$ is used to etch through the n^- layer for ohmic metal deposition. The etch system gives an etch rate that is reasonably low and controllable. The etch rate is approximately 100 Åsec. for the mixture ratio of 1:1:8. To form mesas for device isolation, $NH_4OH/H_2O_2/H_2O$ (1:24:0) is used . The etch rate is relatively high, roughly 3.5 μm/min., but this etchant system has a very high AlGaAs/GaAs selectivity and thus a thin layer of AlGaAs can be used as an etch-stop layer.

Shown in Fig. 4.3 is a scanning electron micrograph of a wet etched GaAs profile. (100)-oriented GaAs is etched in $H_2SO_4/H_2O_2/H_2O$ (1:1:40) at an average etch rate of 0.5 μm/min. The etch depth is 124 μm (measured with DEKTAK Profilometer) with an orig-

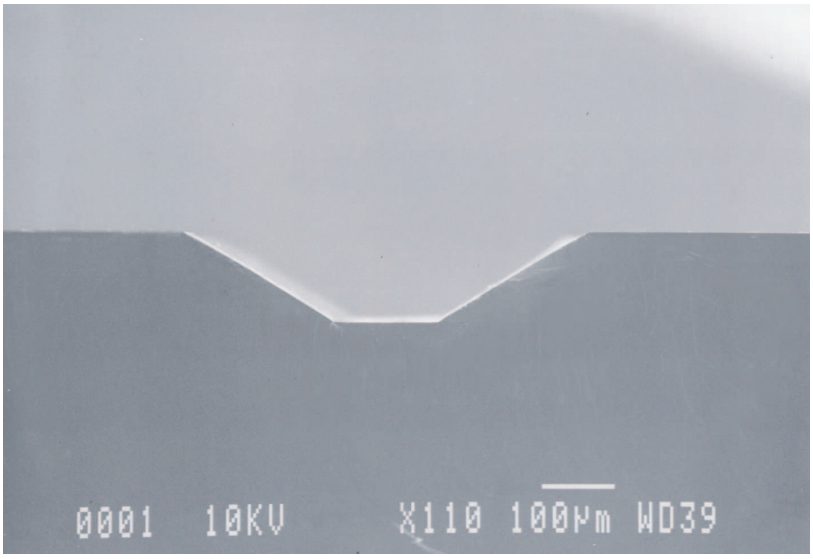


Figure 4.3: Profile of GaAs wet chemically etched in $H_2SO_4/H_2O_2/H_2O$ (1:1:40).

inal opening width of 250 μm. Visual examination of the SEM reveal that the width of opening top is roughly 550 μm whereas the bottom is roughly 145 μm. As mentioned, most GaAs etchants have poor $\{100\}/\{111\}$ selectivity, usually less than 1, resulting in substantial amount of masking-pattern undercutting. In the case for Fig. 4.3, the $\{100\}/\{111\}$ selectivity was approximately 0.83.

4.2.2 Reactive Ion Etching

Dry etching of GaAs, compared with wet chemical etching, provides better dimensional control and its anisotropy can proceed more rapidly in the vertical direction. Therefore, undercutting of masking patterns can be greatly reduced [80]. Dry etching techniques involve plasma etching of any type, in which the plasma generates reactive species that serve to chemically (therefore isotropically) etch material in immediate proximity to the plasma. In most cases, the reactive species (ions) are driven by the voltage applied between the upper and lower electrode to obtain anisotropy. Upon reaching the substrate with a certain kinetic energy, ions sputter the material away from the wafer on the atomic scale. Com-

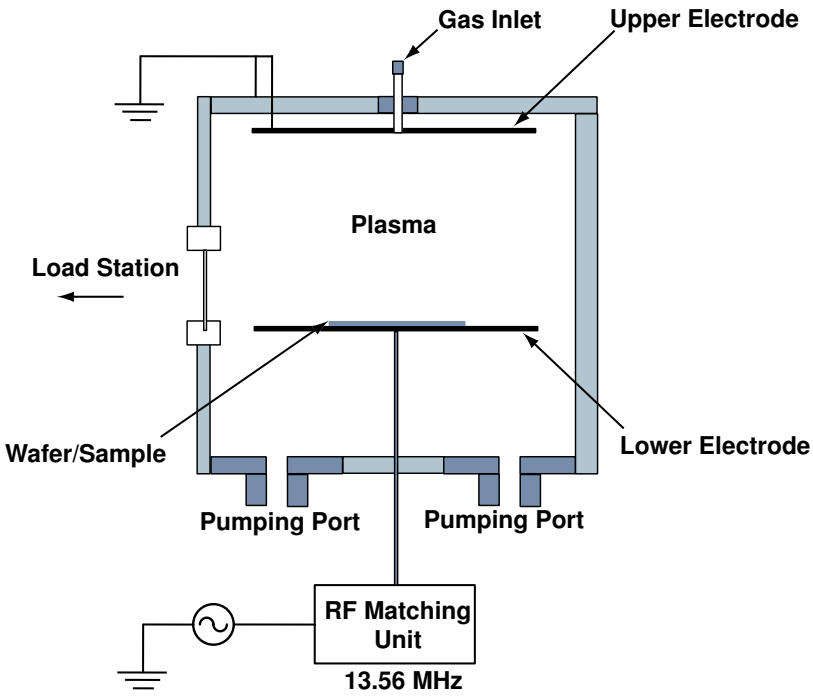


Figure 4.4: Schematic of the reactive ion etching (RIE) system used for GaAs dry etching.

mon problem with plasma etching occurs when the physically sputtered particles are redeposited on the wafer surface. Usually, this "micromasking" mechanism leads to formation of tall, thin columns in the etched trench. Plasma-assisted etching can be highly directional (anisotropic), thus is a suitable technique to form narrow deep holes, for example source via ground connections, in GaAs circuits.

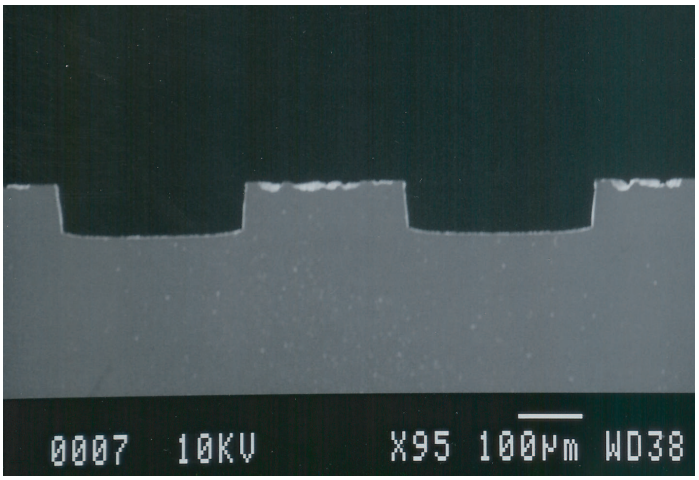
The investigated reactive ion etching (RIE) recipe optimized by Nordheden *et al.* [82] is investigated in this section, with the focus on etch masking issues. The optimized GaAs RIE is utilized in the fabrication of GaAs circuits presented later in this section. The etch is necessary to define each GaAs circuit structure, and the required etch depth is 100 μm. The RIE uses a mixture of $Cl_2/BCl_3/Ar$ plasmas. Chlorine provides the majority of the reactive species while argon is used as a buffer gas. The boron trichloride is added to scavenge oxygen in the chamber and to remove native oxide on the GaAs surface. The gas flow rates in [82] are increased by 50%, from $Cl_2/BCl_3/Ar$ 8/6/20 sccm to 12/9/30 sccm, in an effort

minimize loading effects. Also, the chamber pressure is increased from 15 mT to 27 mT at which the recipe is reported have the highest etch rate, although no major difference in the etch rates is observed. The RF power is controlled by the bias voltage of -300 DCV, which corresponds to roughly 160 W of RF power.

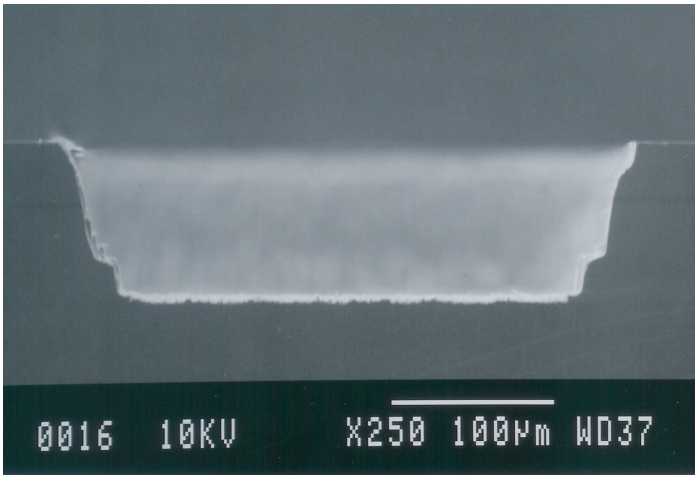
The GaAs dry etching experiments in this chapter are performed in a PlasmaTherm SLR 720 parallel-plate RIE system, the schematic of which is shown in Fig. 4.4. The 4 in. anodized aluminum platen electrode is operated at 13.56 MHz with the upper electrode and chamber walls grounded. The chamber is pumped down to the base pressure of 2×10^{-5} Torr prior to etching. Gas flow rates are controlled with mass flow controllers and the powered electrode is cooled by a circulating chilled water to a temperature of 20°C during the process.

GaAs samples with an approximate size of 1 in.$\times$1 in. are patterned with approximately 30 μm thick, triple coated AZ9260 photoresist. The first two layers are spun at 2000 rpm and the third layer is spun at 4000 rpm. After each spin, photoresist is soft baked for 30 min. in a 90°C oven followed by a 20 min. rest on a flat surface. The patterns are exposed for 315 sec. at UV intensity of 20 mW/cm^2 and developed in AZ400K:H_2O (1:3). The patterned samples are then mounted on 4 inch silicon carrier wafers with 500/2000 Å of titanium/nickel layers and 20 μm thick photoresist. The evaporated metal layers are used as an additional masking layer to protect silicon from being etched thus changing the etch chemistry during RIE. On top of the metal layers of the carrier wafer, AZ9260 is spun twice at 2000 rpm with 30 min. soft bake at 90°C after each spin. The patterned GaAs sample is mounted in the center and baked for 3 min. on a 105°C hotplate, to improve bonding of the GaAs sample and silicon carrier wafer.

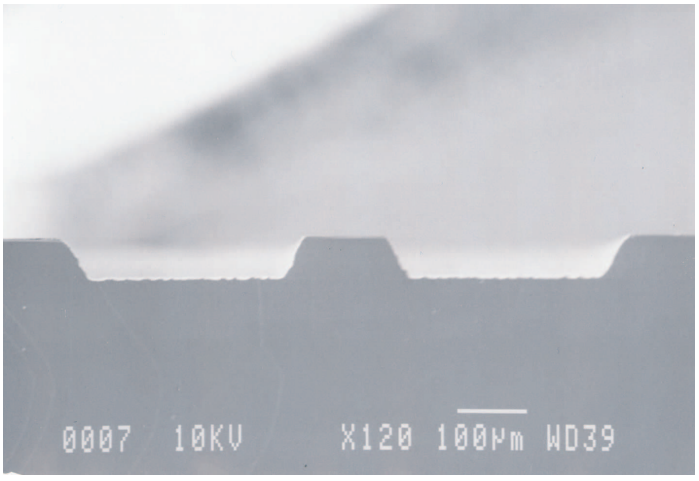
Shown in Fig. 4.5(a) is the etch profile after 200 min. of RIE. The average etch rate is 0.46 μm/min. with a selectivity of 6:1 As can be seen, an excellent vertical profile is obtained. However, as is shown by this figure, signs of surface damage are seen across the entire GaAs wafer. In plasma etches, the ion bombardments not only results in physical



(a) Photoresist not hard baked.



(b) Photoresist not hard baked. Etch performed in 20 min. increments



(c) Photoresist hard baked for 2 hours at 110°C.

Figure 4.5: GaAs profiles after reactive ion etching (RIE).

Figure 4.6: Temperature dots for measurement of the peak temperature during RIE. The circle turns dark when the temperature exceed a certain value, for example 132°C (right).

sputtering of the material, but also increases the temperature of the wafer. Although the wafer chuck is continuously cooled with circulating chilled water throughout the process, effective heat transfer is impeded due to the thick (over 20 μm) photoresist layer on the carrier wafer that is used to protect the carrier wafer and to bond the GaAs sample. It can be also attributed to the low pressure operating condition (therefore low heat convection) and the low thermal conductivity of GaAs (0.46 W/cm·°C at 300 K). The peak temperature of photoresist during 100 min. of RIE, measured with the temperature dots in Fig. 4.6, did not exceed 132°C (132°C is the lowest temperature that is detectable with the temperature dots used for this experiment). However, the continuing ion bombardments on heated photoresist leads to photoresist corrugation, creating valleys where eventually the wafer surface is revealed and damaged (etched). This is illustrated in Fig. 4.7. Microscope images of initial test RIE patterns before and after removal of the convoluted (corrugated) photoresist are shown Fig. 4.8. As can be seen in Fig. 4.8(c), the entire wafer surface is damaged by corrugated photoresist.

Shown in Fig. 4.5(b) is the etch profile of GaAs RIE, in increments of 20 min. The etch recipe is the same as that of Fig. 4.5(a), except the bias is reduced (less negative) to -225 DCV, which corresponds to RF power of roughly 110 W, and the etch is divided into nine 20 min. etches for the total etch time of 180 min., with approximately 10 min. of cooling time between each etch. The modification in the etch recipe is to alleviate photoresist

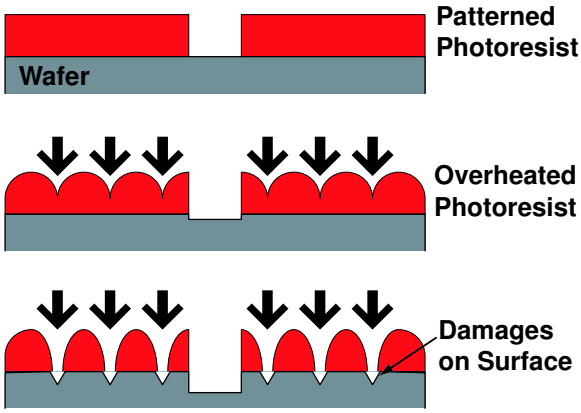
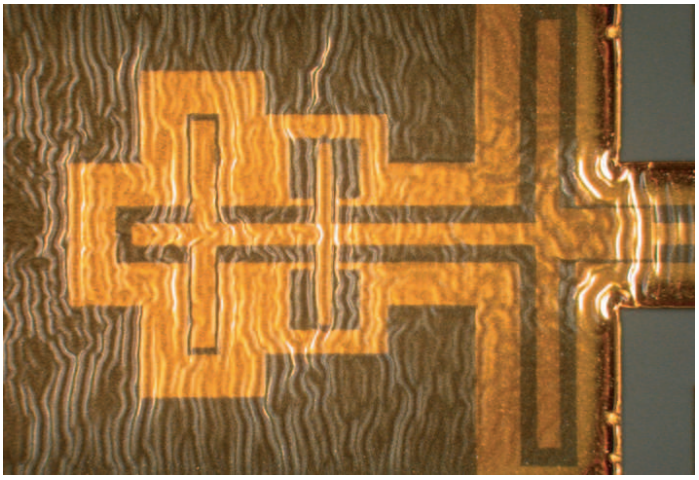


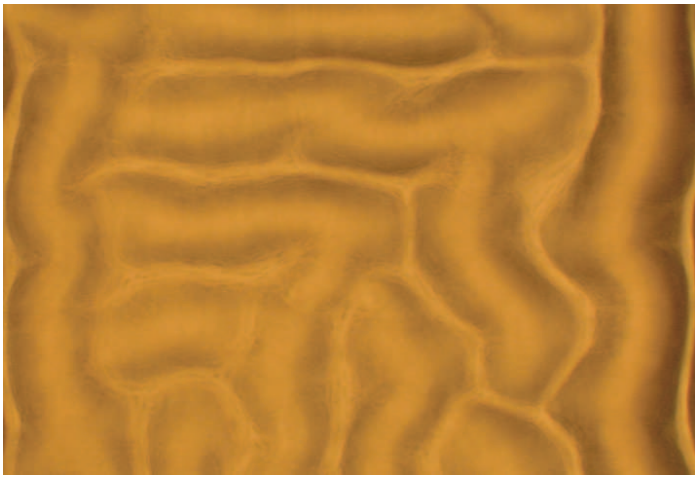
Figure 4.7: Illustration of surface damage due to convoluted photoresist.

heating problems. The decrease in the bias voltage and therefore the RF power reduces the kinetic energy of ions. Therefore average etch rate is reduced by roughly 10% while the selectivity is roughly the same. Also, as can be seen from the sidewall slopes in the two figures (Fig. 4.5 (a) and (b)), the anisotropy is degraded due to reduced ion bombardment. Moreover, there is a discontinuity in the slope which is believed to be due to native oxide formed during every 10 min. of idle time between each etch. Such a discontinuity in the etched profiles is also seen for deep reactive ion etching (DRIE) of silicon when a long etch is divided into a number of short etches. Although the etch recipe is modified to alleviate excessive heating of photoresist problems, the wafer surface damage due to overheated photoresist is still seen.

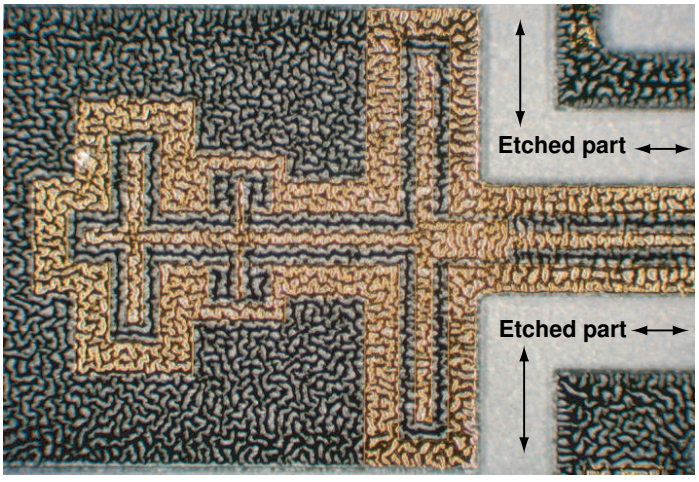
Since the temperature of photoresist does not exceed 132°C during RIE, the problem of overheating can be circumvented by hard baking the photoresist. The heating due to ion bombardment will have minimal effect if the photoresist is hard baked at about the same temperature prior to etching. While hard-baked photoresist provides improved physical/chemical resistances and thus is preferred for masking processes such as RIE, it also leads to an uneven slanted etch profile resulting in loosing of original dimensions. As seen in Fig. 3.13, reflow of photoresist occurs during hard bake, and resist profile at the patterned edge no longer is close to being vertical. This non-vertical photoresist profile is then



(a) Convoluted photoresist.



(b) Closer look at the convoluted photoresist.



(c) Surface damage on the wafer due to heating of photoresist.

Figure 4.8: Convoluted photoresist and the resulting pattern due to ion bombardment and heating during RIE.

transferred to the wafer during RIE, resulting in a similar etch profile and loosing its original dimensions. As mentioned, RIE is required in power combining module fabrication to define each GaAs circuit structure that will later be released from the wafer and placed in a cradle with the same dimensions. Thus, dimension control during GaAs RIE is of critical importance in this work.

Shown in Fig. 4.5(c) is the etch profile after RIE when the patterning resist is hard baked for 2 hours in a 110°C oven prior to etching. Rather than mounting the process wafer on a carrier wafer with already soft-baked photoresist, the GaAs wafer is mounted prior to the 30 min. soft-bake (90°C) of the second photoresist layer on the carrier wafer. This is done to minimize any air gaps between the carrier wafer and the process wafer, and therefore provide efficient cooling of the wafer during RIE. The etch recipe is same as that for Fig. 4.5(a). However, the average etch rate is reduced down to 0.3 μm/min and the selectivity to less than 5:1. The reasons for lowered etch rate and selectivity, as well as degraded surface roughness will be discussed in Section 4.4.3. As is seen in Fig. 4.5(c), the sidewall profiles are less vertical when compared to Fig. 4.5(a) since the non-vertical profile of hard baked photoresist is transferred to the etched trenches. Visual examination of the SEM reveals the top width of the trench is 340 μm and the bottom width is 280 μm, while the width of the opening on the mask is 250μm. However, the surface damage is no longer seen due to increased physical resistance of hard-baked photoresist.

4.2.3 Wafer Lapping

Virtually all GaAs wafers require substrate thinning for thermal and/or electrical reasons [80]. Significant amount of heat is generated within a very small surface area of GaAs devices such as FET's and diodes. The thermal conductivity of GaAs, 0.46 W/cm·°C at 300 K [26], is about 1/3 of silicon and thus GaAs is often considered as a poor thermal conductor. Hence, after front-side processing, GaAs substrate is usually thinned down to 100$\sim$150 μm to achieve low thermal impedance and efficiently transfer the heat to a heat

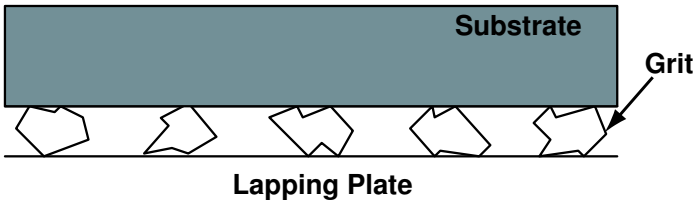


Figure 4.9: Lapping GaAs substrate with grit.

sink attached to the backside. The electrical motivation for thinning GaAs substrates is related to the transmission lines printed on the substrate rather than do GaAs devices. For example, the impedance of a microstrip line is a function of the substrate thickness, and thicker substrate requires wider conductor line which in turn increases the overall circuit size. Also, for high frequency operations, thinner substrates are required to suppress any unwanted propagation modes. Therefore, substrate thinning is required.

Lapping has been the most popular mechanism for wafer thinning. Lapping is not only used to thin III-V substrates for the reasons mentioned above, but also to remove unwanted materials, for example, after molecular beam epitaxy (MBE) growth. Wet etching lacks uniformity while lapping is a relatively simple, yet an effective method to thin wafers with excellent uniformity and reasonable accuracy. A slurry of water and grit (abrasive) is applied between the wafer and the flat lapping plate. As the wafer is moved (rotated) with respect to the lapping plate, the grit mechanically removes GaAs material. This is illustrated in Fig. 4.9 [80]. The grit is usually a very hard compound such as silicon carbide (SiC) or alumina (Al_2O_3) of various sizes. Finer grit gives slower lapping rate and smoother lapped surface. Shown in Fig. 4.10 is a picture of a Logitech PM2 Precision Polishing machine of Solid-State Electronics Lab, University of Michigan, Ann Arbor, in operation. The substrate is mounted on a 3 in. glass carrier chuck using wax, which is then mounted to the sample holder (Logitech PP5 Precision Polishing Jig) using vacuum. The glass lapping plate rotates at a preset speed, and the jig rotates randomly for uniform lapping. The depth of lapping is monitored with the indicator on the jig. Lapping speed is decided by the grit

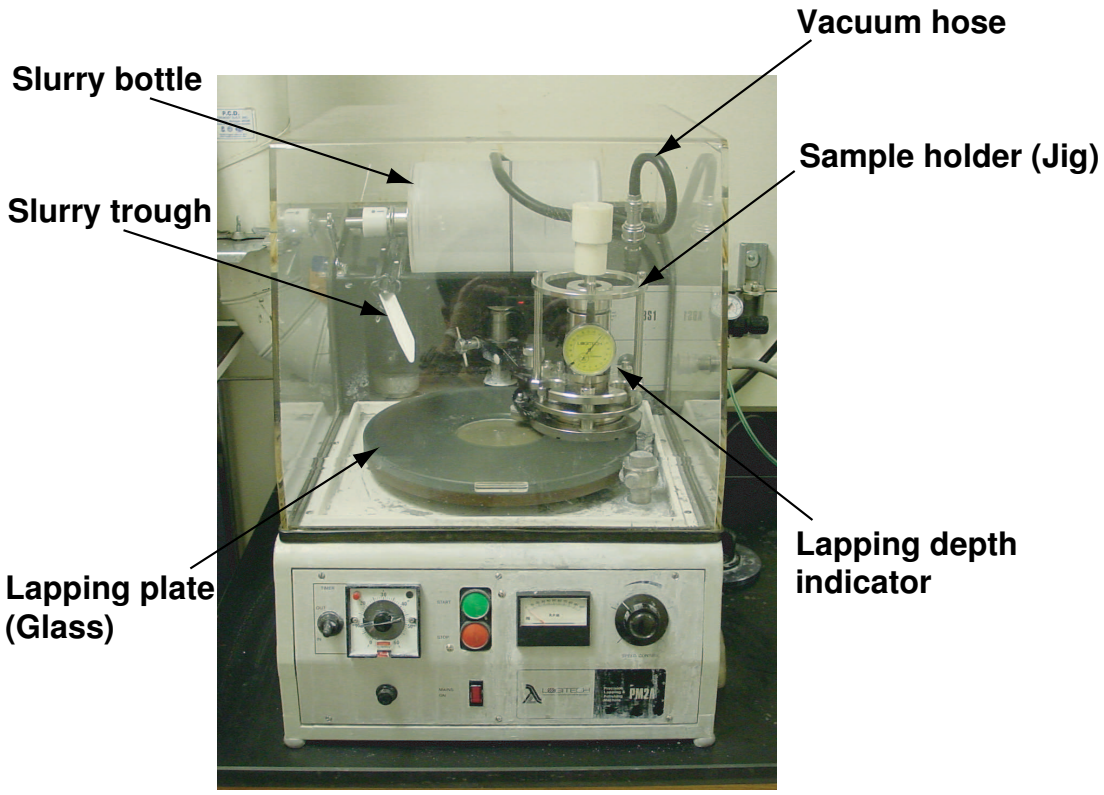


Figure 4.10: Logitech PM2 Precision Polishing machine in operation.

size, glass plate rotational speed, and amount of pressure applied to the sample.

The most important step when lapping GaAs is mounting the substrate upside down on a glass carrier chuck. For bonding the two, wax is usually used for its strong bonding ability. Prior to mounting, photoresist can be spun on the front side of GaAs to avoid direct contact of wax and protect the circuit, for example air bridges. Photoresist can also be used to bond the substrate to the chuck. An nevenly mounted substrate results in unevenly lapped substrate, and moreover, the notoriously fragile GaAs substrate is likely to break/crack or even pulverize during the lapping or unmounting process. In this study, weights are used to achieve maximum flatness when mounting the GaAs wafer (Fig. 4.11). With heated (melted) wax on the glass chuck, the GaAs wafer is placed upside down. A total of 3 weights ($\sim$1 kg) are put on so that the GaAs wafer is pressed down evenly with appropriate pressure. To avoid direct contact of the steel weights to the GaAs wafer, a glass slide is

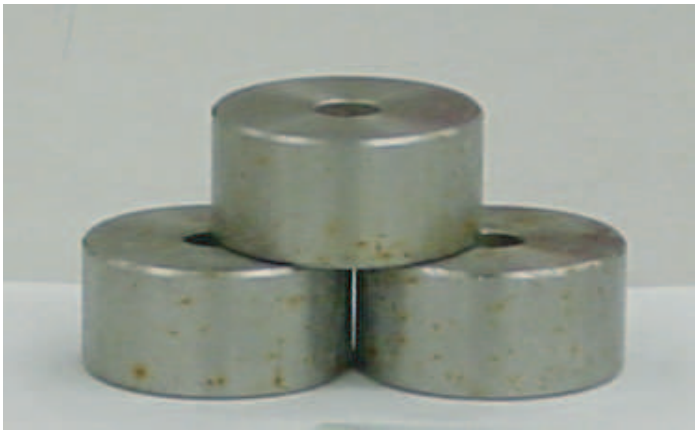


Figure 4.11: Weights (340 g each) are used for maximally even mounting of GaAs substrates on glass chucks.

placed between the two. Prior to mounting, the weights and the glass slide are also heated to the same temperature as the glass chuck. With the weights still on the wafer, the wafer-mounted glass chuck is left for at least one hour at room temperature to cool down.

Lapped substrates are more fragile due to the inevitable crystal damage introduced by lapping and therefore handling thinned ($< 200\mu m$) GaAs wafers needs special care. For subsequent processes, the GaAs substrate can first be mounted on a carrier wafer, then the carrier wafer can be mounted to the glass chuck . In doing so, it is also very important to bond the two wafers with maximum flatness for the same reason mentioned above.

4.3 Module Design

4.3.1 FGC line to waveguide transition

A schematic diagram of an FGC line to waveguide transition can be seen in Fig. 4.1. A rectangular *E*-plane probe is fed by extending the center conductor of a 50 Ω FGC line on a 100 μm GaAs substrate into the waveguide. The waveguide halves are formed by bulk anisotropically etching silicon, resulting in a diamond-shaped waveguide. The bot-

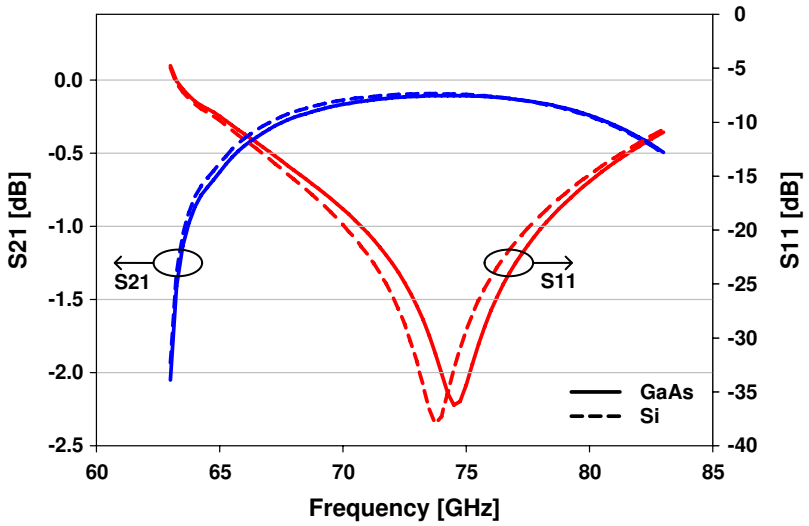


Figure 4.12: Simulated S_{11} and S_{21} of a single FGC line to diamond waveguide transition with a 0.475 cm section of diamond waveguide.

tom half of the waveguide has an additional groove, serving to support the GaAs structure. As mentioned in Chapter 3, such micromachined waveguides are simple to fabricate and can be easily fashioned into micromachined horn antennas. Moreover, provides one of the smoothest sidewalls among various micromachining techniques. This is of critical importance when developing micromachined waveguides since loss in waveguides are in large part due to the surface roughness of the walls. The waveguide dimensions are chosen in order to include the operating frequency range (70-80 GHz) of the frequency doublers in its single mode bandwidth. The width (w in Fig. 4.1) is chosen to be 2.474 mm, which then determines the depth (d in Fig. 4.1) to be 3.5 mm. The first two cutoff frequencies of such a waveguide, calculated with Ansoft HFSS, are 62.3 GHz and 82.6 GHz.

The FGC line to diamond waveguide transition is designed in order for the center frequency of operation to match the frequency at which the frequency doublers have the highest efficiencies. The transition performance depends on the size of the probe, the position of the probe within the waveguide, and the distance between the probe and the waveguide backshort. The transition design is optimized with HFSS. The designed probe size is 796

μm $\times$ 264 μm and is inserted 200 μm into the waveguide. The distance from the backshort to the center of the probe is 2.3 mm. Simulated results of a single transition with a 0.475 cm section of diamond waveguide are shown in Fig. 4.12 where results for silicon and GaAs substrates with same dimensions are shown. GaAs (ε_r=12.9) is assumed to have a zero conductivity (σ) and a tangent loss ($\tan\delta$) of 0.006 whereas silicon (ε_r=11.9) is assumed to have a conductivity of 0.05 $(\Omega \cdot \mathrm{m})^{-1}$ and a tangent loss of 0.004. FGC lines with center/gap/ground dimensions of 70/63/140 μm and shield height of 100 μm are assumed to be lossless. All other metal surfaces (probe, waveguide) are assumed to be gold with a conductivity of 4.1×10^7 $(\Omega \cdot \mathrm{m})^{-1}$.

4.3.2 GaAs Frequency Doublers with Incorporated Probes

The FGC line-based GaAs monolithic frequency multipliers in Chapter 2 were redesigned to incorporate the transition probes designed in Section 4.3.1. The frequency doublers were originally designed using the nonlinear multiple-reflection program described by East *et al*. [37,38] so that the GaAs Schottky barrier diodes have input *Q*'s of two and three. The *Q*=2 diodes have an epitaxial layer doping of $1 \times 10^{17}/\mathrm{cm}^3$, a thickness of 4700 Å and an area of 73.6 $\mu\mathrm{m}^2$ per diode, whereas the *Q*=3 diodes have an epitaxial layer thickness with the same doping and the same thickness, and an area of 65.3 $\mu\mathrm{m}^2$. The FGC line dimensions are optimized so as to minimize the loss in the passive circuitry and therefore maximize the efficiency.

A schematic of the designed *Q*=2 diode frequency doubler with an incorporated transition probe on 100 μm thick GaAs can be seen in Fig. 4.13. The high impedance (71 Ω) FGC lines at the diode inputs are used to resonate the average capacitances of diodes. The input and output matching and isolation networks, each consisting of a pair of open-ended stubs, are designed so that the maximum power of the fundamental frequency is delivered to the didoes and at the same time, the maximum second harmonic output from the diodes is delivered to the output port. For this experiment, the 50 Ω output FGC lines were ex-

tended to 3000 μm and additional space was provided in the input side of the circuit. This is for proper handling and placement of the GaAs structure within the groove. The overall dimensions of the structure is 8.1 mm $\times$ 1.91 mm.

4.4 Fabrication

4.4.1 Diamond Waveguide

For measurement purposes, the structure is fabricated in a back-to-back configuration with a 0.95 cm of diamond waveguide section in between the two probes. The diamond waveguide is fabricated using a (001)-oriented high resistivity (ρ >1000 Ω·cm) silicon wafer with a thickness of 2 mm. At the same time, pits were introduced on both halves to accommodate glass microspheres, thus allowing simple alignment of the top and bottom halves of the waveguide. With 1 μm of thermally grown oxide serving as a masking layer, the silicon wafer is etched in 25% tetramethyl ammonium hydroxide (TMAH) at an average etch rate of 20 μm/hour to form top and bottom halves of the diamond waveguide. The oxide is patterned through standard lithography and by wet chemically etching in buffered hydrofluoric acid (BHF) and the TMAH is held at 80°C throughout the etch. The mask is generated taking into account for the $\{001\}/\{111\}$ selectivity of TMAH, roughly 10/1. To ensure the designed waveguide dimensions, the etch was monitored regularly by comparing

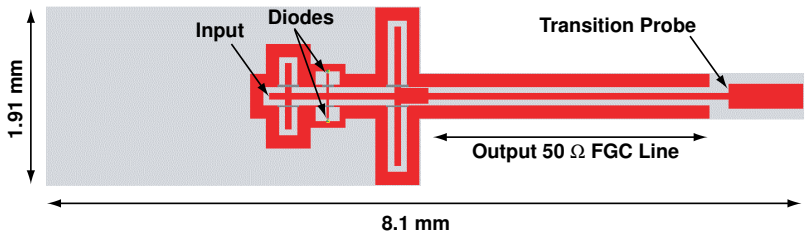


Figure 4.13: Schematic of the designed Q=2 diode frequency multiplier with incorporated transition probe on 100 μm thick GaAs.

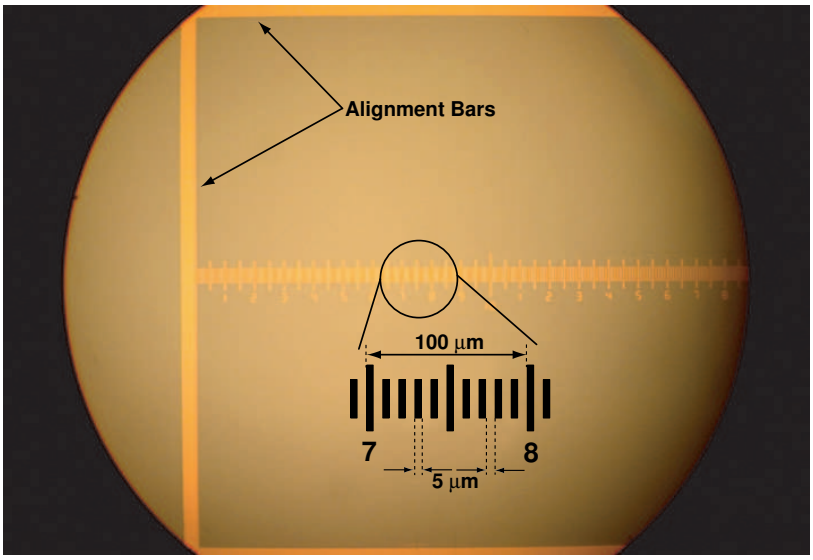


Figure 4.14: Microscope image of ruler patterns on a mask.

the etched feature with the ruler patterns on a mask, shown in Fig. 4.14 . Each bar is 5 μm wide and is separated from each other by 5 μm. A mask aligner is used to accurately align the sample (etch feature) parallel to the alignment bars thus measured lengths/widths accuracy is less than $\pm 5\mu$m.

Then additional grooves were etched 100 μm deep by deep reactive ion etching (DRIE). The groove in the bottom waveguide half serves as a cradle where the GaAs structure is placed, and the grooves top waveguide half serve as the shield over the FGC lines of the GaAs circuit. Finally, the waveguide halves were diced and metallized by sputtering 500 Å of titanium and 2 μm of gold.

4.4.2 Silicon Probes

For complete on-wafer measurements (Fig. 4.15), silicon probe structures at the output was also fabricated. These probe structures were fabricated out of 100 μm thickness high resistivity ($\rho > 2000\ \Omega\cdot$cm) silicon. Etched-through alignment marks, shown in Fig. 4.16(a), are formed by deep etching. Relatively larger features as shown in Fig. 4.16(b)

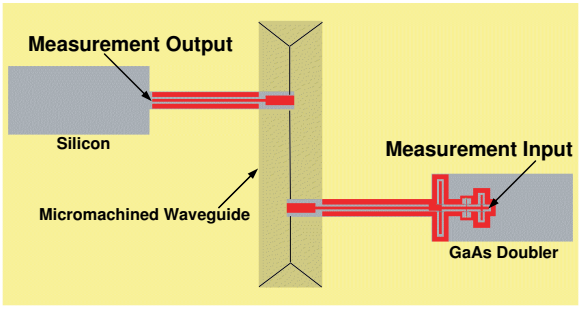
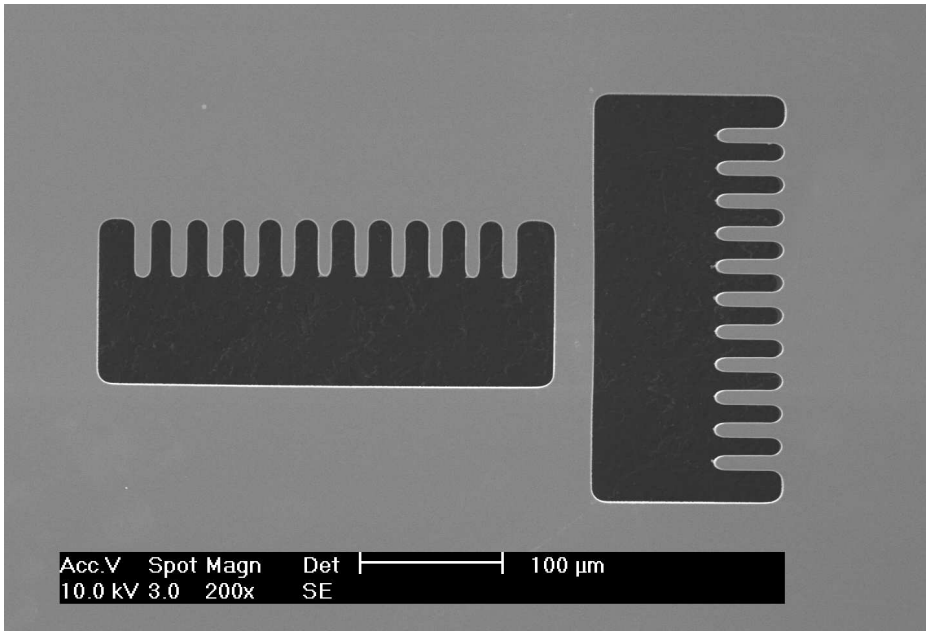


Figure 4.15: Schematic diagram (top view) of the fabricated power combining module. Only the bottom half of the waveguide is shown. A transition probe on silicon was used at the output for measurement purposes.

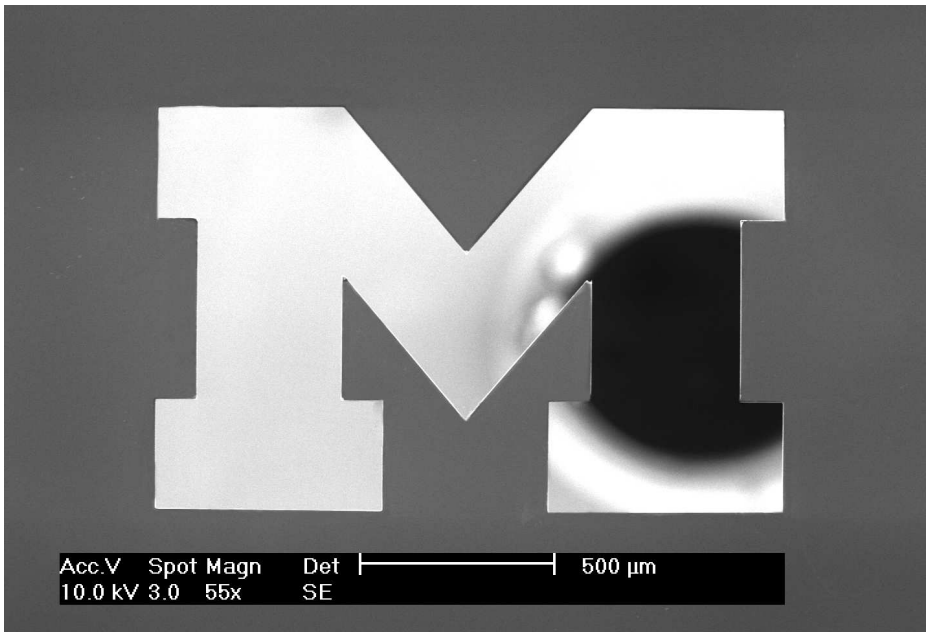
were used to monitor deep etching and avoid excessive etching. Aligned to these etched-through alignment marks, transition probe and FGC line metal layers were patterned with 500 Å of titanium and 1 μm of gold, via standard lift-off process. Then using the DRIE technique, silicon around the probe structure was etched through from the backside. Finally, the remaining photoresist was removed in PRS2000 so that the probes are released from the wafer.

4.4.3 GaAs Frequency Doublers with Incorporated Probes

The GaAs monolithic frequency doublers with incorporated transition probes were fabricated out of (100)-oriented GaAs wafer with a thickness of 625 μm. The epitaxial layer consisted of a 4700 Å thick silicon-doped n^- layer with a doping concentration (N_d) of 1×10^{17} /cm^3 and a 2.5 μm silicon-doped n^+ layer with a doping concentration of 5×10^{18} /cm^3. In between the epitaxial layer and the substrate was a 500 Å thick AlGaAs layer that would be used as an etch-stop layer in the mesa formation process. The passive circuitry was printed with 500 Å of titanium and 1 μm of gold on semi-insulating GaAs after the Schottky diodes were formed and the doped active layer was etched away. Air bridges and fingers were added to equalize the potentials of FGC line ground planes and to connect the anodes to the passive circuitry, respectively. Relatively thick (> 4 μm) metallization was



(a) Deep etched verniers.



(b) Etch monitoring feature.

Figure 4.16: Etched-through alignment marks via DRIE for double side processing. Relatively larger patterns were as in (b) are used to monitor the deep etch.

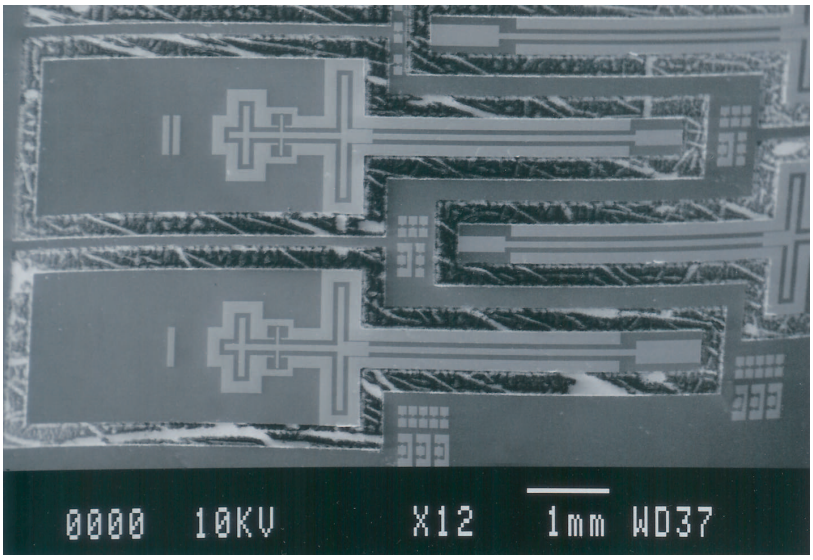


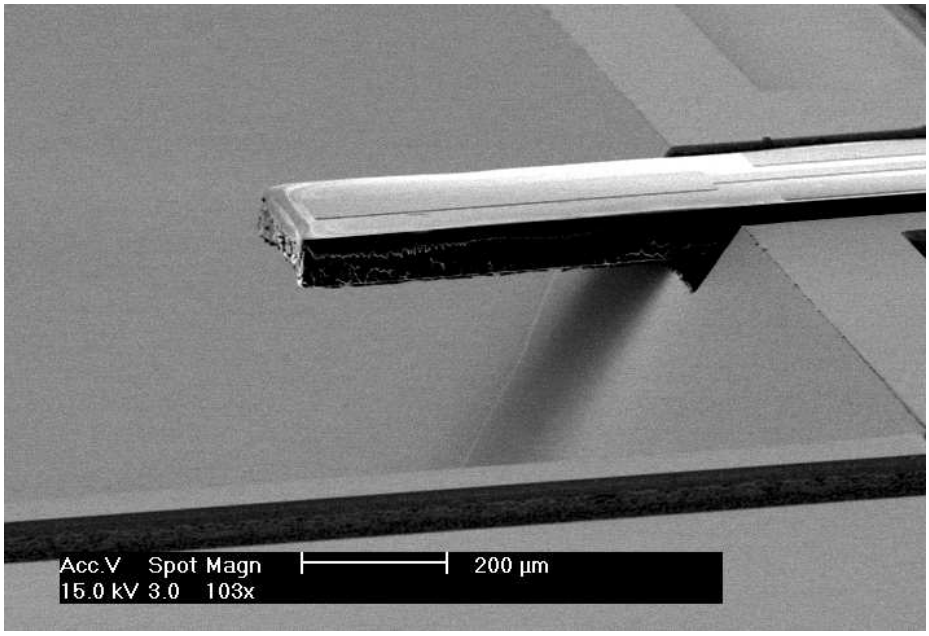
Figure 4.17: A scanning micrograph of an test GaAs wafer with a multiplier test pattern etched using reactive ion etching (RIE).

realized so that these air bridges and fingers can have enough mechanical strength for the subsequent processes.

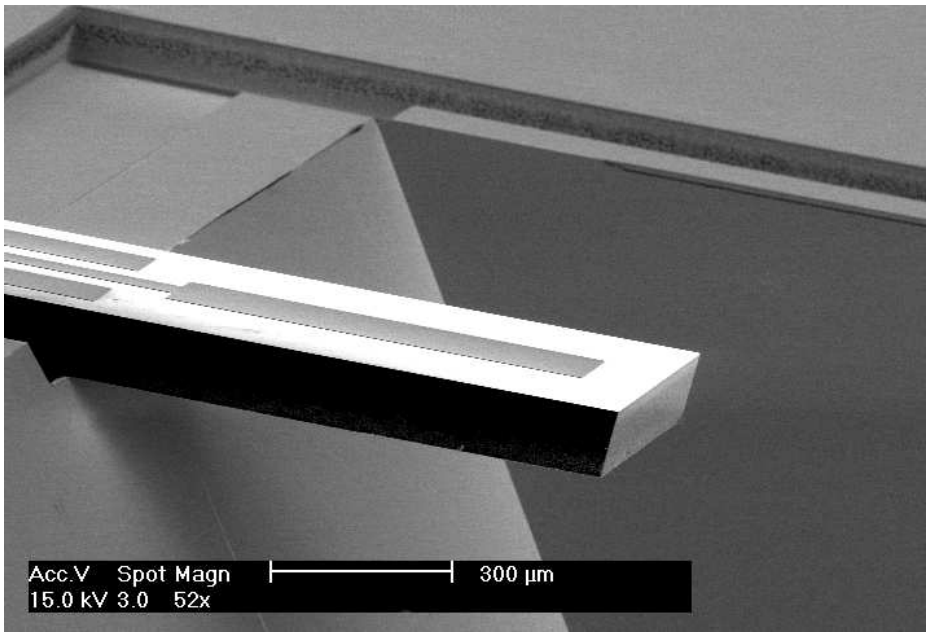
After the Schottky diodes and passive circuitry were formed, GaAs around the structure was etched down 100 μm using conventional reactive ion etching(RIE) to define individual circuits. An example initial test GaAs wafer etched with a multiplier test pattern is shown in Fig. 4.17. Approximately 20 μm of resist is required to mask the etching, and an additional 10 μm is required to protect the air bridges and diode fingers that are approximately 8 μm high. AZ9260 photoresist was spun three times at 2000/2000/4000 rpm with a 30 min. soft bake at 90°C (oven) and 20 min. idle on a flat surface after each spin. The GaAs wafer with patterned photoresist was then mounted on a 4 in. silicon carrier wafer and then baked for another 30 minutes at 90°C (oven) and hard baked for 2 hours at 110°C. The silicon carrier wafer had 20 μm of photoresist, AZ9260 spun twice at 2000 rpm, on top of evaporated 500/2000 Å of titanium/nickel layers. The evaporated nickel is used to mask etching of the silicon, which can affect the etch chemistry. The average etch rate was 0.3 μm/min. and the selectivity was roughly 1:4.5.

A serious impediment to successful plasma etching of GaAs 100 μm deep is the condition of the chamber, especially its cleanness. Plasma etch processes are usually followed by a cleaning etch process typically using a mixture of Ar and O_2 at high pressure. These plasmas, driven at several hundred watts of RF power, are effective for cleaning organic materials and the by-product of fluorine-based silicon plasma etching. By no means, however, are these as effective for cleaning GaAs or other III-V plasma etch by-products. NF_3 plasma is a popular choice for such purposes [83], which was not available for the RIE system at the time of this work. Thus, prior to the RIE run, the chamber was opened to be physically cleaned with 6% H_2O_2 and IPA, followed by a 60 min. cleaning etch process with Ar and O_2 plasmas. However, due to the limited time available in the shared research facility, the chamber was not pumped down to the base pressure of 2×10^{-5} Torr. The etch process was performed at the base pressure level 5$\sim$6 times higher than this level, around 1×10^{-4} Torr). The higher base pressure decreases ion directionality, and thus results in decreased etch rate, anisotropy, selectivity, and increased sidewall roughness. The degraded sidewall roughness can clearly by the difference between Fig. 4.5(a) and Fig. 4.5(c).

After these 100 μm trenches are formed, 10 μm of resist was spun on the wafer to protect the entire circuit on the front side including air bridges and diode fingers. Then the wafer was flipped over and mounted on a 200 μm thick silicon carrier wafer, bonded with photoresist. The bonded wafers are baked for 30 min. in a 90°C oven and for 1.5 hrs. at 110°C, pressed down by three weights in Fig. 4.11 to achieve maximum adhesion and flatness. Using wax, then the carrier wafer is mounted on a 3 in. glass chuck to be loaded to the lapping tool. Again, the sample was pressed down with the same weights to achieve maximally flat mounting. The GaAs substrate was lapped from the backside. When the GaAs wafer was thinned down to the required thickness of 100 μm, the 100 μm deep trenches were revealed so that the individual structures could be released from the wafer. The 200 μm silicon carrier wafer is used to handle thinned wafers when unmounting from the glass chuck and releasing the individual circuits. If there is not a perfect adhesion

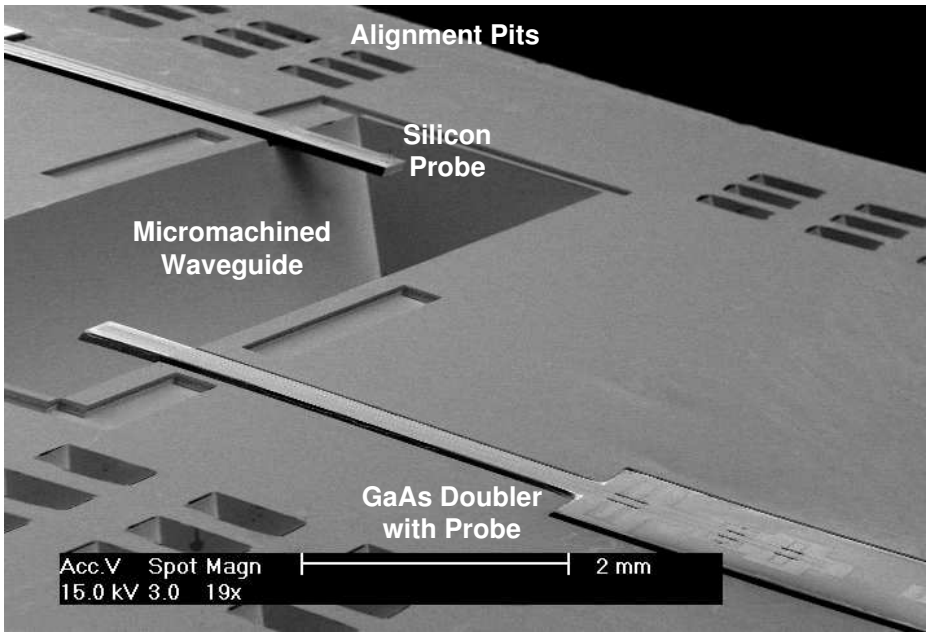


(a) Transition probe on GaAs.

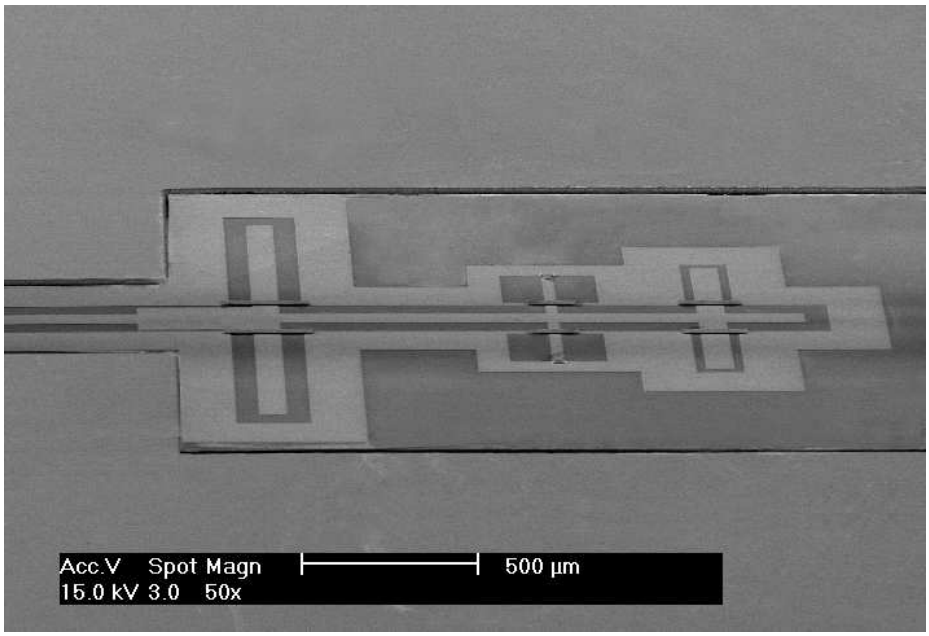


(b) Transition probe on silicon.

Figure 4.18: Scanning electron micrograph of fabricated GaAs probe and silicon probe, placed in cradles on the bottom waveguide half. The difference in sidewall roughness of GaAs conventional RIE and silicon deep RIE is clearly seen.



(a) Bottom half of the module test structure



(b) Q=3 diode multiplier.

Figure 4.19: Scanning electron micrograph of a fabricated power combining module test structure. Only the bottom half of the waveguide is shown in (a).

between the GaAs wafer and the carrier wafer, the GaAs structures are likely to come off during lapping immediately after the trenches are revealed. In order to circumvent this, the final 10 μm is thinned using a wet etchant (NH_4OH:H_2O_2 1:24). Finally, the individual GaAs circuit structures were released and cleaned in PRS1000 and IPA. and Fig. 4.18(a).

Show in Fig. 4.18 are SEM images of the GaAs and silicon transition probes, placed in their cradles. The sidewall roughness of GaAs RIE, degraded due to higher base pressure, can be clearly seen in Fig. 4.18(a). As is evidenced, silicon DRIE provides much smoother sidewalls as seen in Fig. 4.18(b).

A scanning electron micrograph of the bottom half of a fabricated power combining module is shown in Fig. 4.19(a). Shown in the lower right corner is a GaAs monolithic frequency doubler with an incorporated transition probe. Shown in the top left corner is a transition probe on silicon used for complete on-wafer measurements. Fig. 4.19(b) displays the frequency multiplier part of a GaAs structure. The thickness of the GaAs substrate is 100 μm and the GaAs structure is sitting in a 100 μm deep cradle on the bottom of the waveguide. The measured DC characteristics of fabricated Q=2 and Q=3 diodes are summarized in Table 4.1. The 0.9 Ω/contact resistance between the measurement probe and the gold pad is de-embedded from the series resistances (R_s). Comparison with the DC parameters reveals that the fabricated Schottky barrier diodes are almost identical to those in Chapter 2. The n^- layer doping level, calculated from the C/V characteristics of a test diode with an anode area 0.389 mm^2, was 1.1×10^{17} /cm^3.

Table 4.1: Measured DC characteristics of the Q=2 and Q=3 Schottky barrier diodes.

	R_s [Ω]	C_{jo} [fF]	C_p [fF]	I_o [fA]	V_{BR} [V]	η	f_c [GHz]
Q=2	3.3	62	16.3	206	12.6	1.14	778
Q=3	3.3	49	15.8	579	12.6	1.07	984

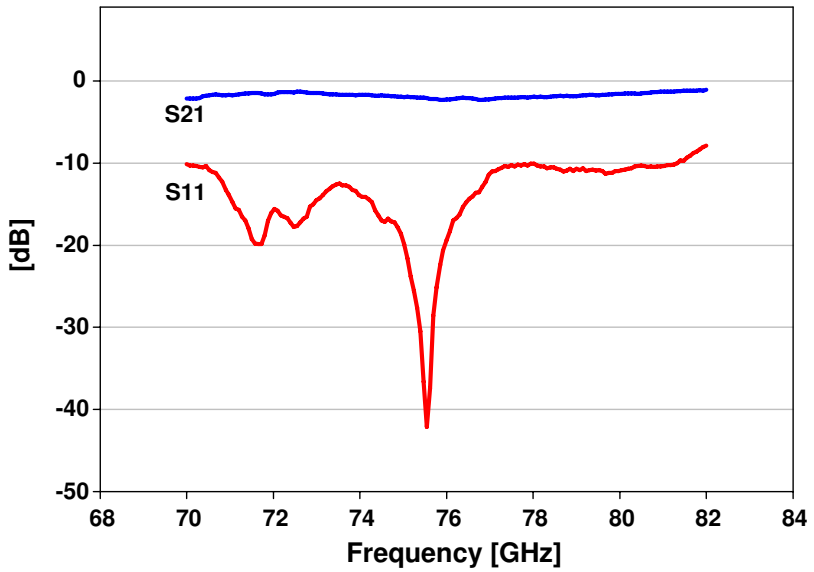
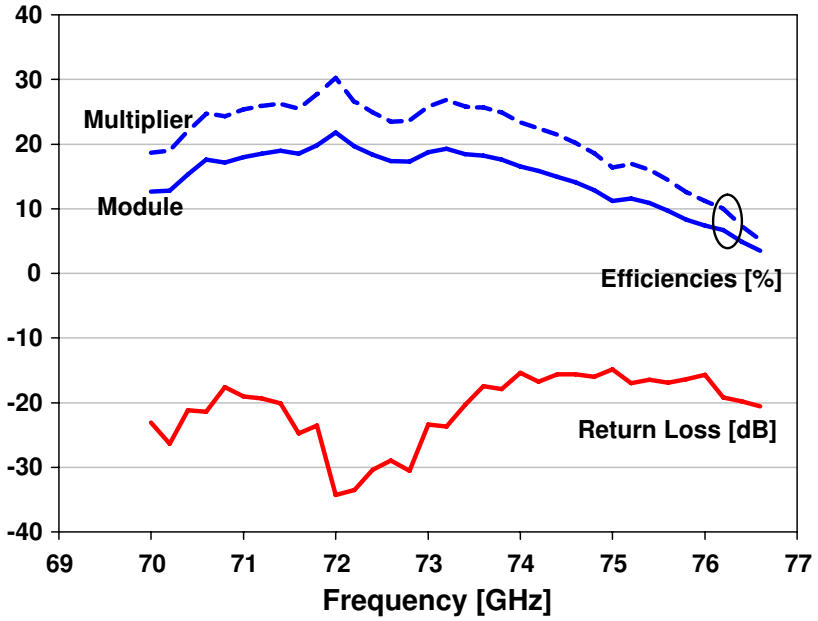


Figure 4.20: Measured results of the back-to-back transition with silicon probes only. The distance between the two probes is 0.95 cm

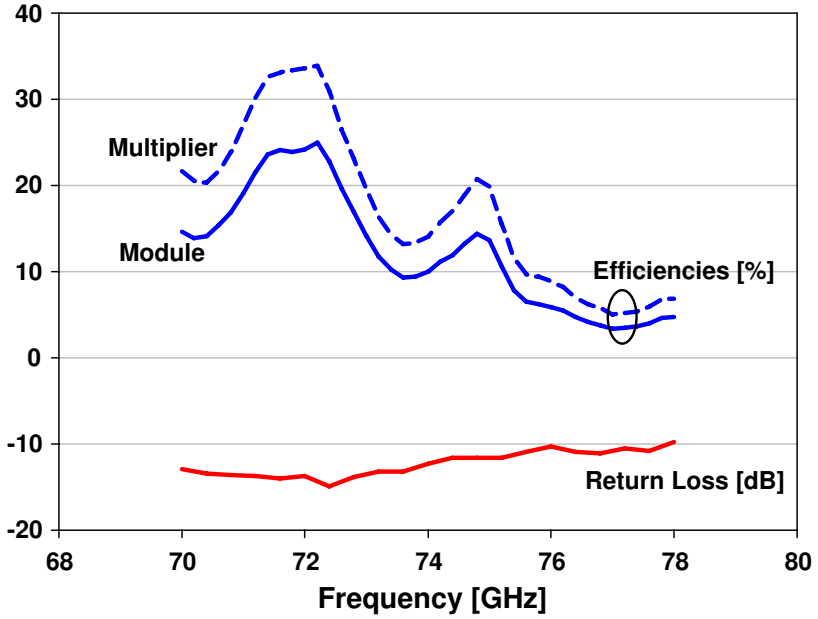
4.5 Experimental Results

To verify the transition performance, the back-to-back transition structure was first measured with silicon probes only. Calibration was achieved with MultiCal [36], a thru-reflect-line (TRL) protocol. The measured results are shown in Fig. 4.20. Loss in the FGC lines is not included, but the loss in the 0.9 cm waveguide section is included in the insertion loss. As can be seen in this figure, the return loss remains better than 10 dB in most of the measured range and the insertion loss is better than 1 dB/transition in a majority of the measured band.

The measurement of the power combining modules is similar to frequency multiplier measurements described in Section 2.6. A *Ka*-band TWT and a variable attenuator was used to vary power levels at the module input. A power meter at the coupled port of a 20 dB coupler on the input side was used to monitor the power delivered to the multipliers. Measurements were taken for the input frequency range of 35 GHz to 40 GHz, with 100 MHz steps. For each frequency points, the input power was varied from 10 dBm up to as



(a) Measured results for the module with Q=2 diode multiplier.



(b) Measured results for the module with Q=3 diode multiplier.

Figure 4.21: Measured efficiencies and return loss for the fabricated power combining modules at the input power levels of 18 dBm. Module efficiencies include multiplier efficiencies, loss in the 3000 μm long multiplier output FGC line, transition loss, and loss in the micromachined waveguide section.

high as 22 dBm, with increments of 1 dBm. Finally, the DC bias was varied at every test points to achieve the maximum performance. The loss in the input and output measurement setup, calculated by measuring the return loss of planar short, open and load standards, was de-embedded in the final efficiency calculation.

Measured efficiencies and return loss versus output frequency for the two types of fabricated modules are shown in Fig. 4.21. As is expected, the module with a lower Q diode multiplier shows relatively lower efficiency and wider bandwidth while the module with a higher Q diode multiplier show relatively higher efficiency and narrower bandwidth. The peak efficiency of the module employing a Q=2 diode multiplier is 21.8% at the output frequency of 72 GHz with an input power of 18 dBm. The peak efficiency of the module employing a Q=3 diode multiplier is 25.0% at the output frequency of 72.2 GHz with input power of also 18 dBm. These efficiencies include the doubler efficiencies, loss in the 3000 μm long 50 Ω output FGC line of the doublers, a GaAs probe transition loss, and loss in 1/2 of the total waveguide section (0.9 cm). By de-embedding these 3 types of losses, efficiencies of the doublers can be calculated. The GaAs probe transition loss and loss in the waveguide section of the module can be approximated from the silicon back-to-back transition measurements Fig. 4.20). This is reasonable since dielectric constants, loss tangents, and resistivities of silicon and GaAs substrates are similar. According to the simulation results in Fig. 4.12, with all the substrate parameters taken into account, the transition performances for both substrates are very close around 72 GHz. Loss in the 3000 μm long doubler output FGC line can be obtained from MultiCal [36] by performing a simple TRL calibration. The calculated doubler efficiencies after de-embedding the losses are plotted in Fig. 4.21. The peak efficiencies are 30.3% and 33.9%, for the Q=2 and Q=3 diode doublers, respectively, both with an input power of 18 dBm. The peak efficiencies are very close to those in Chapter 2. Fig. 4.21 also displays that both modules show excellent return loss across the whole measured band.

In Chapter 2, the Q=2 and Q=3 diode multipliers showed their peak efficiencies at

output frequencies of 76.2 GHz and 76.0 GHz, respectively. The frequency multipliers and thus the power combining modules in this Chapter have their peak efficiencies at 72 GHz and 72.2 GHz, respectively. The shift in the peak efficiency frequency points are due to the difference in the impedances of FGC lines. The frequency multiplier FGC lines in Chapter 2 are fabricated on 625 μm GaAs substrate, whereas the GaAs structure in this Chapter are fabricated out of 100 μm or thinner GaAs substrate due to fabrication error during lapping process. For example, the substrate of the frequency multiplier shown in Fig. 4.19(b) is thinned down to 80 μm. As can be seen from this figure, the GaAs wafer surface is actually lower than the silicon wafer surface. Although full-wave simulations reveal that the transition performance is barely affected by the 20 μm thinner substrate, the frequency multiplier performance is indeed affected due to the changes in the FGC line impedances. FGC lines are relatively insensitive to the substrate thickness as long as the substrate thickness is much larger than the FGC line width ($s+2w$ in Fig. 2.8(b)) [84]. When the substrate thickness is comparable to the FGC line width, the capacitance of the conductor-backed FGC line is increased, and therefore reducing the line impedance. The impedance of the 50 Ω FGC line in the multiplier circuit at 75 GHz, calculated with Sonnet and ADS, is expected to decrease by 9.4% when the substrate is thinned from 625 μm down to 100 μm. If the substrate is thinned even more, for example down to 80 μm, the FGC line impedance is expected to decrease by 13.5 % from its original impedance of 50 Ω.

As was the case with the frequency multipliers in Chapter 2, measured multiplier efficiencies and therefore the module efficiencies as a function of frequency are not smooth curves. This is due to the fact that the DC bias voltage was varied at every test points, to maximize the multiplier performance. Typical bias point was between -5 V and 0 V, with higher (more negative) bias required for lower input power levels. With a fixed bias, smooth efficiency curves are expected as is the case for the frequency multiplier simulated results shown in Fig. 2.14. For example, each bias level will show a curve similar to the gray curves in Fig. 4.22. Since the bias level is adjusted at every test points, the mea-

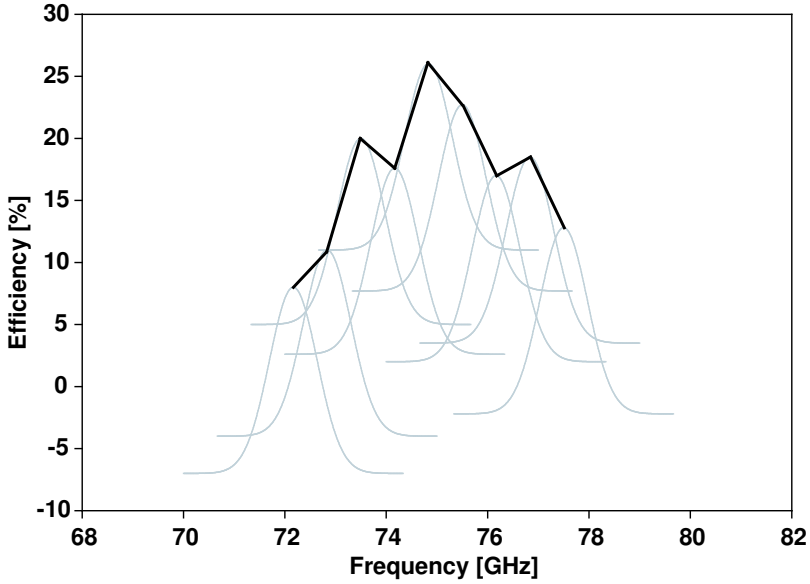
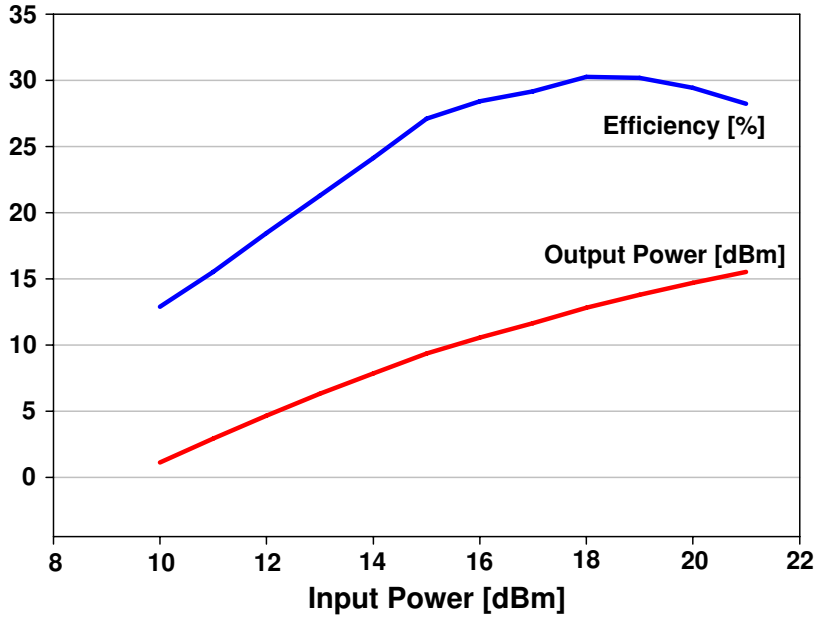
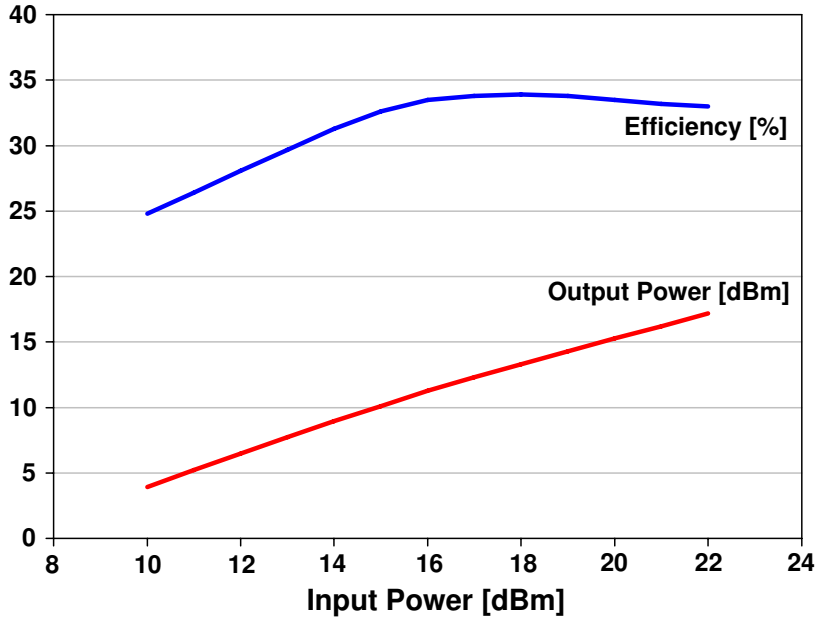


Figure 4.22: Example of multiplier efficiency curves illustrating the roughness if measured efficiency curves in Fig. 2.20, Fig. 2.21, and Fig. 4.21.

sured efficiency curves will be similar to the dark curve shown in the same figure. Another important factor that contributes to the roughness of the efficiency curves is the ripples present in the loss of the input and output measurement sub-systems (see Fig. 2.17(a)). In practice, the small ripples are always seen in every *S*-parameter experiments due to various inevitable measurement errors. In this experiment, the ripples in the loss of the input and output measurement sub-systems are found to be ± 0.16 dB and ± 0.12 dB, respectively. Therefore, the maximum error of the measured output power can be $\frac{\pm 0.16 \pm 0.12}{2} = \pm 0.14$ dB. For example, when the measured output power level is 11 dBm for an input power level of 18 dBm, the efficiency is 20.0%. In the extreme case, when the measured output power is 10.86 dB, 0.14 dB lower than the actual level due to inevitable errors in the measurement setup, the efficiency drops to 19.3%. If the measured output power is 0.14 dB higher than the actual level, the efficiency increases to 20.6%. Although the difference due to the error is small and this error even reduces for larger output power levels (higher efficiencies), it is inevitable and is always seen in efficiency curves.



(a) Module with Q=2 diode multiplier at the output frequency of 72.0 GHz.



(b) Module with Q=3 diode multiplier at the output frequency of 72.2 GHz.

Figure 4.23: Measured efficiencies and output power for the power combining modules.

The module efficiencies can be improved by wafer bonding the two waveguide halves and also by reducing the length of the 3000 μm FGC line section between the doubler output and the probe. There is a significant amount of loss in this section, for example almost 0.7 dB of loss at 72 GHz. As mentioned previously, the purpose of this section is for proper handling and placement of the GaAs structure in the cradle. For instance, if this section is shortened down to 500 μm, the output power levels will be increased by more than 0.5 dB which then increases the peak module efficiencies to 24.8% and 28.4%, respectively. Even when the doubler output FGC line section is shortened, proper handling and placement of the GaAs structure in the cradle can still be achieved by providing enough space on the input side of the multiplier.

Measured module efficiencies and the output power versus the input power at the output frequency of 72 GHz and 72.2 GHz are shown in Fig. 4.23. Due to the large amount of loss (around 9 dB) associated with the input measurement subsystem, the measurement setup was not able to provide more than 21-22 dBm of input power to the multipliers at the frequencies where maximum efficiencies were achieved. Thus, no measurements with higher input power levels were taken at these frequency points. However, as can be seen in the figure, the module output power levels are still not saturated. The efficiencies of both modules start to saturate at the input power level of 16 dBm and are at their peaks at 18 dBm.

4.6 Conclusions

A novel fully-micromachined power combining module that integrates, for the first time, components micromachined out of GaAs and silicon is demonstrated with two different GaAs monolithic frequency doublers. The experimental results are in reasonable agreement with the results expected from the performances of individual module components. The module shows an RF power efficiency of up to 25.0% at the output frequency of

72.2 GHz with an input power of 18 dBm. The module efficiency can be improved further with a minor modification of the circuit and by wafer bonding the waveguide halves..

The biggest challenge in the development of the presented power combining modules lies in reactive ion etching of GaAs for the required depth of 100 μm. Currently, a variety of plasma etching tools specifically designed for GaAs deep etching are commercially available. For example, the plasma etching system Oracle from Trion Technology of Tempe, Arizona, utilizes an electrostatic chuck (E-chuck) to more effectively cool the wafer during the process with helium from the backside, and thus provides capabilities to deep etch GaAs substrates. Wafer cooling is perhaps the biggest issue with deep etching GaAs with conventional RIE systems. Due to the relatively high substrate temperature, the etch selectivity is greatly reduced. It has been to the author's experience that a thin (2000 Å) layer of evaporated nickel, although patterning by wet etching is not straight forward as wet etching other metals, is a very strong plasma etch mask. Etch selectivity as high as 1000:1 has been observed. Unfortunately, nickel mask is not suitable for this work, since metal cannot be directly put on the circuits including diodes. Also, due to the surface topology of diode mesas and air bridges that are as high as 8 μm, photoresist is required to protect the circuit during RIE. The air bridges and diode fingers, shown in Fig. 4.24, are realized with thicker metal layers than usual to provide mechanical strengths in the subsequent processes. In fact, this was the key factor in achieving maximally flat (less than $\pm$ 2.5 μm) mounting for the substrate lapping process.

The power combining module can be cost-effectively micro-fabricated and the passive part of the proposed power combining scheme is well applicable to sub-millimeter and THz range by utilizing the free-standing probe demonstrated in Section 3.5. A silicon micromachined horn antenna can be incorporated with the demonstrated module, and a number of these can be combined together to produce higher output power levels. For example, close to 100 mW of maximum power can be produced at an efficiency of 25% by combining six of the presented power combining module. However additional challenges, such

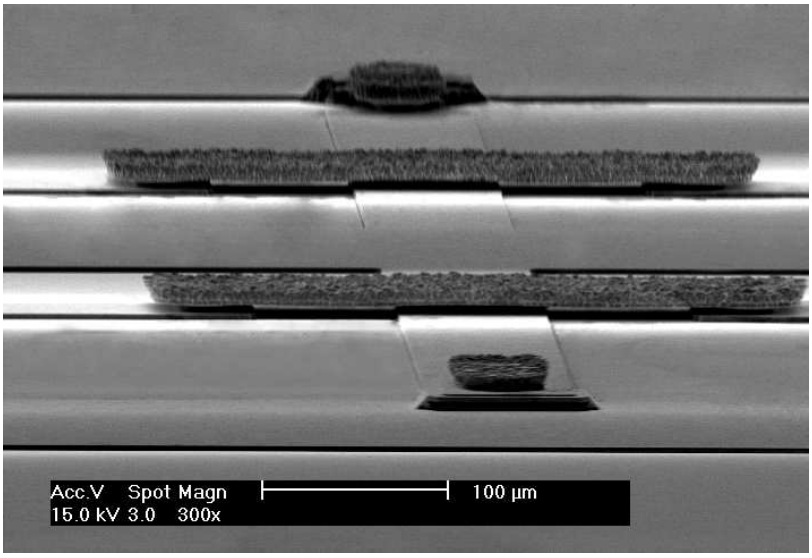


Figure 4.24: Scanning electron micrograph of air bridges and diode fingers after substrate lapping. Relatively thick (> 4 μm) metallization was realized so that the air bridges and fingers can have enough mechanical strength for the subsequent processes.

as phase locking MMIC output signals with suitable power dividing circuits and designing efficiency micromachined horn antenna array that still enables 2D-integration of a number of modules, exist for realizing such a power combining system. Nevertheless, its unique micromachined arrangement for the integration of the heterogeneous components makes the demonstrated power combining module a promising candidate of an efficient power source for millimeter/submillimeter-wave and THz high-power application sources.

CHAPTER 5

Summary and Suggested Future Work

5.1 Summary

A FULLY micromachined power combining module is demonstrated with an RF power efficiency of up to 25% at the output power of 72.2 GHz. In the module, the output signal of a GaAs MMIC frequency multiplier is coupled to a micromachined waveguide via a rectangular transition probe. The waveguide, micromachined in silicon using "split-block" technique, then can be used to feed a highly directive micromachined horn antenna and finally, a number of these modules can be combined together to constitute a fully micromachined waveguide-based power combining system for high-power millimeter-wave applications.

When tested separately, GaAs MMIC frequency multipliers utilized in the demonstrated power combining module show an excellent RF power efficiency of up to 36.1% at the output power of 76.2 GHz. This is the highest efficiency reported for a diode-based MMIC multiplier with the output frequency in the *W*-band (75-110 GHz). In the power combining module, the output of this frequency multiplier is coupled to a micromachined waveguide via a transition probe that couples popular finite ground coplanar line to waveguides. Such a transition, when tested separately in the *W*-band, shows excellent return loss and insertion loss performance across the entire waveguide band. In addition, demonstrated free-standing

probe proves the potential of such transition to be applicable well into the submillimeter-wave and THz regime.

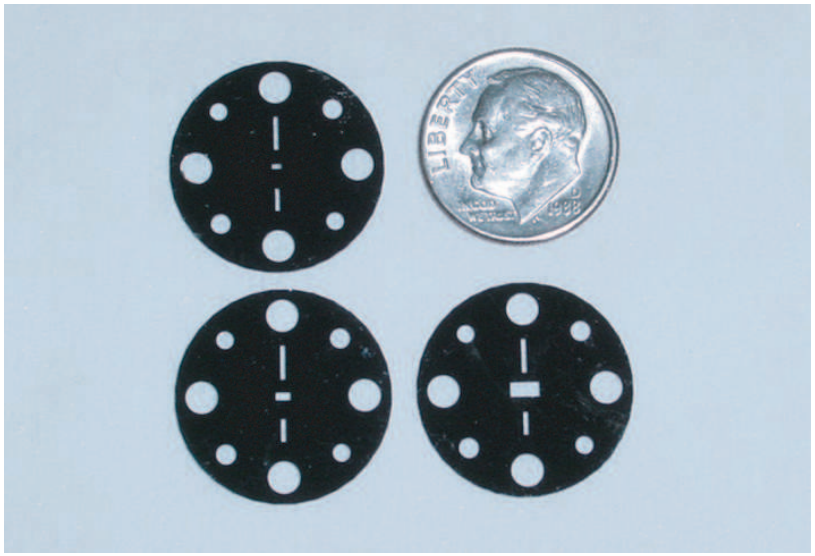
The demonstrated module integrates, for the first time, two heterogeneous components, the compact GaAs MMIC frequency multipliers and silicon micromachined waveguide, through a unique micromachined arrangement. GaAs monolithic circuits provide optimum high frequency performance while silicon micromachined components allow low cost fabrication. In addition, the module efficiency can be improved further by wafer bonding the two waveguide halves and also by reducing the length of the 3000 μm long 50 Ω FGC line section between the multiplier output and the transition probe. Therefore, the proposed power combining system is a promising candidate for a low-cost and efficient power source for high-frequency high-power application sources.

5.2 Suggested Future Work

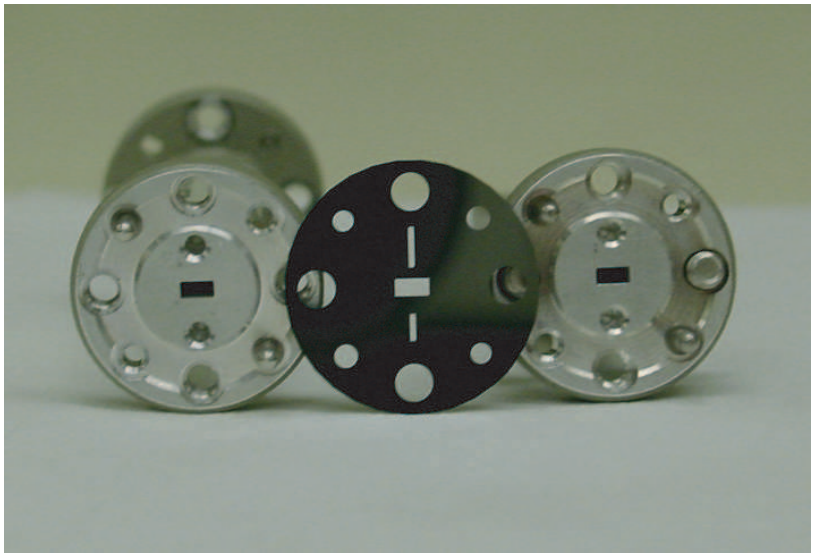
5.2.1 DRIE Waveguides

In Section 3.4, the deep reactive ion etching (DRIE) technique is utilized to develop fully micromachined transitions at WR-10. However, waveguides developed via DRIE have not been investigated alone. Although conventionally machined rectangular waveguides show superior loss performance, DRIE waveguides are expected to exhibit loss that is somewhat higher. This is due to relatively rough sidewalls of DRIE features. Indeed, insertion loss of FGC line to waveguide transition was somewhat higher when DRIE waveguides are employed. Although no measured results are available, WR-3 waveguides (220-325 GHz) have been developed with improved sidewall roughness and sidewall profiles using an optimized DRIE recipe, as shown in Section 3.3. Also, as suggested in the same section, thorough investigations on the sidewall roughness of DRIE features, taking into account the etching time, needs to be performed.

Evaluation of micromachined waveguide performances requires easy use with existing



(a) Micromachined waveguide flanges of WR-3 (top left), WR-5 (bottom left), and WR-10 (bottom right).



(b) Micromachined conventionally machined WR-10 waveguide flanges. The cross sectional dimension of a WR-10 waveguide is 2540 μm $\times$ 1270 μm.

Figure 5.1: Micromachined waveguide flanges. The flanges are fabricated out of 400 μm silicon via DRIE.

waveguide measurement systems. Therefore, a suitable waveguide connections (flanges) need to be developed. The flanges can be also fabricated with the DRIE technique, as shown in Fig. 5.1. Alignment blocks similar to the one shown in Fig. 3.24 can used to accurately align and assemble the micromachined flanges with waveguides.

In fact, development of high performance high frequency micromachined waveguides is an essential part of extending the demonstrated power combining scheme into submillimeter-wave and THz range.

5.2.2 Multifunctional Module

While the power combining module results are promising since it demonstrates the feasibility of proposed power combining system, there remains aspects to be improved. The demonstrated module employs micromachined waveguides developed via wet anisotropic etching of silicon. Although these diamond-shaped waveguides have several advantages, its limited single-mode bandwidth restricts such waveguides from being fully compatible with conventional waveguide systems. Since the transition employing DRIE waveguides has already been designed and demonstrated, not much effort is needed to demonstrate the module with micromachined waveguides with much better compatibility with conventional waveguides. In addition, incorporating highly directive horn antennas and combining a number of such modules to construct the power combining system remain as the ultimate goal. Development of appropriate DC bias network as well as investigations on the power combining efficiency of such a combining system needs to be addressed.

Demonstrated power combining module can be used at high frequency transmitter ends. However, perhaps the most intriguing applications of the demonstrated module are those that utilizes the multifunctionality of the module's passive circuitry. The module can be used also at high frequency receiver ends with, for example, frequency mixers or high frequency detectors in place of the frequency multipliers. High frequency signals, captured by the antenna that is connected to the micromachined waveguide flange, are coupled to

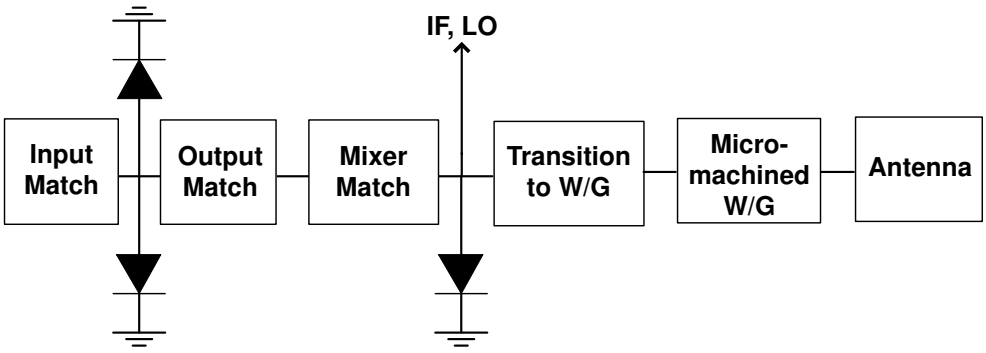


Figure 5.2: Schematic of 183 GHz Radiometer.

an FGC line-based mixer, where the signals are down converted to be processed at lower frequencies. Shown in Fig. 5.2 is a schematic of a radiometer operating at 183 GHz, the research of which has already been initiated by Dr. Jack East at University of Michigan. The complete radiometer block consists of a mixer and a multiplier, which requires use of the demonstrated module's passive circuitry in both directions. Indeed, the demonstrated power combining scheme possesses a potential to be extended to a variety of submillimeter-wave and THz frequency applications.

APPENDICES

Appendix A

Schematic Diagram of Waveguide Blocks for *Ka*-band Transition

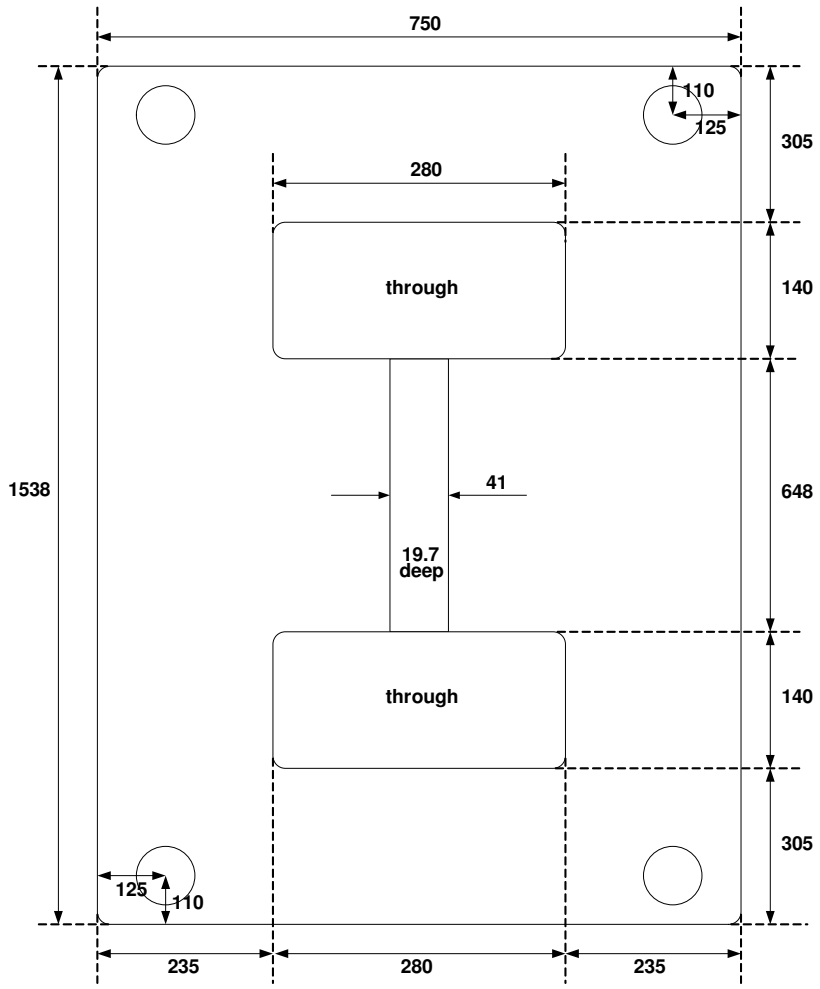


Figure A.1: Schematic diagram of bottom waveguide block for *Ka*-band transition in Section 3.2. The block is conventionally machined out of 1/8 in. thick aluminum.

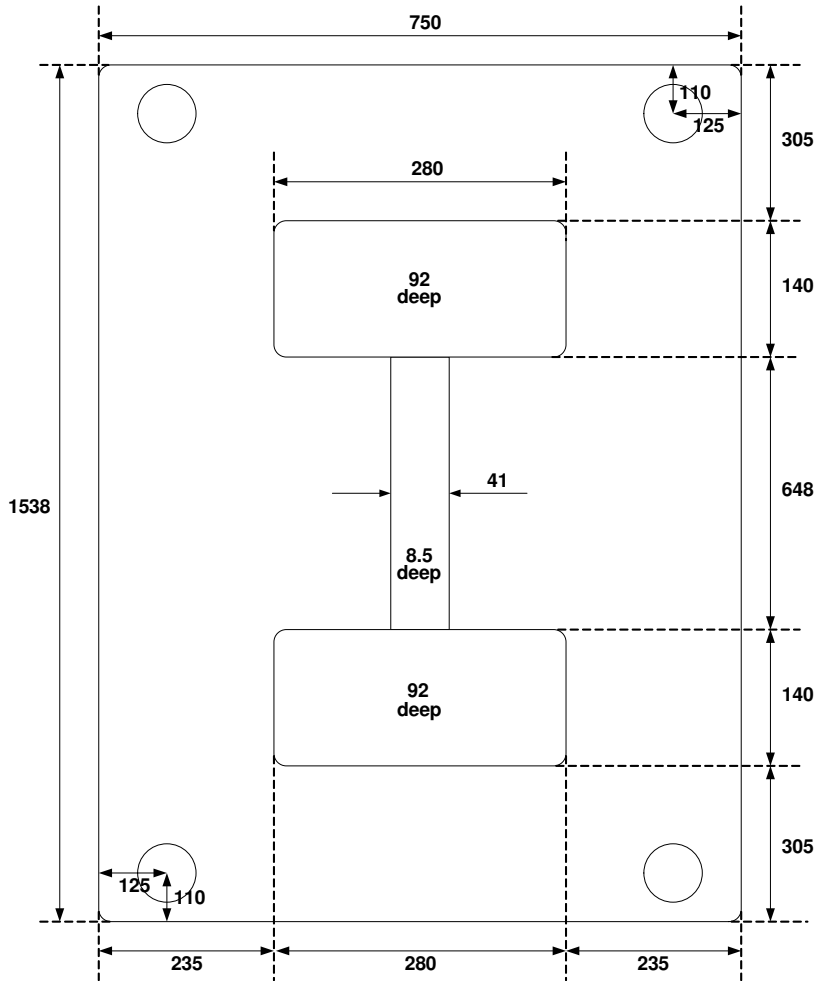
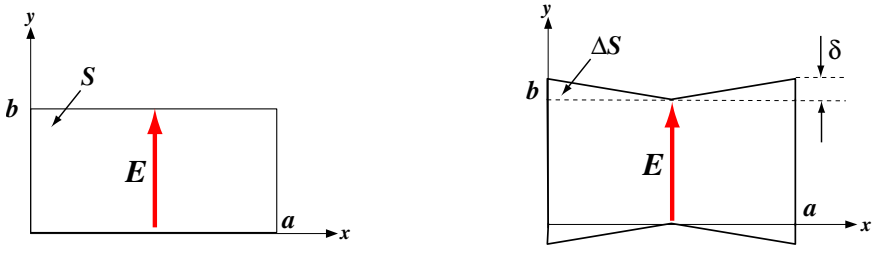


Figure A.2: Schematic diagram of top waveguide block for *Ka*-band transition in Section 3.2. The block is conventionally machined out of 1/8 in. thick aluminum.

Appendix B

DRIE Waveguide Cutoff Frequencies by Perturbation Method

As mentioned in Chapter 3 Section 3.3, the waveguides formed with the DRIE recipe utilized in this work show somewhat negative or reentrant profiles. The cross section of a resulting DRIE waveguide is shown in Fig. B.1(b). The cutoff frequency of such "perturbed"geometry (DRIE waveguide) can be approximated by the cutoff frequency (f_c) of "unperturbed"geometry (rectangular waveguide, Fig. B.1(a)) using perturbation method, and can be expressed as [68]:



(a) Rectangular waveguides. (b) DRIE waveguides.

Figure B.1: Cross sections of rectangular waveguide and DRIE waveguide.

$$\frac{\Delta f_c}{f_c} \approx \frac{\iint_{\Delta S} \left(\mu_o |H_o|^2 - \varepsilon_o |E_o|^2\right) dS}{\iint_S \left(\mu_o |H_o|^2 + \varepsilon_o |E_o|^2\right) dS} \tag{B.1}$$

where E_o and H_o represent the fields of the original geometry excluding any transverse components, i.e. in this case E_x, E_y, H_x, and H_y in S.

For TE_{m0} modes, the electric field and magnetic field components are give as :

$$E_y = \frac{-j\omega\mu_o m\pi}{k_c^2 a} A_{m0} \sin\left(\frac{m\pi x}{a}\right) \exp(-j\beta z) \tag{B.2}$$

$$H_x = \frac{j\beta m\pi}{k_c^2 a} A_{m0} \sin\left(\frac{m\pi x}{a}\right) \exp(-j\beta z) \tag{B.3}$$

$$H_z = A_{m0} \cos\left(\frac{m\pi x}{a}\right) \exp(-j\beta z) \tag{B.4}$$

$$E_x = E_z = H_y = 0 \tag{B.5}$$

where A_{m0} is the amplitude constant for the TE_{m0} mode and $k_c = \left(\frac{m\pi}{a}\right)$, $\beta = \sqrt{k_o^2 - k_c^2}$, and $k_o = \omega\sqrt{\mu_o \varepsilon_o}$.

Even though the magnitude of the electric field ($|E|$) varies from 0 to 1 in S, the field in the perturbed area (ΔS) can be considered as constant since if $\delta \ll b$, ΔS is negligible compared with the original geometry (S). If the electric field in ΔS and can be approximated as the electric field at $x = \frac{3a}{4}$, then Equation B.1 can be simplified as :

$$\frac{\Delta f_c}{f_c} \approx \frac{\left\{\left(\mu_o |H_o|^2_{x=\frac{3a}{4}}\right) - \left(\varepsilon_o |E_o|^2_{x=\frac{3a}{4}}\right)\right\} \cdot \Delta S}{\iint_S \left(\mu_o |H_o|^2 + \varepsilon_o |E_o|^2\right) dS} \tag{B.6}$$

Plugging in the expressions for E_o and H_o in Equations B.2, B.3, and performing the integral further simplifies the equation :

$$\frac{\Delta f_c}{f_c} \approx \frac{\frac{a\delta}{4} \cdot \left(\mu_o \left| Y \sin\left(\frac{3m\pi}{4}\right) \right|^2 - \varepsilon_o \left| X \sin\left(\frac{3m\pi}{4}\right) \right|^2 \right)}{\frac{ab}{2} \left(\mu_o |Y|^2 + \varepsilon_o |X|^2 \right)} \tag{B.7}$$

where $X = \omega\mu_o m\pi / \left(k_c^2 a\right)$ and $Y = \beta m\pi / \left(k_c^2 a\right)$ for TE_{m0} mode.

Thus, for the TE_{m0} mode :

$$\frac{\Delta f_c}{f_c} \approx \frac{\delta}{2b} \cdot \frac{\lambda_o^2\beta^2 - 4\pi^2}{\lambda_o^2\beta^2 + 4\pi^2} \cdot \sin^2\left(\frac{3m\pi}{4}\right) \tag{B.8}$$

where λ_o is the free-space wavelength.

Appendix C

Fabrication Procedures for GaAs Frequency Multipliers

The fabrication procedure details for GaAs frequency multipliers are provided in this appendix. The UV light intensity of the aligner is 20 mW/cm^2. The given developing time and etching time are typical ones. They can vary depending on other conditions, such as humidity. Fresh new developers should always be poured or mixed for consistency. After each chemical process, the wafer should be rinsed thoroughly in cascade DI water for at least 4 min. DI rinse should be at least 10 min. after PRS-*x*000 soaking. Acidic chemicals such as HF often require longer rinses. Plasma asher settings are 100 W at 250 mT, unless specified otherwise. For lift-off processes, ultrasonic bath should be used if necessary.

After annealing, the ohmic contacts should be tested by DC probing two adjacent ohmic pads. Once the ohmic contacts and the Schottky anodes are formed, the test diodes should be tested by DC probing after each steps.

C.1 Wafer Cleaning

1. Immerse wafer in heated Xylene for 2 min.
2. Immerse wafer in Methanol for 2 min.

3. Immerse wafer in Acetone for 2 min.
4. Immerse wafer in Isopropyl Alcohol (IPA) for 2 min.
5. Etch native oxide in BHF for 1 min. followed by DI water rinse.
6. Dehydrate bake at 130°C (hot plate) for 3 min.

C.2 Ohmic Contact Definition

1. Clean wafer by placing in Acetone and IPA for 2 min. each. Dehydrate bake at 130°C (hot plate) for 1 min. Wait until wafer cools down.
2. Spin HMDS/AZ5214-E at 4.5 krpm for 30 sec.
3. Soft bake for 2 min. at 105°C (hot plate).
4. Expose edge bead removal patterns for 1.5 min.
5. Develop in AZ327 for 40 sec.
6. Expose ohmic contact patterns for 4.5 sec.
7. Reverse bake for 1 min. at 130°C (hot plate).
8. Flood expose for 1.5 min.
9. Develop in AZ327 for 40 sec.
10. Plasma ash for 1 min.
11. Etch through n^- layer in H_3PO_4:H_2O_2:H_2O (1:1:8). Typical etch rate is 100 Å/sec. Check with DEKTAK before and after etching.
12. Etch native oxide in BHF for 15 sec.
13. Immediately after drying, load into evaporator and deposit Ni/Ge/Au/Ti/Au 250/325/650/450/2500 Å.
14. Liftoff in Acetone.
15. Immerse in IPA.
16. Immerse wafer in clean Acetone and IPA.
17. Plasma ash at 120 W for 1 min.

18. Anneal ohmic contact metal layers at 240/405/240°C for 20/40/20 sec.

C.3 Schottky Anode Definition

1. Clean wafer by placing in Acetone and IPA for 2 min. each. Dehydrate bake at 130°C (hot plate) for 1 min. Wait until wafer cools down.
2. Spin HMDS/AZ5214-E at 4.5 krpm for 30 sec.
3. Soft bake for 2 min. at 105°C (hot plate).
4. Expose edge bead removal patterns for 1.5 min.
5. Develop in AZ327 for 40 sec.
6. Expose Schottky anode patterns for 4.5 sec.
7. Reverse bake for 1 min. at 130°C (hot plate).
8. Flood expose for 1.5 min.
9. Develop in AZ327 for 40 sec.
10. Plasma ash for 1 min.
11. Etch native oxide in BHF for 15 sec.
12. Immediately after drying, load into evaporator and deposit Ti/Pt/Au 500/500/3000 Å.
13. Liftoff in acetone.
14. Immerse in IPA.
15. Immerse wafer in clean Acetone and IPA.
16. Plasma ash at 120 W for 1 min.

C.4 Mesa Formation

It should be noted that in this step, the image-reversal lift-off photoresist AZ5214-E is used as an etch mask without reversing the image. This is because AZ5214-E provides

better resistance than other AZ18*xx* or AZ9260 photoresist to the etch system used in this step.

1. Clean wafer by placing in Acetone and IPA for 2 min. each. Dehydrate bake at 130°C (hot plate) for 1 min. Wait until wafer cools down.
2. Spin HMDS/AZ5214-E at 2.5 krpm for 30 sec.
3. Soft bake for 2 min. at 105°C (hot plate).
4. Expose edge bead removal patterns for 2 min.
5. Develop in AZ327 for 50 sec.
6. Expose mesa patterns for 4.5 sec.
7. Develop in AZ327 for 50 sec.
8. Hard bake for 1 min. at 130°C (hot plate).
9. Plasma ash for 1 min.
10. Etch mesas in NH_4OH:H_2O_2 (1:24). Typical etch rate is 3.5 μm/min. Examine visually and agitate sample. Use magnetic stirrer if necessary. Etch until all rainbow patterns disappear. Rinse for 10 sec. and immediately follow with an oxide etch in NH_4OH:H_2O (1:15) for 15 sec.
11. Remove remaining photoresist is heated PRS-1000.
12. Plasma ash at 120 W for 1 min.

C.5 FGC Line Patterning

1. Clean wafer by placing in Acetone and IPA for 2 min. each. Dehydrate bake at 130°C (hot plate) for 1 min. Wait until wafer cools down.
2. Spin HMDS/AZ5214-E at 2.5 krpm for 30 sec.
3. Soft bake for 2 min. at 105°C (hot plate).
4. Expose edge bead removal patterns for 2 min.
5. Develop in AZ327 for 50 sec.

6. Expose FGC line patterns for 4.5 sec.
7. Reverse bake for 1 min. at 130°C (hot plate).
8. Flood expose for 1.5 min.
9. Develop in AZ327 for 50 sec.
10. Plasma ash for 1 min.
11. Evaporate Ti/Au 500 Å/1 μm.
12. Liftoff in Acetone. Use ultrasonic bath if necessary.
13. Immerse in IPA.
14. Immerse wafer in clean Acetone and IPA.
15. Plasma ash at 120 W for 1 min.

C.6 Post Definition

1. Clean wafer by placing in Acetone and IPA for 2 min. each. Dehydrate bake at 130°C (hot plate) for 1 min. Wait until wafer cools down.
2. Spin HMDS/AZ1827 at 3 krpm for 30 sec.
3. Soft bake for 30 min. at 90°C (oven).
4. Expose edge bead removal patterns for 1.5 min.
5. Develop in MF351:H_2O (1:5) for 40 sec.
6. Expose post patterns for 12.5 sec.
7. Develop in MF351:H_2O (1:5) for 30 sec.
8. Plasma ash for 1 min.
9. Contour bake for 5 min. on a metal block that has been heated for at least 30 min. in a 130°C oven.
10. Evaporate seed layers of Ti/Au/Ti 500/1500/500 Å.

C.7 Bridge Definition

1. Clean wafer by placing in Acetone and IPA for 2 min. each. Dehydrate bake at 130°C (hot plate) for 1 min. Wait until wafer cools down.
2. Spin AZ1827 at 3 krpm for 30 sec.
3. Soft bake for 30 min. at 90°C (oven).
4. Expose edge bead removal patterns for 1.5 min.
5. Develop in MF351:H_2O (1:5) for 40 sec.
6. Expose bridge patterns for 12.5 sec.
7. Develop in MF351:H_2O (1:5) for 30 sec.
8. Plasma ash for 1 min.
9. Etch exposed top Ti layer in HF:H_2O (1:10) for 5 sec.
10. Electroplate $\sim$3.5 μm in Orotemp-24 gold plating solution held at 55°C. The current level for a certain plating rate differs on various other conditions. Preferred plating rate is $\sim$0.1 μm/min. Check with DEKTAK before and 10 min. after. Electroplate more accordingly.
11. If electroplating was performed in 3440 EECS Laboratory, wafer should be rinsed thoroughly before proceeding to next step. Rinse in cascade water (base bench) for 20 min.
12. Flood expose 3 min.
13. Develop remaining photoresist in MF351:H_2O (1:5) for 1.5 min.
14. Etch top Ti seed layer in HF:H_2O (1:10).
15. Etch Au seed layer in Au etchant. Typical etch rate is 5000 Å$\sim$1 μm/min.
16. Etch bottom Ti seed layer in HF:H_2O (1:10).
17. Remove sacrificial photoresist in heated PRS-1000.
18. Plasma ash at 150 W for 2 min.

Appendix D

Fabrication Procedures for Transition Probes on 100 μm Silicon

The fabrication procedure details for transition probes on 100 μm silicon are provided in this appendix. The UV light intensity of the aligner is 20 mW/cm^2. The given developing time and etching time are typical ones. They can vary depending on other conditions, such as humidity. Fresh new developers should always be poured or mixed for consistency. After each chemical process, the wafer should be rinsed thoroughly in cascade DI water for at least 4 min. DI rinse should be at least 10 min. after PRS-*x*000 soaking. Plasma asher settings are 100 W at 250 mT, unless specified otherwise.

Special care is required when handling 100 μm thick wafers. Before each process step, always follow the wafer mounting process provided in this appendix. Preferred carrier wafers are 400 μm or thicker silicon, slightly larger than the process wafer with any kind of dielectric on both sides.

D.1 Wafer Mounting

1. Clean carrier wafer by soaking in Acetone and IPA for 2 min. each. Dehydrate bake at 130°C (hot plate) for 1 min. Wait until wafer cools down.

2. Spin HMDS/AZ1827 on carrier wafer at 3 krpm for 30 sec.
3. Mount process wafer. Tap gently around edges with back of a pipet, if possible.
4. Place bonded wafers on a flat surface and wait for 2 min.
5. Bake for 30 min. at 120° (oven).

D.2 Alignment Marks

Double side processing is ***preferred*** to avoid exposing Au or other metals, even if buried under photoresist, during DRIE.

1. Clean wafer by placing in Acetone and IPA for 2 min. each. Handle with care. Dehydrate bake at 130°C (hot plate) for 1 min. Wait until wafer cools down.
2. Mount process wafer on a carrier wafer by following wafer mounting steps in D.1.
3. Spin HMDS/AZ9260 at 4 krpm for 30 sec. Spread AZ9260 at 0.5 krpm for 4 sec. prior to spinning.
4. Soft bake for 30 min. at 90°C (oven).
5. Expose alignment mark patterns for 25 sec.
6. Develop in AZ400K:H_2O (1:3) for 1 min.
7. Mount sample on a 4 in. carrier wafer by following wafer mounting steps in D.1.
8. Deep etch using Recipe 1 in Table 3.3. Use a larger aperture to monitor etch. The DRIE etch rate varies much in first 30 min. Examine visually. Do not over etch.
9. Release by placing in Acetone.
10. Immerse in IPA.
11. Plasma ash for 1 min. Handle with care.

D.3 Probe and FGC Line Patterning by Lift-off

1. Clean wafer by placing in Acetone and IPA for 2 min. each. Handle with care. Dehydrate bake at 130°C (hot plate) for 1 min. Wait until wafer cools down.
2. Mount process wafer on a carrier wafer by following wafer mounting steps in D.1.
3. Spin HMDS/AZ5214-E at 2.5 krpm for 30 sec.
4. Soft bake for 2 min. at 105°C (hot plate).
5. Expose metal patterns for 4.5 sec.
6. Reverse bake for 1 min. at 130°C (hot plate).
7. Flood expose for 1.5 min.
8. Develop in AZ327 for 50 sec.
9. Plasma ash for 1 min.
10. Evaporate Ti/Au 500 Å/1 μm.
11. Liftoff in Acetone. Use ultrasonic bath if necessary.
12. Immerse in IPA.
13. Immerse wafer in clean Acetone and IPA.
14. Plasma ash at 120 W for 1 min. Handle with care.

D.4 Probe and FGC Line Patterning by Nickel Electroplating

In order to be suspended in air without the supporting substrate, the metal layers of free-standing probe in Section 3.5 must be thick (> 5 μm) to provide enough mechanical strengths. In this work, this is realized by electroplating nickel described in this section. Nickel is preferred due to the less amount of inherent stress than gold, although further investigation on stress in metal layers is required. It should be noted that wet etching nickel is not straight forward as wet etching other metals.

1. Clean wafer by placing in Acetone and IPA for 2 min. each. Handle with care. Dehydrate bake at 130°C (hot plate) for 1 min. Wait until wafer cools down.
2. Mount process wafer on a carrier wafer by following wafer mounting steps in D.1.
3. Deposit seed layers by sputtering 2000 Å of Ti and evaporating 500 Å of Ni.
4. Spin AZ9260 at 3 krpm for 30 sec. Spread AZ9260 at 0.5 krpm for 4 sec. prior to spinning.
5. Soft bake for 30 min. at 90°C (oven).
6. Expose metal patterns for 40 sec.
7. Develop in AZ400K:H_2O (1:3) for 1 min.
8. Plasma ash for 1 min.
9. Electroplate $\sim$8 μm of Ni. The current level for a certain plating rate differs on various other conditions. Preferred plating rate is $\sim$0.1 μm/min. Check with DEKTAK before and 10 min. after. Electroplate more accordingly.
10. Flood expose for 3 min.
11. Develop remaining photoresist in AZ400K:H_2O (1:3) for 3 min.
12. Etch Ni seed layer in HCl:H_2O (1:1) for 3 min.
13. Etch Ti seed layer in HF:H_2O (1:10) for 10 sec.
14. Repeat above two steps, if necessary.
15. Clean wafer in Acetone/IPA.

D.5 Probe Releasing

1. Clean wafer by placing in Acetone and IPA for 2 min. each. Handle with care. Dehydrate bake at 130°C (hot plate) for 1 min. Wait until wafer cools down.
2. Mount process wafer on a carrier wafer by following wafer mounting steps in D.1.
3. Spin HMDS/AZ9260 at 4 krpm for 30 sec. Spread AZ9260 at 0.5 krpm for 4 sec. prior to spinning.

4. Soft bake for 30 min. at 90°C (oven).
5. Expose etch patterns for 25 sec.
6. Develop in AZ400K:H_2O (1:3) for 1 min.
7. Mount sample on a 4 in. carrier wafer by following wafer mounting steps in D.1.
8. Deep etch using Recipe 1 in Table 3.3. DRIE etch rate varies much in first 30 min. Examine visually.
9. (***For free-standing probe only***) Etch exposed Ti layer of probe in HF:H_2O (1:10) for 5 sec. This is done to relieve the stress coming from the interface of nickel and titanium.
10. Release by placing in Acetone.
11. Immerse in IPA.
12. If necessary, use heated PRS-2000 to clean released probes. Handle with care. Use petri dishes and teflon tweezers.

Appendix E

Fabrication Procedures for Waveguide Transition Structures

The fabrication procedure details for micromachined waveguide transition structures on 2 mm silicon are provided in this appendix. The UV light intensity of the aligner is 20 mW/cm^2. The given developing time and etching time are typical ones. They can vary depending on other conditions, such as humidity. Fresh new developers should always be poured or mixed for consistency. After each chemical process, the wafer should be rinsed thoroughly in cascade DI water for at least 4 min. Acidic chemicals such as HF often require longer rinses. DI rinse should be at least 10 min. after PRS-*x*000 soaking. Plasma asher settings are 100 W at 250 mT, unless specified otherwise.

E.1 2 mm Silicon Wafer Dicing

In order to process 4 in. silicon wafers with 3 in. wafer processing tools (for example MJB-3 aligner), the wafers need to be scribed into smaller pieces. However, for 2 mm silicon wafers, this can be done only by dicing. The following are the dicing parameters :

- Spindle speed : 5.0 krpm

  This is the speed at which blade spins.

- Thickness : 84 mils

  This is the thickness of the wafer and the wafer-mounting blue film.

- Depth per cut : 4 mils

  This is the maximum dicing depth for each travel.

- Height : 2 mils

  This is the remaining height after dicing. For through-wafer dicing, the height should be set slightly less than the blue film thickness ($\sim 3.5\ \mu$m).

- Cutting Speed : 40 mils/sec.

  This is the speed at which the spindle travels with respect to the wafer.

- After dicing, silicon wafers should be cleaned thoroughly by Piranha cleaning in H_2SO_4:H_2O_2 (1:1). Always add acid to H_2O_2. If the wafer is bare (without any dielectric), oxide etch in BHF (or HF:H_2O (1:10)) should always follow.

E.2 DRIE Waveguide

Although the procedures described here assumes only photoresist etch masking layer, additional hard mask such as thermal oxide is preferred to improve sidewall roughness of DRIE features. This is of critical importance when developing waveguides. When using thermal oxide as a secondary mask, reactive ion etching (RIE) is preferred than wet etching for patterning the oxide. If, for any reason, having thermal oxide is not possible, a thin layer of Ni (2000 Å) on 500 Å of Ti may provide equivalent masking. In this step, thick layer of photoresist is realized by coating twice.

1. Clean wafer by placing in Acetone and IPA for 2 min. each. Handle with care. Dehydrate bake at 130°C (hot plate) for 1 min. Wait until wafer cools down.
2. Spin first HMDS/AZ9260 layer at 2 krpm for 30 sec and wait 2 min. with wafer resting on spinner. Spread AZ9260 at 0.5 krpm for 4 sec. prior to spinning.
3. Rest wafer on flat surface for 20 min.

4. Soft bake for 30 min. at 90°C (oven).
5. Rest wafer on flat surface for 20 min.
6. Spin second AZ9260 layer at 2 krpm for 60 sec and wait 2 min. with wafer resting on spinner. Spread AZ9260 at 0.5 krpm for 4 sec. prior to spinning.
7. Rest wafer on flat surface for 20 min.
8. Soft bake for 30 min. at 90°C (oven).
9. Rest wafer on flat surface for 20 min.
10. Expose waveguide patterns for 240∼260 sec.
11. Develop in AZ400K:H_2O (1:3). Developing times from 2 min. to more than 5 min. have been observed.
12. Mount sample on 4 in. carrier wafer by following wafer mounting procedures in D.1.
13. Deep etch using Recipe 1 in Table 3.3. Monitor etch rate by placing thinner (100, 200, 400 μm) silicon wafers with sizes approximately same as waveguide patterns. Measure etch depth with Zygo.
14. Release by placing in PRS-2000.
15. Plasma ash for 3 min. at 120 W.
16. Dice to separate top and bottom waveguide halves using dicing parameters in E.1.
17. Sputter 500 Å of Ti and 2 μm of Au. Static sputtering is required for Au.

E.3 Diamond Waveguide

Although the etch rate of thermal oxide in TMAH is negligible, it is safe to have at least 5000 Å thermal oxide to form 1.27 μm deep V grooves in TMAH. Masks should be generated taking into account the 001/111 selectivity of roughly 10/1.

1. Clean wafer by placing in Acetone and IPA for 2 min. each. Handle with care. Dehydrate bake at 130°C (hot plate) for 1 min. Wait until wafer cools down.

2. Spin HMDS/AZ1827 at 3 krpm for 30 sec.
3. Soft bake for 2 min. at 105°C (hot plate).
4. Expose waveguide patterns for 14.5 sec.
5. Develop in MF351:H_2O (1:5) for 30 sec.
6. Hard bake for 1 min. at 130°C (hot plate).
7. Plasma ash for 1 min.
8. (***Only when patterning oxide by wet etching***) To protect oxide on backside from etching, mountwafer on a carrier wafer by following wafer mounting steps in D.1.
9. Pattern oxide by wet etching in BHF or HF:H_2O (1:10), or by RIE. Typical oxide etch rate in BHF and HF:H_2O (1:10) is 1000 Å/min.
10. Check by measuring the oxide thickness with Ellipsometer or other tool capable of measuring thin film thicknesses. Etch more if necessary.
11. Remove remaining photoresist in Acetone.
12. Immerse in IPA.
13. Immerse wafer in clean Acetone and IPA.
14. Etch oxide for additional 15 sec.
15. Keep sample immersed in DI water. Immediately after removing sample from DI water, place in TMAH that has already been heated to 80°C.
16. When etching is finished, rinse in DI water for 20 min.
17. Dice to separate top and bottom waveguide halves using dicing parameters in E.1.
18. Sputter 500 Å of Ti and 2 μm of Au. Static sputtering is required for Au.

E.4 Deep Etching Probe Cradles

3000 Å of sputtered Ti is used as an additional masking layer in this step.

1. Clean wafer by placing in Acetone and IPA for 2 min. each. Handle with care.

Dehydrate bake at 130°C (hot plate) for 1 min. Wait until wafer cools down.

2. Sputter 3000 Å of Ti.
3. Spin AZ9260. Spinning speed varies depending on waveguide structure. Try different spinning speeds and choose one that provides best protection and uniformity around immediate edges of waveguide. 60 sec. spinning often provides better uniformity. Spread AZ9260 for 4 sec. prior to spinning.
4. Soft bake for 30 min. at 90°C (oven).
5. Expose groove patterns. Set exposure time according to the spinning speed. Typical exposure time is 25 sec. for 4 krpm spins, 40 sec. for 3 krpm spins, and 75 sec. for 2 krpm spins.
6. Develop in AZ400K:H_2O (1:3).
7. Plasma ash for 1 min.
8. Mount sample on 4 in. carrier wafer by following wafer mounting procedures in D.1.
9. Deep etch using Recipe 1 in Table 3.3. Monitor etch rate by placing 100 μm silicon wafers with sizes approximately same as groove patterns. Ensure etch depth of 100 μm by measuring with DEKTAK. Etch more if necessary.
10. Release by placing in PRS-2000.
11. Plasma ash for 3 min. at 120 W.

Appendix F

Fabrication Procedures for GaAs Structure of Power Combining Module

The fabrication procedure details for GaAs structure of the power combining module in Chapter 4 are provided in this appendix. The majority of the process is the same as the frequency multiplier process in Appendix C. The differences are in the air bridge/diode finger step, and the additional RIE and wafer lapping steps to define and release each GaAs structures. Relatively thick (> 4 μm) metallization is realized using a thicker photoresist so that the air bridges and diode fingers have sufficient mechanical for the subsequent processes.

The UV light intensity of the aligner is 20 mW/cm^2. The given developing time and etching time are typical ones. They can vary depending on other conditions, such as humidity. Fresh new developers should always be poured or mixed for consistency. After each chemical process, the wafer should be rinsed thoroughly in cascade DI water for at least 4 min. DI rinse should be at least 10 min. after PRS-*x*000 soaking. Acidic chemicals such as HF often require longer rinses. Plasma asher settings are 100 W at 250 mT, unless specified otherwise. For lift-off processes, ultrasonic bath should be used only if necessary.

After annealing, the ohmic contacts should be tested by DC probing two adjacent ohmic pads. Once the ohmic contacts and the Schottky anodes are formed, the test diodes should

be tested by DC probing after each steps.

F.1 Wafer Cleaning

1. Immerse wafer in heated Xylene for 2 min.
2. Immerse wafer in Methanol for 2 min.
3. Immerse wafer in Acetone for 2 min.
4. Immerse wafer in Isopropyl Alcohol (IPA) for 2 min.
5. Etch native oxide in BHF for 1 min. followed by DI water rinse.
6. Dehydrate bake at 130°C (hot plate) for 3 min.

F.2 Ohmic Contact Definition

1. Clean wafer by soaking in Acetone and IPA for 2 min. each. Dehydrate bake at 130°C (hot plate) for 1 min. Wait until wafer cools down.
2. Spin HMDS/AZ5214-E at 4.5 krpm for 30 sec.
3. Soft bake for 2 min. at 105°C (hot plate).
4. Expose edge bead removal patterns for 1.5 min.
5. Develop in AZ327 for 40 sec.
6. Expose ohmic contact patterns for 4.5 sec.
7. Reverse bake for 1 min. at 130°C (hot plate).
8. Flood expose for 1.5 min.
9. Develop in AZ327 for 40 sec.
10. Plasma ash for 1 min.
11. Etch through n^- layer in H_3PO_4:H_2O_2:H_2O (1:1:8). Typical etch rate is 100 Å/sec. Check with DEKTAK before and after etching.
12. Etch native oxide in BHF for 15 sec.

13. Immediately after drying, load into evaporator and deposit Ni/Ge/Au/Ti/Au 250/325/650/450/2500 Å.
14. Liftoff in Acetone.
15. Immerse in IPA.
16. Immerse wafer in clean Acetone and IPA.
17. Plasma ash at 120 W for 1 min.
18. Anneal ohmic contact metal layers at 240/405/240°C for 20/40/20 sec.

F.3 Schottky Anode Definition

1. Clean wafer by soaking in Acetone and IPA for 2 min. each. Dehydrate bake at 130°C (hot plate) for 1 min. Wait until wafer cools down.
2. Spin HMDS/AZ5214-E at 4.5 krpm for 30 sec.
3. Soft bake for 2 min. at 105°C (hot plate).
4. Expose edge bead removal patterns for 1.5 min.
5. Develop in AZ327 for 40 sec.
6. Expose Schottky anode patterns for 4.5 sec.
7. Reverse bake for 1 min. at 130°C (hot plate).
8. Flood expose for 1.5 min.
9. Develop in AZ327 for 40 sec.
10. Plasma ash for 1 min.
11. Etch native oxide in BHF for 15 sec.
12. Immediately after drying, load into evaporator and deposit Ti/Pt/Au 500/500/3000 Å.
13. Liftoff in acetone.
14. Immerse in IPA.
15. Immerse wafer in clean Acetone and IPA.

16. Plasma ash at 120 W for 1 min.

F.4 Mesa Formation

It should be noted that in this step, the image-reversal lift-off photoresist AZ5214-E is used as an etch mask without reversing the image. This is because AZ5214-E provides better resistance than other AZ18*xx* or AZ9260 photoresist to the etch system used in this step.

1. Clean wafer by soaking in Acetone and IPA for 2 min. each. Dehydrate bake at 130°C (hot plate) for 1 min. Wait until wafer cools down.
2. Spin HMDS/AZ5214-E at 2.5 krpm for 30 sec.
3. Soft bake for 2 min. at 105°C (hot plate).
4. Expose edge bead removal patterns for 2 min.
5. Develop in AZ327 for 50 sec.
6. Expose mesa patterns for 4.5 sec.
7. Develop in AZ327 for 50 sec.
8. Hard bake for 1 min. at 130°C (hot plate).
9. Plasma ash for 1 min.
10. Etch mesas in NH_4OH:H_2O_2 (1:24). Typical etch rate is 3.5 μm/min. Examine visually and agitate sample. Use magnetic stirrer if necessary. Etch until all rainbow patterns disappear. Rinse for 10 sec. and immediately follow with an oxide etch in NH_4OH:H_2O (1:15) for 15 sec.
11. Remove remaining photoresist is heated PRS-1000.
12. Plasma ash at 120 W for 1 min.

F.5 FGC Line Patterning

1. Clean wafer by soaking in Acetone and IPA for 2 min. each. Dehydrate bake at 130°C (hot plate) for 1 min. Wait until wafer cools down.
2. Spin HMDS/AZ5214-E at 2.5 krpm for 30 sec.
3. Soft bake for 2 min. at 105°C (hot plate).
4. Expose edge bead removal patterns for 2 min.
5. Develop in AZ327 for 50 sec.
6. Expose FGC line patterns for 4.5 sec.
7. Reverse bake for 1 min. at 130°C (hot plate).
8. Flood expose for 1.5 min.
9. Develop in AZ327 for 50 sec.
10. Plasma ash for 1 min.
11. Evaporate Ti/Au 500 Å/1 μm.
12. Liftoff in Acetone. Use ultrasonic bath if necessary.
13. Immerse in IPA.
14. Immerse wafer in clean Acetone and IPA.
15. Plasma ash at 120 W for 1 min.

F.6 Post Definition

1. Clean wafer by soaking in Acetone and IPA for 2 min. each. Dehydrate bake at 130°C (hot plate) for 1 min. Wait until wafer cools down.
2. Spin HMDS/AZ1827 at 3 krpm for 30 sec.
3. Soft bake for 30 min. at 90°C (oven).
4. Expose edge bead removal patterns for 1.5 min.
5. Develop in MF351:H_2O (1:5) for 40 sec.
6. Expose post patterns for 12.5 sec.

7. Develop in MF351:H_2O (1:5) for 30 sec.
8. Plasma ash for 1 min.
9. Contour bake for 5 min. on a metal block that has been heated for at least 30 min. in a 130°C oven.
10. Evaporate seed layers of Ti/Au/Ti 500/1500/500 Å.

F.7 Bridge Definition

1. Clean wafer by soaking in Acetone and IPA for 2 min. each. Dehydrate bake at 130°C (hot plate) for 1 min. Wait until wafer cools down.
2. Spin AZ9260 at 4 krpm for 30 sec.
3. Soft bake for 30 min. at 90°C (oven).
4. Expose edge bead removal patterns for 2 min.
5. Develop in AZ400K:H_2O (1:3) for 1∼2 min.
6. Expose bridge patterns for 25 sec.
7. Develop in AZ400K:H_2O (1:3) for 1 min.
8. Plasma ash for 1 min.
9. Etch exposed top Ti layer in HF:H_2O (1:10) for 5 sec.
10. Electroplate ∼6 μm in Orotemp-24 gold plating solution held at 55°C. The current level for a certain plating rate differs on various other conditions. Preferred plating rate is ∼0.1 μm/min. Check with DEKTAK before and 10 min. after. Electroplate more accordingly.
11. If electroplating was performed in 3440 EECS Laboratory, wafer should be rinsed thoroughly before proceeding to next step. Rinse in cascade water (base bench) for 20 min.
12. Flood expose 3 min.
13. Develop remaining photoresist in AZ400K:H_2O (1:5) for 3 min.

14. Etch top Ti seed layer in HF:H_2O (1:10).
15. Etch Au seed layer in Au etchant. Typical etch rate is 5000 Å$\sim$1 μm/min.
16. Etch bottom Ti seed layer in HF:H_2O (1:10).
17. Remove sacrificial photoresist in heated PRS-1000.
18. Plasma ash at 150 W for 2 min.

F.8 Structure Definition

1. Clean wafer by soaking in Acetone and IPA for 2 min. each. Dehydrate bake at 130°C (hot plate) for 1 min. Blow dry with care. Wait until wafer cools down.
2. Spin first HMDS/AZ9260 layer at 2 krpm for 30 sec and wait 2 min. with wafer resting on spinner. Spread AZ9260 at 0.5 krpm for 4 sec. prior to spinning.
3. Rest wafer on flat surface for 20 min.
4. Soft bake for 30 min. at 90°C (oven).
5. Rest wafer on flat surface for 20 min.
6. Spin second AZ9260 layer at 2 krpm for 60 sec and wait 2 min. with wafer resting on spinner. Spread AZ9260 at 0.5 krpm for 4 sec. prior to spinning.
7. Rest wafer on flat surface for 20 min.
8. Soft bake for 30 min. at 90°C (oven).
9. Rest wafer on flat surface for 20 min.
10. Spin third AZ9260 layer at 2 krpm for 60 sec and wait 2 min. with wafer resting on spinner. Spread AZ9260 at 0.5 krpm for 4 sec. prior to spinning.
11. Rest wafer on flat surface for 20 min.
12. Soft bake for 30 min. at 90°C (oven).
13. Rest wafer on flat surface for 20 min.
14. Expose etch patterns for 315 sec.
15. Develop in AZ400K:H_2O (1:3). Developing times from 2 min. to more than 5 min.

have been observed.

16. Prepare a 4 in. silicon carrier wafer with evaporated Ti/Ni 500/2000 Å. Spin first AZ960 layer at 2 krpm for 30 sec. and wait 2 min. with wafer resting on spinner. Spread AZ9260 at 0.5 krpm for 4 sec. prior to spinning. Rest wafer on flat surface for 20 min. Soft bake for 30 min. at 90°C (oven). Rest wafer on flat surface for 20 min. Spin second AZ960 layer at 2 krpm for 60 sec. and wait 2 min. with wafer resting on spinner. Spread AZ9260 at 0.5 krpm for 4 sec. prior to spinning. Rest wafer on flat surface for 20 min.
17. Mound GaAs wafer on carrier wafer.
18. Soft bake for 30 min. at 90°C (oven).
19. Hard bake for 2 hrs. at 110°C (oven).
20. Etch patterns 100 μm deep in PlasmaTherm RIE. Ensure chamber is in good condition prior to etching. Physical cleaning with 6% H_2O_2 prior to etching improves selectivity.
21. Release by placing in Acetone.
22. Immerse in IPA.
23. If necessary, use heated PRS-1000 to clean released probes. Handle with care.
24. Plasma ash at 150 W for 2$\sim$3 min.

F.9 Substrate Lapping

1. Clean wafer by soaking in Acetone and IPA for 2 min. each. Dehydrate bake at 130°C (hot plate) for 1 min. Blow dry with care. Wait until wafer cools down.
2. Spin first HMDS/AZ9260 layer at 2 krpm for 30 sec and wait 2 min. with wafer resting on spinner. Spread AZ9260 at 0.5 krpm for 4 sec. prior to spinning.
3. Rest wafer on flat surface for 20 min.
4. Soft bake for 30 min. at 90°C (oven).

5. Rest wafer on flat surface for 20 min.
6. While GaAs sample is resting, prepare a silicon carrier wafer. Thin 200 μm wafers are preferred. Spin HMDS/AZ960 at 2 krpm for 30 sec. and wait 2 min. with wafer resting on spinner. Spread AZ9260 at 0.5 krpm for 4 sec. prior to spinning.
7. Place the GaAs sample on the carrier wafer upside down. Place a glass slide on flipped GaAs wafer and 3 weights in Fig. 4.11 on the glass to apply pressure.
8. Rest wafers and weights on flat surface for 60 min.
9. Soft bake for 30 min. at 90°C (oven).
10. Hard bake for 1.5 hrs. at 110°C (oven).
11. Using hot plate, heat glass chuck to $\sim$100°C. Apply small amount of wax on glass chuck center and wait until wax melts. Heat glass slide and weight as well.
12. Place bonded wafers on melted wax. Place heated glass slide and weight on wafer to apply pressure. Keep on hot plate for 5 min.
13. Remove from hot plate. Keep the glass slide as well as the weight on wafer. Place glass chuck on thick clean room towel to avoid direct contact between glass chuck and cold table surfaces..
14. Wait until everything cools down to room temperature.
15. Lap substrate down to 100 μm with 3 μm grit at rotational speed of 10$\sim$15 rpm.
16. When lapping is finished, clean with DI water.
17. Heat glass chuck on 130° hot plate and slide off silicon carrier wafer.
18. Clean wafer by placing in heated Xylene.
19. Release GaAs structures by placing in Acetone. Use petri dishes and teflon tweezers. Handle with care.
20. Clean GaAs structures in heated PRS-1000. Use petri dishes and teflon tweezers. Handle with care.

BIBLIOGRAPHY

BIBLIOGRAPHY

[1] F. T. Ulaby, "Scanning the issue, terahertz technology," *Proceedings of the IEEE*, vol. 80, pp. 1659–1661, Nov. 1992.

[2] D. M. Pozar, *Microwave Engineering*. Addison-Wesley, 1990.

[3] S. E. Rosenbaum, B. K. Kormanyos, L. M. Jelloian, M. Matloubian, A. S. Brown, L. E. Larson, L. D. Nguyen, M. A. Thompson, L. P. B. Katehi, and G. M. Rebeiz, "155- and 213 GHz AlInAs/GaInAs/InP HEMT MMIC oscillators," *IEEE Trans. Microwave Theory and Tech.*, vol. 438, no. 4, pp. 927–932, April 1995.

[4] H. Eisele, "High performance InP gunn devices with 34 mW at 193 GHz," *Electronics Letters*, vol. 38, no. 16, pp. 923–924, August 2002.

[5] ——, "Second-harmonic power extraction from InP gunn devices with more than 1 mW in 260-320 GHz frequency range," *Electronics Letters*, vol. 34, no. 25, pp. 2412–2413, December 1998.

[6] H. Eisele, A. Rydberg, and G. I. Hadaad, "Recent advances in the performance of InP gunn devices and GaAs TUNNETT diodes for the 100-300 GHz frequency range and above," *IEEE Trans. Microwave Theory and Tech.*, vol. 48, no. 4, pp. 626–631, April 2000.

[7] Y. Campos-Roca, L. Verweyen, M. Fernández-Barciela, E. Sánchez, M. C. Currás-Francos, W. Bronner, A. Hälsmann, and M. Schlechtweg, "An optimized 25.5-76.5 GHz PHEMT-based coplanar frequency tripler," *IEEE Microwave and Guided Wave Letters*, vol. 10, no. 6, pp. 242–244, June 2000.

[8] X. Mélique, A. Maestrini, R. Farré, P. Mounaix, M. Favreau, O. Vanbésien, J.-M. Goutoule, F. Mollot, G. Beaudin, T. Nŕhi, and D. Lippens, "Fabrication and performance of InP-based heterostructure barrier varactors in a 250-GHz waveguide tripler," *IEEE Trans. Microwave Theory and Tech.*, vol. 48, no. 6, pp. 1000–1006, June 2000.

[9] A. Maestrini, J. Bruston, D. Pukala, S. Martin, and I. Mehdi, "Performance of a 1.22 THz frequency tripler using a GaAs frameless membrane monolithic circuit," *IEEE MTT-S International Microwave Symposium Digest*, pp. 1657–1660, 2001.

[10] M. P. DeLisio and R. A. York, "Quasi-optical and spatial power combining," *IEEE Trans. Microwave Theory and Tech.*, vol. 50, no. 3, pp. 929–936, March 2002.

[11] A. Moussessian, M. C. Wanke, Y. Li, J.-C. Chiao, S. J. Allen, T. W. Crowe, and D. B. Rutledge, "A terahertz grid frequency doubler," *IEEE Trans. Microwave Theory and Tech.*, vol. 46, no. 11, pp. 1976–1981, November 1998.

[12] J. P. Becker, Y. Lee, J. R. East, and L. P. Katehi, "Silicon micromachined power combining modulle," DARPA THz Solid State Sources Review, Tech. Rep., 2000.

[13] A. V. Räisänen, T. J. Tolmunen, M. Natzic, M. A. Frerking, E. Brown, H. Gronqvist, and S. M. Nilsen, "A single barrier varactor quintupler at 170GHz," *IEEE Trans. Microwave Theory and Tech.*, vol. 43, no. 3, pp. 685–686, March 1995.

[14] V. Radisic, M. Micovic, M. Hu, P. Janke, C. Ngo, L. Nguyen, L. Samoka, and M. Morgan, "164-GHz MMIC HEMT Doubler," *IEEE Microwave and Wireless Component Letters*, vol. 11, no. 6, pp. 241–243, June 2001.

[15] H. Zirath, I. Angelov, N. Rorsman, C. Kalrsson, and E. Kollberg, "A balanced *W*-band HFET doubler," *Proc. 23rd European Microwave Conference*, pp. 837–839, September 1993.

[16] M. Morgan and S. Weinreb, "A full waveguide band MMIC tripler for 75-110 GHz," *IEEE MTT-S International Microwave Symposium Digest*, pp. 103–106, 2001.

[17] T. J. Tolmunen and A. V. Räisänen, "An efficient schottky-varactor frequency multiplier at millimeter waves, Part I," *International Journal of Infrared and Millimeter Waves*, vol. 8, pp. 1313–1336, 1987.

[18] D. W. Porterfield, T. W. Crowe, R. F. Bradley, and N. R. Erickson, "A high-power fixed-tuned millimeter-wave balanced frequency doubler," *IEEE Trans. Microwave Theory and Tech.*, vol. 47, no. 4, pp. 419–425, April 1999.

[19] S. Martin, B. Nakamura, A. Fung, P. Smith, J. Bruston, A. Maestrini, F. Maiwald, peter Siegel, E. Schlecht, and I. Mehdi, "Fabrication of 200 to 2700 GHz multiplier devices using GaAs and metal membranes," *IEEE MTT-S International Microwave Symposium Digest*, pp. 1641–1644, 2001.

[20] F. Brauchler, J. Papapolymerou, J. East, and L. Katehi, "*W*-band monolithic multipliers," *IEEE MTT-S International Microwave Symposium Digest*, pp. 1641–1644, 1997.

[21] S.-W. Chen, T. C. Ho, K. Pande, and P. D. Rice, "Rigorous analysis and design of a high-performance 94 GHz MMIC doubler," *IEEE Trans. Microwave Theory and Tech.*, vol. 41, no. 12, pp. 2317–2322, December 1993.

[22] J. Papapolymerou, J. East, and L. Katehi, "A high power *W*-band monolithic FGC doubler," *IEEE Microwave and Guided Wave Letters*, vol. 10, pp. 195–197, May 2000.

[23] M. A. Frerking and J. R. East, "Novel heterojunction varactors," *Proceedings of the IEEE*, vol. 80, no. 11, pp. 1853–1860, November 1992.

[24] R. S. Muller and T. I. Kamins, *Device Electronics for Integrated Circuits*. New York: John Wiley and Sons, 2nd Edition, 1986.

[25] S. A. Maas, *Nonlinear Microwave and RF Circuits*. Boston: Artech House Publishers, 2003.

[26] S. M. Sze, *Physics of Semiconductor Devices*. New York: John Wiley and Sons, 2nd Edition, 1981.

[27] J. A. Calviello, J. L. Wallace, and P. R. Bie, "High performance GaAs quasi-planar varactors for millimeter waves," *IEEE Trans. Microwave Theory and Tech.*, vol. 21, no. 10, pp. 624–630, October 1974.

[28] J. A. Calviello, "Advanced devices and components for the millimeter and submillimeter systems," *IEEE Trans. Microwave Theory and Tech.*, vol. 26, no. 9, pp. 1273–1281, September 1979.

[29] W. Chen, "InP-based Quantum Tunneling Transistors Grown by Chemical Beam Epitaxy," Ph.D. dissertation, University of Michigan, Ann Arbor, MI, 1993.

[30] K. J. Herrick, "W-band Three-Dimensional Integrated Circuits Utilizing Silicon Micromachining," Ph.D. dissertation, University of Michigan, Ann Arbor, MI, 2000.

[31] K. Herrick, T. Schwarz, and L. Katehi, "*W*-band micromachined finite ground coplanar line circuit elements," *IEEE MTT-S International Microwave Symposium Digest*, pp. 269–271, 1997.

[32] J. Papapolymerou, F. Brauchler, J. East, and L. Katehi, "*W*-band finite ground coplanar monolithic multipliers," *IEEE Trans. Microwave Theory and Tech.*, vol. 47, no. 5, pp. 614–619, May 1999.

[33] K. C. Gupta, R. Garg, I. Bahl, and P. Bhartia, *Microstrip Lines and Slotlines*. Boston: Artech House Publishers, 1996.

[34] G. Ponchak, S. Robertson, F. Brauchler, J. East, and L. Katehi, "Finite width coplanar waveguide for microwave and millimeter wave integrated circuits," *ISHM Proc. International Symposium of Hybrid Microelectron*, pp. 517–521, October 1996.

[35] V. Ghione and C. U. Naldi, "Coplanar waveguides for MMIC applications : effect of upper shielding, conductor backing, finite-extent ground planes, and line-to-line coupling," *IEEE Trans. Microwave Theory and Tech.*, vol. 35, no. 3, pp. 260–266, March 1987.

[36] R. B. Marks and D. F. Williams, *De-embedding software*. National Institute of Standards and Technology (NIST), Boulder, CA: Program MultiCal, Version 1.00, 1995.

[37] J. East, E. Kollberg, and M. Frerking, "Performance limitations of varactor multipliers," *International Symposium on Terahertz Technology*, pp. 312–315, March 1993.

[38] J. East, "High frequency limitations of diode frequency multipliers," *International Symposium on Terahertz Technology*, pp. 116–124, 1996.

[39] G. Gonzalez, *Microwave Trnasistor Amplifiers Analysis and Desgin*. New Jersey: Prentice Hall, 2nd Edition, 1997.

[40] J. Papapolymerou, "MMIC passive and active Structures," Ph.D. dissertation, University of Michigan, Ann Arbor, MI, 1999.

[41] C. P. Wen, "Coplanar waveguide : a surface strip transmission line suitable for nonreciprocal gyromagnetic device applications," *IEEE Trans. Microwave Theory and Tech.*, vol. 17, pp. 1087–1090, 1969.

[42] T. Q. Ho and Y.-C. Shih, "Spectral-domain analysis of *E*-plane waveguide to microstrip transitions," *IEEE Trans. Microwave Theory and Tech.*, vol. 37, no. 2, pp. 388–392, February 1989.

[43] W. Grabherr, B. Huder, and W. Menzel, "Microstrip to waveguide transition compatible with mm-wave integrated circuits," *IEEE Trans. Microwave Theory and Tech.*, vol. 42, no. 9, pp. 1842–1843, Septmeber 1994.

[44] Y.-C. Shih, T.-N. Ton, and L. Q. Bui, "Wabeguide-to-microstrip transitions for millimeter-wave applications," *IEEE MTT-S International Microwave Symposium Digest*, pp. 473–475, 1988.

[45] S. C. Shi and J. Inatani, "A waveguide-to-microstrip transition with a DC/IF return path and an offset probe," *IEEE Trans. Microwave Theory and Tech.*, vol. 45, no. 3, pp. 442–446, March 1997.

[46] Y.-C. Leong and S. Weinreb, "Full band waveguide-to-microstrip probe transitions," *IEEE MTT-S International Microwave Symposium Digest*, pp. 1435–1438, 1999.

[47] C. Risacher, V. Vassilev, A. Pavolotsky, and V. Belitsky, "Waveguide-to-microstrip transition with integrated bias-T," *IEEE Microwave and Wireless Component Letters*, vol. 13, no. 7, pp. 262–264, July 2003.

[48] H.-W. Yao, A. Abdelmonem, J.-F. Liang, and K. A. Zaki, "A full wave analysis of microstrip-to-waveguide transitions," *IEEE MTT-S International Microwave Symposium Digest*, pp. 213–216, 1994.

[49] G. E. Ponchak and R. N. Simons, "A new rectangular waveguide to coplanar waveguide transition," *IEEE MTT-S International Microwave Symposium Digest*, pp. 491–492, 1990.

[50] W. Simon and M. Werthen and I. Wolff, "A novel coplanar transmission line to rectangular waveguide transition," *IEEE MTT-S International Microwave Symposium Digest*, pp. 257–260, 1998.

[51] N. Dib and A. Omar, "Analysis of grounded coplanar waveguide fed patches and waveguides," *IEEE MTT-S International Microwave Symposium Digest*, pp. 2530–2533, 1997.

[52] E. Tentzeris, M. Krumpholz, N. Dib, J.-G. Yook, and L. P. B. Katehi, "FDTD characterization of waveguide-probe structures," *IEEE Trans. Microwave Theory and Tech.*, vol. 46, no. 10, pp. 1452–1460, October 1998.

[53] (2003) Advanced Technical Materials, Inc. [Online]. Available: http://www.atmmicrowave.com/

[54] J. D. Jackson, *Classical Electrodynamics*. New York: John Wiley and Sons, 1962.

[55] F. J. Tischer, "Experimental Attenuation of Rectangular Waveguides at Millimeter Wavelengths ," *IEEE Trans. Microwave Theory and Tech.*, vol. 27, no. 1, pp. 31–37, January 1979.

[56] (2003) The MICROWAVE AMATEUR RADIO website. [Online]. Available: http://www.wa1mba.org/

[57] J. P. Becker, "Silicon Micromachined Waveguide Transition and Three-Dimensional Lithography for High Frequency Packaging," Ph.D. dissertation, University of Michigan, Ann Arbor, MI, 2001.

[58] H. Chan, private communication, 2003.

[59] (2003) Surface Technology Systems. [Online]. Available: http://www.stsystems.com/

[60] R. B. B. Gmbh, . U. S. Pat. 4855017 and U. S. Pat. 4784720 and Germany Pat. 4 241 045C1, 1994.

[61] M. J. Madou, *Fundamentals of Microfabrication, The Science of Miniaturization*. Boca Raton: CRC Press, 2nd Edition, 2002.

[62] L. Harle, "Microwave Micromachined Cavity Filters," Ph.D. dissertation, University of Michigan, Ann Arbor, MI, 2003.

[63] J. Bhardwaj, H. Ashraf, and A. McQuarrie, "Dry silicon etching for MEMS," *The Symposium on Microstructures and Microfabricated Systems at the Annual Meeting of the Electrochemical Society*, May 1997.

[64] G. T. A. Kovacs, N. I. Maluf, and K. E. Petersen, "Bulk micromachining of silicon," *Proceedings of the IEEE*, vol. 86, no. 6, pp. 1536–1551, August 1998.

[65] A. A. Ayón, R. Braff, C. C. Line, H. H. Sawin, and M. A. Schmidt, "Characterization of a time multiplexed inductively coupled plasma etcher," *Journal of the Electromechanical Society*, vol. 146, no. 1, pp. 339–349, January 1999.

[66] A. A. Ayón, X. Zhang, and R. Khanna, "Anisotropic silicon trenches 300-500 μm deep emplying time multiplexed deep etching (TMDE)," *Sensors and Actuators, A: Physical*, vol. 91, no. 3, pp. 381–385, July 2001.

[67] K.-S. Chen, A. A. Ayón, X. Zhang, and S. M. Spearing, "Effect of process parameters on the surface morphology and mechanical performance of silicon structures after deep reactive ion etching (DRIE)," *Journal of Micoelectricalmechanical Systems*, vol. 11, no. 3, pp. 264–275, June 2002.

[68] R. F. Harrington, *Time-Harmonic Electromagnetic Fields*. New York: McGraw-Hill, 1961.

[69] J. W. Digby, C. E. McIntosh, G. M. Parkhurst, B. M. Towlson, S. Hadjiloucas, J. W. Bowen, J. M. Chamberlain, R. D. Pollard, R. E. Miles, D. P. Steenson, L. S. Karatzas, N. J. Cronin, and S. R. Davies, "Fabrication and characterization of micromachined rectanguar wavegiude components for use at millimeter-wave and terahertz frequencies," *IEEE Trans. Microwave Theory and Tech.*, vol. 48, no. 8, pp. 1293–1302, August 2000.

[70] C. E. Collins, R. E. Miles, J. W. Digby, G. M. Parkhurst, R. D. Pollard, J. M. Chamberlain, D. P. Steenson, N. J. Cronin, S. R. Davies, and J. W. Bowen, "A new micromachined millimeter-wave and terahertz snap-together rectangular waveguide technology," *IEEE Microwave and Guided Wave Letters*, vol. 9, no. 2, pp. 63–65, February 1999.

[71] J. L. Hesler, K. Jui, R. K. Dahlstrom, R. M. Weikle, T. W. Crowe, C. M. Mann, and H. B. Wallace, "Analysis of an octagonal micromachined horn antenna for submillimeter-wave applications," *IEEE Trans. Antennas and Propagation*, vol. 49, no. 6, pp. 997–1001, June 2001.

[72] K. Hui, J. L. Hesler, D. S. Kurtz, W. L. Bishop, and T. W. Crowe, "A micromachined 585 GHz schottky mixer," *IEEE Microwave and Guided Wave Letters*, vol. 10, no. 9, pp. 374–376, September 2000.

[73] W. R. McGrath, C. Walker, M. Yap, and Y.-C. Tai, "Silion micromachined waveguides for millimeter-wave and submillimeter-wave frequencies," *IEEE Microwave and Guided Wave Letters*, vol. 3, no. 3, pp. 61–63, March 1993.

[74] T. W. Crowe, P. J. Koh, W. L. Bishop, C. M. .Mann, J. L. Hesler, R. M. W. II, P. A. D. Wood, and D. Matheson, "Inexpensive receiver components for millimeter and submillimeter wavelengths," *International Symposium on Terahertz Technology*, pp. 377–384, March 1997.

[75] J. P. Becker, J. R. East, and L. P. B. Katehi, "Performance of silicon micromachined waveguide at *W*-band," *Electronics Letters*, vol. 38, no. 13, pp. 638–639, June 2002.

[76] B. A. Shenouda, L. W. Pearson, and J. E. Harriss, "Etched-silicon micromachined *W*-band waveguides and horn antennas," *IEEE Trans. Microwave Theory and Tech.*, vol. 49, no. 4, pp. 724–727, April 2001.

[77] J. P. Becker, Y. Lee, J. R. East, and L. P. B. Katehi, "A finite ground coplanar line-to-silicon micromachined waveguide transition," *IEEE Trans. Microwave Theory and Tech.*, vol. 49, no. 10, p. 2001, October 2001.

[78] C. M. Mann, "Fabrication technologies for terahertz waveguide," *Proceedings of IEEE International Conference on Terahertz Electronics*, pp. 46–49, September 1998.

[79] V. M. Lubecke, K. Mizuno, and G. M. Rebeiz, "Micromachining for terahertz applications," *IEEE Trans. Microwave Theory and Tech.*, vol. 46, no. 11, pp. 1821–1831, November 1998.

[80] R. Williams, *Modern GaAs Processing Methods*. Boston: Artech House, 1990.

[81] M. J. Howes and D. V. Morgan, *Gallim Arsenide : Materials, Devices, and Circuits*. New York: John Wiley and Sons, 1985.

[82] K. J. Nordheden, X. D. Hua, Y. S. Lee, L. W. Yang, D. C. Streit, and H. C. Yen, "Smooth and anisotropic reactive ion etching of GaAs slot via holes for monolithic microwave integrated circuits using Cl_2/BCl_3/Ar plasmas," *Journal of Vacuum Science and Technology B*, vol. 17, no. 1, pp. 138–144, January/February 1999.

[83] B. Vanderelzen, private communication, 2003.

[84] D. A. Rowe and B. Y. Lao, "Numerical analysis of shielded coplanar waveguides," *IEEE Trans. Microwave Theory and Tech.*, vol. 31, no. 11, pp. 911–915, November 1983.