Three Dimensional Integration and Packaging Using Silicon Micromachining

by

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To my family

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CHAPTER 1

Introduction

1.1 Motivation

EMERGING needs in military and civilian high frequency applications have prompted researchers to investigate silicon micromachining as a novel and innovative way to achieve higher levels of three-dimensional integration, optimum RF performance, low-size and weight. Defense and national security have usually been the driving forces behind recent advantages in communication, radar and sensing systems. However, future solutions for military applications must address two new challenges: (a) offer compatibility to commercially available technologies as a cost saving measure and (b) offer increased flexibility to accommodate the rapid changes imposed by technology market forces. Silicon micromachining introduces a variety of technologies such as Microelectromechanical (MEMS) systems, on-wafer packaging, three-dimensional interconnects, cavity resonators and filters. The integration of all these enabling technologies can lead to miniature multi-functional systems that will include antennas, tuning mechanisms, filters, passive interconnects, and active components on a single chip. Such highly compact systems-on-a-chip can have an abundance of applications both for the military and the civilian market.

1.2 Silicon Micromachining

1.2.1 Physics of Silicon Semiconductors

From the early days of IC industry, silicon has been the substrate of choice. Its thermal and mechanical properties, along with its excellent electrical performance make Si the most appealing candidate for creating integrated circuitry. The maturity of surface and bulk silicon micromachining techniques gave silicon an additional advantage over other substrate materials. Understanding the physics behind silicon micromachining is necessary in order to correctly and fully utilize the superiority of this set of fabrication techniques.

Crystalline silicon forms a covalently bonded structure, the diamond-cubic structure, which has the same atomic arrangement as carbon in diamond form and belongs to the more general zinc-blend classification [1]. The lattice constant for Si is 5.4309 Å and its diamond-cubic lattice is surprisingly wide, with a packing density of 34% compared to 74% of the regular face-centered cubic lattice (fcc). The {111} planes present the highest packing density and the atoms are oriented in such a way that three bonds are below the plane. This explains why the {111} planes are virtually untouched by wet anisotropic etchants.

Silicon micromachining, the ability to fabricate microstructures on the surface or the interior of Si wafers is mainly based on <100> oriented wafers. It is well understood [2] that the intersections of the non-etching {111} planes with the {100} planes (e.g. the wafer surface) are mutually perpendicular and lying along the <110> orientations. Provided a mask opening is accurately aligned with the <100> orientation, which is set by the primary flat of the silicon wafer, only {111} planes will be introduced as sidewalls from the very beginning of the etch. Therefore during etching, truncated pyramids (via-holes) can become deeper, but never wider. After prolonged etching the {111} family of planes is exposed down to their common intersection and

the (100) bottom plane disappears creating a pyramidal pit. The slope of these sidewalls (Fig.1.1) is determined by the angle between the (111) sidewall and the (110) plane and is equal to 54.74^o. As a result of that the width of a rectangular or square cavity bottom plane, W_0, is completely defined by the etch depth, z, and the mask opening, W_m.

$$W_0 = W_m - 2\cot(54.74^o)z \tag{1.1}$$

or

$$W_0 = W_m - \sqrt{2}z \tag{1.2}$$

Vertical walls can also be etched in (100) oriented silicon wafers. If the mask opening is aligned to the <100> orientations (45^o angle with the wafer primary flat) the {100} planes are introduced as sidewalls. Since both the bottom and the sidewalls are from the same {100} group, lateral undercutting equals the vertical etch rate and therefore rectangular channels are created.

Other materials such as glass or ceramics, can be used as substrates at a much lower cost. However, non of these offer the capability to precisely fabricate extremely small features. For many years silicon has been the substrate of choice for the IC industry. The maturity of micromachining techniques, added to silicon's mechanical stability and good thermal properties, can provide a very appealing and profitable combination.

1.2.2 Wet Anisotropic Etching

Wet anisotropic etching is a low-cost, and very accurate method for bulk micromachining of silicon wafers. The etching has three major steps: (a) reactant transport to the surface; (b) surface reaction; and (c) reaction product transport away from the surface. If the rate determining factors are (a) and (c) etching is diffusion limited and

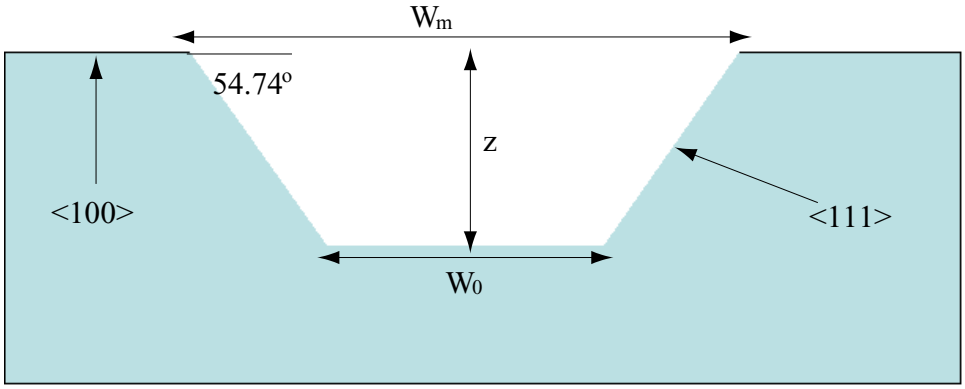


Figure 1.1: Anisotropically etched features in (100) oriented silicon wafers.

may be increased by stirring. If, on the other hand, (b) is the rate determining step, etching is reaction rate limited and depends strongly on temperature, etching material and solution composition [3]. Anisotropic etching, when performed properly, results in geometric shapes bounded by perfectly defined crystallographic planes. Additionally, contrary to isotropic wet etching, it offers excellent lateral dimension control. Unfortunately it is a relatively slow and high temperature process, and therefore appropriate masking techniques are necessary to protect the wafer. A wide variety of etchants have been used for anisotropic etching of silicon, including alkaline aqueous solutions of KOH, NaOH, TMAH, LiOH, CsOH, NH_4OH and quaternary amonium hydroxides, with the possible addition of alcohol. Alkaline organics such as ethylenediamine, choline or hydrazine with additives such as pyrocathecol and pyrazine are employed as well [4]. From the above the more commonly used anisotropic etchants are KOH and TMAH. Their etch rate is reaction rate controlled and therefore temperature dependent. These chemicals have differences in the etch rate of SiO_2 and the surface roughness that they create, thus, depending on the application, the appropriate solution is selected.

As will be analyzed in Chapter 4, where the issue of wet etching will be revisited, there are a lot of conflicting data in the literature on the anisotropic etch rates

of the various silicon crystal planes, especially the higher index ones. This is not too surprising, given the multiple parameters influencing individual results: temperature, stirring, size of etching features, solution concentration, addition of alcohol and other organic materials, surface defects etc. More rigorous experimentation and standardization will be necessary in order to better understand the influence of all these parameters to the etch rates. Nevertheless, several models attempting to explain the anisotropy in the etch rates of the different Si planes have been proposed [5, 6, 7, 8, 9].

1.2.3 Deep Reactive Ion Etching

Wet anisotropic etching is limited by the orientation of the silicon crystal planes. Fabricating smaller features with higher aspect ratios requires a more selective etching technique such as the Deep Reactive Ion Etching (DRIE). The dry anisotropic etching in this work is performed with the use of a Surface Technology Systems (STS) reactive ion etcher. For this system the etch process consists of a repeated cycling between successive etching and passivation steps, using two different gases (C_4F_8 for passivation and SF_6 for etching) and appropriate bias voltage in order to generate plasma. The geometric restrictions imposed by anisotropic wet etching are lifted in the case of DRIE. The sidewall profile departs from the normal by approximately 5^o, but it can be controlled to a great extend by judicious choice of such parameters as etching time, passivation time and RF power. The biggest drawback of DRIE however, is the roughness of the resulting sidewalls. Due to the time-multiplexed gas-feeding process, a horizontal scalloping of the sidewall occurs. This scalloping also varies with the material that is used for masking (hard mask or oxide), therefore an extensive characterization of the process is necessary in order to fully understand the influence that all these parameters have both on the etch profile and the roughness of the sidewalls.

Table 1.1: Packages for RF MEMS

Frequency band	DC-50 GHz for metal-to-metal,10GHz-W band for Capacitive
Insertion loss	<0.1 dB
Return loss	<-10 dB
Bonding Procedure	Low Temperature, Reduced outgassing
Sealing	Hermetic or near hermetic
Ambient	Nitrogen or non-reactive gasses
Materials	Thin film metals, SiO_2, Silicon nitride, no polysilicon

1.3 Packaging for RF MEMS Switches

In the last decade the maturity of surface and bulk micromachining enabled the development of Microelectromechanical systems (MEMS). In the RF area MEMS are mainly used as switches that utilize mechanical movement to achieve a short or an open circuit in a RF transmission line. While excellent performance has been reported for these devices, their operation is very sensitive to environmental factors, such as humidity and small particles. Therefore their integration to real-life systems can be problematic without a low-cost, low-loss hermetic package. Such a packaging scheme should follow some basic requirements, which are summarized in Table 1.1.

One of the major advantages of RF MEMS, compared to their solid state counterparts, is their low insertion loss. In order to retain this capability the total loss introduced by the package, excluding the losses of the feeding lines, should be kept below 0.1 dB, while the return loss should be below -10 dB at the frequency band of operation. In order to keep the loss below that limit the number of necessary interconnects in order to access the device should be kept at a minimum. Moreover use of wire or ribbon bonds should be avoided due to the parasitic inductance that they add.

Regarding the bandwidth of the package two alternatives exist. One it to create a broadband design, allowing the use of one design for different types of switches (metal-

to-metal or capacitive). The second approach is to intensionally introduce resonances in the response, thus achieving excellent performance in a narrower frequency band. The RF transition to the MEMS can be done either using via-holes or by passing the lines directly under the sealing ring. The second approach, although easier to fabricate, offers lower RF and hermeticity performance. The reason is that the feeding line needs to be embedded in some type of dielectric (SiO_2 or BCB) in order to isolate it from the sealing ring. This changes the characteristic impedance of the interconnect and therefore appropriate matching networks need to be introduced. Furthermore, the isolation layer is deposited over the printed interconnect, which is a 2-3 μm thick microstrip or FGC line. This means that the final structure might not be planar and step coverage could create microcracks on the layer. Clearly more research is needed for this type of RF connection to a MEMS device in order to evaluate both its RF performance and long-term hermeticity.

MEMS accelerometers and gyroscopes are been fabricated using thick polysilicon layers which can withstand very high post-processing temperatures. In contrast, RF MEMS are usually created out of thin film metal membranes (thickness: 0.5-2 μm, length: 250-350 μm) suspended a few μm over the substrate. Such a released structure is extremely sensitive to both bonding temperatures and outgassing and therefore not all available sealing techniques are applicable. Currently several technologies are been proposed for packaging of RF MEMS such as epoxy seal, metal-to-metal solder bonding, silicon-glass eutectic using localized heating, gold-gold thermocompression bonding, LPCVD sealing, and surface activated bonding. Low-temperature bonding techniques need to be thoroughly investigated in order to provide a reliable method for sealing RF MEMS.

Finally, in contrast to other MEMS structures RF MEMS need to be packaged in an ambient of nitrogen or other non-reactive gas. This is due to the fact that the gas will act as a damping mechanism for the structure resulting in a low mechanical Q

Table 1.2: Commercially available RF packages.

Company	Alpha	HEI	Shinco	Stratedge	MCS
Material	Alumina Ceramic	Laminate Substrate	Ceramic	Alumina Ceramic	Alumina
Intercon.	3-via cpw, wirebonds, flip-chip	3-via cpw, wirebonds, flip-chip	3-via cpw, wirebonds, flip-chip	3-via cpw, wirebonds, flip-chip	Bump Grid Array
IL(dB)[a]	0.6dB at 20 GHz	1 dB at 46 GHz	n/a	0.6 dB at 45 GHz [b]	1dB at 31.5 GHz
RL(dB)	10 dB at 24 GHz	15 dB at 46 GHz	n/a	18 dB at 45 GHz	20dB at 31.5 GHz
Hermet.	n/a	No	Yes	Near	n/a
Ambient	Air	Air	n/a	Air	Air

[a]Measurements are performed on different materials, different line lengths, and different metal thicknesses therefore are not comparable.

[b]Measurements for this package were performed on a single (not back-to-back) transition.

value and thus increase the reliability of the MEMS. In addition to that, a pressure equilibrium between the inside of the package and the outside environment will make it even more difficult for humidity to flow inside of the package, in the case where a leak channel is present.

Significant work has already been done in RF packages for use with solid state amplifiers, diodes or filters. Some of the available packages are summarized in Tables 1.2 and 1.3. These packages are been offered in a variety of configurations with wide bandwidth of operation and are mainly non-hermetic. Unfortunately, as was mentioned in the previous paragraphs, these packages are not applicable for RF MEMS. Some available packages for MEMS are mentioned in Table 1.4. Many more companies and laboratories are working in this area. However, in most cases, this is research currently under investigation and therefore intellectual properties and trade secrets significantly reduce the available information.

This thesis will present the first published on-wafer packaging scheme for RF MEMS switches for operation up to 40 GHz and beyond. The deembeded measured

Table 1.3: Commercially available RF packages (cont.).

Company	UMS	Gergia Tech	Alcatel	FBH/EADS	Northrop Grumman
Material	Alumina Ceramic	LTCC	HTCC	Si/BCB	LTCC
Intercon.	3-via cpw, wirebonds, flip-chip	3-via cpw, flip-chip	microstrip, ribbon bonds	3-via cpw, wirebonds, flip-chip	3-via cpw, flip-chip
IL(dB)[a]	1 dB at 46 GHz	3 dB at 12 GHz	1.5 dB at 40 GHz	0.6 dB at 30 GHz	n/a
RL(dB)	15 dB at 46 GHz	10 dB at 12 GHz	27 dB at 40 GHz	25dB at 45 GHz	n/a
Hermet.	No	n/a	Yes	N0	n/a
Ambient	Air	n/a	n/a	n/a	n/a

[a]Measurements are performed on different materials, different line lengths, and different metal thicknesses therefore are not comparable.

insertion loss of the transition is 0.06 dB and according to the publicly available data this is the lowest reported loss for any MEMS package. The measured return loss is below -18 dB up to 40 GHz. In compliance with the information summarized in Table 1.1 the RF performance is well within the limits set by the MEMS device. The transition to the device is done through via-holes etched in silicon, meaning that the sealing ring and the feeding lines do not intersect. Its fabrication process is based on standard micromachining techniques and therefore the same architecture can be used with a variety of RF MEMS structures. Additionally, keeping the sealing ring and the feed lines separate provides unprecedented flexibility on the bonding technique used. The only limitation set by the architecture is that the temperature can not go beyond 400^o C since that severely deforms the Au plated lines. However, as was mentioned previously, RF MEMS are also fabricated by thin film metals such as gold or nickel and therefore any temperature above 400^o C will severely deteriorate the MEMS performance as well.

In addition to the aforementioned properties the packaging architecture presented

Table 1.4: MEMS Packages.

Company	Use	Material	Sealing	Hermet.	Ambient
Michigan Prof.Najafi	Resonators	Si/Glass/Si	Localized Heating	Yes	Air
Michigan Prof.Najafi	Resonators	Ni	Thin Films	Yes	Vacuum
Michigan Prof.Wise	Resonators	Si/Glass	LPCVD	Yes	Silane
Berkeley Prof.Lin	Resonators	Si/Glass	Rapid Thermal	Yes	Air
Berkeley Prof.Lin	Resonators	Si/PSG/ SiNi	LPCVD	Yes	Vacuum
Omron	RF<2GHz	Glass	Glass Frit	Yes	n/a
IMEC vzw	RF IL 0.7 dB, RL 22 dB at 40 GHz	Si/ BCB/ AF45	BCB epoxy CPW under seal	No	n/a
IMEC vzw	RF	Solder	Indent Reflow	Yes	n/a
Rockwell	Resonators	SOI Si	Epoxy	Yes	Liquid
Raytheon	Resonators	Si	Thermo-compression	Yes	Vacuum
Lockheed Martin	RF	Si/GaAs/ Polyimide	Stage B epoxy	No	n/a
Tokyo Univ.	Resonators	Si	Surface Activated	Yes	Vacuum

in this thesis is fabricated on the same wafer as the RF MEMS, thus reducing the number of necessary interconnects to a minimum. This topic will be revisited in Chapter 6 where the advantages of this on-wafer approach will be analyzed in detail. Even though the design is compatible with multiple sealing techniques thermocompression bonding is selected. The RF MEMS is hermetically packaged in an ambient of nitrogen. Accelerated tests demonstrated that the mean time to failure of the package is over 200 years in "tropical" conditions.

1.4 Simulation Techniques

High performance electromagnetic simulation tools have been extensively used in this thesis for design and characterization of silicon micromachined components. Since the majority of the investigated structures are three-dimensional in nature High Frequency Structure Simulator (HFSS) [10] is broadly utilized for analyzing vertical transitions, filters and packages. This software allows the user to design arbitrary three-dimensional structures composed of various materials and to excite them with an appropriate electromagnetic source. The architecture is then solved using an adaptive meshing procedure and Finite Element Method (FEM) to provide the electric and magnetics field within the problem region. By post-processing these field values the user can extract the S-parameters, ϵ_{eff}, characteristic impedance of the interconnects, and many other parameters of interest. A two-dimensional FEM solver [11] has also been used for portions of this thesis,mainly for estimating input impedances of various transmission lines.

Planar structures have been analyzed using Method of Moments (MOM) based solvers [12, 13]. MOM relies in solving for the electric current on the structures, instead of the electric field, and is therefore more efficient for two dimensional problems. Additionally, for simulating lumped components and distributed elements Agilent Advanced Design System (ADS) has been used [14].

1.5 Fabrication Facilities

Extensive fabrication is necessary for the completion of this thesis. Most of the experimental work involved is carried out in the Solid State Electronics Laboratory (SSEL) of the University of Michigan. This is a $25 million facility funded by state support and fees generated by industry and academic usage. Central to solid-state electronics research is the microelectronics processing facility. This laboratory, which

is housed in 6000 sq. ft. of class 1000, class 100, and class 10 clean space, is equipped with state-of-the-art tools for materials preparation and characterization with in-situ diagnostics, epitaxial growth, device fabrication with feature sizes smaller than 0.1 μm, and device characterization. The entire facility, is used by over one hundred students and researchers and is managed and maintained by a well-qualified staff. The lab contains all of the major pieces of processing equipment needed to build the components presented in this study. These include mask making, front and back-side photolithography, furnace oxidation systems, dry pattern transfer (plasma, RIE), ion-beam deposition and milling, vacuum evaporation and sputtering, chemical vapor deposition, and bonding.

Additional fabrication steps such as anisotropic wet etching (KOH and TMAH), electroplating, and supercritical CO_2 drying of MEMS devices is performed at the fabrication facilities of the Radiation Laboratory, at the University of Michigan. Finally, for the first part of this thesis, some microwave lines are printed using a milling machine located at the same laboratory.

1.6 Measurement Techniques

The high frequency circuit measurements presented in this thesis are acquired using a HP 8510C Vector Network Analyzer connected to an Alessi probe station. A photograph of the measurement set up is presented in Fig.1.2. For 2-40 GHz measurements the system consists of a HP8350B sweep oscillator connected to a HP8516A S-parameter test set. Model 40A GGB picoprobes are used for on-wafer measurements. For W-band measurements a HP W85104A millimeter-wave test set is supplying signals though WR-10 waveguides and model 120A-BT GGB picoprobes. For all calibrations the Though-Reflect-Line (TRL) method is used with on-wafer calibrations standards fabricated in conjunction with the circuits to be tested. Multical,

developed by NIST, is used to implement the TRL calibration [15]. For the hermeticity tests the reliability testing facilities of the Wireless Integrated Microsystems (WIMS) Center at the University of Michigan are used.

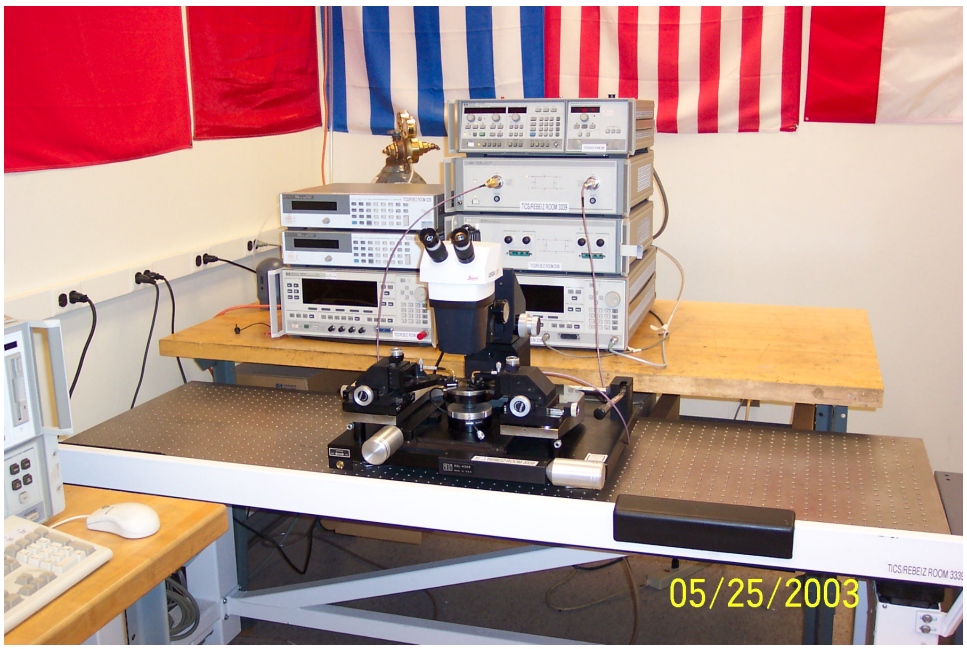


Figure 1.2: Measurement set-up.

1.7 Dissertation Overview

This thesis explores the development of a low-loss, on-wafer package for RF MEMS switches. The use of silicon micromachining and novel photolithographic processing are also investigated to further the case of silicon-based microwave and millimeter wave circuitry.

Chapter 2 examines the problem of cross-talk between adjoining interconnects printed on the same wafer. X and W-band circuits will be theoretically and experimentally investigated, along with the effects of open-end discontinuities, vias printed in close proximity to RF lines, and parasitic fields launched from vertical transitions.

Chapter 3 is devoted to the design and fabrication of low-loss interconnects on low-

resistivity silicon wafers. The purpose of this investigation is to research the possibility of creating high performance lines on low-quality silicon using intermediate polyimide layers micromachined using reactive ion etching. Both theoretical and experimental results will be presented.

Chapter 4 analyzes evanescent mode resonators and filters designed for micromachined silicon wafers. These filters have excellent performance, minute size and are easily integrated with other planar circuits, thus making them very attractive for system-on-a-chip configurations.

Chapter 5 explores the possibility of creating an on-wafer packaging scheme for RF MEMS switches utilizing silicon micromachining. The design and fabrication process for a low insertion loss RF transition will be analyzed in detail along with the measured response of the packaged RF MEMS. Moreover, the use of electrodeposited photoresist for creating multilevel transmission lines will be investigated.

Chapter 6 provides a brief overview of the importance of hermetic packaging along with some details related to reliability metrology and accelerated testing. It concludes with the presentation of the hermeticity tests for the on-wafer packaging scheme developed in this thesis.

Chapter 7 summarizes the accomplishments detailed in this dissertation, illustrates other potential applications of evanescent mode filters, summarizes some potential MEMS tuning mechanisms and introduces the extensive reliability tests to be undertaken for evaluating the hermeticity and durability of the on-wafer package.

CHAPTER 2

Isolation in Three Dimensional Integrated Circuits

2.1 Introduction

WITH ever increasing demands to produce high-density microwave modules, achieving adequate isolation between circuit elements becomes more difficult. This is a particular concern for transceiver applications where high isolation is necessary to ensure receiver sensitivity and prevent leakage between channels. Multi-layer architectures incorporating complex circuits in a common substrate material pose the most challenging isolation problem. When circuits are printed on a common substrate, surface waves excited by planar discontinuities or leaky modes tend to induce parasitic currents on neighboring interconnects and circuits leading to unwanted interference. This parasitic coupling becomes increasingly more problematic as circuits are printed on multi-layered structures for higher density and smaller size. In such structures, proximity effects are dependent on interconnect geometry. Appropriate layout design and relative placement of lines, vias, and vertical transitions is necessary in order to reduce any unwanted interference. It is the purpose of this study to identify the limits imposed in isolation by three-dimensional integration and on-wafer packaging, utilizing silicon micromachining.

As microstrip was the prevalent transmission line in the early 80's investigation

of microstrip-to-microstrip crosstalk and electromagnetic coupling became a critical issue for design and simulation of MMICs [16]. The inaccuracies between the theoretical results and the measured data observed initiated an extensive study of crosstalk using various analytical tools and employing both quasi-static approximations and full-wave solvers. Spectral domain methods are used at [17, 18, 19] where the surface waves are related with the presence of poles in the spectral Green's function associated with the problem. The parasitic cross-talk between various line configurations has also been addressed using the Method of Moments [20], along with Finite Element Method [21] and Finite Difference Time Domain method [22]. In addition, for the same problem, potential and induced EMF methods have been utilized in [23] and the GCM (Generalized Coupling Model) has been used by Swanson [24]. The results of the aforementioned studies are consistent and are corroborated by the present study.

Crosstalk between adjoining interconnects is caused by a variety of mechanisms. Thus, when the distance between the lines is small compared to a dielectric wavelength, the predominant reason for decreased isolation is near-field coupling due to open-end effects and discontinuities. However, when the separation between interconnects increases, the coupling occurs due to the surface waves (TM_0 or TE_0) propagating inside the dielectric substrate. Such modes can be excited by discontinuities but can also be launched by leaky dominant modes. Published studies [17, 18] show that a leaky dominant mode is present at higher frequencies on conventional microstrip lines printed on an isotropic substrate. This mode has a leakage into the TM_0 surface wave and exists independently of and in addition to the usual dominant mode. An important observation is that near the strip the leaky mode has a field distribution that closely resembles that of the bound mode. Therefore, both modes can be excited by conventional microstrip feeds. The critical frequency where the leakage onset occurs is reported to be as low as a few gigahertz depending on the substrate characteristics (thickness and dielectric constant). This leaky mode may interact with other lines or

components in the microstrip package, thus accounting for an increase in crosstalk. As seen in [17, 18], reduction of the thickness and dielectric constant of the substrate can decrease the leakage effects either by moving the critical frequency out of the band of operation or by diminishing the leakage constant. Both can be achieved by local reduction of the substrate thickness. Silicon micromachining with wet etching (potassium hydroxide or tetramethyl amonium hydroxide) can be utilized to create small cavities under the microstrip lines.

The coplanar waveguide, proposed by Wen in 1969, consists of two slots printed on a dielectric substrate. Its principal advantage is that it is well suited for use with field effect transistors, especially at mm-wave frequencies where RF grounding must be close to the device. Via-holes are not necessary for ground equalization and fragile semiconductors need not be made excessively thin. As shown in [25], the loss and dispersion of the CPW are comparable and in some cases better than the ones exhibited by the microstrip lines. For an infinite ground plane the lowest order surface wave mode is the TM_0 and at the frequency where the phase velocity of the surface wave becomes equal or smaller than the velocity of the CPW mode highly dispersion behavior is observed. For conventional substrate thickness between 100 μm and 500 μm this frequency is of the order of hundreds of GHz. However, this is true only for infinite architectures (substrate and interconnects) and straight lines, without any bends or discontinuities. In a realistic structure multiple lines of finite length are printed on a common substrate of finite dimensions [26]. Additionally, these structures are usually packaged including backside metallization, top and/or side metallic walls. The finite dimension of the interconnects, along with the packaging effects can change the leakage properties of the lines significantly and can cause leakage to occur at much lower frequencies than expected [27, 28].

The finite ground coplanar waveguide (FGC) has an additional major advantage in its ability to suppress parasitic modes. If symmetry around the center conductor is

maintained or airbridges are used to equalize the potential on the two ground planes, the coupled slotline mode is eliminated. Reducing the total width of the line bellow $\lambda_g/2$ can move the cut-off frequency out of the band of operation, thus suppressing all higher order modes. Therefore, the FGC line does not require vias for ground equalization, and its propagation characteristics are not sensitive to the substrate thickness and presence of backside metallization. Moreover, the finite ground CPW has lower leakage constant compared with the infinite CPW [19]. In the case of the FGC line the lowest surface wave mode is the TE_0 and therefore leakage occurs at higher frequencies compared to the infinite ground plane CPW line. Tsuji in [19] also illustrates that the reduction of the ground plane width can significantly reduce the leakage constant. A similar observation is made in [29] where the reduction of the ground plane width increased the isolation between two FGC lines. This similarity reveals the strong relationship among the leaky modes and the crosstalk between lines.

According to previous results the onset of leaky modes occurs at much higher frequencies for the FGC line compared with the microstrip line and therefore FGC lines provide a wider single-mode frequency range of operation [18, 19]. Moreover, the FGC line has less field overlap with the surface wave modes than microstrip, and interacts weakly with them [30]. As is illustrated in this reference the coplanar waveguide field overlaps depend strongly on the value of the total width of the line. In this respect the main difference between the two types of interconnects is the degree of freedom in their physical layouts. On a given substrate the microstrip has two degrees of freedom: line width and substrate thickness. Changing both of these, while keeping the line impedance constant, does not change the field overlaps. In contrast, the total width of the CPW (ground plane, slot and line width) can be varied independently of line impedance in order to minimize the field overlap with surface wave modes. After examining all the aforementioned theoretical and experimental results it is expected

that the FGC line will demonstrate better isolation as compared to a microstrip line. Consequently, the following study will focus on FGC interconnects and their behavior.

Details of this study are presented in the subsequent sections. The design and fabrication process for the X and W-band structures is described first, followed by the results for single and multi-layer architectures. The chapter proceeds with the investigation of open-end effects, along with the deterioration in isolation caused by the existence of vias in close proximity to interconnects. Finally, it has been shown [31] that vertical transitions may launch parasitic fields, which couple to adjoining lines and result in increased coupling, if designed improperly. The understanding of these effects on coupling and the required separation to achieve desired isolation is investigated in this research. The outcome of this investigation, as presented in [32], is the creation of an extensive list of three dimensional interconnect architectures and their respective isolation. These results, mainly theoretical in nature, are focused on two frequencies 8 and 32 GHz, since these are the Deep Space frequency bands used by JPL. This chapter describes the experimental and a few of the theoretical results that are acquired. Appendix A is a comprehensive list of all the analyzed architectures.

2.2 Design of Isolation Architectures

In view of the above, this study addresses coupling in multi-layer circuits with microstrip or coplanar waveguide as the underlying interconnect. The circuits under study are designed for X-band (8-12 GHz) as well as W-band (75-110 GHz), and thus different substrates are used. The X-band circuits are fabricated on 1.524 mm thick Duroid with dielectric constant (ϵ) of 2.92. The W-band circuits are fabricated on high-resistivity 100 μm thick silicon with dielectric constant of 11.7. High resistivity silicon wafers with resistivity of 2500 Ω-cm, measured by a four point probe, are used

in order to reduce the losses. Due to the high design frequency of 94 GHz the losses are a major factor in the performance of the circuits. A static 2-D electromagnetic solver is used to design a 50 Ω line for each substrate and line type (Duroid or silicon, microstrip or FGC) [11]. All FGC X-band transmission lines are of dimensions 1520-380-2540 μm (center conductor-aperture-ground), while all microstrip X-band transmission lines presented are of dimensions 2540-7620 μm (signal conductor-ground plane). In W-band, only FGC lines are examined of dimensions 40-24-106 μm (center conductor-aperture-ground).

An efficient tool for analyzing coupling structures should allow analysis of three dimensional topologies with vertical transitions [16] and it should account for frequency dependent effects such as dispersion, radiation, and higher-order mode propagation. All the simulation results presented in this study are obtained with HFSS, which has all of the above characteristics [10]. The structures are analyzed including conductor and dielectric losses and are surrounded by a radiation boundary, which absorbs all the incident fields simulating a free-space environment. However, the fabricated circuits have always finite dimensions and some reflections are bound to happen at the edges of the wafer due to the air-dielectric interface. These reflected fields can couple back to the lines giving slightly different measured data. Nevertheless the simulations performed with this type of modelling gave results that very closely approximate the measurements in the majority of the cases.

2.3 Fabrication of Isolation Structures

2.3.1 X-band Designs

The X-band circuits are fabricated on Rogers Duroid (ϵ=2.94, thickness:1.524 mm) with the use of a milling machine. The interconnects are milled on separate wafers which are then bonded together in order to create the multilayered structures. Cavi-

ties and vias for the vertical transitions have been drilled in the dielectric substrate using appropriate milling tools. SMA connectors are soldered at the one end of each line, leaving the other open. This creates a standing wave, which, as will be shown shortly, increases the coupling by 6 dB if compared to a matched line.

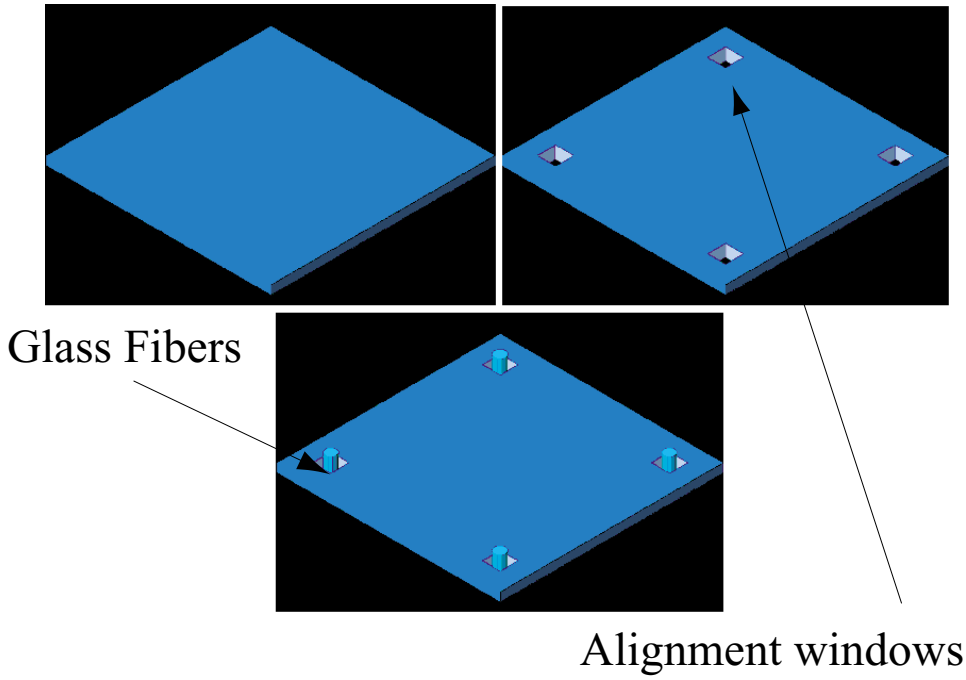


Figure 2.1: Alignment of silicon wafers using glass fibers.

2.3.2 W-band Designs

The W-band circuits are printed on 100 μm thick high-resistivity double-side polished silicon wafers with 6600 Å SiO_2 on both sides. Three wafers are used for the packaged isolation study and are fabricated separately. The four main fabrication steps are thin film resistor deposition, circuit metallization, aperture definition, and anisotropic wet etching of the protective air cavities and probe windows.

For the thin film resistors used on one of three wafers, 700 Å of TaN is deposited using a lift-off process. This thickness results in a sheet resistance of 43 Ω/square based on a four point probe measurement. A lift-off process is also used for the cir-

cuit metallization of Cr/Au (500/9500 Å), and silicon dioxide is patterned to define cavities and probe windows. The silicon dioxide is etched partially or fully in buffered hydrofluoric acid (BHF) at the rate of 1000 Å/min. The final step is to anisotropically etch the oxide-patterned cavities and probe windows in potassium hydroxide (KOH) at an etch rate of 30 Å/hour. Multiple probe windows are opened during the anisotropic etching through both wafers. Glass fibers are inserted through the windows in order to align the samples. The process is performed using an optical microscope and the expected error is of the order of 10-15 μm (Fig. 2.1). The wafers are then bonded together using silver epoxy which is deposited in small quantities at the wafer edges and cured at 150° C. Since the epoxy bumps are on the edges of the wafers, far from any measured circuit, they can not affect the measured coupling.

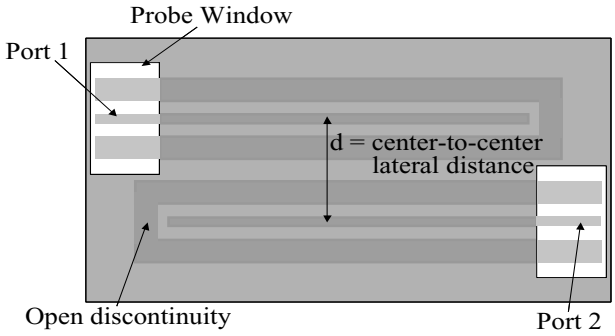
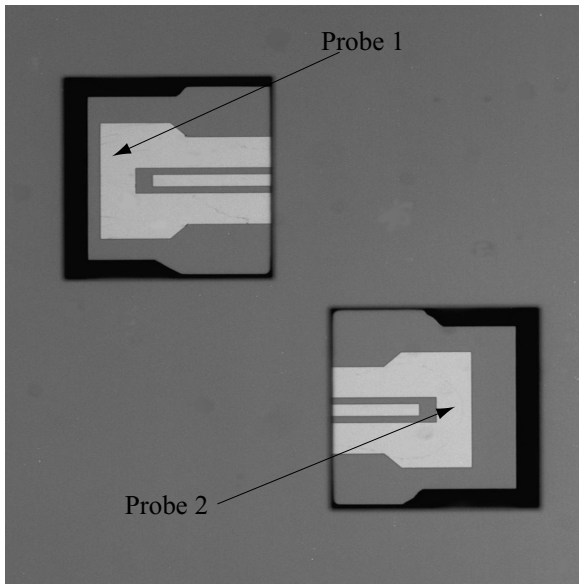


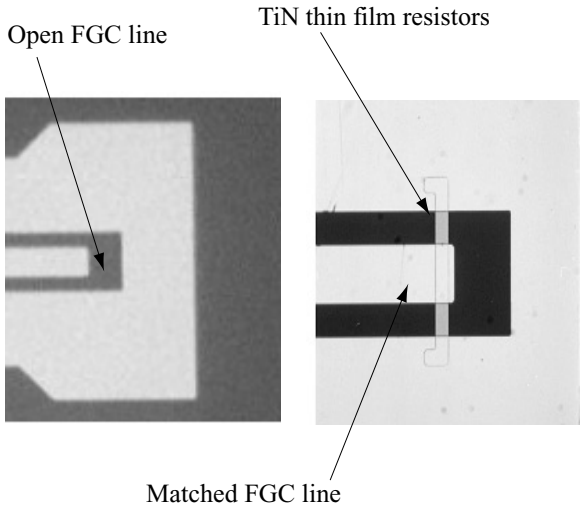
Figure 2.2: Schematic for laterally separated FGC lines showing center-to-center separation and location of probe windows.

2.4 Theoretical and Experimental Results

Two different types of measurement set-ups are used in order to measure the various designs. For the X-band measurements SMA connectors are soldered to the interconnects and then connected to an HP 8722D vector network analyzer via 3.5 mm coaxial cables. Short-Open-Load-Through (SOLT) calibration is performed from 6 to 12 GHz using standard 3.5 mm coaxial calibration standards.



(a)



(b)

Figure 2.3: W-band circuits. (a) Packaged FGC lines printed on a 100 μm silicon wafer. (b) Detailed view of open and matched FGC line terminations.

For the W-band measurements, a HP 8510C vector network analyzer is utilized on an Alessi probe station with 100 μm pitch GGB picoprobes. Through-Reflect-Line (TRL) calibration is performed using on-wafer calibration standards fabricated in conjunction with the circuits to be tested. Multical, developed by NIST is used to implement the TRL calibration [15]. Prior to the measurements all the samples are mounted on 1 mm thick glass slides using photoresist. This is done in order

to provide structural protection to the samples during the measurements and also to ensure that the coupling measured is not affected by the metallic base of the probe station. For both frequency bands the coupling between the lines is taken as the insertion loss between the two inputs leaving the other two open as seen in Fig. 2.2. A basic limitation to all the measurements presented is the undesired signal coupling, which is generated by two independent mechanisms: free-space parasitic radiation and substrate radiation. The former couples the probes when they are in non-contact position and separated by a distance equal to the distance between the two neighboring interconnects. The latter is due to surface waves that are excited in the substrate from the probes as they contact the surface of the layer. The noise floor for the X-band measurements was approximately -60 dB and for the W-band -50 dB.

2.4.1 Single-layer Isolation

Parallel interconnect lines patterned on the same lateral plane are a very common configuration in the majority of MMICs. Usually the lines are connecting various active or passive components and therefore they are matched reducing any undesired reflections and achieving maximum power transfer. Thus, no standing wave is generated on the line due to open-end effects. Parallel FGC lines (both open and matched) fabricated on 100 μm high resistivity silicon wafers are showed in Fig. 2.3. The distance between the center conductors is varied from 450 to 1100 μm (the dielectric wavelength at 94 GHz is 930 μm). The results for the average isolation over the respective frequency band are shown in Fig. 2.4 where measured and numerical results are presented. The measurements are consistent with the simulated results down to the noise floor, and illustrate the superior isolation of FGC lines of better than -45 dB for center-to-center distances larger than 800 μm . The second important observation indicated by the same graph is the fact that the open and matched FGCs differ by 6 dB, as theoretically expected, due to the existence of the standing wave in the open

lines.

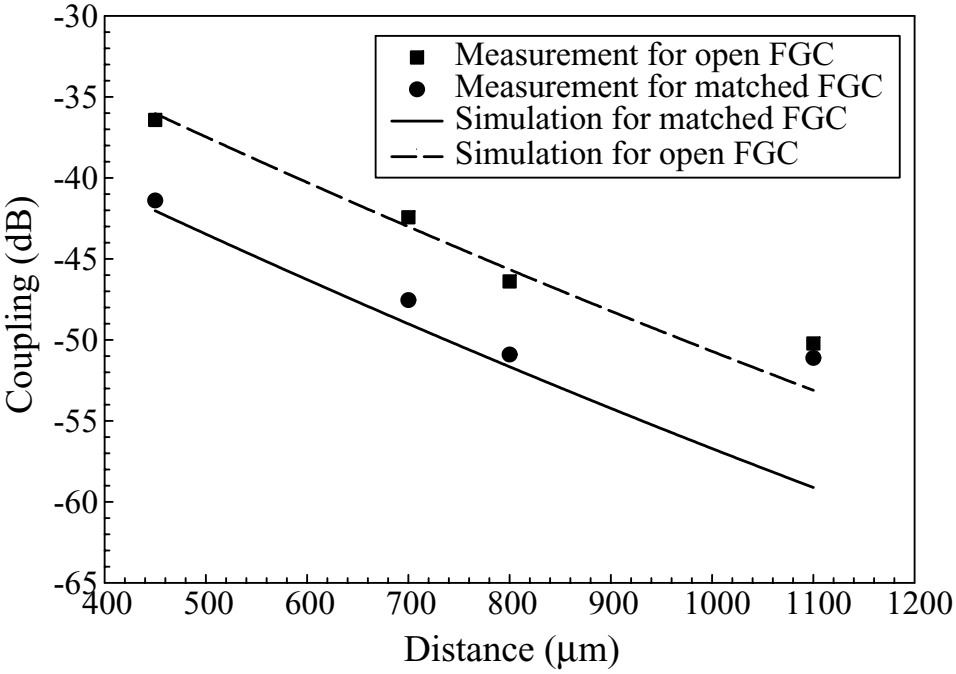


Figure 2.4: W-band measured and numerical results for laterally separated FGC lines showing coupling versus center-to-center spacing.

2.4.2 Multi-layer Isolation

Parallel Architectures

A multilayer environment can include parallel lines printed in close proximity on two vertically separated planes. Both X and W-band measurements and simulations are performed for this configuration. The fabricated X-band structure consists of a combination of a microstrip and an FGC line printed on Duroid (thickness:1.524 mm) with a lateral separation varied from 0 to 25.4 mm. The results for the average coupling are shown in Fig. 2.5 where the agreement between theory and measurements degrades as the distance becomes large and the coupling is comparable to the noise floor. Note that when the two lines are exactly on top of each other the isolation between them is -15 dB, but when the distance approaches one wavelength (21 mm)

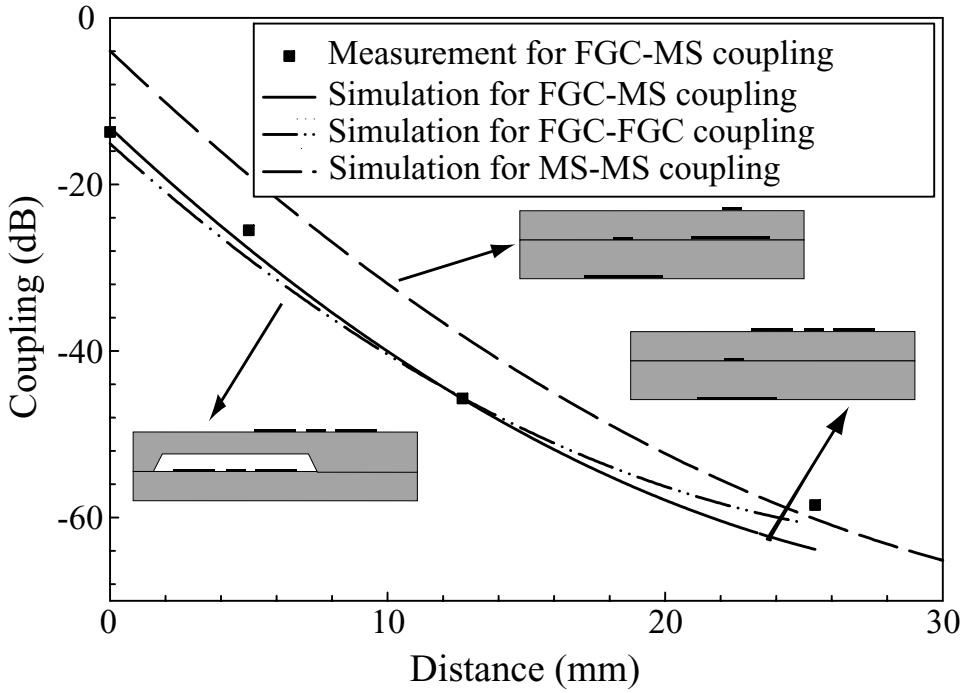


Figure 2.5: X-band measured and numerical results for vertically separated FGC and microstrip lines showing coupling versus center-to-center spacing.

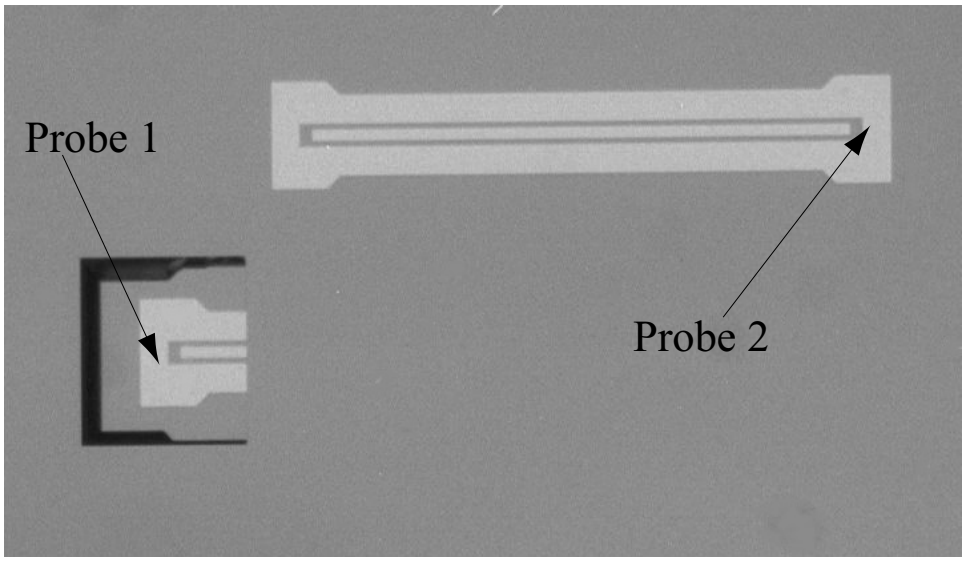


Figure 2.6: W-band FGC lines printed on two 100 μm silicon wafers.

the coupling reduces to -60 dB. Simulated results for microstrip-to-microstrip and FGC-to-FGC lines are included on the same graph. In agreement with the theory

presented in [19], the FGC offers better isolation compared to the microstrip by a factor of 8 dB. However, the combination of microstrip and FGC line offers an isolation which is comparable to the FGC-FGC structure for distances up to 12 mm. These two different types of lines propagate modes which are orthogonal to each other, hence when they are printed in close proximity their fields couple very weakly. When the distance between the lines is expanded the fields leak to the lower substrate mode, which thus becomes the main mechanism that causes increased crosstalk. Therefore, the use of the microstrip-FGC combination could be an alternative design if the use of microstrip lines in a specific circuit is unavoidable.

Parallel W-band FGC lines are fabricated on two 100 μm high resistivity silicon wafers, which are bonded together using silver epoxy. The center-to-center distance is varied from 0 to 1100 μm and the circuits are shown in Fig. 2.6. Measured and simulation results for average coupling over the respective frequency band are shown in Fig. 2.7, where again there is a consistency between simulation and measurements. When the lines are exactly on top of each other, the isolation between them is -19 dB; when the distance approaches one wavelength (930 μm), the isolation increases to -49 dB. In the initial configuration, when the two FGC lines are perfectly aligned and the center-to-center distance is zero, the measured response displays a 10 dB ripple over the frequency of interest. This is attributed to a parallel plate mode that is excited due to the close proximity of the two ground planes. This ripple is significantly reduced as the lines are separated resulting in a 5 dB ripple at 400 μm distance and a 2 dB ripple at 800 μm. The results summarized in Fig. 2.7 correspond to the ripple peak. This ripple is expected to be lower if the two lines are matched, however such a placement of two parallel FGC lines should be avoided if high isolation is needed.

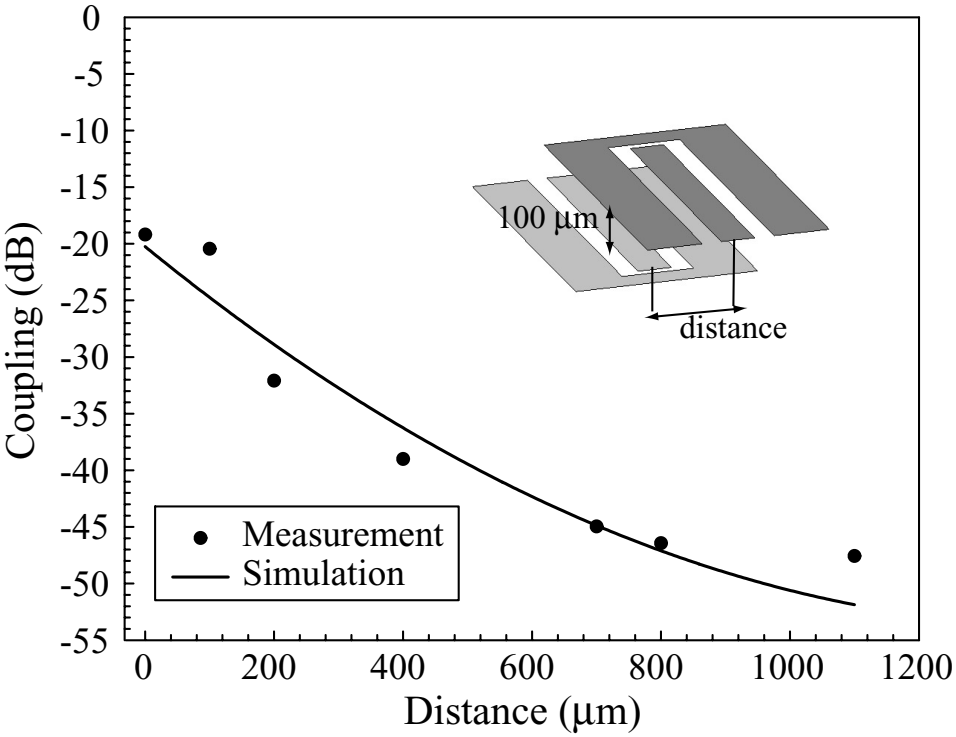


Figure 2.7: W-band measured and numerical results for vertically separated FGC lines showing coupling versus center-to-center spacing.

Perpendicular Architectures

In order to investigate the effects of the vertical separation to various FGC lines configurations multiple simulations for X-band structures are performed. The lines are design to be 50 Ω (106-24-40 μm) printed on 100 μm silicon wafers. A set of parallel and a set of perpendicular FGC lines are analyzed at 8 GHz and the results are displayed in Fig. 2.8 along with the schematics of the two structures, where the dielectric and the cavities have been omitted for illustration purposes. As expected the perpendicular lines offer much better isolation (always better than -55 dB) since the interaction of the two lines is restricted to the cross-over area. This is not the case in the parallel FGC lines where the coupling is -26 dB for 100 μm of vertical distance and is decreased to -35 dB at 500 μm. Therefore, when designing for high isolation in multilayered structures perpendicular FGC lines should be considered.

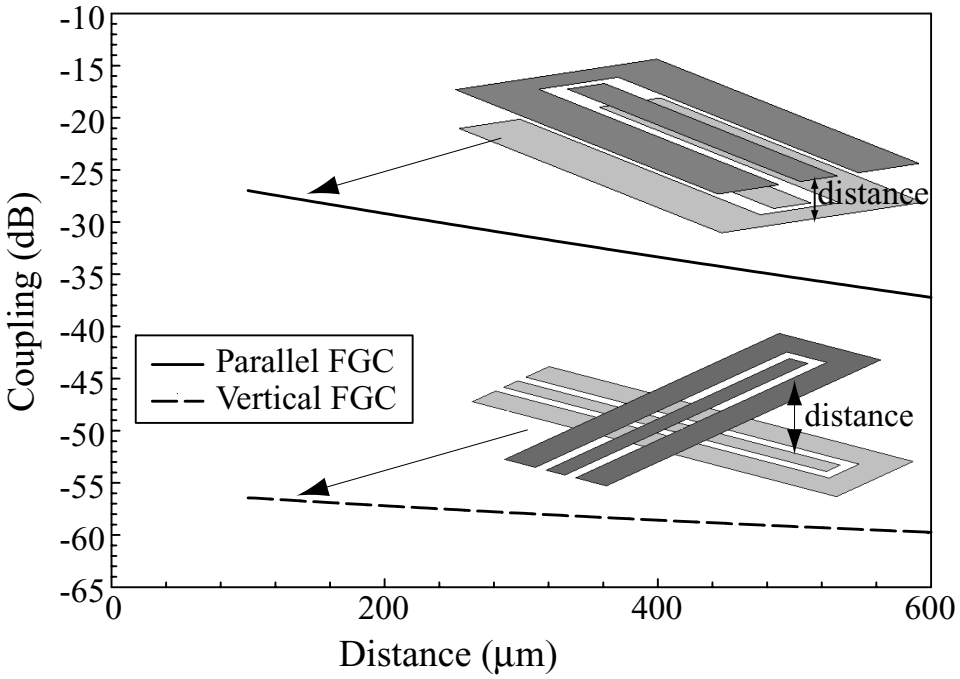


Figure 2.8: Numerical results for vertically separated parallel and perpendicular FGC lines comparing coupling versus vertical separation at 8 GHz.

Additionally, perpendicular FGC lines are studied in terms of their lateral separation. Two 50 Ω lines (2540-381-1524 μm) are printed perpendicularly in Rogers Duroid (ϵ= 2.94, thickness:1524 μm), the vertical distance between them is one and two wafer thicknesses (1524 and 3048 μm) respectively. Both lines are centered with respect to each other and the top line is moved laterally with respect to the lower one. The simulation results are displayed in Fig. 2.9 along with a schematic of the structure. From the results it is apparent that the isolation increases as the top FGC line moves away from the probing position. This trend continues until the top FGC line approaches the open end of the lower line. As expected, the discontinuity effects increase the coupling significantly. These results display the importance of probe placement for accurate coupling estimation. If the separation between the probes is small, the dominant effect responsible for reducing isolation will be the probe-to-probe coupling. On the other hand if the lines are printed close to discontinuities

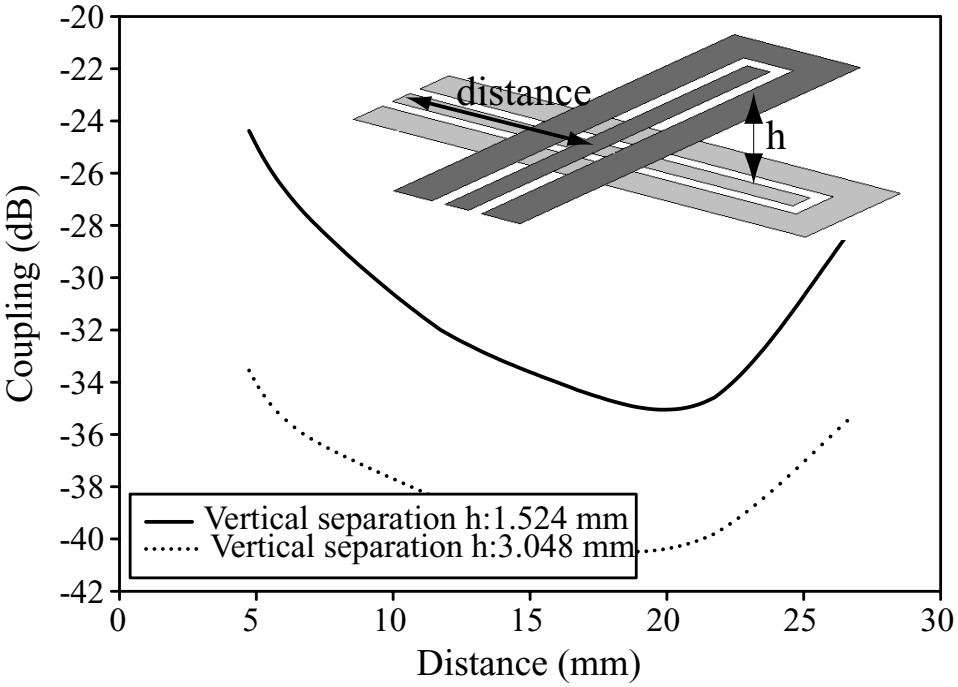


Figure 2.9: Numerical results for vertically separated perpendicular FGC lines showing coupling versus distance at 8 GHz.

less isolation should be expected. The lines in Fig. 2.9 are identical with the X-band results summarized in Fig. 2.5. The comparison between the plots indicates that the perpendicular FGC lines with a vertical separation of 1.524 mm offer an isolation of -31.6 dB, while the parallel FGC couple at -14 dB.

A similar structure for W-band measurements is fabricated in high resistivity 100 μm thick silicon wafers. The fabricated circuits are shown in Fig. 2.10 and the results are presented in Fig. 2.11, where an isolation better than -42 dB is measured. As the two lines are separated, the isolation increases to -47 dB for a distance of 500 μm. These results compared to those provided in Fig. 2.9 show a similar behavior of the perpendicular lines with respect to the lateral separation. A small offset of the two lines can improve the isolation by 3 to 4 dB. However, as was mentioned earlier, increased coupling should be expected if the open end is in close proximity with the top FGC line.

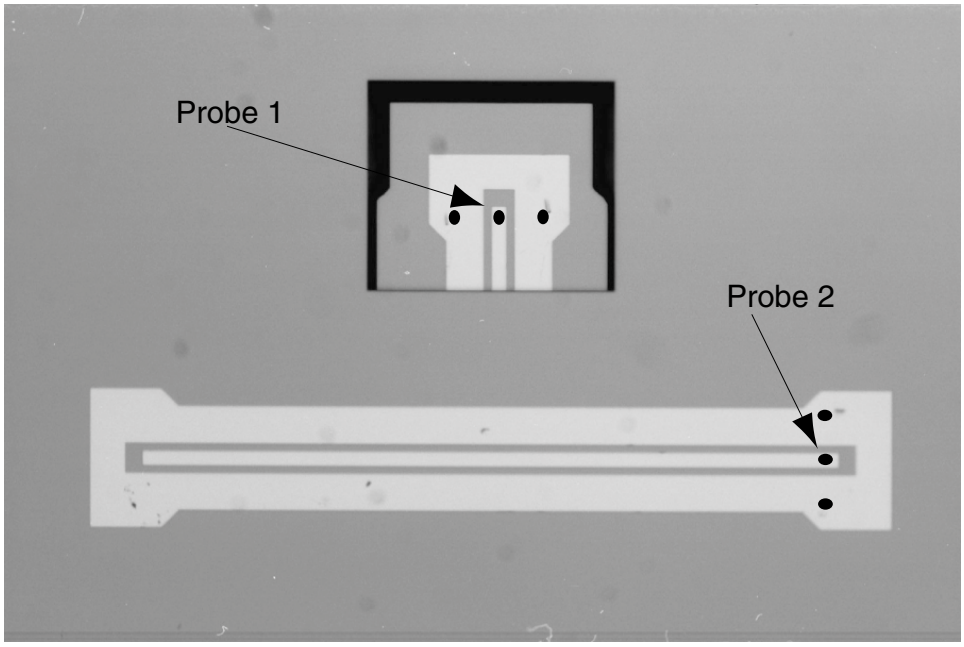


Figure 2.10: W-band perpendicular FGC lines printed on two 100 μm silicon wafers.

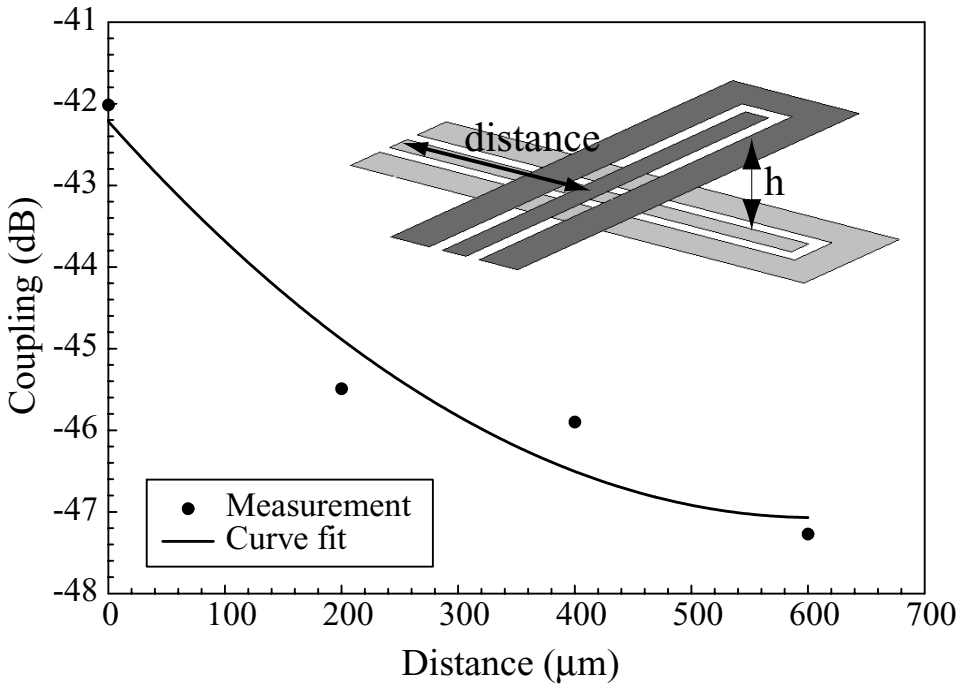


Figure 2.11: W-band measured results for vertically separated FGC lines showing coupling versus distance.

Another important factor when designing multichip modules is the use of vias for vertical transmission of signals or dc-bias lines to multiple stacked wafers. The effects of one via in close proximity to two perpendicular FGC lines with a vertical separation of 100 μm are presented in Fig. 2.12 along with a schematic of the structure. The via is designed as a rectangular box with 80 μm width and it is terminated on both ends with a $\lambda_g/4$ resonant stub. Such a configuration is viewed as a worse case scenario and its purpose is to demonstrate the effects on crosstalk of a parasitic element with a strong standing wave, due to the open stubs. However, as it will become obvious in Chapter 6, DC vias and bias lines can be built close to RF interconnects, especially in the case of packaged RF MEMS switches. DC bias lines are necessary for actuation of the devices and therefore their placement with respect to the RF lines is of major importance. The lines are identical to the interconnects analyzed in Fig. 2.8 and therefore completely comparable with the data summarized in that plot. The existence of the via deteriorates the isolation as much as 9 dB, when the via is in close proximity to the crossover section of the two lines. When the distance is increased over 2000 μm the coupling approximates the ideal case (no via present). The need of vias in a multilayered structure is inevitable; therefore, their appropriate placement is an important design consideration, significantly affecting the isolation.

Moreover, vias are utilized in multi-layered interconnects as a conducting path for vertical transition in different wafers. Fig. 2.13 shows the schematic and Fig. 2.14 the photograph of the fabricated X-band circuit consisting of a FGC transitioned through a wafer and printed in close proximity (2794 μm) to a second FGC line. The transition is accomplished using vias with a diameter of 1200 μm. In order to reduce coupling dielectric cavities with a height of 762 μm are milled on top of all three lines. The isolation with respect to the frequency is shown in Fig. 2.15 where both measurements and simulation results are included. The measurements reveal a 10 dB variation in the coupling between the two lines. This ripple is due to the length of the interconnects

utilized in this transition and not a result of an undesired tuning effect since all the FGC lines are 50 Ω matched interconnects and the dielectric cavities surrounding them resonate well above the investigated frequency band. An isolation of -25 dB at 8 GHz is observed. In order to investigate the improvement in the performance caused by the cavities, another structure is simulated where the dielectric cavity of the top FGC line, which is printed in close proximity with the vertical transition, is inverted. The creation of an extra air layer between the two FGC's increases the isolation to -30 dB at 8 GHz. The simulation of the same perpendicular FGC's, without the vertical transition shows an isolation of -28 dB for the same frequency. These simulations are conducted over the whole X-band frequency range in order to verify that the changes in isolation noticed are not a result of a small frequency perturbation. Consequently, the vertical transition lowered the isolation by 3 dB, while the different placement of the cavities increased the isolation by 5 dB.

As was already mentioned, the vertical transition launches a parasitic mode which couples to the neighboring lines. X-band simulations are performed in order to investigate the variations of this coupling with respect to the distance. The two structures analyzed are presented in Fig. 2.16 where the parameter under consideration is the distance between the edge of the vertical transition and the edge of the line. Two sets of simulations are done for a top line being either a microstrip or a FGC line. Both lines are designed to be 50 Ω (FGC: 106-24-40 μm, microstrip: 45-400 μm) in silicon. As seen in Fig. 2.17 both structures have similar response with respect to the distance from the vertical transition, exhibiting an increase of 13 dB in isolation as the distance changes from 400 to 5000 μm. The FGC line shows less coupling compared to the microstrip line by a factor of 8 dB. In the case of the microstrip line, the existence of the ground plane reduces the coupling between the line and the lower FGC. This fact means that the parasitic field launched at the top edge of the vertical transition is probably the main reason for the increased coupling between the lines.

Therefore, as was reported in the previous paragraph, careful design and appropriate placement of cavities is necessary in order to ensure high isolation.

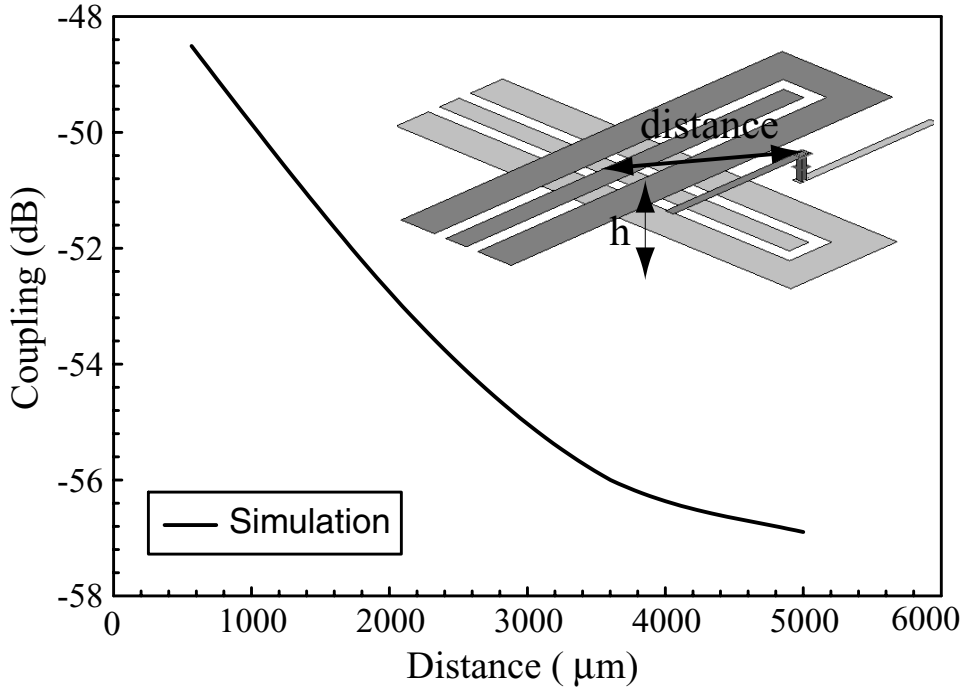


Figure 2.12: X-band numerical results for vertically separated FGC lines adjacent to via showing coupling versus via to cross-section distance.

2.5 Conclusions

A study of W and X-band circuits is presented providing results that can be utilized for the design and fabrication of high-isolation systems. FGC lines in comparison to microstrip have been shown both theoretically and experimentally to give 8 dB higher isolation, for the specific cases and frequency ranges investigated. Interconnects printed in a single or multiple layers and separated by a distance equal to one dielectric wavelength demonstrate an isolation of -50 or -60 dB for W and X-band respectively. Moreover, lines printed in close proximity to open-end discontinuities suffer a degradation in parasitic coupling by as much as 6 dB. Furthermore, the mi-

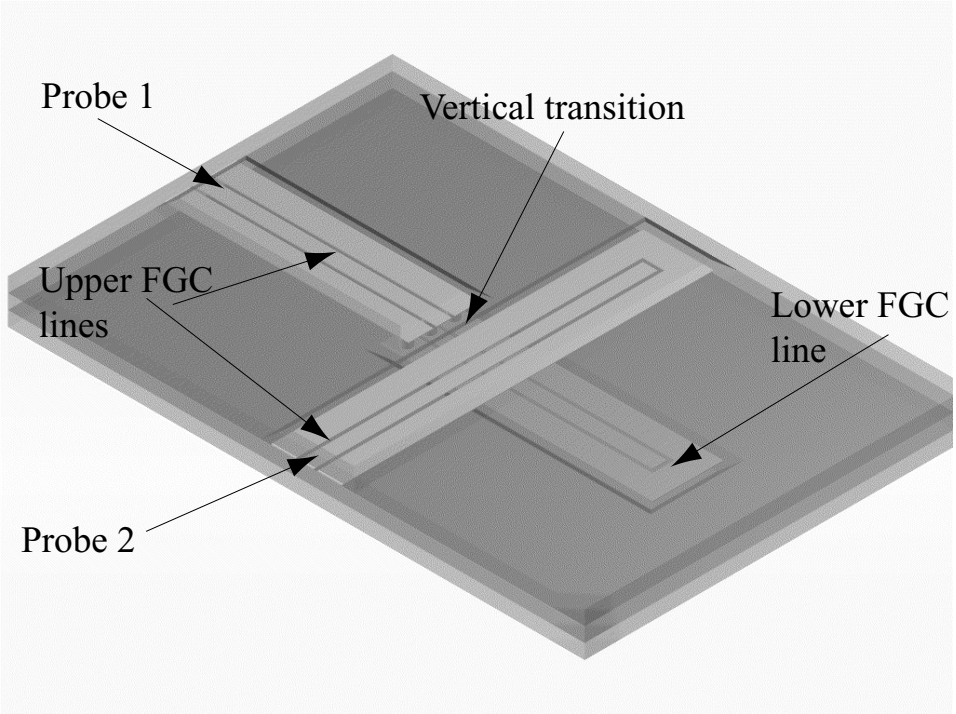


Figure 2.13: Schematic for X-band FGC to FGC vertical transition.

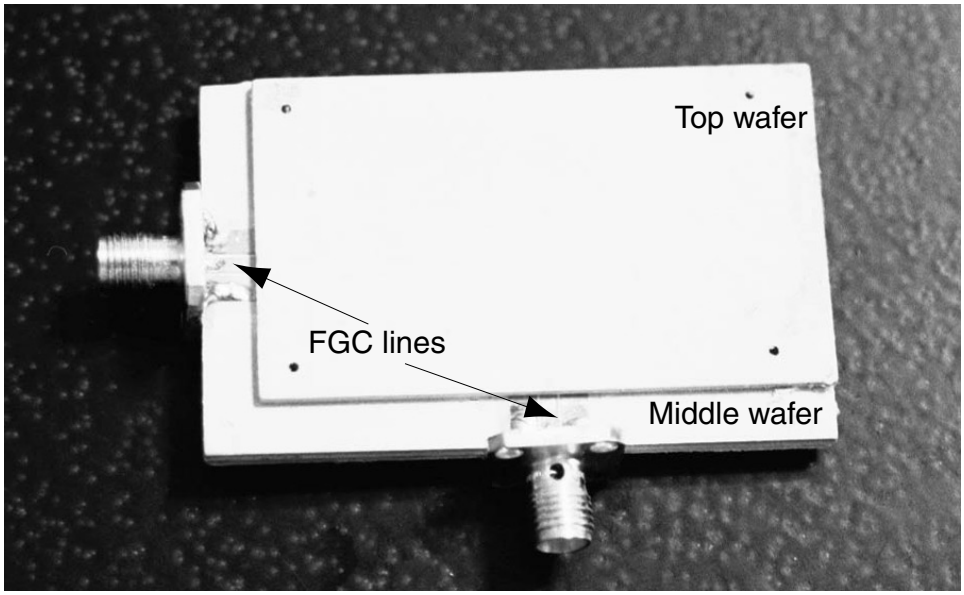


Figure 2.14: X-band vertical transition.

cromachining of dielectric cavities has been studied and shown to provide an increase in isolation on the order of 5 dB. The existence of vias next to RF interconnects

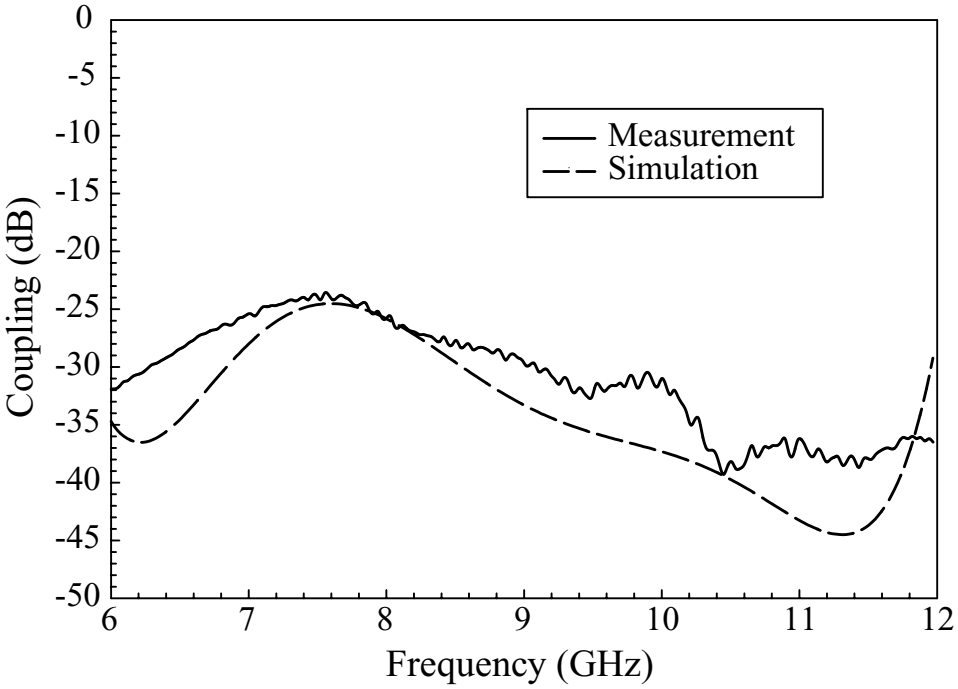


Figure 2.15: X-band measured and numerical results for vertically separated FGC lines incorporating via transition.

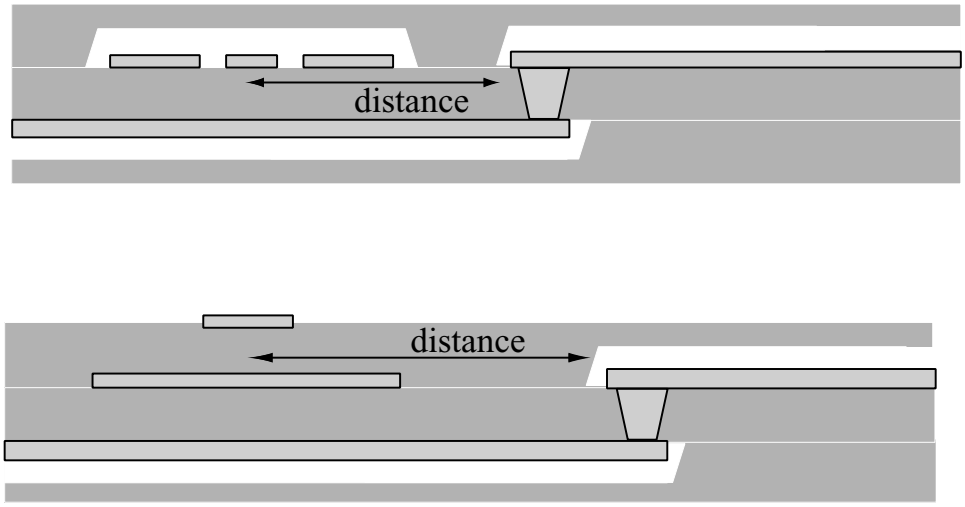


Figure 2.16: Schematics for X-band vertical transitions.

has been investigated as a worse case scenario and demonstrated reduced isolation by 9 dB. Finally, the launching of parasitic modes from vertical transitions has been studied both analytically and experimentally showing the importance of appropriate

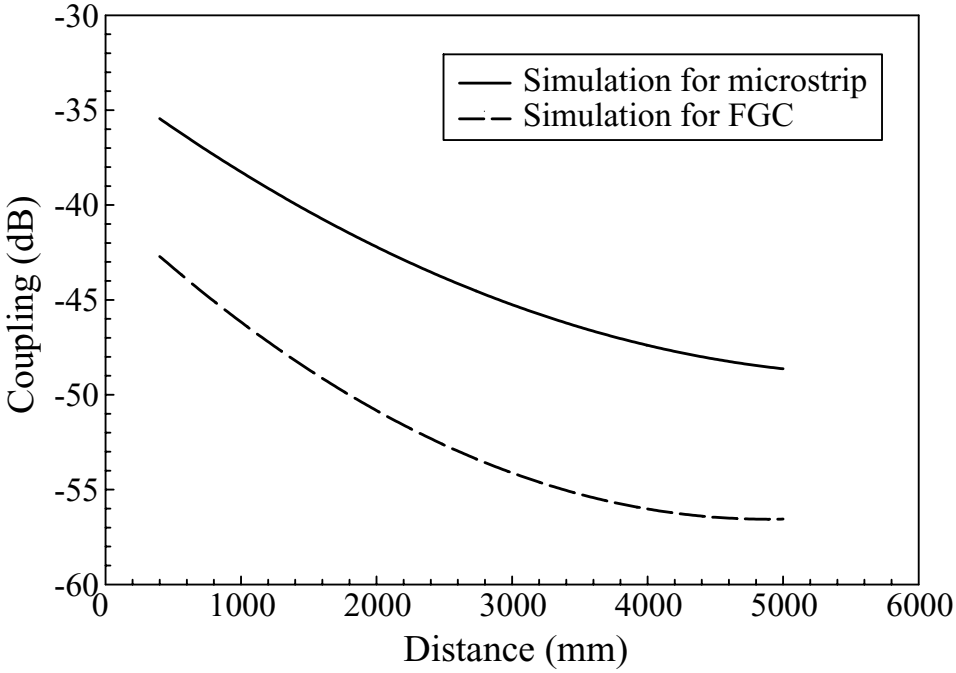


Figure 2.17: Numerical results for vertically separated FGC and microstrip lines incorporating via transition showing coupling versus distance at 8 GHz.

placement of cavities in order to ensure high isolation.

CHAPTER 3

Low-Loss Interconnects

3.1 Introduction

THE upcoming generation of tetherless (terrestrial wireless and satellite) communications technology promises a leap forward in information accessibility with a major increase in economic yield similar to that stimulated by the Internet in the 1990s. Researchers face many technical challenges, but data rates of tens of megabits per second are apparently a realizable goal early in the 21st century. While military systems have used the higher end of the millimeter-wave frequencies for many years, mainstream commercial systems are fairly new at these frequencies. Some of the requirements for such systems include the reduction of the overall size and weight, the ability to produce large quantities quickly with high yield and finally, low fabrication and assembly cost. Silicon, due to its thermal and mechanical characteristics has emerged as one alternative for the fabrication of low-cost radio frequency integrated circuits incorporating both active and passive components along with digital circuitry. However, as the frequencies become higher, low-resistivity silicon wafers, the standard for CMOS processes, are unusable due to their high RF loss. Two approaches have been utilized to overcome this difficulty.

High resistivity silicon (HRS) with resistivity >2500 Ω-cm is one approach to

resolve the loss issue. Transmission lines and passive components printed in HRS behave similarly to the same components fabricated on GaAs or other good microwave substrates. Therefore, already existing lump circuit models can be utilized to accommodate the design. Unfortunately, standard CMOS processes cannot be directly applied to HRS and require extensive modifications. Moreover, the cost per wafer is significantly more than low-resistivity wafers. While this might not be an important factor for basic research or very specialized military applications, it can be a major hurdle for commercial success.

The second approach is to use surface or bulk micromachining in order to minimize the interaction between the electromagnetic fields and the silicon substrate, which is the major mechanism causing dielectric loss. A coplanar waveguide suspended in air will have significantly less attenuation compared to a conventionally printed line due to the value of the dielectric constant. Additionally, the existence of the air substrate reduces the substrate modes, dispersion and losses due to parasitic radiation. It also provides improved electrical performance for discontinuities such as shorts, opens, steps and bends. This idea has been utilized in [33, 34] where a $SiO_2/Si_3N_4/SiO_2$ membrane is used as a building block on top of which the interconnect is fabricated. The measured results demonstrated an effective dielectric constant of 1.1 at 40 GHz and an almost 70% reduction in attenuation. Based on the same fabrication process a membrane-suspended microstrip line has been created [35] with excellent performance and has been utilized in resonators, filters, diplexers, and oscillators.

Even though membrane suspended interconnects demonstrate excellent RF performance they are extremely fragile and require large wafer area. In addition, the necessary dual side fabrication process and the complicated circuit layout prompted researchers to investigate other easier to implement solutions. Herrick in [36] proposes the removal of dielectric material from the aperture regions of coplanar waveguides using anisotropic etching. This reduces both the line capacitance and the current

density in the conductors and as a result, the line exhibits lower loss and lower parasitic capacitance. Measurements illustrate an almost 50% reduction of the effective dielectric constant (2.72 from the original value of 5.6). Similarly the loss is reduced by approximately 40%, with a 2.5 dB/cm improvement at 94 GHz. A detailed study of the effects of various geometric parameters on the measured characteristics of the interconnects is summarized in [37]. The effort presented culminated in the design and fabrication of a low-pass filter with a cut-off frequency at 55 GHz and a pass-band insertion loss of 0.8 dB at 35 GHz.

Reducing the dielectric loss can also be achieved by elevating the metal lines from the substrate [38]. In this approach lines are printed in 560 μm thick glass wafers by electroplating 3 μm of Au. In one case only the center conductor is elevated by 15 μm, while in the second both the center conductor and the ground planes are elevated at the same height. The measured results show a 52% and a 28% reduction in attenuation, compared to a conventional CPW line, for the two cases respectively. Unfortunately such a structure significantly complicates the fabrication process, negates one of the major advantages of the CPW lines, which is its planarity, and makes the fabrication of air-bridges necessary for ground equalization almost impossible.

Another solution suggested by researchers [39, 40] is to use polyimide layers, in order to develop novel RF transmission lines on CMOS-grade silicon substrates. Thin-Film Microstrip lines (TFMS) have been created by printing the ground plane on top of the silicon substrate, subsequently depositing a polyimide layer on top and finally, defining the signal line over it. As is demonstrated in [41] very low attenuation is possible since the ground plane completely shields the electromagnetic fields from the lossy silicon wafer. Furthermore, since via-holes are easily etched though the polyimide, multilayer interconnects are possible.

Compared to the microstrip case the coplanar waveguide requires significantly thicker polyimide layer in order to get acceptable attenuation. The reason for that

is that the interaction of the electromagnetic field and the lossy silicon substrate is stronger due to the absence of a ground plane. However the attenuation of the CPW line can be reduced by following the same approach as in [36], only this time the polyimide from the aperture regions is removed. This lowers the effective dielectric constant, line capacitance, and current density on the interconnect. This chapter will start with a small explanation of the simulation technique used for the presented analyses. It will proceed with the description of finite coplanar waveguides printed on low-resistivity silicon wafers. Subsequently, microstrip lines both on low-resistivity silicon and optical polymers will be presented.

3.2 Theoretical Analysis

As was already mentioned, the main purpose for the removal of polyimide from the slot regions of the CPW lines is the reduction of the effective dielectric constant and thus the interaction of the electromagnetic fields with the lossy substrate. In order to substantiate this claim a theoretical analysis using a two dimensional finite element code [11] has been used. The cross section of the interconnects is designed on top of a 500 μm thick silicon substrate, which acted as a substrate. The structure is surrounded by a radiation boundary simulating the region outside the drawing space as being infinitely large, thus, effectively isolating the model from other voltage or current sources. An initial course mesh consisting of triangular elements is created at the beginning of the solution process. The discretization of the problem area is adaptively refined until the solution converges, i.e. the energy changes between two consecutive passes are small.

From the computed values of the electric field at the nodes of the triangular elements, two dimensional contour plots for the magnitude of the electric field are generated. Additional parameters such as the effective permittivity and the charac-

teristic impedance are extracted. As usual, the capacitance of the interconnects is computed by integrating the dot product of the electric field and the electric flux density over the cross section of the structure. By solving the problem once without the dielectric and once with it, the characteristic impedance, Z_c, and the effective permittivity, ϵ_{eff}, are evaluated from the following equations:

$$Z_c = \frac{1}{c\sqrt{C_{diel}C_0}} \tag{3.1}$$

$$\epsilon_{eff} = \frac{C_{diel}}{C_0} \tag{3.2}$$

where c is the speed of light.

3.3 Coplanar Waveguides on Low-Resistivity Silicon Substrates

3.3.1 Fabrication Process

Four sets of coplanar waveguides are fabricated on 385 μm thick low resistivity silicon wafers. The fabrication process is completed at the NASA Glenn Research Center. DuPont PI-1111 polyimide is deposited and cured to a thickness Hp of 6.35, 8.83, 14.59, and 20.15 μm. Its dielectric constant is ϵ_r=2.8. Subsequently 0.02 μm of Ti and 1.5 μm of Au are deposited using a standard lift-off process. Reactive ion etching is then utilized in order to remove the polyimide from the slot regions. The outcome of this process is presented in Fig. 3.1.

The measurements are performed using a vector network analyzer and a probe station. A quartz spacer is placed between the silicon substrate and the probe station wafer chuck in order to eliminate any unwanted parallel plate modes. A Through-

Reflect-Line calibration routine [15] provided by NIST with on-wafer delay lines are utilized for accurately calibrating the analyzer from 1 to 40 GHz. For each line the parameters measured are the attenuation constant α and the effective dielectric constant ϵ_{eff}.

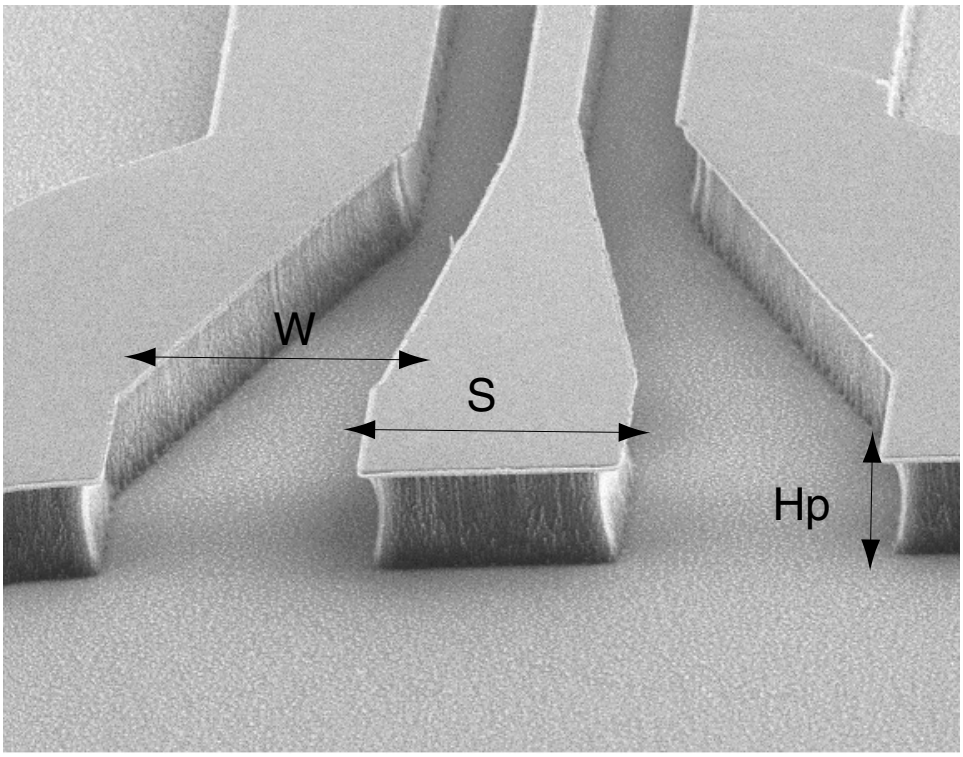


Figure 3.1: Scanning electron image of micromachined CPW on low-resistivity Si wafer with an etched polyimide interface.

3.3.2 Theoretical and Experimental Results

The measured attenuation of the CPW lines is illustrated in Fig. 3.2 where the improvement on the performance after etching the polyimide is obvious. At 40 GHz there is a 28% reduction in attenuation for the CPW with the thin polyimide layer and a 35% reduction for the thick polyimide. Interestingly, these numbers are comparable to the results acquired in [36] for micromachined CPW on high resistivity silicon wafers. For the case presented in this figure the width of the center conductor is 10

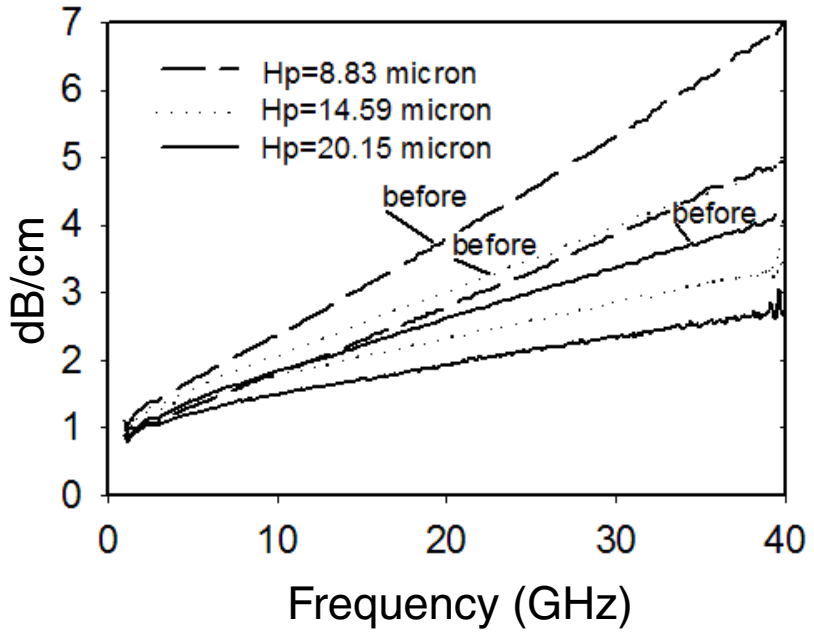


Figure 3.2: Measured attenuation of CPW lines (S=10, W=9 μm) before and after etching the polyimide.

μm while the slots are 9 μm. It appears that the attenuation varies as the square root of frequency (α=ak^n, where n=0.5), therefore the attenuation is dominated by conductor losses. As is shown in [42], at high frequencies, narrower CPW lines on polyimide have lower attenuation than wider lines. This is contrary to the attenuation characteristics of CPW interconnects on insulating substrates, which are dominated by conductor loss for both narrow and wide lines.

In addition to the attenuation, the effective permittivity after etching the polyimide also varies with the line geometry. If no interaction between the electromagnetic fields and the lossy silicon occurs the permittivity should be 2.8. Higher dielectric constant implies that part of the fields enter the silicon wafer. After the polyimide is etched and more of the fields are in the air, both above the lines and in the slot

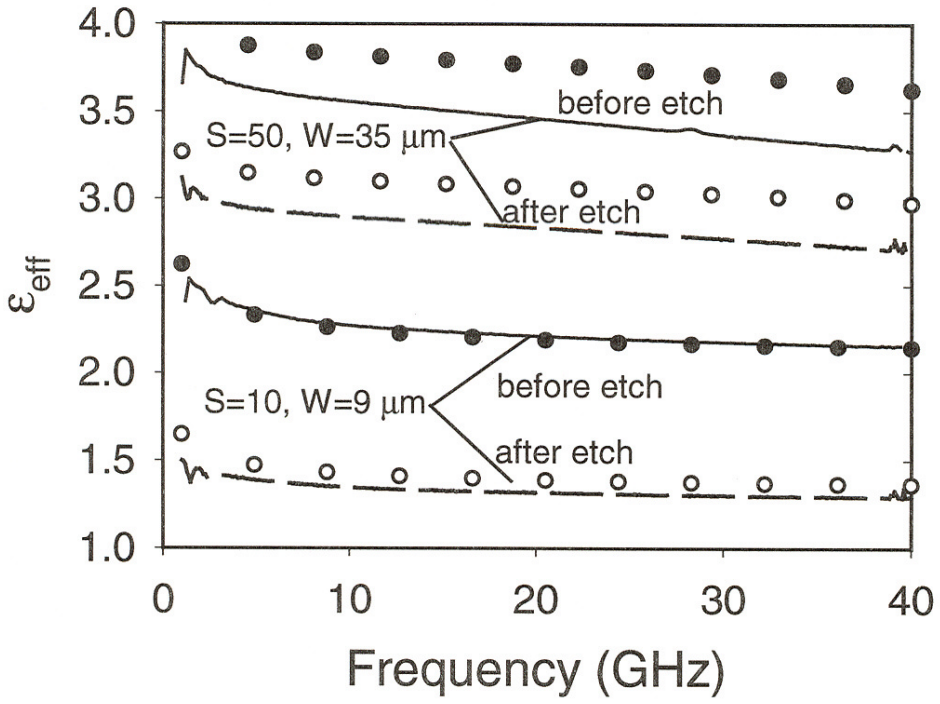


Figure 3.3: Measured and calculated effective permittivity of micromachined CPW lines with Hp=20.15 μm.

regions, ϵ_{eff} should be approaching 1. The measured results of ϵ_{eff} as a function of frequency are presented in Fig. 3.3 both for a wide and a narrow CPW line. There is excellent agreement between the theoretical and measured results, which indicates the accuracy of both methods. The small differences between the two are due to difficulties in accurately describing the physical structure in the two-dimensional FEM solver since the profile of the etched polyimide is curved. As can be observed from the measurements ϵ_{eff} is large prior to the etching of the polyimide. This indicates that the electric field is still interacting with the silicon wafer. Etching the polyimide from the slots reduces the permittivity by 17% on the wide CPW and 36% on the narrow CPW line.

The aforementioned results imply that the magnitude of the electric field in the silicon is reduced after etching the polyimide, especially for the case of the narrow CPW lines. Theoretical analysis has been utilized to verify this claim. Fig. 3.4

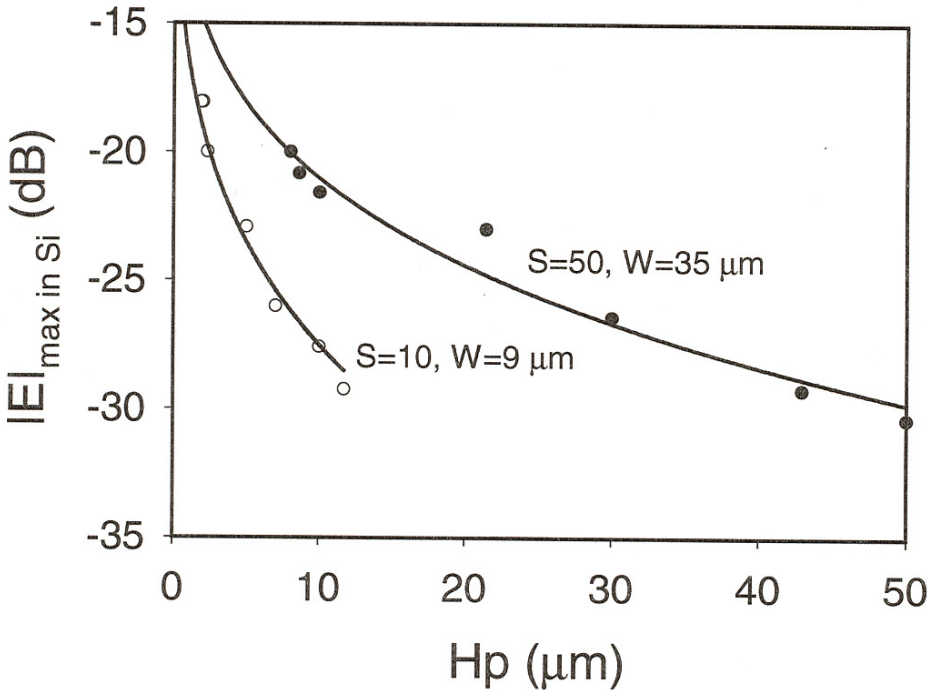


Figure 3.4: Maximum electric field in Si after polyimide etching.

presents the maximum electric field entering the silicon substrate for CPW lines with dimensions 50-35 μm and 10-9μm (center conductor width-slot width respectively) as a function of Hp. Fig. 3.5 summarizes the magnitude of the electric field for CPW lines of dimensions 50 μm and 35 μm (center conductor width and slot width respectively) and Hp=8, 20, and 50 μm respectively. It is seen that the electric fields are concentrated along the metal edges of the CPW slots, and the field magnitude inside the silicon decreases as Hp increases. As was suspected from the measurements the maximum electric field inside the silicon wafer is significantly lower for the narrow CPW case compared to the wide one.

In [42] the attenuation of such lines is compared to the one exhibited by CPW lines of the same characteristic impedance fabricated on high resistivity silicon wafers. Prior to etching the polyimide the lines on HRS are superior. However, after removing the polyimide, the lines demonstrate similar attenuation at lower frequencies, while the proposed interconnect has a 1.5 dB/cm higher loss at 40 GHz.

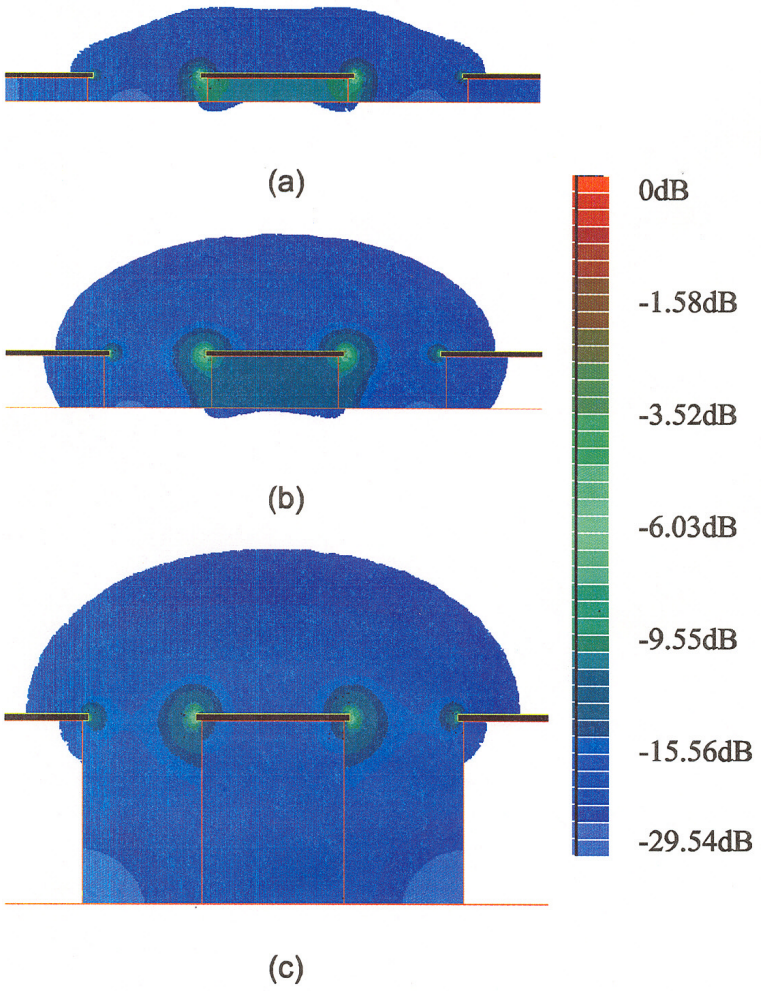


Figure 3.5: Calculated electric field magnitude for CPW lines with S=50 μm, W=35 μm, and (a) Hp=8 μm, (b) Hp=20 μm, and (c) Hp=50 μm.

3.3.3 Design Rules

In order to establish design rules for such interconnects, the measured ϵ_{eff} may be used. Fig. 3.6 shows the measured results for CPW lines on polyimide before and after etch. In order for the field interaction to be low, the ϵ_{eff} should be less than 1.9 (ϵ_{eff}=(2.8+1)/2). This requires that (S+2W)/Hp<3. By utilizing the acquired theoretical results the maximum magnitude of the electric field inside the silicon wafer is presented in Fig. 3.7. In order for that to be less than -30 dB, (S+2W)/Hp must be less than 2. Therefore a reasonable design rule for the low-loss CPW lines on

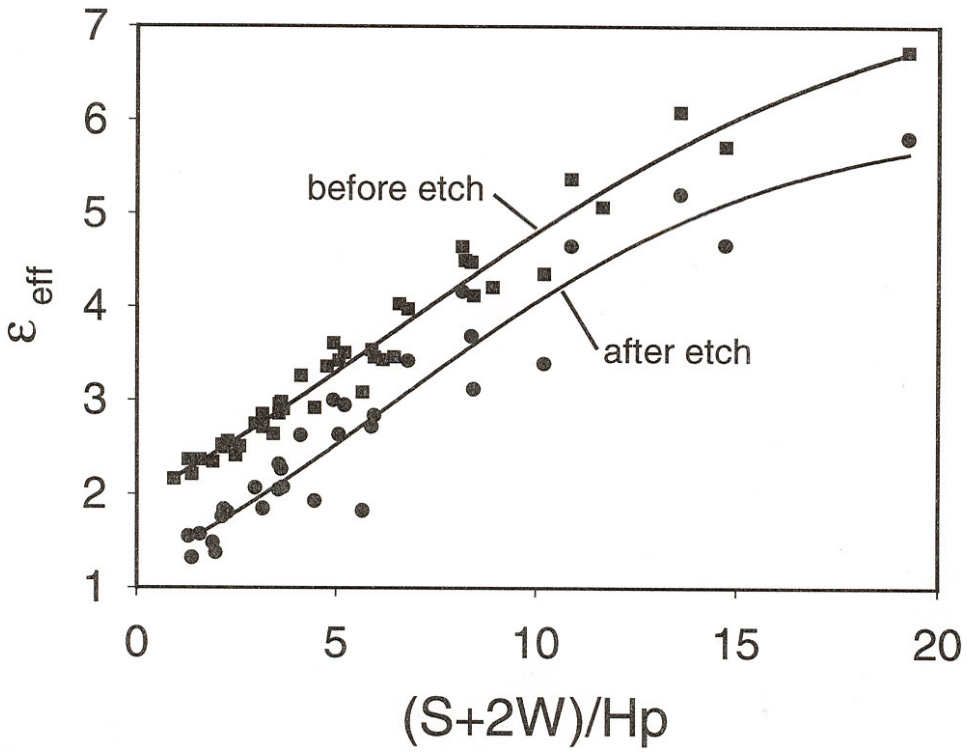


Figure 3.6: Measured effective permittivity before and after polyimide etching as a function of (S+2W)/Hp (frequency=20 GHz).

low-resistivity silicon with etched polyimide is (S+2W)/Hp<3.

3.4 Thin Film Microstrip Lines on Low-Resistivity Silicon Substrates

3.4.1 Fabrication Process

Coplanar waveguides are not the only type of interconnects used in the RFIC community. A significant number of circuits is designed based on microstrip lines. Similarly to the CPW, microstrip lines suffer from high attenuation when printed on low resistivity silicon wafers. One approach to resolve this issue it to create Thin Film Microstrips (TFMS) which have low loss and may be manufactured using standard

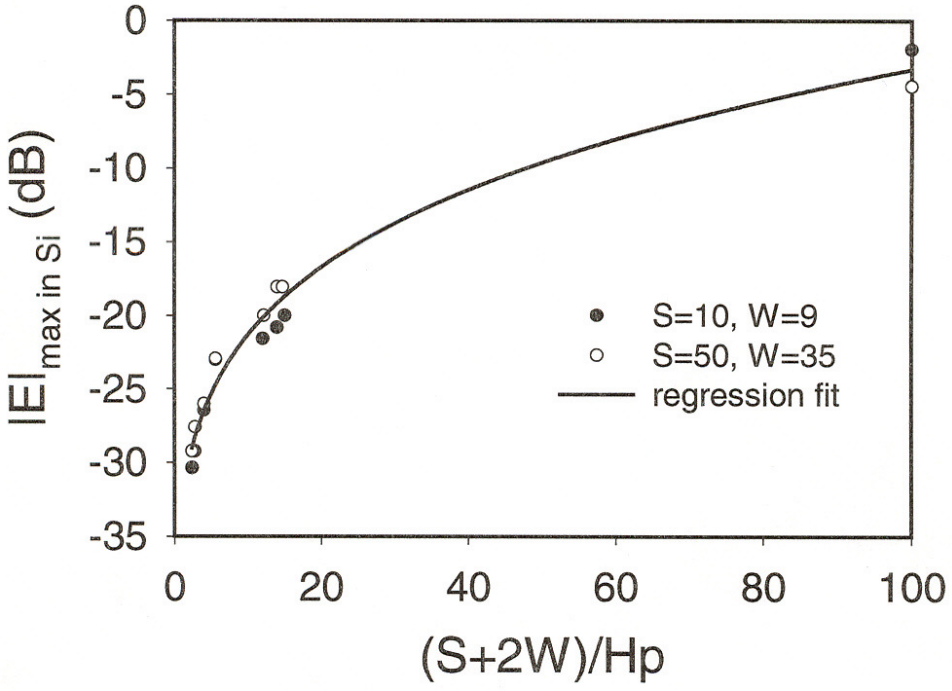


Figure 3.7: Maximum electric field in the Si after polyimide etching as a function of (S+2W)/Hp.

silicon processing steps [43]. A schematic of such an interconnect is presented in Fig. 3.8. Typically, a large area of the top side of the silicon wafer is metallized to form the ground plane of the TFMS. Thus, its width can be considered infinite and therefore there is almost no interaction between the electric field (which exist between the signal line and the ground plane) and the lossy silicon wafer. On top of the ground plane a thin layer of polyimide is then deposited and subsequently the signal strip is printed using a standard lift-off deposition technique. The ground plane consists of 0.02 μm of Ti and 1.5 μm of Au, while the signal line is formed by 0.02 μm of Ti and 1.6 μm of Au. The polyimide used is PI-2611 with a measured dielectric constant of 3.12 and a loss tangent of 0.002 [44].

As was already mentioned, standard TFMS lines have wide ground planes in order to shield the electric field from the lossy dielectric. Therefore a system based on such interconnects can not be compact and is very possible to suffer from unwanted

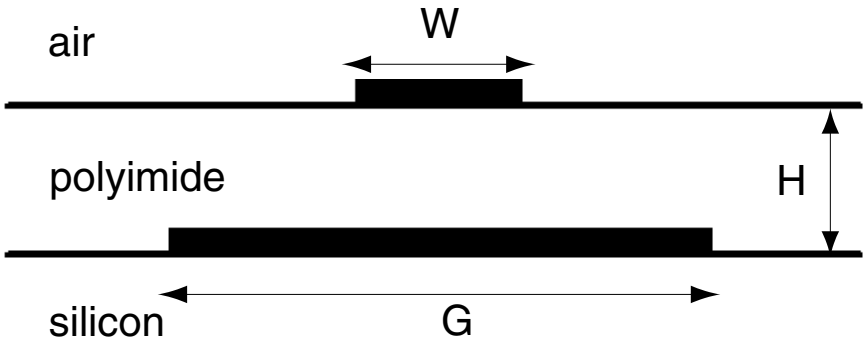


Figure 3.8: Schematic of Thin Film Microstrip Lines (TFMS)

parallel plate modes due to the abundance of metal layers. The aim of this research is to investigate the possibility of reducing the width of the ground plane to sizes comparable to the strip line. For the purposes of such a study TFMS lines of widths 23 and 52 μm are utilized. The characteristic impedance of these are calculated at 52 and 30 Ω respectively. Ground planes of widths G equal to 2W, 3W, 5W, and 9W are characterized.

3.4.2 Theoretical and Experimental Results

The measured attenuation for the two types of TFMS lines is presented in Fig. 3.9. As expected while the width of the ground plane increases the attenuation decreases. However, the difference between the wide and narrow case is less than 0.8 dB/cm for the 23 μm case and 0.5 dB/cm for the 52 μm. From the measured results it is deduced that the minimum required ground plane width for low-loss operation is 3W. There is no significant improvement in the performance for wider ground planes. As mentioned in [41] similar behavior is noticed for the measured effective permittivity, since there is almost no change in its value for ground planes wider than 3W.

The measurements demonstrate that it is possible to use narrow ground planes on CMOS grade silicon wafers without a penalty in attenuation. Unfortunately the origin of this attenuation is undetermined. Because of the excellent agreement between the

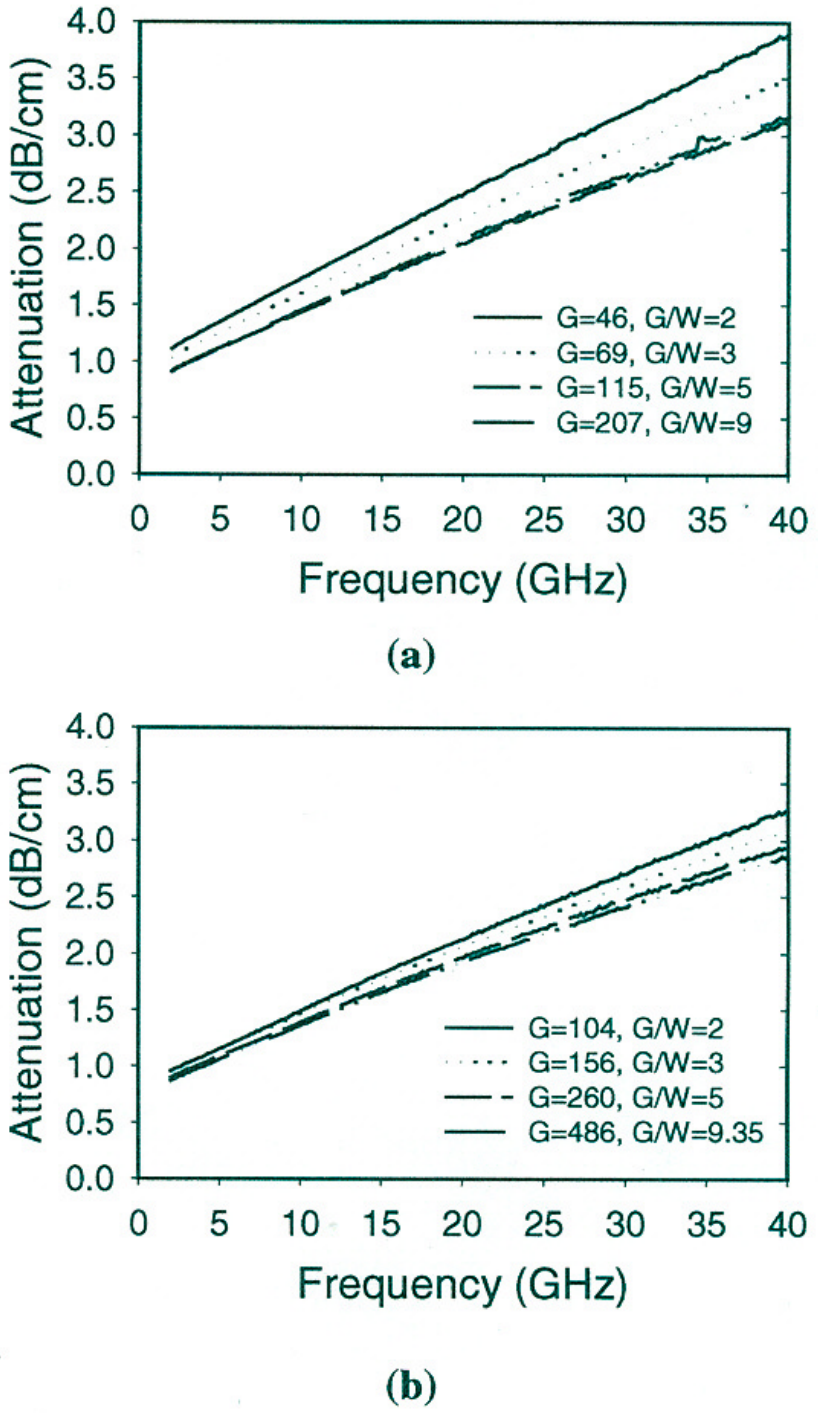


Figure 3.9: Measured attenuation of TFMS lines as a function of frequency with (a) W=23 μm and (b) W=52μm.

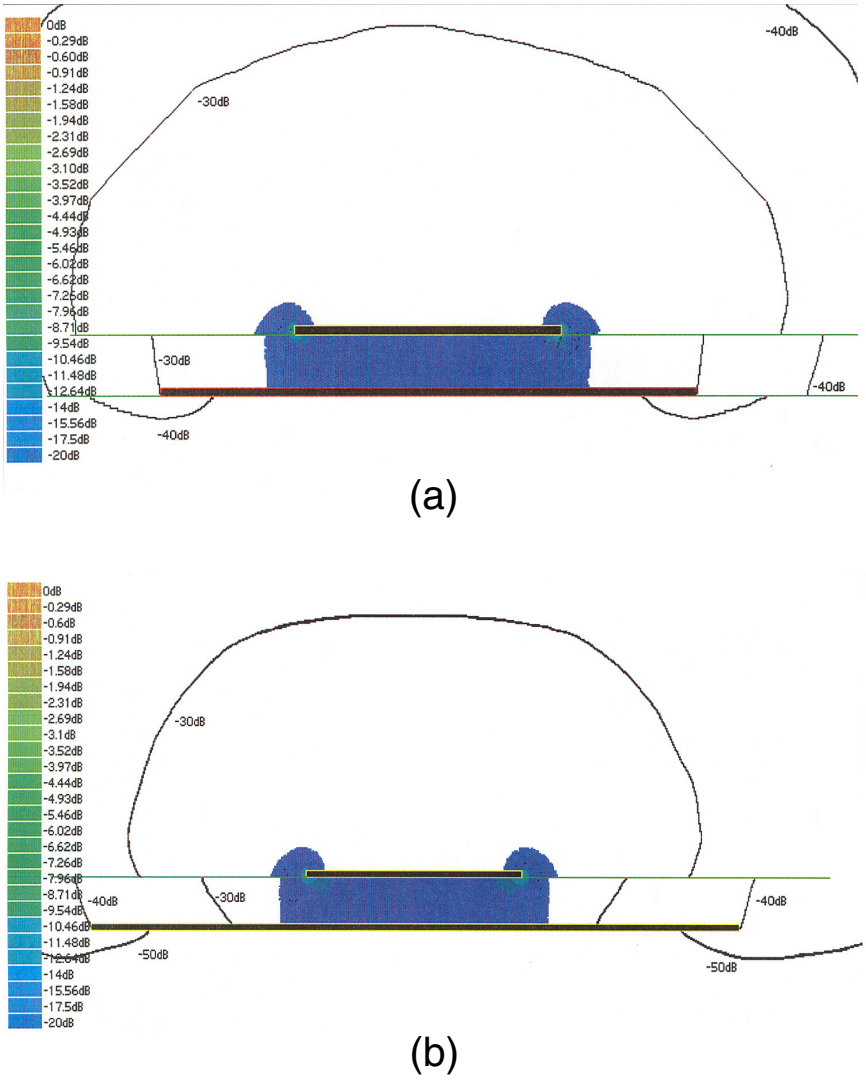


Figure 3.10: Calculated electric field for TFMS with W=52μm and (a) G/W=2 and (b) G/W=3.

measured and theoretical data, it is possible to use the theoretical analysis to answer this question. The two existing possibilities are that the high loss is due to either high electric field concentrations inside the lossy silicon wafer or high conductor loss due to higher current densities. In Fig. 3.10 the magnitude of the electric field for two cases is presented. It is clearly seen that most of the field lines are concentrated immediately below the strip line. The maximum electric field inside the silicon wafer as a function of the G/W ratio is shown in Fig. 3.11. It is observed that the magnitude decreases

as the ratio increases regardless of the width of the microstrip line. Additionally, the current densities on the ground plane are summarized in Fig. 3.12. As the width increases the current density decays rapidly and it increases again at the edge of the ground plane. Based on these results it can be claimed that the attenuation is dominated by conductor losses and not dielectric losses inside the silicon wafer. Even for the narrow ground plane case the electric field is 30 dB bellow its maximum magnitude directly under the strip line. Therefore it can be safely stated that the measured differences in the attenuation are not caused by the very weak electric field inside the wafer. The theoretical results for the current densities indicate strongly that the higher attenuation for the narrow line is due to the higher conductor losses.

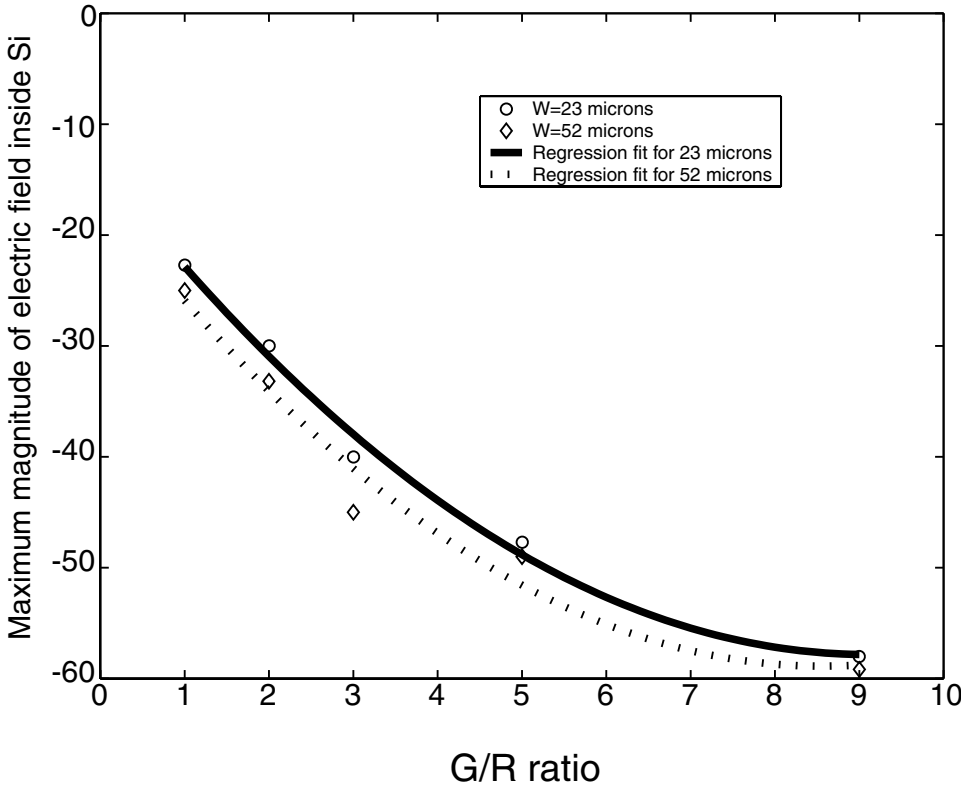


Figure 3.11: Maximum electric field inside the Si wafer for W=23μm and W=52μm.

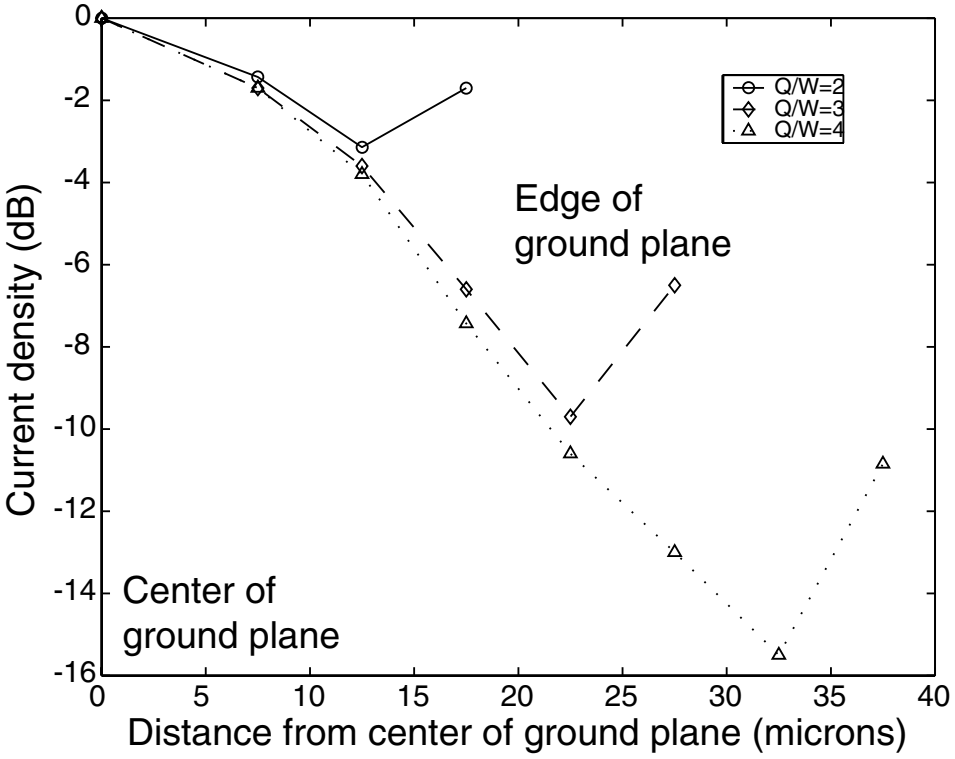


Figure 3.12: Calculated current density on ground plane.

3.5 Thin Film Microstrip Lines on Quartz Substrates

3.5.1 Optical Polymers

Thin film microstrip lines can be also fabricated using optical polymers instead of polyimide. This will allow the integration of optical modulators and MEMS devices on a single chip and can thus provide the building blocks for complicated optoelectronic systems. In order to investigate the feasibility of such an approach some initial RF characterization is performed on such substrates. A cross section of the samples is illustrated in Fig. 3.13. A 500 μm quartz wafer is used for the fabrication of the lines. A layer of gold is deposited on the wafer, forming the ground plane of the TFMS lines. Such an "infinite" ground plane has the advantage of isolating the

Table 3.1: Characteristics of optical polymers

Material	Refractive index
Epoxylite01	1.54
Epoxylite02	1.524
LD3Polymer	1.61

electromagnetic fields from the quartz wafer, thus the only loss measured can be attributed to conductor losses and to losses due to the optical polymers. After the deposition of the ground plane three polymer layers are applied. In sample A the layers are: 4.5 μm of Epoxylite02, 2.2 μm of LD3, and 4.3 μm of Epoxylite01. For sample B the layers are: 4.5 μm of Epoxylite02, 2.3 μm of LD3, and 4.3 μm of Epoxylite01. The characteristics of the polymers are summarized in Table 3.1.

Figure 3.13: Cross section of samples with optical polymers.

3.5.2 Design and Fabrication Process

Initially 50 Ω TFMS lines are designed on the optical polymers for RF operation. Due to the small value of the dielectric permittivity of these materials the total width of the lines is 30 μm. Since the available measurement probes are for CPW interconnects there is a need for a coplanar-to-microstrip transition operating well at the respective frequencies of operation. Such a uniplanar transition has been introduced in [45] demonstrating a 0.3 dB insertion loss and a return loss below 17 dB for W-band operation. The transition utilized $\lambda_g/2$ radial stubs in order to achieve

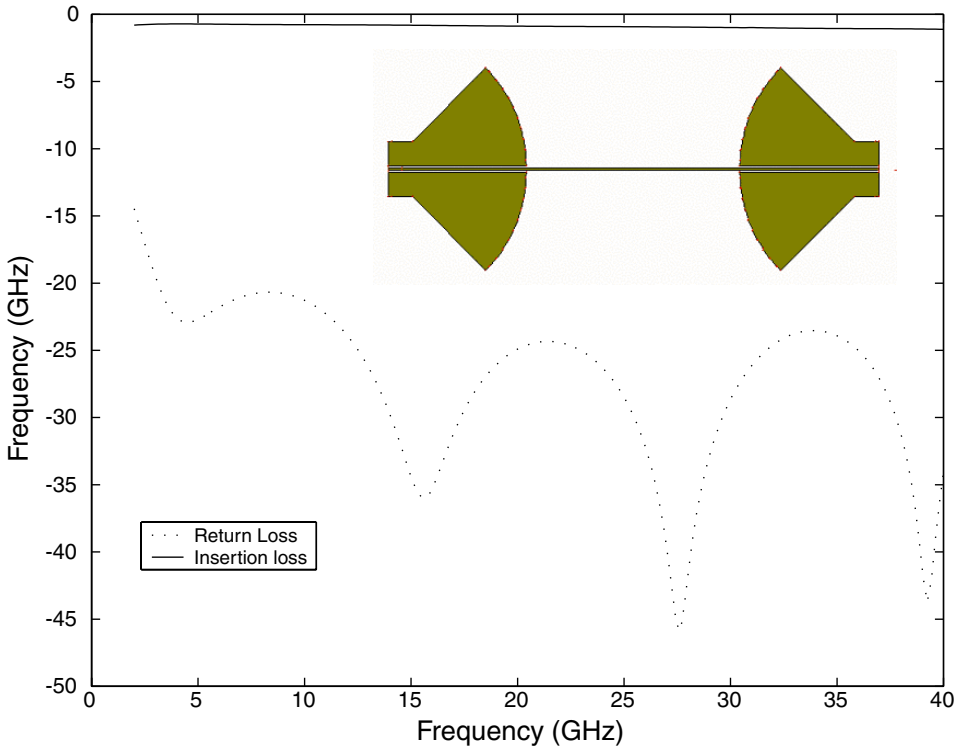


Figure 3.14: Simulated response and schematic of CPW-to-microstrip transition.

ground equalization between the coplanar and the microstrip ground planes and thus no via-holes are necessary. The transition demonstrates a 20% bandwidth at W-band for a 100 μm thick silicon wafer. The same design is utilized in the case of the optical polymers. Now however, the total thickness of the dielectric is significantly less (11 μm) and consequently a more broadband response is attainable. For the design of the transition a 2-dimensional moment method code has been used [12] and the outcome of the design process is presented Fig. 3.14.

For the fabrication of the microstrip lines, initially a seed layer of Cr/Au (200/400 Å) is evaporated on the samples. Appropriate photoresist is spun cast on the samples, exposed using a conventional aligner and developed. Subsequently, 4.5 μm of Au is electroplated to form the signal lines. The optical polymers used are sensitive to solvents and therefore striping the photoresist by immersing the samples in Acetone or PRS-2000 is not possible. Instead the samples are flood exposed on the aligner

and overdeveloped. This process successfully removes the unwanted photoresist and allows the etching of the Cr/Au seed layer. The resulting lines are presented in Fig. 3.15.

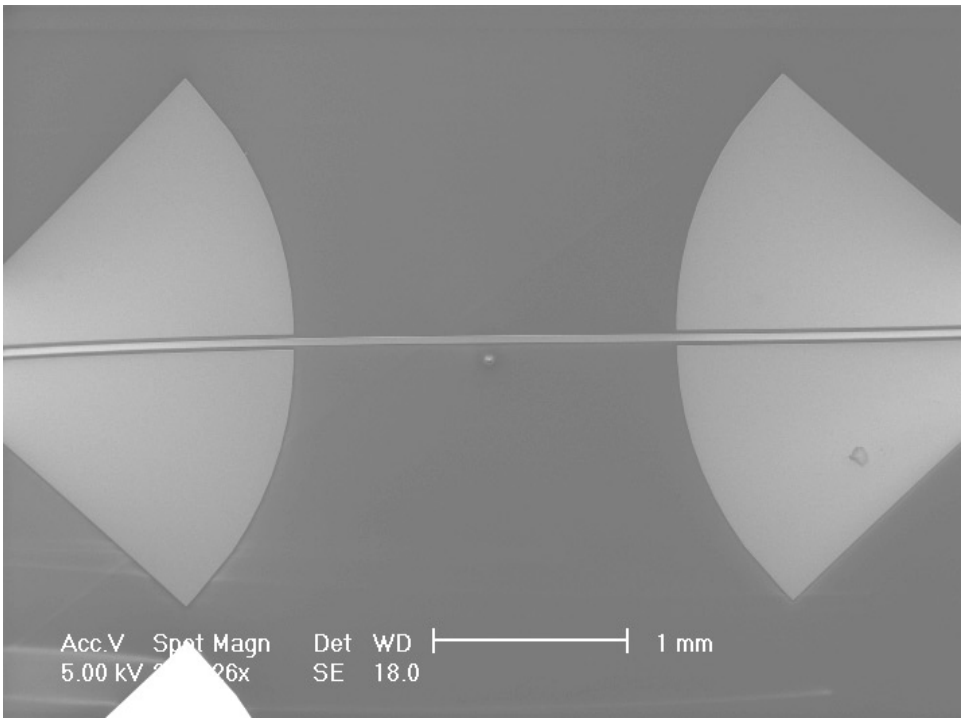


Figure 3.15: Scanning electron image of fabricated TFMS line.

3.5.3 Theoretical and Experimental Results

For the X-band measurements, a HP 8722D vector network analyzer is utilized on an Alessi probe station with 150 μm pitch GGB picoprobes. Through-Reflect-Line (TRL) calibration is performed using on-wafer calibration standards fabricated in conjunction with the circuits to be tested. Multical, developed by NIST is used to implement the TRL calibration [15]. Delay lines of lengths 7.278mm, 7.72mm, 8.604mm, 11.256mm, 16.561mm, and 20.096mm have been used for both the calibration of the system and the characterization of the RF losses. The measured attenuation of the two types of lines is presented in Fig. 3.16 from where it can be

observed that both lines have similar response with sample B being slightly lossier.

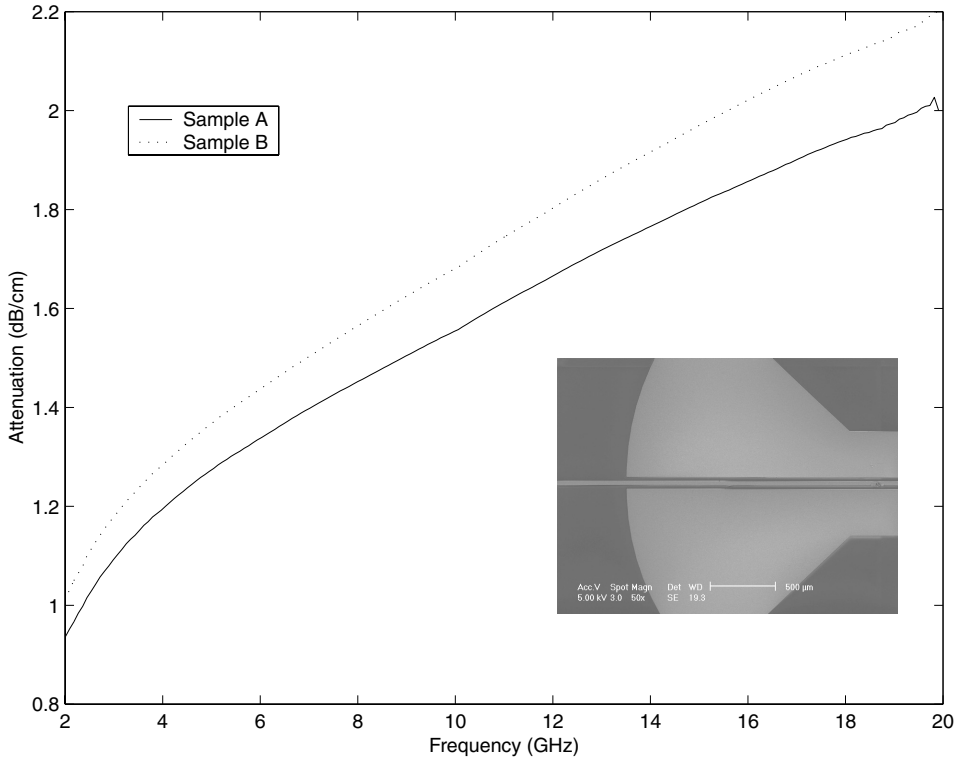


Figure 3.16: Measured attenuation of TFMS lines.

3.6 Conclusions

In this chapter various types of interconnects have been characterized for high frequency applications. Printing coplanar waveguides on top of polyimide and subsequently etching the material from the slot regions has been shown to provide very good performance. Comparable attenuation to high resistivity lines is reported while essential design rules have been proposed. Additionally, thin film microstrip lines have been studied, using polyimide as the intermediate dielectric. The effects of the finite ground plane have been investigated and the combination of measured and theoretical results illustrate that the dominant mechanism causing increased attenuation is the conductor loss. Finally, microstrip lines have been fabricated on optical polymers.

A coplanar waveguide-to-microstrip transition is designed offering excellent response up to 40 GHz. Theoretical analysis and measured results help to characterize the performance of the interconnects on these materials.

CHAPTER 4

Silicon Micromachined Evanescent Mode Filters

4.1 Introduction

SATELLITE communications require optimum high frequency performance, lightweight hardware, advanced packaging, high density interconnect technology and high reliability. The use of electronics in space poses interesting but grand challenges. It provides the opportunity for using revolutionary concepts in circuit design, fabrication, and implementation in order to achieve what is considered by today's standards as ultimate performance at minimal volume and very low cost. Typical communication satellites employ traditional waveguide front-end architectures due to excellent electrical performance and high reliability. However, these systems are extremely massive and utilize large volume mostly attributed to the low-insertion loss waveguide switch, diplexer, and waveguide packaged solid-state power amplifier. These three components are interconnected by waveguide sections for compatibility resulting in a large system. Despite that, waveguide has been the transmission medium of choice for space applications due to its low-loss. Replacement of the waveguide components by micromachined ones without substantially affecting the electrical performance can lead to a breakthrough in wireless communications.

Silicon micromachined resonators and filters have already been demonstrated

[46, 35, 47] and showed excellent RF performance. Even though the attainable Q values were less than those reported for waveguide-based systems, their small size and weight makes them very appealing. Furthermore, these filters can be monolithically integrated with conventional planar technology, thus making possible the design of complete communication systems on a single chip. The integration of packaged RF MEMS on the same wafer can provide the ability to tune the system at different frequencies of operation.

Historically, the development of microwave passive filter networks consists mainly on finding distributed components which can provide inductive and capacitive reactances to replace the lumped elements employed by the filter prototype. Although distributed networks are necessary for high Q-reactance elements, it is not essential for these networks to be based on conventional transmission line types of structures. For some years now literature has been accumulating on network design using waveguide sections below their cut-off frequency [48, 49, 50]. Lebedev and Guttsait [51] first discovered that resonant behavior can be achieved by any evanescent mode if appropriate terminating conditions (a conjugate reactance) for that mode are provided.

4.1.1 Basic Theory

The basic mathematical analysis of evanescent mode waveguides starts with the investigation of a metallic rectangular structure in which both dielectric and air-filled regions are interspersed in a periodic manner [52]. Comparatively large internal reflections exist in such a combined unit and it is customary to employ Floquet's theorem to determine the propagation constant of the complete region. The waveguide under examination is excited by a TE_{10} mode which is evanescent in the air-filled regions and propagating in the dielectric loaded regions. The analysis begins by expressing the fields in the two regions independently in terms of the incident and reflected waves and then applying Floquet's theorem and appropriate boundary conditions. Follow-

ing the mathematical steps described in [52] the TE_{10} mode in the evanescent region is given by the following equations:

$$E_y = \sin\left(\frac{\pi x}{a}\right) e^{-\alpha z} \tag{4.1}$$

$$H_x = j\left(\frac{\epsilon}{\mu}\right)^{1/2}\left[\left(\frac{f_c}{f}\right)^2 - 1\right]^{1/2} \sin\left(\frac{\pi x}{a}\right) e^{-\alpha z} \tag{4.2}$$

$$H_z = j\left(\frac{\pi}{a}\right)\frac{1}{\omega\mu}\cos\left(\frac{\pi x}{a}\right) e^{-\alpha z} \tag{4.3}$$

4.1.2 Quality Factor of an Evanescent Mode Resonator

The aforementioned equations describe the TE_{10} mode of a resonator assuming large but finite conductivity of the walls. The Q factor of a guide excited by such a mode can be evaluated in the usual way as the ratio of stored to dissipated energy. Thus

$$Q = \frac{\omega \times \text{peak stored energy}}{\text{power loss}} = \frac{\omega U_P}{W_L} \tag{4.4}$$

The peak stored energy is given by

$$U_P = \frac{\epsilon ab}{8\alpha}\left[2\left(\frac{f_c}{f}\right)^2 - 1\right]\left(1 - e^{2\alpha l}\right) \tag{4.5}$$

while the power loss is

$$W_L = R_s|J|^2 \tag{4.6}$$

where R_s is the surface resistance of the resonator. Following the analysis in [52] the quality factor of the evanescent mode filter is:

$$Q = \frac{\omega\mu}{R_s}\frac{ab}{2}\frac{1 - \frac{1}{2}(f/f_c)^2}{\left[1 - \frac{1}{2}(f/f_c)^2 + b\right]} \tag{4.7}$$

The quality factor of a WR90 waveguide as a function of frequency is presented in Fig.4.1 for both the propagating and the evanescent modes. Below the cut-off frequency the Q exhibits a maximum, while above f_c it is a monotonic increasing function of frequency. By differentiating equation (4.7) the frequency where this maximum occurs can be evaluated by:

$$\left(\frac{f}{f_c}\right)^2 = 2 + 5\frac{b}{a} - \sqrt{25\left(\frac{b}{a}\right)^2 + 16\frac{b}{a}} \tag{4.8}$$

This curve represents the quality factor of an inductive element; in practice it will be necessary to add the loss of the capacitive element in order to obtain the total Q factor of the resonator. Therefore the Q factor given by equation (4.7) should be considered ideal and the actual factor measured should be lower, depending on the capacitive element used to create the resonant behavior.

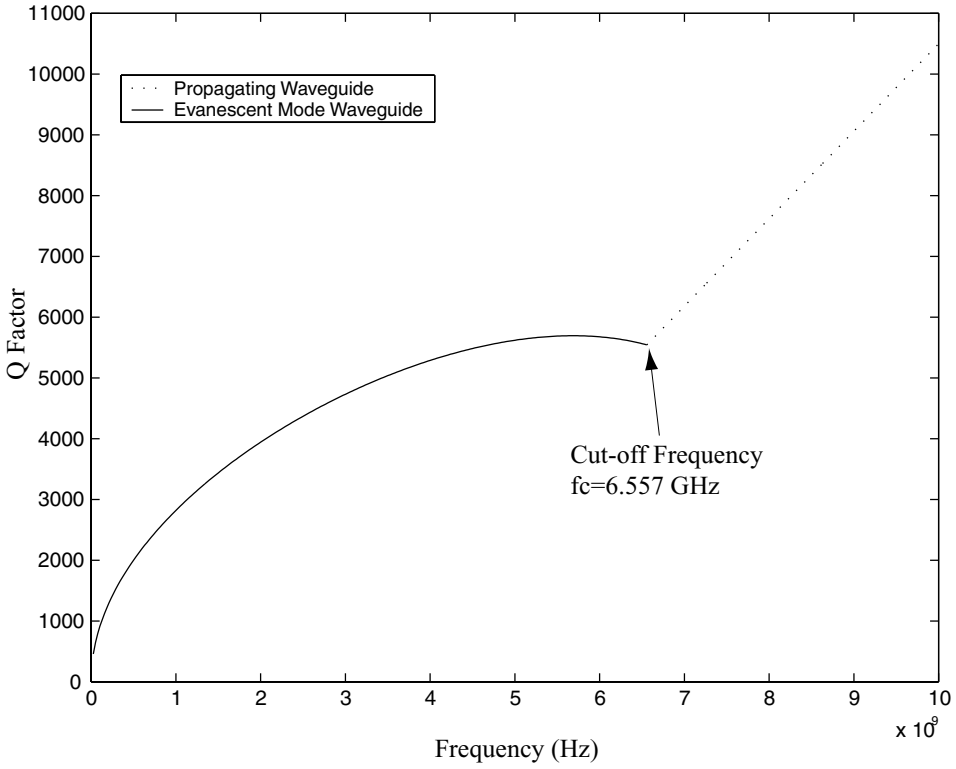


Figure 4.1: Quality factor of the TE_{10} mode in a WR90 waveguide.

The work presented in this chapter will start with some details regarding the design process followed for the creation of the resonators and the two-pole filters in high resistivity silicon wafers. The fabrication issues connected with this effort will then be presented, along with the necessary steps taken to address them. Subsequently, the measured results for these structures will be presented and the chapter will conclude with some proposed tuning mechanisms for evanescent mode filters and suggestions for their fabrication.

4.2 Design Process

4.2.1 Geometrical Properties

As was previously mentioned, an evanescent mode waveguide demonstrates an inductive behavior, therefore a capacitive discontinuity is necessary in order to create resonances. Such a discontinuity can have a variety of forms. A "capacitive" iris has been analyzed in [53] and is shown to behave as a capacitive susceptance above the cut-off frequency and as an inductive obstacle below it. Therefore the iris is in fact a resonator by itself centered at f_c. A capacitive strip is investigated at [54]. This discontinuity has the ability to create two different resonances: a series resonance, resulting from cancelling out the inductive property of the strip by its increased capacitance as it approaches the bottom waveguide wall; and a parallel resonance due to the width of the strip. Finally, a discontinuity extensively analyzed is the capacitive post which can achieve capacitive susceptances ranging from zero to virtually infinity. This obstacle has been experimentally and theoretically investigated [55, 56]. Both analyses refer to waveguides above cut-off, however there seems to be a qualitative agreement between these results and future research performed on evanescent waveguide filters [57, 58].

Fabricating an evanescent resonator utilizing silicon micromachining limits the

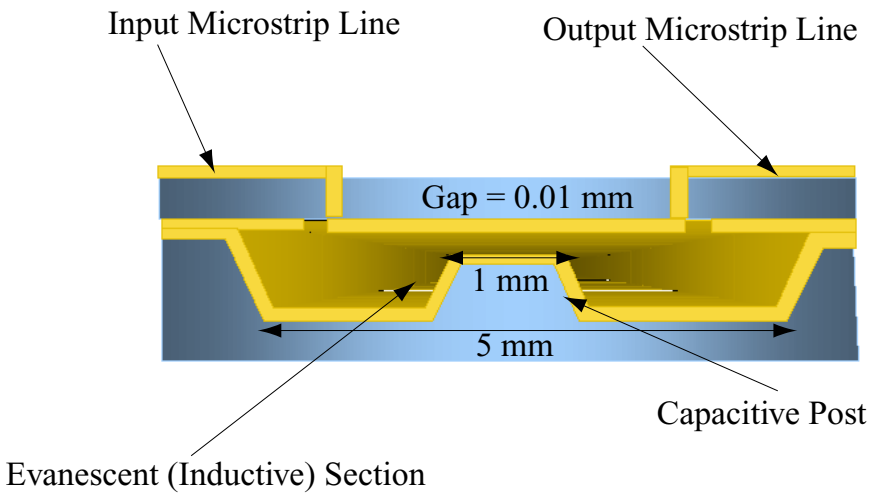


Figure 4.2: Schematic of evanescent mode resonator.

available options for creating a capacitive discontinuity. A capacitive post can be easily fabricated using anisotropic etching and the capacitance it provides can be accurately controlled by its area and the distance between the top of the post and the opposite waveguide wall. However, due to the etching process, the resulting post has a pyramidal shape, and this fact makes any possible theoretical analysis extremely complicated. In contrast to the aforementioned theoretical research pertinent to capacitive metal posts, the proposed structure has an extended slanted sidewall, approximately 320 μm in length on each side, due to the orientation of the silicon crystal planes (Fig.4.2). This sidewall has both an inductive (due to its length) and a capacitive (due to its variable proximity to the top wall) behavior and therefore an extensive theoretical analysis is necessary in order to fully understand its performance and create its equivalent circuit. This difficulty promted the use of a full wave simulator for the analysis of the structure [10]. Based on the acquired results [59] increasing the capacitance of the post moves the resonance frequency at higher values but reduces the Q factor. Increasing the length and height of the evanescent regions (on each side of the post) increases both the resonance frequency and the value of Q. However, since the height of the cavity is set by the thickness of the silicon wafer

used, the design procedure involves only the other dimensions of the cavity and the post.

An initial attempt to fabricate such a resonator is published in [60] where the material used is Duroid and the dimensions of the resonator are 20 mm by 17 mm by 2 mm for the cavity and 7 mm by 7 mm by 1.9 mm for the post. The measured results showed a resonance at 3 GHz and an unloaded Q value of 247. A subsequent effort, at the time, to fabricate the resonator in silicon failed, due to fabrications issues, which will be analyzed in the following sections.

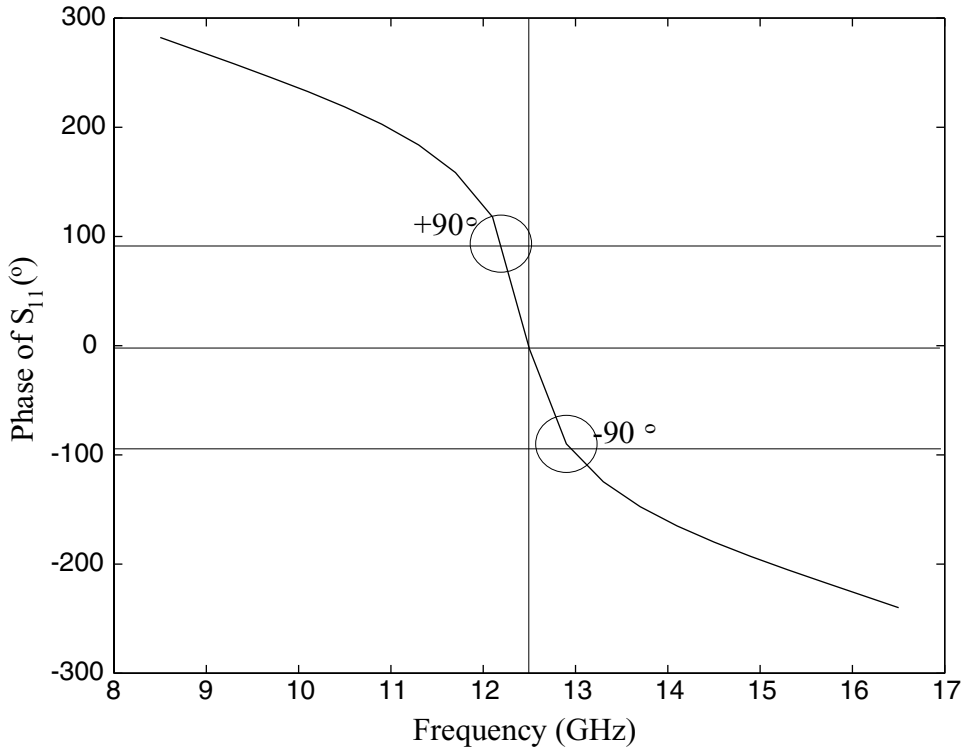


Figure 4.3: Simulated phase of insertion loss for extraction of the external quality factor.

4.2.2 External Coupling

Coupling to a micromachined resonator can be performed with a variety of techniques as analyzed in [47]. The method selected herein is a transition from a microstrip

line to a feeding slot placed on the top wall of the cavity. In contrast to the aforementioned references the feeding microstrip line is not terminated with an open stub. The reason been that the total length of the cavity is insufficient for the creation of a $\lambda_g/4$ open stub. Instead the microstrip line is terminated with a via-hole that connects the line to the ground plane. In order to design for the optimum slot dimensions the external Q of the resonator is taken into account. The external Q can be extracted by looking at the phase of the return loss for a one-port resonator. Using a full wave solver [10] the effects of the feeding lines are deembeded and the simulated phase with respect to frequency is evaluated; one case is presented in Fig.4.3. At the resonant frequency the deembeded curve passes though 0^o phase, and the fractional bandwidth can be evaluated from the $\pm 90^o$ points. Then the external Q can be calculated from:

$$Q_e = \frac{f_o}{\Delta f} \tag{4.9}$$

Based on these results the dimensions of the coupling slot were chosen to be 3 mm by 0.3 mm.

In addition to that, since the measurements will be performed using CPW-based probes, a CPW-to-microstrip line transition needs to be included in the design. As was already mentioned, via-holes are utilized for terminating the feeding microstrip line, thus the ground transfer from the CPW to the microstrip line is performed with vias as well. The final simulated results for the resonator are presented in Fig.4.4 and as can be observed the resonant frequency occurs at 12.7 GHz and the unloaded Q can be evaluated at 450. However, the depicted simulation assumed no conductor losses. If conductor and dielectric losses are introduced in the model the expected value of the unloaded Q is approximately 340.

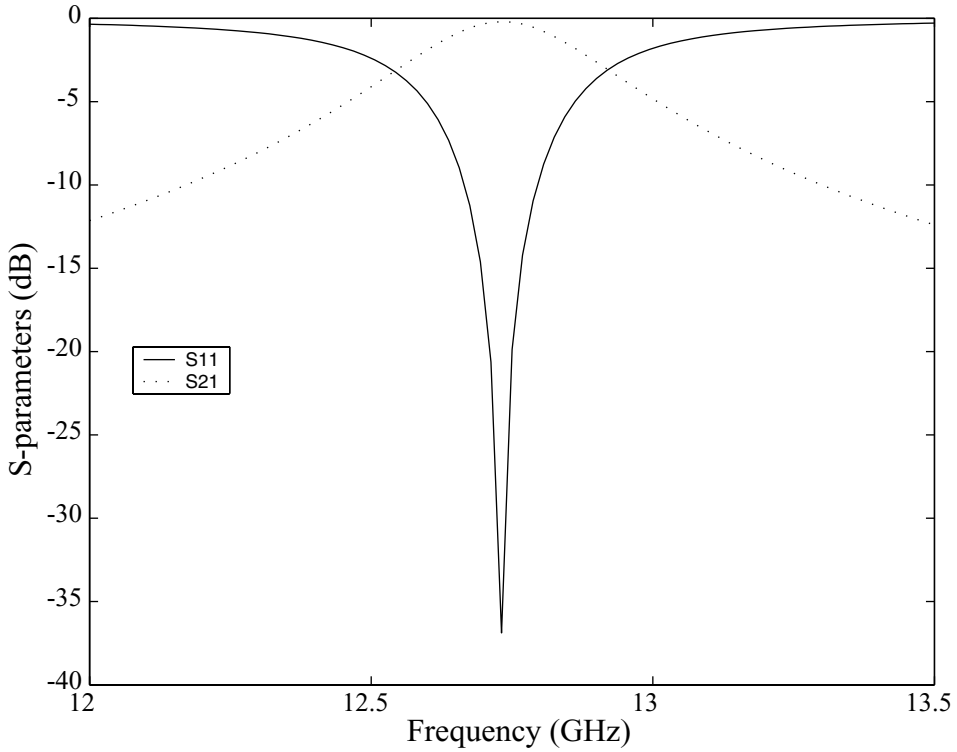


Figure 4.4: Simulated response of one-pole evanescent mode resonator.

4.2.3 Two-pole Filter Design

Following a similar approach a two-pole filter can be designed by intersecting two resonators together. The dimensions of the coupling slots, the capacitive posts and the width of the cavities are kept constant. The only parameter that changes is the distance between the two post which sets the total length of the filter. The post-to-post distance also affects the frequencies where the two poles occur and subsequently the overall bandwidth of the filter. Changing the coupling between the two posts can shift the poles and this is something that can be utilized for tuning the filter at different frequencies. The schematic of the two-pole filter along with its response are presented in Fig.4.5, where the simulated bandwidth is 3% and the bandpass ripple is 0.24 dB.

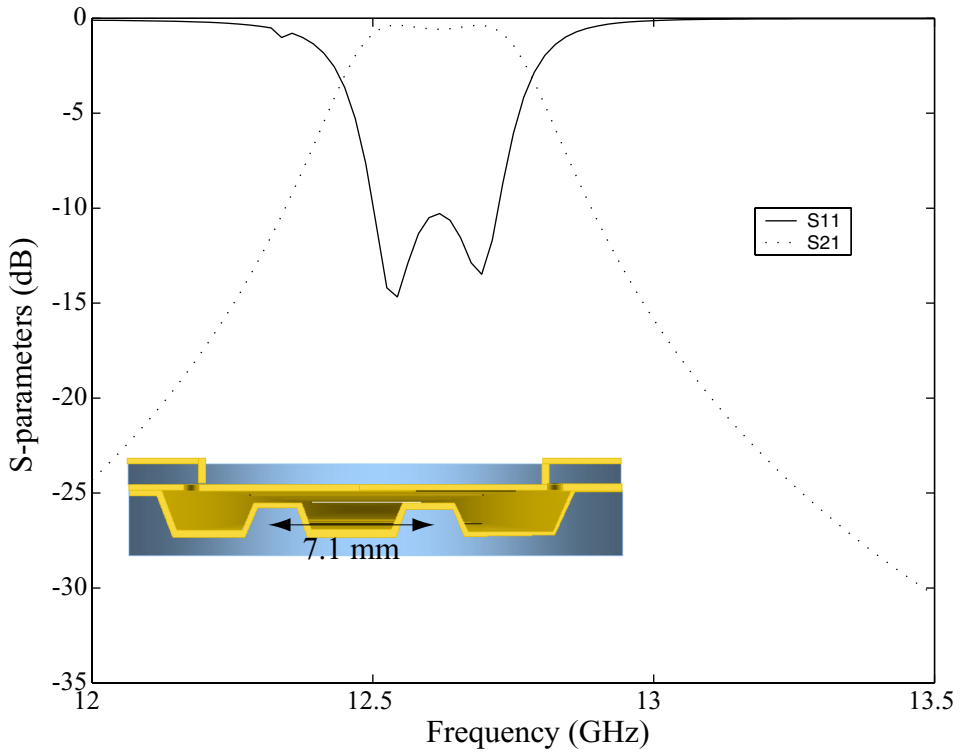


Figure 4.5: Simulated response and schematic of two-pole evanescent mode filter.

4.3 Fabrication Process

Fabrication of the evanescent mode resonators is a multiphase process involving both surface and bulk micromachining. The samples used are one 500 μm and one 100 μm thick high-resistivity double-side polished silicon wafer, with 8700 Å of SiO_2 thermally grown on both sides to allow for dual side processing. On the lower wafer: (a) SiO_2 is patterned on the top side and etched partially in the post region and fully in the remaining cavity using buffered hydrofluoric acid (BHF); (b) the oxide-patterned cavities are etched in tetramethyl amonium hydroxide (TMAH) up to a depth of 440 μm , while the post remains protected by a thin SiO_2 layer; (c) the SiO_2 from the post is striped; (d) the wafers are then placed in TMAH for an additional 10 μm etching, resulting in a 450 μm depth and a 10 μm gap for the post; (e) a 400/800 Å of Cr/Au seed layer is deposited via sputtering in order to ensure uniformity and

subsequently 4 μm of Au are electroplated inside the cavity.

For the top, a 100 μm thick high-resistivity double-side polished silicon wafer, is utilized: (a) 500/9500 Å of Cr/Au is deposited on the back-side using lift-off process to form the coupling slots; (b) SiO_2 is patterned on the top side of the wafer using infrared (IR) alignment and etched fully in buffered hydrofluoric acid (BHF); (c) the oxide-patterned vias are etched in potassium hydroxide (KOH); (d) a seed layer of Cr/Au is deposited via sputtering and subsequently, 4 μm of Au are electroplated to form the microstrip lines; (e) 1000 Å of plasma enhanced chemical vapor deposition (PECVD) SiO_2 is patterned over the location of the post and etched using reactive ion etching (RIE). This thin layer isolates the two Au surfaces (the top wall of the cavity and the post) and prohibits their bonding during the final fabrication step.

The mechanism utilized for accurately aligning the two wafers together prior to the thermocompression bonding will be analyzed in detail in the following chapter. In short, specially designed shapes are etched on both wafers using a deep reactive ion etching (DRIE) ensuring vertical sidewalls. Similarly shaped alignment keys are then placed inside the groves and the two wafers are locked in place. After that, the wafers are placed inside the EV-501 bonder and the filter is created. The bonding procedure will also be described in detail in the next chapter.

Alternatively, the fabrication of such filters can be performed using a deep reactive ion etching (DRIE). This will allow the formation of perfect rectangular posts without the use of compensating structures and will improve the control of the gap between the cavity and the post. Two 500 μm thick Si wafers are initially bonded together using thermocompression bonding. The SiO_2 for the filter cavities is patterned and the wafers are placed in TMAH for a short 10 μm deep etch. This short TMAH etch has the advantage of increased uniformity along the Si wafer. Subsequently, the cavity will be covered by a metal hard-mask for the DRIE etching. This metal can be deposited via sputtering and can then be patterned and etched from the cavity, except

from the region where the post will be located. Patterning the photoresist inside a 10 μm deep cavity can be performed either using a regular negative photoresist or, as will be mentioned in the following chapter, using an electro-deposited solution. The wafers are then placed in the DRIE and are etched for 500 μm. The etch will stop when the metal is revealed, thus ensuring a uniform depth along the filter. The fabrication of the top wafer is identical to the one analyzed previously, therefore after alignment the three wafers are bonded together forming the evanescent mode filter. Nevertheless, for such a process to be successful extensive characterization of the DRIE system is necessary.

4.4 Silicon Micromachining of Convex Corners

4.4.1 Addressing Undercutting of Convex Corners

The formation of a rectangular post inside the cavity has an intrinsic difficulty since the post is a combination of four convex corners. A convex corner is defined as the corner bounded by the fastest etching crystal planes in silicon. The etching of rectangular convex corners in anisotropic etching solutions like potassium hydroxide (KOH) or tetramethyl ammonium hydroxide (TMAH) leads to a deformation of the edges due to corner undercutting [61, 62, 63]. The emerging planes at the convex corners have been determined by various authors as {212} [64, 65], {411} [66, 67], {31x} [65, 68, 69], and {212} [70]. The differences in the reported emerging planes are due to the different solutions that the various investigators used and the different conditions under which they performed their experiments (temperature, solution concentration, steering). As an example Dorsch in [71] demonstrates how the emerging bevelling planes at the convex corners change during the etching due to an increase in the silicon content in the aqueous KOH solution. Initially the {411} planes are revealed but as the silicon contend becomes more than 150 mg/cm^3 the planes approach the

{311}.

One method of reducing the undercut is by adding chemical additives to the etchant [72, 73]. While this technique reduces the undercut rate, it also reduces the anisotropy ratio between crystal planes and may ultimately create problems in the structure development [74, 75]. Another method for preventing corner undercutting is to add special compensating structures at the corners of the mask layout. A variety of structures have already been proposed by researchers in the referenced work, for use with KOH or EDP, however, as was already mentioned, the etching characteristics are severely affected by the conditions of the experiment. Therefore a thorough investigation of such structures for an etching in 25wt.% TMAH at 85^{o}C is necessary. Measured by a variety of methods [76, 77] the etch rate of TMAH (25wt.%,85^{o}C) is 0.5 μm/min while the {111}/{100} etch rate ratio is 0.05. The etch rate of SiO_2 is minimal and measured at 0.1 nm/min. This is the main reason for which the etching of the 450 μm deep filter cavity is performed using TMAH.

4.4.2 Test Results

In order to investigate the characteristics of various compensating structures a test mask is designed and a study is performed aiming at discovering the optimum structure that will allow the formation of rectangular posts. All the compensating structures tested can be designed in such a way at to protect the convex corners for etch depths up to 500 μm. Unfortunately the dimensions of the rectangular post (1x1 mm) and the total width of the evanescent mode cavity limit the possible length of the compensating structures and thus reduce the number of available options. For this study, all the samples are etched in TMAH for depths of 100, 200, 300 and 450 μm respectively. After each etch the samples are inspected using an optical microscope and a scanning electron imaging system in order to evaluate the appropriate dimensions of the compensating structures which can adequately protect the convex

Table 4.1: Characteristics of compensating structures (e: etch depth, all dimensions are in μm)

Compensating Structure	Dimensions
a	d=5e
b	l=5e,d=2e
c	c=2.25e-116.76
d	c=2.25e-116.76,d=3.15e+163.33
e	c=2e,d=3.4e-80
f	c=2.25e-116.76,d=2.1e+14.49

corners. The characteristics of all the compensating structures studied are summarized in Fig.4.6, while Table 4.1 presents the outcome of the experiment. Fig.4.7 is a scanning electron image of a rectangular post after the etching. Four different structures have been used for each convex corner and this explains the differences in the exposed bevelling planes. The only compensating structure compatible with the dimensions of the evanescent-mode resonator that can endure the necessary 15 hours TMAH etch is case (f). For this case a photograph of the created rectangular post after a 450 μm TMAH etch is included in Fig.4.8 where the formation of a well defined rectangular angle is evident.

4.5 Measured Results

The outcome of the fabrication process is presented in the next figures. Initially a scanning electron image of the front side of the wafer is shown (Fig.4.9) including the cpw-to-microstrip transition. As was already mentioned, the coupling from the microstrip line to the filter slot is performed by shorting the signal line to its ground plane. This is done using an appropriate via as illustrated in Fig.4.10. The via is utilized instead of an open stub since the total length of such a stub is very long compared to the evanescent mode cavity. On the backside of the top wafer, two

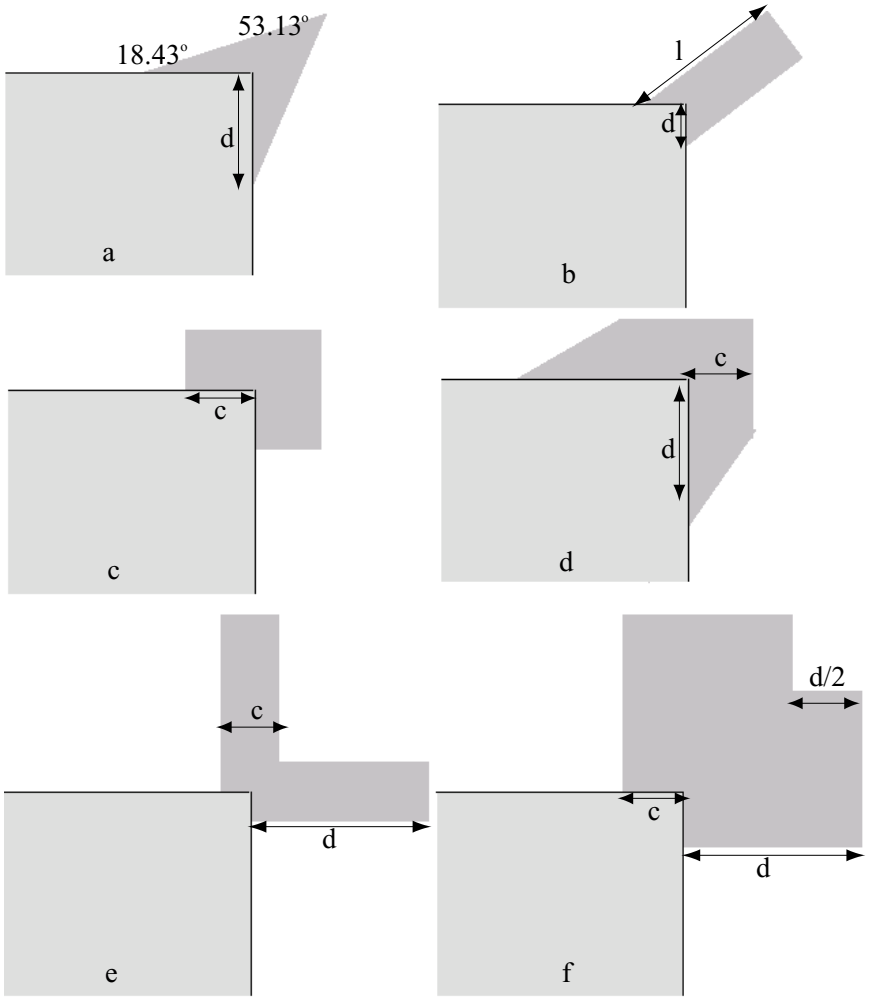


Figure 4.6: Compensating structures for convex corners.

coupling slots have been created as shown in Fig.4.11. Finally, the lower wafer, which includes the 450 μm deep cavity and the capacitive post is presented in Fig.4.12 from where it can be observed that the compensating structure used have sufficiently protected the convex corner.

For the measurements, a HP 8510C vector network analyzer is utilized on an Alessi probe station with 150 μm pitch GGB picoprobes. Through-Reflect-Line (TRL) calibration is performed using on wafer calibration standards. The standards are designed in such a way as to move the reference point 200 μm prior to the ground equalization vias of the FGC lines. Therefore the losses of the FGC-to-microstrip

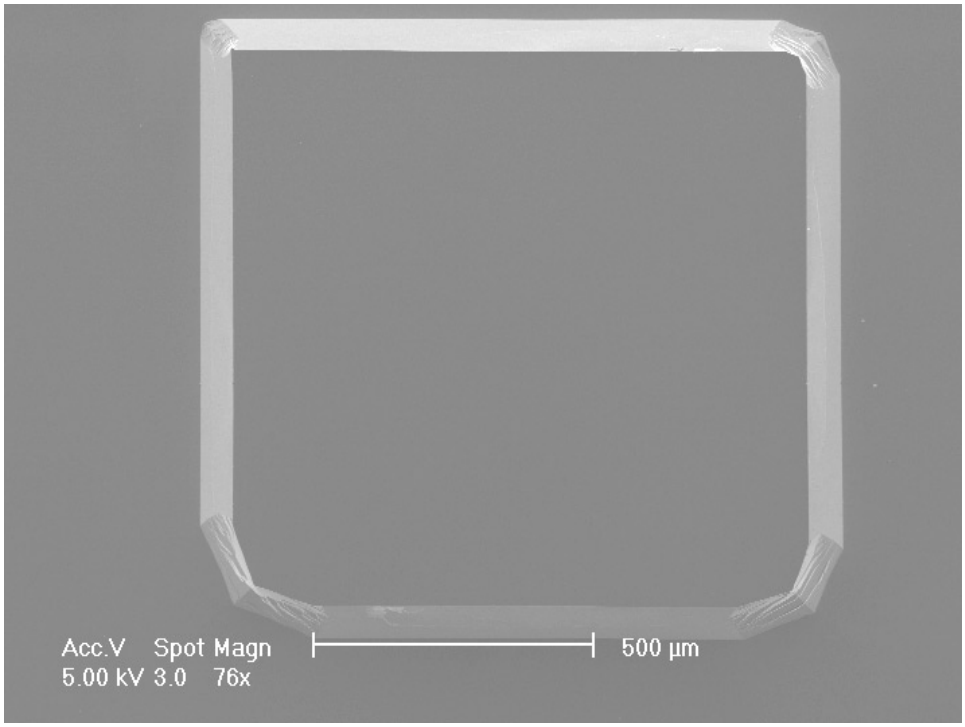


Figure 4.7: Scanning electron image of etched rectangular post.

transition, along with the losses of the microstrip line that feeds the filter are included in the measurements. For the single-pole resonator the results are summarized in Fig.4.13. The resonant frequency occurs at 14.1 GHz, or 1.4 GHz higher than the theoretically predicted value. This means that the gap on the capacitive post is approximately 12 μm instead of the desired 10 μm. The unloaded Q can be extracted to be 310 which is 8.8% lower than the theoretically expected value of 340.

The measured response of the two-pole filter is presented in Fig.4.14, where a 2.7% bandwidth is observed with an insertion loss of 2.1 dB at 13.9 GHz. HFSS simulations including dielectric and conductor losses predicted a bandwidth of 3% with an insertion loss of 1.4 dB at 12.7 GHz, so there are again some minor discrepancies on the total gap of the capacitive posts. On the same wafer, through microstrip lines of various lengths have been fabricated. By measuring their response it is possible to evaluate the loss of each component. It appears that the loss of the FGC-to-microstrip

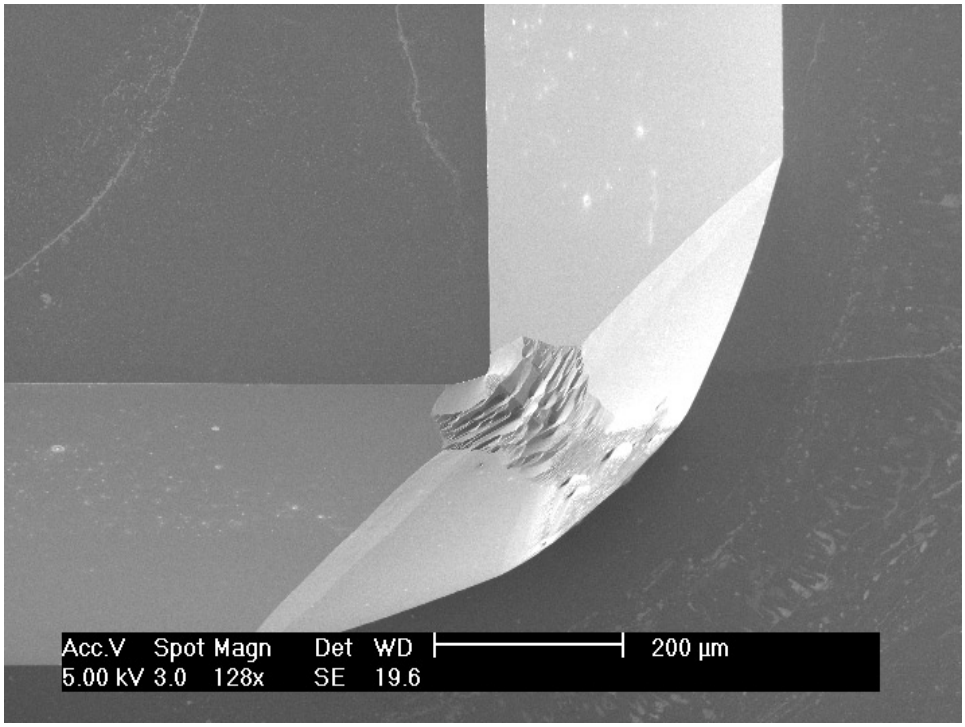


Figure 4.8: Scanning electron image of etched angle at 450 μm.

transition is 0.2-0.3 dB in the bandwidth of operation while the loss of the feeding microstrip, i.e. the line up to the coupling slot, is approximately 0.26 dB at 13.9 GHz. Thus, by taking these losses into account the insertion loss on the filter pass-band is 0.89 dB which is close to the value predicted in Fig.4.5.

The measured results demonstrate a phenomenon that is reported in [78]. The out-of band insertion loss is around 60 dB below and 30-40 dB above the passband. Furthermore, a resonance seems to occur around 15 GHz, which alters the isolation provided by the filter. To further investigate this, a method-of-moment simulation of the top wafer is performed. The cpw-to-microstrip transition, along with the shorting vias and the slot lines are included in the model. The theoretical results and the schematic are summarized in Fig.4.15 where one resonance appears in the 10-20 GHz range. In [78] this is attributed to spurious surface waves launched in the substrate by the FGC-to-microstrip transition. In the case presented here the distance between

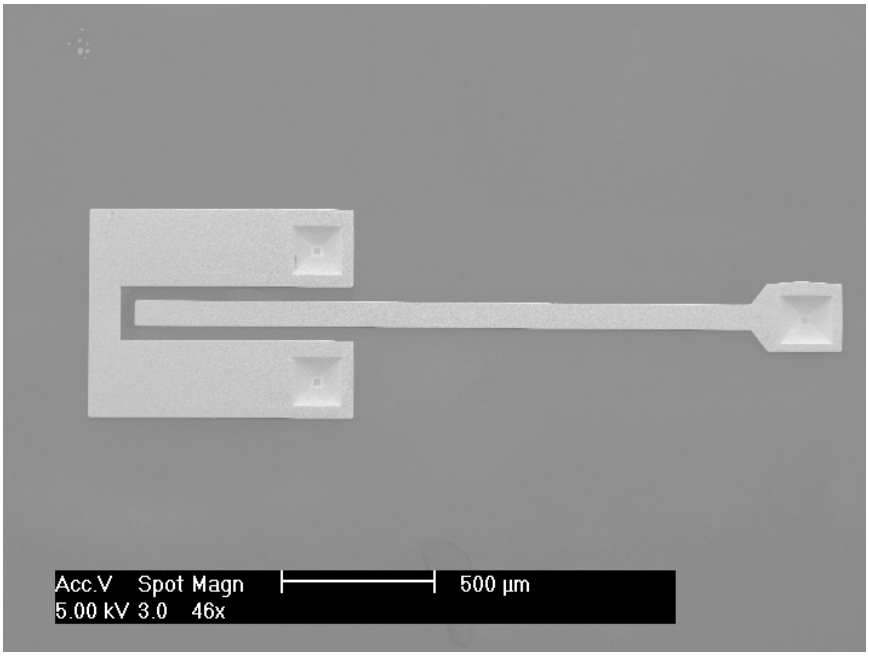


Figure 4.9: Scanning electron image of front side of the wafer. The cpw-to-microstrip transition is presented along with the shorting via.

the two vias shorting the signal line to the ground is approximately 1 cm, which equals half a wavelength for the surface wave mode at 15 GHz (ϵ_{eff} is 1.005). Further research is needed in order to remove all the parasitic resonances from the response. Moreover, as was mentioned in Chapter 2, leaky modes on microstrip lines have been reported for frequencies as low as 5 GHz. Therefore, the feeding microstrip line is another mechanism causing leakage to the surface modes. A suggestion for a possible solution to the problem will be the replacement of the microstrip line with an FGC line coupling to a double slot for feeding the cavity. Such a feeding technique has been used for slot antennas and, if appropriately designed, it could be used for filters.

4.6 Tunable Evanescent Mode Filters

The electrical performance of the evanescent mode resonators and filters is determined by a number of geometrical parameters including the gap between the post

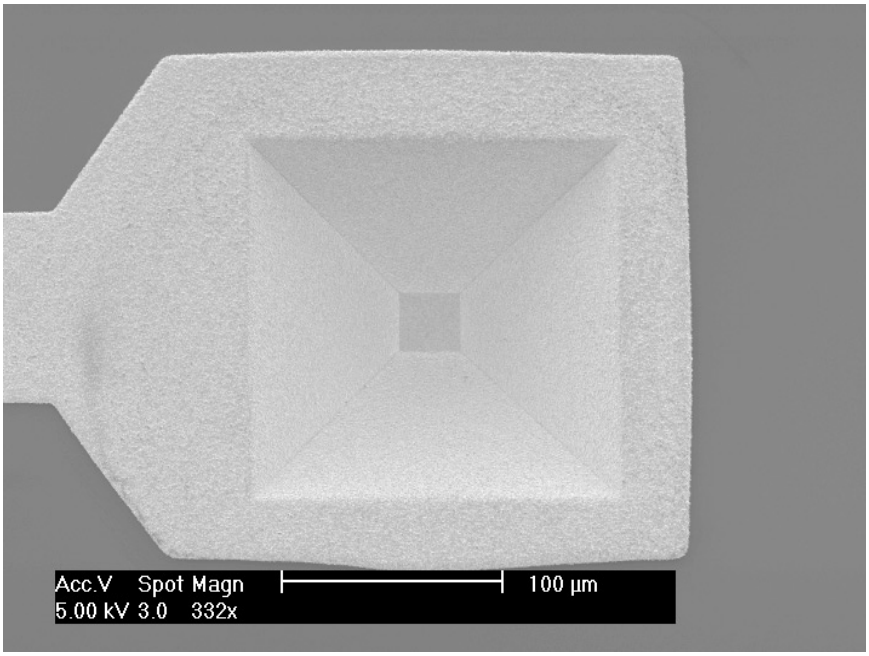


Figure 4.10: Scanning electron image of via transition that connects the microstrip line to the ground plane, thus coupling the RF signal to the filter.

and the cavity, as well as the length of the evanescent sections. These types of filters are characterized by small sizes due to the ability of an excited evanescent wave to vary fast with distance. In fact, as the operating frequency reduces below cut-off, the attenuation constant of each evanescent mode increases forcing the field to vary exponentially versus distance in a way similar to static fields. This property may be used to tune the filters since small variations in the geometrical characteristics of the cavity caused by appropriately located MEMS devices can result in large variations in the center frequency and bandwidth. Electronic tuning of the filters with MEMS requires placement of the switches in locations where small changes in dimensions will cause large changes in electrical performance. In addition, the same capability can be utilized to explore other functions such as frequency hoping and switching. To satisfy these requirements MEMS should be placed at low-Q positions within the filter, specifically near evanescent mode cavities. There are two main mechanisms which could be utilized for tuning the filter: tuning of the capacitive post and tuning

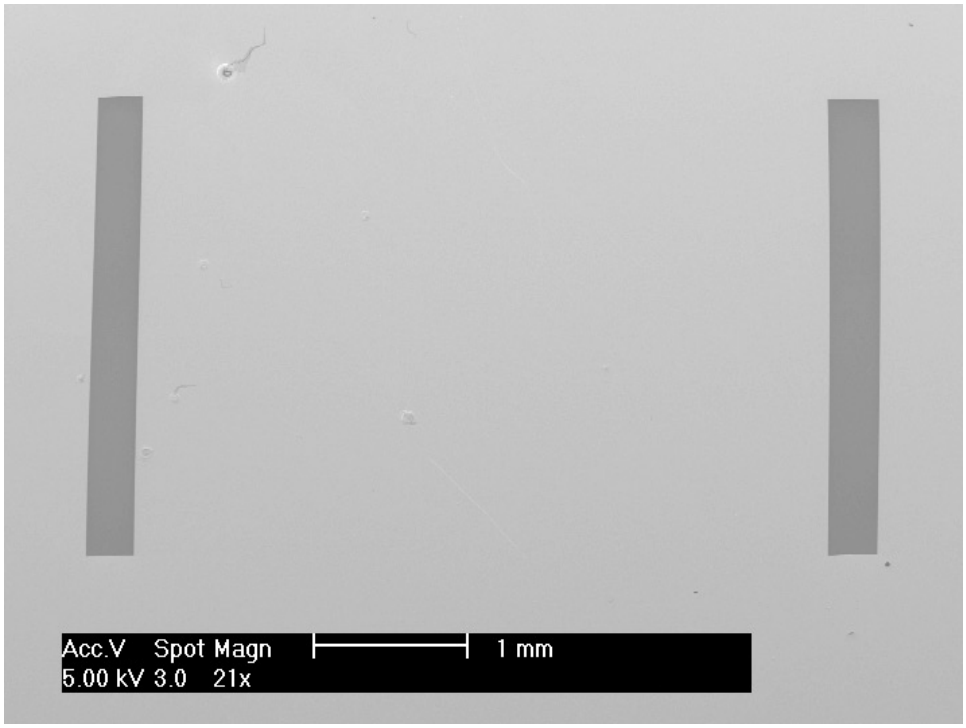


Figure 4.11: Scanning electron image of back side of the wafer. The two coupling slots are presented.

of the coupling slots.

4.6.1 Tuning of the Capacitive Post

The capacitance introduced by the metallized pyramidal post integrated inside the filter can be electronically varied. A membrane diaphragm appropriately located can adjust its position and distance from the top of the pyramid by use of a DC bias voltage between the electrode of the diaphragm and the cavity metal. In this way the gap can be altered by a substantial percentage resulting in considerable tuning of the filter center frequency and out-of-band performance as can be seen in Fig.4.16. Also, when the diaphragm collapses on the post, the filter is switched off. Such architectures can provide very reliable switched filters and diplexers. The MEMS device shown in Fig.4.17 can be employed when small deflections are required. In addition to that

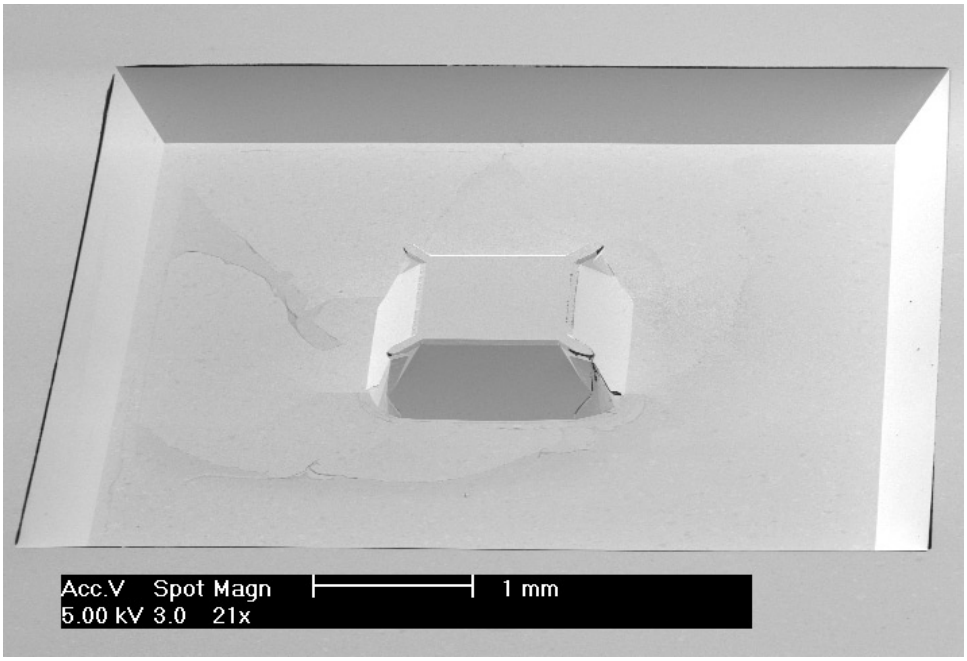


Figure 4.12: Scanning electron image of the cavity wafer.

a third electrode placed outside the cavity of the filter can be utilized in order to increase the range of motion.

4.6.2 Tuning of the Coupling Slots

A second mechanism for tuning the filter response is the use of MEMS switches to electronically alter the length of the coupling slots. Such a device, shown in Fig.4.18, can be a capacitive or metal-to-metal type of switch, mounted on top of the slot that couples the input and output microstrip lines to the evanescent mode cavity. When the switches are in the down position their large capacitance can effectively shorten the length of the slot and considerably influence the coupling. Of course some leakage will always occur and therefore extensive analysis is necessary in order to find the optimum locations for the MEMS. Furthermore, slots can be used for controlling the coupling between the capacitive posts (Fig.4.19). An auxiliary evanescent mode cavity coupled through a slot to the main filter can be created. By electronically

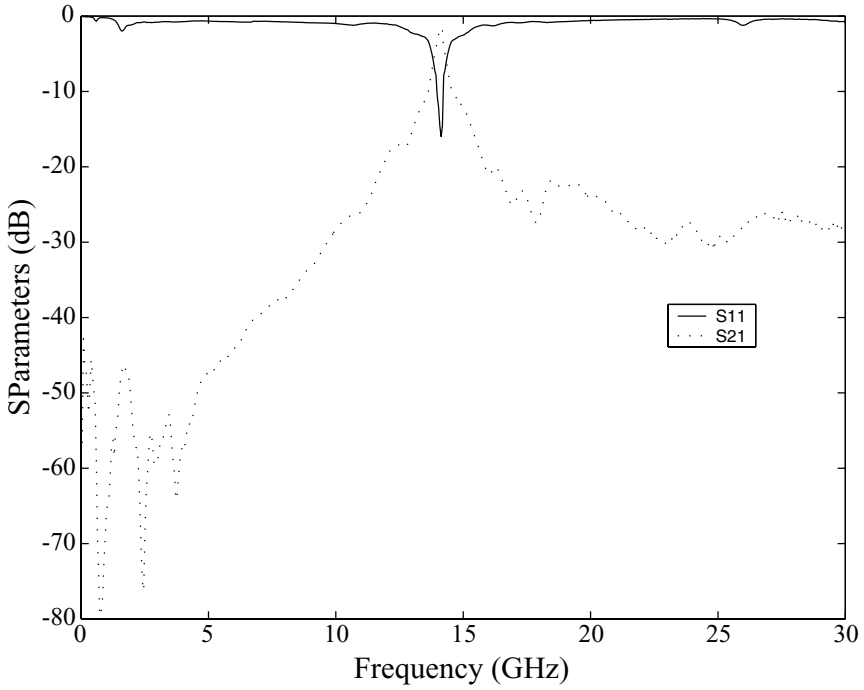


Figure 4.13: Measured response of evanescent mode resonator.

varying the length of the slot, the internal coupling between the posts is altered. The necessary steps for designing and fabricating a MEMS device inside the filter cavity are complicated. However, the problem is almost identical to creating an on-wafer package for a MEMS device. Such an architecture will be presented in the following two chapters, demonstrating the ability to fabricate and operate MEMS devices inside sealed cavities.

4.7 Conclusions

In this chapter a silicon micromachined evanescent mode resonator is presented. The resonator demonstrate an unloaded Q of 310 at 14.1 GHz. The design is then extended to a two-pole filter with a bandwidth of 2.7% and an insertion loss of 2.1dB at 13.9 GHz. In order to fabricate these structures an extensive investigation of compensating structures for convex corners is undertaken. These structures can

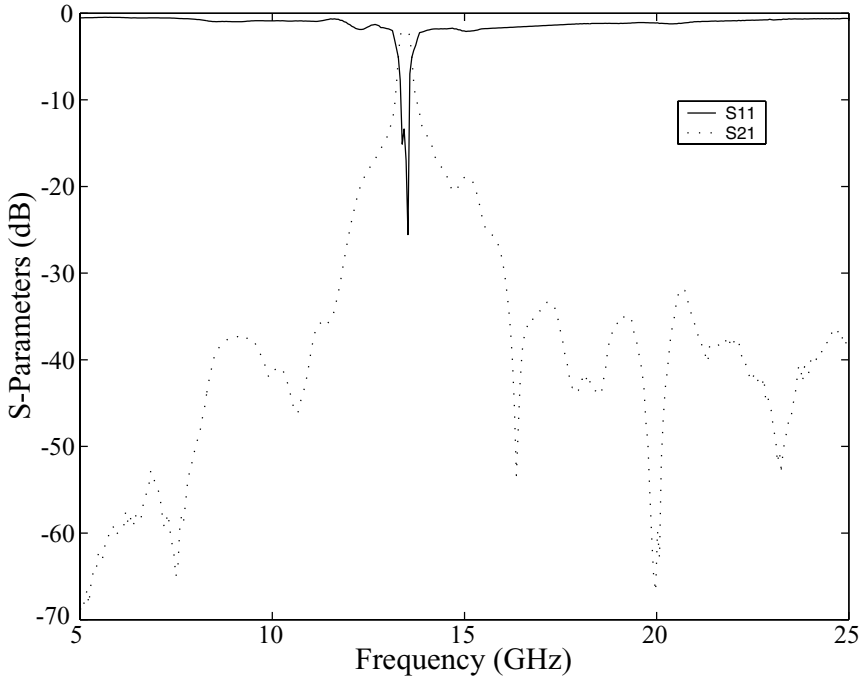


Figure 4.14: Measured response of evanescent mode two-pole filter.

adequately protect the four corners of the rectangular capacitive post for etch depths up to 450 μm. Furthermore, the possibility of tuning an evanescent mode filter is investigated. Such a tuning can be performed by using MEMS devices located either on top of the capacitive post or on top of the coupling input and output slots. Preliminary theoretical results are also presented.

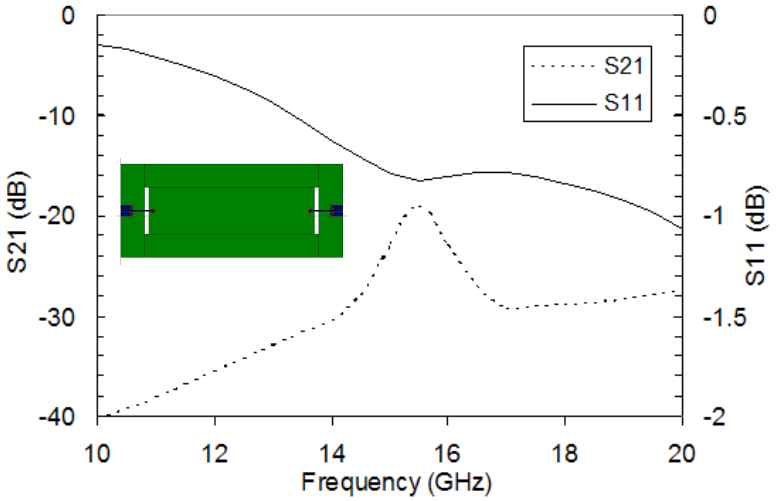


Figure 4.15: Simulated results of top wafer, including cpw-microstrip and microstrip-slot line transition.

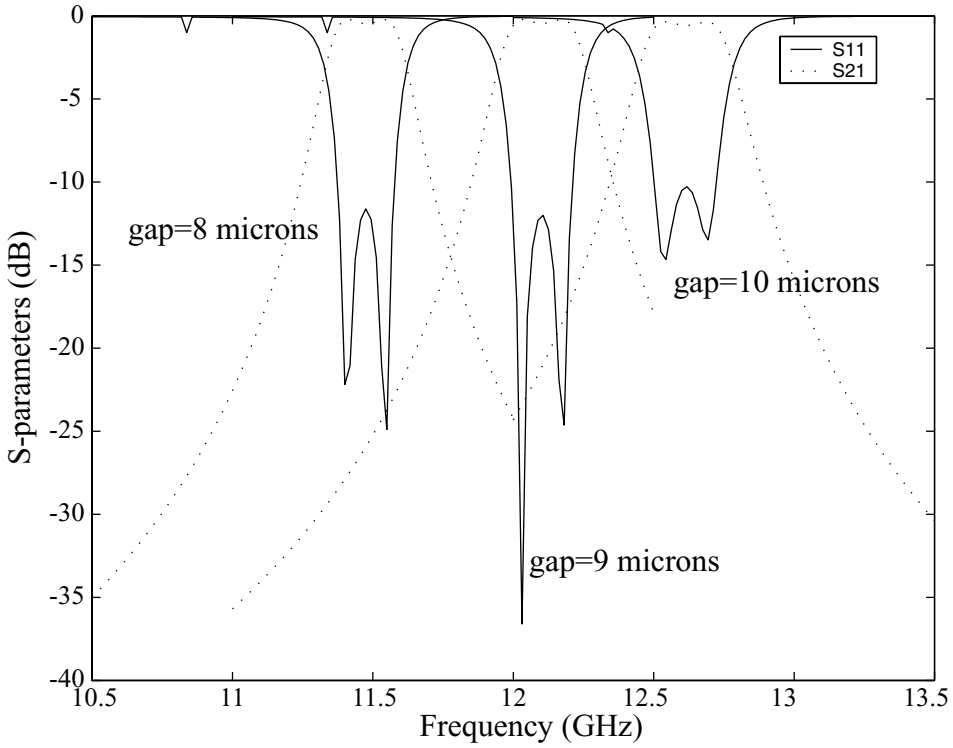


Figure 4.16: Simulated response of tunable evanescent mode filter.

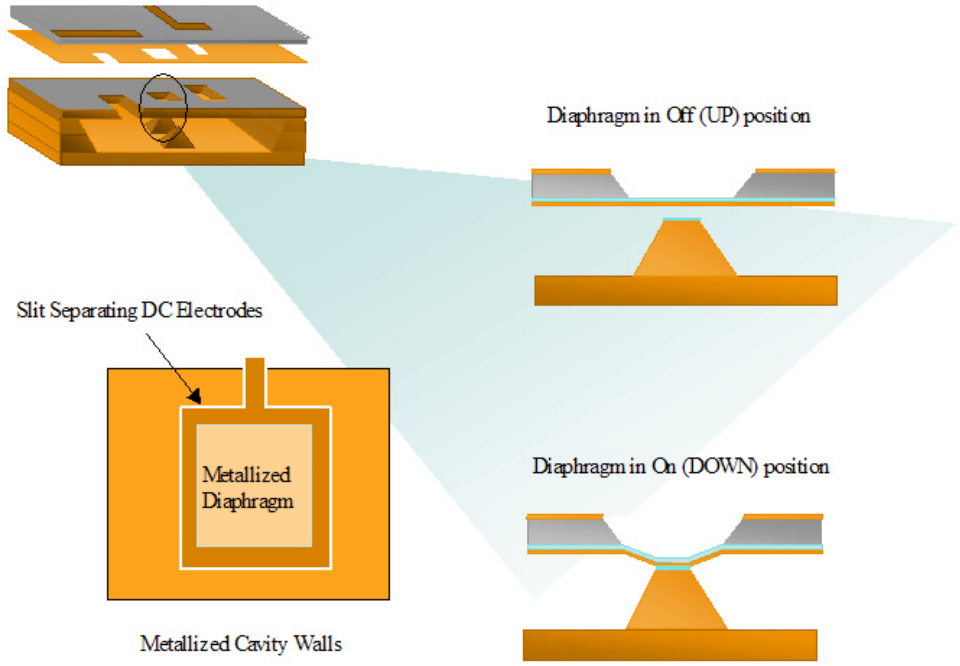


Figure 4.17: Schematic of the proposed tuning mechanism.

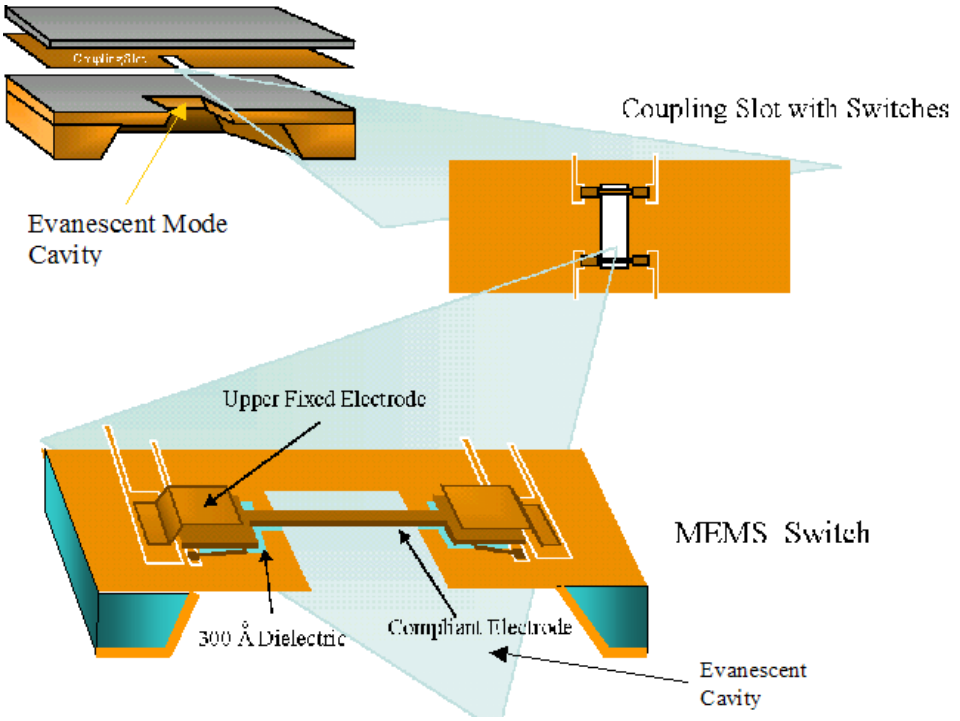


Figure 4.18: Schematic of the proposed tuning mechanism.

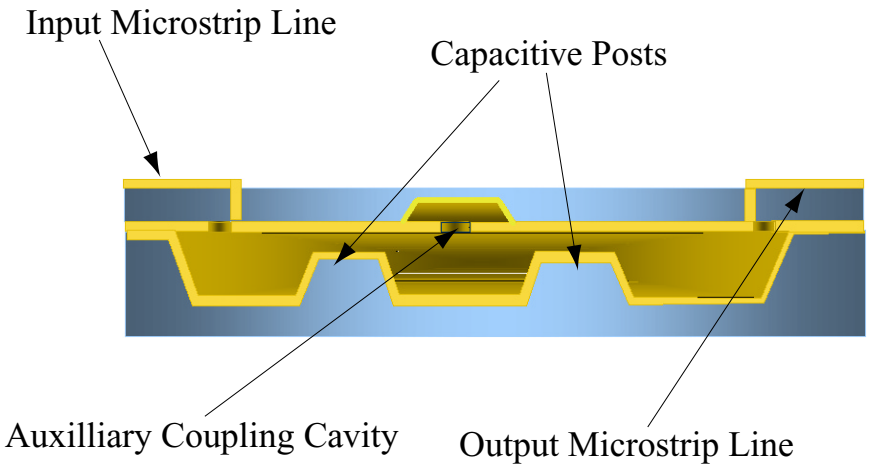


Figure 4.19: Tuning an evanescent mode filter via an auxiliary cavity.

CHAPTER 5

Silicon Micromachined Packages for RF MEMS Switches

5.1 Introduction

5.1.1 RF MEMS Switches

IN the last decade, the maturity of surface and bulk micromachining techniques, which are mainly applied to silicon, enabled the development of microelectromechanical systems (MEMS). These are small devices, which are typically used as sensors and actuators in a wide variety of applications. In the RF area MEMS are mainly used as switches that utilize mechanical movement to achieve a short or an open circuit in a RF transmission line [79, 80, 81]. Such devices demonstrate remarkable advantages over their solid-state counterparts (p-i-n diodes or FET switches): near-zero power consumption, very high isolation, low insertion loss, highly linear response and very low cost. Nevertheless, MEMS are relatively slow compared to p-i-n diodes, are incapable of handling high power due to self-actuation, and they require high actuation voltages (20-80 V). Additionally, reliability is still low and packaging is a very complicated and costly issue.

RF MEMS switches are the specific microelectromechanical switches that are de-

signed to operate at RF-to-millimeter-wave frequencies (0.1 to 100 GHz). The forces required for the mechanical movement can be obtained using electrostatic, magnetostatic, piezoelectric, or thermal designs. To-date, only electrostatic-type switches have been exhibited at 0.1-100 GHz with high reliability (100 million to 10 billion cycles) and wafer-scale manufacturing techniques. RF MEMS technology can find a large number of applications in the design of phased arrays for radars and communication systems, in switching and reconfigurable networks, and in low-power oscillators and amplifiers.

A low actuation voltage RF MEMS switch has been developed [82] and tested recently to demonstrate actuation voltages as low as 6 Volts with an on-to-off capacitance ratio of 48. Power handling measurements show no "self-biasing" or failure for power levels up to 6.6 W [83] while, RF measurements demonstrate an isolation of -26 dB at 40 GHz, which can be tuned by appropriately adding inductive beams [84]. The operation of the RF MEMS switch requires DC as well as RF interconnects which carry the DC voltage and RF current from the probe pads to the device. The MEMS air-bridge in the off position is suspended approximately 3 μm on top of the finite ground coplanar waveguide (FGC) line. Therefore its capacitance is relatively small, in the order of 30-40 fF, and allows the RF signal to pass though the line. In order to actuate the switch a dc bias voltage is applied between the air-bridge of the switch and the ground plane of the FGC line. This electrostatic voltage pulls down the switch and increases significantly the capacitance on the line to approximately 1-1.7 pF and this capacitance effectively blocks any RF signal from passing through the FGC. The demonstrated down capacitance of the switch depends on the area of the actuation pads and the thickness of the silicon nitride dielectric layer used.

5.1.2 Packaging Techniques

Integrated circuit (IC) packaging and its testing has evolved over the past years due to the maturity of the IC industry, the availability of a highly advanced infrastructure , and the wide applications of the integrated circuits. The package has four major functions [85]:

1. *Signal distribution*, involving mainly topological and electromagnetic considerations.
2. *Power distribution*, pertaining to electromagnetic, structural, and material aspects.
3. *Heat dissipation (cooling)*, involving structural and material considerations.
4. *Environmental protection*, providing mechanical support and isolating the chip from harsh conditions (radiation, high temperature, humidity).

Arguably the thin-film interconnections within semiconductor IC chips are an important packaging component. All these interconnects are not considered packaging in the common parlance. The packaging begins at the interface of these ICs and other components. This is considered as the first-level package, where an IC chip and its interfaces are enclosed in a single-chip module (SCM). Groups of multiple SCMs, along with other components such as resistors, capacitors, filters can be attached onto various substrates or boards, thus constituting the second-level packaging. The third-level packaging may be the outer shell of a portable device.

Millimeter wave systems for commercial, scientific or military applications are rapidly emerging requiring development of high-frequency packaging technologies. For high-density, high-frequency (5-100 GHz) packages the performance requirements are very stringent, since poor design and fabrication can lead to increased cavity resonances and cross-talk between neighboring circuits [32]. Many materials can be utilized for packaging including plastic and alumina which offer low cost, both, however, suffer from poor electrical performance at frequencies beyond 10 GHz. Silicon

on the other hand has been extensively used and studied in the electronics industry [86]. Its electrical properties have enabled the semiconductor industry to use it as the primary dielectric material in developing ICs while the mechanical properties of Si have been utilized since 1950's [87, 88] to develop high performance MEMS structures. These two properties in addition to the thermal characteristics of Si make it an appealing candidate for packaging high-frequency circuits.

As the packaging technology matured over the years the techniques used for interconnecting the chips evolved from wire bonding, to tape automated bonding (TAB) and to Flip-chip bonding [89]. For RF applications, such as the ones addressed in this study, the performance of the interconnects is of major importance in characterizing the overall quality of the package. For 5-100 GHz operation, it is best to use RF transitions based on via holes (wide-band designs) or on electromagnetic coupling though the wafer (20-30% bandwidth). Already existing designs [90] offer a wide bandwidth of operation having an insertion loss of 1.5 dB at 25 GHz (including a 3000 μm though line) and a return loss, which is lower than -10 dB up to 30 GHz. However, this package is fabricated in alumina and therefore the connection of a Si or GaAs chip inside the package using wire bonding will further degrade its performance. Silicon on-wafer packaging using micromachining is a very appealing alternative, since it can combine the fabrication of a wide variety of passive or active components with the RF vertical interconnects and the packaging cavity in a single wafer. Thus, it eliminates the need for wire bonding or solder bumps, which reduce the operational bandwidth due to unwanted parasitics.

The fabrication techniques used in packaging from the IC industry can be carried over to MEMS devices. However, the requirements of MEMS packaging are different from those of the IC packaging. MEMS packaging is application specific, and different designs are needed for different applications. The packaging technique used is probably the most critical part of RF MEMS. It is the most expensive step in the

fabrication process and will ultimately determine the performance and longevity of the device. A common practice for packaging MEMS devices is to bond a recessed cap onto a micromachined wafer. However, conventional wafer bonding techniques (fusion and anodic bonding [91, 92]) cannot be employed when temperature-sensitive materials are used due to the high temperatures involved in these processes. This problem prompted researchers to investigate low temperature bonding techniques. Unfortunately these new bonding methods depend highly on the bonding material, surface treatment and surface flatness [93], although localized heating can be used to overcome these difficulties [94].

5.1.3 Previous Work in Three-Dimensional Interconnects

Silicon micromachining has been applied to many microwave and millimeter-wave circuits, and has introduced new methods of vertical integration. To this effect, a micromachined three-via interconnect has been developed and fabricated for CPW-based circuits providing signal transfer through a silicon wafer [95]. The two finite grounds have been connected at the end of the line to short-circuit any undesired horizontally polarized wave, launched due to the open-end effects. The presence of the short requires a quarter-wave CPW stub (thus, limiting the bandwidth of the transition to approximately 10%) to provide an RF open to fields that would tend to propagate horizontally pass the via structure. Furthermore, to cancel the inductive behavior of the via and improve the return loss, a capacitive bridge has been introduced right before the via structure. Measured results for a back-to-back transition showed a 1.82 dB insertion loss and -30 dB return loss at 94 GHz. After accounting for the loss of the FGC feeding lines, the loss due to each transition is approximately 0.6 dB, from which 0.2 dB is attributed to radiation losses and 0.4 dB to ohmic losses.

Similar to the single-layer transition, a multilayered transition may be performed

by cascading multiple transitions. To achieve such a cascade, direct contact transition from one side of a wafer to the facing side of an adjacent wafer needs to be included. This can be done with an extended section of FGC line electroplated to a specified height above the rest of the circuit metal to form three gold bumps. When this is done on facing sides of two silicon wafers, contact is achieved using thermal compression. Measured results presented in [96] demonstrate an insertion loss of 0.32±0.02 dB from 90 to 98 GHz, with return loss below -30 dB. Subtracting the line loss from the total insertion loss yields 0.23±0.03 dB loss for the two wafer-to-wafer transitions.

An alternative approach for performing vertical transition in silicon wafers is to develop lines that provide access to both the top surface and the depths of a silicon micromachined wafer. The patterning of the lines inside the cavities is executed using a special technique developed at the University of Michigan [97] which allows the formation of multilevel FGC lines. These transitions have an average insertion loss of less than 0.08 dB across the 2-40 GHz frequency range and are extremely compact, therefore they are very appealing for high-density packaging schemes.

5.1.4 On-Wafer Packaging for RF MEMS Switches

Contrary to the existing MEMS packaging technologies presented in the previous sections, an on-wafer approach is characterized by the fact that the RF MEMS device and its packaging structure are fabricated on the same wafer thus eliminating the need of wire-bonding transitions. The two factors that prohibit the use of commercially available packages for RF MEMS devices are cost and performance. Specifically, the manufacturing cost of a ceramic package outweighs the cost of the MEMS device by a few orders of magnitude. Additionally, the insertion loss of this package is much higher than the insertion loss of the MEMS device and deteriorates with frequency due to high parasitic inductances introduced by the transition between the package and the chip. Furthermore, these 1st level packaging schemes require chip mounting

and therefore are susceptible to thermomechanical failures and fatigue due to thermal mismatches, creep and delamination.

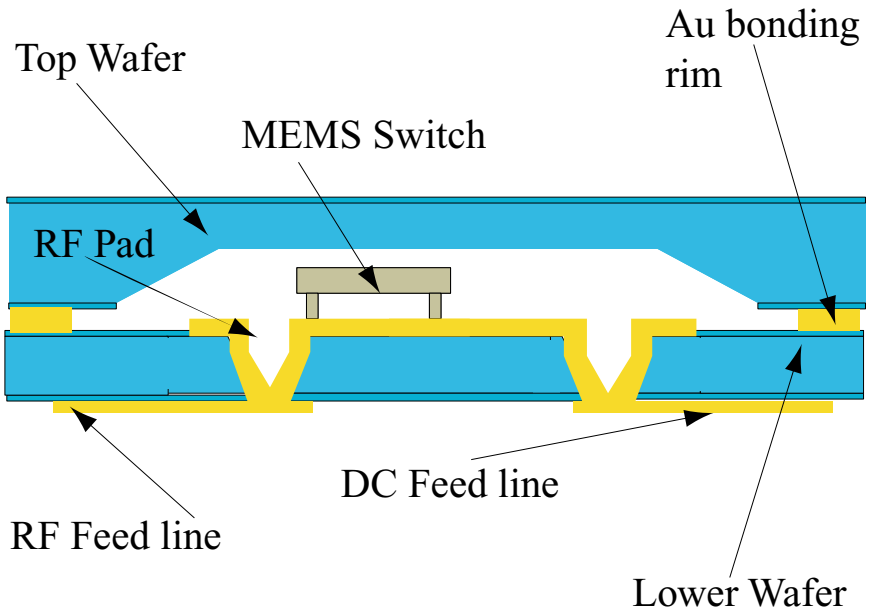


Figure 5.1: Schematic of packaged RF switch with DC and RF via transitions.

In the proposed architecture two high resistivity silicon wafers, which are aligned and bonded to provide the required environmental control, are utilized for the package. The package incorporates both DC and RF through-wafer transitions designed to operate well for their respective DC and RF signals. The DC and RF pads are printed on the opposite side of the Si wafer that carries the switch (Fig.5.1) and are then transitioned via appropriate through-wafer transitions [37]. This technique for transitioning inside the package reduces the required number of interconnects for accessing the encapsulated RF MEMS to a minimum.

This point can be clarified with a conceptual schematic of a tunable microstrip patch antenna array or a tunable frequency selective surface (Fig.5.2). Packaged RF MEMS are necessary for tuning the antenna. Two methods for placing these devices are presented in the graph. In the first option, the MEMS are mounted via flip-chip on top of the wafer. This will require an additional transition from the patches to

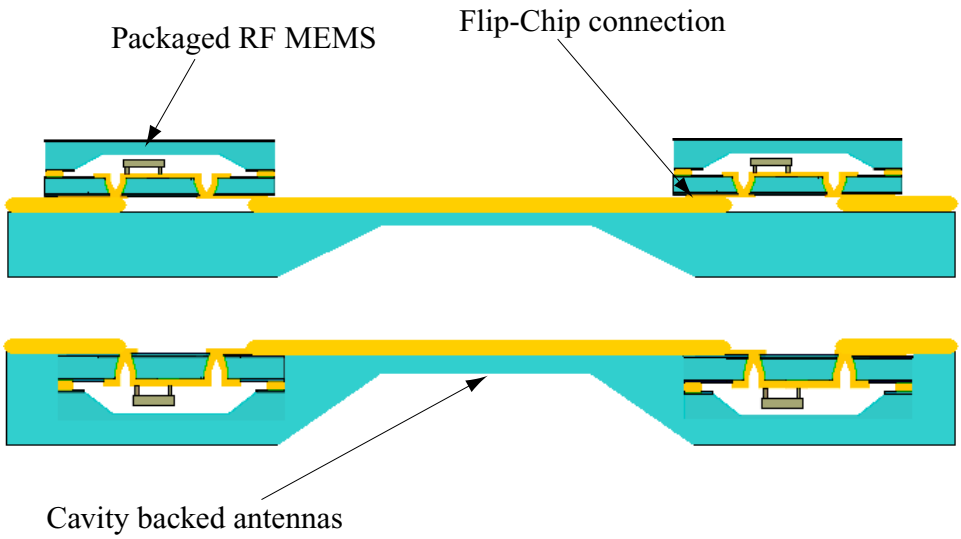


Figure 5.2: Schematic of a tunable patch array using packaged RF MEMS.

the switches which can be performed by electroplating a gold bump on the opposite sides of the wafers to be connected and then bond them together. Such a technique has been demonstrated for W-band operation and can be easily scaled down to Ka-band [96]. However, even though this transition has a very good performance, it will degrade the overall system. The optimum solution is presented in the lower part of the figure. There, the MEMS devices are printed on the back side of the wafer that holds the patch antennas. The metal of the patch acts as the backside for the via-hole transitions. Subsequently, a second thicker wafer is utilized for creating both the packaging cavities for the MEMS and the backside cavities for the antenna elements. Using such a technique, the required interconnects for accessing the devices are kept to a minimum, while the tuning elements are placed on the backside of the antenna. Therefore, any parasitic influences to the near field and pattern of the antenna are removed. Similarly, on-wafer packaged RF MEMS can be used for tuning filters, amplifier matching networks or phase shifters, thus offering an extremely compact system-on-a-chip with excellent RF performance.

This chapter will start with a description of an initial attempt to create an on-

wafer packaging scheme on micromachined silicon wafers. The attempt is successful, but the RF response of the package needed improvement. Therefore, a second design is created, where attention is focused on the effects caused by the via discontinuities. Additionally, a fabrication process that allows the formation of FGC lines along the depths of a micromachined cavity and along its sidewalls is investigated.

5.2 Initial Attempt for Packaging of RF MEMS

5.2.1 Design Process

The most important component for constructing an on-wafer package is designing a RF transition with low insertion and return loss. Until recently the main target for package designers was to keep the return loss below -10 dB. However, the importance of insertion loss has risen significantly over the last decade, since the popularity of low-loss devices such as MEMS increased. A via-hole transition for FGC components has already been designed for W-band operation [95]. This transition uses a short stub for tuning the response at 94 GHz and additional capacitive air-bridges for matching the parasitic inductance. In the initial attempt to create an on-wafer package this transition has been used as a guide. The use of a short stub has been rejected since its length is prohibitive ($\lambda_g/4$ at 20 GHz equals 1518 μm). Additionally, a 10% bandwidth at 20 GHz is extremely narrow for any practical purpose. Instead an open stub is utilized for tuning the response at 20 GHz, which is selected as the target frequency [98].

For the RF transition a 50 Ω FGC line (50-80-50 μm) expands to a much wider 50 Ω FGC line (90-220-90 μm) in order to allow for the anisotropic etching of the vias. The transition has been designed using a method of moments code [13] and optimized for low loss in K-band. Furthermore, no capacitive air-bridges are utilized, since it is necessary to keep the backside of the wafer planar. The sealing of the

package is provided by a gold ring surrounding the RF transition and the DC bias vias. This being the first time this fabrication process is attempted, it is decided to keep the bonding ring as far from the transition as possible in order to facilitate the lithography.

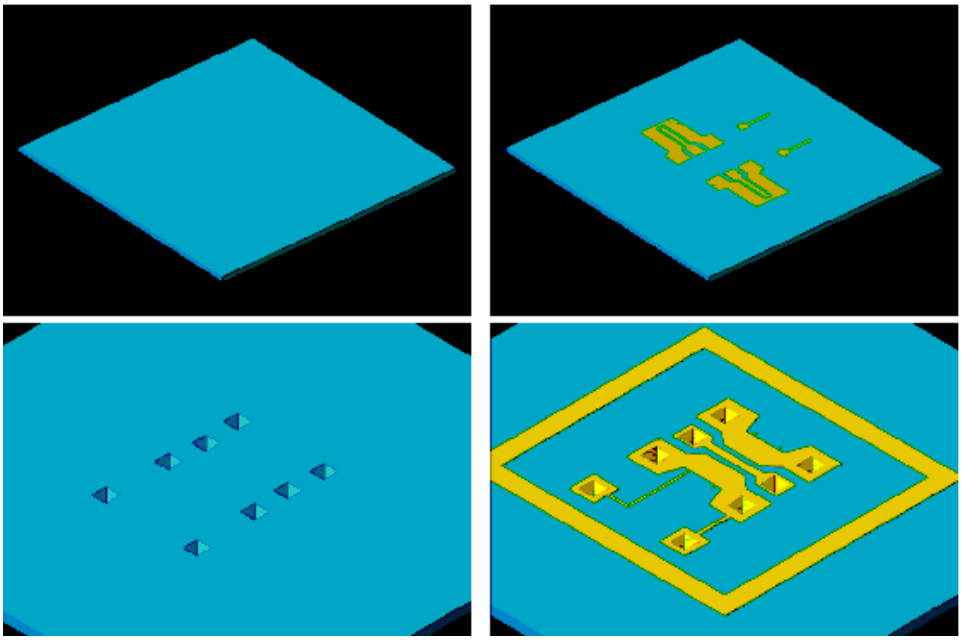


Figure 5.3: Fabrication process of lower silicon wafer.

5.2.2 Fabrication Procedure

The fabrication process involves the combination of two separate procedures. One designed for the RF transition and a second designed for the MEMS switch. These processes were independently designed and combining them is not a trivial matter. Many steps needed to be reconsidered in order to be compatible with subsequent parts of the fabrication. A 100 μm thick high-resistivity double-side polished silicon wafer with 8700 Å SiO_2 on both sides is used. On the lower wafer:(a) 500/9500 Å of Cr/Au are deposited using lift-off process; (b) SiO_2 is patterned on the top side of the wafer using infrared (IR) alignment and etched fully in buffered hydrofluoric acid

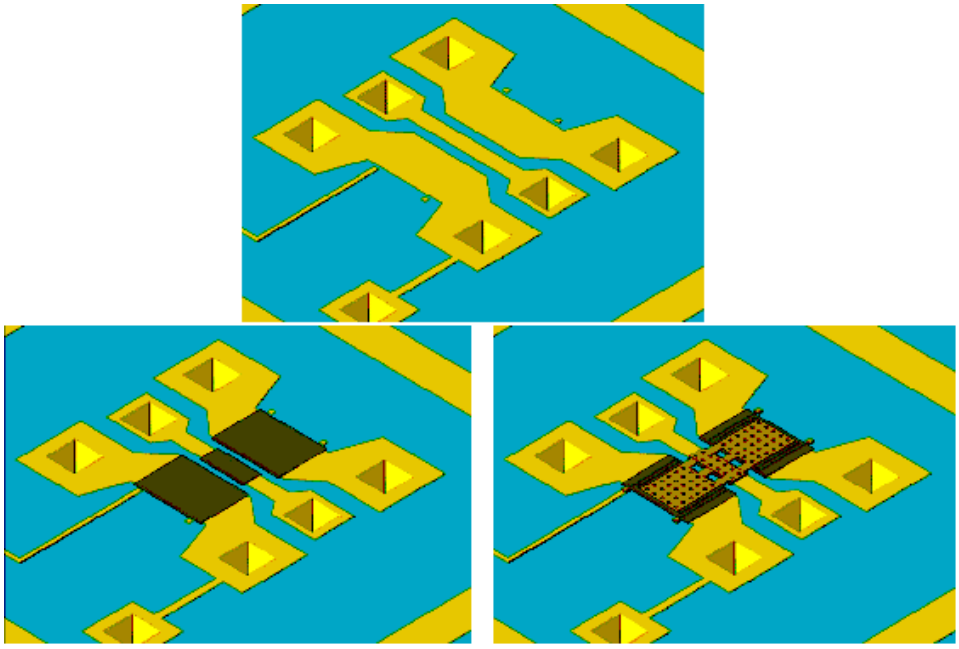


Figure 5.4: Fabrication process of RF MEMS.

(BHF) at a rate of 1000 Å/min ; (c) the oxide-patterned vias are etched in potassium hydroxide (KOH) at an etch rate of 30 Å/hour; (d) using a modified lift-off technique, simultaneous metallization of surface patterns and vias can be achieved. Along with the circuit metal a square ring is patterned around each circuit in order to be used for thermocompression bonding (Fig.5.3).

The second step is the fabrication of the MEMS switch. The original fabrication process presented in [99] is appropriately modified for compatibility with the via process. On the aforementioned wafer: (a) 2000 Å of plasma enhanced chemical vapor deposition (PECVD) silicon nitride is patterned over the location of switch actuation; (b) a sacrificial layer of 3μm thick polyimide DuPont PI2545 is spun cast, soft baked, and patterned for anchor points; (c) 2 μm of Ni is electroplated to define the switch structure; (d)sacrificial etching of the polyimide layer and supercritical CO_2 drying and release of the switch structure are performed. The outcome of the process is shown in Fig.5.4 and Fig.5.5.

A 400 μm thick Si wafer is used to create the packaging cavity on the top wafer. A lift-off process is used for the metallization of Cr/Au (500/9500 Å) in order to fabricate a square metallic ring on the lower side of the wafer. SiO_2 is patterned on both sides of the wafer using infrared (IR) alignment to define cavities and probe windows for the final alignment prior to bonding. The SiO_2 is etched partially or fully in buffered hydrofluoric acid (BHF) at a rate of 1000 Å/min. The final step is to anisotropically etch the oxide-patterned cavities and probe windows in potassium hydroxide (KOH) at an etch rate of 30 Å/hour (Fig.5.6).

Thermocompression bonding of the two wafers is achieved using an Electronic Visions EV 501 Manual Wafer Bonder. The samples are aligned together using the probe windows and fabricated alignment marks. Once aligned the wafers are clamped together in the bond fixture and are heated to 350^o Celsius. 200 N of force is applied for 30 minutes on the samples in order to achieve proper adhesion.

5.2.3 Measured Results

The packaged switch is presented in Fig.5.5 where both wafers are shown. In Fig.5.7 the MEMS switch wafer is presented. The DC vias are connected to the FGC ground plane and to the switch anchor points, while the distance between the RF vias and the switch is 200 μm. In Fig.5.8 the measured response of the vertical transition is displayed. For the measurements, a HP 8510C vector network analyzer is utilized on an Alessi probe station with 150 μm pitch GGB picoprobes. Through-Reflect-Line (TRL) calibration is performed using on wafer calibration standards fabricated in conjunction with the circuits to be tested. Multical, developed by NIST, is used to implement the TRL calibration [15]. After deembeding the loss of the FGC feeding line the transition demonstrates a 0.2 dB insertion loss, a 32 dB return loss at 20 GHz and a 55% bandwidth. Thus, the loss due to each transition is approximately 0.05dB. One hundred circuits are fabricated with 94% yield and tested with very similar and

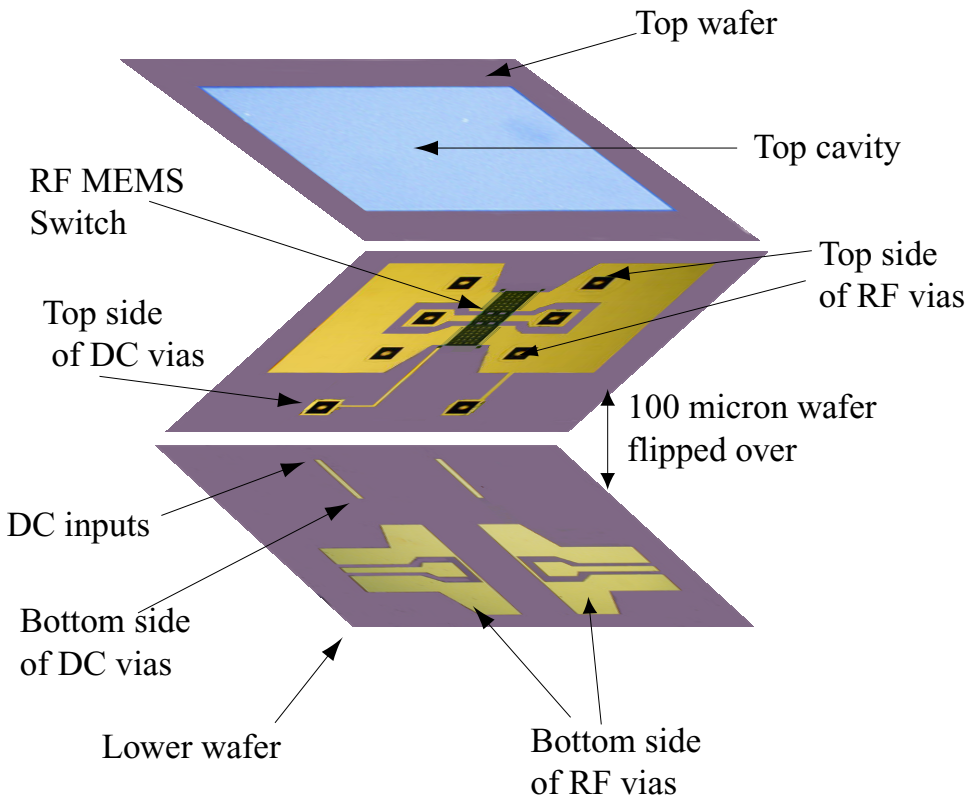


Figure 5.5: Photograph of fabricated transition, MEMS switch and packaging cavity.

consistent results.

The subsequent step is to fabricate the MEMS switch on the same wafer (Fig.5.7). The measured response of this system is presented in Fig.5.9, where both the up-state and down-state measurements are included. When the switch is in its up position the response is similar to the one illustrated in Fig.5.8. The capacitance of the switch at that position is 38 fF and therefore has some minor effects on the response of the circuit. Moreover the loss due to individual MEMS RF switches is in the order of 0.16 dB at 40 GHz [82] and henceforth the insertion loss of the total circuit is increased. The down state capacitance of the switch can be extracted from the S-parameters to be 1.3 pF and the switch demonstrates an isolation of approximately -22 dB at 40 GHz. The resonance occurring around 29 GHz is due to the RF transition, an optimum design of which can increase the bandwidth of operation and remove

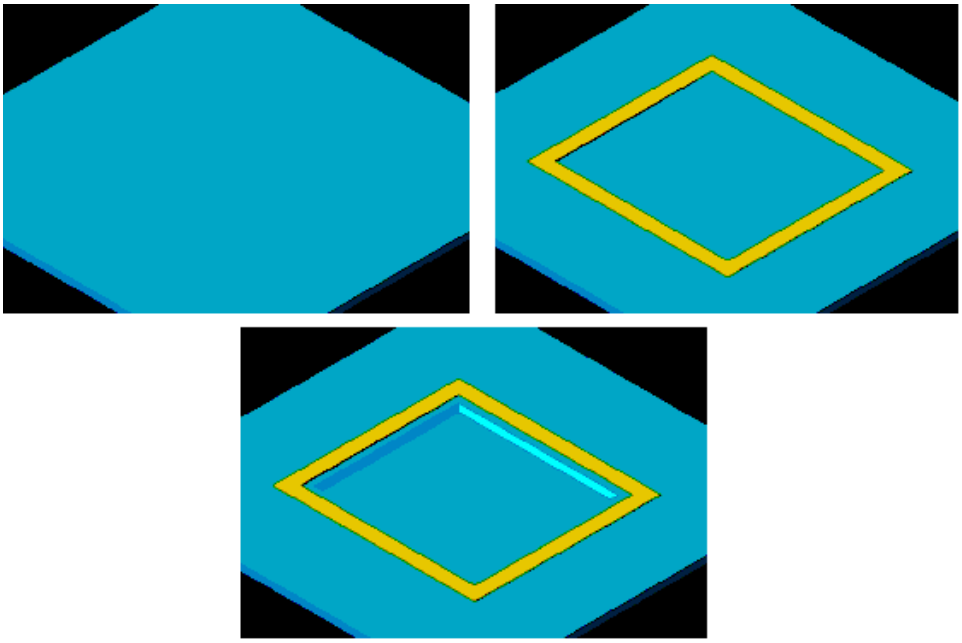


Figure 5.6: Fabrication process of top silicon wafer.

any unwanted resonances. However, this initial attempt demonstrated the ability to fabricate an on-wafer packaging structure and successfully operate RF MEMS devices inside it. Comparing the two measurements it can be concluded that the operation frequency band for the packaged RF MEMS switch is between 11 and 24 GHz, offering an insertion loss of 0.15 dB (switch loss included) and an isolation of -16 dB at 24 GHz.

5.3 Improved RF Transition

5.3.1 Design Process

Two main mechanisms exist causing unwanted resonances in the response of a transition designed to operate at high frequencies. The via-holes have an equivalent impedance and capacitance controlled by their geometric properties, such as length, shape, and surface area. This implies that the equivalent circuit of a via-hole transi-

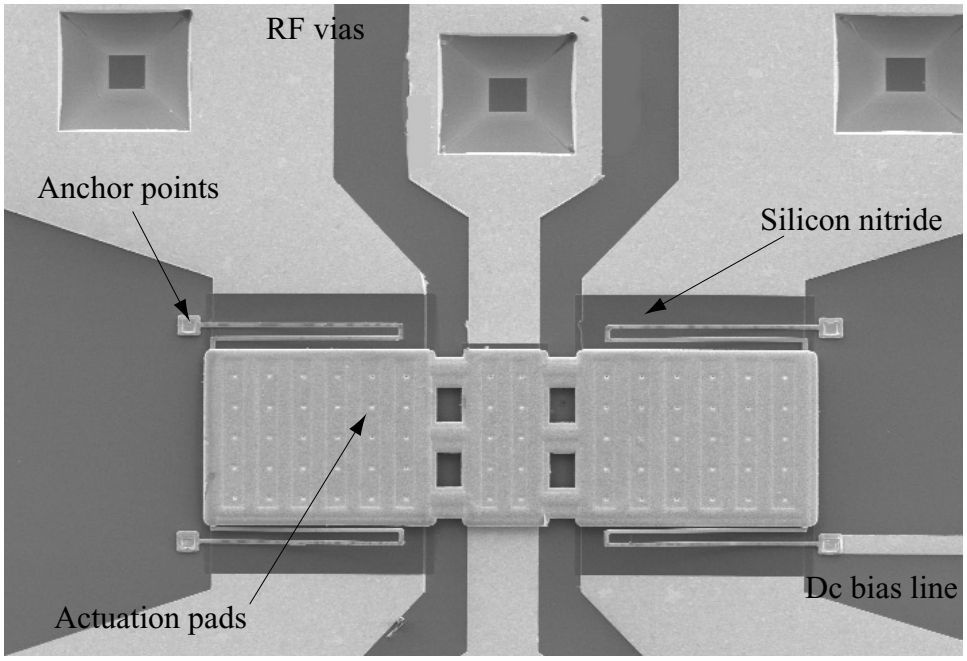


Figure 5.7: Scanning electron image of RF MEMS suspended over via-hole transition.

tion is characterized by an impedance value. Any mismatches between this impedance and the characteristic impedance of the feeding lines that connect to the transition will cause unwanted reflections in the area between the two vias (in the case of a back-to-back transition). These multiple reflections can create a standing wave on the line, thus significantly deteriorate its performance. Moreover, the via-holes themselves can radiate. As is demonstrated in [31] the abrupt change in the propagation characteristics of a line can cause the launching of a parasitic field, which couples to adjoining lines and degrades the response of the transition.

Unfortunately the initial design presented earlier suffered from both these effects. Improving its performance required significant theoretical investigation using full-wave solvers and circuit simulators [10, 14]. The stubs that were previously used to tune the transition at 20 GHz have been removed, since the simulation results demonstrated that they caused deleterious effects to the bandwidth. Removing the stubs also has an additional benefit in simplifying the modified lift-off process which

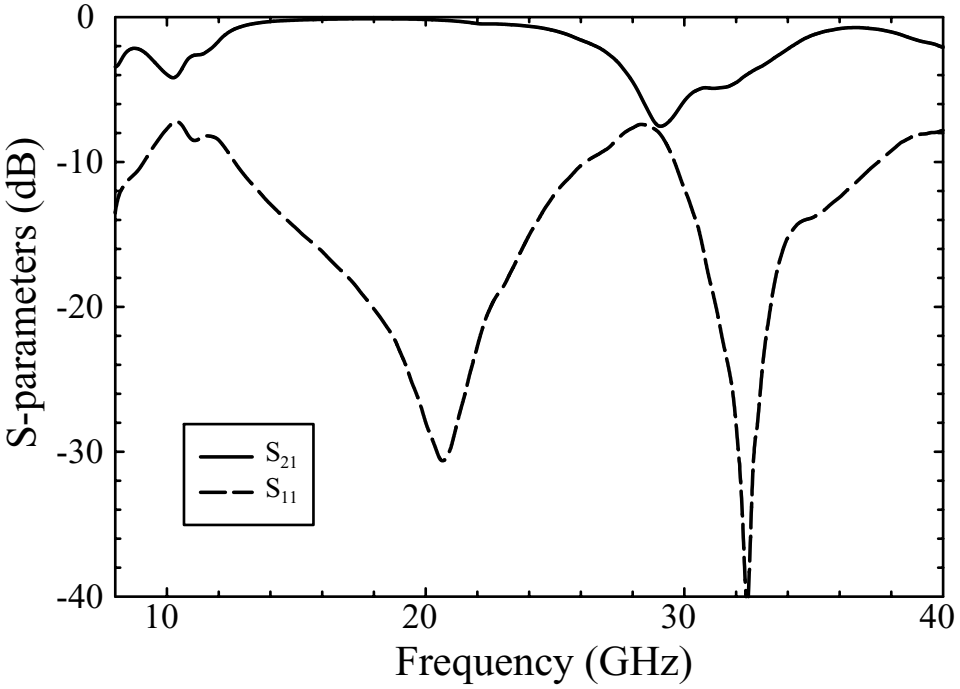


Figure 5.8: Measured response of RF back-to-back transition.

is utilized for the metallization of the vias. The slot regions of the FGC lines are now open on both sides, allowing easier access for the solvents to lift the metal during the lift-off.

Correcting the matching between the characteristic impedances of the vias and the feeding lines required more effort. An equivalent circuit [100, 101, 102, 103] has been developed in order to describe the behavior of the cpw based via-holes (Fig.5.10). For the circuit: the inductance is controlled mainly by the length and width of the vias, the capacitance from the total area of the upper and lower walls, and the conductances are due to the dielectric and radiation losses. Based on the simulation tools mentioned earlier a relationship is established between the geometric characteristics of the vias and the values of the inductances and capacitances in the circuit. As a result of that the FGC feeding lines can be slightly altered in such a way as to better match the impedance of the via-holes. The outcome of this process [104] is presented in Fig. 5.11 where a scanning electron image of the improved RF transition is shown.

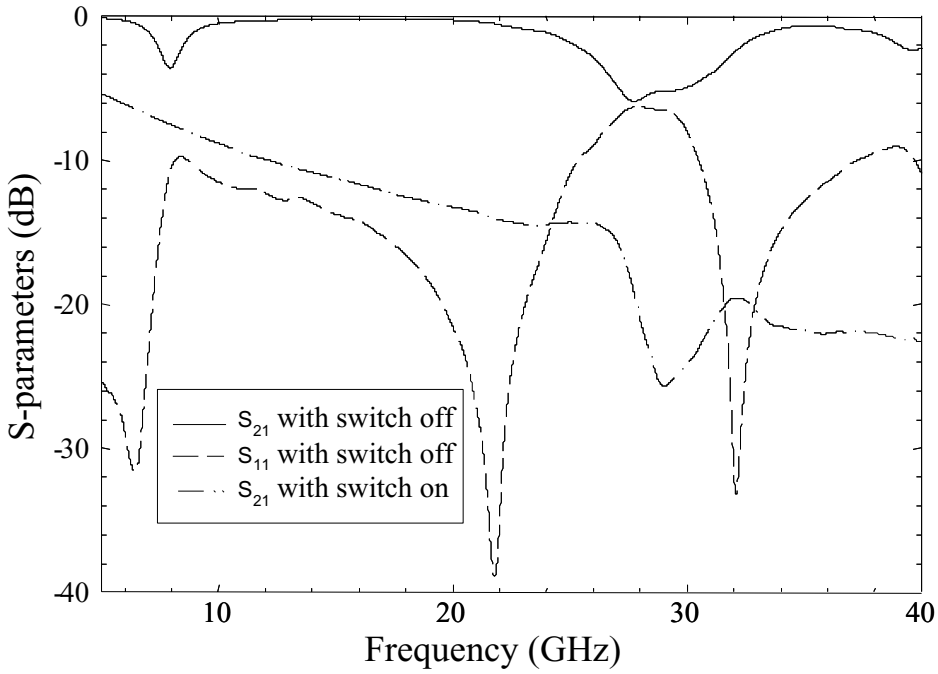


Figure 5.9: Measured response of packaged RF MEMS switch.

5.3.2 Measured Results

The measured response of the vertical back-to-back transition is displayed in Fig. 5.12 where an operation bandwidth from DC-40 GHz with a return loss lower than -25 dB throughout the band is observed. The measurements summarized in the figure include a 2700 μm through line, therefore the total insertion loss is around 0.4 dB at 38 GHz. If the losses from the FGC feeding lines are deembeded, the transition demonstrates a 0.06 dB loss up to 40 GHz and thus the loss due to each individual via transition is insignificant and approximately 0.03 dB. Taking into account the fact that no external wire bonding is needed in order to achieve signal propagation, this is the only loss introduced by the package. The response has four resonances which need to be removed in order to optimize the transition. Theoretical analysis of the package revealed that the 8 and 28 GHz resonances are due to the Au rectangular bonding ring that surrounds the transition. Additionally, the resonances at 14 and 22 GHz are due to the close proximity of the two DC vias to the FGC line. As will

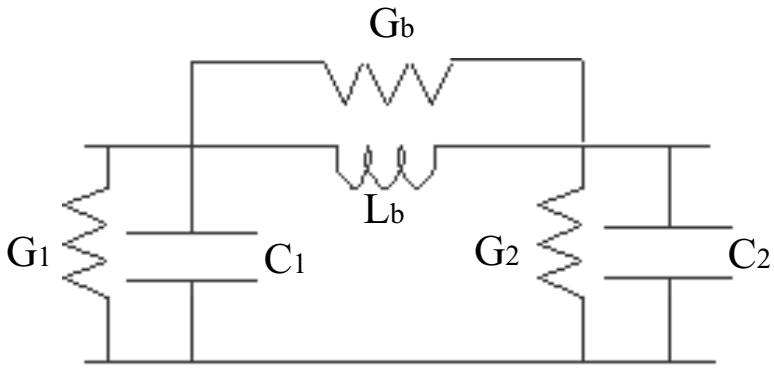


Figure 5.10: Equivalent circuit of via transition.

be presented in the following chapter, different placement of the DC vias, along with small alterations on the size of the bonding ring can push all the resonances higher than 40 GHz.

After the initial measurement, the RF MEMS switches are fabricated on the same wafers. A scanning electron image of the switch suspended over the RF transition is presented in Fig. 5.13. The measured response of the packaged RF MEMS switch is summarized in Fig. 5.14. The return loss at higher frequencies is increased due to the capacitance introduced by the switch in the up position, but it is always below -10 dB. When the switch is in the down position its capacitance increases to 1.3 pF (as can be extracted from the S-parameters) and the measured isolation is approximately -23 dB at 40 GHz. The observed performance is identical to the one demonstrated by an unpackaged switch. These measured results illustrate that the broad bandwidth of this package renders it applicable for both low and high frequency MEMS devices.

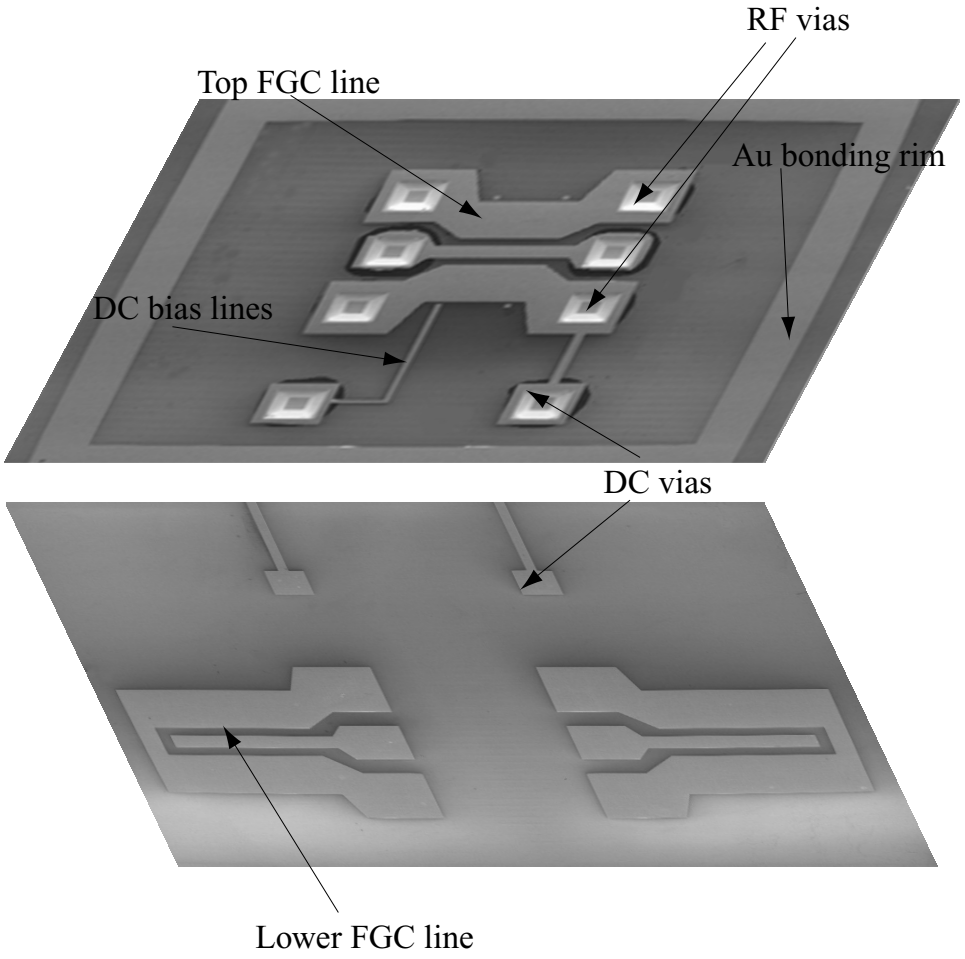


Figure 5.11: Scanning Electron Micrograph of RF transition through 100 μm Si wafer.

5.4 RF Transition Utilizing Multilevel Finite Ground Coplanar Waveguides

5.4.1 Introduction

A logical extension of the aforementioned packaging structure is its fabrication on thicker silicon wafers [105]. However, this should be done while keeping the total length of the via transitions as short as possible, in order to maintain the parasitic inductances at a minimum. In the proposed packaging scheme, presented in Fig. 5.15,

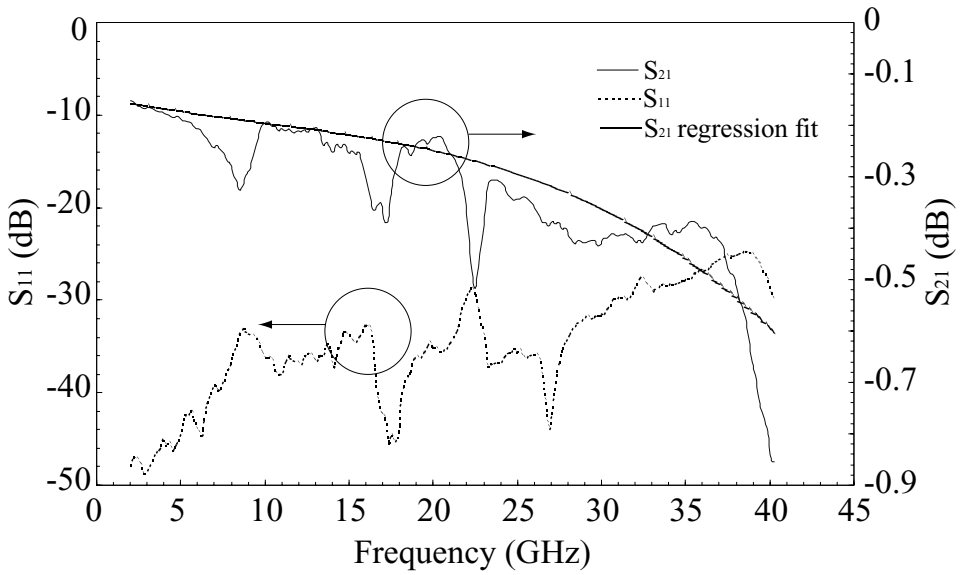


Figure 5.12: Measured response of improved RF back-to-back transition.

the thickness of the silicon wafer is locally reduced at 100 μm using anisotropic etching. FGC lines are then patterned inside the cavities and along the sidewalls forming multilevel interconnections; vias are then etched from the top forming the final transition. Conventional photoresist deposition through a "spin-on" technique fails to simultaneously pattern features in the depths of a micromachined cavity, along its sidewalls and on the top surface of the wafer. The main reason is that due to the spinning process the photoresist coverage is not uniform, exhibiting significant streaking of resist near corners on the top surface, accumulation at the junction of merging crystal planes internal to the cavity, and minimum coverage on the ledge that extends into the cavity. An alternative method of depositing photoresist proposed by researchers is electrophoretic (EDP) deposition [106].

Instead of spinning the resist, during EDP the sample to be coated is immersed in an appropriate solution and serves as the anode in an electro-platting process. The term electrophoretic stems from the motion of the charged photoresist particles towards the anode due to the existence of an electric field. For the presented inves-

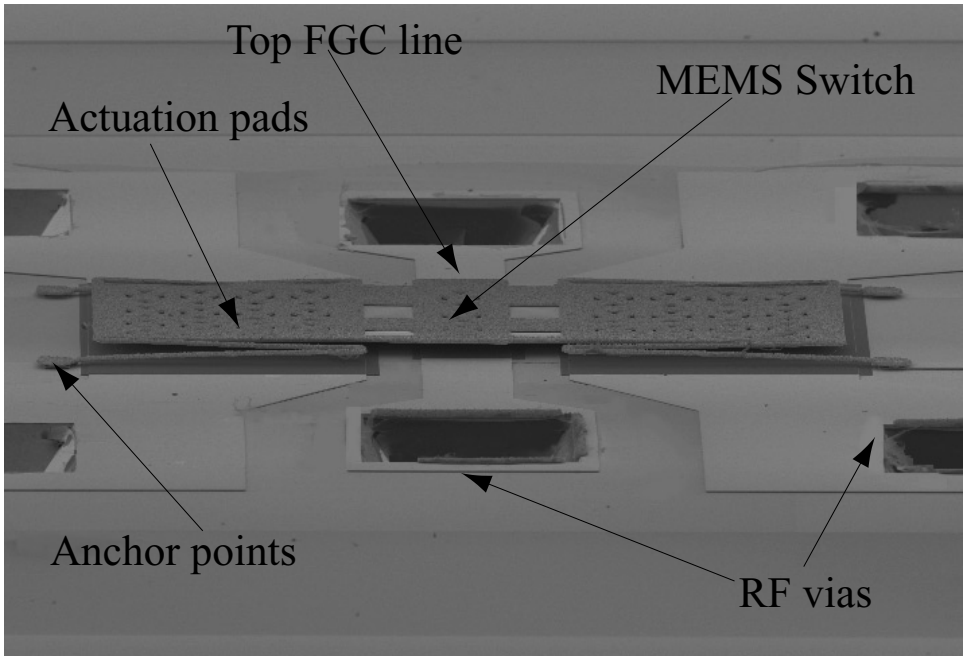


Figure 5.13: Scanning electron image of RF MEMS switch suspended over the RF transition.

tigation the photoresist utilized is Shipley's PEPR-2400 [107], a positive depositing resist, developed originally for use in the circuit board industry. Departing from its original use, this photoresist is utilized for developing a special deposition technique at the University of Michigan [108], which allows the formation of multilevel FGC lines. These transitions have an average insertion loss of less than 0.08 dB across the 2-40 GHz frequency range and are extremely compact, therefore they are very appealing for high-density packaging schemes [97]. Additionally, using the same approach, 100 μm wafers can be locally thinned to 40 μm and allow the fabrication of packages with operational bandwidth from DC to 100 GHz.

5.4.2 Fabrication Procedure

Initially the fabrication process presented in [97] is used (Fig. 5.16): 200 μm thick high-resistivity double-side polished (100) silicon wafers with 8700 Å of SiO_2 are anisotropically etched in tetramethyl ammonium hydroxide (TMAH). For the elec-

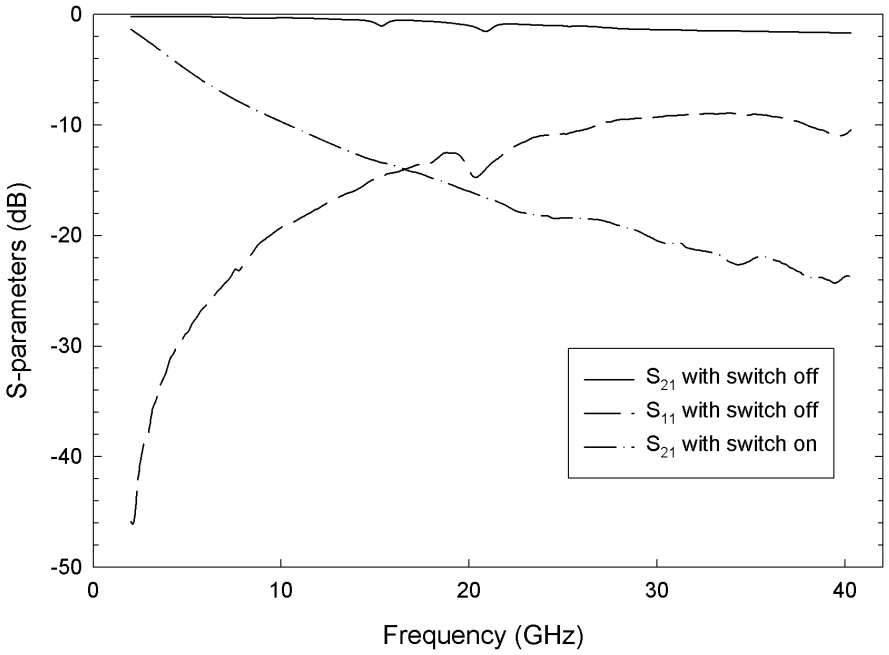


Figure 5.14: Measured response of RF MEMS switch.

trophoretic deposition the samples are coated by a metallic seed layer and are then immersed into a bath of suitable photoresist, such as Shipley's PEPR 2400. By applying a potential difference between the sample to be coated and a counter electrode a uniform, conformal coverage of the wafers can be achieved. The parameters that control the quality and thickness of the photoresist coverage are the bath temperature, the resist concentration, and the deposition voltage.

Contrary to its original design, for the purposes of this study, PEPR-2400 is used as a lift-off mask. It is found that in order to achieve the correct photoresist profile a vacuum drying procedure needs to be followed. The reason is that a 10 min long softbake on a hotplate seemed to cause deleterious effects on the adhesion quality of the resist. Additionally, the heating temperature reflowed the photoresist, thus creating non-uniformity. However, as shown in Fig. 5.17, the vacuum drying created roughness on each side of the FGC lines. This effect deteriorates the RF

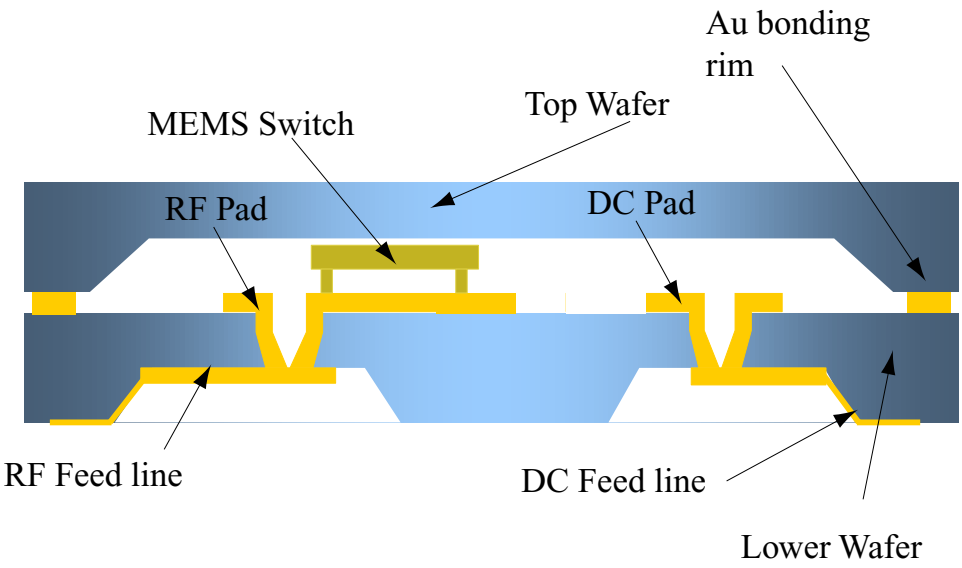


Figure 5.15: Schematic of packaged RF MEMS switch with DC and RF via transitions along with multilevel FGC transitions.

performance, especially at higher frequencies. Therefore, an extensive experiment is initiated in order to characterize the drying of the resist. It is found that a short 110^o C oven softbake can significantly improve the quality of the printed lines (Fig. 5.18). Additionally, due to its short duration and the fact that it is performed in an oven and not on a hotplate, the softbake did not create any adhesion problems and it improved the uniformity of the resist over the wafer. Thus, it rectified the overall yield of the process. However, as is always the case, the softbake caused the resist to reflow, reducing its total thickness and therefore making it difficult to successfully perform a lift-off with 1 μm of deposited Au. In contrast, the maximum reliably attainable metal thickness, is found to be 4000 Å . As will be shown in the measured results this increases the total observed RF loss. Since the creation of a multilayer micromachined package requires a significant number of fabrication steps, the softbaking approach is preferred since it offered improved yield.

After the deposition the desired pattern is exposed with a conventional mask aligner, and developed. A lift-off technique is utilized to achieve the final metal

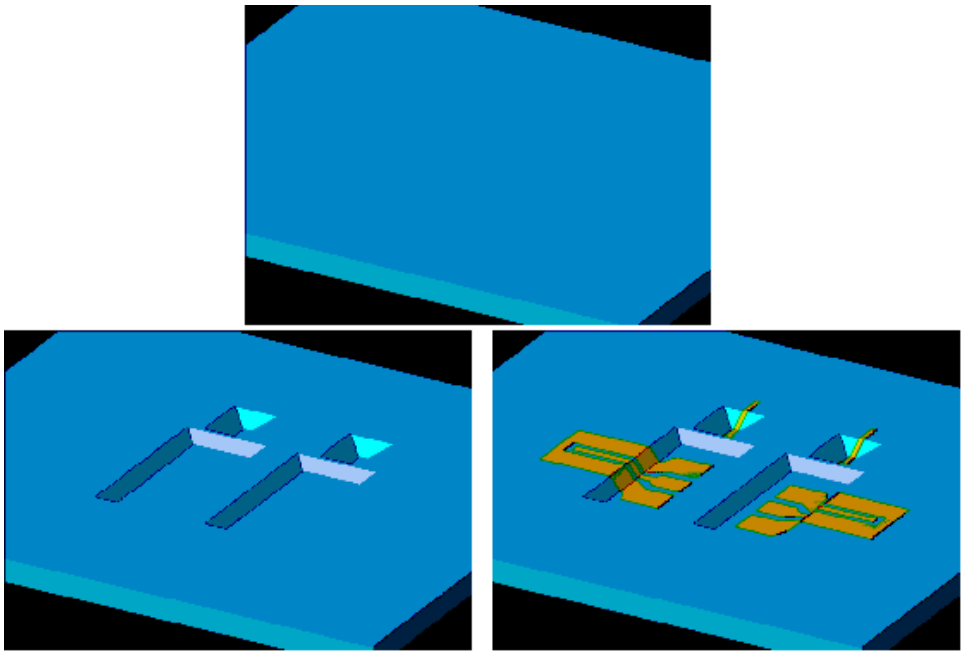


Figure 5.16: Fabrication process for multilevel FGC lines.

deposition. A scanning electron image of the DC and RF interconnects transitioning inside a 100 μm deep micromachined cavity are presented in Fig. 5.19 and Fig. 5.20. The next step in the fabrication process is the anisotropic etching and metallization of the via-holes from the top side of the wafer. Unfortunately, this step created some difficulties, which will be analyzed in detail in the following section.

5.4.3 Passivation Issues

Creating a multilevel packaging structure similar to the one suggested in Fig. 5.1 necessitates the use of two separate wet anisotropic etchings. The first one forms the transitioning cavities on the backside of the wafer and the second the via-holes from the top. As was already mentioned, the first wet etching is performed using TMAH in order to acquire smooth sidewalls and the second using KOH, which is better suited for creating smaller features. However, as can be observed in Fig. 5.21 after the initial TMAH etch, there is exposed silicon in the sidewalls and the lower wall of the

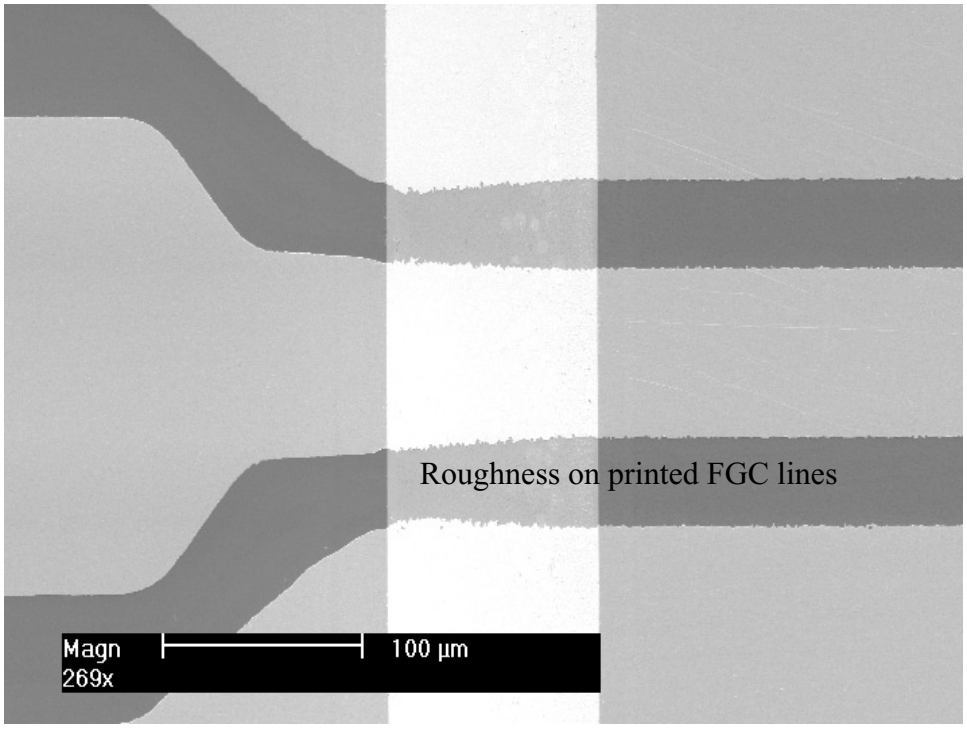


Figure 5.17: Fabricated FGC lines after vacuum drying and metal deposition.

cavities. The exposed silicon needs to be protected, because it can be attacked during the subsequent KOH etch. The problem is mainly focused on the lower walls of the cavities where the fastest etching planes {100} are exposed. Conversely, the exposed planes on the sidewalls are the {111}. Since these are the slowest etching planes, the subsequent KOH bath leaves the sidewalls unharmed.

A variety of materials have been tried for achieving backside passivation. In all the tests the same process is followed. The multilevel FGC lines are created first, then an infrared (IR) backside alignment is performed, the SiO_2 is patterned on the top side of the wafer to form the vias, and the wafers are then placed inside a KOH solution at 65^o C for the necessary 5 hours etch. Initially, thick metal layers (Cr, Au, Cu) are deposited on the wafer. Unfortunately, it appeared that the adhesion to the already existing multilevel FGC lines is problematic. The subsequently deposited metal layers, did not adequately cover the areas surrounding the FCG lines, and thus

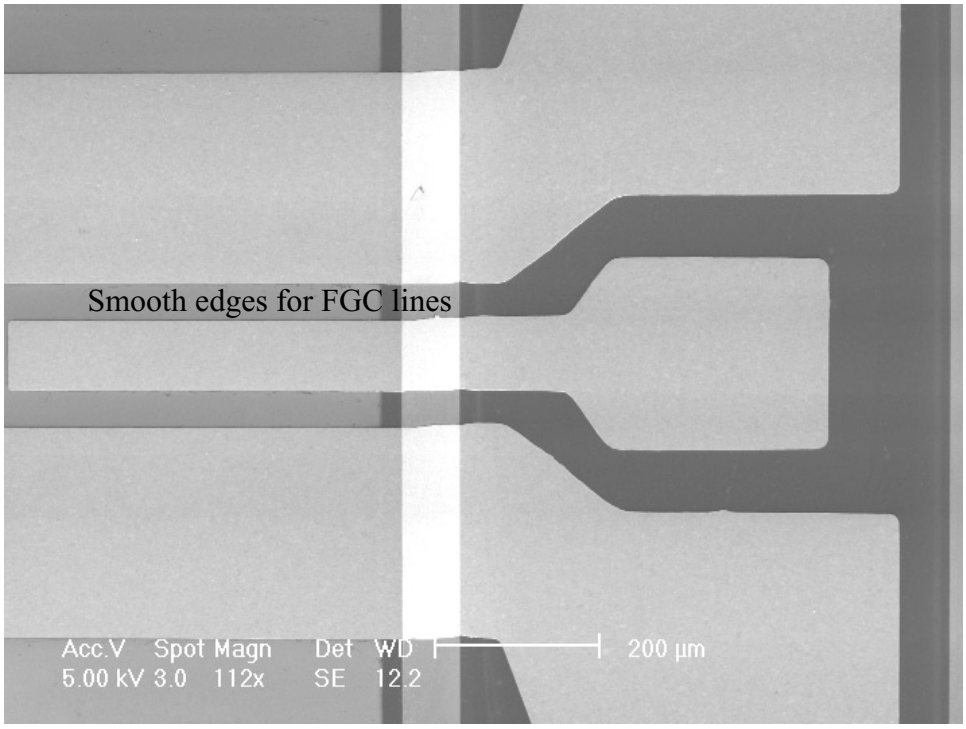


Figure 5.18: Fabricated FGC lines after short softbake and metal deposition.

allowed KOH to attack the underlying silicon.

A second attempt is made using dielectrics deposited with a Plasma Enhanced Chemical Vapor Deposition (PECVD) technique. 1 μm of SiO_2 is not able to protect the backside during the 5 hours KOH etch. The reason being that the quality of the PECVD SiO_2 is much lower compared to the thermally grown one and therefore the pinholes of the SiO_2 provided easy access to the silicon layer. Subsequently 1 μm of silicon nitride is tested. As is shown in Fig. 5.22 even after 1 hour of soaking into KOH problems start occurring. The silicon nitride deposited on the cavity sidewalls and the slot regions is fractured. The main mechanism causing this is the insufficient step coverage of the thick dielectric layer. As was mentioned, the exposure of the {111} planes in the sidewalls will create no additional problems, however, the bare silicon revealed in the slot regions is detrimental. KOH penetrates the silicon nitride layer and starts attacking the underlying silicon. Scanning electron images taken for

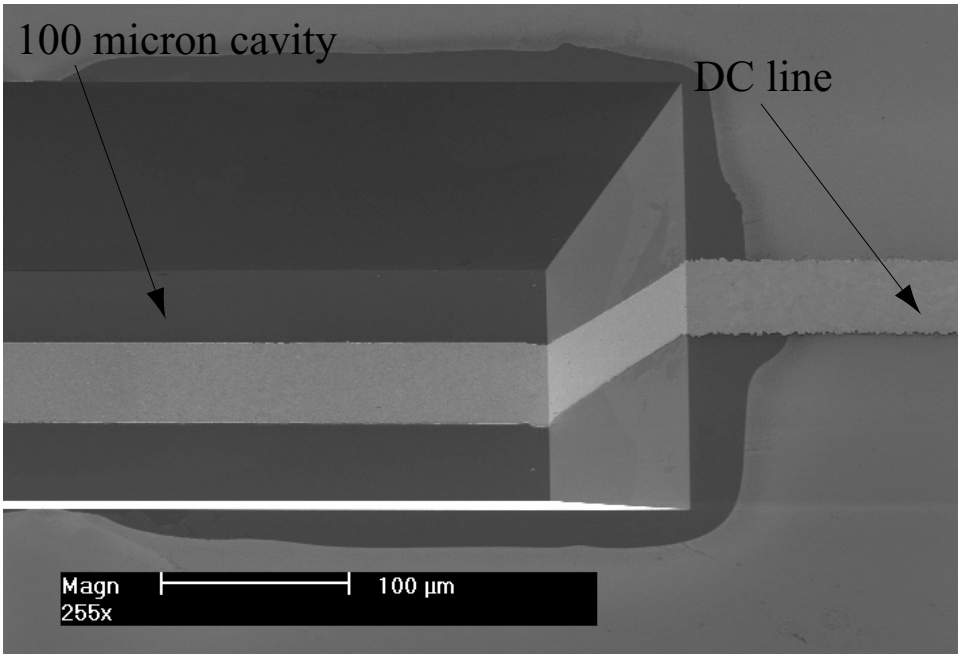


Figure 5.19: Scanning electron image of DC bias line transitioning inside a 100 μm deep cavity.

the same wafer every 30 minutes revealed this progressive mechanism of destruction. The silicon nitride is pealed off creating cracks and holes, which permit the etching solution to attack the wafer. After an additional hour of soaking in KOH the FGC lines, due to metal stresses, are released from the wafer and curl upwards.

The failure of materials readily available to provide adequate protection during the second wet anisotropic etch initiated an investigation to other solutions used in the industry. It is found that the optimum material for this purpose is sealing black wax [109]. This specific type of wax is designed for providing protection during soaking in base solutions. The process followed is that the wax is placed on a glass slide and melted at 130^o C. The wafer is then carefully mounted on the slide, making sure that the wax covers its backside and corners. The mounting procedure needs to be done extremely slowly since any extra pressure can shutter the 200 μm thick silicon wafer. After the KOH etch the wafers are released using a sequence of warm and cold xylene, acetone and isopropyl alcohol baths.

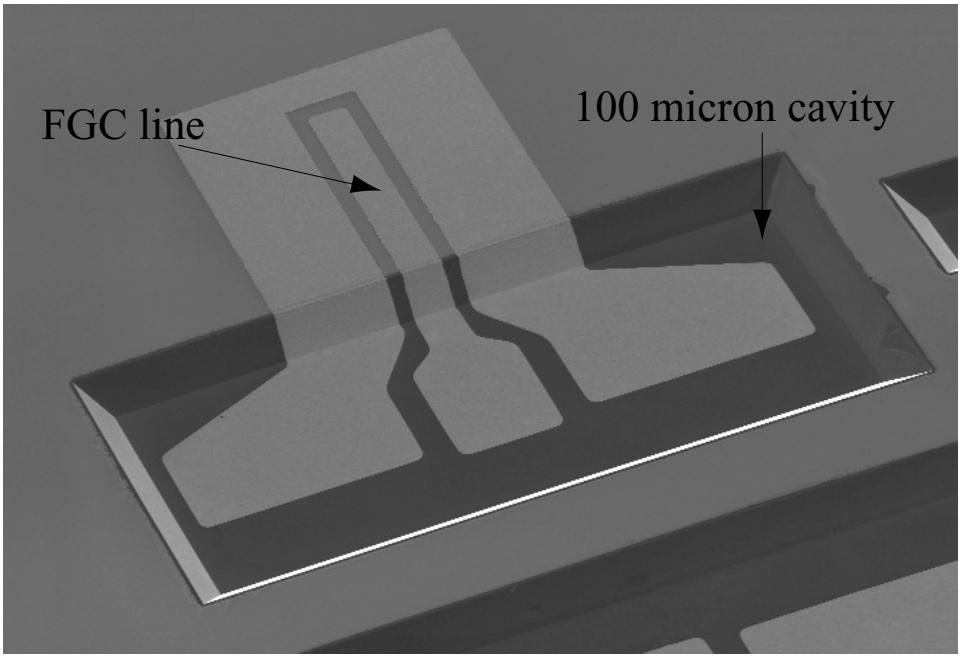


Figure 5.20: Scanning electron image of a finite ground coplanar waveguide transitioning inside a 100 μm deep cavity.

5.4.4 Measured Results

A scanning electron image of the RF transition is given in Fig. 5.23. The measured response of the transition is presented in Fig. 5.24. Similar to Fig. 5.12 the return loss is lower than -25 dB up to 40 GHz. As expected the insertion loss is increased due to the thin metallization of the feeding lines and is approximately 0.7 and 0.9 dB at 20 and 40 GHz respectively (including a 2700 μm long through line). The fabrication of multilevel FGC transitions have been demonstrated for metal thicknesses up to 1 μm, albeit with lower yield. Such a metallization will decrease the insertion loss to 0.5 and 0.7 dB at 20 and 40 GHz respectively. If the losses from the FGC feeding lines are deembeded, each transition demonstrates a 0.1 dB loss at 40 GHz which is divided approximately to 0.03 dB for the via-hole and 0.07 for the multilevel FGC line.

The thinner metallization is not the only mechanism that increases the insertion

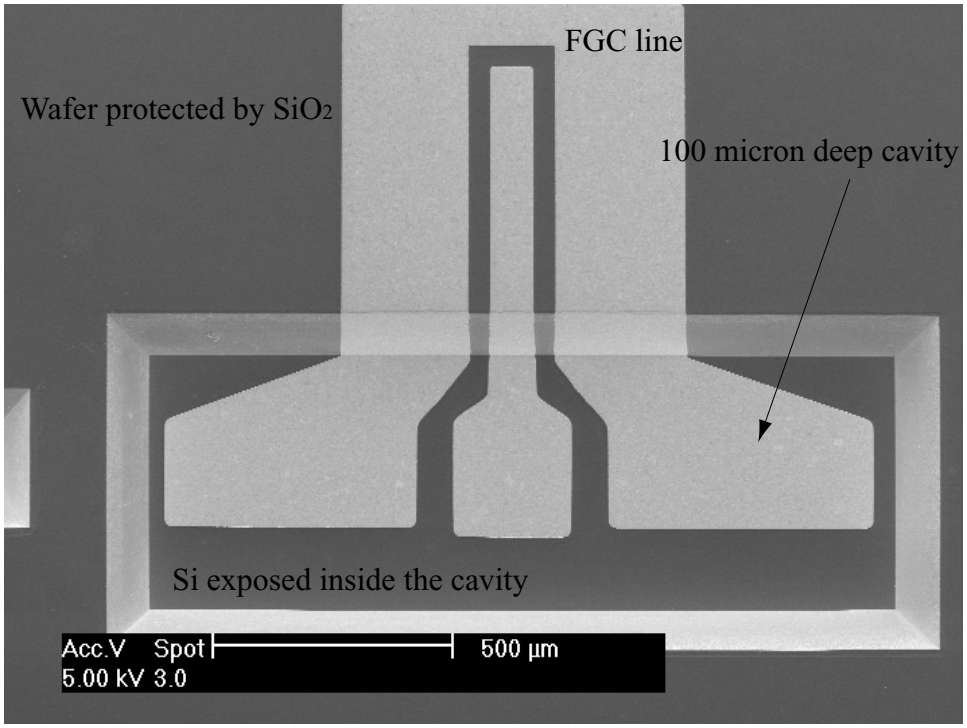


Figure 5.21: Exposed Si at the sidewalls and lower walls of the 100 μm deep cavity.

loss of the multilevel transition. As can be observed in the scanning electron images of the fabricated transitions the printed FGC line is not perfectly uniform along its length. Diffraction of UV light occurs during the pattern exposure step due to the 100 μm gap that exists between the mask and the bottom of the micromachined cavity. This unwanted diffraction tends to smear patterns and the lines resolved on the bottom surface of the cavity are of different dimensions compared to the FGC guides on top. Additionally, bulging of the transmission lines at the intersection of the cavity surface and the slanting sidewall is an artifact of increased photoresist thickness at such locations, resist drying procedure, and light diffraction. Since these effects are consistent in all the printed architectures, a compensating structure can be utilized in the masks in order to correct these problems.

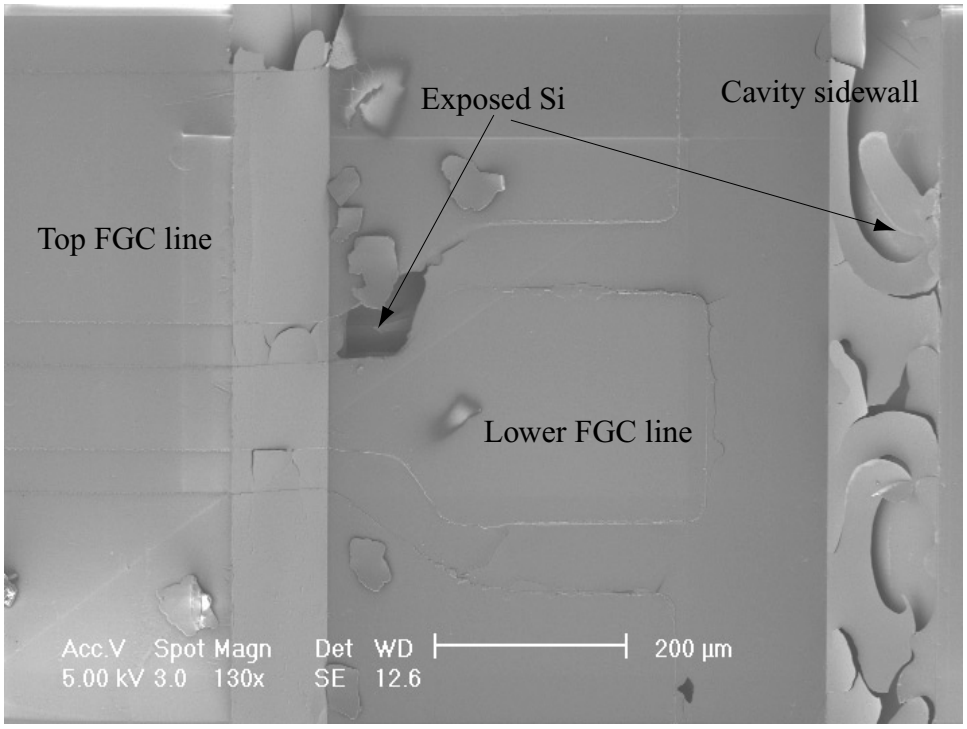


Figure 5.22: Scanning electron image demonstrating the failed attempt to passivate the backside using silicon nitride.

5.5 Conclusions

In this chapter the design and fabrication of an on-wafer silicon micromachined packaging structure for RF MEMS switches is presented. An initial attempt to fabricate the architecture is successful, albeit the RF performance is deteriorated due to an unwanted resonance at 29 GHz. After an extensive study on the effects of the via transition an improved design is investigated and the outcome demonstrate a DC to 40 GHz bandwidth and an extremely low insertion loss. Additionally, the possibility of creating a similar packaging scheme on thicker wafers through the use of electrophoretic photoresist deposition is successfully researched.

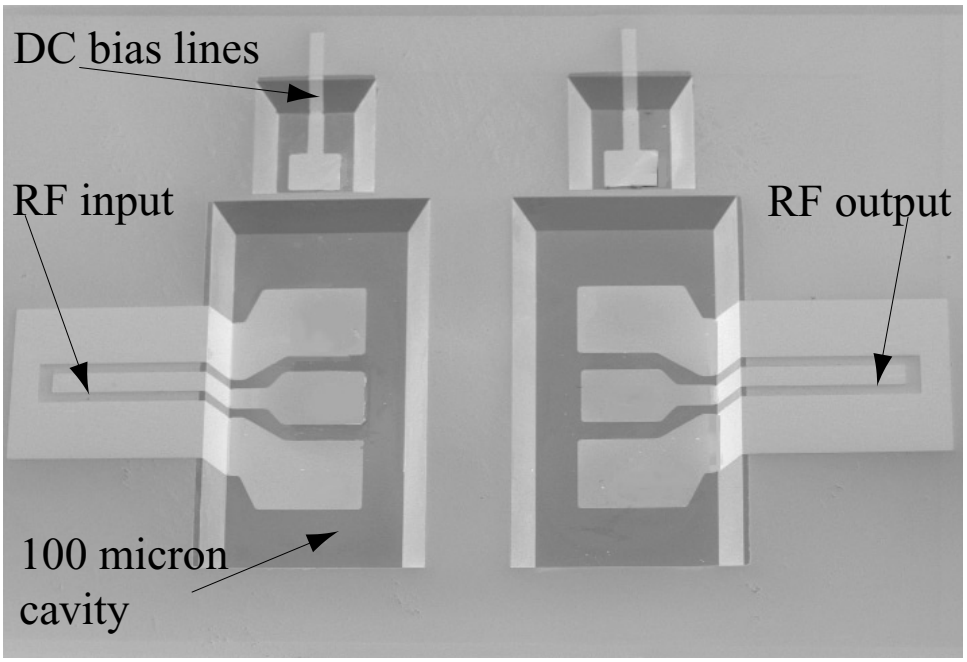


Figure 5.23: Scanning electron image of the multilevel RF transition

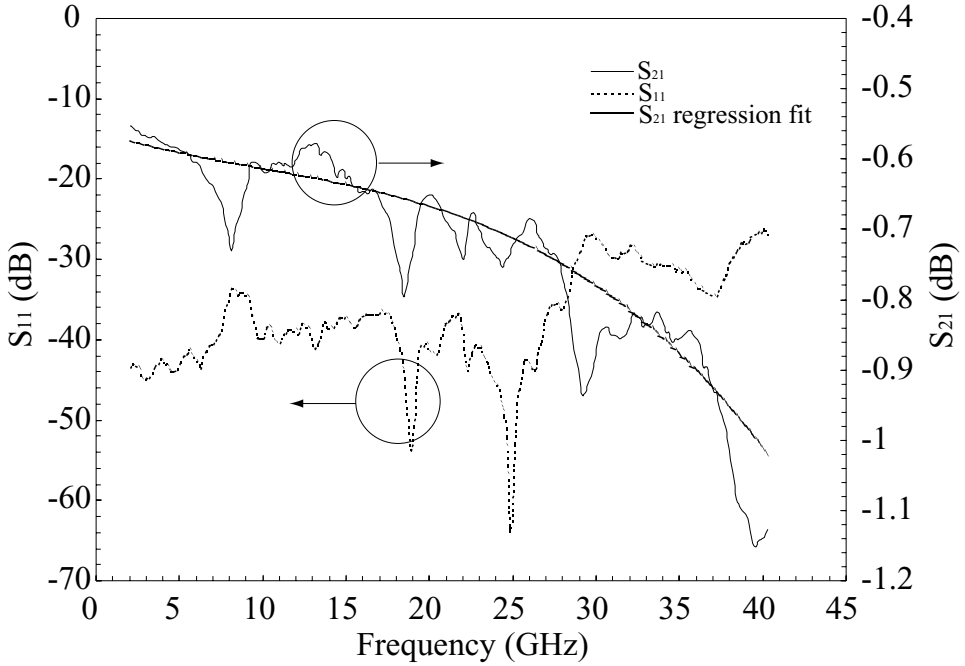


Figure 5.24: Measured response of RF back-to-back transition.

CHAPTER 6

Improved RF Package for Hermetic Sealing

6.1 Introduction

6.1.1 Importance of Hermetic Sealing

EMERGING military, space and commercial communications systems, are placing a high premium on low-cost, small, light-weight RF electronic components, while at the same time increasing demands for higher functionality. To maximize data transfer, reduce size and minimize operation cost, communications front-ends are forced to move to higher frequencies. Commercial and military satellite, some commercial terrestrial, and space borne communications systems are operating or being designed for the Ka-band (25-40 GHz). This trend necessitates the utilization of high performance RF packages that operate well at that frequency band. This is especially true for military systems where high reliability and mechanical integrity are paramount to mission success along with excellent RF performance. The harsh conditions of the modern battlefield with extreme temperatures, high mechanical loadings and vibrations, high humidity levels, dust and intense electromagnetic fields make the issue of RF packaging a very critical one.

While the RF MEMS technology has demonstrated the potential to revolutionize

the architecture of modern communications systems, it has not been designed for performance in harsh environments as required for use in future combat systems or space applications. RF MEMS technology requires further development to be able to provide successful performance under large temperature variations, strong vibrations, space radiation and handle low as well as high RF power. Recent developments have shown that the existing MEMS technology has exhibited long and short-term time and temperature-dependent effects on performance observed at a micro and macro scale levels [110, 111]. These effects may have an adverse impact on device characteristics and include but are not limited to: (a) RF Thermal Effects and Stress Redistribution in Thin-Film Metals; (b) Stiction in MEMS Contact Relays; (c) Stiction and Dielectric Charging in MEMS Capacitive Devices. The importance of these mechanisms in switch lifetime and endurance depends on the architecture and on the environmental factors under which these MEMS devices operate. The environmental operating conditions can be controlled via the use of an appropriate package that combines the properties of traditional IC packages along with compatibility with planar technology.

The first major concern in any package is its ability to minimize water penetration. Water alone will not cause failure or corrosion inside the package [112]. However, it is the vehicle for contaminants like negative (Cl^-, F^-, $NO_3{}^-$, $SO_4{}^{2-}$, $PO_4{}^{3-}$) and positive (Na^+, K^+) ions to cause performance degradation. These ions are the residues of the various processing steps and their removal from the interior of the package prior to sealing is not always successful [113]. Additionally, humidity can cause stiction of the MEMS membrane. Some researches report that relative humidity of 30% can have deleterious effects on the switch performance [110].

There are four contributors to the moisture within a package [85]: (a) the sealing ambient; (b) the absorbed and dissolved water from the outgassing of the materials that form the package; (c) the water created by chemical reactions within the package

and (d) the leakage of external moisture though the seal itself. An ideal packaging environment for RF MEMS is an extremely dry ambient of Ar or N_2 at a pressure close to 1 atm. This ambient can act as a damping mechanism for the switch membrane. Additionally, maintaining a pressure equilibrium between the inside of the package and the outside world will reduce the possibility of flow of external gasses to the package. Typically, N_2 is formed from a liquid-N_2 source which has moisture levels of 10ppmv or less [114]. Therefore an ambient atmosphere of nitrogen is ideal for a hermetic MEMS package.

A typical packaging cavity for MEMS switches has a volume of $2x10^{-7}$ liters and therefore it is extremely sensitive to any outgassing resulting from the carrier and recessed cover substrates. This outgassing is attributed to desorption of moisture or gases absorbed in the substrate, and to gases (such as hydrogen) that are trapped in the electroplated Au lines. Desorption can easily be eliminated by vacuum baking the substrates to 120-150^{o}C [115]. Additionally, getters for hydrogen, moisture or even particles can be integrated inside the MEMS package, either surrounding the device or printed on the recessed cover [116]. Moreover, a chemical reaction between hydrogen and oxygen is theoretically possible within the package. This is a very possible reaction since its free energy is highly negative (-54K calories), however, the rate of the reaction is extremely slow at ordinary temperatures and pressures [117]. This effect is therefore not a big concern, unless a suitable catalyst resides inside the package.

Reducing the leakage of external moisture inside the package can be addressed by forming a hermetic seal. Moisture related problems prompted the military and aerospace industries to require hermetic packages in order to achieve high reliability and long life. A hermetic package is theoretically defined as one that prevents the diffusion of He below a leak rate of 10^{-8} cm^3/sec. For such packages the sealing materials are usually inorganic (glasses or metals), while organic materials such as

epoxies, plastics and polymers are used for non-hermetic packaging. Non-hermetic packages are a cost efficient method to encapsulate devices and today they account for approximately 90-95% of all device packages. Nevertheless, as was already mentioned, the implementation of RF MEMS on real systems requires hermetic sealing and therefore such a packaging scheme needs to be utilized. No material is truly hermetic to moisture. The permeability to moisture of glasses, ceramics and metals, however is orders of magnitude lower than any plastic or organic material. Therefore, a hermetic package can be either metal or ceramic. The sealing of such a package can be performed by a variety of techniques [85]: Fused metal seals, soldering, brazing, welding and glass sealing.

6.1.2 Thermocompression Bonding

Historically, some of the earliest uses of wafer-to-wafer bonding were for packaging of pressure sensors [118]. These bonds were performed at low temperatures (below 450^o) and involved either field-assisted silicon-to-glass bonding (anodic) or an intermediate-layer bond between silicon wafers using a gold thin film [119]. In general, these bonding processes operate under two basic conditions. First, the two bonding surfaces must be flattened to have intimate contact for bonding. Second, proper processing temperatures and applied pressures are required to provide the bonding energy. Low-temperature wafer bonding has been under study mainly for die attachment and electrical interconnects with the bulk of research centered on the eutectic or lowest melting temperature. Of the eutectic-solder-based bonding, eutectic gold wafer bonding at 363^oC (2.85 % Si and 97.1% Au by weight) [120] has been most highly promoted due to low minimum liquidus temperature and widespread use in die bonding. Eutectic gold bonding has been extensively analyzed in [121, 122, 123, 124] where the quality of the bond is ascertained through visual inspection of grain boundaries or load measurements.

Recent studies however, demonstrate that the actual mechanism involved in Au-Si wafer bonding is controversial [125, 126]. The issue is created from the fact that an intermediate layer of Ti or Cr is often separating Si and Au. Simple considerations do support the idea that the incorporation of such a layer should have an effect on the bonding. These materials have been reported to be diffusion barriers and up to some extend this is the reason for their use. The very low solubility of Ti and Cr to silicon would prevent the Au-Si eutectic composition from being reached by diffusion of Si through the Ti into the gold. Extensive experimental investigation [125] demonstrated that reliable bonding is achieved after 60 min annealing at 600^{o}C (or 20 min at 800^{o}C). Moreover, silicide grains are formed at the bonding interface. Therefore researchers proposed that the actual bonding is initiated by the dissolution of the oxide layer by silicidation of the Ti adhesion/barrier layer. The subsequent direct Au-Si contact enables the formation of the eutectic phase. It needs to be added however, that none of these investigations took pressure into account. It is obvious that further detailed research is necessary in order to understand the exact mechanisms that form gold bonds.

For the purposes of this study an experimental verification of the above theory is attempted using an EV 501 bonder. Many silicon wafers with deposited Cr and Au layers on opposite sides are bonded at various temperatures. It is observed that at temperatures above 400^{o}C the electroplated Au is severely deformed, a fact that will cause degradation of the RF performance of the package. A scanning electron image of a deformed gold layer is presented in Fig. 6.1. Additionally, it is noted [78] that when an intermediate layer of Ti is used the deformation of the Au layer occurs at 370^{o}C. Therefore it can be claimed that a Cr adhesion layer behaves slightly better during the bonding process. Furthermore, at temperatures below 370^{o}C the wafers are only partially bonded and can be easily separated using a pair of tweezers. Successful bonds are achieved only when the bonding temperature is kept at 380 and

390^oC and the bonding pressure at 60 N/cm^2. A scanning electron image of such an attempt is shown in Fig. 6.2. It needs to be clarified however, that all these results strongly depend on the available bonder.

The quality of the bond is also controlled by the pre-bonding cleaning of the wafers. It has been demonstrated [127, 128] that surface films and contaminants are responsible for failed bonding attempts. There are two general groups of surface films: oxide films and absorbed organic and water vapor films. Since Au does not easily form an oxide when in contact with the atmosphere, oxide films are not a big concern. Unfortunately, films might be created by other impurities. Therefore, the attempted pre-bonding cleaning starts with a solvent cleaning followed by an ultra-violet exposure. Then the wafers are placed inside an oven and heated at 150^oC in order to reduce any possible outgassing from the materials. Finally, an additional drying mechanism is utilized during the bonding. Initially the samples are brought in contact and heated at 200^oC. Then the pressure inside the chamber is reduced to 1 mbar and immediately N_2 is purged increasing the pressure back to 1 atm. The sequence of pumping and purging is repeated three times. The flow of N_2 inside the chamber is kept low in order not to harm the released MEMS structures. Nevertheless, it can help to remove water molecules attached on the internal surfaces of the package (with weak Van-der-Waals forces), thus reducing even more the possibility of outgassing. Finally, the temperature is increased at 390^oC, a pressure of 60 N/cm^2 is exerted and the wafers are bonded while N_2 is being purged in the bonder. With this bonding procedure an ambient atmosphere of nitrogen is created inside the packaging cavity.

6.1.3 Accelerated Testing Techniques

To ensure package reliability, extensive testing needs to be performed before a new device can be delivered. Ideally, the tests should be conducted in the same envi-

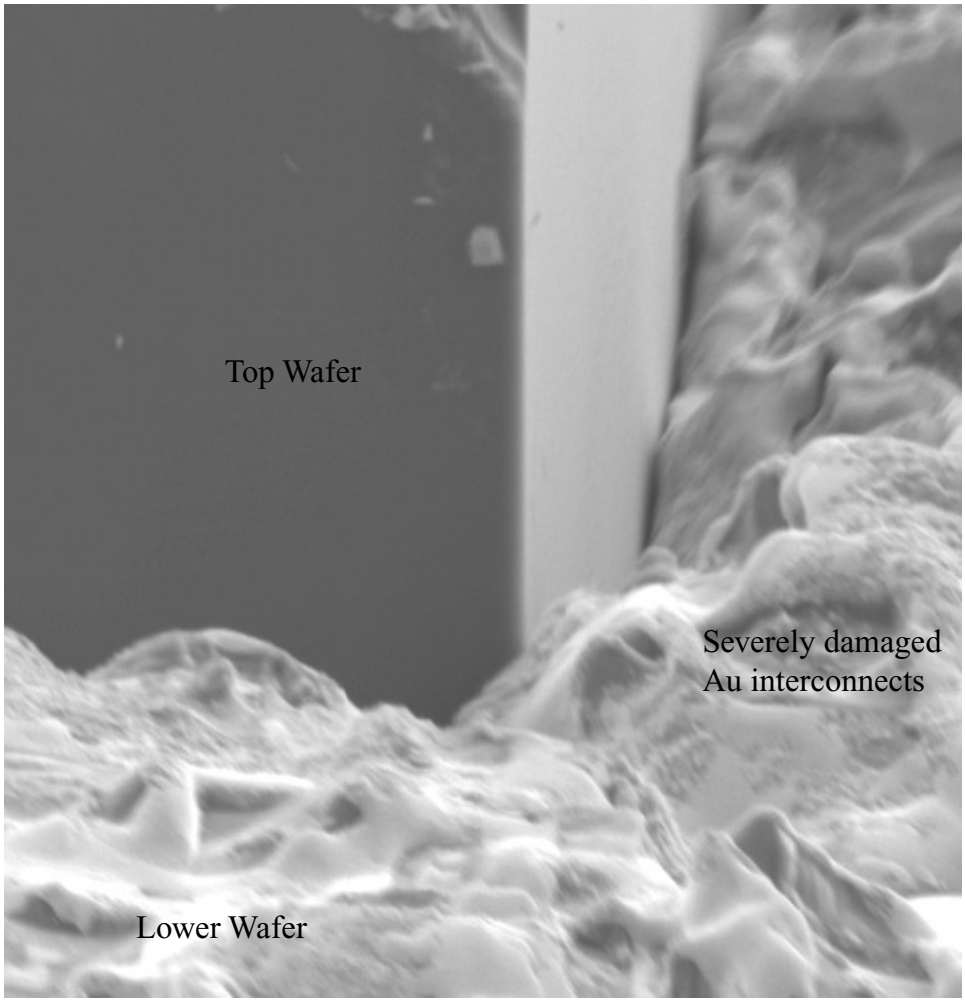


Figure 6.1: Scanning electron image of deformed Au layer after a thermocompression bonding at 410^{o}C.

ronment as the one in which the package will be used. However, the designed service life for many electronic products is long enough to prohibit reliability testing under actual service conditions. To perform reliability tests within a reasonable amount of time, under a well-controlled environment, accelerated tests are commonly carried out in a laboratory. In accelerated tests, the devices are subjected to much higher "stress" than they would experience under normal usage condition. This accelerates the failure mechanisms, so that various failure modes can be observed much sooner than would happen in actual conditions [129, 85], thus reliability data can be collected

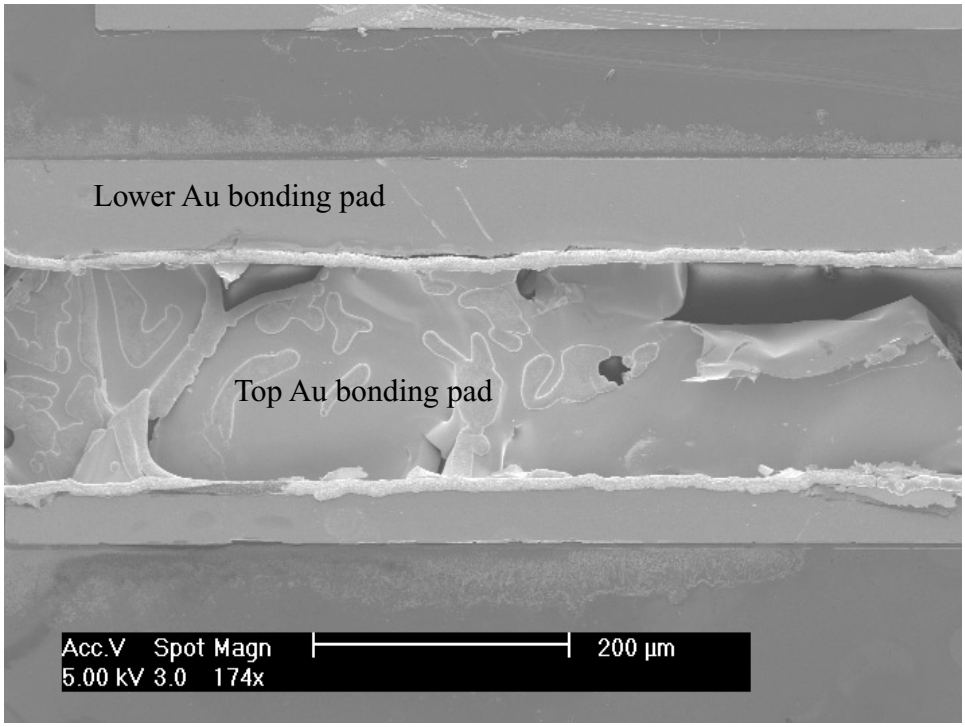


Figure 6.2: Scanning electron image of successful thermocompression bond at 380^{o}C. The top wafer is pulled and the Au remained attached to the lower Au layer demonstrating the strength of the bond.

within a much shorter period of time.

During the 1960s Western Electronics developed the 85/85 test in which components were placed in an 85^{o}C and 85% Relative Humidity (RH) environment with or without an electric bias. Initially a common criteria for passing the test was 1000 hours of 85/85. During the 1980s the 85/85 lifetimes began to far exceed the 1000 hours, and it became apparent that waiting time for the completion of each test was excessively long. This led to more aggressive Highly Accelerated Stress Test (HAST). These tests involve much higher temperatures and RH in order to expedite their outcome [130]. A very commonly used HAST test [131, 132] utilizes an autoclave chamber at 130^{o}C, 2.7 atm of pressure and 100% RH. This is the HAST test selected for demonstrating the hermeticity of the on-wafer RF MEMS packaging structure.

In order for the accelerated test to have any significance, a model is needed to

correlate the accelerated results to normal operating conditions. This can be accomplished by formulating reliability models that relate accelerated environmental tests to actual field life. Two methods have been proposed: relate the accelerated Mean-Time-To-Failure (MTTF) of a specific device to that of the same device at different conditions using a statistical model; or through comprehensive, fundamental modelling of the physical activities at the molecular level leading to degradation and failure. The latter technique is of course preferable, however models based on these theories are still at a research level in the industry [133]. The former approach incorporates statistically significant data obtained from well-planned and consistently executed tests in order to form a probabilistic model allowing extrapolation to other conditions. One extensively used model for acquiring such an extrapolation is proposed by Peck [134, 135]. This model can relate the MTTF of HAST results to normal operating conditions (temperature and RH) and will be analyzed in more detail in the following section.

6.1.4 Reliability Metrology

Reliability is the characteristic of an object that provides a required function whenever such a function is sought. For a microelectronic component reliability is the probability that the component will be operational within acceptable limits for a given period of time. Typically, failure patterns for any manufactured article follow the same "bathtub" shape [85, 136]. Failures at short times (called early failures or infant mortality) cause an initial reduction of the failure rate, and are due to manufacturing faults which are very difficult to detect. Since they occur very early in the device's expected lifetime they represent the costliest type of failure. After this initial reduction the failure rate become almost constant. During this period intrinsic failures occur, which are due both to manufacturing errors or extensive usage. This period represents the most useful part of a device's lifetime and needs to be as

extended as possible. Finally, wearout failures begin to become significant as normal wearout mechanisms start to take their toll on the components that are manufactured within acceptable specifications. This effect causes the failure rate to increase again, thus the terminology "bathtub curve" is created.

Weibull Distribution

The cumulative failure function F(t) is defined as the fraction of the original devices that have failed by the time t, or equivalently the probability that a given device will have failed by time t. In order to be able to compare failure patterns for devices, semi-empirical reliability distributions are used to reduce the observed and often incomplete failure data to easily quantified parameters. The most widely used distribution for this purpose is the two-parameter Weibull distribution mainly due to its ability to represent all three distinct regions of the bathtub curve [137, 129]. The cdf and pdf of the Weibull are:

$$F(t) = 1 - e^{-\left(\frac{t}{\lambda}\right)^{\beta}} \tag{6.1}$$

$$f(t) = \frac{\beta}{\lambda}\left(\frac{t}{\lambda}\right)^{(\beta-1)} e^{-\left(\frac{t}{\lambda}\right)^{\beta}} \tag{6.2}$$

The failure rate is given by:

$$h(t) = \frac{f(t)}{1 - F(t)} = \frac{\beta}{\lambda}\left(\frac{t}{\lambda}\right)^{(\beta-1)} \tag{6.3}$$

The two parameters of importance are λ, the lifetime parameter which is related to the MTTF and β, the shape parameter which determines how the failure frequency is distributed around the average lifetime. It is dimensionless and usually between 0.5 and 2. A shape parameter of unity means that the chances of device failure is constant with time. A smaller β indicates that there is a higher probability of early failures,

perhaps due to manufacturing defects, and a β >1 means that wearout failures are causing an increase in the failure rate. The MTTF is evaluated as:

$$MTTF = \int_0^\infty tf(t)dt = \lambda\Gamma\left(1 + \frac{1}{\beta}\right) \tag{6.4}$$

where $\Gamma()$ is the gamma function.

Curve Fitting

As can be observed from equation 6.4 the two parameters λ and β are needed in order to calculate the MTTF of the device. The extraction of these two parameters from the raw measured data is performed by fitting the data to an appropriate Weibull distribution. This extraction can be performed either graphically, using appropriate Weibull-Probability plots, or analytically. All the results in this thesis are acquired with the analytic technique.

The procedure followed for this evaluation [137] starts with the estimation of $F(t_i)$ using the median rank approximation. Thus:

$$F(t_i) = \frac{i - 0.3}{n + 0.4} \tag{6.5}$$

where t_i is the time when the i-th failure occurred and n the total number of devices under test. After the completion of the test, i.e. the failure of all the devices, the least square method can be applied for the evaluation of the parameters.

$$\hat{X} = \frac{1}{n}\sum_{i=1}^{n} ln\left[ln\left(\frac{1}{1 - F(t_i)}\right)\right] \tag{6.6}$$

$$\hat{Y} = \frac{1}{n}\sum_{i=1}^{n} lnx_i \tag{6.7}$$

and subsequently

$$\beta = \frac{n\sum_{i=1}^{n}(lnx_i)(ln\left[ln\left(\frac{1}{1-F(t_i)}\right)\right]) - n^2\hat{X}\hat{Y}}{[n\sum_{i=1}^{n}(lnx_i)^2] - \left[\sum_{i=1}^{n} lnx_i\right]^2} \tag{6.8}$$

$$\lambda = e^{\left(\hat{Y}-\frac{\hat{X}}{\beta}\right)} \tag{6.9}$$

Nevertheless, on many occasions it is not practical to wait until the completion of the accelerated test in order to evaluate the MTTF of the devices. In this case the test is terminated after a prearranged time T>0, and the data are said to be rightly singly censored [138]. The test starts with N devices of which, after time T, n are failed and c=N-n are still operational. The estimation of the Weibull distribution parameters can now be performed using linear estimators and an appropriate likelihood function. For the case of singly censored samples described by a Weibull distribution this function is:

$$L = \left[\prod_{i=1}^{n}\left(\frac{\beta}{\beta^{\lambda}}\right)x_i^{\beta-1}\right][1-F(T)]^c\, e^{-\sum_{i=1}^{n}\left(\frac{x_i}{\lambda}\right)^{\beta}} \tag{6.10}$$

After some algebraic manipulation [138] finding the maximum of the likelihood function results in assessing the value of β that solves the following equation:

$$\frac{\left(\sum_{i=1}^{n} x_i^{\beta} lnx_i\right) + cT^{\beta}lnT}{\left(\sum_{i=1}^{n} x_i^{\beta}\right) + cT^{\beta}} - \frac{1}{\beta} = \frac{1}{n}\sum_{i=1}^{n} lnx_i \tag{6.11}$$

Solving this equation using Newton's iterative method can provide the estimated value of β. For the life parameter:

$$\lambda = \left[\frac{\left(\sum_{i=1}^{n} x_i^{\beta}\right) + cT^{\beta}}{n}\right]^{\frac{1}{\beta}} \tag{6.12}$$

Acceleration Factor

Once the accelerated tests are performed, an acceleration factor (AF) can be defined as the ratio of the actual time to failure under normal operating conditions to that under accelerated test conditions. This acceleration factor can predict the actual lifetime of the device, based on the accelerated laboratory tests. Ideally these factors are based on the fundamental modelling of the physical activities at the molecular level leading to degradation and failure. However, such models require a-priori knowledge of the failure mechanisms and are extremely complicated to acquire. Instead of that, empirical probabilistic models have been created which can predict the MTTF of tested devices under normal operation conditions. The majority of these approximations is based on the Eyring model [139], which is an extension of the well understood Arrhenius model. The Eyring model takes into account multiple stresses (temperature and relative humidity) and thus is ideal for HAST tests [140]. The most widely accepted acceleration transform has been quantified by Peck [134, 135]. The relationship that provides the MTTF for normal operating conditions relative to the accelerated ones is:

$$AF = \frac{\left(RH^{-n}e^{\frac{\Delta E_a}{kT}}\right)\text{normal}}{\left(RH^{-n}e^{\frac{\Delta E_a}{kT}}\right)\text{accelerated}} \tag{6.13}$$

where RH is the relative humidity, T the absolute temperature and k the Boltzmann constant. According to the model the recommended values for n is 3 and for the activation energy ΔE_a is 0.9 eV.

6.2 Improved RF Transition Design

6.2.1 Removal of Parasitic Resonances

A package for RF MEMS switches have been demonstrated in the previous chapter. Its response is repeated in Fig. 6.3. As can be observed from the graph the measured results of the back-to-back transition include four parasitic resonances at 8,14,22 and 28 GHz. These resonances are independent of the MEMS switch, since they occur even when a simple back-to-back transition is measured, and appear consistently in all the samples. Using a commercially available finite element solver [10] a theoretical analysis of the structure is performed and it revealed the existence of two mechanisms causing these parasitic effects: the gold bonding ring that surrounds the structure and the DC bias lines that are used for the actuation of the switch.

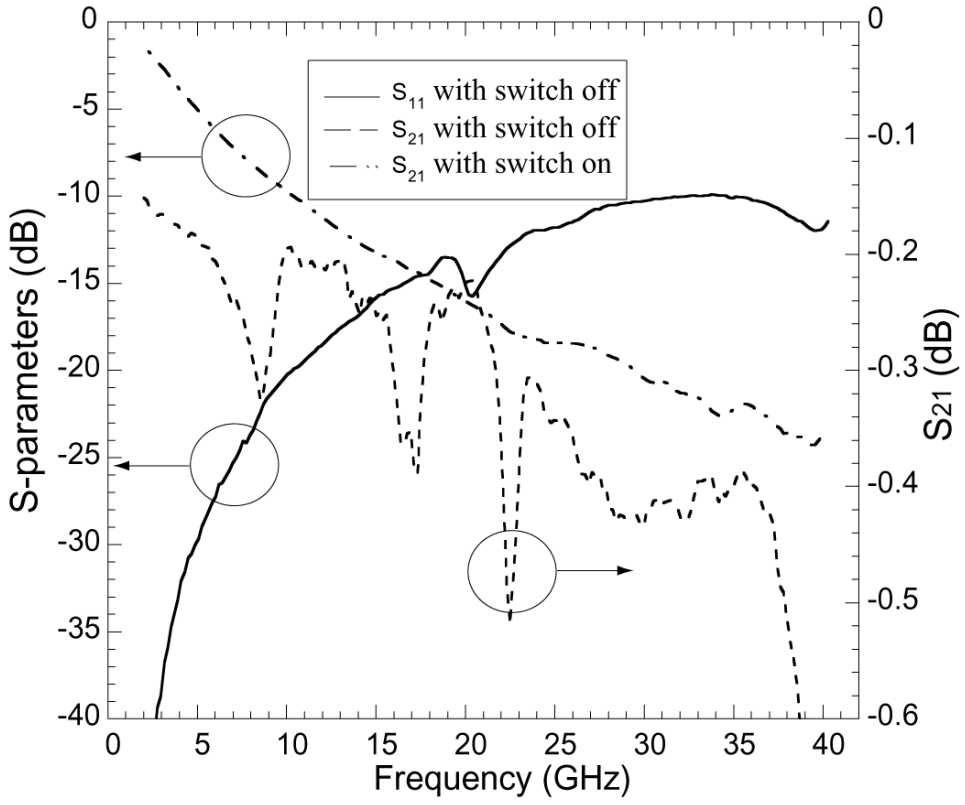


Figure 6.3: Measured response of packaged RF back-to-back transition and MEMS switch.

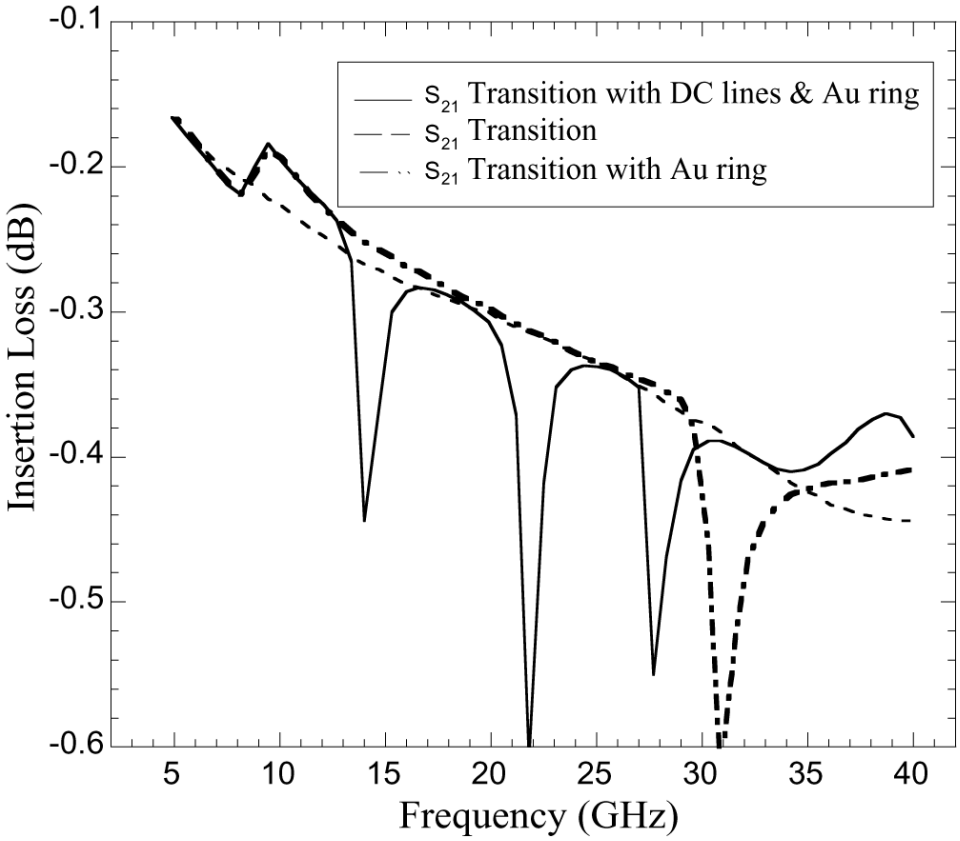


Figure 6.4: Simulated results for RF back-to-back transition.

The idea of an on-wafer packaging scheme implies that a sealing ring will be created on the same wafer as the structure to be encapsulated. Since hermeticity is a basic requirement for MEMS packaging Au-to-Au bonding is the method selected for sealing the package. However, a metallic square ring resonates at the frequencies where its total length equals a wavelength and for the structure under consideration this occurs at 8 and 28 GHz. This result can be clearly observed in Fig. 6.4 where some of the simulated results acquired are presented. In this graph the response of the transition without the gold ring and the DC bias lines, along with the two cases where these elements are added, is shown. The initial case, where only the back-to-back transition is solved, illustrates no parasitic resonances and a total insertion loss that very closely approximates the measured result in Fig. 6.3. Subsequently,

the Au ring is added and two resonances at 8 and 28 GHz appear. One method for eliminating this effect is by reducing the ring's total length and thus, pushing the resonances at higher frequencies. In the new transition, which will be presented shortly, this method is utilized. The ring is reduced at 1.7x1.8 mm and the parasitic effect of the ring is pushed at 36 GHz. This result is illustrated in Fig. 6.5 where the simulated response of the new transition is presented. The graph includes both a single RF transition (with the addition of the DC vias and bias lines) and the same transition with the Au bonding ring.

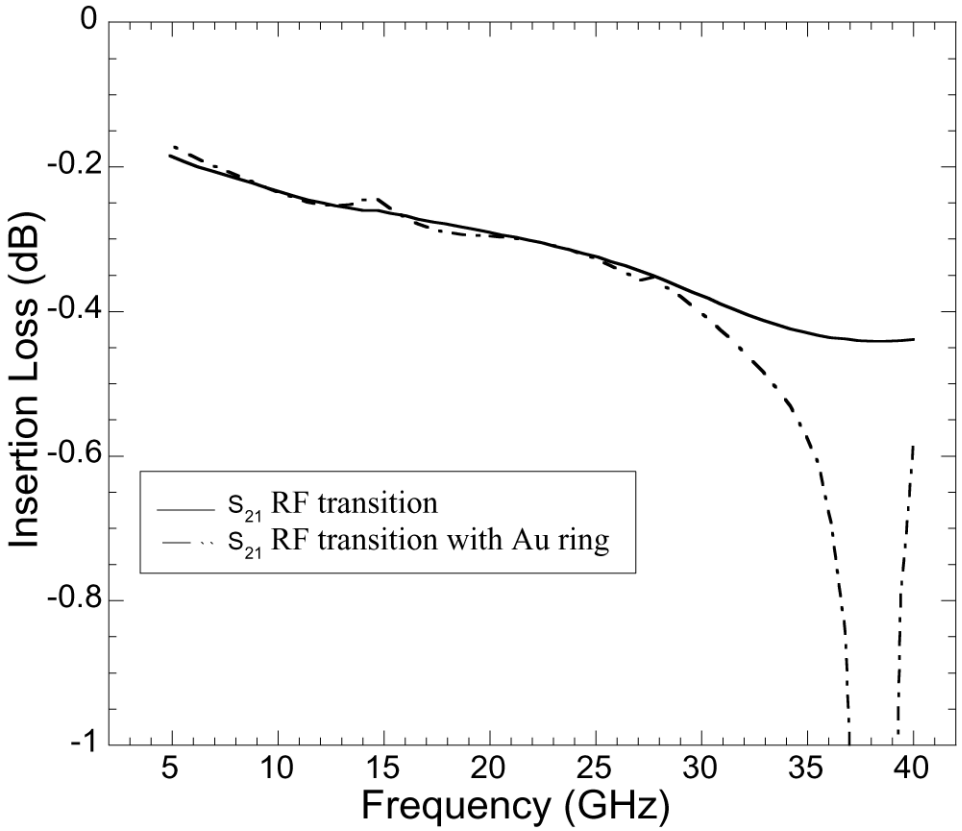


Figure 6.5: Simulated results for improved RF back-to-back transition.

As was mentioned earlier, a second mechanism that causes parasitic effects is the length of the DC bias lines. In particular the problems are caused by the line that connects one of the DC vias to the ground plane of the FGC line. This connection is required for the activation of the switch, since it creates the necessary voltage

difference between the FGC line and the suspended air-bridge. As can be observed in Fig. 6.4 the addition of the bias lines creates the two resonances at 14 and 22 GHz. Varying the length of these lines (effectively changing the distance between the DC vias and the FGC ground plane) moves the resonances by as much as 4 GHz. By analyzing the structure with just the DC vias (no bias lines present) it is deduced that the vias cause no parasitic effect. The addition of the bias line that connects one of the DC vias to the anchor point of the switch cause no resonance as well. When the bias line that connects to the FGC ground plane is added the two resonances at 14 and 22 GHz appear. Therefore, it is presumed that this parasitic effect is caused by a resonance created by the bias line (on both the front and the back-side of the wafer) and the FGC ground plane. Removing this parasitic effect is more complicated compared to the ring effect, the reason being that the two effects are convoluted and a single solution needs to address both. The ring needs to surround both the top FGC line and the two DC vias and bias lines. Therefore the placement of the DC vias controls the length of the ring. The optimum results, presented in Fig. 6.5, are acquired when the two DC vias are placed in opposite sides and in close proximity to the RF transition. Thus, both the DC bias lines and the Au bonding ring have the minimum possible length. In Fig. 6.6 the field distribution inside the dielectric is presented. As can be observed from the graph the field is stronger along the FGC line. However, a very strong field is launched by the edge of the dc bias line. The field concentrated at the Au bonding ring is -15 dB and the coupling seems to occur at the areas where the FGC line crosses below the ring. Moreover, due to the asymmetry of the structure the coupled field is more intense on the lower part of the ring compared to the top. Additional theoretical simulations show that with minor layout changes the maximum frequency that the parasitic resonances can be pushed is 55 GHz. In order to reduce the length of the bonding ring more a different technique, such as deep reactive ion etching (DRIE), will be necessary for the creation of the via-holes.

The vias etched using DRIE are isotropic, meaning that their shape is not limited by the crystal plane orientation. However, metallizing such vias is extremely challenging due to their high aspect ratio, surface roughness and steep sidewalls.

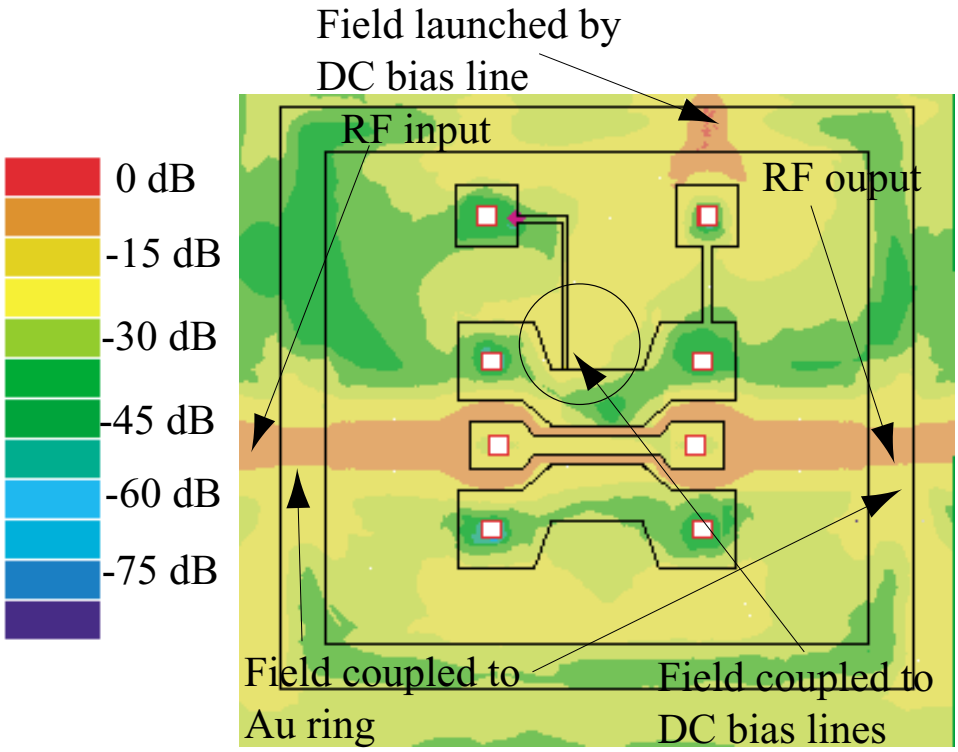


Figure 6.6: Magnitude of the electric field underneath the Au bonding ring and the top FGC line.

6.2.2 Fabrication Procedure for Improved Hermeticity

In the previous chapter the fabrication process necessary for the formation of the packaged RF MEMS was presented in detail. It was mentioned that the metallization of the vias is achieved using a deposition technique which is introduced in [95]. This procedure allows the simultaneous metallization of the side wall of the vias and the top FGC line via a "modified" lift-off. However, the final thickness of the metal can not exceed 1 μm due to the photoresist utilized. This thickness is adequate for W-band operation where the skin depth is approximately 0.25 μm, but insufficient for K

band operation (skin depth of 0.5 μm at 20 GHz). Therefore the measured RF loss presented in Fig. 6.3 can be potentially reduced. Instead of a lift-off the metallization is now achieved by sputtering a thin seed layer of Cr/Au immediately after the vias are anisotropically etched in potassium hydroxide (KOH), thus making sure that no native oxide is created on the lower walls of the via-holes. The use of a sputtering machine also ensures a more uniform coverage of the via sidewalls. Subsequently, 4 μm of Au are electroplated to form the FGC line. During the electroplating step the vias are also metallized along with the square ring of Cr/Au which is deposited around each circuit in order to be used for thermocompression bonding. The final metal thickness is larger than the skin depth even at the lower frequencies of operation and therefore the RF performance of the transition can be significantly improved. In parallel with this, the thicker metallization addresses a different weakness of the original design in which the hermeticity of the sealing was threatened by the thin metallization of the via walls. The lower walls of the via-hole transitions were approximately 2 μm thick (1 μm of Cr/Au from each side) and humidity could diffuse inside the packaging cavity. By increasing the metal thickness on the via walls the sealing quality can be significantly improved. A scanning electron image of the new vias is presented in Fig. 6.7, where the thicker metallization is observed. The outcome of this new fabrication process is presented in Fig. 6.8. In the new layout the DC bias lines are replaced by shorted pads and placed on each side of the FGC waveguide. In addition the thicker deposited Au layer will improve both the hermeticity of the package and its RF performance by reducing the insertion loss.

6.2.3 Wafer-to-Wafer Alignment Technique

The last step prior to sealing the packages is to accurately align the wafers with respect to each other. This alignment needs to be relatively precise since the width of the bonding ring on each package is 200 μm. Any mismatches will reduce the area

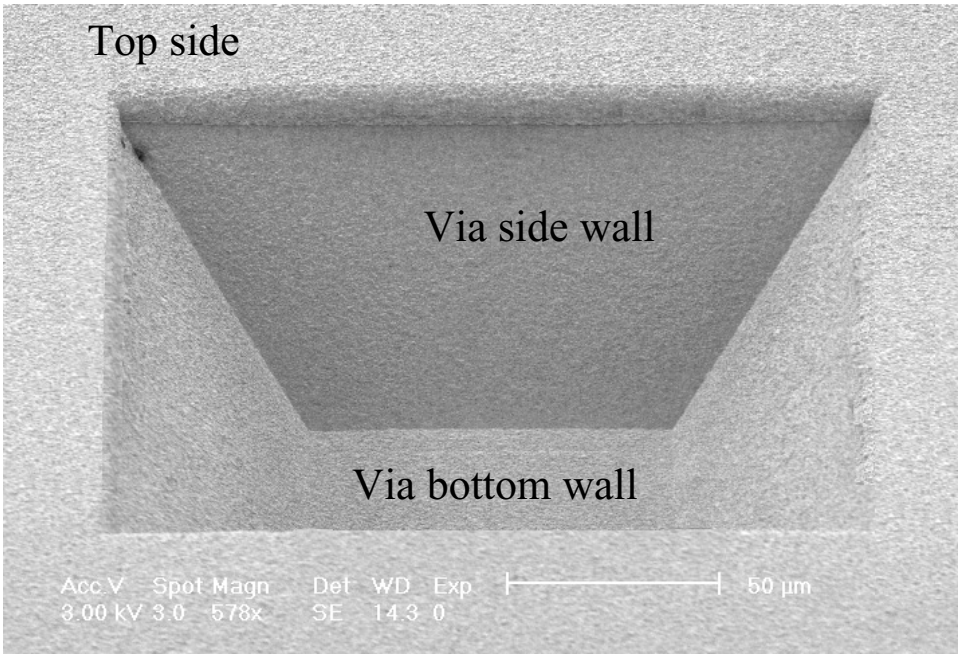


Figure 6.7: Scanning electron image of electroplated via-hole.

of overlap between the two bonding rings (one on each side of the opposite wafers), thus deteriorating the hermeticity of the sealing.

The available EV-501 bonding system is connected to an aligner with backside capabilities. Ideally, the wafers to be bonded are aligned together using appropriate printed marks on their surfaces and are subsequently placed inside the bonder. Unfortunately this is only applicable for full 4- or 5-inch wafers. During this fabrication smaller silicon pieces (1x1 inch) are being used. This implies that a new pre-bonding alignment mechanism needs to be utilized. One available technique is the use of glass spheres as alignment keys. In this approach pyramidal holes of appropriate dimensions are etched on both wafers using TMAH to accommodate one-half of a glass sphere's volume. The glass spheres are then dropped inside the holes and the two wafers are aligned. The main problem with such an approach is that since the diameter of each sphere is 596 μm their use with 100 μm thick wafers is prohibited. The spheres need to be completely covered inside the silicon wafers otherwise the

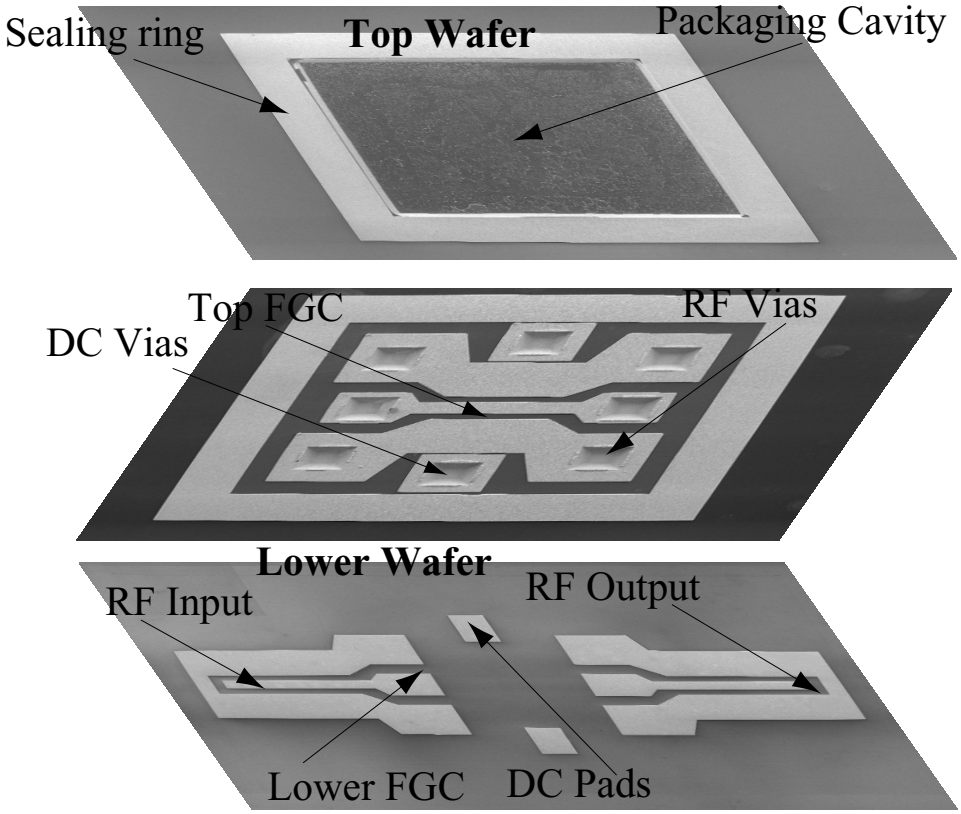


Figure 6.8: Scanning electron image of improved RF transition.

thermocompression bonding will not be successful. Therefore, their use is possible only if the total thickness of the wafer stack is larger than 600 μm.

A second alignment technique has been developed at the University of Michigan by Mr. Y.Lee [141]. In this case the idea of etching groves on both wafers and then use similarly shaped alignment keys is repeated only this time the glass spheres are replaced with silicon wafer pieces. This approach has three major advantages: since the keys are crosses and rectangles of various sizes, the accuracy that they provide is drastically improved compared to the glass spheres. Moreover, both the keys and the necessary groves are etched using DRIE and therefore their sidewalls are almost vertical, increasing the accuracy. Finally, in contrast to the spheres, the thickness of the alignment keys can be reduced to 200 μm, thus making it suitable for alignment of two 100 μm thick silicon wafers. A scanning electron image of a 100 μm deep

etched cross is shown in Fig. 6.9.

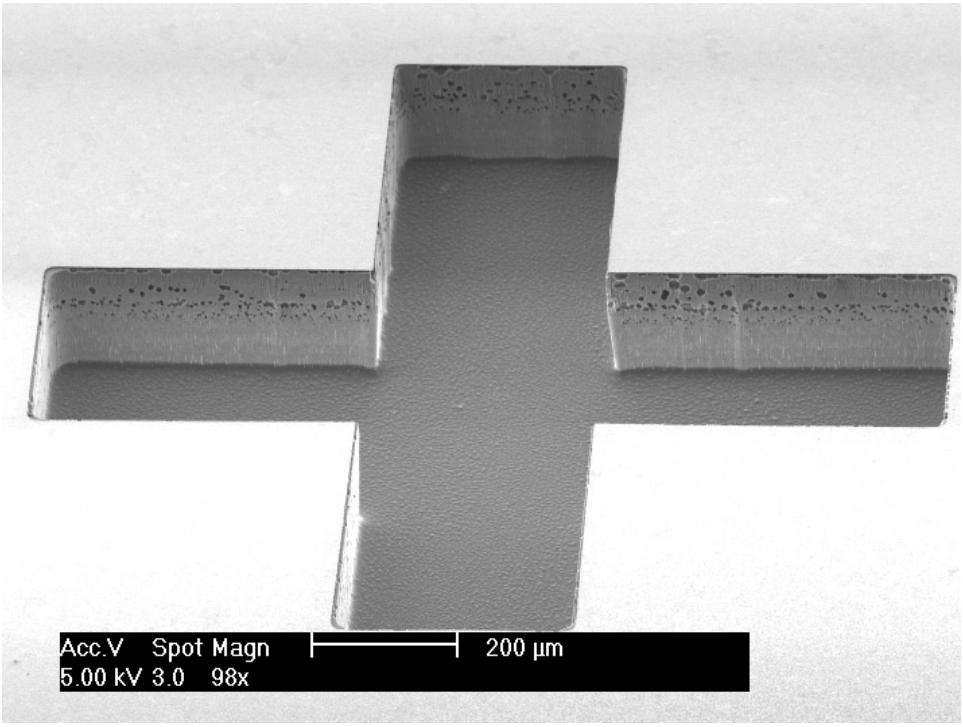


Figure 6.9: Scanning electron image of DRIE etched alignment mark.

6.2.4 Measured Results

The measured response of the vertical back-to-back RF transition is displayed in Fig. 6.10. In order to demonstrate that the effects of the DC bias lines have been removed two cases are included in this figure. The transition is measured by itself and subsequently the DC vias and bias lines are added. By comparing the two results it is obvious that the addition of the bias lines has no effect on the RF response of the package. The measurements summarized in the figure include a 2.7 mm through line; therefore the total insertion loss is around 0.3 dB at 40 GHz. If the losses from the FGC feeding lines are deembeded, the transition demonstrates a 0.06 dB loss up to 40 GHz and thus the loss due to each individual via transition is again 0.03 dB. Additionally, the return loss is below -20 dB up to 40 GHz and therefore the

transition is applicable for operation even higher than 40 GHz.

In the subsequent figure (Fig. 6.11) the measured results of the transition including the bonding ring are presented. As was previously mentioned, the reduction of its length moved the resonant frequency at 38 GHz. From the graph it is observed that the measurement very closely approximates the theoretical expectation. The inclusion of the bonding ring reduces the operational bandwidth of the package below 40 GHz. However, if a non-hermetic or polyimide sealing is utilized (for non-MEMS applications) the package can be operated at higher frequencies.

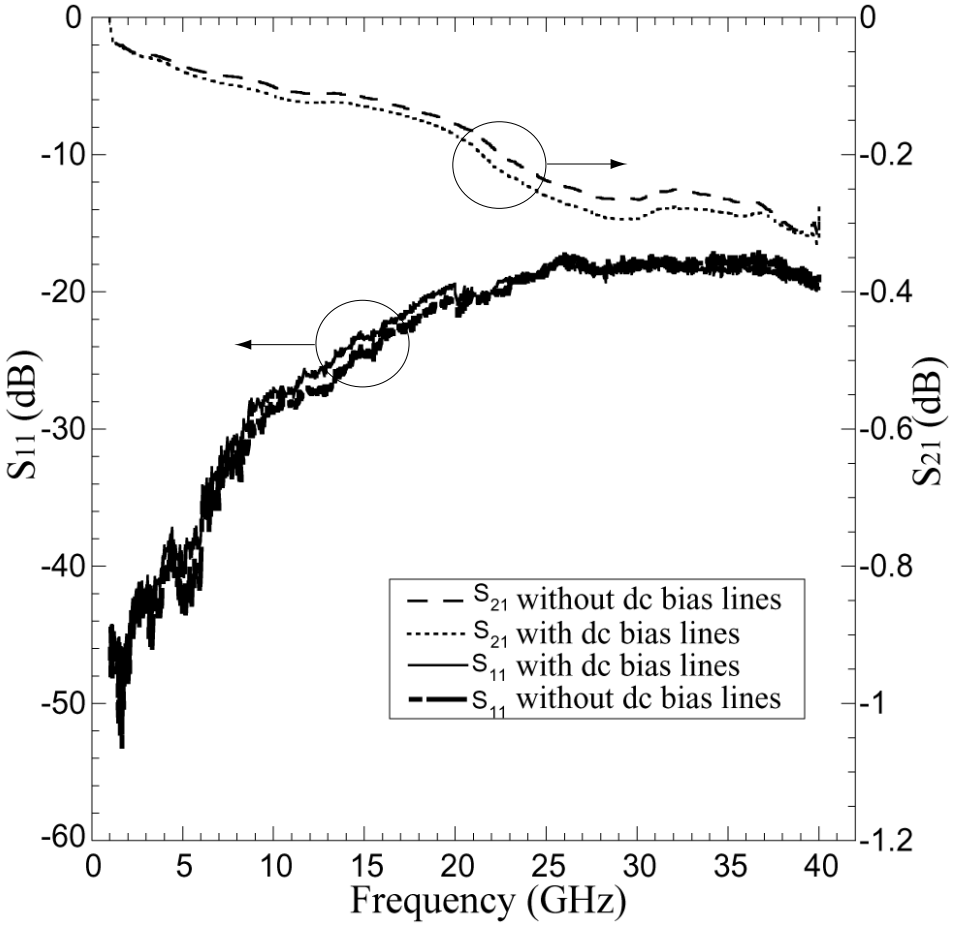


Figure 6.10: Measured response of RF back-to-back transition with and without DC bias lines and vias.

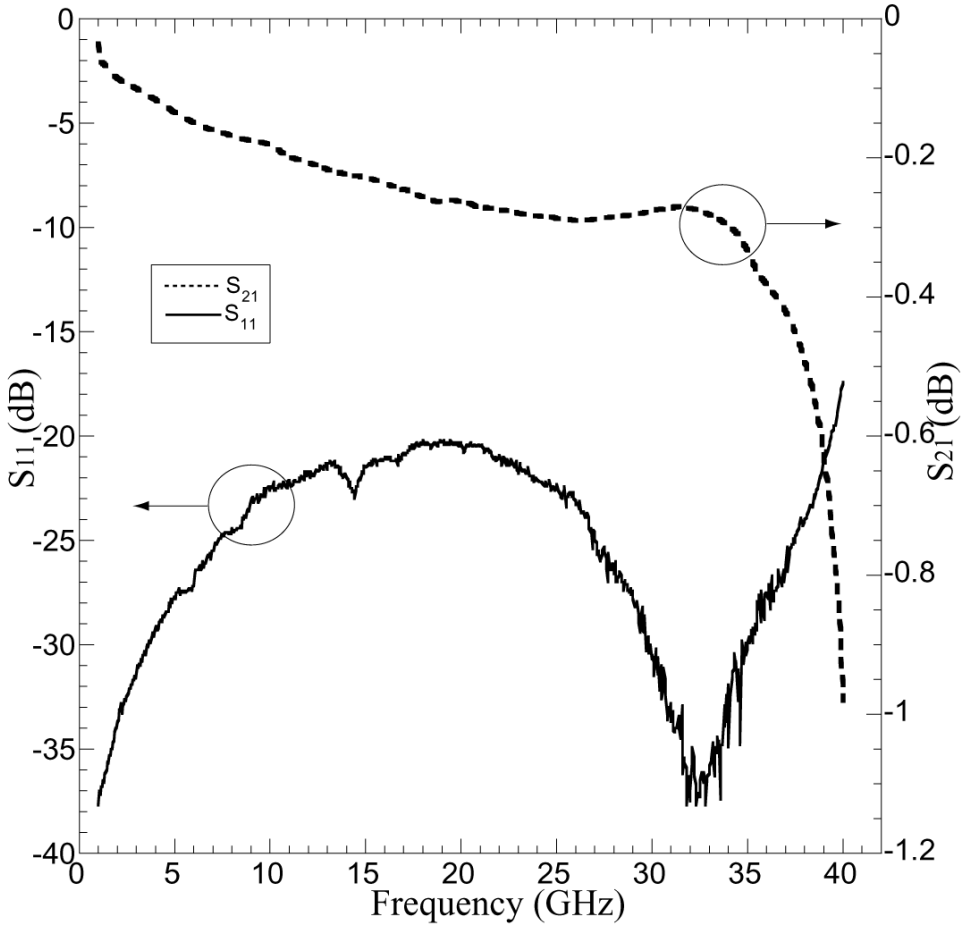


Figure 6.11: Measured response of RF back-to-back transition including the Au bonding ring.

6.3 Hermeticity Testing

6.3.1 Testing Structure

A suitable package for encapsulation of RF MEMS needs to offer both exceptional RF performance and hermetic sealing. The actual moisture content inside the package is made up of contributions from moisture released by the sealing materials and the package itself, the sealing ambient, and the moisture leaking through the seal. In order to test for hermeticity, the environment inside the package must be monitored for moisture penetration. This can be done by two types of structures: humidity

and dew-point sensors [142]. Humidity sensors have been extensively used for RH measurements. They consist of a porous dielectric layer sandwitched between two electrodes. Any water penetrating the package gets traped in this dielectric layer, and therefore it increases the measured capacitance of the sensor [143, 144]. The sensor presented in [143] for example is highly linear (non-linearity is calculated to be less than 2%RH), stable (drift was less than 3%RH after 10 days of testing), and its hysterisis is about 1.75%RH. The integration of an electroplated copper coil on the sensor [145] creates a resonant structure whose resonant frequency changes with respect to the absorbed humidity. Such a sensor has the additional advantage that it can be monitored from outside the package using a low frequency loop antenna. Humidity sensors are excellent candidates for a HAST test, unfortunately their fabrication process is relatively complicated.

In contrast, a dew-point sensor is based on an interdigitated structure and has been previously used for lifetime testing of hermetic packages [146, 147]. The operating principle is based on a large impedance change between the closely spaced electrodes of the sensor, which can be detected outside of the package though the via-holes. Once moisture condenses on the surface of the electrodes, the total impedance of the dew point sensor will decrease and this can be measured through micromachined vias by an impedance meter. The structure is simple, compatible with the fabrication technology used, and has good sensitivity. Since this accelerated test is viewed as an initial attempt to characterize the hermeticity of the RF package the simplicity of the dew-point sensor made it very appealing. As will be mentioned later, a more extensive test based on He leakage measurement (MIL-STD-883) is necessary for demonstrating the package's ability to be used for military and space applications. The fabrication of the dew-point sensor is performed by depositing a thin layer of Cr/Au using a lift-off process. The only challenge is the integration of the interdigitated structure with the micromachined vias. A scanning electron image of the fabricated sensor is

presented in Fig. 6.12 and Fig. 6.13.

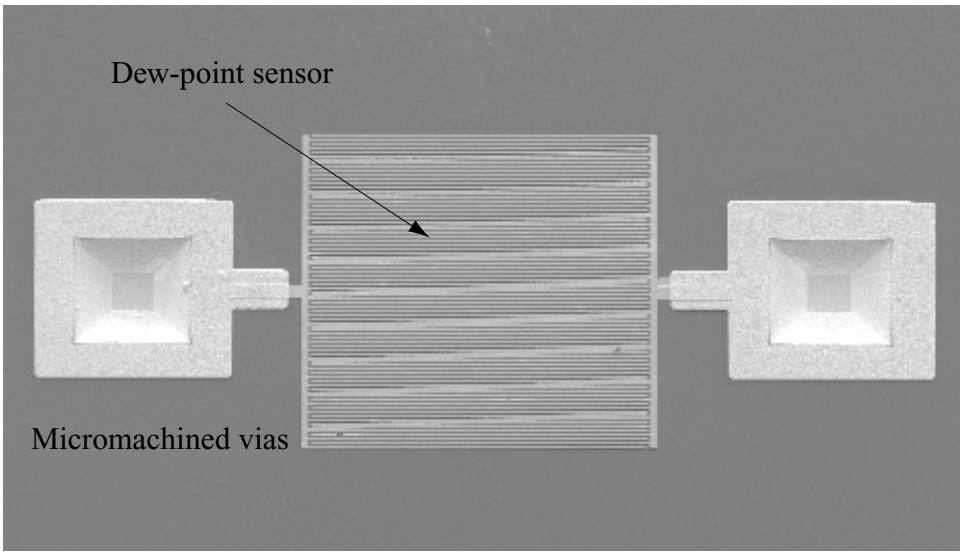


Figure 6.12: Fabricated dew-point sensor for hermeticity testing.

6.3.2 Testing Procedure

The accelerated testing is performed in an autoclave chamber provided by Prof. Najafi at the Wireless Integrated Microsystems (WIMS) center in the University of Michigan. The devices are placed inside the chamber filled with high temperature and pressurized steam (130^{o}C, 2.7 atm, 100% RH). The pressurized steam can penetrate small crevasses caused by bonding effects. Moreover, the elevated temperature and humid environment can raise corrosion against the bonding interface. The packaged dew-point sensors are removed from the autoclave and their impedance is measured using a probe station and an HP impedance meter. A photograph of the measurement set up is presented in Fig. 6.14

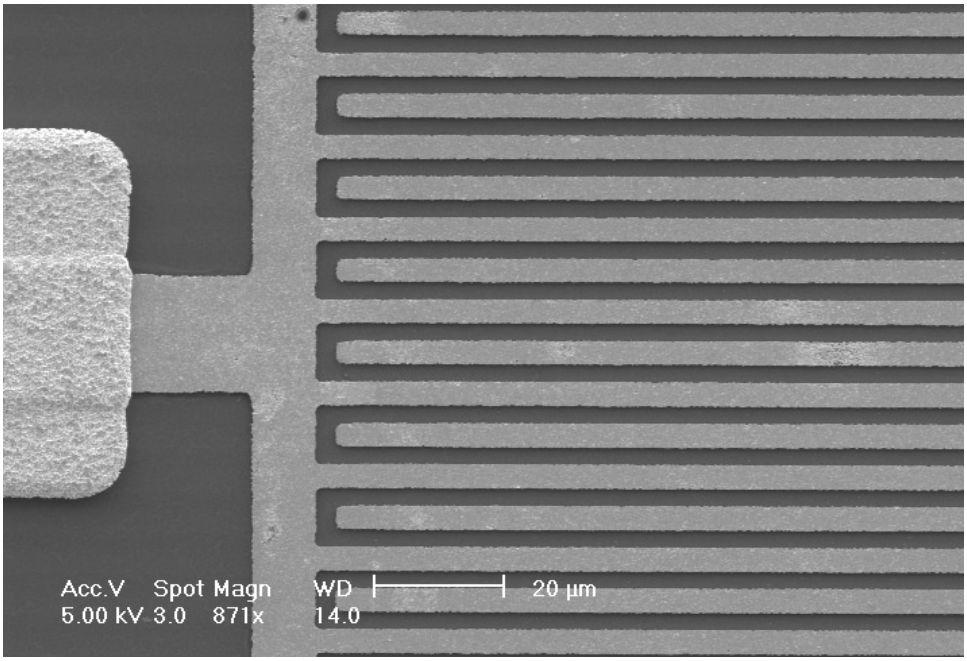


Figure 6.13: Detail of the fabricated dew-point sensor.

6.3.3 Measured Results

The first set of sensors is packaged under vacuum. Each packaging cavity included a dew-point sensor and two vias as illustrated in Fig. 6.12. The outcome of this experiment is presented in Fig. 6.15 where it is shown that 12 samples are destroyed in the first hour and the last sensors failed after 750 hours inside the chamber. It is interesting to notice that the failures initiated at the edges of the wafers, where the bonding is not ideal, and slowly move towards the center of the silicon piece. A typical measured response of one of the sensors is presented in Fig. 6.16 where an increase in the impedance phase is obvious after 120 hours of testing. Based on these results the failure rate graph is presented in Fig. 6.17. After the completion of the test the acquired data are fitted with a Weibull distribution. Performing a least square analysis the values of the life and shape parameters are extracted (β=0.745, λ=184) and subsequently the MTTF is evaluated. The final results are included in Table 6.1, from where it is observed that the MTTF is 220 hours. Compared to an 85/85 test

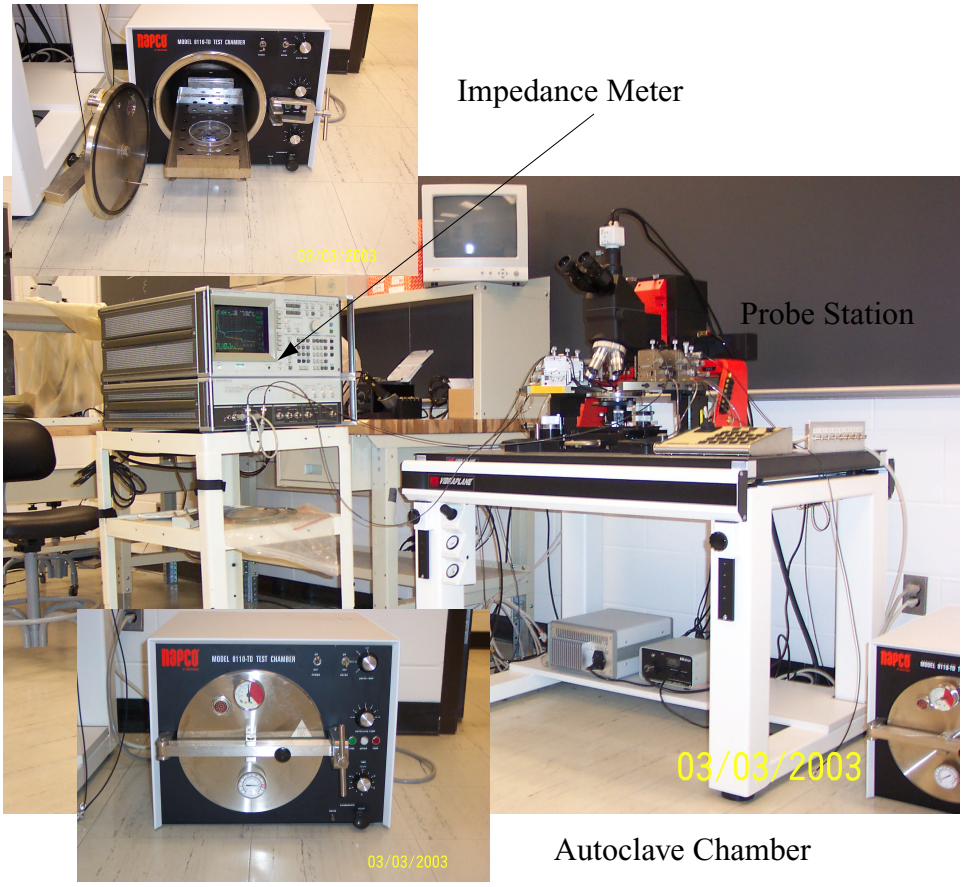


Figure 6.14: Measurement set up for accelerated tests.

the acceleration factor is 42 and thus the MTTF in such conditions will be 385 days. The 90% confidence intervals [148] are 296.3 days to 473.7. Based on the same model the AF for jungle conditions (35^{o}C, 95%RH) is 3400 and therefore the MTTF will be 86.5 years with a 90% interval ranging from 65.7 to 105.1 years.

Sealing RF MEMS under vacuum is not the best approach. An atmosphere of an ambient gas is necessary in order to be used as a damping mechanism for the switch membrane. Ideally this gas should be Ar or N_2. Unfortunately this was not available at the time of the testing and therefore an atmosphere of dry clean room air is sealed inside the package. There is a second advantage in having a 1atm gas inside the cavity. If there exists a leakage channel around the seal, there will be no pressure difference between the outside environment and the inside of the package

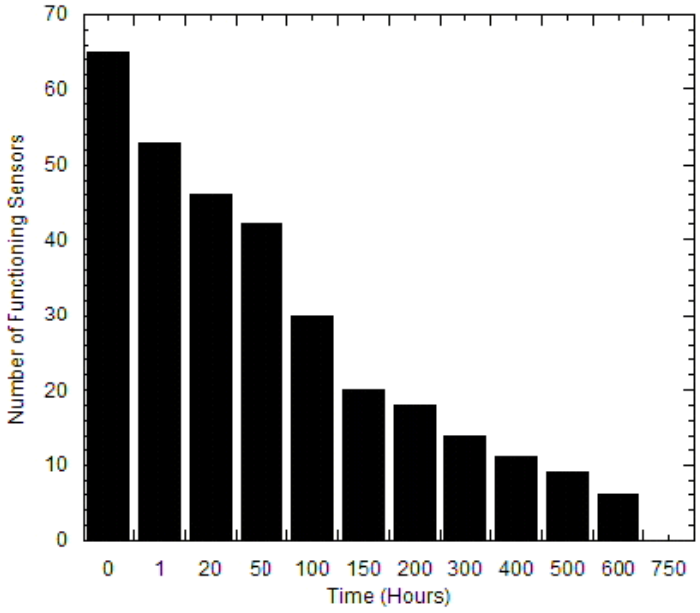


Figure 6.15: Operating dew-point sensors with respect to time.

Table 6.1: Results for packages under vacuum

Conditions	Acc. Factor	MTTF	90% Lower Interval	90% Upper Interval
130^{o}C,100%RH		220 hours	169.3	270.7
85^{o}C,85%RH	42	385 days	296.3	473.7
35^{o}C,95%RH	3400	86.5 years	65.7	105.1

to cause humidity to flow inside. This is not the case when the packages are sealed under vacuum. Therefore a second set of sensors are created and bonded following this procedure.

The same accelerated test is performed. This time more attention is invested on the pre-bonding alignment, which resulted in a reduction of the early failures. The outcome of the test is summarized in Fig. 6.18. The test is terminated after 1000 hours with 12 sensors still operating. Working with censored data means that instead of using a least square technique to extrapolate the Weibull distribution parameters, a maximum likelihood estimation is utilized. This estimation takes into account the

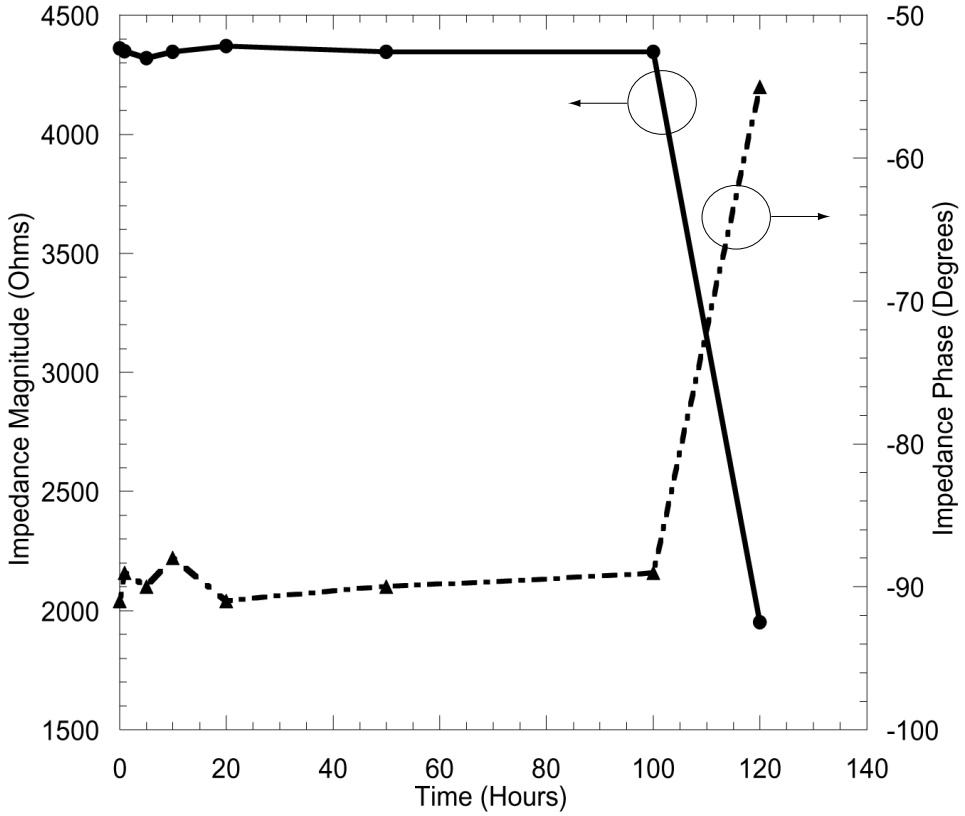


Figure 6.16: Typical response of dew-point sensor versus time inside the autoclave chamber.

number of samples that are still operating after the end of the test and evaluates the life and shape parameters of the distribution (β=0.768, λ=494). The failure rate for this experiment is shown in Fig. 6.19. Similarly to the previous case Table 6.2 illustrates all the results. As is expected the packages with the 1 atm of dry air perform significantly better with respect to their MTTF which is now 577 hours, although this improvement is partially attributed to better pre-bonding alignment as well. This results corresponds to 1010 days in 85/85 conditions (with a 90% confidence interval of 854.2-1165.3 days). Additionally, the MTTF in jungle conditions is 224 years with a 90% interval of 189.4-258.4 years.

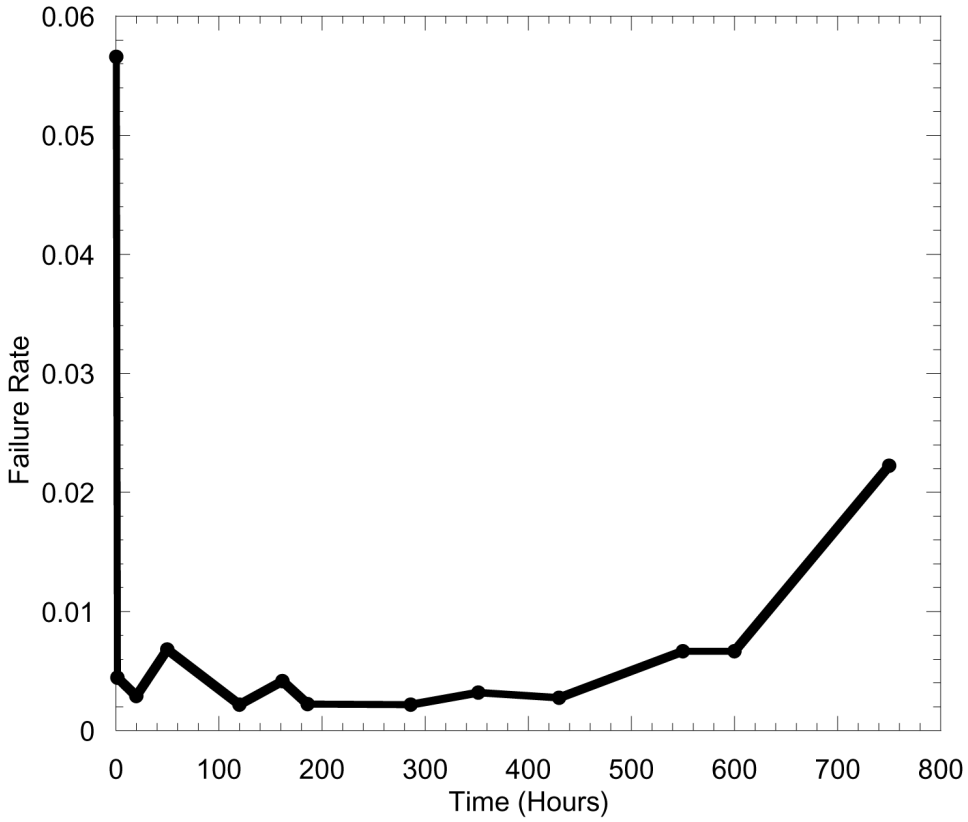


Figure 6.17: Failure rate for vacuum sealed sensors.

6.4 Conclusions

In this chapter an improved RF package is presented. Initially, the underlying theory behind accelerated testing and reliability metrology is presented. The process for eliminating the unwanted resonances on the measured response is analyzed in detail along with a new fabrication process that allowed the deposition of thicker metal layers. The measured results of the improved RF transition are also presented. The chapter ends with the results for the accelerated testing in an autoclave chamber which demonstrated its hermeticity.

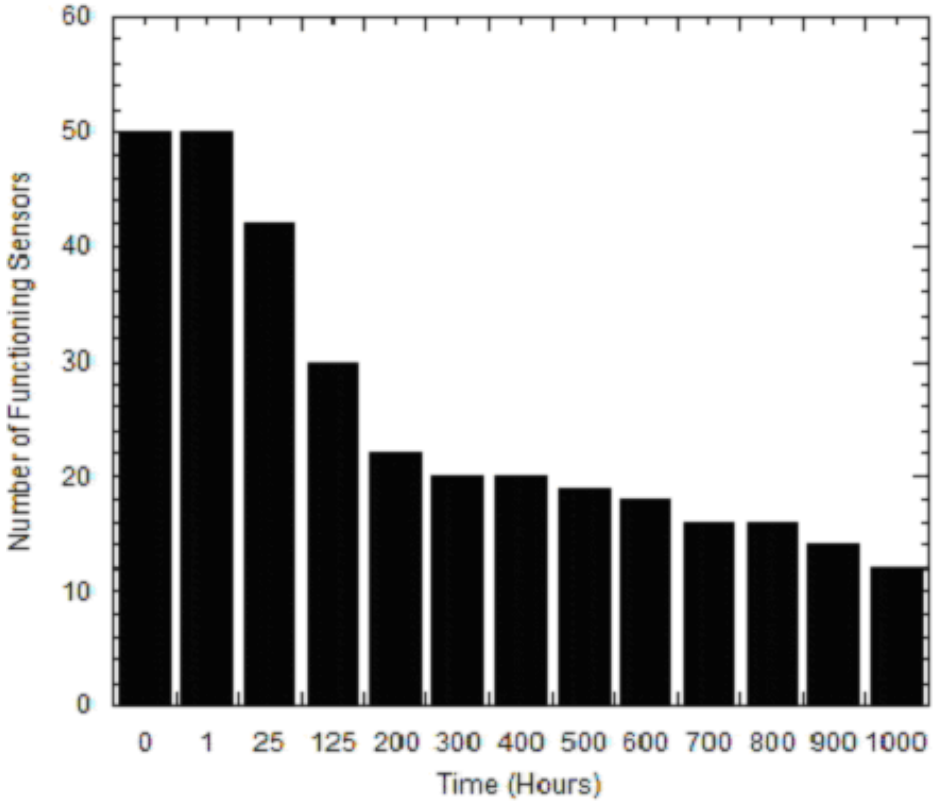


Figure 6.18: Operating dew-point sensors with respect to time.

Table 6.2: Results for packages under 1 atm of dry air

Conditions	Acc. Factor	MTTF	90% Lower Interval	90% Upper Interval
130^{o}C,100%RH		577 hours	488.1	665.9
85^{o}C,85%RH	42	1010 days	854.2	1165.3
35^{o}C,95%RH	3400	224 years	189.4	258.4

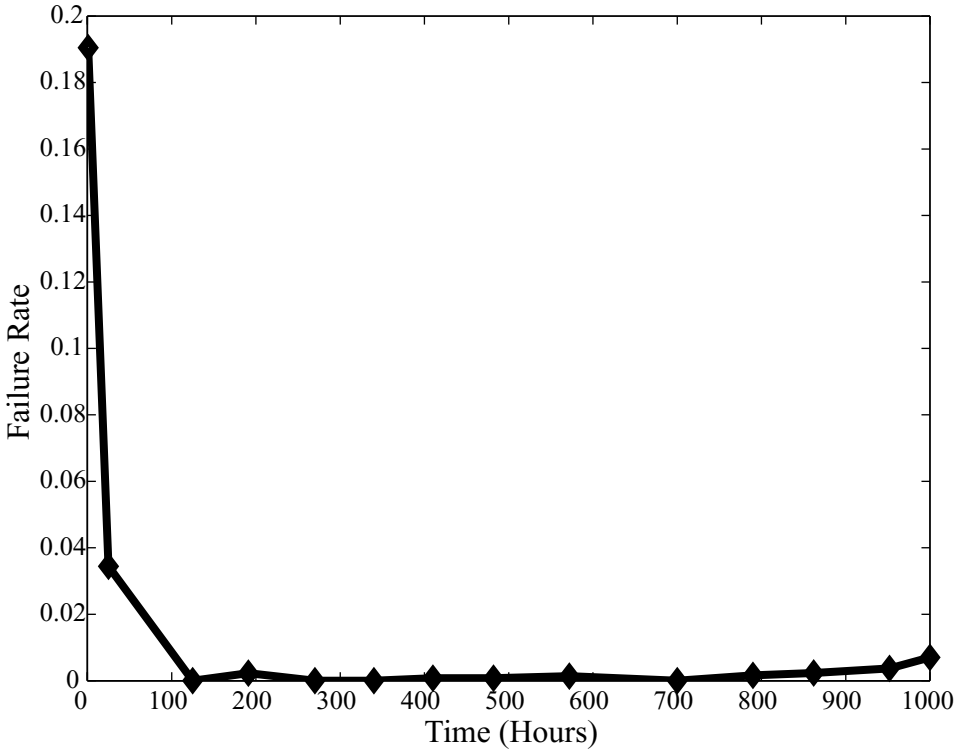


Figure 6.19: Failure rate for sensors packaged in dry air.

CHAPTER 7

Conclusions

7.1 Summary

THIS thesis presents a variety of novel structures made possible with the use of silicon surface and bulk micromachining. An extensive study for the isolation provided by various types of interconnects is presented. Multiple configurations of finite ground microstrip lines, finite ground coplanar waveguides (FGC), and transitions have been analyzed for silicon and duroid substrates. The results included in this thesis illustrate the implications of parasitic coupling associated with interconnects printed in parallel or perpendicular configurations, lines located in close proximity to open-end discontinuities, vias etched near FGC lines, and finally vertical transitions through wafers. The conclusions of this study can be employed in order to reduce parasitic interference between interconnects for both X and W-band.

Low-loss FGC waveguides and microstrip lines have also been investigated. The possibility of achieving good RF performance on low resistivity silicon wafers with the use of intermediate polyimide layers is proposed. The measurements presented demonstrate the feasibility of such an approach.

Evanescent mode filters micromachined on high resistivity silicon wafers have been included in this research. Such structures offer a high Q value and can be easily

integrated with other planar architectures. Due to their small size, these resonators can be tuned using appropriate MEMS devices.

Starting an investigation of possible tuning mechanisms for micromachined cavities led to the design of an on-wafer packaging scheme for RF MEMS switches. The final outcome of this effort, after two iterations involving improvements both in the fabrication process and the circuit layout, is a DC-to-40 GHz package with an insertion loss of 0.06 dB due to the via transitions. Since this is an on-wafer package no wire-bond or other type of interconnect is necessary for accessing the encapsulated device.

Nevertheless, in order for this package to be suitable for RF MEMS, its hermeticity needs to be demonstrated. An initial test design for this purpose is performed using packaged dew-point sensors placed inside an autoclave chamber. The measurements show a mean time to failure of 577 hours under accelerated harsh conditions (130^{o}C, 2.7 atm, 100% RH), while a statistical model relates this expected lifetime to normal operating conditions.

7.2 Future Work

7.2.1 Evanescent Mode Filters

The theoretical analysis of the evanescent mode filters is performed using HFSS. This three-dimensional FEM solver provided excellent results, however its computational efficiency is significantly impaired by the addition of microstrip transmission lines. A simulation tool combining various numerical methods (FEM/FDTD for three dimensional structure and MOM for planar architectures) will be an excellent asset for accurately solving such complicated structures. Such a tool can also help creating an equivalent circuit based on the geometrical characteristics of the filters (evanescent inductive sections or capacitive posts). This circuit is necessary in order to develop a

complete filter synthesis procedure, which will allow the design of filters with desirable response.

Evanescent mode filters are characterized by small sizes due to the ability of an excited evanescent wave to vary fast with distance. This property may be used to tune the filter since small variations in the geometrical characteristics of the cavity caused by appropriately located MEMS devices can result in large variations in the center frequency and bandwidth. Two tuning mechanisms are proposed for achieving this additional functionality. Metal-to-metal or capacitive switches can be fabricated on the external slots, thus effecting the external coupling, or on an internal slot located next to an auxiliary cavity, effecting the internal coupling. Moreover, a moveable membrane can be suspended over the capacitive posts and can be used to adjust the gap between the posts and the top wall of the cavity. Simulation results show that significant frequency hopping can be achieved with such a mechanism.

Fabricating tunable evanescent mode filters requires a repeatable and reliable fabrication process providing very accurate control of the distance between the post and the cavity walls. Such a possible fabrication process utilizing three silicon wafers and DRIE has been proposed.

7.2.2 Packaging of RF MEMS

Alternative Fabrication Technique for via-holes

In the work presented in this thesis wet anisotropic etching has been utilized for creating vias. A new method for depositing thicker metal layers is developed. However, completely filling the vias with metal using this procedure is not possible. An attempt to electroplate gold inside wet etched vias failed because the Au was attached to the bottom wall of the via, but could not be deposited on the slanted sidewalls of the cavities. The outcome of the process is a mushroom shape of gold plated at the center of the via-hole.

One alternative for creating filled vias is the use of DRIE for etching the silicon, which will result in rectangular holes through the wafers. A process for creating such vias and metallizing them with MoCVD deposited Cu has already been established. However, until now this process is only capable of metallizing blind vias etched in thick silicon wafers and is not applicable for gold. Designing a new fabrication process for creating completely filled vias that are capable of connecting interconnects on both sides of a silicon wafer will be a significant step. Furthermore, utilizing such via transitions will allow the operation of the presented RF on-wafer package above 60 GHz, since the smaller area required for the DRIE vias can lead to a shorter bonding ring. An initial attempt to create such vias has been performed during the work for this thesis and has demonstrated some difficulties which will need to be addressed. The sidewalls of the DRIE etched vias are almost vertical and rough, which makes them extremely difficult to metallize. An extensive characterization of the STS DRIE can succeed in developing a process that forms smooth sidewalls slightly slanted. Such a characterization will need to involve different masking materials, gas ratios, and via dimensions.

Hermeticity Testing

Evaluating the ability of a package to withstand extreme environmental conditions, mechanical and thermal loadings requires extensive, well planned testing. Such a process is already under way in order to determine the quality of the on-wafer packaging scheme. The sealing quality of the package can be tested by a standardized He leakage test [149], during which the package is placed inside a He pressurized vessel. If a leak channel exists, some of the pressurized gas will enter the package. After removal from the vessel, the device under test is connected to a He leak detector and the leak rate of He is measured. Depending on the internal volume of the package the military standard sets the acceptable values of measurable He leak rate. Additionally,

thermal cycling [150] will be performed in order to demonstrate any mismatches in the thermal coefficients of the materials used. Moreover, the mechanical endurance will be tested with random and shock vibrations simulating a missile lift-off. Dynamic vibration and shock tests are performed to simulate the launch vibro-acoustics and upper-stage pyrotechnic separation events. Sinusoidal vibration covers mid-frequency (5-100 Hz) launch vehicle-induced transient loading events. Random vibration test simulates launch vehicle-induced acoustic excitations during lift-off, transonic and maximum dynamic pressure events. Random vibration takes place over a broad frequency range, from about 10 Hz to 2000 Hz. In a launching environment, random vibration is caused primarily by acoustic noise in the payload fairing, which in turn is created by external aerodynamic forces due to dynamic pressure and reflection of rocket exhaust from the ground. Pyroshock test simulates the structurally transmitted transients from explosive separation devices, including pyrotechnic fasteners utilized to separate the spacecraft from the upper stage of the missile.

For the purposes of this test a new capacitive MEMS device is designed and its schematic is presented in Fig.7.1. Due to the difference in the up and down capacitance of the cantilever beam, a measurement will immediately illustrate if the switch is in the up or down position following a mechanical vibration test and thus if it survived the test or collapsed due to the mechanical loading.

After characterizing the package and demonstrating its reliability, the encapsulated RF MEMS switches can be utilized as tuning mechanisms for a variety of structures. Steerable and tunable antennas with on-wafer packaged MEMS will be possible, along with tunable components such as filters, phase shifters, and matching networks.

Theoretical Analysis

Theoretical models for the description of the thermal and mechanical loading on both the RF MEMS switch and the package are necessary. Such models, combined

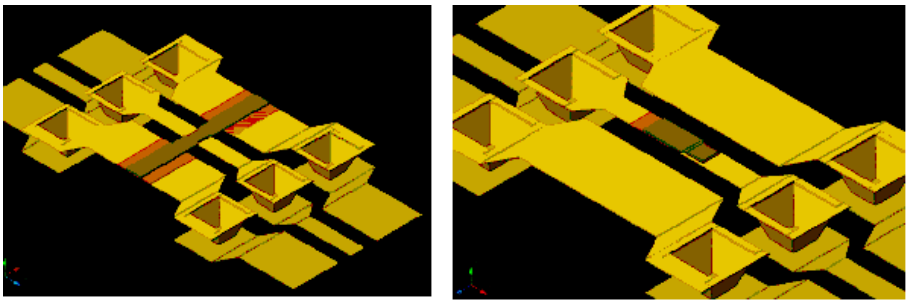


Figure 7.1: Schematic of the proposed MEMS based structures for reliability testing.

with the aforementioned reliability tests will be extremely helpful in pinpointing the failure mechanisms of the structure. Locating the correct failure mechanisms is the first step for improving both the package's and the MEMS' reliability and lifetime. As an example, theoretical and experimental work have demonstrated an increase in the temperature of the RF MEMS during its operation [151, 152]. An appropriate cooling mechanism can be introduced in the package to accommodate for this effect. Moreover, humidity and temperature sensors can be integrated inside the package for in-vivo testing.

Novel RF Transition

Based on the technology described in this thesis a more compact RF transition for on-wafer packaging can be created. Instead of using two wafers for forming the RF transition and the packaging cavity, the vias and the cavity can be integrated in a single wafer. This means that accessing the encapsulated device will be done from the top of the wafer. For such a design to be successful a wafer-to-wafer transition will be necessary along with some careful design of the lines in order to avoid possible mismatches. There are some major advantages involved with such an approach. The RF MEMS will be fabricated on an independent 400 μm thick wafer, which, if thermal mismatch issues are resolved, could be different from silicon. Additionally, separating the package from the MEMS, while keeping the on-wafer nature of the

design, provides unprecedented flexibility, by allowing mass production of packages and MEMS at different foundries and subsequent sealing.

APPENDICES

Appendix A

Isolation Study

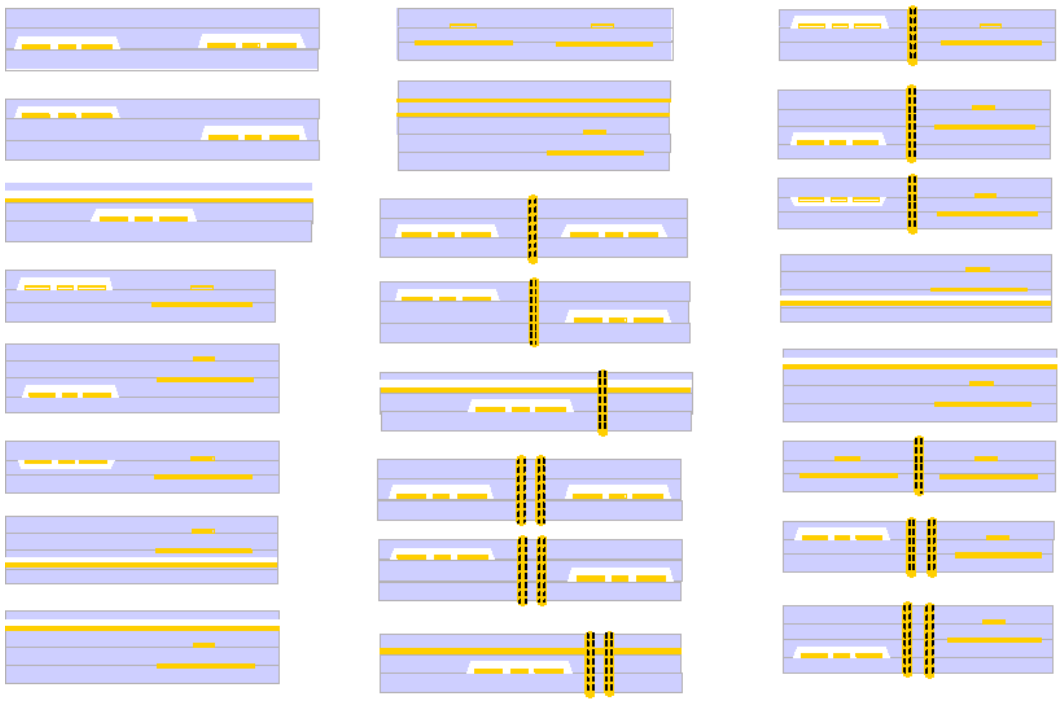


Figure A.1: Structures analyzed for isolation at 8 and 32 GHz.

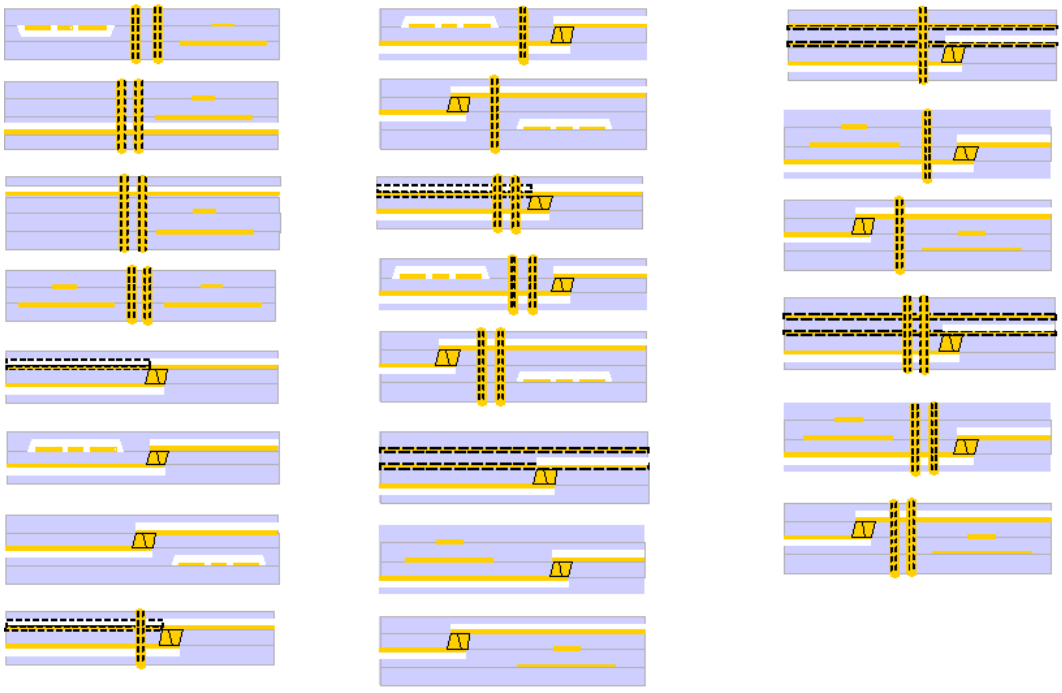


Figure A.2: Structures analyzed for isolation at 8 and 32 GHz.

Appendix B

Fabrication Processes

B.1 Introduction

This appendix provides detailed fabrication processes for the various structures presented in this thesis. Section B.2 lists the wafer cleaning procedures. In Section B.3 handling details for wafers of various thicknesses are mentioned. In Section B.4, the process parameters for the various photoresists used in this work are given. Section B.5 details the electrophoretic photoresist deposition. The fabrication steps necessary to etch silicon wafers in TMAH and KOH are summarized in Sections B.6 and B.7 respectively. Section B.8 provides the deep reactive ion etching parameters. Section B.9 gives an accounting of the fabrication steps for creating various types of interconnects. Finally, Section B.10, describes the formation of RF MEMS switches.

B.2 Wafer Cleaning

1. Solvent clean
   (a) Soak in acetone for 2 minutes.
   (b) Soak in isopropyl alcohol for 2 minutes.
   (c) Dry using N_2 gun.

2. Organic "piranha" clean
    (a) Mix 1:1 hydrogen peroxide and sulfuric acid.
    (b) Soak sample in solution for 10 minutes.
    (c) Rinse in de-ionized (DI) water for 10 minutes.
    (d) Dry using N_2 gun.

B.3 Silicon Wafer Handling

1. 100 μm and 200 μm thick silicon wafers
    (a) Spin positive photoresist 1827 on appropriately diced glass slide at 2.5 krpm.
    (b) Swab edges of slide with acetone.
    (c) Mount wafer on glass slide, carefully pressing corners.
    (d) Softbake on hotplate for 2 minutes at 80^{o}C.
    (e) Hardbake on hotplate for 3 minutes at 130^{o}C.
2. 400 μm and 500 μm thick silicon wafers
    (a) Dice wafers to appropriate dimensions.
    (b) If backside protection of the SiO_2 is needed, spin 1827 and hardbake for 2 minutes at 130^{o}C.
    (c) No mounting on glass slides in necessary.

B.4 Photoresist Recipes

1. HMDS Adhesion Promoter
    (a) Spin adhesion promoter at the same speed as the given photoresist.
    (b) Spin for 30 sec.
2. Positive Photoresist 1827

(a) Spin photoresist at 3 krpm for 30 sec.

(b) Align and expose for 12 sec.

(c) Develop in MF 351:DI (1:5) for 40 sec.

(d) Hardbake on hotplate for 3 minutes at 130^{o}C.

3. Image Reversal Photoresist 5214

(a) Spin photoresist at 2.5 krpm for 30 sec.

(b) Soft bake on hotplate for 2 minutes at 105^{o}C.

(c) Align and expose for 4.5 sec.

(d) Image reversal bake for 1 minute at 130^{o}C.

(e) Flood expose with clear mask for 90 sec.

(f) Develop in AZ 327 for 40 sec.

4. Positive Photoresist 9260

(a) Spin photoresist at 4 krpm for 30 sec.

(b) Rest wafer horizontally for 20 minutes.

(c) Soft bake on hotplate for 3 minutes at 110^{o}C.

(d) Align and expose for 45 sec.

(e) Develop in AZ 400k:DI (1:3) for 1-2 minutes.

(f) Hardbake in oven for 30 minutes at 90^{o}C.

5. Positive Photoresist 1813

(a) Spin photoresist at 2 krpm for 30 sec.

(b) Soft bake on hotplate for 2 minutes at 105^{o}C.

(c) Align and expose for 7 sec.

(d) Develop in MF 351:DI (1:5) for 20 sec.

(e) Hardbake on hotplate for 3 minutes at 130^{o}C.

B.5 Electrodeposited Photoresist

1. Solution preparation
   (a) Fill PEPR-2400:DI (1:1) mixture up to 1800 ml.
   (b) Set stirrer to 200 rpm.
   (c) Set hotplate probe at appropriate temperature.
2. Deposition preparation
   (a) Turn on HP 6035A power supply.
   (b) Run appropriate deposition routine from the computer.
   (c) Select deposition time and voltage.
   (d) After deposition is completed, remove sample from photoresist beaker.
   (e) Rinse sample with DI water.
   (f) Dry using N_2 gun.

B.6 Wet Anisotropic Etching in KOH

1. Wafer Preparation
   (a) Use 1827 to pattern features as described above.
   (b) Etch SiO_2 using BHF at a rate of 1000 Å/min.
   (c) Remove remaining photoresist in acetone overnight.
   (d) Soak wafer in IPA.
   (e) Dip in BHF for 30 sec to remove any native oxide.
   (f) Rinse and place in DI water.
2. KOH etch
   (a) Fill beaker with 700 ml of DI water, set stirrer at 300 rpm and hotplate probe at 30^{o}C.
   (b) Slowly add 350 gr of KOH.
   (c) Since process is exothermic, wait until temperature is stabilized before

adding more KOH to the solution. Keep temperature below 85^{o}C.

(d) Set hotplate probe temperature at 65^{o}C.

(e) Immerse wafers in solution.

(f) After completion of the etch, rinse wafers in DI water.

(g) Dry using N_2 gun.

B.7 Wet Anisotropic Etching in TMAH

1. Wafer Preparation

   (a) Use 1827 to pattern features as described above.

   (b) Etch SiO_2 using BHF at a rate of 1000 Å/min.

   (c) Remove remaining photoresist in acetone overnight.

   (d) Soak wafer in IPA.

   (e) Dip in BHF for 30 sec to remove any native oxide.

   (f) Rinse and place in DI water.

2. TMAH etch

   (a) Fill beaker with 150 ml of TMAH, set hotplate probe at 85^{o}C.

   (b) Immerse wafers in solution, watch for the formation of bubbles revealing the etching of silicon.

   (c) After completion of the etch, rinse wafers in DI water.

   (d) Dry using N_2 gun.

B.8 DRIE Process Parameters

1. Wafer Preparation

   (a) Use 1827 to mount samples on 4 inch full thickness silicon wafer.

   (b) Hardbake mounted samples in oven for 30 minutes at 120^{o}C.

2. Etch preparation

   (a) Load samples.

   (b) Pump down time 30 sec.

   (c) He leak test, duration 1 minute.

   (d) Maximum permissible He rate 10 mT/min.

3. Etch process

   (a) Pump down time 30 sec.

   (b) Gas stabilization.

   (c) User defined process time.

   (d) Pump out time is 30 sec.

   (e) Passivation for 7 sec.

   (f) Etching for 13 sec.

   (g) APC mode manual.

   (h) APC setting is 67^o.

   (i) Base pressure is 0.2 mT.

   (j) Pressure trip is 94 mT.

   (k) C_4F_8 flow is 85 sscm.

   (l) SF_6 flow is 160 sscm.

   (m) O_2 and Ar flow are 0 sscm.

   (n) RF power is 250 W.

   (o) Coil generator: etch is 800 W, and passivation is 600 W.

   (p) Platten generator: etch is 250 W, passivation is 0 W.

B.9 Thin Film Metal Deposition

1. Lift-off process

   (a) Use 5214 to pattern features as described above.

(b) Evaporate Cr/Au, 500/9500 Å.

(c) Soak samples in acetone overnight.

(d) Rinse wafer in IPA.

(e) Dry using N_2 gun.

2. Electroplating process

(a) Flood sputter (or evaporate) a seed layer of Cr/Au.

(b) Heat Orotemp Au-platting solution at 55^{o}C and set the stirrer at 200 rpm.

(c) Mount sample on cathode holder.

(d) Adjust power source until appropriate current density is achieved.

(e) Rinse wafer in DI water.

(f) Dry using N_2 gun.

B.10 RF MEMS

1. Evaporate lower FGC interconnect using lift-off.
2. A thin layer of plasma enhanced chemical vapor deposited (PECVD) silicon nitride is patterned over the location of switch actuation.
3. Spin a sacrificial layer of 3μm thick polyimide DuPont PI2545, soft bake it, and pattern it for anchor points.
4. Electroplate 2 μm of Ni to define the switch structure.
5. Etch the sacrificial layer of the polyimide using hot PRS-2000.
6. Perform supercritical CO_2 drying and release the switch membrane.

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