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Design and Analysis of Series and Shunt MEMS Switches

by

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A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
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To my mother and father,
Jean and Roger Muldavin.

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PREFACE

This thesis presents series and shunt RF Micro-Electro-Mechanical (MEMS) switches and varactors, emphasizing the electromagnetic modeling and design as well as mechanical modeling. Comprehensive modeling and design are verified by extensive fabrication and testing of both series and shunt MEMS devices. These devices were implemented into high-isolation (-60 to -40 dB from 2 to 40 GHz) switch circuits. Also, a detailed electro-mechanical 1-dimensional dynamic simulation has been done for MEMS switches and varactors. It is also the author's goal to establish general performance parameters and limitations of MEMS devices.

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CHAPTER 1

INTRODUCTION

1.1 What are MEMS Switches and What are They Good For?

One of the fundamental components of any modern electronic circuit is a variable impedance. The simplest example of a variable impedance is the mechanical switch that you flip off every night when you turn off the lights before bed. From the mechanical movement provided by your fingers, the switch changes its reactance from a direct contact (DC) short to an open circuit, interrupting the flow of electrical current to the light bulb. Semiconducting devices such as diodes and transistors can also act as switches, interrupting or allowing the flow of electricity. In this case, the variable impedance is caused by applied bias voltages that change the impedance, or ability of the semiconducting material to conduct electricity. Micro-Electro-Mechanical (MEMS) switches are devices which use mechanical movement to achieve a short circuit or an open circuit in the radio frequency (RF) transmission-line. These devices are extremely small, about the width of a human hair (45-65 μm). Figure 1.1 shows part of a MEMS device is shown on a penny to give an idea of the size.

RF MEMS switches are the specific micro-mechanical switches which are designed to operate at RF to mm-wave frequencies (0.1 to 100 GHz). The forces required for the mechanical movement can be obtained using electrostatic, magneto-static, piezoelectric or thermal designs. As of the year 2001, only electrostatic-type switches have been demonstrated at 1-100 GHz with high reliability (more than Millions of switch cycles, and in some



Figure 1.1: Photomicrograph of a MEMS device on a penny. (Courtesy Sandia National Labs.)

cases, Billions of switch cycles over the lifetime of the switch).

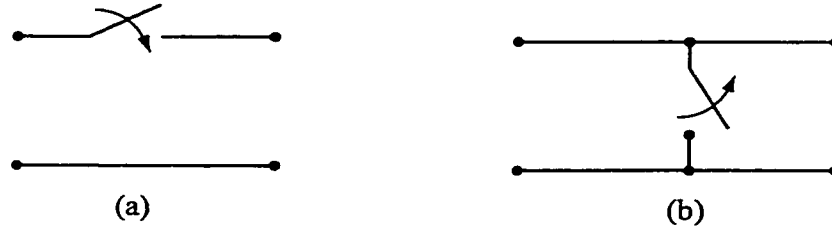


Figure 1.2: Series (a) and shunt (b) configurations of MEMS switches.

RF MEMS switches come in two configurations: series and shunt (Fig. 1.2). A series switch either interrupts the signal conductor (open circuit) or makes the signal conductor continuous through DC metal-to-metal contact. A shunt switch either shorts the signal conductor to the ground conductor (short circuit) or leaves them unconnected, allowing the signal to pass. Series switches are most suited to low frequency applications (0-30 GHz) and shunt switches are most suited to higher frequency applications (15-100 GHz).

Solid state devices such as PIN diodes or FET switches, are the current standard technology for RF switches. The advantages of MEMS switches over PIN diode or FET switches are:

1. *Extremely Low Power Consumption:* Electrostatic actuation requires 10-120 V, but consumes little current, leading to a very low power dissipation. This is advantageous in satellite systems, or in large re-configurable antennas or phased arrays requiring thousands of elements.
2. *Very High Isolation:* RF MEMS series switches are fabricated in air, and therefore, have very low off-state capacitances (2-8 fF) resulting in excellent isolation at 0.1-30 GHz.
3. *Very Low Insertion Loss:* RF MEMS series and shunt switches have an insertion loss of -0.1 dB up to 40 GHz since only metal layers are being used and not semiconductors.
4. *Very High Cutoff Frequency:* The figure of merit for a series switch is the cutoff frequency, $f_c = 1/(2\pi R_s C_u)$, where R_s is the resistance in the on-state (pass state) and C_u is the capacitance in the isolation state. The cut-off frequency is 30-80 THz

for MEMS switches while it is only 1-2 THz for PIN diodes and 0.2-0.5 THz for FET switches.

5. *Intermodulation Products:* MEMS switches are mostly linear devices and therefore result in very low intermodulation products. Their performance is around 30 dB better than PIN or FET switches.
6. *Low Cost and Easy Integration:* RF MEMS switches are fabricated using surface micromachining techniques, and therefore, can be built on quartz, Pyrex, LTCC, mechanical-grade high-resistivity silicon or GaAs substrates.

Despite all of these advantages, RF MEMS switches also have their share of problems. The presently largest disadvantage is that they are not currently commercially available. Several of the other disadvantages are:

1. *Relatively Low Speed:* The switching speed of most MEMS switches is around 3-40 μ s. This is acceptable for many applications except certain communication and radar systems.
2. *Reliability:* The reliability of mature MEMS switches is 0.1-4 Billion cycles. This is acceptable for many applications, but there is a large need for switches with 20-200 Billion cycles. Also, the long term reliability (years) has not yet been addressed.
3. *Packaging:* MEMS switches need to be packaged in inert atmospheres (Nitrogen, Argon, etc..) and in very low humidity, necessitating effectively hermetic or near-hermetic seals. For this reason, packaging costs are currently high and are unproven for MEMS switches. The packaging technique itself may adversely effect the reliability of the MEMS switch.
4. *Power Handling:* Most MEMS switches cannot handle more than 10-20 mW with high reliability, and 0.1-10 W MEMS switches simply do not exist today. It is the author's opinion that fundamental changes in the actuation mechanism and fabrication must be made to accommodate high power MEMS switches.

5. *Cost*: While MEMS switches have the potential of very low cost, it is hard to beat the cost of a \$0.3-0.6 single-pole double-throw PIN or FET switch, tested, packaged and delivered. MEMS switches still need a lot of time to break into the low cost wireless market, and will be first used in high-performance defense and satellite systems.

Having said the above, the main application areas of MEMS switches are (Fig. 1):

1. *Radar Systems for Defense Applications (5 to 94 GHz)*: Phase shifters for satellite-based radars (20 Billion cycles), missile systems (0.1-1 Billion cycles), long range radars (20-100 Billion cycles).
2. *Automotive Radars*: 24, 60 and 77 GHz (1-2 Billion cycles and 10 years).
3. *Satellite Communication Systems (12-35 GHz)*: Switching networks with 4×4 and 8×8 configurations and reconfigurable Butler matrices for antenna applications (0.1 Million cycles). Switched filter banks (0.1-100 Million cycles depending on the application). Also, phase shifters for multi-beam satellite communication systems (10-20 Billion cycles).
4. *Wireless Communication Systems (0.8-6 GHz)*: Switched filter banks for portable units (0.1-1 Million cycles), switched filter banks for basestations (0.1-10 Billion cycles), general SP2T to SP4T switches (0.1-10 Billion cycles), transmit/receive switches (2-4 Billion cycles and 5-20 μ s switching time), and antenna diversity SP2T switches (10-100 Million cycles).
5. *Instrumentation Systems (0.01-50 GHz)*: These require high performance switches, programmable attenuators, SPNT networks and phase shifters, capable of at least 20-40 Billion cycles and 10 years of operation, especially in industrial test benches.

1.2 Comparison of MEMS Switches with PIN Diode and Transistor Switches

To become commercially viable, the MEMS switch has to compare favorably over the PIN or FET in several areas. Table 1.1 shows a comparison between MEMS switches and

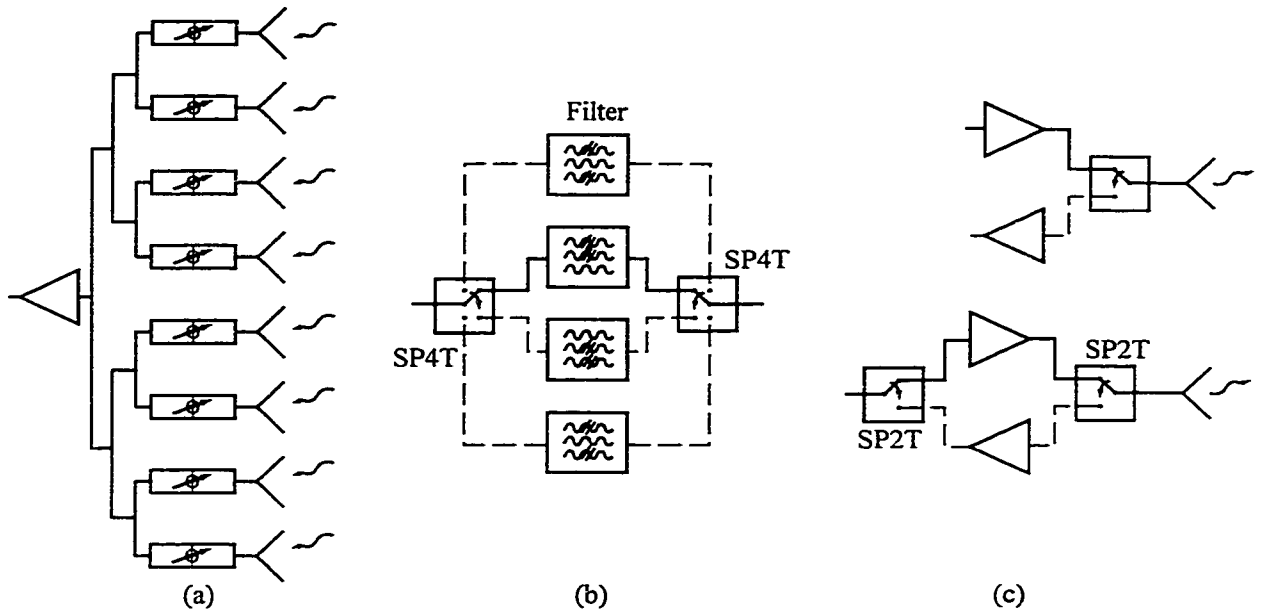


Figure 1.3: Some application areas of MEMS switches: Phased arrays (a), switched-filter banks for wireless applications (b) and SP2T T/R switches (c).

PIN diode and transistor switches. It is hard to make an accurate comparison over a large range of RF power levels since the size of diode and transistor switches can be easily increased for large power applications. This, in turn, has a substantial effect on the switch isolation, insertion loss, switching speed and power consumption. Still, it is evident that MEMS switches, for low to medium power applications, offer a far superior performance compared to solid-state switches (except in the switching time).

1.3 MEMS Market

The field of MEMS has seen tremendous growth in the recent years. Some accounts estimated MEMS as a \$10 Billion market in 2000 and projections of \$30 to \$40 Billion by 2002. MEMS technologies can allow the inexpensive integration of simple components into much more complex systems, giving significant advantages to RF and photonic systems. Current applications include accelerometers, pressure, flow, and chemical sensors, and micro-optical switches and displays. Accelerometers for automotive applications are

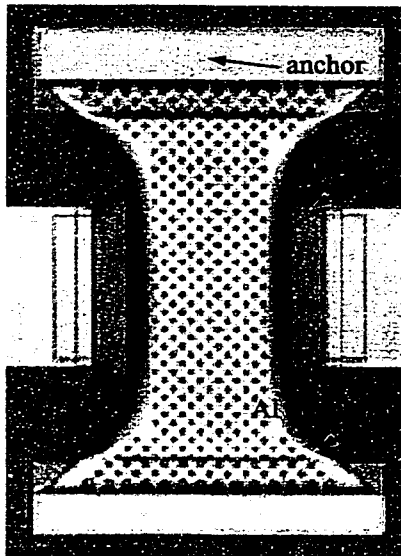
Parameter	RF MEMS	PIN	FET
Voltage [V]	30-80	± 3 -5	2-5
Current [mA]	0	± 3 -20	0
Power Cons. [mW]	0.03-0.06	5-100	0.05-0.2
Switching Time	1-30 μ s	2-60 ns	2-60 ns
C_{up} (series) [fF]	1-6	20-50	30-60
R_{on} (series) [Ω]	0.5-2	2-4	4-6
C_{up} (shunt) [fF]	20-80	n/a	n/a
R_{on} (shunt) [Ω]	0.05-0.25	2-4	4-6
Cutoff Freq. [THz]	20-80	1-4	0.3-0.5
Isolation (1-10 GHz)	V. High	High	Medium
Isolation (10-40 GHz)	V. High	Medium	Low
Isolation (60-100 GHz)	High	Medium	None
Loss [dB]	0.05-0.2	0.4-1.2	0.4-1.6
Power Hand. [W]	0.01-0.5	0.1-10	0.1-3
Intermodulation [dBm]	+66-80	+27-45	+27-45

Table 1.1: Performance comparison of FETs, PIN diode, and RF MEMS switches.

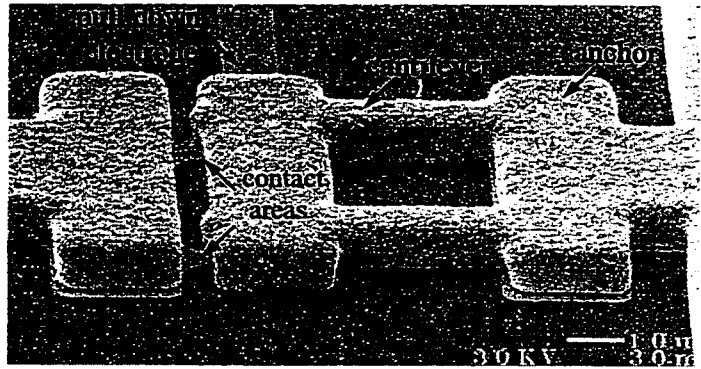
by far the largest part of the marketplace today, with optical and biomedical applications following close behind. RF MEMS are still mostly in the research and development stage but have great potential in the areas of automotive radar and wireless communications.

1.4 State of the Art

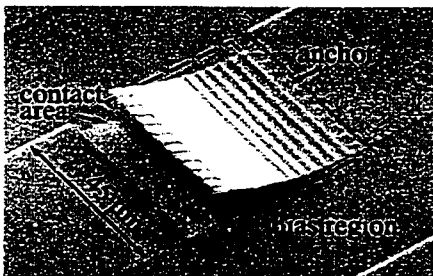
The following Industry, University and Government Laboratories are a few of the many that have developed RF MEMS shunt or series switches between 1994 and 2000: Raytheon, Analog Devices, Motorola, Rockwell Science Center, Hughes Research Labs, Samsung, NEC, Thomson-CSF, Lincoln Laboratories, U.S. Air Force Research Labs, University of California Berkeley, University of Michigan, and University of Illinois. Analog Devices, Motorola, and Rockwell Science Center have developed the most mature series switches. Raytheon has developed the most mature shunt switch. None of these companies expects to ship packaged MEMS switches before 2003. Examples of some of these switches are shown in Fig. 1.4.



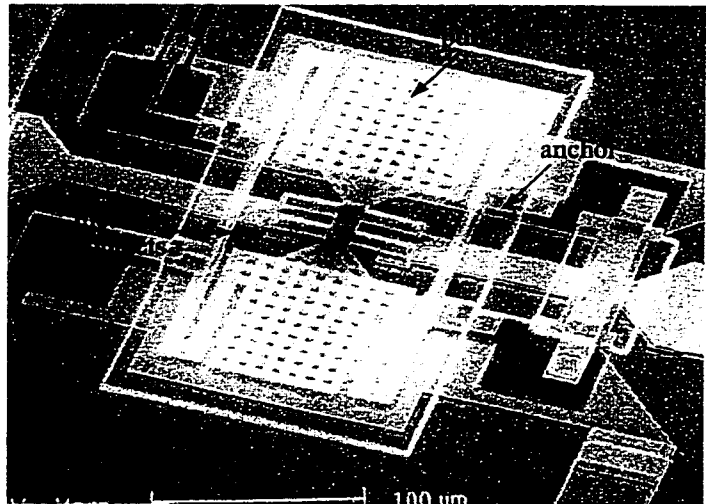
(a)



(b)



(c)



(d)

Figure 1.4: Photomicrographs of the Raytheon shunt capacitive (a), Analog Devices series (b), Lincoln Labs series (c), and Rockwell Science Center series (d) MEMS switches.

1.5 Fabrication Techniques

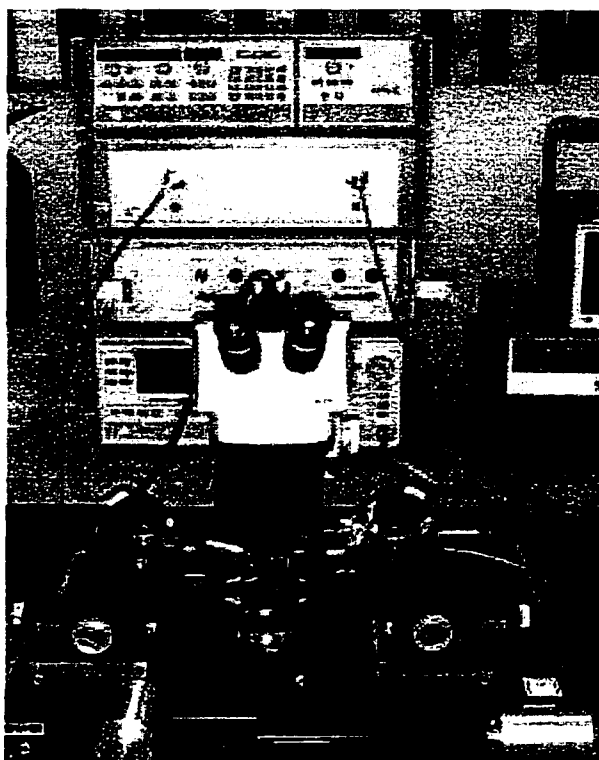
The advent of modern photolithographic techniques and surface micro-machining that has allowed the miniaturization and mass production of today's semiconductor integrated circuits has also allowed for the creation of micro-electro-mechanical devices. Photolithography is the process of depositing and patterning photo-sensitive materials, such as photoresist, on planar surfaces. These patterned materials are often used to mask a portion of the wafer from the effects of a particular process, such as evaporative deposition of metals, on the surface of a wafer. These masking materials can also be used to protect portions of the wafer from etching processes that selectively remove materials. The process of selectively depositing and removing materials from the surface of a wafer is known as surface micro-machining.

Because of the extremely small size, on the order of the width of a human hair, these fabrication techniques takes place in clean controlled environments. A piece of dandruff on the surface of a wafer is enough to ruin a circuit or device. Typical clean rooms are rated at class 100 to class 1000, meaning they have 100 to 1000 particles per cubic feet of air. The devices presented in this thesis were fabricated in a class 100 clean room at the University of Michigan. A detailed description of the fabrication techniques used to create the devices presented in this thesis is included in Appendix A.

1.6 Measurement Techniques

Because of the wave nature of high frequency signals, special equipment must be used to measure the electrical performance of RF MEMS. The most commonly used equipment is a vector network analyzer (VNA), which measure the voltage amplitude and phase at the input and output form of an RF device under test (DUT). The measurements in this thesis were performed using an HP8510C VNA capable of measuring signals from 0.2 to 110 GHz (see Fig. 1.5).

RF signals in a circuit environment are carried on transmission line (t-lines). Waveguides and coaxial cables are used to connect large components. Planar transmission lines



(a)



(b)

Figure 1.5: On wafer probe station (a) and HP8510C VNA (b) used at the University of Michigan.

are used to connect components on the surface of a wafer. On wafer probes connect the planar transmission lines to the coaxial cables and the network analyzer. These transmission lines and connectors change the magnitude and phase of the signals traveling to and from the VNA and the DUT. Calibration techniques are used to remove the unwanted effects and measure the performance of the DUT alone. The calibrations in this work were performed using an on wafer calibration technique called Multical, developed by NIST [1]. This technique uses the Thru-Reflect Line (TRL) method and on wafer standards, yielding very accurate loss data.

1.7 Thesis Overview

This thesis presents series and shunt RF MEMS switches and varactors, emphasizing the electromagnetic modelling and design as well as mechanical modelling. Comprehensive modelling and design are verified by extensive fabrication and testing of both series and shunt MEMS devices. It is also the author's goal to establish general performance parameters and limitations of MEMS devices.

CHAPTER 2

ELECTROMAGNETIC MODELING OF SHUNT SWITCHES

2.1 Introduction

There are two basic switches used in RF to millimeter-wave circuit design: The shunt switch and the series switch. The ideal series switch results in an open circuit in the transmission line when no bias voltage is applied (up-state position), and a short circuit in the transmission line when a bias voltage is applied (down-state position). Ideal series switches have infinite isolation in the up-state position, and zero insertion loss in the down-state position. MEMS series switches are used extensively for 0.1-40 GHz applications. They offer high isolation at RF frequencies, around -50 dB to -60 dB at 1 GHz, and rising to -20 to -30 dB at 20 GHz. In the down-state position, they result in very low insertion loss, around -0.1 to -0.2 dB at 0.1-40 GHz.

The shunt switch is placed in shunt between the transmission line and ground, and depending on the applied bias voltage, it either leaves the transmission line undisturbed or connects it to ground. Therefore, the ideal shunt switch results in zero insertion loss when no bias is applied (up-state position) and infinite isolation when bias is applied (down-state position). Shunt capacitive switches are more suited for higher frequencies (5-100 GHz). A well designed shunt capacitive switch results in low insertion loss (-0.04 to -0.1 dB at 5-50 GHz) in the up-state position, and acceptable isolation (more than -20 dB at 10-50 GHz) in the down-state position.

This chapter details the electromagnetic modelling of MEMS shunt switches. It does not concentrate on one switch geometry, but tries to give an overview on how to model the capacitance, inductance and resistance of MEMS switches (CLR model), and how to extract the CLR model from S-parameter measurements or simulations.

2.2 Physical Description of MEMS Shunt Switches

A MEMS shunt capacitive switch is shown in Fig. 2.1. The switch geometry follows the same definitions as Chapter 6. The switch is suspended at a height g above the dielectric layer on the transmission line, and the dielectric thickness is t_d with a dielectric constant ϵ_r . The switch is L μm long, w μm wide, with a thickness of t μm . The width of the transmission line is W μm . The substrate can be silicon, GaAs, Alumina, LTCC, or a quartz dielectric.

The MEMS shunt switch can be integrated in a coplanar-waveguide (CPW) or in a microstrip topology. In a CPW configuration, the anchors of the MEMS switch are connected to the CPW ground planes. In a microstrip configuration, one anchor is connected to a quarter-wave open stub which results in a short circuit at the bridge. The second anchor of the bridge is either left unconnected, or is connected to the bias resistor.

A DC voltage is applied between the MEMS bridge and the microwave line. This results in an electrostatic force which causes the MEMS bridge to collapse on the dielectric layer, largely increasing the bridge capacitance by a factor of 30-100. This capacitance connects the transmission line to the ground and acts a short circuit at microwave frequencies, resulting in a reflective switch. When the bias voltage is removed, the MEMS switch returns back to its original position due to the restoring spring forces of the bridge. The mechanical modelling of MEMS bridges is detailed in Chapter 6.

Typical values of the switch geometry are a dielectric thickness of 1000-1500 Å, a relative dielectric constant of 5.0-7.6 depending on the nitride material used, a bridge height of 1.5-5 μm , a length around 250-400 μm , and a width between 25 and 180 μm depending on the switch capacitance required. The length is rarely shorter than 200 μm due to the sharp increase of the actuation voltage with decreasing bridge length. The width is limited to

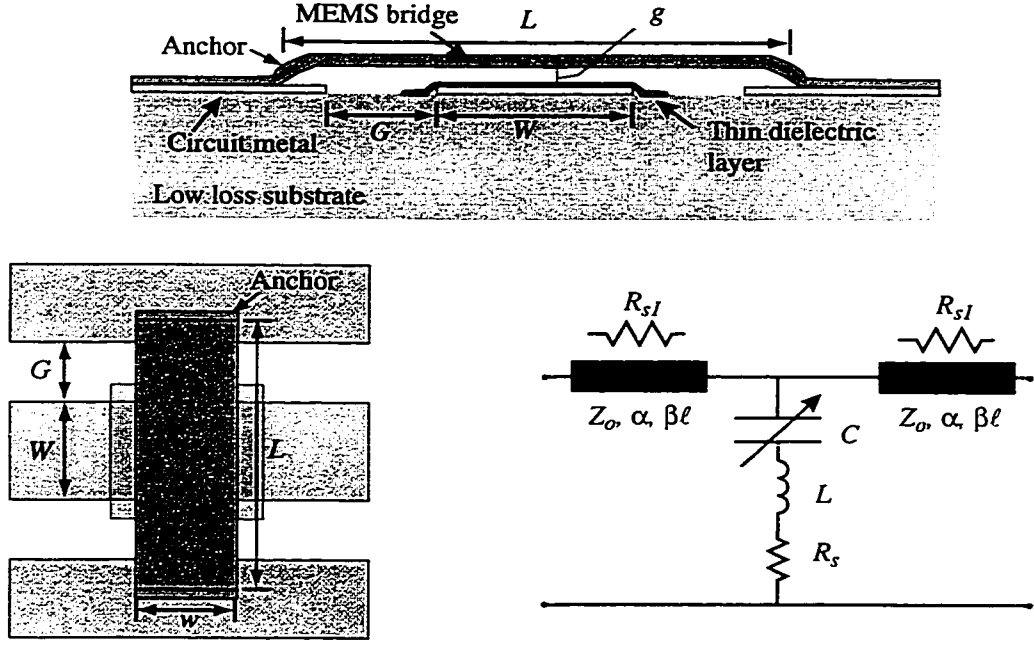


Figure 2.1: Illustration of a typical MEMS shunt switch shown in cross-section and plan-view. The equivalent circuit is also shown.

200 μm so as to result in a flat contact area between the MEMS bridge and the t-line.

2.3 Circuit Model of the MEMS Capacitive Shunt Switch

The MEMS shunt switch is modelled by two short sections of transmission line and a lumped CLR model of the bridge with the capacitance having an up-state and a down-state value. The t-line sections are of length $(w/2) + \ell$ where $\ell = 20 \mu\text{m}$ is the distance from the reference plane to the edge of the MEMS bridge. Typical values for mm-wave switches are a capacitance of 35 fF/2.8 pF, an inductance of 6-12 pH and a series resistance of 0.2-0.3 Ω . For X-band switches, the capacitance is 70 fF/5.6 pF with an inductance of 4-5 pH and a series resistance of 0.1-0.2 Ω (the modelling of the bridge CLR values will be presented in the next section).

The switch shunt impedance is given by:

$$Z_s = R_s + j\omega L + \frac{1}{j\omega C} \quad (2.1)$$

with $C = C_u$ or C_d depending on the position of the switch. The LC series-resonant frequency of the switch is:

$$f_o = \frac{1}{2\pi\sqrt{LC}} \quad (2.2)$$

and the impedance of the shunt switch can be approximated by:

$$Z_s = \begin{cases} \frac{1}{j\omega C} & \text{for } f \ll f_o, \\ R_s & \text{for } f = f_o, \\ j\omega L & \text{for } f \gg f_o. \end{cases} \quad (2.3)$$

The CLR model behaves as a capacitor below the LC series resonant frequency and as an inductor above this frequency. At resonance, the CLR model reduces to the series resistance of the MEMS bridge. For $C_u = 35$ fF, $C_d = 2.8$ pF, and $L = 7$ pH, the resonance occurs at $f_o = 322$ GHz and 36 GHz when the switch is in the up-state and down-state position, respectively. It is for this reason ($f_o = 322$ GHz) that the inductance of the bridge plays absolutely no role in the up-state position for $f < 100$ GHz. Therefore, in the up-state position, the MEMS bridge can be accurately modeled as a shunt capacitance to ground. As will be seen later, the inductance plays an important role in the down-state position.

The cutoff frequency is defined as the frequency where the ratio of the off (up-state) and on (down-state) impedance degrades to unity, and is:

$$f_c = \frac{1}{2\pi C_u R_s} \quad (2.4)$$

and $f_c = 30$ THz for a switch with $C_u = 35$ fF and $R_s = 0.15 \Omega$. This figure of merit has been extensively used with Schottky and PIN diodes, and approximately describes the performance of the device (loss, isolation, and upper frequency of operation). However, it is not strictly applicable to MEMS shunt switches. The reason is that the switch inductance limits the down-state performance at a much lower frequency than f_c . A better value to use for the upper frequency of operation is $2f_o$, since the MEMS shunt switch results in acceptable isolation up to twice the LC resonant frequency in the down-state position.

$w \times W [\mu\text{m}^2]$	$g [\mu\text{m}]$	$C_u [\text{fF}]$	$C_{pp} [\text{fF}]$	$C_f [\text{fF}]$	C_f/C_{pp}
40×100	4	13.8	8.8	5	57%
80×100	4	23.4	17.6	5.8	33%
110×100	4	38.6	30.8	7.8	25%
140×160	4	59.2	49.3	9.9	20%
40×100	1.5	29.8	23.2	6.5	28%
80×100	1.5	55.6	46.6	9	19%

Table 2.1: Simulated static capacitance of a MEMS bridge ($L = 300 \mu\text{m}$, $t = 2 \mu\text{m}$, $t_d = 1500 \text{ \AA}$, $\epsilon_r = 7.6$)

2.4 Electromagnetic Modeling of MEMS Shunt Switches

2.4.1 Off-State Capacitance

The parallel plate capacitance of the MEMS shunt switch is:

$$C_{pp} = \frac{\epsilon_o w W}{g + \frac{t_d}{\epsilon_r}} \quad (2.5)$$

The second term in the denominator is due to the finite thickness of the dielectric, and if neglected, the parallel plate capacitance is equal to the standard formula of $C = \epsilon_o A / (g + t_d)$, where $A = wW$. For a dielectric thickness of 1500 \AA , a relative dielectric constant of 7.6 (Si_xN_y) and a bridge height of $4 \mu\text{m}$, neglecting the second term results in an underestimation of the parallel plate capacitance by 3%, and for a height of $1.5 \mu\text{m}$, the error increases to 10%. However, if the capacitance is calculated as $C = \epsilon_o A / g$, then the error is 0.5% and 1.3% for a bridge height of $4 \mu\text{m}$ and $1.5 \mu\text{m}$, respectively, and results in a more accurate approximation.

The fringing field capacitance of MEMS switches is a substantial portion of the total capacitance as indicated in Table 1. The calculation is done by solving for the total capacitance using a 3-D electrostatic program called Maxwell 3D [2] and subtracting the parallel plate capacitance derived above. It is seen that the fringing capacitance is around 20% to 60% of the parallel plate capacitance depending on the bridge dimensions and height. Therefore, the fringing capacitance cannot be neglected in the analysis even for low bridge heights.

Some MEMS switches are fabricated with a set of closely spaced holes in the bridge

membrane. This is done to allow the removal of the sacrificial layer using dry etching (Plasma Etching) techniques, and to allow a faster operation of the switch by reducing the air damping underneath the bridge (see Chapter 6 for more detail). The holes are typically 4-6 μm in diameter spaced at a period of 5-6 μm in a triangular or hexagonal lattice. The height of the bridge is typically 3-4 μm . The capacitance of this structure is simulated using Maxwell 3D and results in the same capacitance as a bridge fabricated using a continuous sheet of metal. This is due to the fringing fields which completely cover the holes. The rule of thumb is that the hole diameter should be less than $3g$ so as not to affect the up-state parallel-plate capacitance.

The up-state capacitance can also be derived using electromagnetic software packages, such as IE3D, Sonnet or HFSS. The structure is numerically simulated including the thin dielectric layer, and if the dielectric layer is neglected, then the height of the bridge should be considered as g . The resulting S-parameters (mainly S_{11}) are fitted using a simple model consisting of capacitor in shunt with two sections of $50\ \Omega$ transmission lines (or any known impedance). The fitted capacitor values agree well with the electrostatic values obtained above (Table 1). In order to get an accurate value of the up-state capacitance, the input and output t-line impedances should be known to within $\pm 1\ \Omega$. Otherwise, the error resulting from the fitting of the S-parameters can have a large effect on the fitted value of the up-state capacitance (see Section 3.5.1).

2.4.2 Down-State Capacitance and Capacitance Ratio

The MEMS switch capacitance in the down-state position can be easily calculated using $C_d = \epsilon_0 \epsilon_r A / t_d$. In this case, the thickness of the dielectric is so small that the fringing capacitance can be neglected. The up-state/down-state capacitance ratio is:

$$\frac{C_d}{C_u} = \frac{\frac{\epsilon_0 \epsilon_r A}{t_d}}{\frac{\epsilon_0 A}{g + \frac{t_d}{\epsilon_r}} + C_f} \quad \text{with } C_f = 0.3 - 0.4 C_{pp} \quad (2.6)$$

For a capacitance area of $80 \times 100\ \mu\text{m}$, a dielectric thickness of 1000 (1500) \AA , $\epsilon_r = 7.6$, and a height of 1.5 μm and 4 μm , the capacitance ratio is 60 (38):1 and 120 (80):1, respectively.

It is tempting to make the dielectric layer as thin as possible to increase the capacitance ratio. However, it is impractical to deposit a Si_xN_y layer which is thinner than 1000 Å due to pin-hole problems in thin dielectric layers. Also, this dielectric layer must be able to withstand the actuation voltage (20-50 V) without dielectric breakdown. It is for this reason that this layer is typically 1000-1500 Å thick in all MEMS switches built today.

The down-state capacitance can be degraded if the MEMS bridge layer or dielectric layer are not perfectly flat. This can be due to the deposition parameters of the nitride or the fabrication process of the MEMS bridge. The down-state capacitance is:

$$C_d = \frac{\epsilon_o A}{2} \left(\frac{1}{d_1 + \frac{d_2}{\epsilon_r}} + \frac{\epsilon_r}{d_2} \right) \quad (2.7)$$

where, A is the capacitive area of the bridge, d_1 is the amplitude of the roughness, d_2 is the dielectric thickness, and ϵ_r is the relative dielectric constant of the dielectric layer. Figure 2.2 shows the reduction in the down-state capacitance assuming a perfectly flat dielectric layer, and a roughness 0-500 Å in the MEMS bridge. The contact area is assumed to be 50% of the total bridge area. The dielectric layer is 1000-1500 Å thick with $\epsilon_r = 7.6$. It is seen that a capacitance degradation of 30-35% occurs for a roughness of 100 Å (10 nm). If the roughness is large and results in a contact area of only 20%, then the down-state capacitance will be around 20% of the parallel-plate value for a roughness of 200 Å.

Several researchers have proposed the use of high dielectric-constant ceramics such as Strontium-Titanate-Oxide (STO) or Barrium-Strontium-Titanate (BST) with ϵ_r between 40 and 200. This results in theoretical capacitance ratios of 400-3000 for 1000-1500 Å thick dielectrics, and allows the fabrication of very small MEMS capacitive shunt switches with high isolation at 2-10 GHz. Fig. 2.2b presents the capacitance degradation for a roughness 0-100 Å and a 50% contact area. It is seen that the down-state capacitance is highly dependent on the roughness of the material used, and a roughness of 40 Å results in a degradation of 50% in the total capacitance. If the surface is very rough and results in a contact area of only 15%, then the down-state capacitance will be 15% of the parallel-plate value for a roughness of 40 Å. This may still be acceptable since the down-state capacitance is very high.

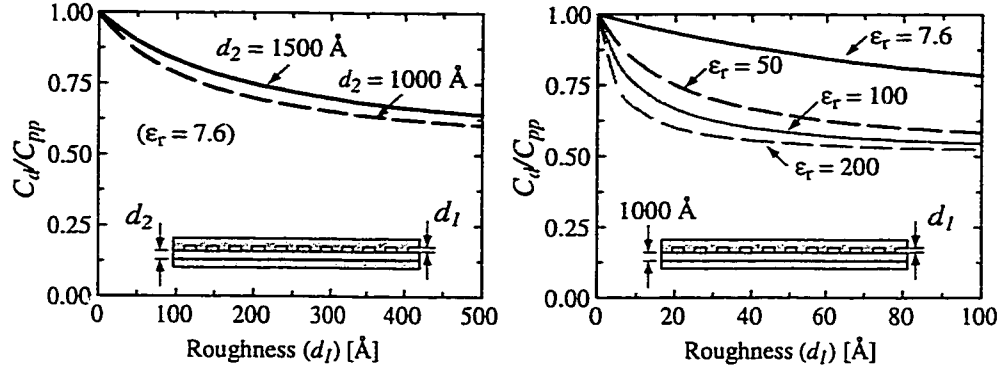


Figure 2.2: Simulated down-state capacitance degradation versus roughness in the overlying bridge layer for low (a) and high (b) dielectric constant materials.

2.4.3 Current Distribution

The current distribution at 30 GHz of a MEMS bridge in the up-state position, with a width of 80 μm , and suspended 3 μm above the t-line is shown in Fig. 2.3a. The up-state capacitance of the MEMS switch is around 32 fF. The switch is placed in a CPW configuration, but the results are the same for a microstrip design. The normalized current distribution is obtained using IE3D [3] or Sonnet [4]. It is seen that there is no RF current on the bridge portion which is above the center of the line. This is expected since the RF current is carried at the edge of the t-line at microwave frequencies. Also, notice that the current is concentrated on the edge of the bridge over the CPW gap. If the bridge width is changed to 40 μm , the current distribution remains unchanged, always hugging the edges of the MEMS bridge.

The same analysis was done for a microstrip line implementation. The results (not shown) indicate that there is no current on the bridge above the center of the microstrip line, and that the current starts from the edge of the microstrip line to the anchor of the bridge which is connected to the $\lambda/4$ open-stub.

The current distribution in the down-state position with $w = 80$ μm and $C_d = 0.5$ pF is shown in Fig. 2.3b. It is seen that the current is concentrated on *one edge* of the MEMS bridge since this edge presents a short circuit to the incoming wave. From Fig. 2.3a and

Fig. 2.3b, it is expected that the up-state inductance and resistance of the MEMS switch are different from the down-state values. However, as discussed before, only the down-state inductance is of importance since it affects the operation of the switch at mm-wave frequencies.

2.4.4 Series Resistance

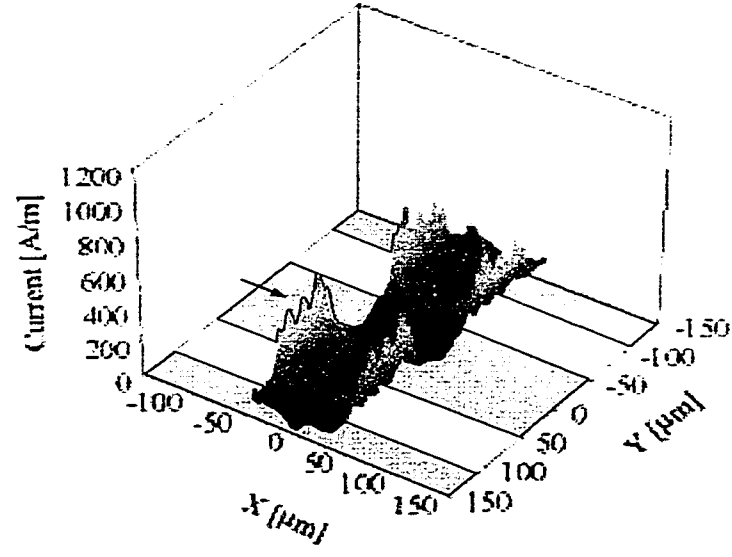
There are two components to the series resistance of the MEMS switch. The first component, R_{s1} , is due to the transmission-line loss and can be calculated using:

$$\alpha = \frac{R_{s1}/\ell}{2Z_o} \quad (2.8)$$

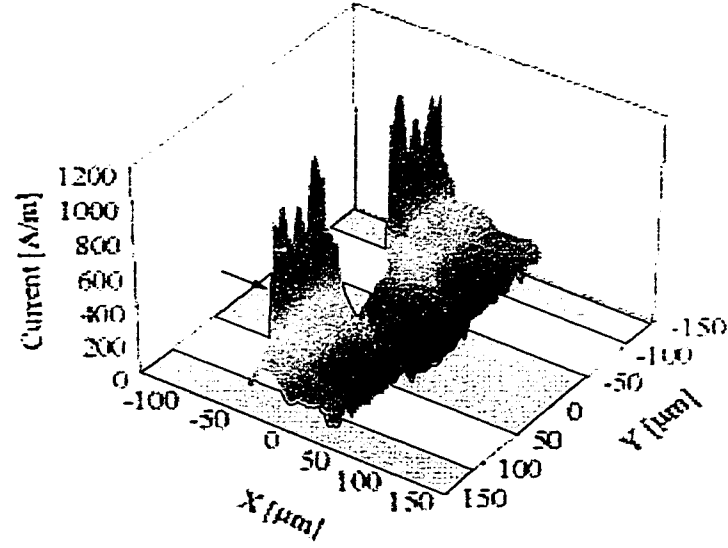
where α is the line loss (both ohmic and dielectric) in Np/m (1 Np = 8.69 dB). The second component is R_s , which is due to the MEMS bridge only and is calculated below (see Fig. 2.1).

The measured attenuation of the CPW or microstrip line can be used to derive R_{s1} . For the switch in the up-state position and $S_{11} \leq -10$ dB, we assume that the current on the t-line is un-affected by the bridge. For a 50 Ω CPW line with $G/W/G = 60/100/60$ μm on high-resistivity silicon with an 8000 Å-thick Au center conductor and 2 μm -thick Au ground planes, the measured attenuation is $\alpha = 1.7$ dB/cm (0.20 Np/cm) at 30 GHz, and varies approximately as \sqrt{f} with frequency. A switch length (the distance between the reference planes) of 160 μm results in a line loss of 0.027 dB (0.0031 Np) and $R_{s1} = 0.32$ Ω . For a 100 Ω CPW line with 8000 Å-thick Au metalization and $G/W/G = 100/100/100$ μm on quartz, the measured attenuation is $\alpha = 0.4$ dB/cm (0.046 Np/cm) at 30 GHz, and results in a line loss of -0.005 dB (0.0006 Np) and an equivalent R_{s1} of 0.06 Ω . Microstrip lines have considerably less loss than CPW lines, and result in R_{s1} of 0.05-0.1 Ω on silicon substrates at 10-40 GHz (for Au or Al), and 0.02-0.05 Ω on quartz substrates.

There is one caveat that is worth mentioning. Some fabrication procedures require the use of a thin Titanium or Tungsten layers or other refractory metals underneath the MEMS bridge so as to obtain a very smooth electrode and dielectric layer. The resistivity of these metals is around 5-10 \times higher than that of Au or Al, and therefore, the associated R_{s1} will be around 1-2 Ω , depending on the dimensions of this t-line section. This results in -0.1 to



(a)



(b)

Figure 2.3: Simulated current distribution on the MEMS bridge in (a) the up-state and (b) the down-state for an $80\text{ }\mu\text{m}$ wide MEMS bridge over a $60/100/60\text{ }\mu\text{m}$ CPW line. A 1 W wave is incident from the left and travels in the $+x$ -direction.

−0.2 dB of loss in the refractory metal section alone, and dominates the loss of the MEMS switch.

The resistance of the MEMS bridge, R_s , is much harder to calculate due to the different current distributions in the up-state and down-state positions (Fig. 2.3b). Simple equivalent models based on simulated current distributions and the assumption of uniform current penetration to a skin depth in the metal can be derived and applied the calculation of the bridge resistance, R_s . However, as shown in Section 2.5, the bridge resistance in the down-state position can be accurately extracted from the measured S-parameters.

The skin depth is $\delta = 1/\sqrt{f\pi\mu\sigma}$ and for a Au (and Al) bridge, the skin depth is $0.73\ \mu\text{m}$ ($0.84\ \mu\text{m}$) at 10 GHz and $0.42\ \mu\text{m}$ ($0.48\ \mu\text{m}$) at 30 GHz. If the bridge thickness is smaller than two skin depths, the switch resistance is constant with frequency. For thick Au MEMS bridges ($t > 1.5\ \mu\text{m}$), the switch resistance changes with frequency as \sqrt{f} above 30 GHz due to the skin depth effect, and is constant at lower frequencies. For thin Au or Al bridges ($0.5\text{--}1\ \mu\text{m}$), the bridge resistance is constant up to 60 GHz.

2.4.5 Inductance

A simple and accurate way to model the switch inductance in the down-state position is to assume that the capacitance of the switch is large enough so that it is a short circuit above the center conductor. The bridge is then modeled using numerical electromagnetic techniques (IE3D [3], Sonnet [4], HFSS [5]). This results in an efficient computation since the dielectric layer is completely ignored. The modeled S-parameters from 1–60 GHz are fitted to an RL model, and the series resistance and inductance are extracted. Again, it is important that the input and output t-lines be exactly $50\ \Omega$ (or of known impedance) so as to result in an accurate fitted model. The numerical software does not result in accurate values for the series resistance, but results in excellent modelling of the bridge inductance.

The switch inductance and capacitance can also be *uniquely* determined to within $\pm 3\%$ from a fit to the measured 2–40 GHz S-parameters (see Section 2.5.2 for details). Table 2.2 shows the simulated inductance and a comparison with fitted values obtained from down-state measurements (Fig. 2.4). Notice that for a bridge width from $20\ \mu\text{m}$ to $140\ \mu\text{m}$, the

w [μm]	Sonnet [pH]	HFSS [pH]	Measured [pH]
20	17.8	15.8	15
30	14.5	13.5	12.5
50	10.7	10.5	9.5
80	7.1	8	7
110	5.3	5.8	5.1
140	3.9	4.4	–

Table 2.2: MEMS bridge inductance for several bridges with various widths ($L = 300 \mu\text{m}$, $t = 2 \mu\text{m}$). The CPW line dimensions are $G/W/G = 60/100/60 \mu\text{m}$ on high-resistivity silicon.

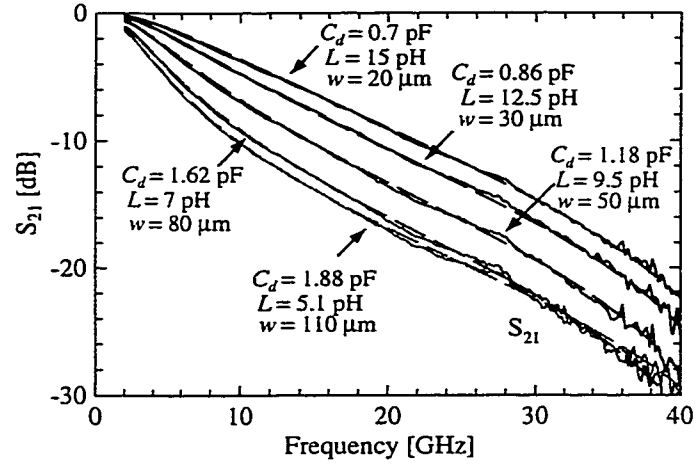


Figure 2.4: Measured and fitted down-state S-parameters for MEMS switches of various widths.

w [μm]	30/100/30	60/100/60
30	7.7	14.5
80	3.5	7.1
140	1.9	3.9

Table 2.3: Simulated MEMS bridge inductance [pH] using Sonnet for CPW line dimensions on high-resistivity silicon of $G/W/G = 30/100/30$ μm ($L = 200$ μm , $t = 2$ μm) and $G/W/G = 60/100/60$ μm ($L = 300$ μm , $t = 2$ μm).

inductance changes by a factor of 3 and not 7, indicating that the RF current in the down-state position is concentrated on the first edge of the bridge, and is weakly dependent on the width of the bridge. Simulations using Sonnet indicate that the bridge inductance remains constant (to within ± 0.5 pH) for $t = 0.5\text{-}4$ μm .

The bridge inductance is mainly determined by the portion of the bridge over the CPW gaps and is not dependent on the portion of the bridge over the center conductor. This is due to the current distribution on the CPW line (or microstrip line) which is concentrated on the edges of the conductors. Table 2.3 presents the simulated inductance of a MEMS switch fabricated in a $G/W/G = 30/100/30$ μm CPW line on a high-resistivity silicon substrate. In this case, the input and output CPW line impedance is $43\ \Omega$. Notice that the bridge inductance is approximately half that of Table 2.2 due to the reduction in the CPW gap dimensions.

An experiment was done to further prove that the bridge inductance is determined by the CPW gap width. In this case, the width of the portion of the bridge over the gaps of the CPW line ($G/W/G = 60/100/60$ μm) is held constant at 40 μm , and the width of the bridge over the center conductor of the CPW is varied. The measured S-parameters were again fit to a *CLR* model (Fig. 2.5). The fitted capacitance varied from 1 pF to 1.78 pF as w increases, but the switch inductance was constant at 11 pH for the three cases.

The inductance for low spring-constant bridges has also been modeled using numerical techniques (Sonnet). It is seen that the inductance is nearly the same (8.4 pH versus 7.7 pH) since the RF current is carried at the edge of the MEMS bridge (Fig. 2.6). However, a very low spring-constant design with a thin meander support to the bridge anchor results in a large bridge inductance, and could affect the operation of the switch above 10 GHz.

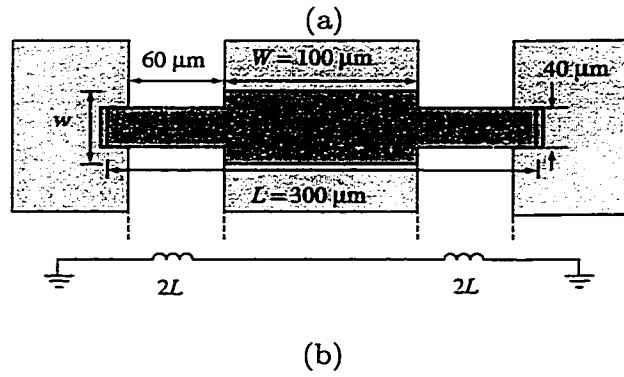
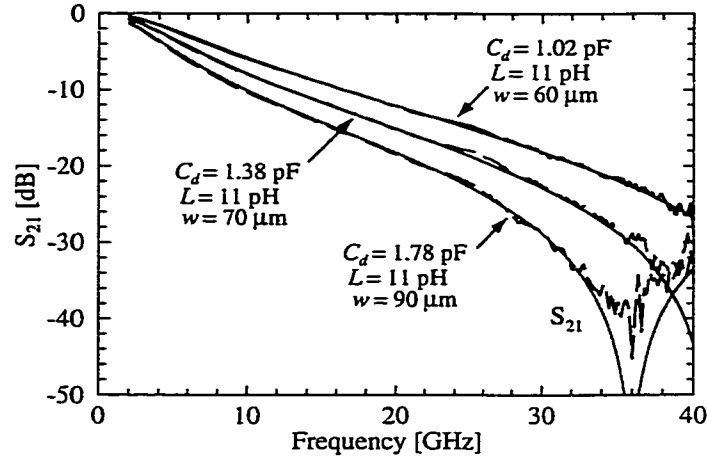


Figure 2.5: Down-state measured and fitted S-parameters for MEMS switches where the width of the section over the center conductor is varied and the portion over the CPW gap is held constant (a). The schematic and equivalent circuit for the inductance is shown in (b).

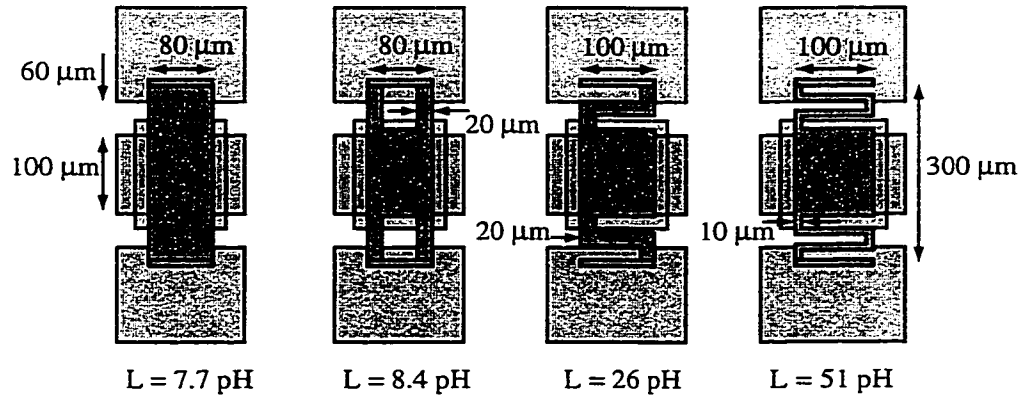


Figure 2.6: Simulated inductance for low spring-constant MEMS bridges.

Finally, the inductance of a MEMS shunt switch in a microstrip implementation is very similar to the value obtained using a CPW configuration. If the MEMS switch is connected to ground using a via-hole, then the total inductance in series with the bridge capacitance is $L + L_{via}$. Typical via-hole inductances are around 50-150 pH and could significantly affect the down-state performance at mm-wave frequencies (see Chapter 3 for more details).

2.4.6 Loss

The loss of a MEMS shunt switch is sometimes taken to be $|S_{21}|^2$. The decrease in S_{21} does not necessarily indicate power loss in the switch, but can simply be due to an increase in the reflected power from the switch ($|S_{11}|^2$). The loss of a MEMS switch is better derived from the S-parameters as:

$$Loss = 1 - |S_{11}|^2 - |S_{21}|^2 \quad (2.9)$$

and this can be easily calculated using a microwave circuit simulator (HP-Libra [6]) or using measured values. The loss in dB is given by: $Loss(dB) = 10 \log(1 - Loss)$, and is a negative number. However, in many cases, it is quoted as a positive number. The MEMS shunt switch loss is composed of two parts: 1) the t-line loss underneath the bridge and to the reference planes ($e^{-\alpha \ell}$), and 2) the MEMS bridge loss.

The power loss in the MEMS bridge is $P_{loss} = I_s^2 R_s$, where I_s is the current in the bridge. The MEMS bridge loss is:

$$Loss = \frac{\text{Power loss in MEMS bridge}}{\text{Power incident on the MEMS switch}} = \frac{I_s^2 R_s}{|V^+|^2 / Z_o} \quad (2.10)$$

$$Loss = \left| \frac{2Z_s || Z_o}{Z_s || Z_o + Z_o} \right|^2 \frac{1}{|Z_s|^2} R_s Z_o \quad (2.11)$$

where Z_s is given in Eq. 2.1. In the up-state position and for $S_{11} \leq -13$ dB, we have $Z_s \gg Z_o$ and the MEMS bridge loss becomes:

$$Loss = \omega^2 C_u^2 R_s Z_o \quad (2.12)$$

In the down-state position and for $S_{21} \ll -10$ dB, we have $Z_s \ll Z_o$ and the MEMS bridge loss is:

$$Loss = \frac{4R_s}{Z_o} \quad (2.13)$$

For small loss values, and in the up-state position, the total loss is:

$$Loss = e^{-\alpha\ell} + \omega^2 C_u^2 R_s Z_o \quad (2.14)$$

where ℓ is the distance between the reference planes which are defined at $20 \mu\text{m}$ from the edge of the MEMS bridge ($\ell = w + 2 \times 20 \mu\text{m}$). In the down-state position, the loss can be approximated by:

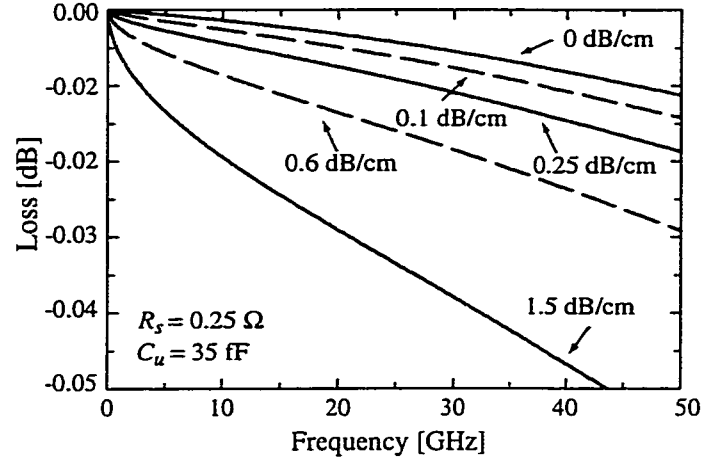
$$Loss = e^{-\alpha\ell/2} + \frac{4R_s}{Z_o} \quad (2.15)$$

since the current is reflected on the first edge of the MEMS bridge. The loss of a MEMS switch with $C_u = 35 \text{ fF}$, $C_d = 2.8 \text{ pF}$, $L = 7 \text{ pH}$, and $R_s = 0.25 \Omega$ (constant with frequency) is shown in Fig. 2.7. The loss is plotted for an $80 \mu\text{m}$ -wide bridge. The line loss is assumed to be $0.1\text{-}1.5 \text{ dB/cm}$ and varying as \sqrt{f} with frequency, which is typical of Au and Al microstrip and CPW t-lines on quartz and silicon substrates. It seen that the switch loss is dominated by the t-line loss in the up-state position. Therefore, the measured loss of a MEMS switch is directly dependent on the width of the bridge and the definition of the reference planes. In the up-state position, it is very hard to measure a switch loss of $0.01\text{-}0.06 \text{ dB}$ at $1\text{-}40 \text{ GHz}$. One way of obtaining an accurate loss value is to measure $6\text{-}10$ closely spaced switches and divide the insertion loss by the number of switches.

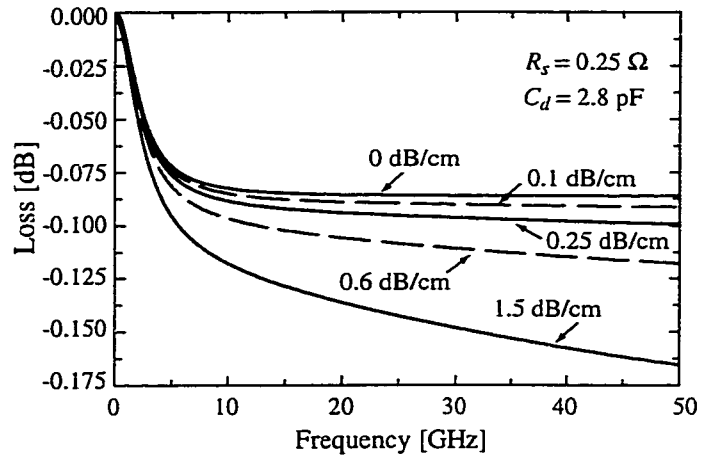
The loss in the down-state position is needed if a reflection-type phase shifter or modulator is used, and is $0.05\text{-}0.15 \text{ dB}$ for $S_{21} \leq -10 \text{ dB}$ and $R_s = 0.25 \Omega$. The effect of the line loss is dominated by the switch resistance, and is around 0.1 dB at all frequencies of interest.

2.5 Fitting CLR Parameters to S-Parameter Shunt-Switch Measurements

The CLR values can be extracted accurately from S-parameter measurements. In this case, the MEMS switch is fabricated and measured from $1\text{-}40 \text{ GHz}$ using on-wafer calibration techniques. The TRL calibration technique can be used to define the reference planes to be $20 \mu\text{m}$ from the MEMS bridge.



(a)



(b)

Figure 2.7: Up-state (a) and down-state (b) simulated loss for various values of R_s and α . The reference planes are $20 \mu\text{m}$ from the edge of the MEMS switch ($w = 80 \mu\text{m}$).

2.5.1 Up-State Capacitance

The S-parameters are first measured in the up-state position and the measured data (S_{11}) is fitted to get the up-state capacitance of the switch. The inductance and resistance are not fitted using this measurement since their effect is negligible in this case.

In the up-state position, the reflection coefficient is (neglecting LR_s):

$$S_{11} = \frac{-j\omega C_u Z_o}{2 + j\omega C_u Z_o} \quad (2.16)$$

and for $S_{11} \leq -10$ dB or $\omega C_u Z_o \ll 2$:

$$|S_{11}|^2 \simeq \frac{\omega^2 C_u^2 Z_o^2}{4} \quad (2.17)$$

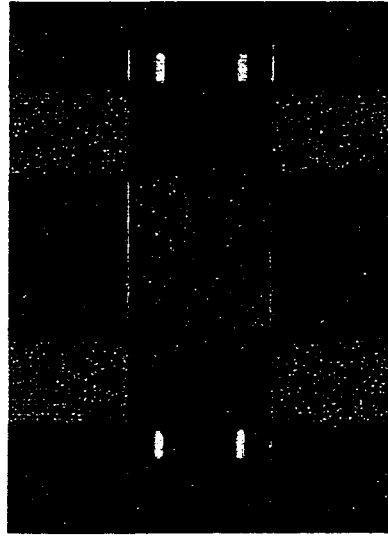
The above equations result in a straightforward determination of the up-state capacitance of the MEMS shunt switch from the measured data. Fig. 2.8 shows the measured and fitted up-state reflection coefficient of a MEMS switch with $w = 80 \mu\text{m}$, $W = 100 \mu\text{m}$, and $g = 1.5 \mu\text{m}$ [7]. It is seen that the up-state capacitance (70 fF) agrees well with the electrostatic value derived above (68 fF).

2.5.2 Down-State Capacitance and Inductance

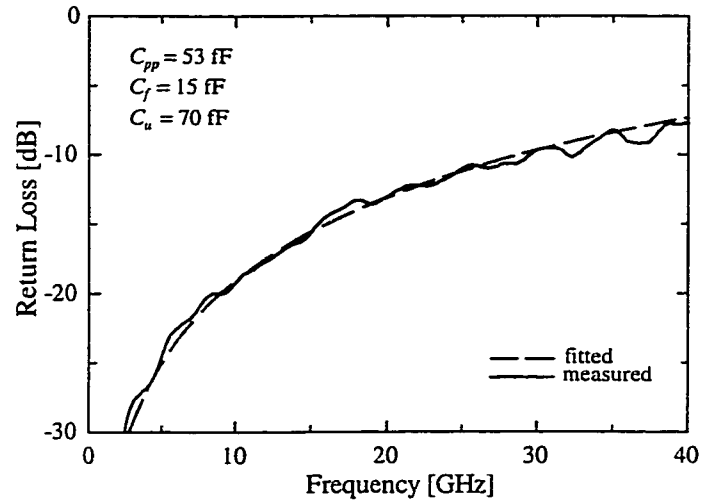
The S-parameters are measured with the switch in the down-state position, and a CLR model is fitted to the measured data (S_{21}) using Libra. Figure 2.9 shows a typical switch in the down-state position and the fitted CL values [7]. The isolation in the down state is given by:

$$|S_{21}|^2 \simeq \begin{cases} \frac{4}{\omega^2 C_d^2 Z_o^2} & \text{for } f \ll f_o \\ \frac{4R_s^2}{Z_o^2} & \text{for } f = f_o \\ \frac{4\omega^2 L^2}{Z_o^2} & \text{for } f \gg f_o \end{cases} \quad (2.18)$$

Notice that the capacitance solely controls the response up to $\sim f_o/2$ (1-20 GHz in this case). Once the capacitance is determined, the inductance value controls the resonant frequency location. Even if the resonant frequency of the MEMS switch is beyond the measurement bandwidth, the inductance has a strong effect on the slope of S_{21} after $f_o/3$ and this can be used to fit an accurate model of the switch inductance.

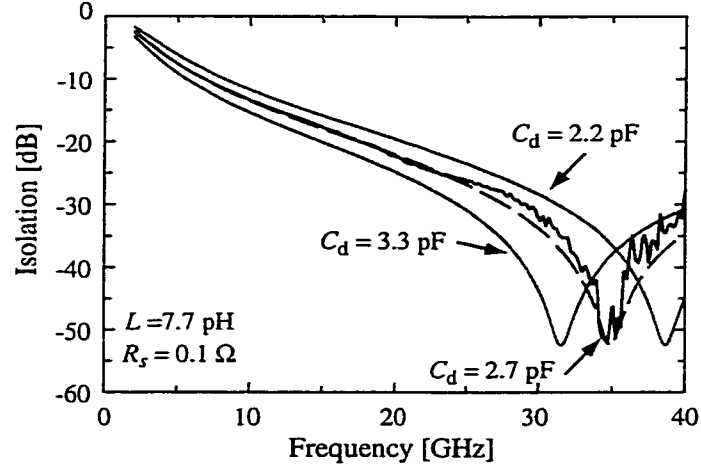


(a)

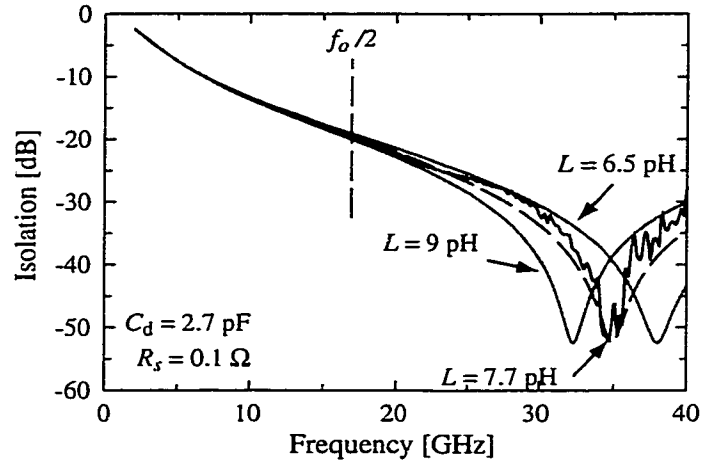


(b)

Figure 2.8: Photomicrograph (a) of a MEMS shunt switch and (b) the up-state measured and fitted return loss for an $80 \mu\text{m}$ wide bridge with a nominal gap height of $1.5 \mu\text{m}$. The CPW center conductor is $100 \mu\text{m}$ wide.



(a)



(b)

Figure 2.9: Down-state measured and fitted isolation for a MEMS shunt switch, showing the accuracy of the *CLR* fit over 1-40 GHz. ($L = 300 \mu\text{m}$, $w = 80 \mu\text{m}$, $W = 100 \mu\text{m}$, $t_d = 1500 \text{ \AA}$.)

The switch inductance and capacitance are *uniquely* determined to within $\pm 3\%$ from a fit of the equivalent circuit to the measured 2-40 GHz S-parameters. As indicated above, the down-state capacitance is dependent on the surface roughness and cannot be easily modelled. The inductance agrees quite well with full-wave modelling.

It should be noted that the fitting works well for a shunt switch in a CPW configuration, where the switch is directly connected to the CPW ground plane. If the switch is connected to a microstrip $\lambda/4$ open stub, the isolation response is significantly altered by the frequency response of the stub (see Chapter 3), and therefore, the measured isolation cannot be used to determine the down-state capacitance and inductance of the switch. If the microstrip MEMS switch is connected to the ground plane using via-holes, then the fitted inductance is the series combination of the MEMS bridge and the via-hole inductance.

There are some CPW switch implementations which result in a very low bridge inductance. In this case, the insertion loss in the down-state position is solely determined by the down-state capacitance and is:

$$S_{21} = \frac{1}{1 + j\omega C_d Z_o / 2} \quad (2.19)$$

and for $S_{21} \ll -10$ dB and $\omega C_d Z_o \gg 2$:

$$|S_{21}|^2 \simeq \frac{4}{\omega^2 C_d^2 Z_o^2} \quad (2.20)$$

The measured isolation can then be used to determine the down-state capacitance as long as the measurement is taken far away from the LC resonant frequency. For example, for $C_d = 3$ pF and $L = 1-2$ pH, the resonant frequency is 65-90 GHz, and Eq. (2.20) is valid up to 20-30 GHz.

2.5.3 Series Resistance of the MEMS bridge

The series resistance in the down-state of the MEMS bridge is best fitted around the LC resonant frequency. In this case, the switch impedance is $Z_s = R_s$ and S_{21} is:

$$S_{21}|_{\omega_o} = \frac{2R_s||Z_o}{R_s||Z_o + Z_o} \simeq \frac{2R_s}{Z_o} \quad (2.21)$$

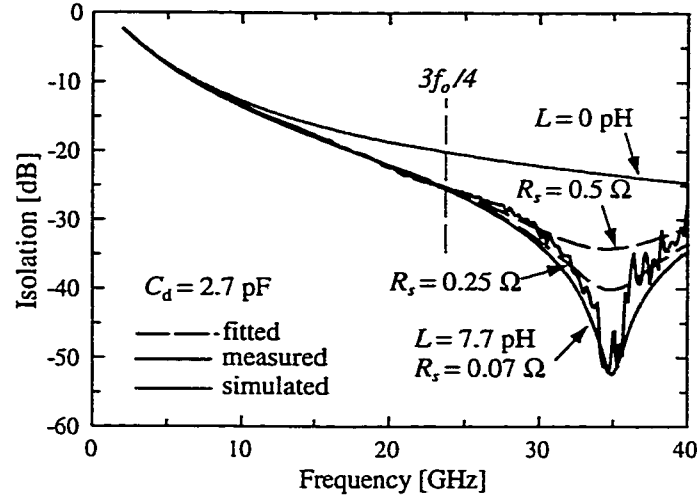


Figure 2.10: Down-state measured and fitted isolation for a MEMS shunt switch, showing the effect of the inductance and resistance (R_s) on the fit. ($L = 300 \mu\text{m}$, $w = 80 \mu\text{m}$, $W = 100 \mu\text{m}$, $t_d = 1500 \text{ \AA}$.)

Fig. 2.10 shows the fitted S-parameter for a Au switch fabricated at the University of Michigan with $C_d = 2.7 \text{ pF}$, $L = 7.7 \text{ pH}$ and $R_s = 0.07 \Omega$ [7]. The response for $R_s = 0.07 \Omega$, 0.25Ω and 0.5Ω are included for comparison. It is seen that as the series resistance gets smaller, the resonance in S_{21} gets sharper and deeper (-48 , -40 , -34 dB , respectively). In fact, an excellent calibration to -50 dB is needed to be able to measure a series resistance of 0.1Ω . Also, the series resistance has virtually no effect at $f < 3f_o/4$, so it is important to measure the S-parameters of the switch around the down-state resonant frequency. The bridge resistance in the up-state position can be found by measuring 6-10 switches in series and using Eq. (2.8) and (2.12).

Fig. 2.10 also shows the simulated S-parameters for $L = 0 \text{ pH}$. It is clear from that the inductance and resistance cannot be ignored in the down-state position. The LC resonant frequency for most shunt switch designs is 20-100 GHz, depending on the dimensions of the switch. Therefore, the isolation in the down-state position can be dramatically increased (20^+ dB) by designing for the required LC_d resonant frequency.

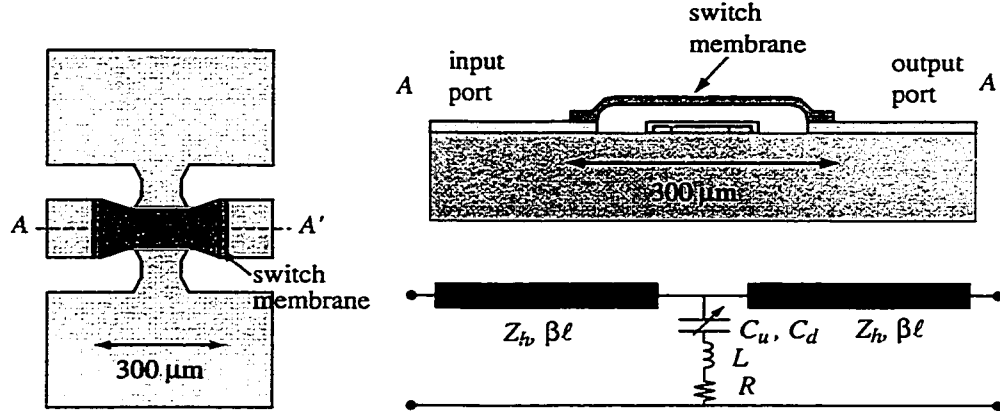


Figure 2.11: Illustration of a MEMS inline shunt capacitive switch.

2.6 Inline MEMS Capacitive Shunt Switches

An implementation of an inline MEMS capacitive shunt switch is shown in Fig. 2.11. In this case, the MEMS bridge is fabricated as part of the microwave t-line, and the shunt connection to the CPW ground, or to a microstrip $\lambda/4$ stub, are directly patterned on the wafer. The mechanical operation of the inline MEMS shunt switch is identical to the standard design, and the actuation voltage is applied between the center conductor of the t-line and the ground plane. The electromagnetic and circuit modelling presented above (up and down-state capacitance, inductance, loss, and parameter fitting) also apply to this novel switch, with the exception that the parameters of the sections of t-line before and after the shunt capacitance are that of the switch membrane. These sections of t-line typically have an impedance of 60-70 Ω and therefore tend to cancel some of the up-state capacitance of the MEMS switch. The main advantage of the inline MEMS switch is that the mechanical design is independent of the shunt inductance (defined by the metal connecting the capacitive section to the ground plane), and it is possible to build very low inductance (2-5 pH) switches for mm-wave operation. Alternatively, high-inductance switches can also be built for X-band operation while still maintaining a large spring constant design.

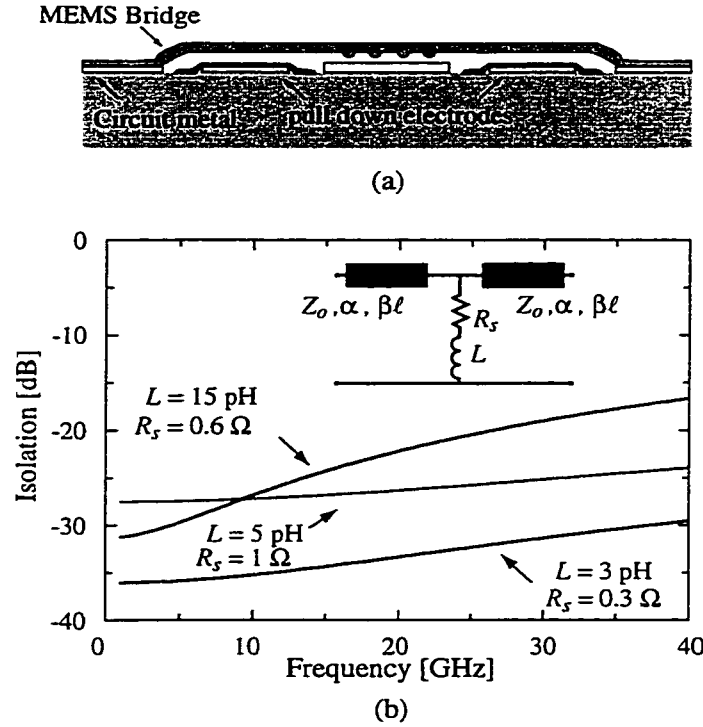


Figure 2.12: A DC-contact MEMS shunt switch with two pulldown electrodes, and the simulated isolation in the down-state position.

2.7 DC-Contact MEMS Shunt Switches

DC-contact shunt switches are similar to MEMS capacitive shunt switches except that a separate electrode is used to pull the membrane (bridge) to the down-state position (Fig. 2.12). Therefore, it is possible to result in a metal-to-metal contact between the t-line and the ground plane without affecting the electrostatic forces on the switch.

The modelling of a DC-contact shunt switch in the up-state position is identical to the capacitive shunt switch, except that the nitride layer is removed underneath the bridge. The up-state capacitance, inductance, and loss can be modeled as described in Section 2.4 above. In the down-state position, a DC-contact switch results in an $R_s L$ circuit-model in shunt with the t-line, where R_s is the sum of the contact resistance and the bridge resistance, and is around 0.5-2 Ω for most designs (see Section 4.2 on MEMS series switches). The isolation is given by:

$$S_{21} = \frac{2(R_s + j\omega L) \parallel Z_o}{(R_s + j\omega L) \parallel Z_o + Z_o} \simeq \frac{2(R_s + j\omega L)}{Z_o + R_s + j\omega L} \quad (2.22)$$

$$|S_{21}|^2 \simeq \begin{cases} \left(\frac{2R_s}{Z_o}\right)^2 & \text{for } \omega L \ll R_s, \\ \left(\frac{2\sqrt{2}R_s}{Z_o}\right)^2 & \text{for } \omega L = R_s, \\ \left(\frac{2\omega L}{Z_o}\right)^2 & \text{for } \omega L \gg R_s. \end{cases} \quad (2.23)$$

Notice that the isolation is dominated by the switch inductance for $f \geq R_s/(2\pi L)$. For a switch with $R_s = 1 \Omega$ and $L = 5$ pH, $S_{21} = -28$ dB at 0.01-20 GHz and decreases gradually to -25 dB at 40 GHz. The isolation is dependent on the switch inductance of mm-wave frequencies, and is only -16 dB at 40 GHz for $L = 15$ pH (Fig. 2.12). This means that DC-contact shunt switches should not be used above 20 GHz with via-holes if high isolation is desired.

The extraction of the CLR parameters of the DC-contact shunt switch follows the same approach as the capacitive shunt switch. The up-state capacitance can be determined from S_{11} in the up-state position and Eq. (2.17). The contact resistance and switch inductance can be determined from S_{21} in the down-state position using Eq. (2.23). It is hard to determine the switch inductance if it is less than 5 pH, since it has a minimal effect on the measured isolation. However, it can be accurately simulated using numerical techniques.

CHAPTER 3

MEMS SHUNT SWITCHES AND HIGH-ISOLATION SWITCH CIRCUITS

3.1 Introduction

In the previous chapter, we concentrated on the electromagnetic and circuit modeling of MEMS switches. In the case of shunt switches, the model consists of a CLR circuit with an inductance of 2-30 pH depending on the design of the MEMS bridge. The associated resistance is around 0.1-0.25 Ω . The up-state capacitance is 20-100 fF and the down-state capacitance is 0.5-50 pF depending on the area and height of the bridge, the thickness and type of the dielectric layer used, and the smoothness of the dielectric and bridge surfaces. The associated on/off-state capacitance ratio is between 40 and 500. The inductance plays an important role in the response of MEMS CPW capacitive shunt switches and can actually increase the isolation by 20 dB at mm-wave frequencies.

This chapter covers the design of microwave and mm-wave shunt switches, and also their use in resonant circuits for high-isolation designs. One can also design absorptive switches, and single-pole multiple throw switches, all with very low loss. Effectively, the low parasitics associated with the MEMS technology result in easy-to-design MEMS switch circuits. It is expected that MEMS switch circuits will quickly find their way into low-loss phase shifters, switched oscillator and filter banks (single-pole and multiple-throw designs), satellite switching networks (absorptive switches, etc..), and wideband high-isolation instrumentation switches (network analyzers, automatic testers, etc..).

3.2 Biasing of MEMS Switches

The biasing of MEMS DC-contact series switches is achieved using 1-100 k Ω resistors attached to the pull-down electrode. A high-resistance line is used since it offers excellent isolation from the microwave circuit. Also, a very small amount of current (sub μ A level) is needed for the switching process (Fig. 3.1a), and the high-resistance lines do not result in a voltage drop in the bias circuit. The microwave t-line is kept at DC-ground and no DC-blocking capacitors are needed between the MEMS switches.

A similar biasing arrangement is used for MEMS capacitive switches in a microstrip circuit. In this case, the bias circuit is attached to the MEMS bridge anchor while the microstrip line is DC grounded (Fig. 3.1b). In a CPW implementation, the bias voltage can be applied to the center conductor using a bias-T, or using a resistive tap to the center conductor (Fig. 3.1c). For several MEMS switches which must be actuated independently, one must use DC-block capacitors the different MEMS switches and different resistive taps to the center conductor. The resistive lines are typically covered with a thick nitride layer so as to isolate them from the CPW ground metal layer.

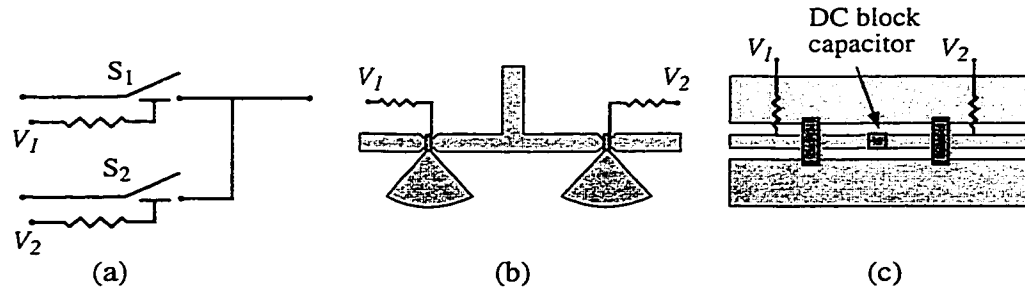


Figure 3.1: Bias arrangement for (a) series switches, (b) microstrip capacitive switches, and (c) CPW capacitive switches.

In contrast, the biasing circuit for a PIN diode is quite complicated. The diode requires +2 V and -6 V. The negative voltage is needed for depleting the intrinsic-layer to result in a very low capacitance. Also, the diode consumes 1-20 mA of current depending on its size, and therefore, the bias circuit must be an LC network or its equivalent $\lambda/4$ t-line implementation. A complete bias circuit is shown in Fig. 3.2a, and it is evident that the

PIN diode occupies a substantial amount of space on the microwave circuit. Also, it is hard to integrate several diodes close to each other (for example, a SP4T switch) since each diode requires a lot of passive components around it.

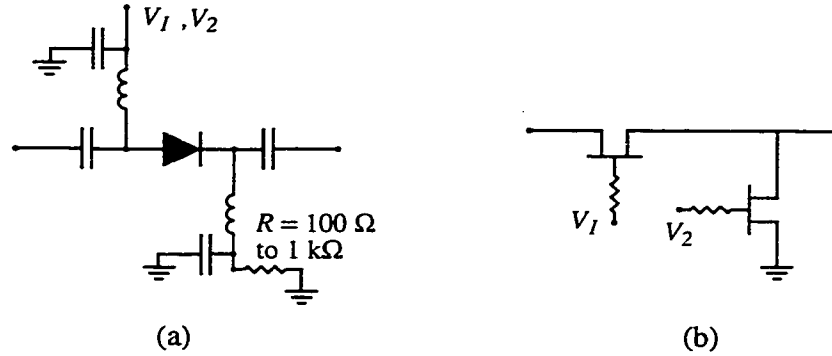


Figure 3.2: Bias arrangement for (a) PIN diode, and (b) a transistor switch.

The biasing of transistor switches is also quite easy (Fig. 3.2b). The transistor requires 1-3 V on its gate, and this can be done using a 10-100 k Ω resistors (again, the gate does not consume any current). However, transistor switches suffer from a relatively high insertion loss above 6 GHz, and a low intermodulation product level. Transistor switches are used in non-critical switching applications, and provide an excellent cost-to-performance ratio.

3.3 Design of CPW MEMS Shunt Capacitive Switches

3.3.1 C-band to X-Band Designs

Consider a MEMS shunt switch with capacitance C_u and C_d connected in shunt across a t-line of impedance Z_o . In the up-state position, the reflection coefficient is:

$$S_{11} = \frac{-j\omega C_u Z_o}{2 + j\omega C_u Z_o} \quad (3.1)$$

and for $S_{11} < -10 \text{ dB}$ and $\omega C_u Z_o \ll 2$:

$$|S_{11}|^2 \simeq \frac{\omega^2 C_u^2 Z_o^2}{4} \quad (3.2)$$

and Figure 3.3 presents the up-state reflection coefficient for bridge capacitances. The loss in the up-state position is dependant on the definition of the reference planes and is less

than -0.1 dB up to 50 GHz (see Chapter ?? for details.) In the down-state position, the CLR model results in a resonant frequency given by $f_o = 1/2\pi\sqrt{LC_d}$. However, for resonant frequencies above 25 GHz, and for X-band operation, the inductance and series resistance of the CLR model can be neglected and the insertion loss (isolation) is:

$$S_{21} = \frac{1}{1 + j\omega C_d Z_o/2} \quad (3.3)$$

and for $S_{21} < -10$ dB and $\omega C_d Z_o \gg 2$:

$$|S_{21}|^2 \simeq \frac{4}{\omega^2 C_d^2 Z_o^2}. \quad (3.4)$$

The insertion loss can also be written as:

$$|S_{21}|^2 = \frac{1}{S_{11}^2} \left(\frac{C_u}{C_d} \right)^2 \quad (3.5)$$

Eq. (3.5) determines the isolation obtained knowing the capacitance ratio and the allowable up-state reflection coefficient, and is plotted in Fig. 3.4. It is universal for capacitive shunt switches with no inductance effects, and is independent of the technology used and number of switches employed.

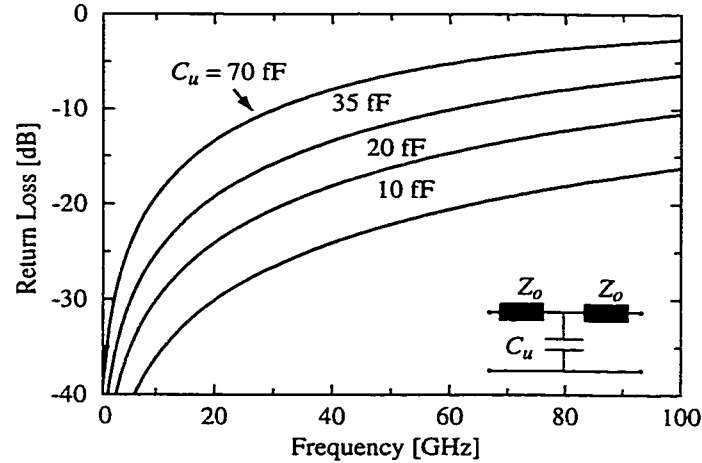


Figure 3.3: Calculated reflection coefficient for different up-state bridge capacitances.

A typical down-state capacitance using MEMS bridges is 6-8 pF for a 1000 Å nitride layer, and results in an isolation of around -20 dB at 10 GHz. This capacitance is limited

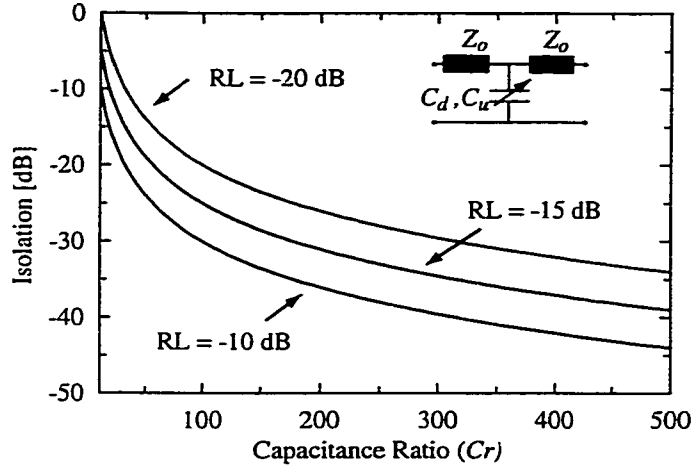


Figure 3.4: Calculated isolation versus allowable off-state reflection coefficient and capacitive ratio for a CPW shunt MEMS switch.

by the area of the MEMS bridge (around $160 \times 180 \mu\text{m}$) and the contact planarity between the dielectric and the MEMS bridge. If more isolation is desired using shunt capacitive switches, then it is possible to put two or three MEMS bridges close to each other (see Section 3.4.4). In this case, the isolation is improved by 6 dB for the two bridge designs, and 9.5 dB with the third bridge ($3 \times$ capacitance). The penalty paid is the increase in the up-state reflection coefficient. Section 3.5 presents T and π -switch circuits which results in excellent isolation while still maintaining a good match. The insertion loss for the two and three-bridge circuits is minimal for $R_s = 0.1\text{-}0.25 \Omega$.

Another solution is the use of very high dielectric constant materials for the dielectric layer. In this case, a down-state capacitance of 30-60 pF can be achieved, resulting in -32 to -38 dB of isolation at 5 GHz using Eq. (3.4). The LC resonant frequencies of these switches is around 6-12 GHz ($C_d = 30\text{-}60$ pF, $L = 6\text{-}12$ pH) which makes them ideal for 2-20 GHz operation.

3.3.2 X-Band Switch Examples

Two basic X-band shunt capacitive switches were developed at the University of Michigan. The first switch, shown in Fig. 3.5 has a standard configuration with the membrane

fixed at the two ground planes and spanning the center conductor of the CPW line. The second type of switch is the inline capacitive switch where the membrane spans a gap in the CPW center conductor.

Standard Configuration

The standard shunt capacitive MEMS switch is shown in Fig. 3.5. The single MEMS switch is fabricated on a CPW line with dimensions of $G/W/G = 60/100/60 \mu\text{m}$ (50Ω) for DC-40 GHz measurements on a high-resistivity silicon substrate ($3000 \Omega\text{cm}$). The switch length, is $300 \mu\text{m}$ and the anchors are $40 \mu\text{m}$ from the CPW ground plane edge. Various membrane widths are used in this work, from $20 \mu\text{m}$ to $140 \mu\text{m}$ so as to achieve different switch capacitance and inductance values. The membrane height is $g_o = 1.5\text{-}2 \mu\text{m}$, and the membrane thickness, t , is $1\text{-}2 \mu\text{m}$. This switch configuration is covered in detail in Chapter 2.

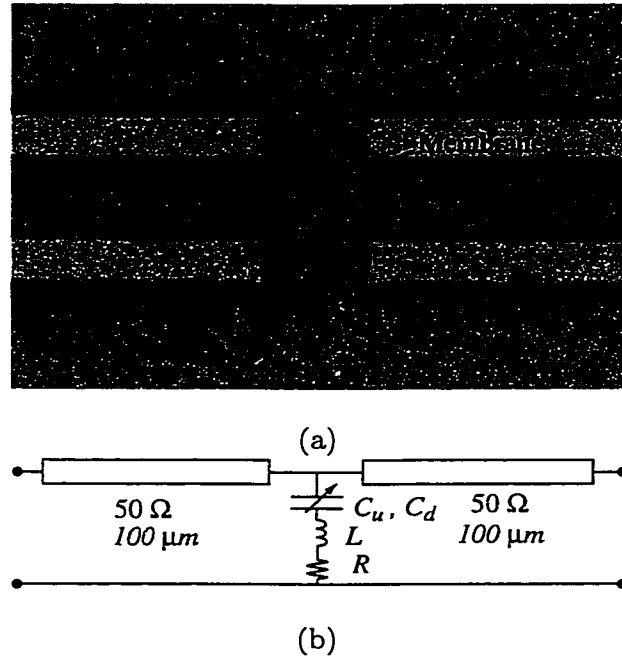


Figure 3.5: Photomicrograph of a X/K-band standard shunt capacitive switch (a) and equivalent model (b).

Fabrication: The MEMS switch was implemented on 400 μm thick high-resistivity silicon substrate ($\epsilon_r = 11.9$) covered with 4000 Å SiO_2 using finite-ground CPW [8]. The CPW lines are defined using a liftoff process by evaporating a 300/8000 Å layer of Ti/Au. Next, a 1000-2000 Å PECVD Si_3N_4 layer is deposited and patterned. Then, a 1.5-2 μm thick sacrificial layer of photoresist is deposited and patterned. The thickness of this layer determines the nominal gap height g_o of the membrane. A 300/1000/1000 Å Cr/Au/Ti seed layer is evaporated, and then patterned to remove the top Ti layer so that the membranes and the circuit metal, excluding the area underneath and near the membrane, can be electroplated with Au at the same time. The Au is electroplated in a 55° cyanide based solution with a current density of 2-4 mA/cm². The electroplating thickness is approximately 2-2.5 μm . The sacrificial layers are removed using Ti, Cr, and Au etchants to remove the seed layers and Acetone to remove the resist layer. To avoid collapsing the membrane during drying, the structure can be released using a (CPD) critical point drying system [9], which uses the critical point of CO_2 to avoid the collapsing surface tension forces of etch release liquids. See Appendix A for further details on the fabrication process.

The Au membrane switches have a low compressive residual stress under the process parameters described above. However, the compressive stress only slightly decreases the pulldown voltage of the switch since the mechanical stress due to the spring constant is much larger than the residual stress. A material with a slightly tensile residual stress is preferred. The choice of Au as the membrane material was determined by process availability. Typical pulldown voltages for these switches are 12-25 V, depending on the plating rate, membrane thickness, resist profile, and vertical stress gradients.

Inline Configuration

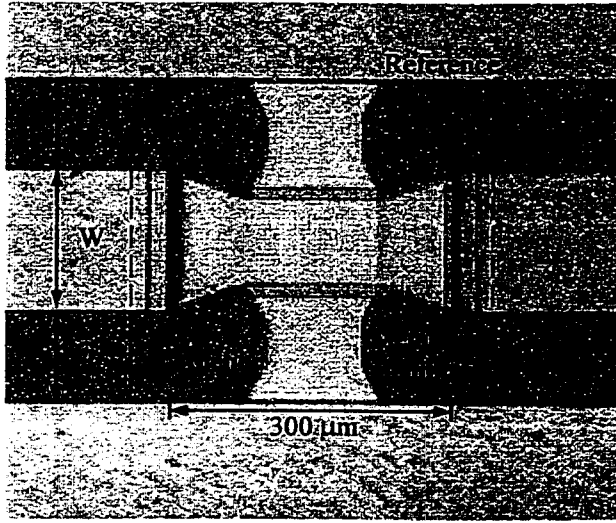
The inline capacitive switch is shown in Fig. 3.6. The MEMS bridge is defined in the CPW center conductor, and is suspended over a 4000 Å-thick layer which connect together the two grounds of the CPW line. The idea of an inline air-bridge has been demonstrated before using standard air-bridge technology and is applied here for MEMS switches. A nitride layer is defined over the central portion of the bridge, and forms the capacitive contact between the center conductor and the ground plane once the bridge is pulled down.

The advantages of this approach is that it isolates the mechanical characteristics of the MEMS bridge from the electrical connection to the ground. In other words, one can now use a narrow high-inductance or a wide low-inductance connection to the ground plane (in a microstrip or CPW implementation) without changing the mechanical spring constant of the MEMS bridge.

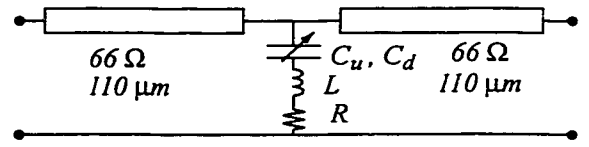
Another advantage of the inline switch in the up-state are the short high-impedance transmission line section due to the height of the bridge. This occurs at the left and right sides of the central bridge portion and help tune out the up-state capacitance. In both the X/K-band and the Ka/V-band switches, the equivalent transmission line impedance is 66Ω with a length of 100-120 μm . The model shown in Fig. 3.8b is used to accurately fit the up-state return loss of the switch.

Fabrication: The MEMS bridge is fabricated using the standard techniques described before [7]. First, a 4000 Å gold layer is defined which includes the CPW line and ground-to-ground connection. Next, a 2000 Å-thick nitride layer is deposited using a PECVD process at 250°C. A 1.5 μm -thick photoresist layer is used as the sacrificial layer, and the MEMS air bridge is fabricated using a Ti/Au sputter deposition with a total thickness of 9000 Å. The CPW line and MEMS bridge anchors are electroplated to a total thickness of 2.5 μm , and the MEMS bridge is released using a critical point drying process. The length of the MEMS bridge is 300 μm and the width depends on the required capacitance. The MEMS switch is biased using an external bias-T circuit between the CPW center conductor and ground. The pull-down voltage was 18 ± 2 V, and the applied voltage was set at 25 V. The extracted spring constant is 40 ± 10 N/m using a nominal gap height of 1.5 μm .

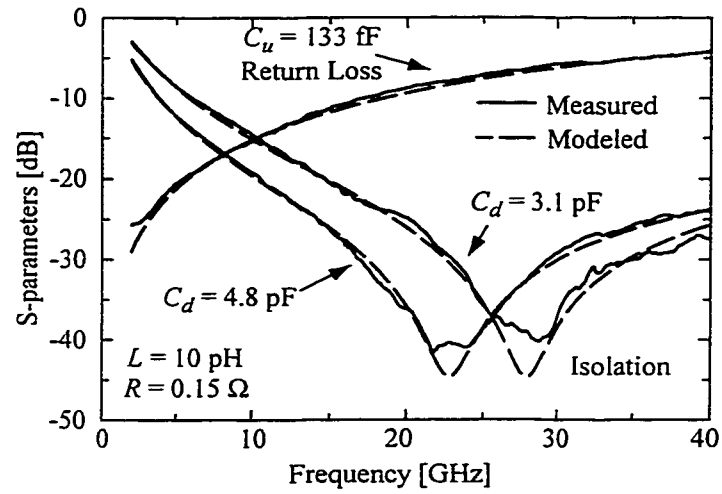
Measurements: The measured S-parameters for an inline X/K-band capacitive switch with a capacitive contact area of $140 \times 100 \mu\text{m}$ -square are shown in Fig. 3.6. The 50Ω CPW line dimensions are $G/W/G = 96/160/96 \mu\text{m}$ on a silicon substrate. The measured line loss is 0.25 dB/cm at 2 GHz and increases to 1.25 dB/cm at 40 GHz. The measured up-state capacitance is 133 fF and agrees well with the electrostatic simulations which predict a parallel-plate capacitance of $C_{pp} = 93$ fF and a fringing capacitance of $C_f = 31$ fF. The measured loss in the up-state position follow the $1 - |S_{11}|^2$ response. Isolation measurements are shown with the bridge fabricated in the down-state position, and with the bridge pulled



(a)



(b)



(c)

Figure 3.6: Photomicrograph of a X/K-band inline shunt capacitive switch (a), equivalent model (b), and measured S-parameters of a X/K-band inline shunt capacitive MEMS switch with a pulled-down switch ($C_d = 3.1$ pF) and a fabricated-down switch ($C_d = 4.8$ pF).

down using 25 V. The isolation measurements fit well a CLR model with $L = 10$ pH and $R = 0.15 \Omega$. The maximum parallel-plate capacitance is 4.8 pF ($C_{max} = \epsilon_r A/d$), and the achievable pulled-down capacitance is 3.1 pF ($0.65C_{max}$). The difference is due to the roughness of the dielectric/bridge layer, and due to slight curling in the bridge preventing a complete conformal contact when the bridge is pulled down. The capacitance ratio is 24 due to the low height of the MEMS bridge. However, as shown in [10], this switch can be used in a tuned T or π -circuit to result in excellent isolation at 10 GHz and above.

3.3.3 Millimeter-Wave Shunt Switches

The MEMS shunt switch with a length of 250-350 μm is ideal for mm-wave operation. The up-state performance of the MEMS switch is given by Eq. (3.2), and $C_u = 30$ -50 fF results in an S_{11} of -13 to -17 dB at 30 GHz. However, in the down-state position, the inductance of the bridge plays an important role since the LC resonant frequency of the MEMS switch is between 25 and 60 GHz. Therefore, Eq. (3.4) does not apply at 20-60 GHz. At the resonant frequency, the isolation is limited by the series resistance of the switch and was derived in Chapter 2:

$$|S_{21}|^2 = \left(\frac{2R_s}{Z_o} \right)^2 \quad (3.6)$$

The isolation is between -34 dB and -40 dB for a series resistance of 0.5-0.25 Ω . The isolation is independent of the down-state capacitance value as long as the resonant frequency is around 25-60 GHz. The loss of the switch in the up-state position is minimal and is typically limited by the definition of the reference planes (see Chapter 2 for more detail).

The response of a typical 35 GHz MEMS switch with $C_u = 35$ fF, $C_d = 2.8$ pF, $L = 8$ pH and $R_s = 0.25 \Omega$ is shown in Fig. 3.7. In this case, the down-state LC resonance is at 34 GHz. The insertion loss at 32-38 GHz is -40 dB and is limited by the bridge series resistance. The up-state capacitance of $C_u = 35$ fF can be achieved with a 4 μm high bridge with an area of $120 \times 120 \mu\text{m}$. The bandwidth of operation in a CPW implementation is limited by $S_{11} = -12$ to -10 dB at 50-60 GHz.

It is also easy to design a low reflection switch at 60 GHz by decreasing the up-state capacitance to 20 fF ($S_{11} \leq -15$ dB at 60 GHz). This can be achieved with an area of

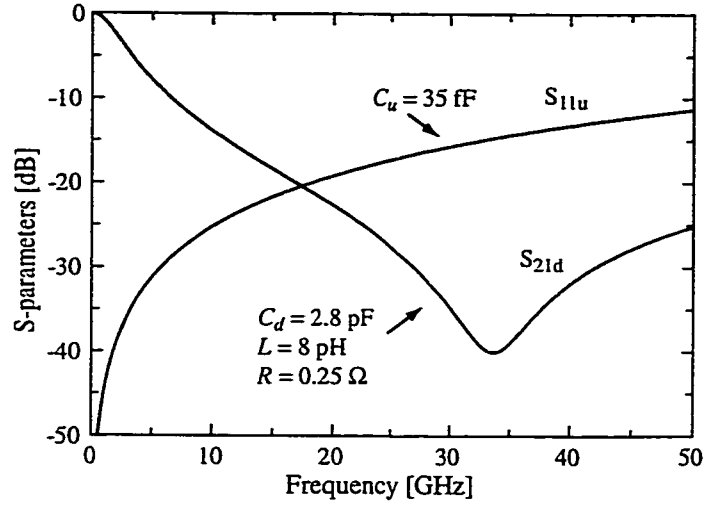


Figure 3.7: Simulated S-parameters for a Ka-band CPW MEMS shunt switch.

$60 \times 90 \mu\text{m}$ for a height of $4 \mu\text{m}$, and an associated inductance of around 10 pH . For a capacitance ratio of 60, the down-state capacitance is 1.2 pF and the resonant frequency is 46 GHz . This switch results in excellent performance up to 70 GHz .

Ka/V-Band Inline Switch Configuration

Again, both standard and inline mm-wave shunt capacitive switches were developed at the University of Michigan. The standard design is shown in Fig. 2.8, and the measured S-parameters for a Ka-Band *inline* mm-wave switch are shown in Fig. 3.8. The 50Ω CPW-line dimensions are $G/W/G = 60/100/60 \mu\text{m}$ (Fig. 3.8). There is a 6000 \AA -thick oxide layer in the CPW gaps, and the measured loss is 0.5 dB/cm at 2 GHz and increases to 1.5 dB/cm at 40 GHz . The capacitive contact area is $140 \times 60 \mu\text{m}$ -square and results in a measured up-state capacitance of 67 fF . This agrees with a height of $1.7 \mu\text{m}$ ($C_{pp} = 48 \text{ fF}$, $C_f = 18 \text{ fF}$). The measured down-state performance shows a maximum capacitance of 2.8 pF and a pulled-down capacitance of 2.2 pF ($0.79C_{max}$). This means that the MEMS bridge is being pulled down conformally and the reduction in the capacitance is solely due to the roughness of the dielectric. The inductance is reduced to 7.7 pH (as compared to 10 pH for the X/K-band switch). due to the smaller CPW gap (see [7]). The capacitance ratio is 33, and the Ka/V-band inline switch can be used at 15 GHz to 60 GHz using a T

or π -match circuit.

The pull-down voltage was 21 ± 3 V, and the applied voltage was set at 40 V. The extracted spring constant is 24 ± 8 N/m. The estimated mechanical resonant frequency is 54 kHz assuming the modal mass is dominated by the central 200 μm portion. The calculated mechanical quality factor (Q) is 0.24, due to the absence of holes, and yields estimated switching times of 9-20 μs for $V_s = 2V_p - 1.5V_p$.

3.3.4 W-Band Shunt Switches

If operation at 70-100 GHz is desired, then the switch off-state capacitance should be decreased to $C_u = 15$ fF for a reflection coefficient of -13 dB at 90 GHz. In a CPW configuration on silicon using a G/W/G of 25/45/25 μm and for a height of 3 μm , the up-state capacitance can be achieved using a 70 μm wide bridge. The bridge inductance is around 6-8 pH due to the small CPW gap (see Chapter 2). The estimated series resistance is 0.25-0.5 Ω at 80-100 GHz for a 1 μm -thick Au bridge. The up-state insertion loss is less than -0.1 to -0.15 dB for most designs. For a capacitance ratio of 80 and an down-state capacitance of 1.2 pF, the resonant frequency is 50 GHz, and the switch isolation is -25 dB at 90 GHz. However, if one chooses a capacitance ratio of 30 and a down-state capacitance of 0.45 pF, then the resonant frequency is pushed to 83-95 GHz and this results in excellent performance at 90 GHz (Fig. 3.9).

The low capacitance ratio can be achieved using a thicker dielectric or a lower dielectric constant material. The moral of the story is that, at W-band frequencies, a high down-state capacitance is not the crucial factor in determining the isolation of the shunt switch, and careful attention should be paid to the LC resonant frequency of the CPW shunt switch.

3.3.5 Novel Metal-to-Metal Contact Inline Shunt Switch

The inline shunt switch can be made to operate at low RF frequencies (DC-10 GHz) using a metal-to-metal contact (Fig. 3.10). The isolation of DC-contact switches is presented in detail in Chapter 2. In this design, two metal layers are defined underneath the bridge. The first layer is the pull-down electrode, and is fabricated using a 3000 Å-thick layer of

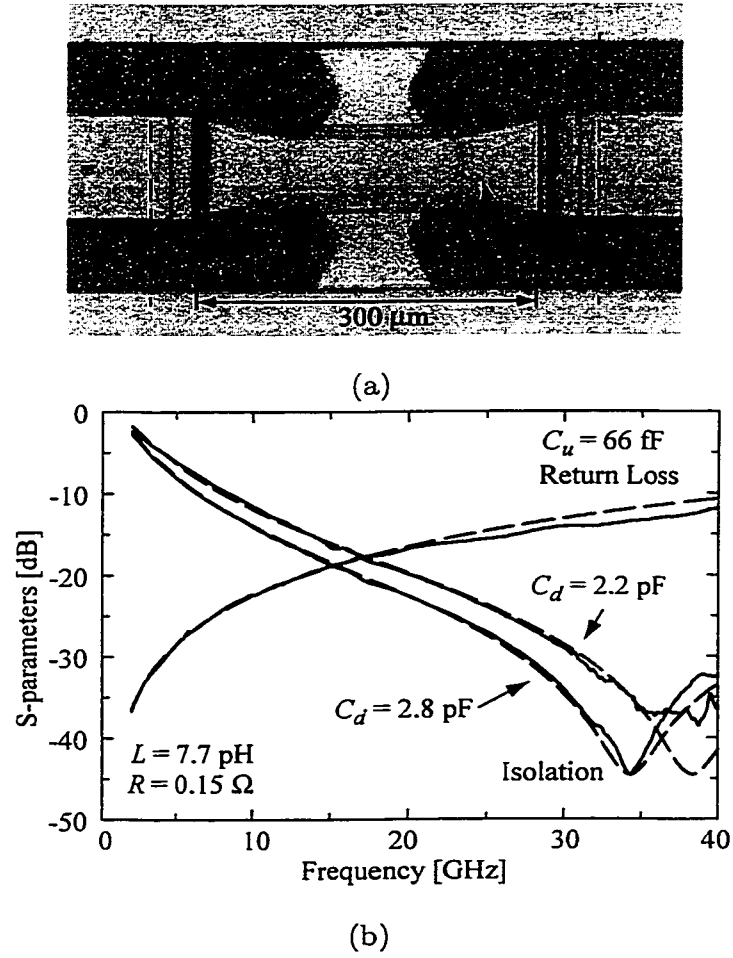


Figure 3.8: Photomicrograph of a Ka/V-band inline shunt capacitive switch (a). Measured (solid) and fitted (dashed) S-parameters of a Ka/V-band inline shunt capacitive MEMS switch (b).

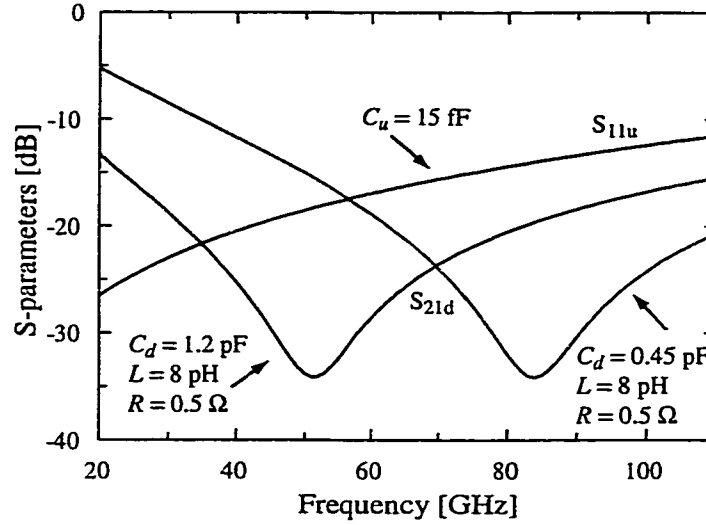
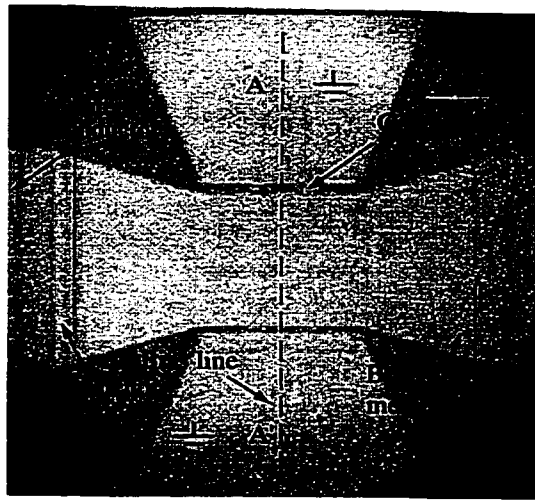


Figure 3.9: Simulated S-parameters for a W-band CPW MEMS shunt switch with $C_d = 1.2$ pF and $C_d = 450$ fF.

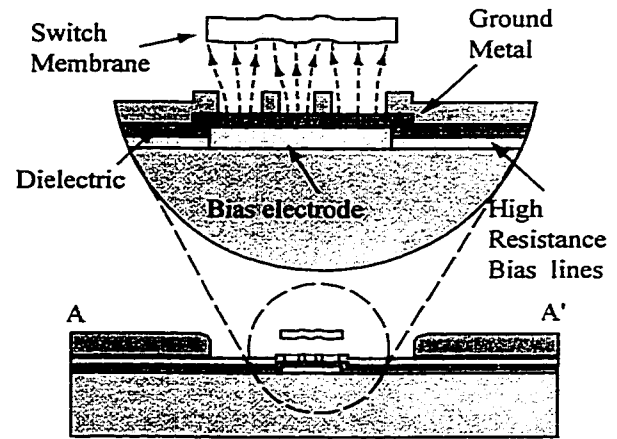
gold. The pull-down electrode is connected using high-resistivity bias lines to the edge of the ground plane. A 2000 Å-thick nitride layer is used to isolate the bias lines from the CPW ground plane. The nitride layer is also deposited over the pull-down electrode. A 4000 Å-thick Au layer with is deposited on top of the nitride and is connected to the CPW ground using the “bow-tie”-shaped (low inductance) gold pattern. The top metal layer forms the metal-to-metal contact with the MEMS bridge, and connects the MEMS bridge to the ground. The MEMS bridge is fabricated as described above using a sacrificial 1.5 μm -thick layer.

The top metal layer has a 10 μm hatch pattern underneath the center of the bridge with openings of 30 μm -square. The openings are essential to allow the static fields from the pull-down electrode to exert a force on the MEMS bridge. This novel electrode design allows for the placement of the pull-down electrode at the center of the bridge, thereby resulting in maximum bridge deflection for a specific applied voltage. The voltage is applied at the bias electrode and the CPW center conductor is connected to the DC ground.

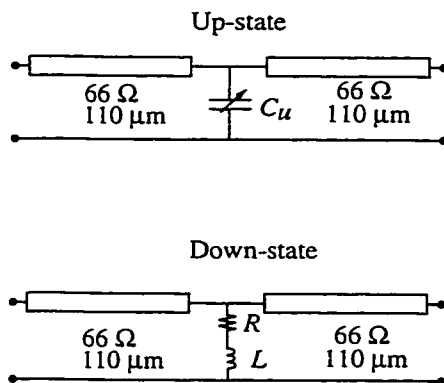
The inline switch is fabricated in a G/W/G=96/160/96 μm CPW line with a center electrode dimensions of 140 \times 100 μm -square. The pull-down voltage is 35 V and the applied



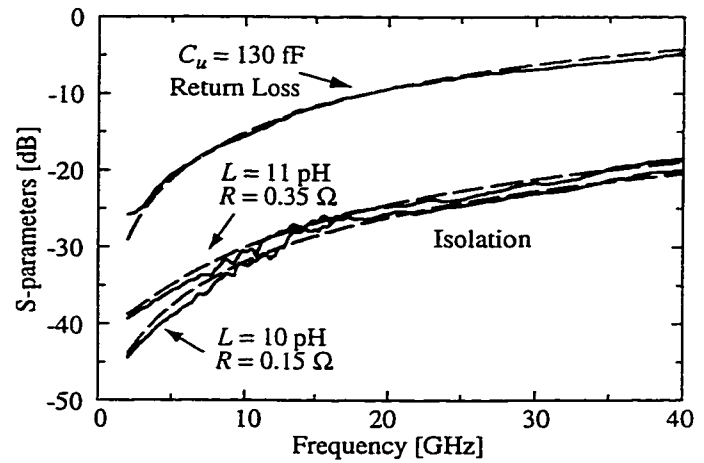
(a)



(b)



(c)



(d)

Figure 3.10: Photomicrograph of a DC contact inline shunt MEMS switch (a) and an illustration of the DC-contact inline shunt MEMS switch (b). Equivalent circuit in the up-state and down-state (c) and measured (solid) and fitted (dashed) S-parameters of an inline shunt DC MEMS switch (d).

voltage is 50 V due to the reduced pull-down area (a result of the metal hatch pattern). The measured up-state capacitance is 130 fF and is the same as the capacitive inline switch described above. The measured contact resistance is very low, around 0.15-0.35 Ω , because the electrostatic force is applied at the same location as the metal-to-metal contact area. This may be one of the advantages of this novel design. The switch results in an isolation of -40 dB at 0.1-3 GHz. The measured isolation is limited by the inductance to ground and is better than -20 dB at 40 GHz. The isolation at 40 GHz can be improved by 6 dB if a CPW gap of 40-50 μm is used, thereby resulting in an inductance of 5-6 pH.

The metal-to-metal inline switch can be further improved by choosing different metals with higher contact reliability (AuBe, AuTi, Pt, ErPt, ..) and by fabricating bumps in the MEMS bridge to contact at specific points with a higher pressure per contact. In our case, the contact resistance of Au/TiAu was repeatable over two months in laboratory experiments with the wafer dried at 80°C for 20 minutes and then flushed with nitrogen before testing. No lifetime tests were done for this switch, however, the reliability of such a switch design is very important to successful commercialization.

3.4 Inductively-Resonant High-Isolation X-Band Shunt Switches

One way to obtain a higher isolation at X-band frequencies is to increase the shunt inductance of the switch so as to lower the resonant frequency. Figure 3.11 shows the isolation of a MEMS switch with $C_d = 2.7$ pF and $R = 0.35$ Ω for varying inductance values ($L = 8$ -64 pH). It is seen that the LC resonance frequency can be lowered to X-band frequencies with the use of a 40-60 pH inductance. Inductively-tuned MEMS shunt switches result in less bandwidth than standard shunt switches but with higher isolation around the resonant frequency.

A MEMS switch inductance of 15-40 pH can be achieved with the use of a narrow bridge width and a meander support structure (see Chapter 2). A large shunt inductance can also be synthesized by adding a high-impedance section of transmission line between the MEMS bridge and the ground-plane (Fig. 3.12). By properly choosing the length of this line, the series resonant frequency can be pushed down to the X-band frequency range. The only

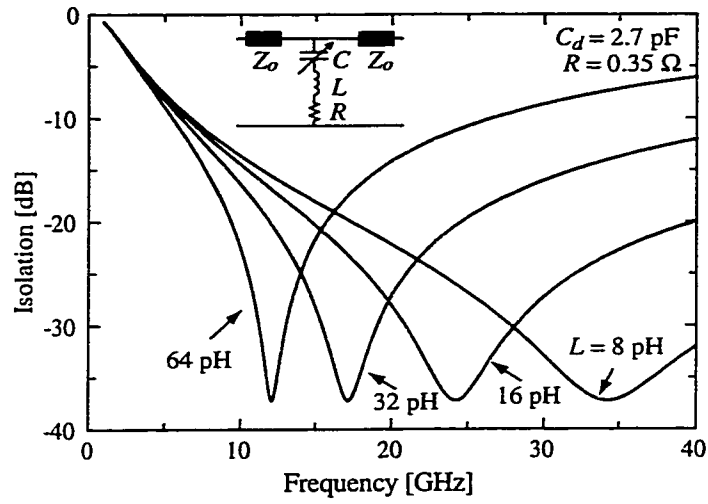


Figure 3.11: Simulated isolation of a MEMS shunt switch with a down-state capacitance of 2.7 pF and various values of inductance.

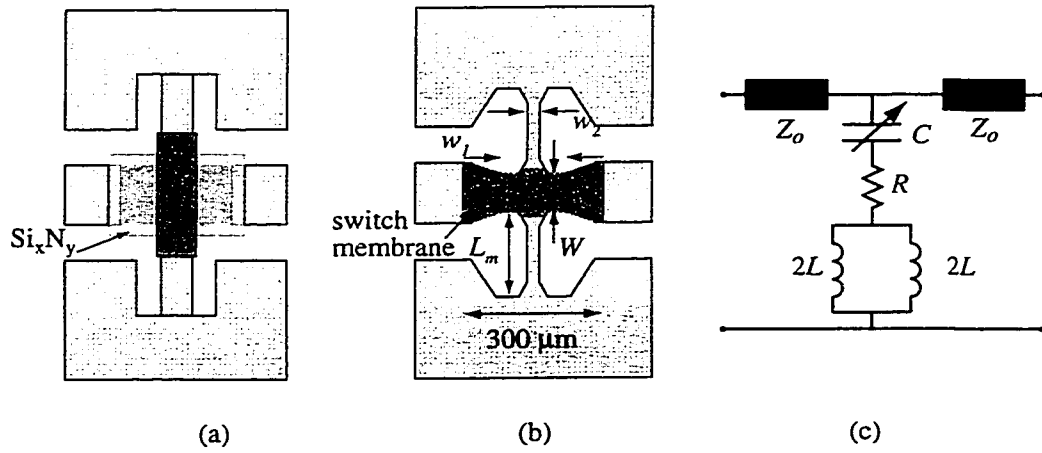


Figure 3.12: Inductively resonant MEMS shunt switch implementations (a,b) and an equivalent circuit model (c).

concern in this design is that the inductance and down-state capacitance of the switch must be carefully controlled so as to result in the correct resonant frequency.

3.4.1 Standard Configuration

Several inductively resonant MEMS shunt switches have been fabricated for X-band operation using a $50\ \Omega$ CPW line implementation ($96,160,96\ \mu\text{m}$) on a high resistivity silicon substrate. The fabrication procedure is based on a $300\ \mu\text{m}$ long, $6000\ \text{\AA}$ thick sputtered gold bridge, suspended $2.5\ \mu\text{m}$ above the center conductor. In this case, the metalization underneath the bridge is a smooth layer of $2000\ \text{\AA}$ thick refractory metal covered by a dielectric of $2100\ \text{\AA}$ of silicon nitride. The width of the capacitive section of the MEMS bridge (portion over center conductor of the CPW line) is $100\ \mu\text{m}$ or $150\ \mu\text{m}$ depending on the design. The length of the inductive section is either $0\ \mu\text{m}$ (no ground indentation) or $150\ \mu\text{m}$. The CPW line and the inductive section are $1.3\ \mu\text{m}$ thick.

The measurements are based on an on-wafer TRL calibration [1] and are referenced to $40\ \mu\text{m}$ from either side of the MEMS bridge (Figure 3.13). The calibration was not optimal and the noise floor was limited to $-35\ \text{dB}$ over the 2-20 GHz range. This is much higher than the normal value of $-60\ \text{dB}$.

Figure 3.13 shows the measured and fitted performance of a $100\ \mu\text{m}$ wide bridge in the down-state. The fitted parameters for no inductive tuning are $C = 4.8\ \text{pF}$, $L = 12\ \text{pH}$ and $R_s = 0.3\ \Omega$. This results in a resonant frequency of 21 GHz. The resonance with a $150\ \mu\text{m}$ long inductive transmission line section is shifted to 11 GHz, and the isolation is better than $-30\ \text{dB}$ from 11-13 GHz. The isolation is limited to $-35\ \text{dB}$ by the TRL calibration. Still, at 10-12 GHz, there is a 6-8 dB improvement in the isolation over the standard design. The fitting of the tuned bridge is done by taking the C , L values of the MEMS bridge and adding two short sections of $56\ \Omega$ CPW transmission line using Libra [6]. For both switches, the up-state insertion loss and return loss up to 13 GHz were less than $-0.2\ \text{dB}$ and $-15\ \text{dB}$ respectively.

Figure 3.14 represents the measured and fitted performance of two inductively tuned $150\ \mu\text{m}$ wide bridges, each with a $150\ \mu\text{m}$ long inductive section. The center-to-center

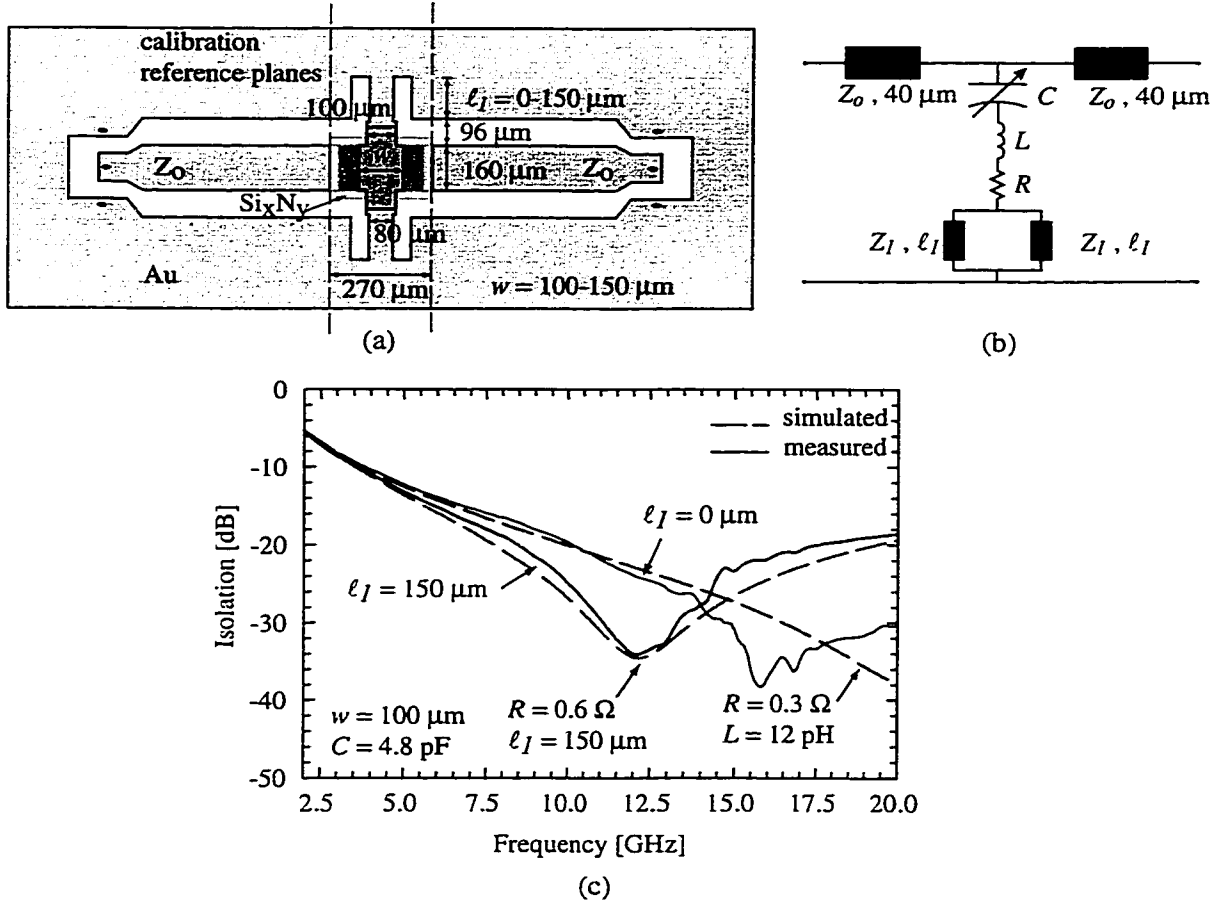


Figure 3.13: An inductive resonant MEMS shunt switch implementation (standard configuration) and its equivalent circuit model (a,b), and simulated and measured isolation in the down-state position for MEMS shunt switches with $w = 100 \mu\text{m}$ and $\ell_I = 0$ and $150 \mu\text{m}$ (c).

separation between the bridges is $300\ \mu\text{m}$. The measured isolation is better than $-30\ \text{dB}$ from 7-12.5 GHz. Note the resonance in the down-state isolation around 4 GHz due to the effect discussed in Section 3.5.2. The simulated performance predicts a much higher isolation, using Libra and using a full-wave simulator (Sonnet [4]). The discrepancy is due to the TRL calibration. The up-state insertion loss and return loss are less than $-0.4\ \text{dB}$ and $-15\ \text{dB}$, respectively, up to 13 GHz. The insertion loss and isolation may be improved by using thicker metal underlying the bridge and electroplated ($2\text{-}3\ \mu\text{m}$) transmission lines.

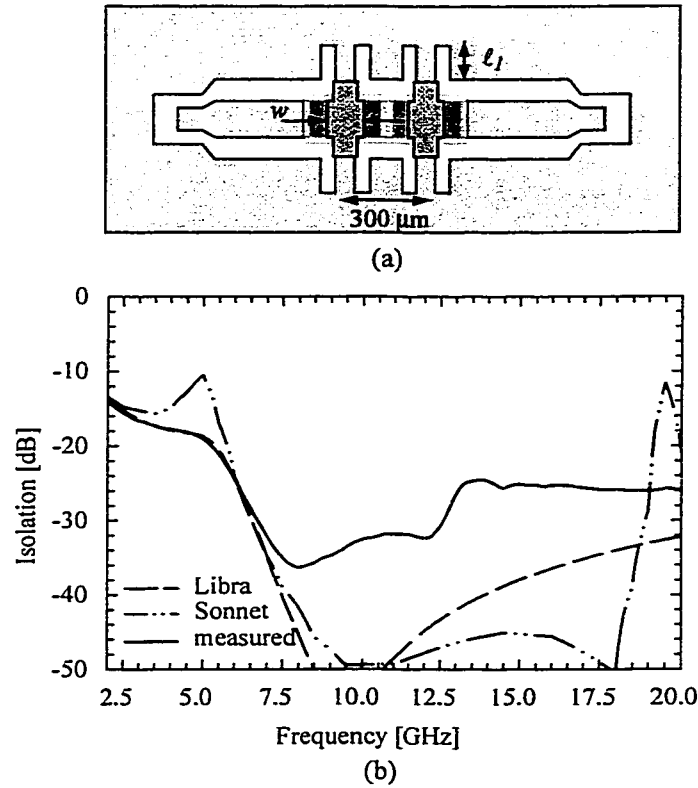


Figure 3.14: Simulated and measured S-parameters for a double MEMS shunt switch with $w = 150\ \mu\text{m}$, $\ell_1 = 150\ \mu\text{m}$, and $G/W/G = 96/160/96\ \mu\text{m}$. The equivalent circuit (Libra) and fullwave moment method (Sonnet) simulations predict higher isolation than the measurements indicate. This is due to the calibration floor of only about $-35\ \text{dB}$.

L_m [μm]	w_1 [μm]	w_2 [μm]	W [μm]	C_d [pF]	L [pH]	f_o [GHz]
176	140	60	100	4.5	32	13.3
176	140	40	100	4.5	38	12.2
266	140	40	100	4.5	47	10.9
266	140	30	100	4.5	52	10.4

Table 3.1: Fitted MEMS switch inductance (L) for several designs with various inductive section geometries. The CPW line dimensions are $G/W/G = 96/160/96$ μm on high-resistivity silicon.

3.4.2 Inline Configuration

An inline inductively-tuned MEMS shunt switch has been fabricated for X-band operation in a CPW configuration (96,160,96 μm) on a high-resistivity silicon substrate (3.12a). The in-line MEMS bridge is 300 μm long and is suspended 1.5 μm above the nitride layer. The thin inductive section, labeled w_2 in Fig. 3.12a, is widened to 140 μm underneath the MEMS bridge to result in a pull-down voltage of 15-20 V.

The inductance and down-state capacitance resonate at $\omega = 1/\sqrt{LC_d}$ with a quality factor of $Q = \frac{1}{R}\sqrt{\frac{L}{C_d}}$, where R is the resistance of the ground-line (Fig. 3.12). Figure 3.15 shows that a switch with $W = 100$ μm , $w_1 = 140$ μm , $L_m = 266$ μm , and $w_2 = 40$ μm has an equivalent inductance (L) of 47 pH, a down-state capacitance (C_d) of 4.5 pF, and a resistance (R) of 0.15 Ω . The switch resonates at 10.9 GHz with a quality factor of 21. The transmission line geometry around the switch (L_m , W , w_1 , w_2) can be modified to give different values of switch inductance and capacitance thereby resulting in different frequencies (Table 3.1) and in [11].

The measured and fitted down-state S-parameters for the MEMS shunt switch with $C_d = 4.5$ pF and various ground-line geometries are shown in Fig. 3.15. The up-state insertion loss and return loss were less than -0.2 dB and -15 dB, respectively, up to 13 GHz. As the line connecting the two ground planes becomes thinner or longer, the switch equivalent inductance increases, the resonant frequency decreases, and the Q of the resonance increases (bandwidth decreases). The isolation of a single shunt capacitive switch may therefore be increased by 10 to 20 dB at the expense of reduced bandwidth.

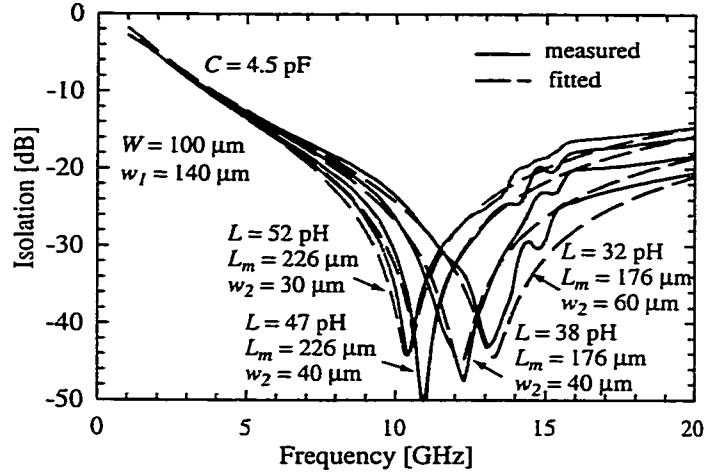


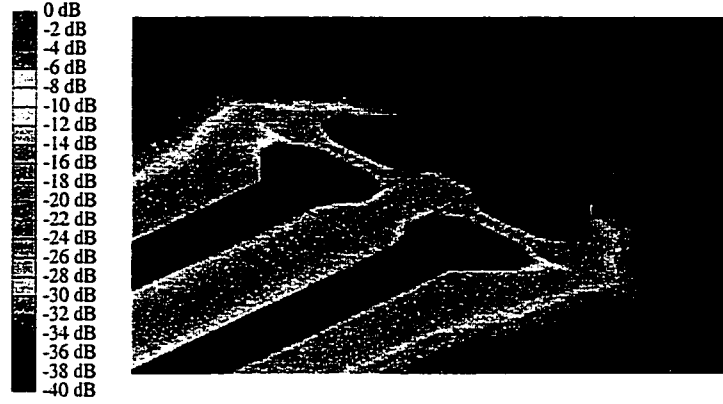
Figure 3.15: Measured and fitted isolation of MEMS shunt capacitive switches with various ground-line geometries ($W = 100 \mu\text{m}$, $w_1 = 140 \mu\text{m}$).

3.4.3 Comparison with EM Simulations

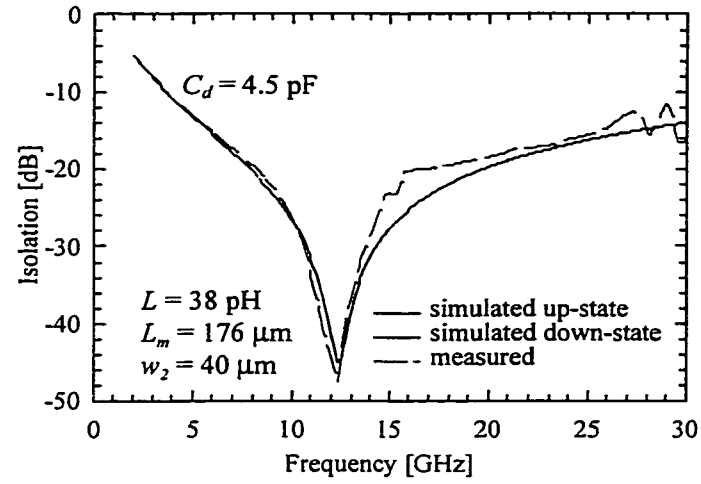
A full-wave Sonnet simulation of an inline capacitive shunt MEMS switch in the down-state is shown in Fig. 3.16. The switch was also fabricated in the down-state to ensure an ideal parallel-plate capacitance. The measured and simulated results (Fig. 3.16b) agree very well. Sonnet is a moment method full-wave simulator with an analytic Green's function formulation and the ability to include dielectric "bricks" in arbitrary locations. This allows accurate simulation and equivalent model extraction of the exact down-state performance of MEMS capacitive switches. At the date of publication of this thesis, Sonnet is the only commercially available code that can accurately perform this simulation.

3.4.4 Inline Double-Capacitance Design

Since the down-state capacitance of a shunt capacitive switch is limited partly by the mechanical limit of the width, the use of two inductively-resonant switches placed next to each other has been proposed. For the single switch shown in Fig. 3.17, the capacitive area is $100 \times 130 \mu\text{m}^2$ and the inductive lines are $125 \mu\text{m}$ long with a width of $15 \mu\text{m}$. The model follows the inductively-resonant approach with $C_d = 2.3 \text{ pF}$ and $L = 42 \text{ pH}$ (fitted from



(a)



(b)

Figure 3.16: Down-state (a) simulated average current distribution, and (b) simulated and measured S-parameters for an inline shunt capacitive MEMS switch. The switch is fabricated in the down-state position.

measured data).

The switches shown in Fig. 3.17 were fabricated to study the effect of multiple capacitive and inductive sections on the performance of MEMS shunt switches. The double-capacitance design is shown in Fig. 3.17b,d and is composed of independent capacitive switches with a gap of $20\text{ }\mu\text{m}$. Contrary to intuition, the gap in the capacitive section has a significant effect on the down-state isolation of the switch at X-band frequencies as shown in Fig. 3.18. The model is composed of two C_d , L , R circuits separated by a t-line length of $100\text{ }\mu\text{m}$ which is the distance between the inductive sections. Notice that the t-line length is not $20\text{ }\mu\text{m}$ (gap distance) since the delay between the two ground-plane connections must be taken into account. This model predicts a spurious resonance in the isolation response (Fig. 3.18). The spurious resonance is demonstrated using S-parameter measurements in the down-state position. Full wave EM simulations using Sonnet predict this spurious resonance (Fig. 3.18) as well. The difference between the measured and Sonnet simulations and the Libra circuit simulation is most likely due to coupling effects not taken into account in the equivalent circuit. However, these results show that placing two capacitive switches very close together can lead to some unwanted reduction in the down-state isolation.

3.5 Matching of Shunt Capacitive Switches

There are many cases when a large down-state capacitance is needed for high isolation, and where a large capacitance ratio cannot be achieved due to the fabrication technique used. This results in a high up-state capacitance and therefore high reflection losses. For example, to obtain an isolation of -26 dB at 10 GHz , a down-state capacitance of 12.8 pF is needed (using 3 MEMS switches of 4.3 pF each). For a capacitance ratio of 80, the up-state capacitance is 160 fF which results in an up-state reflection coefficient of -12 dB at 10 GHz . Another example is for a Ka-band switch with a down-state capacitance of 2.8 pF and a capacitance ratio of 40. In this case, the up-state capacitance is 72 fF which results in a -10 dB reflection coefficient at 30 GHz . The T and π -match circuits detailed below, provide an excellent solution to high up-state capacitance bridges.

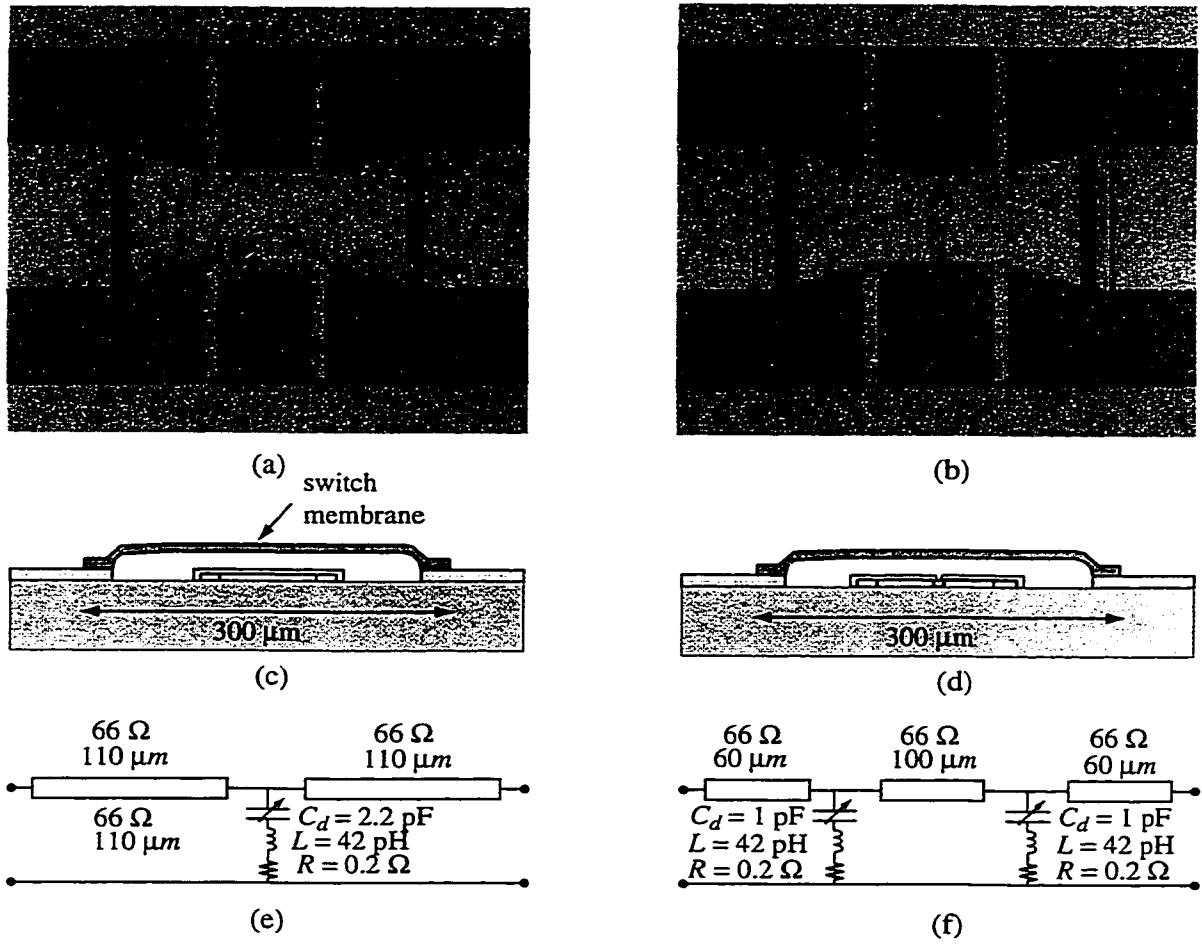
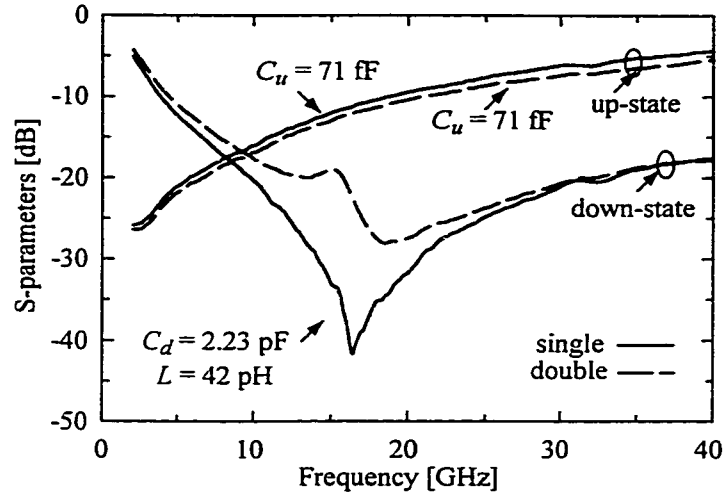


Figure 3.17: Photomicrograph of a MEMS X-band shunt switch (a) with one capacitive section, (b) with two capacitive sections, respective cross-sectional views (c,d), equivalent circuits (e,f), and measured response.

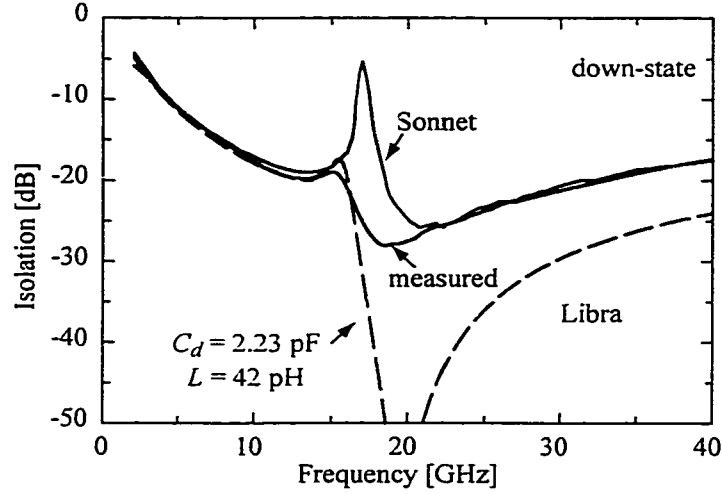
3.5.1 The T-match

One way to match the up-state capacitance is to use two short high-impedance sections of t-lines before and after the switch (Fig. 3.19a). These sections behave as series inductors and provide an excellent match at the design frequency. This is called a T-match circuit. The matching inductance can be derived from:

$$Z_{in} = (Z_o + j\omega L) \parallel \left(\frac{1}{j\omega C_u} \right) + j\omega L \quad (3.7)$$



(a)



(b)

Figure 3.18: Measured response of a MEMS X-band shunt switch with one (single) and two (double) capacitive sections (a), and simulated and measured isolation using Sonnet and Libra.

and $Z_{in} = Z_o$ results in:

$$L = \frac{1 \pm \sqrt{1 - (\omega C_u Z_o)^2}}{\omega^2 C_u} \quad (3.8)$$

There are two solutions for L , and the shortest t-line implementation results in:

$$L \simeq \frac{C_u Z_o^2}{2} \quad \text{for } \omega C_u Z_o < 0.2 \quad (3.9)$$

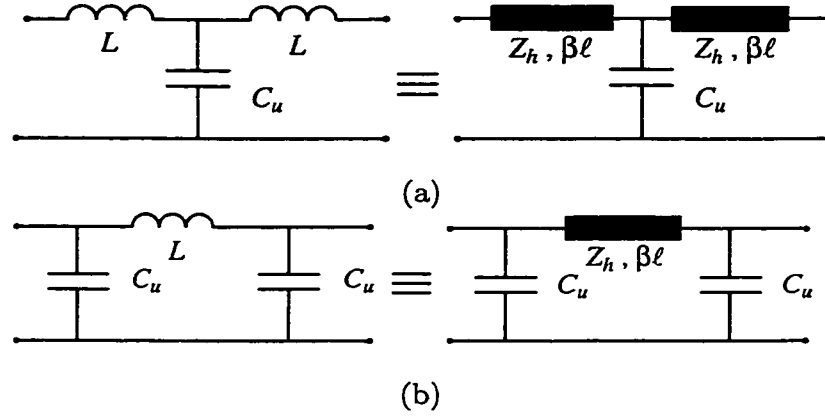


Figure 3.19: Layout for the T (a) and π (b) match circuits.

The equivalent high-impedance line (Z_h) with length (ℓ) is then obtained from [12]:

$$\beta\ell = \frac{\omega L}{Z_h} \quad \text{or} \quad \ell = \frac{Lv_o}{Z_h \sqrt{\epsilon_{eff}}} \quad (3.10)$$

where ϵ_{eff} is the relative effective dielectric constant of the t-line and $v_o = 3 \times 10^8$ m/s is the speed of light in free space. It is seen from Eq. (3.8) that there is a solution only for $\omega C_u Z_o < 1$, and the maximum up-state capacitance is $C_u = 318$ fF and 106 fF at 10 GHz and 30 GHz, respectively. For the case above with $C_u = 160$ fF at 10 GHz, Eq. (3.8) results in $L = 214$ pH. The corresponding line length is 394 and 320 μm for $Z_h = 65 \Omega$ and 80Ω respectively, using Eq. (3.10). The simulated line length using Libra for a perfect match at 10 GHz is 605 μm for $Z_h = 80 \Omega$. It is seen that Eq. (3.10) considerably underestimates the line length even for high impedance matching networks. For $Z_h = 65 \Omega$, the Libra simulations do not result in a possible solution (perfect match) at 10 GHz. This is explained in more detail below.

A more accurate solution for the t-line implementation can be obtained for the T-match circuit using the impedance transformation equations. The electrical length of the t-lines for a match condition at the input and output ports is given by ($S_{11} = 0$):

$$\tan(\beta\ell) = \frac{Z_h^2 - Z_o^2 \pm \sqrt{(Z_o^2 - Z_h^2)^2 - \omega^2 C_u^2 Z_h^4 Z_o^2}}{\omega C_u Z_h^3} \quad (3.11)$$

and

$$\tan(\beta\ell) \simeq \frac{\omega C_u Z_h Z_o^2}{2(Z_h^2 - Z_o^2)} \quad \text{for} \quad Z_h^2 - Z_o^2 \gg \omega C_u Z_h^2 Z_o \quad (3.12)$$

which simplifies to Eq. (3.9) and (3.10) when $Z_h \gg Z_o$. Again it is seen from Eq. (3.11) that a solution only exists for $\omega C_u Z_o Z_h^2 < Z_o^2 - Z_h^2$ which can be written as:

$$\omega C_u Z_o < 1 - \left(\frac{Z_o}{Z_h} \right)^2 \quad (3.13)$$

The maximum allowable up-state capacitance at 10 GHz is 130 fF and 194 fF for $Z_h = 65 \Omega$ and 80Ω , respectively. This is much smaller than the value given by the solution criteria of Eq. (3.8). The line length obtained from Eq. (3.11) agrees perfectly with Libra simulations for $C_u = 160$ fF and $Z_h = 80 \Omega$ at 10 GHz (see values above). For 30 GHz applications, the maximum allowable capacitance is 43 fF and 64 fF for $Z_h = 65 \Omega$ and 80Ω , respectively using Eq. (3.13). This seems to indicate that there is no solution for the case discussed above with $C_u = 72$ fF. This is not entirely true. One can still achieve a good match, down to -20 dB, by using Z_h and $\beta\ell$ which correspond approximately to values obtained for case of the maximum allowable capacitance. This is shown in Fig. 3.20b for $C_u = 72$ fF, where $Z_h = 80 \Omega$, $\ell = 314 \mu\text{m}$ results in a perfect match at 25 GHz and a -23 dB match at 30 GHz. The same idea applies for 10 GHz with $C_u = 160$ fF and $Z_h = 65 \Omega$. The T-match method can also be applied to V-band and W-band switches for up-state capacitances of 15-25 fF.

The isolation response of the T-match circuit is given by the MEMS shunt switch (C_d, L, R) , and is not very sensitive to the lengths of the inductive sections. In the up-state position, the insertion loss of T-match circuits is less than 0.15-0.2 dB up to W-band frequencies. As mentioned earlier, the inline capacitive shunt MEMS switches have a reduction in the up-state return loss as compared to the standard shunt design due to the partial T-match inherent in their design.

3.5.2 The π Match

Another way to obtain an excellent match and high isolation is to use the π match circuit (Fig. 3.19). In this case, a short section of high-impedance line is used between two shunt switches to result in an impedance match. The matching inductance can be derived from:

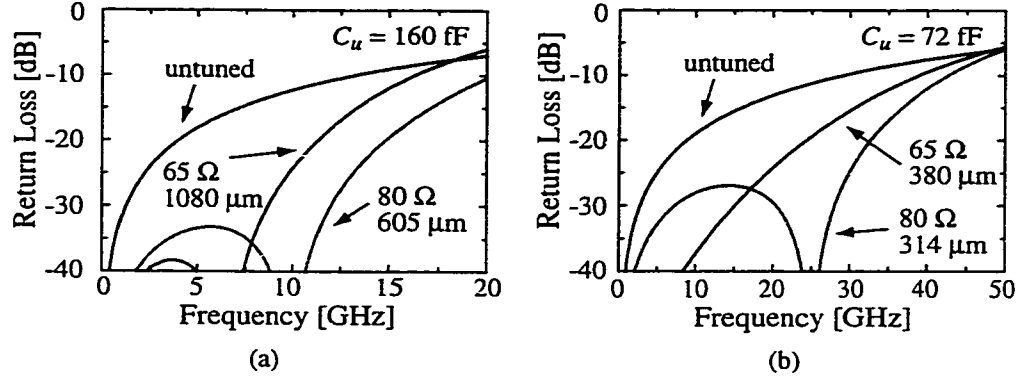


Figure 3.20: Simulated return loss for the T-match circuits at (a) 10 GHz and (b) 30 GHz.

$$Z_{in} = ((Z_o || \frac{1}{j\omega C_u}) + j\omega L) || \frac{1}{j\omega C_u} \quad (3.14)$$

and $Z_{in} = Z_o$ results in:

$$L = \frac{2Z_o^2 C_u}{1 + (\omega C_u Z_o)^2} \quad (3.15)$$

with

$$L \simeq 2Z_o^2 C_u \quad \text{for} \quad \omega C_u Z_o < 0.2 \quad (3.16)$$

and the high-impedance line length can be obtained from Eq. (3.10) above. A more accurate solution can be derived using transmission line theory. Setting $S_{11} = 0$, we obtain:

$$\tan(\beta\ell) = \frac{2\omega_o C_u Z_h Z_o^2}{Z_h^2 - Z_o^2 + (\omega_o C_u Z_h Z_o)^2} \quad (3.17)$$

which simplifies to Eq. (3.16) for $Z_h \gg Z_o$. Note that there is always a solution irrespective of the value of C_u .

The π match is ideal for microwave and mm-wave applications and results in a wideband match and very high isolation for reasonable down-state capacitance values. Fig. 3.21 presents the S-parameters for an X-band π circuit with $C_u/C_d = 80$ fF/6.4 pF and $L = 400$ pH calculated using Eq. (3.16). The corresponding line length is $735 \mu\text{m}$ on silicon for $Z_h = 65 \Omega$, calculated using Eq. (3.16) and (3.10). The exact value is $1307 \mu\text{m}$, using Eq. (3.17).

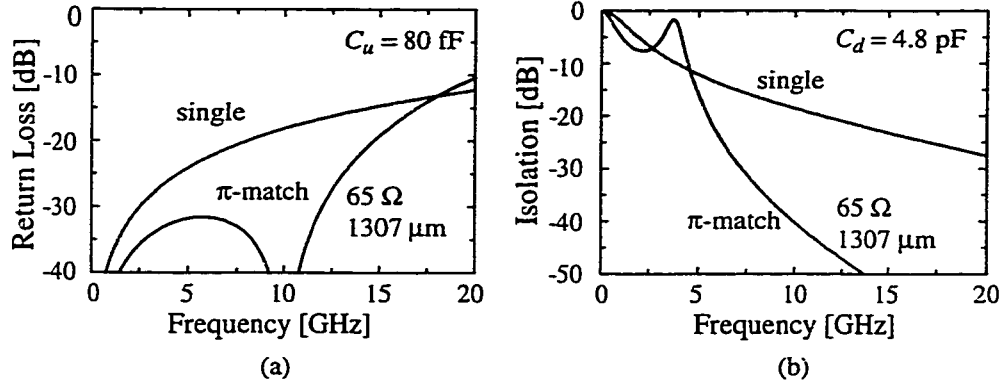


Figure 3.21: Simulated return loss for the π -match circuits ($Z_h = 65 \Omega$ and $\ell = 1307 \mu\text{m}$) at 10 GHz in the (a) up-state and (b) down-state positions.

An approximate formula for the down-state isolation of the π -match circuit is given as:

$$|S_{21d}|^2 \simeq \frac{4}{\omega^4 C_d^4 Z_h^2 Z_o^2} \left(\frac{1 + \tan^2(\beta\ell)}{\tan^2(\beta\ell)} \right) \quad \text{for } \beta\ell > 0.2 \quad (3.18)$$

For $\beta\ell < 0.1$, the isolation becomes similar to that of a single shunt switch but with double the capacitance value. However, if $\beta\ell < 0.1$, the switch is no longer matched. The improvement in isolation of the π -circuit over a single switch is approximately a factor of $2\times$ in dB due to the transforming effect of the inductive section. It is for this reason that the π -match circuit is ideal for high-isolation switches. In the up-state position, the insertion loss of π -match circuits is less than -0.2 dB up to W-band frequencies.

The π -match is also very useful for W-band operation if a large uncertainty is present in the down-state capacitance value (and thus, the LC resonant frequency), and ensures a very high isolation independent of the down-state capacitance value, as long as it is higher than 0.2 pF. This is illustrated in Fig. 3.22 for $C_u = 16$ fF and $C_d = 320$ fF.

3.6 Design of High-Isolation Tuned Shunt Switches

In many communication and radar applications, a high-isolation switch is needed over a specified bandwidth. The bandwidth is relatively narrow, around $0.5\text{--}4$ GHz for a center frequency of $8\text{--}40$ GHz. The specifications of such a switch is an excellent match in the up-

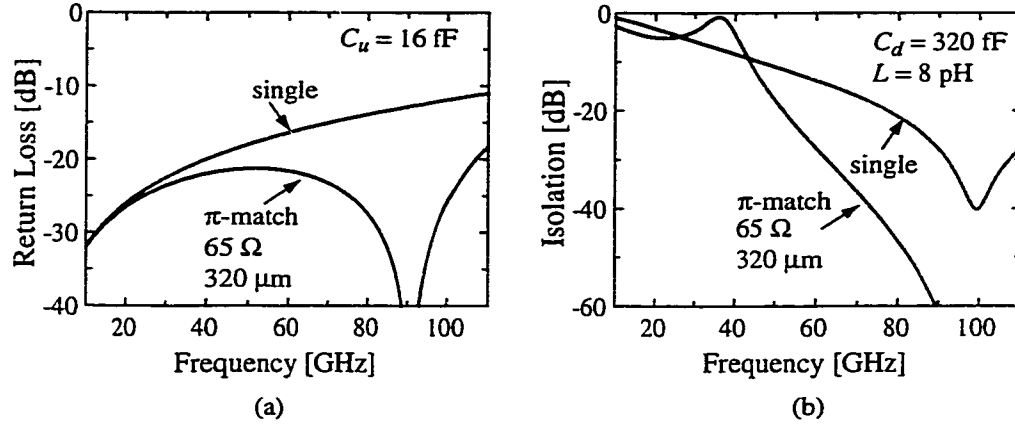


Figure 3.22: Simulated return loss for the π -match circuits at 90 GHz in the up-state (a) and down-state (b) positions.

state position ($S_{11} < -20$ dB), and very high isolation in the down-state position ($S_{21} < -40$ to -50 dB).

The above specifications can be easily met using a single MEMS series switch with $C_u = 2$ fF (up to 10 GHz), or a series/shunt switch design (up to 50 GHz). If a capacitive shunt switch technology is used, then one can achieve such isolation requirements using a tuned approach. The design, shown in Fig. 3.23a, consists of two shunt switches separated by a high-impedance section of transmission line. The length of the midsection is chosen such that the reflection from the first switch and the reflection from the second switch cancel when the switches are in the up-state position. The tuned design has been used extensively with PIN diode switches at 10-100 GHz, and results in an excellent match in the up-state position, and very high isolation in the down-state position. The tuned switch is essentially the same as the π -match case and the design equations are given in Section 3.5.2.

3.6.1 A Ka-Band Tuned Switch

A 30 GHz tuned switch on a high-resistivity silicon substrate was built at the University of Michigan ($C_u = 60$ fF, $\beta\ell = 65^\circ$, $Z_h = 65 \Omega$) [7, 10]. The up-state insertion loss is -0.2 to -0.4 dB from 20-40 GHz, and is effectively the loss of the midsection line with 8000 Å of gold (Fig. 3.23b). The nominal gap height was lowered from 4.0 μm to 1.5 μm , thereby

decreasing the pull-down voltage from 50 V to 15 V for a typical 300 μm long gold bridge. The down-state capacitance is $C_d = 1.1$ pF, resulting in a capacitance ratio of 20. This is due to the surface roughness of the bridge and dielectric layer and is lower than the theoretical capacitance ratio of 45. Still, the isolation is better than -30 dB above 26 GHz. The measured isolation above 30 GHz was limited by substrate isolation and probe-to-probe coupling. A 2.2 pF down-state capacitance results in an isolation greater than -40 dB above 22 GHz, and -54 dB at 30 GHz.

3.7 The Cross Switch

In an effort to further increase the bandwidth and down-state isolation of the tuned shunt switch, a novel “cross” switch was developed (Fig. 3.24a). The inline and shunt switch-pairs produce two independent reflection nulls (Fig. 3.24b) [10]. In the up-state position, the CPW line impedances and electrical lengths can be optimized to give an excellent return loss over a wide bandwidth. In the down-state position, the two shunt stubs present an additional short circuit at the cross node resulting in very high isolation. The only complication of this implementation is the associated parasitics of the cross-junction, which can be modeled using modern EM simulation tools.

The measured and simulated S-parameters of a typical cross switch are shown in Fig. 3.24b. The midsection line impedance, Z_1 , is 66 Ω with a length of 350 μm and the shunt section line impedance, Z_2 , is 50 Ω with a length of 170 μm . The tuned cross switch results in an up-state reflection coefficient of less than -20 dB from 22-38 GHz, with a measured insertion loss of -0.3 to -0.6 dB, respectively. Even with the non-optimal down-state capacitance, the cross switch attained greater than -40 dB isolation from 17-40 GHz for $C_{d1} = 1.5$ pF and $C_{d2} = 0.66$ pF, with inductances of $L_1 = 9$ pH and $L_2 = 12$ pH. If a higher down-state capacitance ratio ($C_r/C_d = 45$) was achieved, the cross design would produce an isolation greater than -60 dB above 12 GHz, and more than -90 dB at 30 GHz.

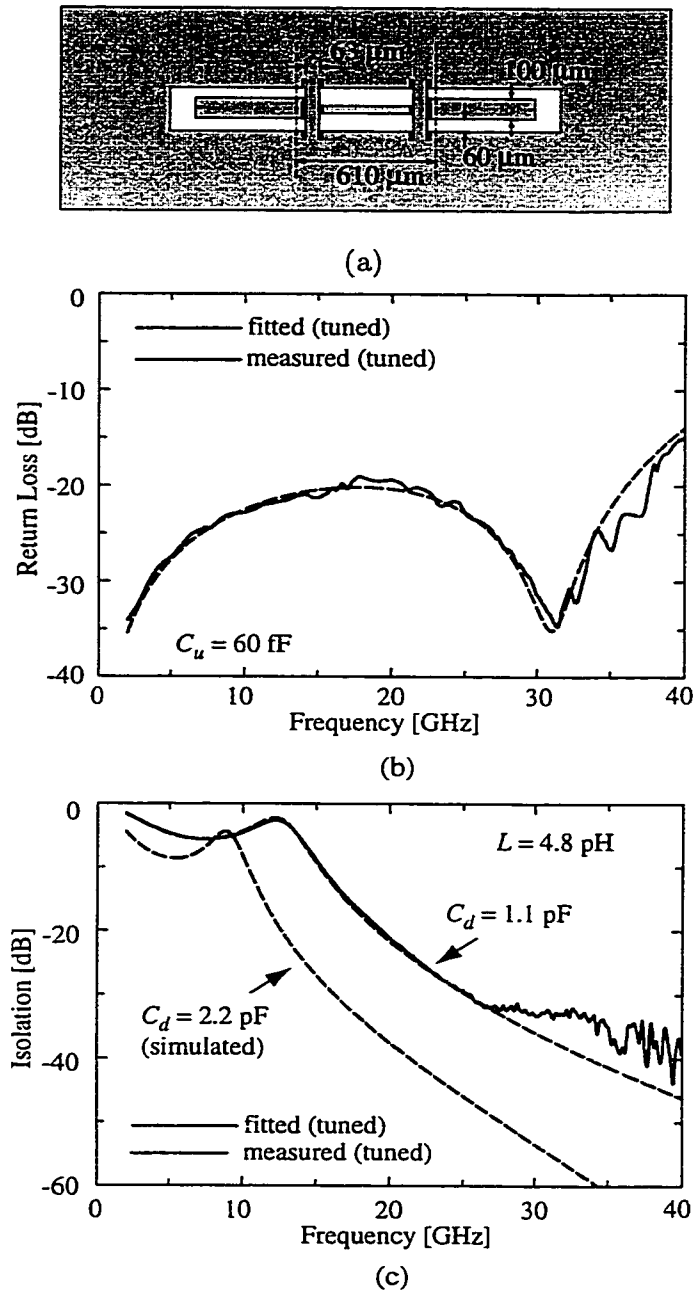


Figure 3.23: Physical implementation of the shunt Ka-band tuned MEMS switch (a), and measured S-parameters (b,c).

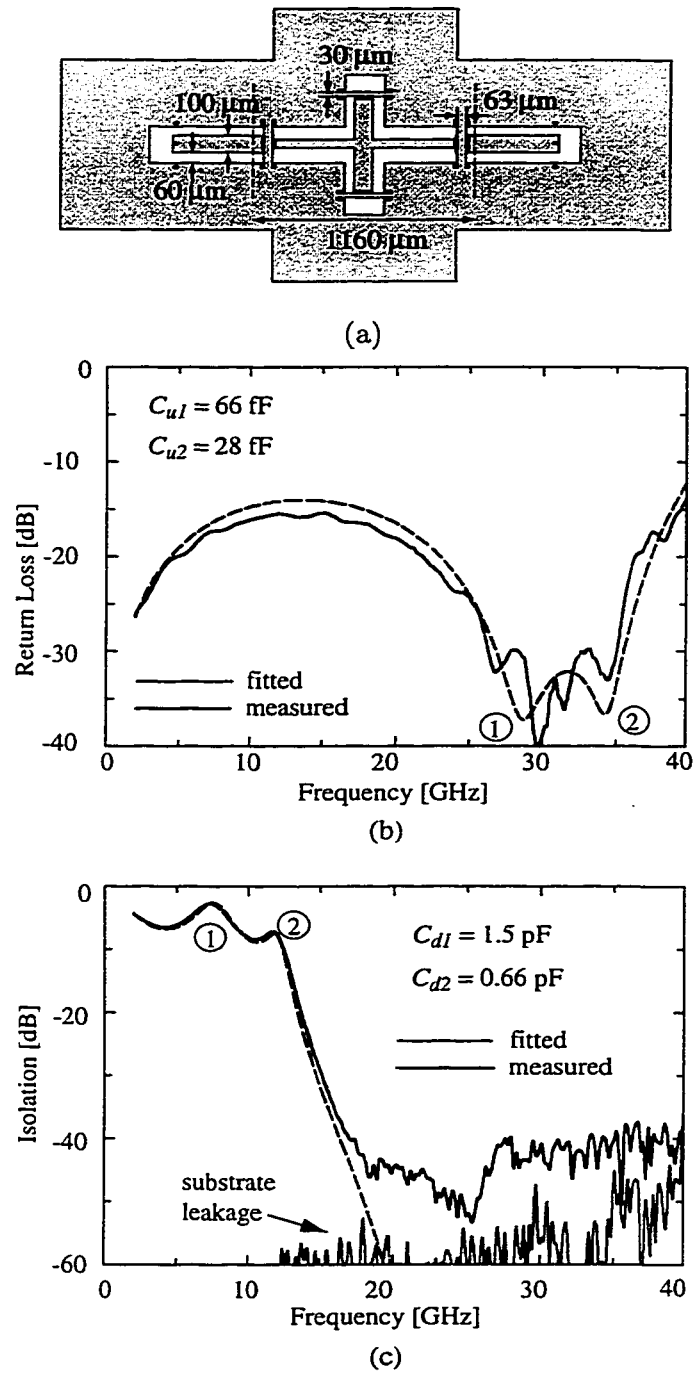
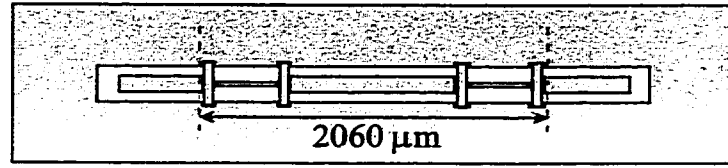


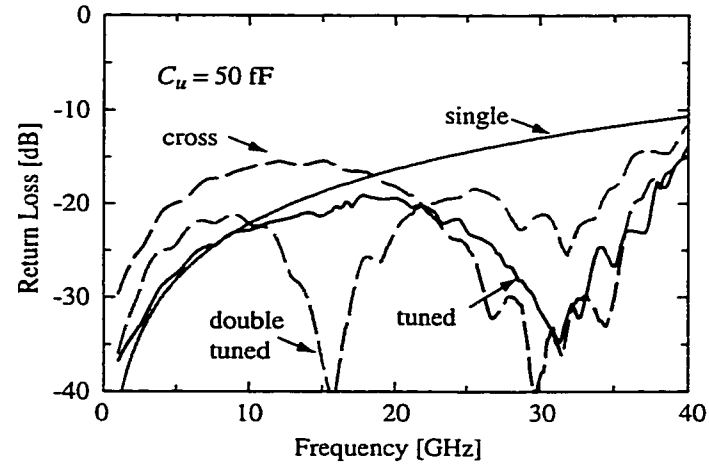
Figure 3.24: Physical implementation of the shunt Ka-band MEMS tuned cross switch (a), and measured S-parameters (b,c). The location of the nulls in the return loss, labeled (1) and (2), are controlled by the inline and parallel resonant structures, respectively.

3.8 The Double Tuned Switch

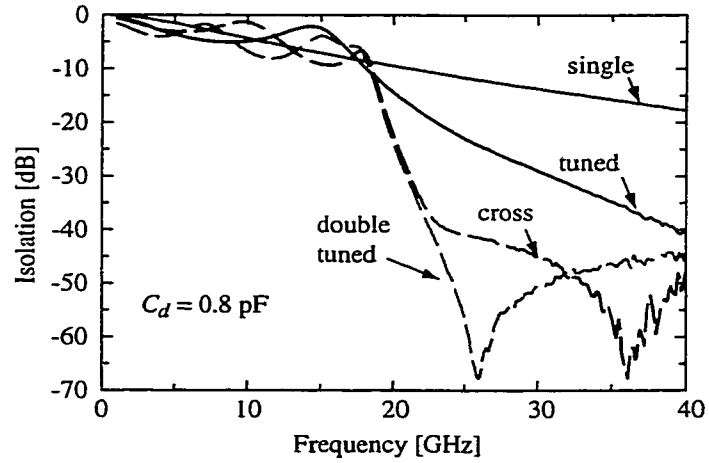
The desire to achieve even higher isolation leads to the incorporation of more membrane switch elements. Cascading two of the tuned switches is the next logical step. The simplest way to do this is to separate the two cascaded sections by approximately a quarter wavelength transmission line of impedance Z_o . A plot comparing the up and down-state measured S-parameters for a single, tuned, cross and a double tuned switch for $C_d = 0.8$ pF is shown in Fig. 3.25. This improvement in isolation over a single switch or the simple tuned switch comes at the expense of size and increase in the insertion loss. The cross switch has very similar performance while taking up much less area. In practice the isolation is limited to approximately -60 dB by the presence of substrate modes. These unwanted substrate modes can be reduced for very high isolation applications by micro-machining mode suppressing structures in the substrate [13]. Other linear four or more membrane switches can be developed with similar performance. As the number of membrane switch elements increases, the design begins to resemble the distributed MEMS phase shifters and wideband switches of Barker *et al.* [14].



(a)



(b)



(c)

Figure 3.25: Physical implementation of the shunt Ka-band MEMS tuned cross switch (a), and measured S-parameters (b,c).

CHAPTER 4

ELECTROMAGNETIC MODELING OF SERIES SWITCHES

The series MEMS switch can be modeled using many of the same techniques that are used to model shunt MEMS switches. This chapter covers the electromagnetic modelling of capacitive and DC-contact MEMS series switches.

4.1 Physical Description of MEMS Series Switches

Several different MEMS series switch are shown in Fig. 4.1 and Fig. 4.2. The switch geometry follows the same definitions as for the shunt switch. A 40-100 μm gap (open circuit) is created in the microwave t-line when the switch is in the up-state position resulting in high isolation. When the switch is activated, it falls down on the t-line and creates a short circuit between the open ends. Series switches are, for most designs, DC contact switches and can work at low frequencies (100 MHz and lower). Since the MEMS switch creates a DC contact with the t-line when activated, a separate electrode is needed to mechanically actuate the switch. When the bias voltage is removed, the MEMS switch returns back to its original position due to the internal restoring forces of the cantilever.

The cantilever is fabricated using a low-stress nitride or oxide layer (1-2 μm thick) with a metal portion at its tip (Fig. 4.1). This metal contact layer is composed of a 0.5-2 μm -thick Au layer or other proprietary metals, and is isolated from the actuation portion of the cantilever by 30-60 μm of nitride (or oxide). This results in very low parasitics in the

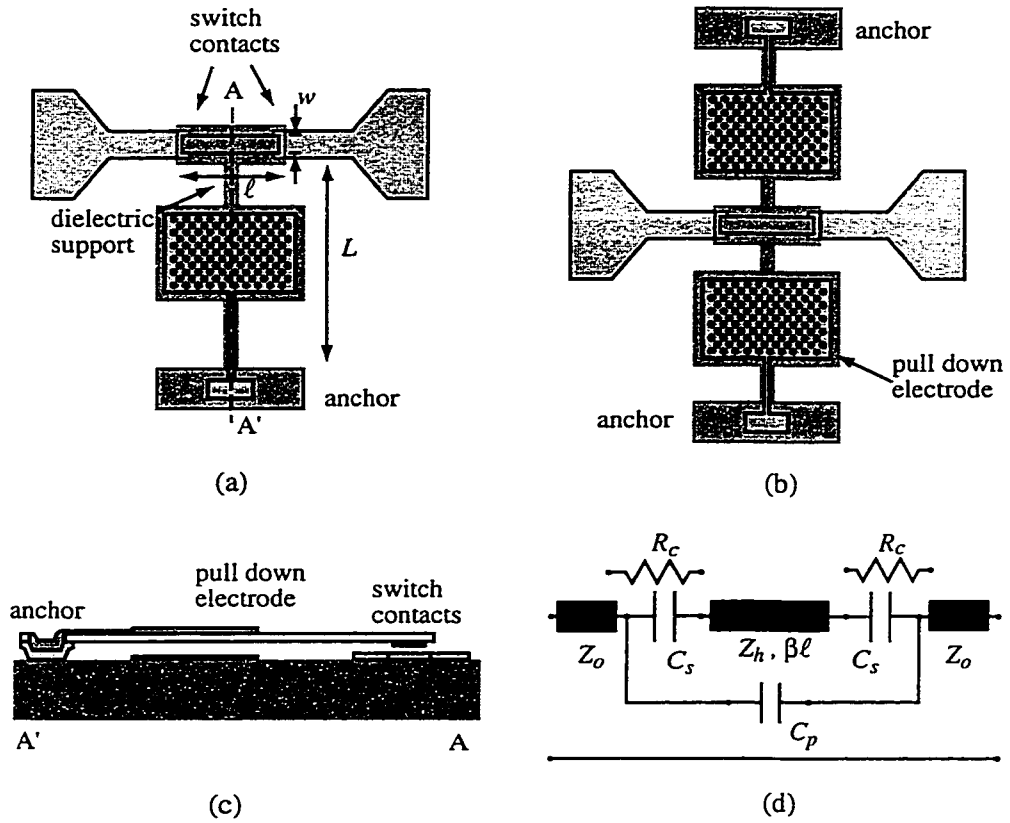


Figure 4.1: DC-contact MEMS series switches with two contact areas (a,b), cross-section view (c), and the equivalent circuit model (d).

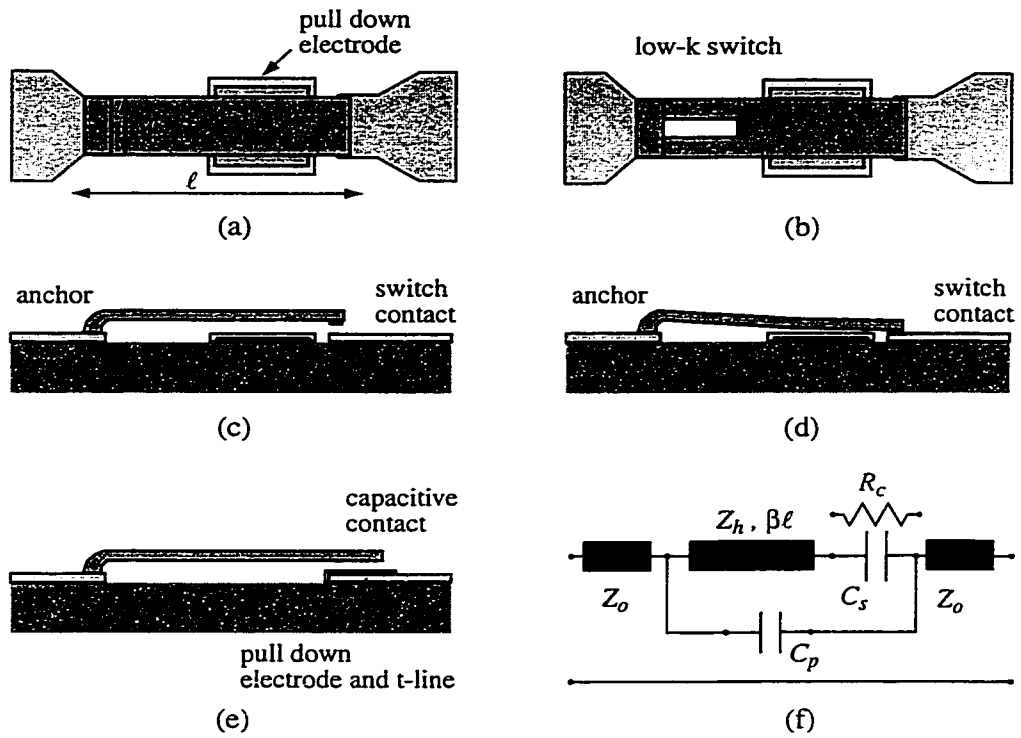


Figure 4.2: Inline DC-contact MEMS series switches with one contact area (a,b), cross-section in the up and down-state positions (c,d), cross-section of a capacitive inline switch (e), and general circuit model (f).

up-state position. Another metal layer is needed under the actuation electrode and should be connected to the DC actuation circuit (ground or V_s). The actuation pad is insulated from the beam with a 1-2 μm -thick dielectric layer (oxide or nitride). An array of closely spaced holes are placed in the actuation electrode to increase the speed of the switch. In some designs, the metal contact layer also has a closely spaced array of holes to further increase the speed of the switch.

Typical values of the series switch geometry are a height of 1.5-3 μm , a total length of $L = 300\text{--}400\ \mu\text{m}$, and an inline length of $\ell = 80\text{--}160\ \mu\text{m}$ depending on the t-line gap and the contact area of the switch. The microwave t-line is 20-60 μm wide, and the metal-to-metal contact area is generally much less than the width of the microwave t-line. The actuation pad is placed 100-200 μm from the anchor. This distance is rarely shorter than 70 μm due to the sharp increase of the actuation voltage with decreasing electrode placement (see Chapter 6 for details). The resulting pull-down voltage is 15-60 V depending on the switch design.

The series switch can be implemented in a CPW or microstrip configuration. In the CPW implementation, the actuation circuit is built on top of the ground plane of the CPW line. A series switch can also be built with one cantilever arm, or with two arms on both sides of the t-line, effectively becoming similar to a fixed-fixed beam design (Fig. 4.1).

Some series switches are built with a cantilever arm in the direction of the microwave t-line (Fig. 4.2). The operation of these switches is similar to the cantilever switches except that there is only one contact area between the switch and the microwave t-line. The inline series switch must have a continuous metal path from its anchor to the contact area since the RF/microwave current passes by the entire switch. The inline switch is around 300-400 μm long and the actuation electrode is typically placed 200-250 μm from the anchor to result in a reasonably low pull-down voltage (15-50 V). Again, a thick silicon nitride (or oxide) layer is used to DC isolate the switch from the actuation electrode. The inline series switch can also be fabricated using a low spring-constant design which results a lower actuation voltage (Fig. 4.1). Further details on the mechanical characteristics of the inline switch can be found in Chapter 6.

The series switches described in Figs. 4.1 and 4.2 can also be fabricated with a capacitive

contact between the cantilever arm and the t-line. The main advantage of this design is the elimination of the metal-to-metal contact resistance and the associated metal-to-metal welding in high power applications. Note that for the inline switch, a separate electrode is not needed to pull the cantilever arm in the down-state position since the DC pull-down voltage can be applied directly on the t-line (Fig. 4.1). The main disadvantage of capacitive series switches is that they do not provide a short-circuit at RF frequencies (100 MHz to 2 GHz) since the down-state capacitance is typically 1-4 pF. However, with the use of very high dielectric-constant materials ($\epsilon_r = 40-200$), it is possible to extend the frequency range of capacitive series switches to 1 GHz or below.

4.2 Electromagnetic Modeling of MEMS Series Switches

4.2.1 Up-State Capacitance:

The up-state capacitance is composed of a series capacitance (C_s) between the t-line and the switch metal, and a parasitic capacitance (C_p) between the open ends of the t-line. The total up-state capacitance of the series switch is the same for a DC-contact switch or a capacitive series switch, and is:

$$C_u = \frac{C_s}{2} + C_p \quad (4.1)$$

for a cantilever switch with two contact areas (Fig. 4.1d), and

$$C_u = C_s + C_p \quad (4.2)$$

for an inline switch with one contact area (Fig. 4.2f).

The contact area between the MEMS switch and the t-line is around $5 \times 5 \mu\text{m}$ for metal-to-metal contact switches, and around $50 \times 60 \mu\text{m}$ for capacitive series switches. In general, small bumps are defined on the cantilever so as to have a small contact area and a large contact force for metal-to-metal switches.

The series capacitance, C_s , is composed of a parallel-plate component ($C_{pp} = \epsilon A/g$) and a fringing component which is around 30-60% of C_{pp} (see Section 2.4.1 on shunt switches). The parasitic capacitance can be calculated using electromagnetic software packages, such

as IE3D, Sonnet or HFSS. Figure 4.3 shows the simulated parasitic capacitance versus frequency for various line widths and line-to-line separations on silicon and quartz substrates. It is seen that for a CPW center line width of $40\text{ }\mu\text{m}$, C_p is less than 2 fF (or 4 fF) for a separation of $60\text{ }\mu\text{m}$ on quartz (or silicon) substrates. The parasitic capacitance must also take into account the fringing capacitance to the actuation electrode. This is best calculated using numerical techniques, and is negligible if the electrode is $40\text{-}60\text{ }\mu\text{m}$ away from the t-line.

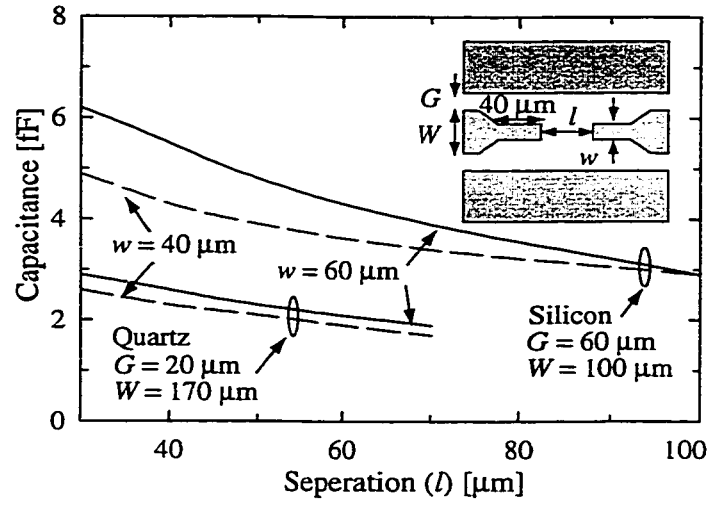
The capacitance of several MEMS series switch geometries are presented in Chapter 5. It is seen that a C_u of 2-6 fF can be easily achieved for a height of $1.5\text{-}3\text{ }\mu\text{m}$, a line width of $30\text{-}40\text{ }\mu\text{m}$, an electrode separation of $40\text{-}60\text{ }\mu\text{m}$, and a t-line gap of $60\text{-}100\text{ }\mu\text{m}$. The 2-6 fF up-state capacitance results in very high isolation up to mm-wave frequencies.

4.2.2 Current Distribution

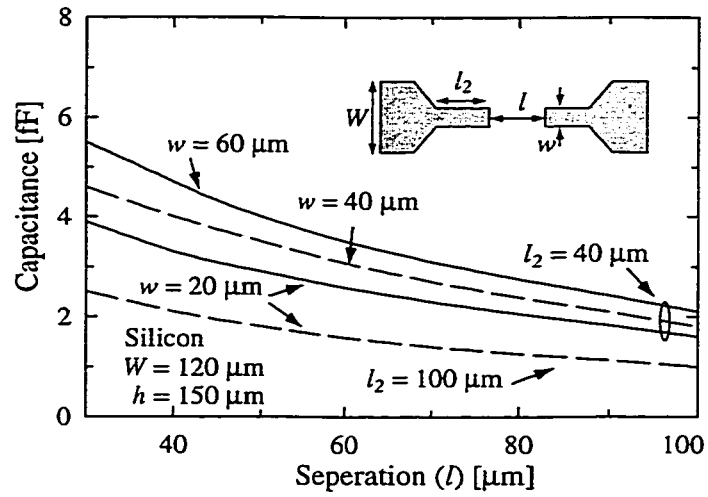
The current distribution on a series switch in the down-state position is very similar to that of the microstrip or CPW t-line. The reason is that the series switch is simply a continuation of the t-line. Simulations have shown that the current is concentrated on the edge of the metal bridge, even if the bridge is only $40\text{ }\mu\text{m}$ wide. Therefore, small holes can be placed in the center part of the MEMS cantilever without changing the current distribution (the holes may be needed for a faster operation of the switch). Also, in the case of the standard cantilever implementation, there is very little RF current on the pull-down electrode. This is due to the small capacitance between the MEMS suspended electrode and the pull-down electrode ($< 1\text{ fF}$).

4.2.3 Down-State Resistance

The series resistance of the MEMS switch is that of a short section of transmission line together with a DC contact resistance. The contact resistance depends on the size of the contact area, the mechanical force applied and the quality of the metal-to-metal contact [15]. Hyman measured a gold-to-gold contact resistance of $0.1\text{ }\Omega$ for an applied force of $100\text{-}500\text{ }\mu\text{N}$, a contact area of $20\text{ }\mu\text{m}^2$ and a current of $0.1\text{-}10\text{ mA}$. The contact



(a)



(b)

Figure 4.3: Parasitic capacitance (C_p) for various gap and line geometries on silicon and quartz substrates for CPW (a) and microstrip designs (b).

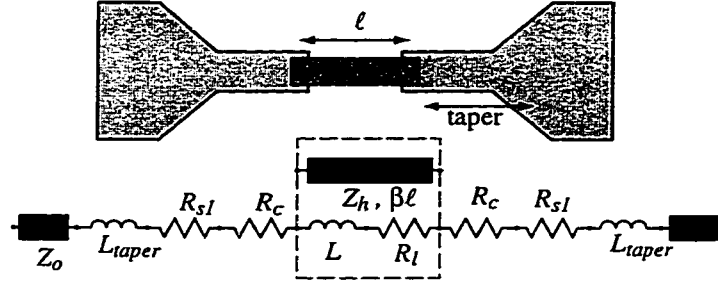


Figure 4.4: Equivalent circuit for the series switch in the down-state position.

resistance is sensitive to the current density and heat dissipation in the contact layer, and doubles for a current of 50 mA. The values above are given for very clean gold layers, and practical contact resistances are around 0.5-1 Ω per contact area.

The MEMS series switch resistance between the contact areas is dependent on its length and width. The switch resistance is obtained by calculating the loss of a t-line of the same dimensions of the MEMS switch and using Eq. (2.8) to determine the equivalent series resistance. The switch resistance is typically $R_l \leq 0.25 \Omega$ for a switch length of 100 μm , a width of 40 μm , and a thickness of 0.5-1 μm . Also, one must add the t-line loss (and equivalent resistance, R_{s1}). This depends on the definition of the reference planes, and can be obtained from the t-line attenuation and using Eq. (2.8). The total switch resistance is (Fig. 4.4):

$$R_s = 2R_c + 2R_{s1} + R_l \quad (4.3)$$

for a cantilever switch with two contact areas,

$$R_s = R_c + 2R_{s1} + R_l \quad (4.4)$$

for an inline switch with one contact area, and

$$R_s = 2R_{s1} + R_l \quad (4.5)$$

for a capacitive contact switch.

For DC-contact switches, the series resistance is dominated by R_c . The total switch resistance is 1-2 Ω depending on the contact area and applied force.

4.2.4 Loss

The loss of a MEMS series switch can be calculated from the measured values or using a circuit simulator, as $Loss = 1 - |S_{11}|^2 - |S_{21}|^2$. It can also be derived from the CLR circuit using the same approach as the shunt switches. The power loss in the series switch is $P_{loss} = I_s^2 R_s$, where I_s is the current in the switch, and R_s is given by Eq. (4.3)-(4.5) depending on the number of the contact areas. The intrinsic loss of the MEMS series switch is (neglecting t-line loss):

$$Loss = \frac{4R_s Z_o}{|Z_s + 2Z_o|^2} \quad (4.6)$$

In the up-state position, $Z_s = \frac{1}{j\omega C_u}$, and the loss becomes:

$$Loss = 4\omega^2 C_u^2 R_s Z_o \text{ for } S_{21} \ll -10 \text{ dB} \quad (4.7)$$

This loss is insignificant since the capacitance in the up-state position is 2-8 fF, and the loss at 10-30 GHz for $R_s = 1 \Omega$ is less than -0.001 dB (t-line loss is not included).

In the down-state position, $Z_s = R_s + j\omega L$, and the loss becomes:

$$Loss = \frac{R_s}{Z_o} \text{ for } \omega L \ll Z_o \quad (4.8)$$

where R_s is the total resistance of the switch. For a total contact and switch resistance of 1-3 Ω , the loss is -0.1 to -0.3 dB, and is nearly independent of frequency. The loss of the microwave t-line up to the reference planes should also be included to obtain the total switch loss.

The capacitive series MEMS switch does not suffer from the contact resistance effects, and its loss is entirely defined by the reference planes and the taper of the t-line around the switch. Therefore, capacitive series MEMS switches should result in a very low insertion loss in the down-state position, around -0.05 to -0.1 dB, depending on the definition of the reference planes.

4.2.5 Inductance

The MEMS switch is accurately modeled using C_s and C_p , and a short section of high-impedance t-line with a width w (20-40 μm) and suspended g μm above the substrate.

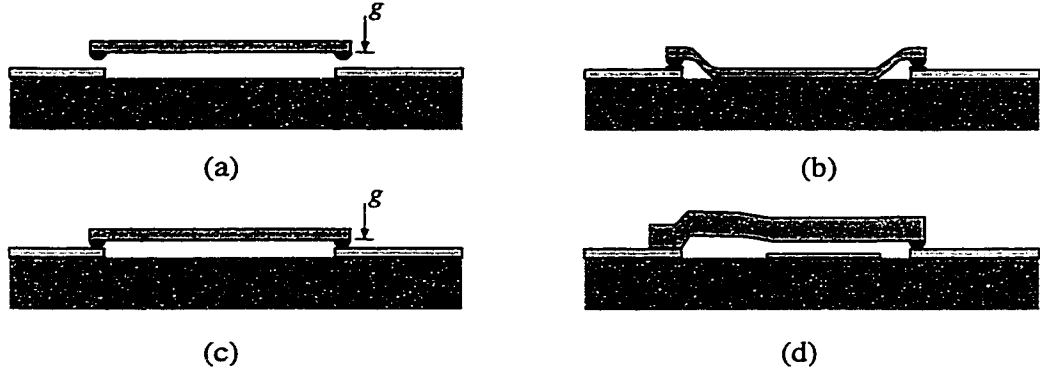
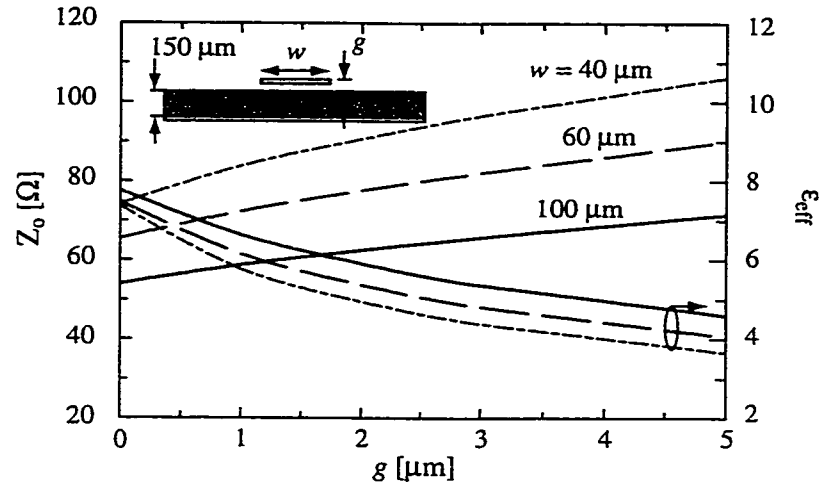


Figure 4.5: Illustrated cross section of a MEMS series switch in various configurations: (a) up-state position, (b) down-state position with no residual height, (c,d) down-state position with a residual height, g .

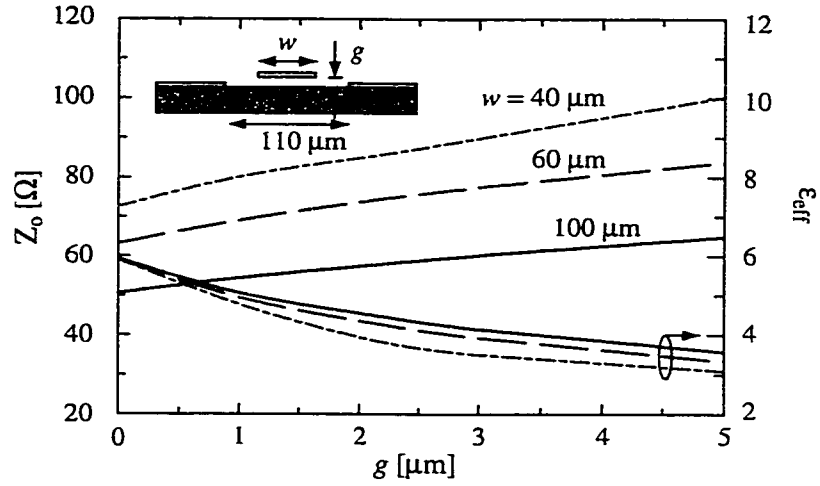
The height is 1.5-4 μm in the up-state position, and 0-2 μm in the down-state position depending on the mechanical force used and the stiffness of the cantilever (Fig. 4.5). The t-line parameters vs. height from the substrate are shown in Fig. 4.6. These are calculated using electrostatic techniques or a microwave circuits software [2, 6]. In the down-state position, it is possible to model the t-line (with length ℓ) by a series inductance given by [12]:

$$L = \frac{Z_h \beta \ell}{\omega} = \frac{Z_h \ell}{v_p} \quad \text{for } \ell < \frac{\lambda_g}{12} \quad (4.9)$$

where v_p is the phase velocity of the high-impedance t-line ($v_p = c/\sqrt{\epsilon_{eff}}$, $c = 3 \times 10^8$ m/s is the speed of light). Alternatively, the switch can simply be modeled by the short t-line in a circuit simulator. It is seen that the equivalent series inductance in the down-state position is 30-80 pH for practical designs ($\ell = 60$ -100 μm , $g = 1$ -2 μm). There is an additional equivalent inductance that should be taken into account, especially in microstrip configurations. In this case, the t-line is tapered from 120-250 μm wide to 30-60 μm wide around the switch. This effect should be included in the circuit simulator as varying short sections of high-impedance lines if the down-state reflection coefficient of the switch is to be accurately predicted at 20-60 GHz.



(a)



(b)

Figure 4.6: Simulated t-line parameters of a MEMS series switch suspended $g \mu\text{m}$ above a silicon substrate for (a) microstrip and (b) CPW configurations.

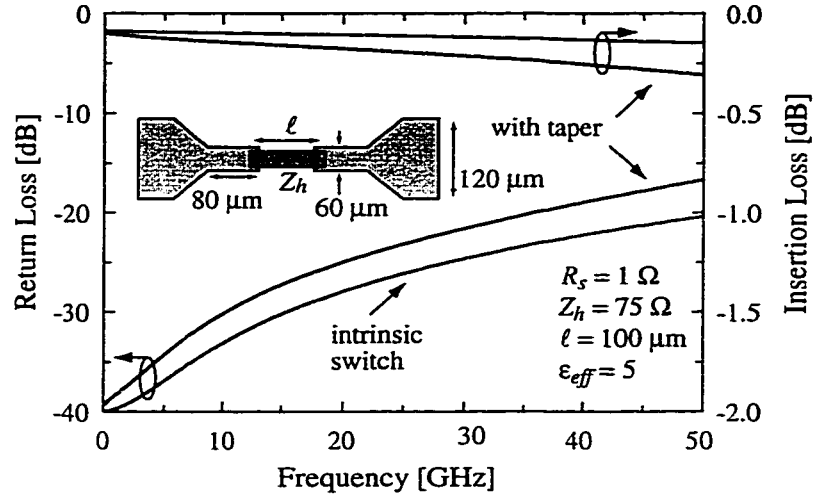


Figure 4.7: Down-state performance of a MEMS series switch on a 150 μm silicon substrate with and without the tapered microstrip sections and associated microstrip line loss.

In the up-state position and for the one-contact switch, the short t-line ($Z_h, \beta\ell$) has little effect on the isolation. It is interesting to note that the short high-impedance t-line does improve the isolation of a two-contact switch. This is detailed in Section 4.3.

Fig. 4.7 shows the down-state performance for a DC-contact series switch with $R_s = 1 \Omega$, $Z_h = 75 \Omega$, $\ell = 100 \mu\text{m}$, and $\epsilon_{eff} = 5$ ($L = 56 \text{ pH}$). The down-state performance of the MEMS switch *alone* results in very low insertion loss and an excellent match up to 50 GHz. The down-state performance changes if a microstrip line loss of 0.2 dB/cm at 10 GHz is assumed (and changing as \sqrt{f} with frequency above 5 GHz), together with a microstrip-line taper as shown in Fig. 4.7. In this case, the reflection loss increases to -16 dB at 50 GHz due to the added inductance from the tapered t-line sections. The switch insertion loss is dominated by the t-line loss and reflection coefficient above 20 GHz.

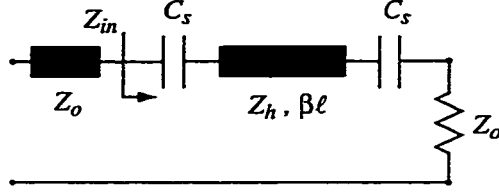


Figure 4.8: Up-state model of a MEMS series switch with two contact points.

4.3 Fitting CLR Parameters to DC-Contact Series Switch Measurements

The CLR values of the MEMS series switch can be extracted from the S-parameter measurements obtained using on-wafer calibration techniques. The TRL calibration technique can be used to define the reference planes on the wafer.

4.3.1 Up-State Capacitance

The series switch is modeled using one or two series capacitors and a high-impedance section of t-line of length ℓ , impedance Z_h and effective dielectric constant ϵ_{eff} (Fig. 4.1, Fig. 4.2). If one neglects the high-impedance t-line between the contact areas, the isolation is calculated as:

$$S_{21} = \frac{2j\omega C_u Z_o}{1 + 2j\omega C_u Z_o} \quad (4.10)$$

where $C_u = C_s/2 + C_p$ for a two-contact switch and $C_u = C_s + C_p$ for a one-contact switch. For $S_{21} \ll -10$ dB and $2\omega C_u Z_o \ll 1$:

$$|S_{21}|^2 \simeq 4\omega^2 C_u^2 Z_o^2 \quad (4.11)$$

Equation 4.11 results in a straight-forward determination of the up-state capacitance from the measured isolation data. This method results in the correct value of C_u for the one-contact switch, i.e, the inline switch of Fig. 4.2. However, neglecting the high-impedance t-line section, even if short, results in erroneous values for C_u for the two-contact switch. This is quite surprising and is explained below.

The exact model of the two-contact switch must take into account the short high-impedance t-line between the two series capacitors (Fig. 4.8). In the up-state position, the

short high-impedance section *cannot* be modeled as a small inductance since it is bounded by two series capacitances each having a very high reactance. The only way to calculate the switch response is to calculate the input impedance of the switch using t-line equations. Neglecting C_p , the calculated impedance at the input port is:

$$Z_{in} = Z_c + Z_h \frac{(Z_o + Z_c) + jZ_h \tan(\beta\ell)}{Z_h + j(Z_o + Z_c) \tan(\beta\ell)} \quad (4.12)$$

where Z_c is the series capacitor impedance ($Z_c = 1/j\omega C_s$). The transmitted power to port 2, or the isolation, can be calculated as:

$$|S_{21}|^2 = 1 - |S_{11}|^2 \quad (4.13)$$

$$|S_{21}|^2 \simeq 4\omega^2 Z_o^2 \frac{(C_s/2)^2}{\left(1 + \frac{\ell}{2Z_h C_s v_p}\right)^2} \quad \text{for } \beta\ell \leq 0.1 \quad (4.14)$$

where v_p is the phase velocity of the high-impedance t-line ($v_p = c/\sqrt{\epsilon_{eff}}$). The high-impedance line actually *improves* the isolation of the series switch, and results in an effective capacitance, C'_u , which is equal to:

$$|S_{21}|^2 = 4\omega^2 C_u'^2 Z_o^2 \quad (4.15)$$

$$C'_u = \frac{(C_s/2)}{\left(1 + \frac{\ell}{2Z_h C_s v_p}\right)} \quad (4.16)$$

Note that C'_u is smaller than $C_s/2$ for all values of C_s . For $C_s = 4$ fF, $\ell = 60$ μm , $Z_h = 75$ Ω , and $\epsilon_{eff} = 5$, the effective capacitance is $C'_u = 0.57(C_s/2)$, and results in an improvement of 4.9 dB in the isolation response over the standard case with $C_u = C_s/2$ (Fig. 4.9). The improvement is independent of frequency up to $\beta\ell = 0.1$ which occurs around 50 GHz for the case outlined above. The improvement is not as high if the parasitic capacitance is taken in the calculation (1.6 dB instead of 4.9 dB for $C_p = 3$ fF).

The effective capacitance, C'_u , can be determined in a straightforward manner using the measured isolation response (or numerical simulations) together with Eq. (4.15). However, the high-impedance t-line characteristics and C_p must be well known if an accurate value of C_s is desired.

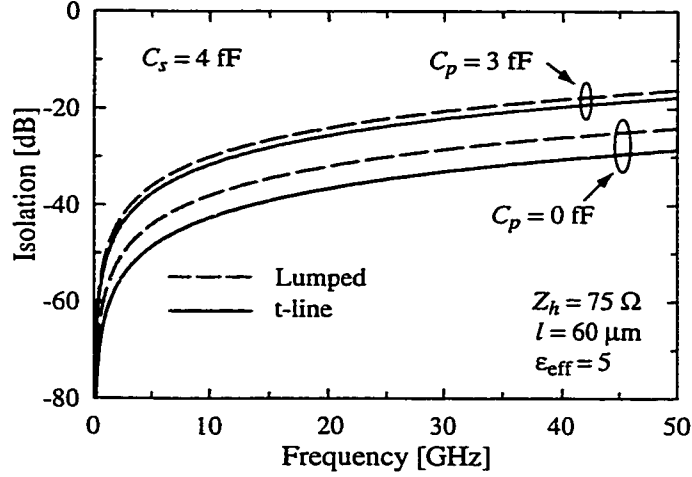


Figure 4.9: Simulated isolation of a two-contact series switch with and without the effect of the short high-impedance t-line.

4.3.2 Down-State Resistance and Inductance

The MEMS switch resistance can be determined from the measured loss in the down-state position and Eq. (4.8). One must be careful to de-embed the reflection loss $(1 - |S_{11}|^2)$ from S_{21} if the intrinsic switch loss is to be determined. Note that in this extraction method, R_s includes the short t-line sections around the switch up to the reference planes. Still, R_s will be dominated by the contact resistance of the switch for most designs.

There is another way to extract R_s . The equivalent series impedance of a DC-contact switch in the down-state position is given by:

$$Z_s = R_s + j\omega L \quad (4.17)$$

and for $Z_s = R_s$, ($\omega L \ll R_s$),

$$|S_{11}|^2 = \left(\frac{R_s}{2Z_0} \right)^2 \quad (4.18)$$

where L is the inductance of the switch in the down-state position. Therefore, it is straightforward to determine R_s from the measured reflection coefficient at low frequencies. This occurs at $f \leq 3$ GHz for $R_s = 2 \Omega$ and $L = 30$ pH. The only problem with this technique is that the reflection coefficient must be accurately known to -34 to -40 dB for $R_s = 1$ - 2Ω .

The down-state inductance of the MEMS switch can also be extracted from the measured

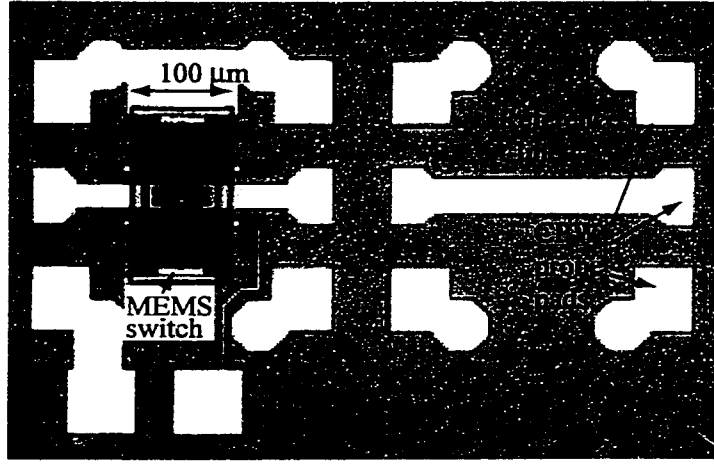


Figure 4.10: Photomicrograph of the RSC series switch and a reference t-line for calibration.

S_{11} values. In this case, the reflection coefficient is fitted to an R/t-line model or an RL model, with the t-line or L controlling the response at mm-wave frequencies. The switch impedance and reflection coefficient are:

$$Z_s = j\omega L \text{ for } \omega L \gg R_s \quad (4.19)$$

$$|S_{11}|^2 = \left(\frac{\omega L}{2Z_o} \right)^2 \quad (4.20)$$

This results in an accurate fitting of the switch inductance if S_{11} measurements are available at 20-50 GHz. Note that this is the total inductance of the switch (up to the reference planes) and includes the t-line taper around the switch.

4.4 Example: The Rockwell Science Center MEMS Series Switch

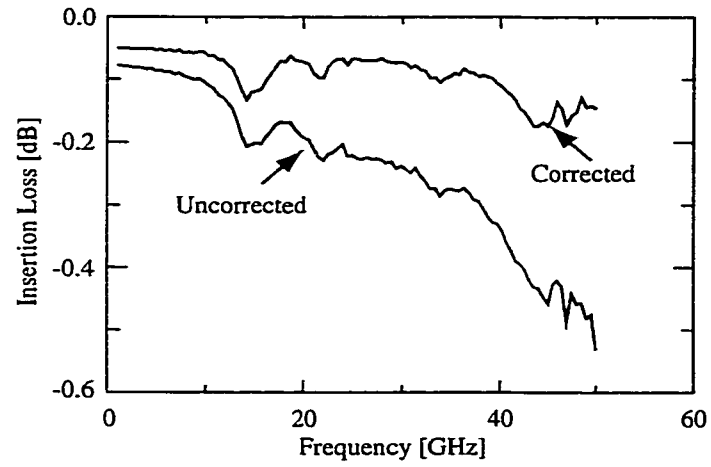
The RSC MEMS series switch and its S-parameter measurements are shown in Figs. 4.10, 4.11. The reader is referred to [16] for the fabrication details of this switch. The measured up-state isolation results in a perfect fit to $C'_u = 1.75$ fF. The measured corrected down-state insertion loss results in a loss of -0.1 dB up to 40 GHz and a switch resistance of 1Ω . The

corrected loss is obtained by subtracting the measured thru-line loss (without the MEMS switch) from the insertion-loss measurements of the switch. The corrected measurements is therefore referenced to the switch contact points, and is solely due to the switch resistance. The measured reflection coefficient is completely dominated by the t-line around the switch (and associated via-holes) and therefore, it is very hard to extract the down-state series inductance of the switch. Still, it is better than -20 dB up to 30 GHz.

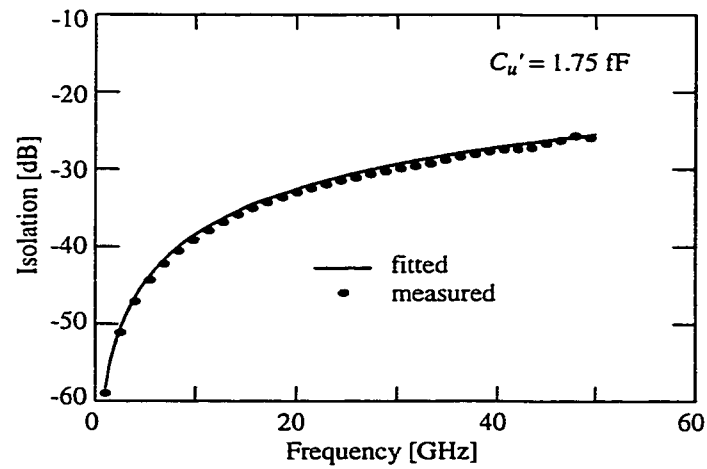
4.5 Fitting CLR Parameters to Capacitive Series Switch Measurements

In the up-state position, the capacitive series switch is identical to the DC-contact series switch, and the analysis of Section 4.3 is also applicable to capacitive series switches.

In the down-state position, it is best to fit the measured S-parameters to a model consisting of a down-state capacitor (or capacitors) in series with a short section of t-line. At RF frequencies ($f < 1$ GHz), the down-state capacitance dominates the switch performance, and results in a poor insertion loss (for $C_d < 4$ pF). The capacitance can therefore be fitted using the measured insertion loss and Eq. (4.16) but with C_u replaced by C_d for a two-contact switch, and using Eq. (4.11) for a one-contact switch. At mm-wave frequencies, both S_{11} and S_{21} should be used to determine the characteristics of the short section of high-impedance t-line.



(a)



(b)

Figure 4.11: Measured (a) down-state and (b) up-state data for the RSC series switch (data obtained from the Rockwell Science Center).

CHAPTER 5

MEMS SERIES SWITCHES AND HIGH ISOLATION SWITCH CIRCUITS

5.1 Introduction

In the previous chapter, we concentrated on the electromagnetic and circuit modeling of MEMS series switches. In the case of DC-contact series switches, the up-state capacitance can be designed to be very low, around 2-5 fF, resulting in high isolation up to 50 GHz. The down-state performance is limited by the metal-to-metal contact resistance of 1.0-1.5 Ω , resulting in an insertion loss of -0.1 to -0.15 dB. Series switches with capacitive contact pads are very similar to DC-contact switches except that they do not operate well below 4 GHz with silicon-nitride dielectrics. The loss of the switch is so low that one must take into account the effect of the surrounding transmission line (taper, etc..) in order to get an accurate model of the switch circuit.

This chapter covers the design of microwave and mm-wave series switches, and also their use in circuits for high-isolation designs. It is seen that one can easily obtain low-loss circuits exhibiting high isolation up to 40 GHz.

5.2 Design of MEMS DC-Contact Series Switches

The design of MEMS series switches is considerably less involved than shunt switches. First, the microstrip and CPW implementations are nearly identical since the microstrip

design does not involve the use of resonant stubs. The only difference is that in the microstrip design, the transmission line must be tapered from 60-250 μm wide (depending on the substrate height) to 30-40 μm wide around the series switch. As discussed in Chapter 4, this results in a small inductance in series with the MEMS switch which could be easily modeled using microwave circuits software (or full-wave numerical methods).

Consider the MEMS switch with capacitance C_u connected in series across a transmission line of impedance Z_o . In the up-state position, the capacitance is so small that the inductance can be neglected, and the isolation is:

$$S_{21} = \frac{2j\omega C_u Z_o}{1 + 2j\omega C_u Z_o} \quad (5.1)$$

and for $S_{21} < -10$ dB and $2\omega C_u Z_o \ll 1$:

$$|S_{21}|^2 = 4\omega^2 C_u^2 Z_o^2 \quad (5.2)$$

The isolation of the switch is determined by the up-state capacitance, and as seen in Chapter ??, this can be made to be quite small (2-5 fF). The reader is referred to Section 4.3 for more detail on the up-state capacitance calculation and the effect of the short high-impedance section of the MEMS switch on the isolation response. Fig. 5.1 shows the isolation vs. the up-state capacitance from 1-100 GHz. For an up-state capacitance of 2-4 fF, the series switch results in an isolation of -57 to -51 dB at 1 GHz, -46 to -40 dB at 4 GHz, -37 to -31 dB at 10 GHz, -27 to -21 dB at 30 GHz and -18 to -12 dB at 90 GHz. This performance is not yet attainable by any solid-state device.

For completion, the reflection loss in the up-state position is:

$$|S_{11}|^2 \simeq 1 - 4\omega^2 C_u^2 Z_o^2 \quad (5.3)$$

and is equal to 1 for all practical purposes.

In the down-state position, the switch model reduces to an LR_s circuit, with R_s given by the contact resistance of the switch, and L is the inductance of the MEMS switch (see Chapter 4 for more detail). The insertion loss is ($\omega L \ll R_s$):

$$S_{21} = 1 - \frac{R_s}{2Z_o} \quad (5.4)$$

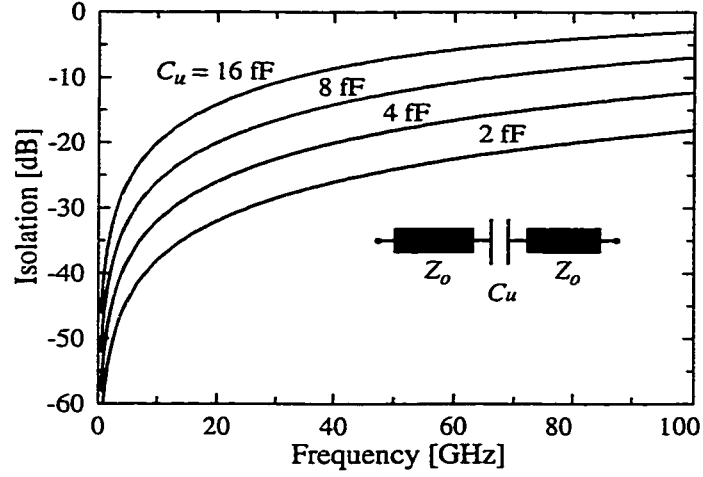


Figure 5.1: Simulated isolation vs. up-state capacitance for a MEMS series switch.

and the switch net loss is $R_s/2Z_o$ (-0.1 to -0.2 dB for $R_s = 1-2 \Omega$). The reflection loss of a DC-contact series switch in the down-state position is discussed in detail in Chapter 4.

The performance of DC-contact series switches is so close to the ideal switch, especially at $f < 40$ GHz, that the only parameter to be designed is the up-state capacitance. It is perfect for wireless applications (1-5 GHz) as a high isolation switch in mobile telephones. For this application, several small contact points can be used to improve the reliability of the DC contact.

In certain cases, a high-isolation series switch is required at 40-90 GHz, and this cannot be achieved even with $C_u = 2$ fF. This can be solved by using two series switches next to each other 5.2. The isolation of two series switches separated by $200 \mu\text{m}$, each with $C_u = 3$ fF, is -45 dB at 40 GHz, -40 dB at 60 GHz and -33 dB at 90 GHz. The insertion loss is -0.2 to -0.3 dB for $R_s = 1-1.5 \Omega$. This is indeed a spectacular performance not attainable by any technology to-date. The same idea can be used for large area, large power series switches. Just cascade two switches to increase the isolation if the up-state capacitance of one switch does not provide the required isolation at the design frequency.

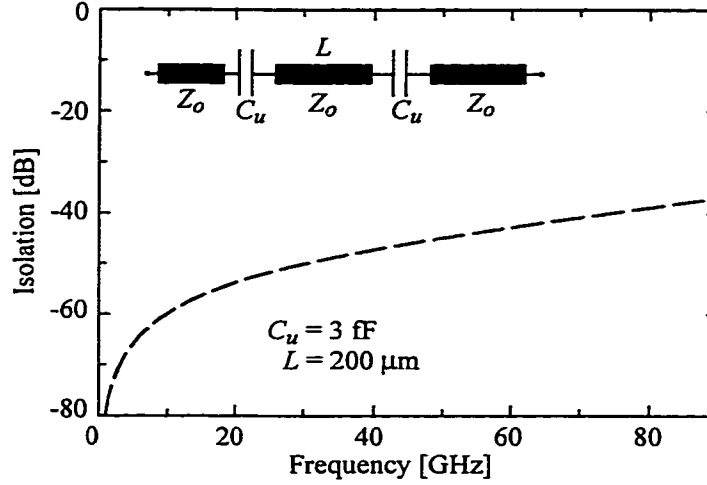


Figure 5.2: Simulated isolation for two 3 fF series switches separated by 200 μm . The isolation is very high up to 90 GHz.

5.3 All-Metal Series Switch

MEMS series switches have been demonstrated from 1-100 GHz for low-loss applications [16, 17]. Most series switches fabricated using a cantilever-based design which is composed of a stress-balanced $\text{Si}_3\text{N}_4/\text{Al}$ or SiO_2/Al beam (or dual beam as in the case of the Rockwell MEMS switch). On the other hand, the inline series switch of Northeastern/Analog Devices is based on a 5-8 μm -thick gold-plated cantilever [18]. This switch has also shown some outstanding performance, but requires a very special gold-plating technique which is very hard to reproduce.

A new all-metal series switch was developed which can offer high isolation at 0.1-30 GHz. The switch is based on a fixed-fixed beam approach, and therefore, is not very sensitive to the residual stress in the supporting beam. The advantage of this switch is that it is easy to fabricate and does not require special processing with dielectric beams or a thick low-stress electroplated cantilever. Also, the fabrication process of the novel series switch is compatible with capacitive (or DC-contact) shunt switches, allowing the construction of a high-isolation DC-40 GHz series/shunt switch.

The all-metal series switch is shown in Fig. 5.3. The series switch is composed of a gold bridge which is suspended 1.5 μm over the microwave t-line, and a 80 μm wide opening is

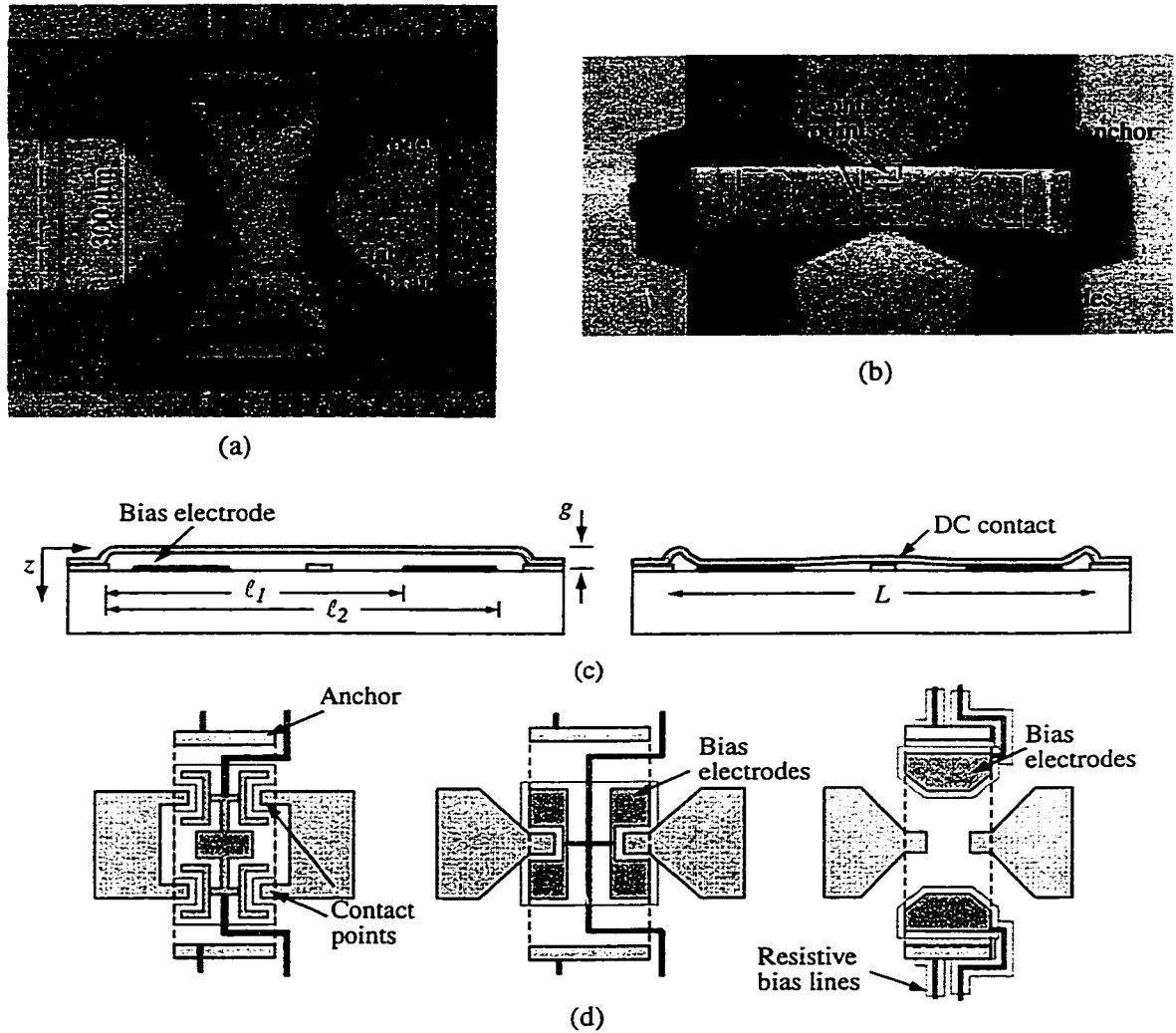


Figure 5.3: Photomicrograph (a) and SEM (b) of the all-metal MEMS series switch, an illustration of the cross section of a MEMS series switch in the up-state, and down-state position (c), and three different pull-down electrode geometries (d).

defined in the t-line. The length of the MEMS bridge is 300 μm and the width depends on the t-line gap. In most cases, the width is around 100-120 μm thus ensuring a 10-20 μm overlap with the t-line. The bridge is anchored at both sides, and in a coplanar waveguide (CPW) implementation, the anchors do not touch the CPW ground planes. The MEMS air bridge is fabricated using a Ti/Au sputter deposition with a total thickness of 9000 Å. Two pull-down electrodes are defined near both anchors of the switch, and are connected to the supply voltage using a resistive bias line. When the switch is pulled down, it makes a metal-to-metal contact with both sides of the t-line, thus achieving DC continuity between the input and output ports. When the switch is in the open position, it offers a low series capacitance and excellent isolation at 0.1-30 GHz. The switch is fabricated using the published techniques described in [7].

The disadvantage of this switch is its higher up-state capacitance, around 6-9 fF instead of 2-4 fF. Also, when the switch is pulled down, it connects two short stubs (150 μm) to the microwave t-line. These stubs have minimal effect on the operation of the switch up to 30 GHz, but do result in an increase in the reflection coefficient of the switch above 40 GHz (down-state). Still, the design shown in Fig. 5.3, with its advantages described above, result in an excellent high-isolation switch from DC-26 GHz.

It is important to note that the all metal series switch is compatible with a microstrip implementation. Actually, it is easier to build since the ground plane is not near the anchors of the bridge, and the bias lines need not be isolated from the ground plane metal using a nitride layer.

Mechanical Modeling: The spring constant of a fixed-fixed beam with off-center electrodes can be derived using the principle of superposition, as the displacement at the center of the beam versus a point force which is applied at a position x' on the beam (Fig. 5.3). This type of analysis is covered by Baker [19] in detail and is applied here to the all-metal series switch geometry in, giving a spring constant:

$$k = \frac{-4t^3wE(\ell_2 - \ell_1)}{L^3(\ell_2 - \ell_1) - 3L^2(\ell_2^2 - \ell_1^2) + 3L(\ell_2^3 - \ell_1^3) - (\ell_2^4 - \ell_1^4)} + \frac{2tw(1 - \nu)\sigma(\ell_2 - \ell_1)}{L(\ell_2 - \ell_1) - \frac{1}{2}(\ell_2^2 - \ell_1^2)} \quad [\text{N/m}] \quad (5.5)$$

for $\ell_2 - \ell_1 \leq L/2$, where L , w , t , ℓ_1 and ℓ_2 are the length, width, thickness of the bridge,

distance from far anchor to start and end of the bias pad, σ is the residual stress in the beam, E is the Young's modulus of the gold membrane and ν is Poisson's ratio. The pull down electrode area is $2(\ell_2 - \ell_1) \times w$. The calculated spring constant in Eq. (5.5) is higher than a center-pulled bridge since more force is required near the anchors to move the bridge in the center. The spring constant of a gold bridge with $L = 300 \mu\text{m}$, $w = 140 \mu\text{m}$, $t = 0.9 \mu\text{m}$, $\ell_1 = 205 \mu\text{m}$, $\ell_2 = 260 \mu\text{m}$ and $\sigma = 10\text{-}30 \text{ MPa}$ is $k = 21\text{-}63 \text{ N/m}$. The pull-down voltage for the case above with a gap height of $1.5 \mu\text{m}$ is $13\text{-}22 \text{ V}$. In general, it is good to use $1.3\text{-}1.6V_p$ for optimal switching performance [20].

In order to ensure that the bridge contacts well the microwave t-line, we have purposely fabricated the t-line around 4000 \AA thicker than the pull-down electrode. Also, as seen in Figure 5.3, different pull-down electrodes were used so as to ensure that an electrostatic force is applied around the center of the bridge.

Electromagnetic Modeling: The switch of Fig. 5.3 was modeled using a full-wave EM simulator (Sonnet). The CPW line dimensions are $G/W/G = 96/160/96 \mu\text{m}$. The opening in the CPW line was defined at $80 \mu\text{m}$. It was found that the up-state capacitance due to the CPW lines alone for an $80 \mu\text{m}$ gap is 5 fF (C_p). The equivalent circuits for a series switch in the up and down-states are shown in Fig. 5.4a,b. The simplified equivalent circuits for the up and down-state are shown in Fig. 5.4c,d. As discussed in Section 4.3, the center transmission line section reduces the effective parallel plate capacitance. The Sonnet simulation of the bridge predicts the total capacitance ($C_t = C_p || C_{ut}$) to be 9 fF . The capacitance is due to the fringing fields (C_p) between the CPW lines and the bridge structure, and the parallel-plate capacitance of the two contact areas in series.

One way to reduce the up-state capacitance is to use a narrow $100 \mu\text{m}$ long center conductor around the switch. This reduces the fringing capacitance to 3.8 fF and the total capacitance to 5.5 fF , at the expense of a larger equivalent series inductance in the t-line. The series inductance increases the reflection coefficient in the down-state position to -20 dB at 26 GHz (Fig. 5.5). This was not done in our design, but is an excellent way of increasing the isolation by 5 dB . Simulations indicate that it is not advantageous to increase the narrow center conductor length to more than $120 \mu\text{m}$ since the isolation will be limited by the CPW gap capacitance and the switch parallel-plate capacitance.

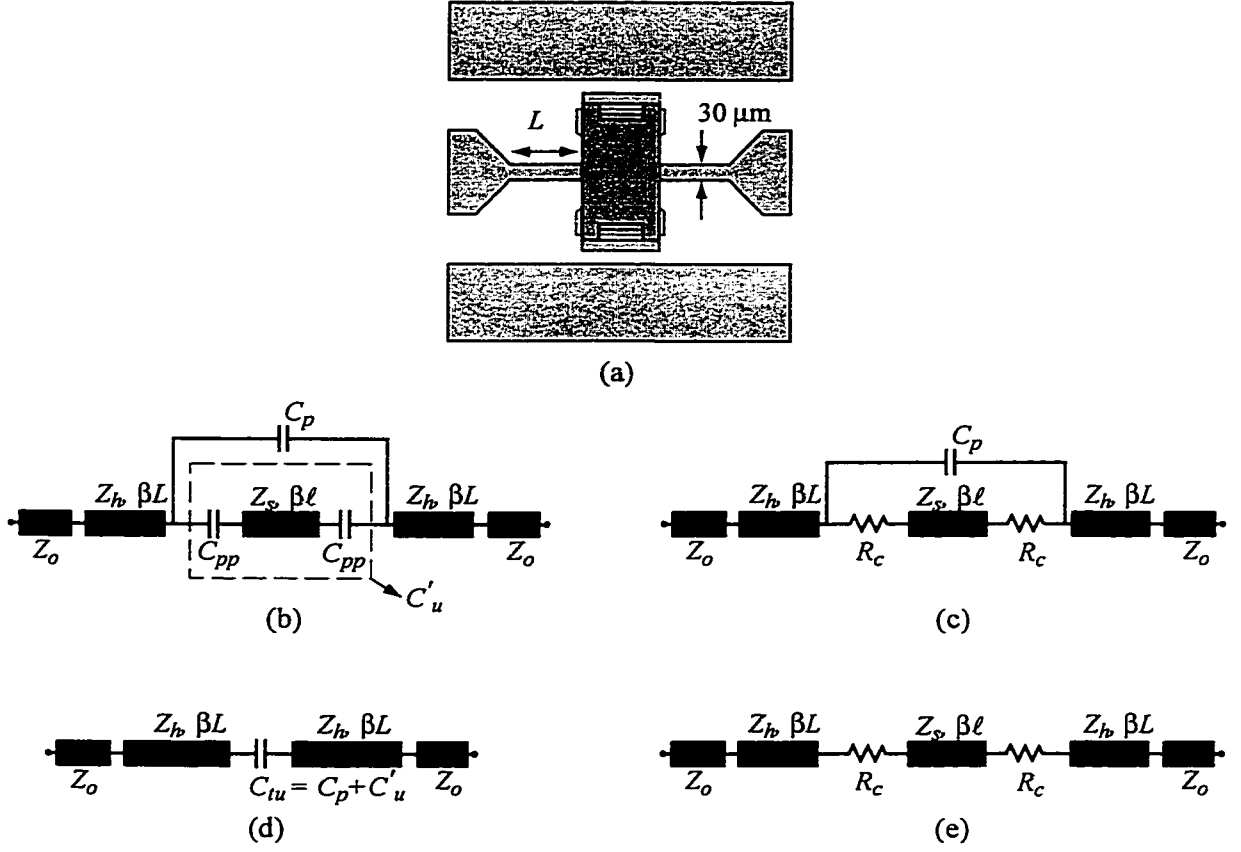
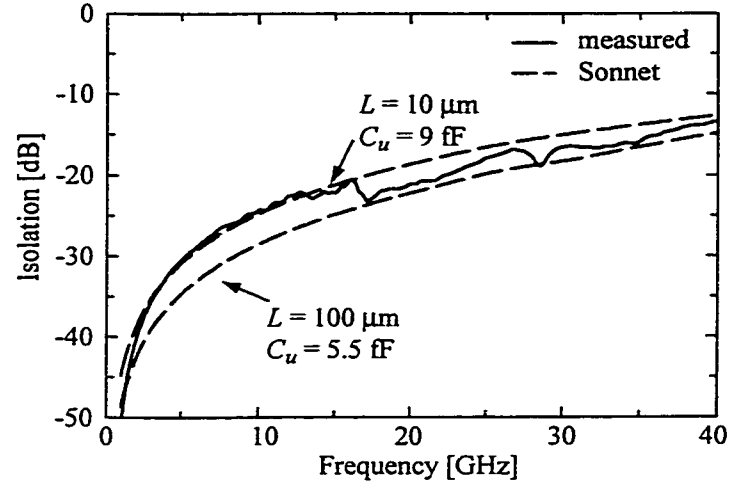
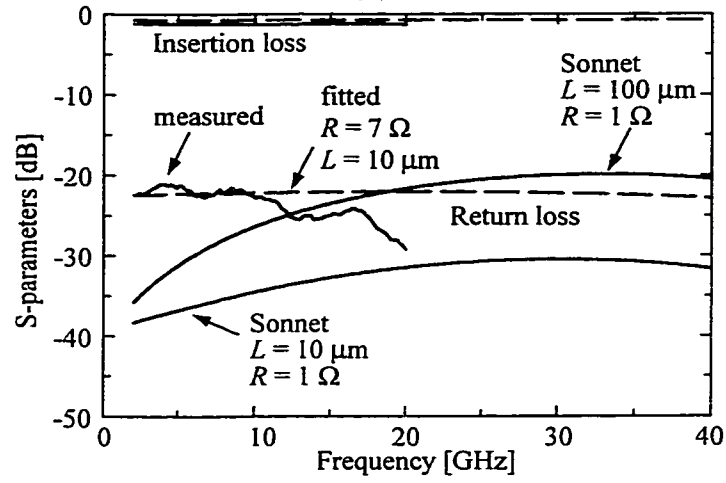


Figure 5.4: Layout (a), equivalent circuits for the all-metal series switch in (b) the up-state position, (c) the down-state position, and (d,e) simplified models for the up and down-states, respectively.

Measurements: The measured response of the switch is shown in Fig. 5.5. The pull-down voltage was around 40 V and an actuation voltage of 45-50 V was applied. The isolation fits well a $C_u = 9\ \text{fF}$ model and we observe small resonances in the isolation at 20 GHz due to the coupling of the anchor of the bridge with the CPW ground plane. The down-state return loss is better than $-20\ \text{dB}$ up to 26 GHz, showing that the $150\ \mu\text{m}$ stubs have virtually no effect below 30 GHz. The insertion loss varied between $-0.5\ \text{dB}$ to $-2.0\ \text{dB}$ depending on the fabrication run, and was independent of frequency up to 26 GHz. We were experiencing problems in the removal of the sacrificial layer and this seriously affected the contact resistance ($3\text{-}5\ \Omega$ per contact). If the switch was fabricated in the down-state position, the measured insertion loss was less than $-0.1\ \text{dB}$ up to 26 GHz, showing that



(a)



(b)

Figure 5.5: Measured and simulated isolation (a) of an all-metal series MEMS switch. Extending the length of the tapered section to $100 \mu\text{m}$ increases the isolation by 5 dB. Measured and simulated S-parameters of an all metal series MEMS switch in the down-state (b). The high contact resistance dominates the measured response.

the measured loss in Fig. 5.5 is due to the contact resistance and not to leakage through the high-resistance bias lines.

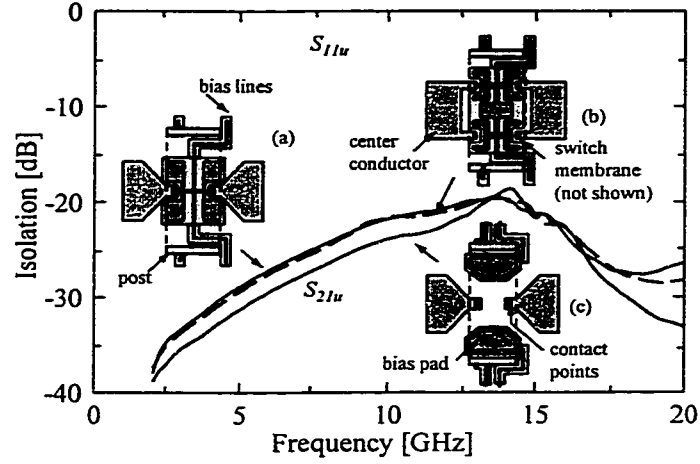


Figure 5.6: Measured S-parameters of an all metal series MEMS switch in the up-state for different pull-down electrode geometries.

The switch was also measured with different electrode geometries (Fig. 5.6). The electrodes are extended to the center of the bridge to result in an additional pull-down force near the contact area. An actuation voltage of 45-50 V was also used for these electrodes. The isolation decreased by only 2 dB from 1-40 GHz, showing that the up-state capacitance increased to 10 fF. This is a small price to pay for a larger contact force. However, due to processing problems, the switch still resulted in the same contact resistance (3-5 Ω).

5.4 Improved All-Metal Series Switch

The electromagnetic modeling presented in Section 4.2 allowed for the modification of the all-metal series switch as shown in Fig. 5.7. The tapered section of t-line leading up to the switch was extended to reduce the parasitic capacitance of the t-line. The switch was rotated 90° to take advantage of the reduction of the effective up-state capacitance with the presence of an intermediate transmission section in the form of the switch membrane (see section 4.3). The switch has meandering springs to help reduce the pull-down voltage and the center of the switch is electroplated to help ensure a flat switch and good DC-contact.

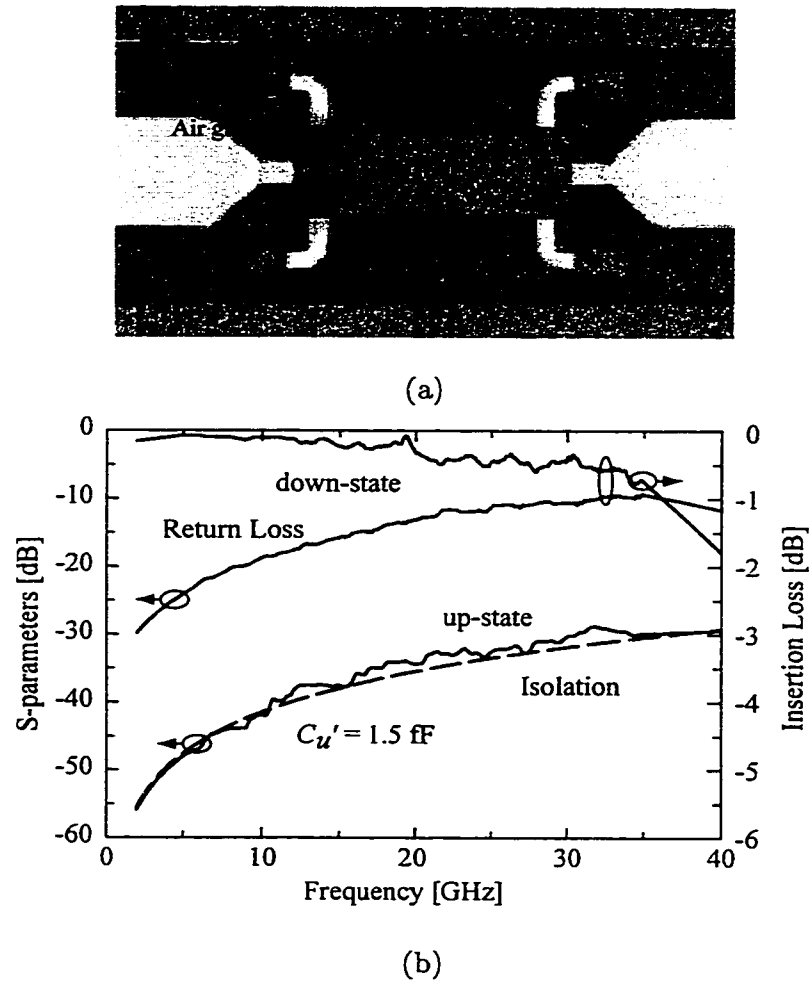


Figure 5.7: Photomicrograph an improved MEMS all-metal series switch (a), and the measure S-parameters in the up-state and down-state positions (b).

The measured isolation is better than -40 dB up to 10 GHz and better than -30 dB up to 40 GHz. The fitted up-state capacitance is 1.5 fF. Due to fabrication problems with the bias lines and the Si_3N_4 layer, the switch could not be pulled down. Therefore, the switch was also fabricated in the down-state position to check the optimal performance of the switch ($R = 0 \Omega$). The measured return loss in the down state position is better than -10 dB up to 40 GHz. A fully-operational switch will be presented in a later paper pending successful fabrication.

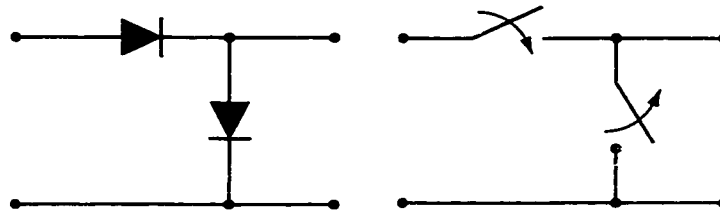


Figure 5.8: Typical series/shunt PIN diode or FET switch circuit.

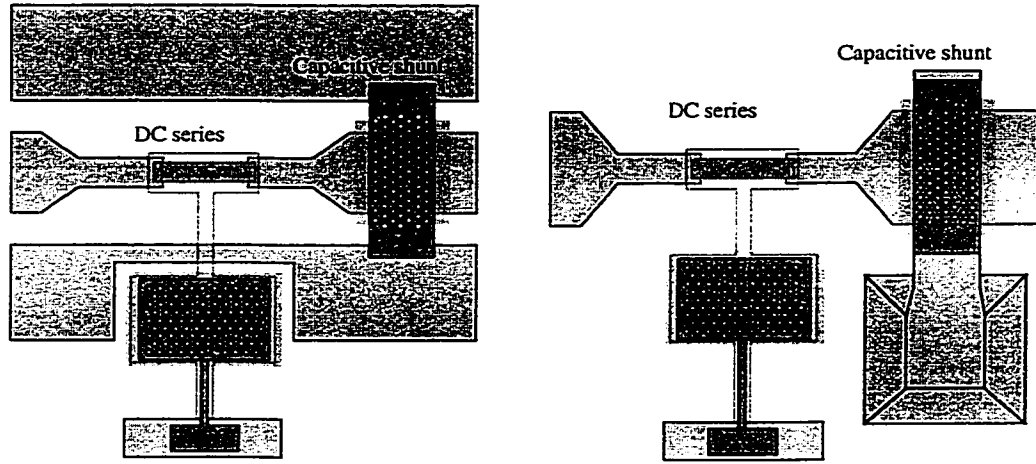
5.5 Design of Series/Shunt MEMS Switches

The workhorse of wideband PIN diode or FET switches is the series/shunt configuration shown in Fig. 5.8. The isolation is provided by the series diode at the lower end of the bandwidth, and by the shunt diode at the high end of the bandwidth. The diodes are biased in a complimentary fashion, that is, when the switch is ON, the series diode is activated while the shunt diode is reverse biased. When the switch is OFF, the series diode is reverse biased and the shunt diode is activated. Using GaAs PIN diodes or FET transistors, it is possible to build DC-26 GHz switches with an isolation of at least -35 to -40 dB over the entire bandwidth, and an insertion loss of -0.5 dB at 1 GHz and -1.5 dB at 26 GHz [21].

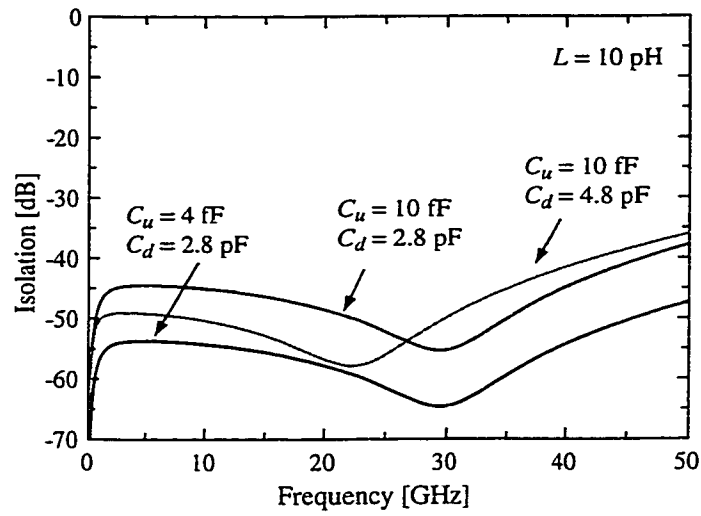
The DC-contact series/capacitive-shunt topology can be easily integrated using MEMS technology. Some standard implementations are shown in Fig. 5.9, and the response for various capacitance combinations (C_u -Series, C_d -Shunt) is shown in Fig. 5.9. It is possible to attain an isolation of -40 to -50 dB with an insertion loss of less than -0.3 to -0.4 dB from DC-50 GHz. The isolation is not sensitive to the t-line length between the series switch and the shunt switch (d_s) since the shunt switch presents a short at high frequencies. The upper frequency of operation is limited by the dimensions of the CPW line, or in the case of a microstrip design, by the thickness of the supporting dielectric substrate and the via-hole inductance. (If a capacitive series switch is used, the lowest frequency of operation will depend on the down-state capacitance except if a DC-contact shunt switch is used).

5.5.1 All-Metal Series/Shunt MEMS Switches

The novel series switch was integrated with a standard CPW capacitive shunt switch to result in a high-isolation series/shunt switch (Fig. 5.10). Both switches are fabricated in



(a)



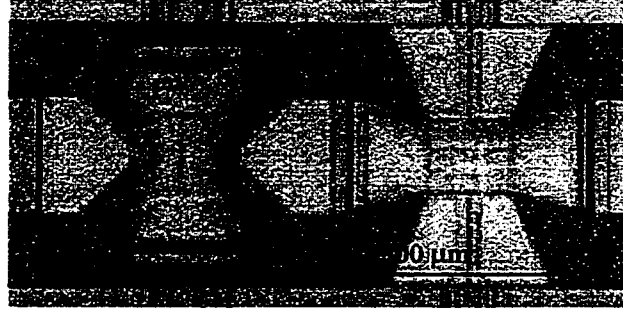
(b)

Figure 5.9: CPW and microstrip implementations of the series/shunt switch (a) and simulated isolation (b) for various values of C_u (series), C_d (shunt).

exactly the same process steps, and the only difference are the anchor connections and bias electrodes. The capacitive shunt switch is $300\text{ }\mu\text{m}$ long, with a width of $100\text{ }\mu\text{m}$ and results in an up-state capacitance of 70 fF and a down-state capacitance of 3.1 pF . The height of the capacitive switch is identical to the series switch ($1.5\text{ }\mu\text{m}$). The pull-down voltage is $18\text{--}22\text{ V}$.



(a)



(b)

Figure 5.10: Photomicrograph of a series/shunt switch with (a) a capacitive shunt switch and (b) a DC-contact shunt switch.

Figure 5.11 shows the measured isolation of the series/shunt switch when the series switch is in the up-state position and the shunt switch is in the down-state position. The isolation is better than -40 dB up to 40 GHz . We believe that the intrinsic isolation of the series/shunt is much better than the measured response, but is limited to -35 dB by radiation in the $96/160/96\text{ }\mu\text{m}$ CPW line, even at 10 GHz . The measured insertion loss of the series/shunt switch in the pass-state (series-down, shunt-up) was again given by the contact resistance of the series switch and was -0.5 to -2 dB depending on the

fabrication run. The measured reflection coefficient in the pass-state was less than -15 dB up to 40 GHz, and is due to the up-state capacitance of the shunt switch ($C_u = 70$ fF). If the series switch is fabricated down, the reflection loss does not change, and the measured insertion loss is less than -0.1 dB up to 20 GHz.

The series switch was also fabricated with an inline DC-contact shunt switch. This shunt switch was published in [22] and will not be repeated here. The only difference in the two designs is the measured isolation at low frequencies. The DC-contact shunt switch results in excellent isolation at DC-5 GHz which adds to the isolation of the series switch. The resulting isolation of the series/shunt switch was better than -60 dB up to 5 GHz. The measured insertion loss and reflection coefficient in the pass-state were very similar to the case of a capacitive shunt switch (Fig. 5.5).

5.6 Design of MEMS Capacitive Series Switches

The design of MEMS capacitive series switches in the up-state position is identical to MEMS DC-contact switches, and result in an isolation given by Eq. (5.2). In the down-state position, the insertion loss is given by:

$$S_{21} = \frac{2j\omega C_d Z_o}{1 + 2j\omega C_d Z_o} \quad (5.6)$$

and for $\omega \gg \frac{1}{2C_d Z_o}$, the insertion loss is equal to 0 dB. In fact:

$$|S_{21}|^2 = \begin{cases} -0.53 \text{ dB} & \text{for } \omega = 4/2C_d Z_o \\ -0.34 \text{ dB} & \text{for } \omega = 5/2C_d Z_o \\ -0.18 \text{ dB} & \text{for } \omega = 7/2C_d Z_o \\ -0.08 \text{ dB} & \text{for } \omega = 10/2C_d Z_o \end{cases} \quad (5.7)$$

For $C_d = 1$ pF, $S_{21} = -0.34$ dB to -0.08 dB at 8-16 GHz. Therefore, capacitive series switches are ideal for X-band frequencies and above. Also, remember that the reduction in S_{21} is solely due to the series capacitance, and this can be tuned with a series inductance to result in an isolation of 0 dB (Fig. 5.12). The price paid is a reduction in the insertion-loss bandwidth. The equations for the match condition for each of the circuits shown in Fig. 5.12

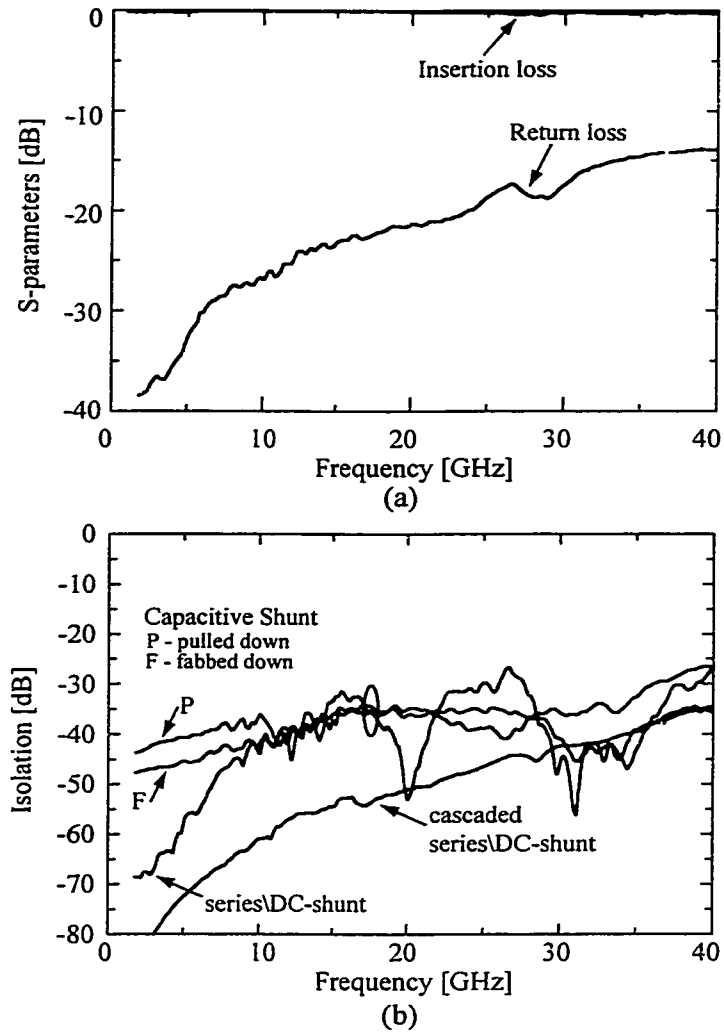


Figure 5.11: Measured S-parameters of several MEMS series/shunt switches in the isolation-state and pass-state. The "cascaded" curve shows the isolation of a measured series and shunt S-parameters cascaded in a circuit simulator. The measured insertion loss is for a series/shunt switch with the series switch fabricated in the down-state position.

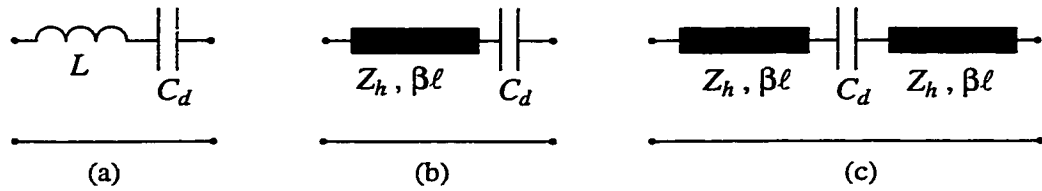


Figure 5.12: Equivalent circuits for inductive matching of series capacitive switches in the down-state.

are ($S_{11} = 0$):

$$L = \frac{1}{\omega^2 C_d} \quad (5.8)$$

for the inductor alone,

$$\tan(\beta\ell) = \frac{Z_h}{\omega C_d (Z_h^2 - Z_o^2)} \quad (5.9)$$

for a single t-line,

$$\tan(\beta\ell) = \frac{Z_h \omega C_d}{Z_o^2} \left[(Z_h^2 - Z_o^2) \pm \sqrt{(Z_h^2 - Z_o^2)^2 - \frac{Z_o^2}{\omega^2 C_d^2}} \right] \quad (5.10)$$

for the double t-line, and this simplifies to:

$$\tan(\beta\ell) \simeq \frac{Z_h}{2\omega C_d (Z_h^2 - Z_o^2)} \quad (5.11)$$

when $Z_h \gg Z_o$ ($Z_h = 80 \Omega$). For the single t-line match of Fig. 5.12b, there is no perfect match solution, but Eq. (5.9) results in minimum reflection loss given by:

$$|S_{11}|^2 \simeq \frac{1}{4\omega^4 C_d^4 (Z_h^2 - Z_o^2)^4} \quad (5.12)$$

For the double t-line match, Eq. (5.10) results in a perfect match as long as the following condition is satisfied:

$$\omega C_d Z_o > \frac{1}{\left(\frac{Z_h}{Z_o}\right)^2 - 1} \quad (5.13)$$

and the minimum down-state capacitances that can be tuned are $C_d = 770$ fF and 340 fF for $Z_h = 65 \Omega$ and 80Ω , respectively, at 6 GHz.

Fig. 5.13 shows the match condition achieved at 6 GHz for $C_d = 1$ pF. The corresponding t-line lengths on silicon are $2490 \mu\text{m}$ and $1580 \mu\text{m}$ for the single section match with $Z_h =$

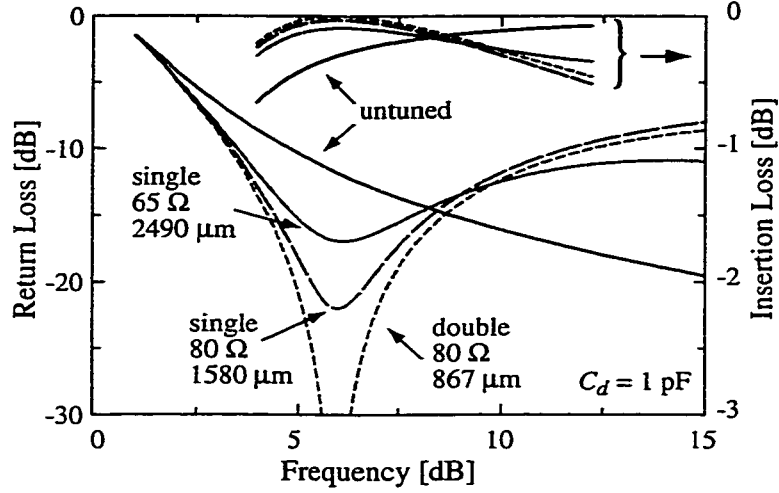


Figure 5.13: Return loss and insertion loss for different inductive matching cases of a series capacitive switch.

65 Ω and 80 Ω , respectively. It is seen that the 65-80 Ω matching section results in 6-12 dB improvement over the non-matched case. The corresponding insertion loss is -0.30 dB for the non-tuned case, and -0.09 dB and -0.03 dB for the 65 Ω and 80 Ω single-section match. The double-section match results in $\ell = 1736$ μm and 867 μm for $Z_h = 65$ Ω and 80 Ω , respectively, and a perfect match at 6 GHz. The inductive match with $L = 700$ pH results in a very similar performance to the double section case with $Z_h = 80$ Ω . Notice that the tuned match results in improved performance (S_{21}) up to 8.5 GHz, and degrades quickly at higher frequencies. The t-line lengths are quite large, even on silicon, and result in an additional loss which is not taken into account in the S_{21} calculations. For low frequencies (1-6 GHz), it is advisable to use lumped high-Q planar inductors. Finally, the inductive matching section have virtually no effect on the up-state performance (isolation) of series capacitive switches.

The isolation of the series capacitive switch can also be written as:

$$S_{21}(\text{dB}) = 20 \log_{10} \left(\frac{5-10}{C_r} \right) \quad (5.14)$$

where the factor (5-10) depends on the choice of the insertion loss in the down-state position ($S_{21} = -0.34$ to -0.08 dB). Equation (5.14) shows that it is hard to obtain a high isolation

with $C_r = 40\text{-}80$. Series capacitive switches therefore result in an isolation of around -20 dB for $C_r = 40\text{-}80$.

The down-state capacitance should be at least 6 pF for an RF capacitive series switch (1-2 GHz operation). It is hard to achieve this capacitance value with a silicon nitride dielectric without the use of a large overlap area, and this will degrade the isolation in the up-state position. For example, for $C_d = 6.4$ pF and $C_r = 80$ ($C_u = 80$ fF), the untuned insertion loss is -0.18 dB at 1.8 GHz with an associated isolation of only -21 dB in the up-state position. Therefore, it is expected that high-dielectric constant materials with $C_r = 100\text{-}500$ will play an important role in RF capacitive series switches. One of the drawbacks of RF capacitive series switches is the relatively low power handling of the series configuration as is discussed in Chapter 6.

CHAPTER 6

MECHANICAL MODELING

6.1 Introduction

Micro-mechanical series and shunt switches have shown some very impressive results (insertion loss and isolation) from 0.1 to 100 GHz [7, 23, 24], and have been employed in low-loss phase shifters at 10 GHz, 35 GHz and 40-100 GHz. The electrical performance of MEMS switches are now well understood. A MEMS DC-contact series switch is accurately modelled by a capacitance in the up-state position, and a resistance in the down-state position. A MEMS shunt capacitive switch is accurately modeled by a capacitance in the up-state position, and a CLR model in the down-state position [7, 25]. The mechanical analysis of MEMS switches has not followed a parallel approach, and the goal of this paper is to introduce a simple 1-D electro-mechanical model which predicts general trends and important parameters of the switching mechanism of RF MEMS switches.

Modeling the full electro-dynamic motion of a MEMS switch during actuation is a complicated task. The strongly coupled interaction of structural deformation with the electrostatic force and the “squeeze film” damping presents many challenges for numerical simulators. Several commercial and research groups have developed software solutions with good success [26, 27]. The limitations of these software packages are manifested in long simulation times, very demanding computational resources, and the inability to couple the RF electromagnetics to the electro-dynamic model. It is for this reason that we present a simple 1-D electro-mechanical model used to efficiently explore switching dynamics, RF

power handling and two-tone RF mixing effects, the effect of the damping Q on switching time, and the effect of resistive-damping and gap stops to result in a reduced impact energy.

6.2 Electro-Mechanical Model of MEMS Switches

The simplest mechanical model for a MEMS switch is the 1-D mass-spring-damper system shown in Fig. 6.1 with the assumption of parallel-plate motion. The lumped mass (m), the stiffness (k), and the damping (b), can be estimated from the modal mass, stiffness, and damping as calculated from analytic solutions [19] or extracted from 3D simulation tools such as Coventor [26], ANSYS [27], and IntelliSuite [28]. The governing equation of motion is given by:

$$mz'' + bz' + kz = F(z, t) \quad (6.1)$$

where the damping coefficient may be a function of gap height ($g = g_o - z$) and velocity, and $F(z, t)$ is the external forcing function due to the electrostatic attraction across parallel plate capacitance. This is a second order system with a resonant frequency of $\omega_o = \sqrt{\frac{k}{m}}$ and a quality factor given by:

$$Q = \frac{k}{\omega_o b} \quad (6.2)$$

The frequency domain solution of equation 6.1 is given by:

$$\frac{X(\omega)}{F(\omega)} = \frac{1}{k} \frac{1}{1 + j\frac{\omega}{Q\omega_o} - \left(\frac{\omega}{\omega_o}\right)^2} \quad (6.3)$$

The frequency response of a switch with $\omega_o = 2\pi 50$ kHz and $Q = 0.2, 1, 5$ is shown in Fig. 6.2, normalized to $\frac{X(0)}{F(0)}$. This is accurate for small displacements with a constant damping (b). Most RF MEMS switches have a resonant frequency of 20-120 kHz, and a quality factor of $0.25 < Q < 4$.

A general expression for the electrostatic forcing function is given by:

$$\begin{aligned} F_e &= -\frac{dU_c}{dz} \\ &= -\frac{1}{2}V_c^2 \frac{dC}{dz} \quad \text{for constant voltage} \\ &= -\frac{1}{2}Q^2 \frac{dC^{-1}}{dz} \quad \text{for constant charge} \end{aligned} \quad (6.4)$$

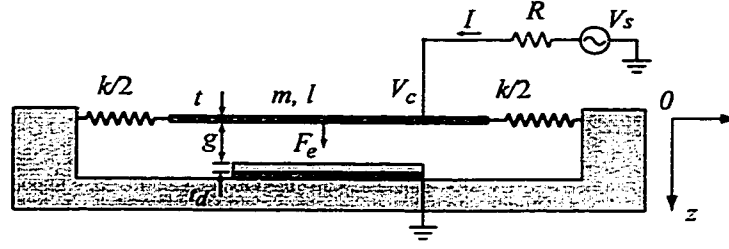


Figure 6.1: Coordinate system and simplified mechanical model of a MEMS fixed-fixed beam switch.

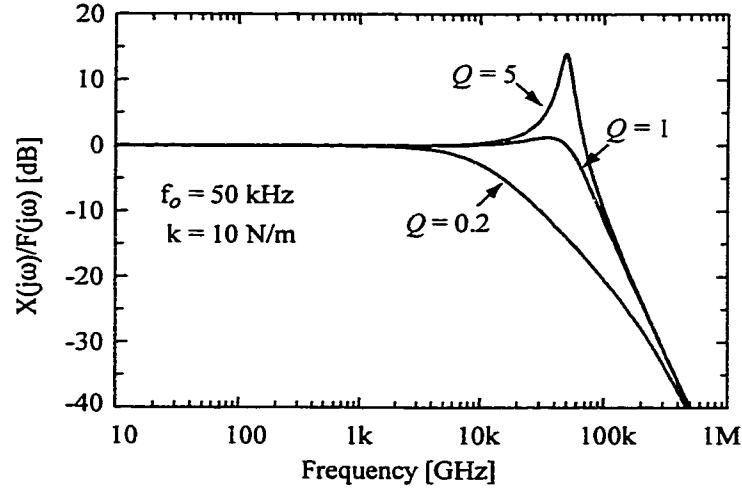


Figure 6.2: Simulated frequency response of a MEMS switch with $\omega_o = 2\pi 50$ kHz and $Q = 0.2, 1, 5$

where the constant voltage case is the most common expression, $i(t)$ is the switching current, and the constant charge case should be used for charge pumped devices. The electrical model, coupled to the mechanical model through the parallel-plate capacitance, results in the following governing equation for the drive voltage:

$$V_c = V_s - i(t)R = V_s - \left(C \frac{dV_c}{dt} + V_c \frac{dC}{dt} \right) R \quad (6.5)$$

where V_s is the source voltage, V_c is the voltage across the parallel-plate capacitance, and R is the bias resistance. Including the bias resistance in the electromechanical model can have some important effects on the total and kinetic energy of the switch at the point of contact [29, 30].

The expression for the parallel plate capacitance including the dielectric layer on the bottom electrode is:

$$C_{pp} = \frac{\epsilon_o A}{g_o + t_d/\epsilon_r - z} = \frac{\epsilon_o A}{g + t_d/\epsilon_r} \quad (6.6)$$

where g_o is the nominal gap height, and t_d is the thickness of the dielectric with a relative dielectric constant ϵ_r . The fringing capacitance (C_f) in the up-state is 20-30% of the parallel plate capacitance for solid beams. The fringing capacitance will be neglected in most of the analysis to follow. However, it will be addressed in one example in Section 6.6.3.

6.3 Static Analysis

Static analysis of the simple mechanical model yields several important parameters such as the pull-down voltage (V_p) and the hold down-voltage (V_h), and estimates of RF power handling of a MEMS switch. For the static analysis, the governing equation becomes:

$$k(g_o - g) = F_e = \frac{dU_c}{dg} \quad (6.7)$$

where $z = g_o - g$. For the case of constant charge and $C = C_{pp}$, equations 6.7, 6.4 and 6.6 yield the following relation for the switch height versus total available charge:

$$g = g_o - \frac{Q^2}{2k\epsilon_o A} \quad (6.8)$$

showing that the height can theoretically be continually adjusted to any fraction of g_o . The charge required to pull the switch to the down-state (Q_s) can be calculated from Equation 6.8:

$$Q_s = \sqrt{2g_o k \epsilon_o A} \quad (6.9)$$

For a switch with $g_o = 2.5 \mu\text{m}$, $A = 100 \times 60 \mu\text{m}^2$, and $k = 10 \text{ N/m}$, Q_s is around 1.6×10^{-12} Coulombs. In practice, it is very difficult to create an ideal charge pump and this method of actuation is not used.

For the case of constant voltage and $C = C_{pp}$, equations 6.7 and 6.6 yield the following relation for the applied voltage versus switch height for static equilibrium:

$$V = \sqrt{\frac{2k(g_o - g)(g + t_d/\epsilon_r)^2}{\epsilon_o A}} \quad (6.10)$$

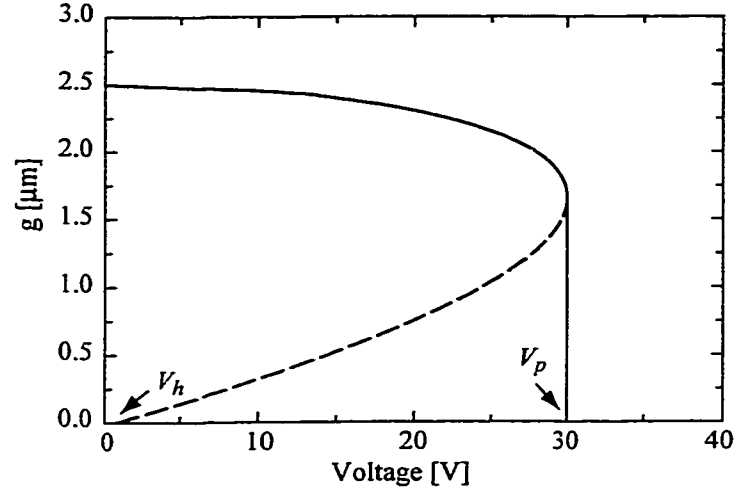


Figure 6.3: Graph of the static voltage height relationship for a MEMS shunt switch with $g_o = 2.5 \mu\text{m}$, $t_d = 0.2 \mu\text{m}$, $\epsilon_r = 7.6$, $k = 10 \text{ N/m}$, and a capacitive area of $100 \times 60 \mu\text{m}^2$ (b).

Starting from $g = g_o$ and slowly increasing the applied voltage, the bridge will follow the curve shown in Fig. 6.3 until it reaches an unstable point at $g = \frac{2}{3}g_o - \frac{t_d}{3\epsilon_r} \simeq \frac{2}{3}g_o$, where the bridge will collapse to the down-state position. The voltage corresponding to the unstable point is called the pull-down voltage (V_p) and is given by:

$$V_p = \sqrt{\frac{8k}{27\epsilon_o A} \left(g_o + \frac{t_d}{\epsilon_r}\right)^3} \quad (6.11)$$

For $g_o = 2.5 \mu\text{m}$, $k = 10 \text{ N/m}$, $t_d = 0.2 \mu\text{m}$, $\epsilon_r = 7.6$, and $A = 100 \times 60 \mu\text{m}^2$ (or $80 \times 80 \mu\text{m}^2$), the pull-down voltage is 30 V.

When the bridge is in the down-state position ($g = 0$), equation 6.10 yields the solution for the hold-down voltage:

$$V_h = \sqrt{\frac{2kg_o(t_d/\epsilon_r)^2}{\epsilon_o A}} \quad (6.12)$$

For $g_o = 2.5 \mu\text{m}$, $k = 10 \text{ N/m}$, $t_d = 0.2 \mu\text{m}$, $\epsilon_r = 7.6$, and $A = 100 \times 60 \mu\text{m}^2$, the hold-down voltage is 0.81 V. The hold-down voltage can be expressed in terms of the pull-down voltage:

$$V_h = \frac{\sqrt{27}}{2} \frac{t_d}{g_o \epsilon_r} V_p \quad (6.13)$$

There are some series switch designs where there is a stable gap of g in the down-state position. In this case, the hold-down voltage is given by Eq. 6.10 and is shown in Fig. 6.3

(dashed curve) for the switch parameters given above. For $g = 0.5 \mu\text{m}$, the hold-down voltage is 14.5 V.

6.4 Limit Expressions for Switching Time

The switching time is another important parameter for MEMS switches. A closed form expression for the switching time for an acceleration limited case (AL) is derived using the Newtonian dynamic equation of motion and neglecting the damping underneath the MEMS switch or cantilever (see Barker [19]). Also, the applied force is assumed to be constant and is given by the electrostatic force due to a voltage V on the MEMS bridge, and is:

$$F_e = \frac{1}{2} \frac{\epsilon_o w W V^2}{g_o^2} \quad (6.14)$$

The dynamic equation of motion becomes:

$$m \frac{d^2 z}{dt^2} + kz = F_e = \frac{1}{2} \frac{\epsilon_o w W V^2}{g_o^2} \quad (6.15)$$

where m is the mass of the bridge (or modal mass), and z is the displacement from the up-state position. The initial conditions are $z = 0$ and $dz/dt = 0$ at $t = 0$ (switch is at rest), and the switching time is calculated for $z = g_o$, and is [19]:

$$t_s = \frac{V_p}{\omega_o V_s} \sqrt{\frac{27}{2}} \quad (6.16)$$

where $\omega_o = \sqrt{\frac{k}{m}}$ is the mechanical resonant frequency of the bridge, V_s is the source (applied) voltage, and V_p is the pull-down voltage given in Equation 6.11. The switching time is dependent on the applied voltage. The higher the applied voltage, the faster the switch. This analysis is accurate if the applied voltage is larger than $1.4V_p$ and the system has low viscous damping ($Q > 1$).

If the system is damping limited (DL), then a similar equation can be derived, as was done by Castaner and Senturia [30, 31] with the assumption of constant damping with gap height, and neglecting the acceleration and spring component. The equation of motion becomes:

$$b \frac{dz}{dt} = F_e \quad (6.17)$$

and can be solved with integral or estimated with difference methods. The solution using integral methods and $F_e = \frac{1}{2} \frac{\epsilon_o w W V^2}{g^2}$ gives the following estimate:

$$t_s = \frac{2bg_o^3}{3\epsilon_o AV_s^2} \simeq \frac{9V_p^2}{4\omega_o Q V_s^2} \quad \text{for } V_s \gg V_p \quad (6.18)$$

Another estimate can be made by assuming a constant F_e (Eq. 6.14) and a constant velocity approximation ($\frac{dx}{dt} = \frac{g_o}{t_s}$). This switching time estimate is given by:

$$t_s = \frac{2bg_o^3}{\epsilon_o AV_s^2} \simeq \frac{27V_p^2}{4\omega_o Q V_s^2} \quad \text{for } V_s \gg V_p \quad (6.19)$$

For the damping limited case, equation 6.19 tends to over-estimate the switching time and equation 6.18 tends to underestimate the switching time.

The time that it takes a switch to release from the down-state is strongly dependant on the damping coefficient. Without damping, the switch would oscillate at its natural resonant frequency for an indefinite period of time. It is for this reason that RF MEMS switches that do not have a latch mechanism in the up-state position will always require a system Q near 1, and therefore an gaseous environment near atmospheric pressures.

6.5 Details of the Viscous Damping Mechanism

The viscous damping of MEMS devices has been studied extensively for small displacement [32, 33, 34, 35, 36, 37]. The effect of holes on the damping coefficient has also been studied [38, 36]. Because the application areas have been accelerometers and condenser microphones, large displacement effects have not been as thoroughly studied. However, Sadd et al. [39] and Veijola et al. [35] have proposed the inclusion of multiplicative displacement functions to account for changes in the damping and viscosity of a squeeze film versus gap height, respectively. A short review of squeeze film damping effects follows.

Squeeze Film Effects: The effects of squeeze film damping can be easily experienced in everyday life with the clap of a hand or the motion of a sheet of paper dropped onto a desk. All of the air that was underneath the sheet of paper must flow to the edges. Because the air is made up of individual gas particles which undergo many collisions with other particles (viscous flow) and the sheet of paper while making their way to the edge,

the random collisions with the sheet of paper result in a force that resists the down-ward motion of the paper. Instead of sheets of paper, MEMS research has been done on viscous flow between parallel plates.

When the gap height between the plates changes very quickly, not all of the air has time to escape without compression and the gas-film stores kinetic energy, acting more like a spring than a damper. A non-dimensional squeeze number can be defined for a given flow geometry and can be thought of as the ratio of flow velocity that ensures no compression to the achievable viscous flow velocity. For a rectangular parallel plate the squeeze number is given by [32]:

$$\sigma = \frac{12\mu d^2 \omega}{P_a g^2} \quad (6.20)$$

where d is the characteristic width of the plate, ω is the frequency of an oscillating plate and P_a is the ambient pressure. When holes are present in the plate, d can be interpreted as approximately twice the average escape distance for the film. At low squeeze numbers, the air flows from the gap without compression and the viscous damping is the dominant effect. When the squeeze number is high ($\sigma > 15$), the air-film is compressed as it flows from the gap and the “air spring” effect is dominant [33]. For STP and $\omega = 2\pi 100$ kHz, a 100 μm -square plate without holes has a squeeze number below 50 until a $g = 0.5$ μm . The same plate with holes spaced at 10 μm apart has a squeeze number below 15 until $g = 0.1$ μm . Since well designed MEMS switches have holes, neglecting the “air-spring” effect can be justified.

Viscosity Variation vs. Height: When examining large displacement effects in squeeze-film damping, the average distance between collisions, called the mean free path (λ), becomes important and is given by:

$$\lambda = \frac{1}{\sqrt{2}\pi N \sigma_x^2} \quad (6.21)$$

where N is the number density and σ_x is the scattering cross-section of the particles. The mean free path of air at STP is approximately 0.1 μm . The ratio of the gap height to the mean free path is called the Knudsen’s Number ($K_n = \lambda/g$). For small K_n , particle-particle interactions dominate resulting in viscous flow. When the gap height is on the order of the mean free-path (large K_n), particle-wall interactions become important, reducing the flow

resistance, or viscosity (μ), thru a “slip-effect” were particles can have fewer interactions before escaping. The viscosity of an ideal gas is given as:

$$\mu = 1.2566 \times 10^{-6} \sqrt{T} \left(1 + \frac{\beta}{T}\right)^{-1} \quad (6.22)$$

where $\beta = 110.33 \text{ K}$ and T is in Kelvin. At STP, equation 6.22 results in $\mu = 1.845 \times 10^{-5} \text{ kg/ms}$. A relation for the viscosity as a function of the gap height, or equivalently K_n , is given by Veijola et al. [35]. This equation takes into consideration the “slip-effect” discussed above, and is:

$$\mu_e = \frac{\mu}{(1 + 9.638 K_n)^{1.159}} \quad (6.23)$$

Damping Variation vs. Height: The damping coefficient for a rectangular parallel-plate geometries has been derived from a linearized form of the compressible Reynolds gas-film equation [32, 33]:

$$b = \frac{3}{2\pi} \frac{\mu A^2}{g_o^3} \quad (6.24)$$

The damping is seen to be a strong function of the nominal gap height g_o . To correct this equation for large displacements, Sadd and Stiffler [39] proposed the following multiplicative displacement function:

$$f_d = \left(1 - \left(\frac{g_o - g}{g_o}\right)^2\right)^{-\frac{3}{2}} \quad (6.25)$$

Combining equations 6.23, 6.24, and 6.25 yields the large displacement-compensated equation for the damping coefficient. The corresponding Q ($Q = \frac{k}{\omega_o b}$) is:

$$Q_e = Q_o \left(1 - \left(\frac{g_o - g}{g_o}\right)^2\right)^{\frac{3}{2}} \left(1 + 9.638 \left(\frac{\lambda}{g}\right)\right)^{1.159} \quad (6.26)$$

where Q_o is the nominal small displacement quality factor of the MEMS switch at $g = g_o$. This displacement compensated equation can now be incorporated in the the non-linear electro-mechanical model of Section 6.2. It will be shown that equation 6.26 has only a small effect on the calculation of the pull-down switching time, but has a much greater effect on the release time.

6.6 Numerical Simulations of the Switching Mechanics

The equations governing the simple 1-D nonlinear model described in the previous sections can be readily solved with a non-linear simultaneous differential equation solver such as Mathematica [40]. The voltage waveform V_s can be an arbitrary continuous function of time to allow investigation of phenomena such as pull-down, release, power handling, intermodulation, and source noise effects.

The equations governing the 1-D model are summarized as:

$$mz'' + bz' + kz = \frac{1}{2} \frac{\epsilon_o w W V^2}{\left(g_o + \frac{t_d}{\epsilon_r} - z\right)^2} + F_c \quad (6.27)$$

$$V_c = V_s - i(t)R = V_s - \left(C \frac{dV_c}{dt} + V_c \frac{dC}{dt}\right) R \quad (6.28)$$

$$C_{pp} = \frac{\epsilon_o A}{g_o + t_d/\epsilon_r - z} \quad (6.29)$$

$$b = \frac{k}{\omega_o Q} \quad \omega_o = \sqrt{\frac{k}{m}} \quad (6.30)$$

$$Q = Q_o \quad \text{Constant Damping} \quad (6.31)$$

$$Q = Q_o \left(1 - \left(\frac{g_o - g}{g_o}\right)^2\right)^{\frac{3}{2}} \left(1 + 9.638 \left(\frac{\lambda}{g}\right)\right)^{1.159} \quad \text{Variable Damping} \quad (6.32)$$

$$g = g_o - z \quad (6.33)$$

$$F_c = \frac{k_1 A}{(g_o - z)^3} - \frac{k_2 A}{(g_o - z)^{10}} \quad (6.34)$$

where F_c represents the attractive Van der Waals forces (first component) and the repulsive nuclear contact forces (second component) between the metal and dielectric layers [41, 42]. The constants $k_1 = 10^{-80}$ Nm determines the surface energy due to the Van der Waals attraction and $k_2 = 10^{-75}$ Nm⁸ determines the equilibrium distance from the surface, in this case 75 Å. These numbers are a strong function of the micro-structure of the surface and were chosen here to allow easy convergence of the numerical simulations. In general, surface interactions are very complex and cannot be modeled well by lumped 1-D models such as the one presented here.

For convenience, we will choose the following switch parameters for all of our simulations: $t_d = 0.2 \mu\text{m}$, $t = 0.8 \mu\text{m}$, $w = 60 \mu\text{m}$, $W = 100 \mu\text{m}$, $l = 300 \mu\text{m}$, $k = 10 \text{ N/m}$, $m = \frac{1}{2}\rho t w l$, $g_o = 2.5 \mu\text{m}$, $V_p = 30 \text{ V}$, and changing only Q and the switch metal (m). The mass is taken to be half of the total mass of the bridge to account for the holes and the modal effects on the bridge (or cantilever). The up-state capacitance is 21 fF (no fringing) and the down-state capacitance is 1.6 pF (75 Å air gap). The above equations are programmed using Mathematica v4 [40], and can be solved in less than 1 minute on an 800 MHz Pentium III processor based PC.

This simple 1-D nonlinear model is valid for fixed-fixed beam and cantilever switches. It is intended to give an estimate of the switch operation and to study the trends in the switching mechanism. Also, the analysis is used to investigate ways to reduce the impact energy of the switch. For series switches, the analysis applies mostly to the pull-down electrode and not the metal-to-metal contact. Still, the velocity, acceleration, and impact energy of the contact can be extracted from the motion of the pull-down electrode.

6.6.1 Switching Time

The switching time for a MEMS switch is composed two parts: the pull-down time and the release time, with the latter dominating. Figure 6.4 presents the time-domain pull-down solution for constant damping (CD) and variable damping (VD) of a MEMS gold bridge with $V_s = 40$ and 60 V , and $Q = 0.5$ and 1 . The solution is valid until contact is achieved, and this is for $g = 0$ (or $z = g_o$). The dynamic motion can be separated into three distinct regions. As the voltage is first applied, the motion is momentum or acceleration limited ($0 < t < 3 \mu\text{s}$, $2.5 < g < 2.4 \mu\text{m}$). As the velocity increases, the viscous damping becomes the dominant term and the velocity becomes constant (see equation 6.18). At around 1/3 of the original gap height, the electrostatic forces become much larger than any of the other forces, and the switch slams to the down-state position.

It is seen that the total pull-down time is dominated by the upper-2/3 damping-limited region ($2.3 < g < 0.8 \mu\text{m}$), especially when V_s is only slightly larger than V_p . Since most of the change in the quality factor for the variable damping case occurs in the lower 1/3 region

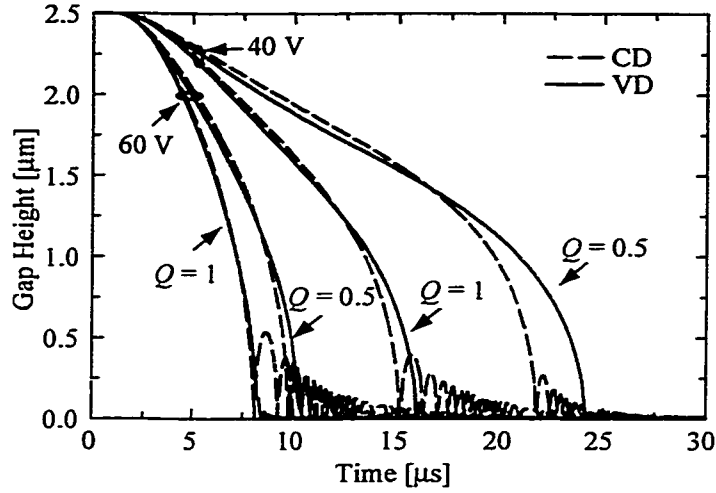


Figure 6.4: Simulated pull-down comparing the effect of displacement compensated damping (VD) and constant damping (CD) for the MEMS gold switch described in Section 6.6 for different V_s and Q .

of the switch, there is only a slight difference between the calculated pull-down times for the two damping cases (see Table 6.1), with the largest difference occurring for low quality factors and low applied voltages.

Figure 6.5 presents the time-domain release solution for CD and VD of a MEMS gold bridge with $Q = 0.5, 1$. The initial restoring force is $kg_o = 25 \mu\text{N}$. The release time is defined as the time it takes the switch to settle to within $\pm 5\%$ of the original gap height. The effect of variable damping is much greater for the calculation of the release time and

Q	V_s/V_p	Gold		Aluminum
		CD [μs]	VD [μs]	VD [μs]
1	1.2	20.6	22.4	7.5
1	1.3	14.1	14.9	6.9
1	1.7	9.3	9.6	3.5
1	2.0	7.1	7.3	2.7
0.5	1.2	34.0	40.1	12.4
0.5	1.3	8.7	9.3	9.3
0.5	1.7	12.2	13.1	4.9
0.5	2.0	8.7	9.3	3.4

Table 6.1: Comparison of pull-down times for variable damping (VD) and constant damping (CD) of a gold MEMS switch described in Section 6.6.

is summarized in Table 6.2. Since the variable damping is greatest when the switch is just releasing from the dielectric, and the restoring force from the spring is linear with displacement (unlike the electrostatic force), the largest effect on the switch motion is seen in the lower 1/3 of the release cycle.

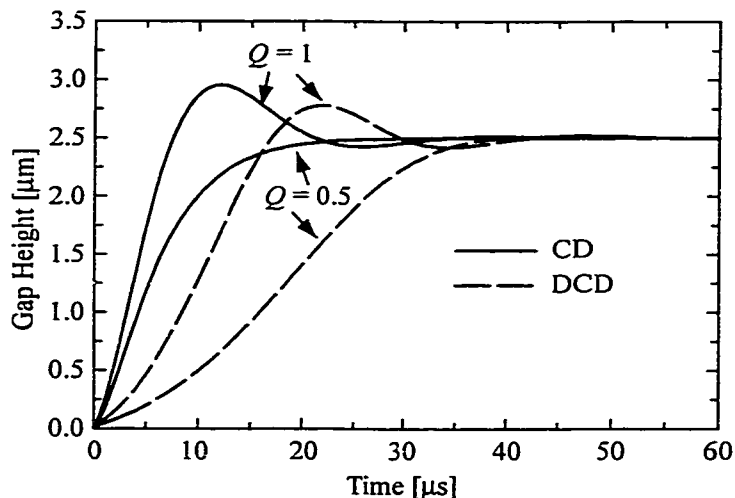


Figure 6.5: Simulated release comparing the effect of displacement compensated damping (DCD) and constant damping (CD) for the MEMS gold switch described in Section 6.6.

It is expected that an aluminum switch will be much faster since its mass is approximately $7\times$ smaller than a gold switch. The results for an aluminum bridge with identical mechanical properties as above are also presented in Tables 6.1 and 6.2. The mechanical natural resonant frequency of the aluminum switch is 114 kHz.

Q	Gold		Aluminum	
	CD [μ s]	VD [μ s]	CD [μ s]	VD [μ s]
0.5	16	32	5.7	12.5
1	19	27	6.7	10.2
2	46	52	14.5	16.4

Table 6.2: Comparison of release times for variable damping (VD) and constant damping (CD) of a gold MEMS switch described above.

The non-linear simulations can also be used to check the validity of the acceleration-limited (AL) and damping-limited (DL) closed-form expressions for the switching time (Eq.6.18-6.19). For the gold switch outlined above, the simulated and closed-form expres-

sions are compared for different Q in Fig. 6.6 and Table 6.3. It is seen that the AL case results in an excellent estimate for the switching time for $V_s/V_p > 1.4$ and $Q > 1$. However, the DL case with equations 6.18 and 6.19 results in coarse bounding-estimates of the switching time for $Q < 0.5$. The same applies for an aluminum switch.

Q	V_s/V_p	VD [μ s]	DL ₁ [μ s]	DL ₂ [μ s]
0.2	1.2	78.5	29	87
0.2	1.5	35.1	19	56
0.2	2.0	17.1	10	31
0.5	1.2	33.5	12	35
0.5	1.5	16.5	7.5	22
0.5	2.0	9.1	4	12

Table 6.3: Comparison of pull-down times for variable damping (VD) and damping-limited (DL₁ and DL₂) estimates of a gold MEMS switch described in Section 6.6 (DL₁ is Eq. 6.18 and DL₂ is Eq. 6.19).

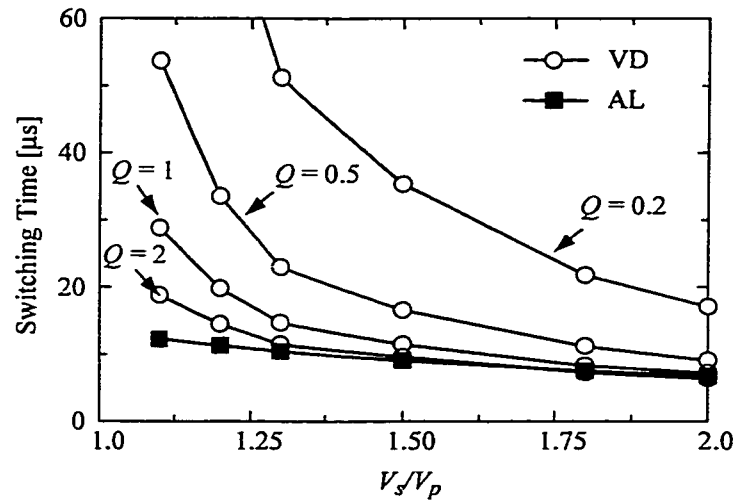
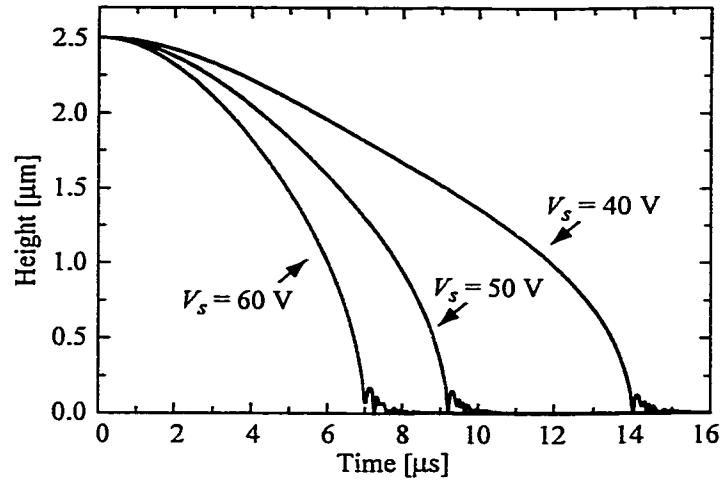
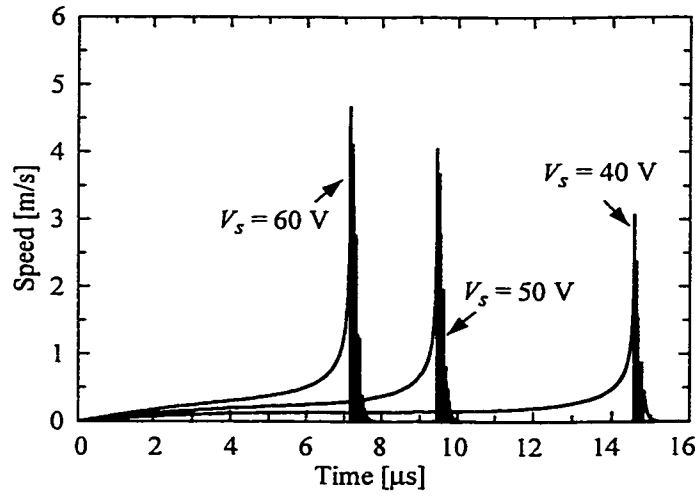


Figure 6.6: Comparison of pull-down times for variable damping (VD) and acceleration limited (AL) estimates for the MEMS gold switch described in Section 6.6.



(a)



(b)

Figure 6.7: Simulated pull-down (a) and velocity (b) for a gold MEMS switch with $g_o = 2.5 \mu\text{m}$, $Q = 1$, $k = 10 \text{ N/m}$, $f_o = 43 \text{ kHz}$, $V_p = 30 \text{ V}$ and a capacitive area of $100 \times 60 \mu\text{m}^2$ (b).

6.6.2 Switching Velocity, Acceleration, Current, and Energy

The solution of the MEMS bridge position versus time can be used to extract the switching velocity and current. The switching current is given by:

$$i(t) = \frac{dq}{dt} = C \frac{dV}{dt} + V \frac{dC}{dt} \quad (6.35)$$

The switching height and velocity versus time are given in Figure 6.7 for the switch de-

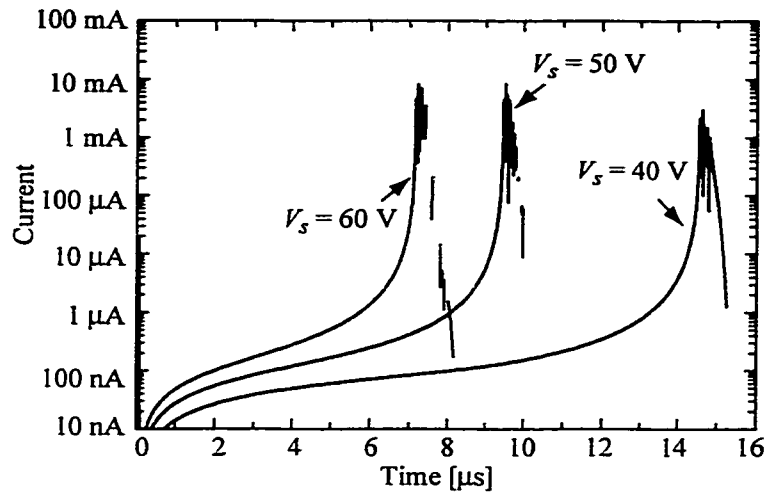


Figure 6.8: Simulated current for a gold MEMS switch with $g_o = 2.5 \mu\text{m}$, $Q = 1$, $k = 10 \text{ N/m}$, $f_o = 43 \text{ kHz}$, $V_p = 30 \text{ V}$, and a capacitive area of $100 \times 60 \mu\text{m}^2$.

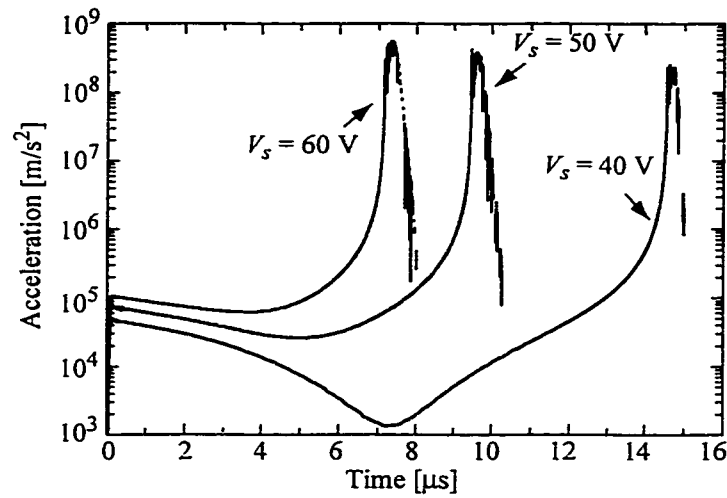


Figure 6.9: Simulated acceleration for a gold MEMS switch with $g_o = 2.5 \mu\text{m}$, $Q = 1$, $k = 10 \text{ N/m}$, $f_o = 43 \text{ kHz}$, $V_p = 30 \text{ V}$, and a capacitive area of $100 \times 60 \mu\text{m}^2$.

scribed above with $R = 0 \Omega$. The switch undergoes an initial acceleration and then quickly reaches a “damping-limited” velocity for most of the switch cycle. Near the end of the switch cycle the bridge accelerates very quickly as the electrostatic forces become much greater than the damping forces. Notice that the peak switching current occurs just near the end

of the switching cycle where the bridge speed is the highest and the capacitance is changing rapidly, and is 3-8 mA for $V_s = 40-60$ V, which is quite significant for low-power and low-current systems (Fig. 6.8). The bridge speed is 3-5 m/s near the point of impact, which translates to 11-18 km/hr. This is indeed very impressive for a bridge which moves only $2.5 \mu\text{m}$.

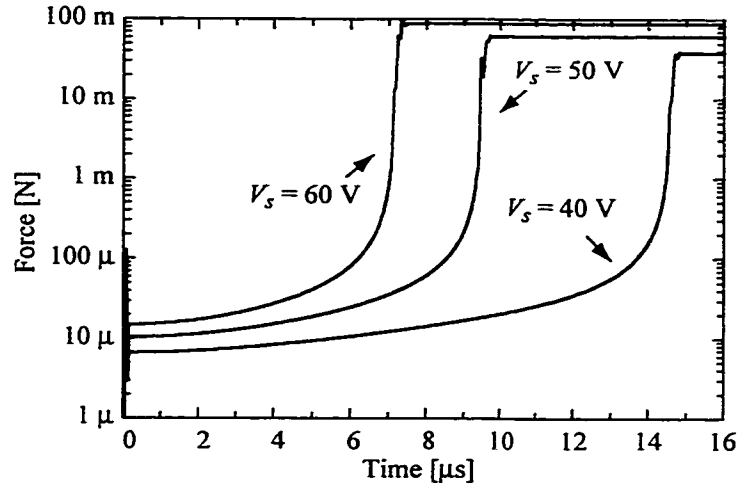


Figure 6.10: Simulated electric force for a gold MEMS switch with $g_o = 2.5 \mu\text{m}$, $Q = 1$, $k = 10 \text{ N/m}$, $f_o = 43 \text{ kHz}$, $V_p = 30 \text{ V}$, and a capacitive area of $100 \times 60 \mu\text{m}^2$.

Figure 6.9 shows the acceleration for the switch describe above. In the first part of the switching cycle, the switch quickly develops an acceleration near 10^5 m/s^2 or 10,000g, where g where $g = 9.8 \text{ m/s}^2$ is the gravitational acceleration constant. The acceleration drops in the damping limited part of the switching cycle, but reaches $5 \times 10^8 \text{ m/s}^2$ near the point of impact. The high acceleration is due to the electrostatic force on the switch which becomes very high as the gap approaches $0 \mu\text{m}$ (Fig. 6.10). This has a direct effect on the impact energy and reliability of the switch.

Switching Energy: The energy consumed in the switching process can be calculated as the sum of the electric and mechanical energy in the MEMS bridge. The mechanical energy is the energy stored in the bridge spring and is given by $E_m = kg^2/2$. The electrical energy is the energy stored in the MEMS capacitor, and is $E_e = C_d V_s^2/2$ (assuming $C_d \gg C_u$).

V_s [V]	R [Ω]	E	E_R	E_k	E_c	E_d
40	0	2.75	0	0.82	1.39	0.54
50	0	4.42	0	1.48	2.23	0.71
60	0	6.32	0	2.11	3.18	1.03
40	100 k	0.72	0.19	0.19	0.16	0.17
50	100 k	1.00	0.27	0.33	0.23	0.17
60	100 k	1.31	0.39	0.49	0.26	0.17

Table 6.4: Energy balance for a gold MEMS switch with $g_o = 2.5 \mu\text{m}$, $Q = 1$, $k = 10 \text{ N/m}$, $f_o = 43 \text{ kHz}$, $V_p = 30 \text{ V}$, and a capacitive area of $100 \times 60 \mu\text{m}^2$. Energy is in nJ.

The energy delivered by the source and consumed in the switching process is calculated as:

$$E = V_s \int i(t)dt = E_e + E_m + E_R + E_k + E_d \quad (6.36)$$

where V_s is the source voltage (40-60 V), $i(t)$ is the switching current, E_e , E_m are the mechanical and electrical energy defined above, $E_k = \frac{1}{2}mv^2$ is the kinetic energy of the MEMS bridge, E_d is the energy dissipated in the damping mechanism, and $E_R = R \int i(t)^2 dt$ is the energy dissipated in the resistor (in this case $R = 0 \Omega$). For a bridge with $Q = 1$, $k = 10 \text{ N/m}$, and $V_s = 40\text{-}60 \text{ V}$, the total switching energy used is 2.75-6.32 nJ for the case of $R = 0 \Omega$ (Tab. 6.4). The potential energy stored in the stretched membrane, E_m , is very small (31 pJ) and is not included in Table 6.4. The damping component contributes to the energy balance and accounts for 13-20% of the total switching energy ($Q = 1$).

A plot of the energy components versus time is shown in Fig. 6.11 for $V_s = 50 \text{ V}$ and $Q = 1$. It is seen that the switching energy remains below 0.3 nJ up to $10.3 \mu\text{s}$ and then quickly rises to 4 nJ in the last $0.1 \mu\text{s}$ (Fig. 6.11). This is again due to the very high forces at the end of the switching cycle. At $t = 10.4 \mu\text{s}$, $g = 0.14 \mu\text{m}$ and, therefore, $K_n \approx 0.5$. The gas dynamics are dominated by particle-wall interactions (slip-effect) and viscous flow accounts for only 14% of the flow [43], questioning the validity of Eq. 6.26. Also, when the gap is near $0.1 \mu\text{m}$, the roughness of the switch surfaces, non-parallel plate deformations, and the etch-release holes will all have a significant effect on the switching energy. Therefore, the results for $g < 0.1 \mu\text{m}$ should only be used to show general trends.

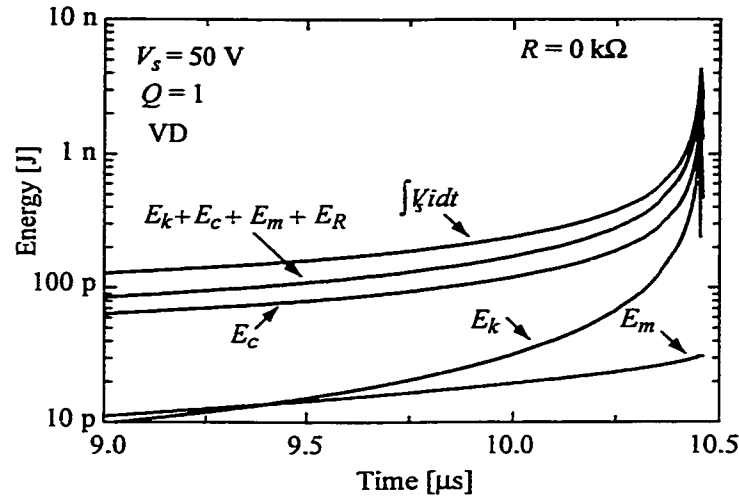


Figure 6.11: Simulated energy components versus time for the gold switch described in Section 6.6 for $V_s = 50$ V, $R = 0$ k Ω , and $Q = 1$.

6.6.3 Effect of Fringing Capacitance

The up-state fringing capacitance for MEMS shunt capacitive switches is between 0.2 and $0.6C_{pp}$ for most switches. The down-state fringing capacitance reduces to less than $0.05C_{pp}$. To study the effect of the fringing capacitance on the switch mechanics, the formula for switch capacitance is changed to:

$$C = \frac{\epsilon_o A}{g_o + \frac{t_d}{\epsilon_r} - z} \left(1.4 - 0.35 \frac{z}{g_o} \right) \quad (6.37)$$

which give a 40% fringing capacitance at $g = g_o$ and a 5% fringing capacitance at $g = 0$ μ m.

The external forcing function is similarly modified and is given by:

$$F_e = \frac{1}{2} \frac{\epsilon_o w W V^2}{\left(g_o + \frac{t_d}{\epsilon_r} - z \right)^2} \left(1.4 - 0.35 \frac{z}{g_o} \right) - \frac{1}{2} \frac{\epsilon_o w W V^2}{\left(g_o + \frac{t_d}{\epsilon_r} - z \right)} \left(\frac{0.35}{g_o} \right) \quad (6.38)$$

The simulated bridge height, velocity, and current versus time are shown in Figs. 6.12 and 6.13 for the gold switch discussed above with $V_s = 50$ V and $Q = 1$. It is seen that the fringing capacitance has some effect on the pull-down time, but little effect on the velocity and current near the point of impact. The switching time is reduced with fringing because the forces are greater in the upper 2/3 of the switching cycle. The impact velocity and energy are not significantly altered because the fringing capacitance is greatly reduced in the last

1/3 of the switching cycle. This means that the fringing capacitance of a switch should be taken into account for switching time estimates, but makes little difference for the other aspects of the switching mechanics.

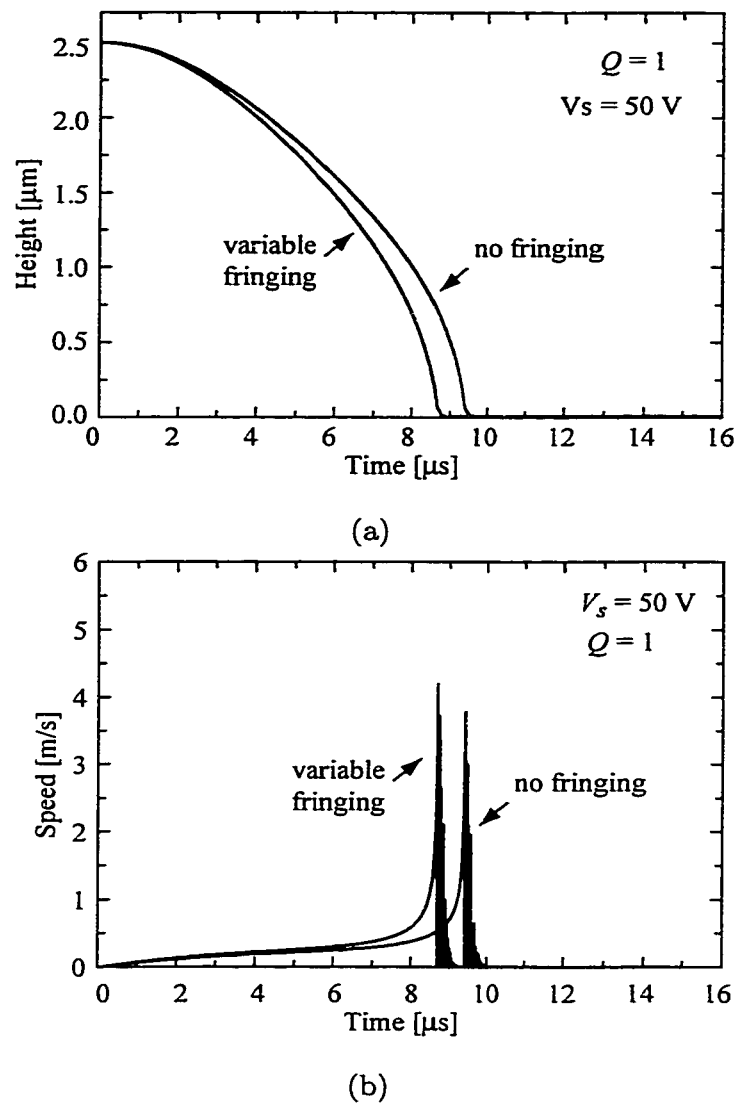


Figure 6.12: Simulated switch position (a) and velocity (b) versus time for the gold switch described in Section 6.6 for $V_s = 50$ V, $Q = 1$, and $R = 0$ k Ω , with and without a variable fringing capacitance (40-5%).

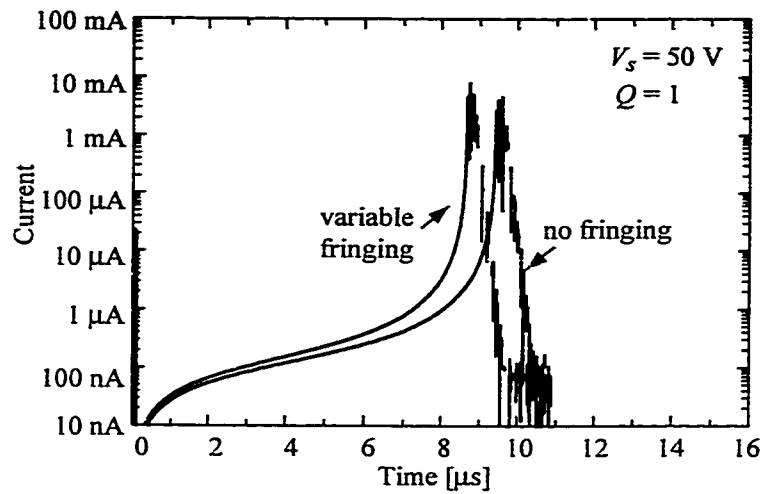


Figure 6.13: Simulated switching current versus time for the gold switch described in Section 6.6 for $V_s = 50$ V, $Q = 1$, and $R = 0$ k Ω , with and without a variable fringing capacitance (40-5%).

6.6.4 Resistive Damping

Reducing the impact energy of a MEMS switch may extend the lifetime of the switch. For shunt MEMS switches a reduced impact energy may reduce metal hardening that can make membranes more susceptible to fatigue. For series MEMS switches, reducing the impact energy may reduce hardening and dislocations in the metal crystal structure which may increase the metal-to-metal contact resistance.

Most RF MEMS switches have high impedance bias lines between the source and the switch. The presence of a 20 k Ω to 1 M Ω bias resistor reduces the total and kinetic energy of the MEMS switch near the point of contact by causing the voltage across the switch to drop when there is a rapid change in capacitance and therefore a large switching current 6.14. This method has been studied by Senturia et al. [29] and can be used to extend the mechanical lifetime of the switch. Figure 6.15 presents the kinetic energy at the point of impact for the switch similar described above with $Q = 0.5, 1$ and 2 , and $V_s = 50$ V. The kinetic energy near impact can be dramatically reduced by using a very high impedance bias resistor. A bias resistance of 1 M Ω reduces to kinetic energy near the point of impact from 1.34 nJ to 0.11 nJ for a switch with $Q = 1$ and $V_s = 50$ V.

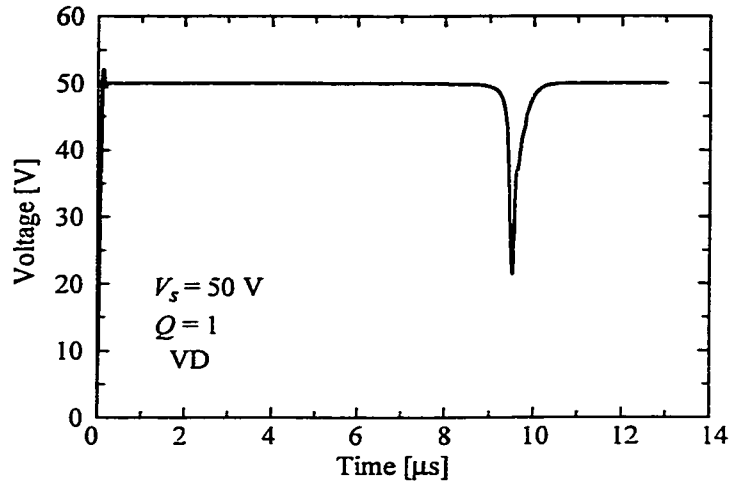


Figure 6.14: Simulated switch voltage (V_c) versus time for the gold switch described in Section 6.6 for $V_s = 50$ V, $Q = 1$, and $R = 100$ k Ω .

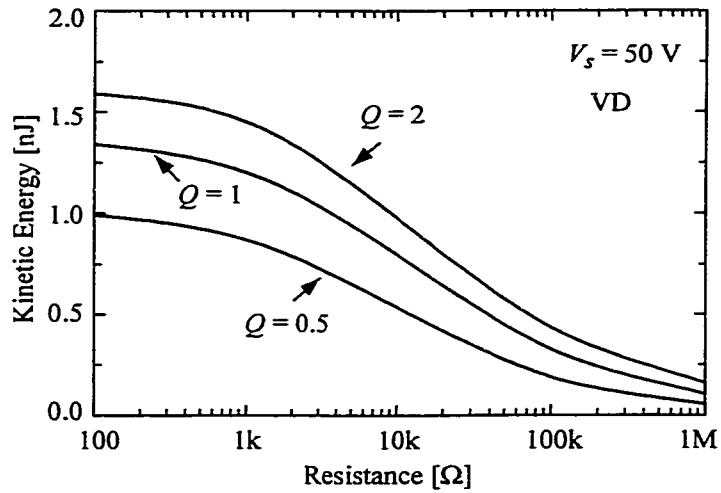


Figure 6.15: Simulated kinetic energy at the point of impact versus bias resistance for the gold switch described in Section 6.6 for different Q .

The energy components for $V_s = 50$ V, $Q = 1$, and $R = 100$ k Ω are shown in Fig. 6.16. The total switch energy is 1 nJ and the kinetic energy is 0.33 nJ. Notice that the energy does not increase dramatically in the last 0.1 μ s as in the case of $R = 0$ Ω . This is due to the voltage waveform on the switch which drops from 50 V to 12 V in the last 1 μ s of

the switching cycle. The switching time is $9.5 \mu\text{s}$, the impact velocity is 2 m/s , the peak switching current is 0.35 mA . This corresponds to a $0.3 \mu\text{s}$ increase in the switching time, a 2 m/s decrease in the impact velocity, and an 8 mA decrease in the switching current as compared to the $R = 0 \Omega$ case. The reason for the dramatic decrease in the current is due to the $C \frac{dV}{dt}$ and $V \frac{dC}{dt}$ current components which are in opposition to each other ($C \frac{dV}{dt}$ is negative, $V \frac{dC}{dt}$ is positive).

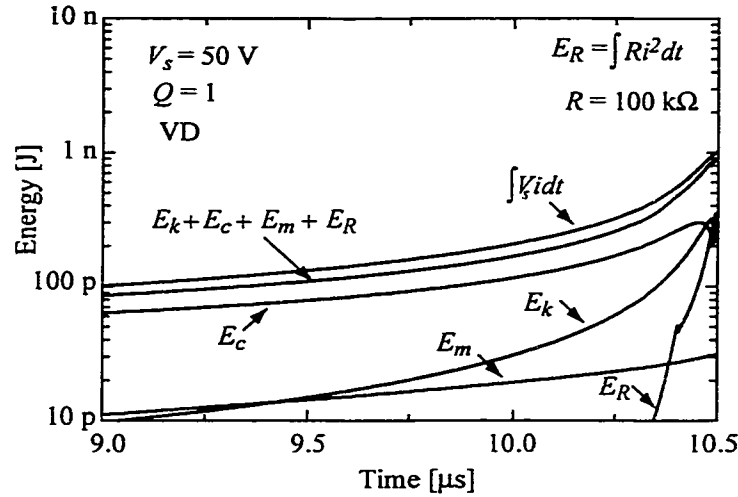


Figure 6.16: Simulated energy components versus time for the gold switch described in Section 6.6 for $V_s = 50 \text{ V}$, $R = 100 \text{ k}\Omega$, and $Q = 1$.

The large bias resistances have little effect on the release mechanics of the switch. The only effect is a delay in the release time by the 2-3 RC time constants if the switch is held down using a voltage which is much greater than the hold-down voltage. In other words, the voltage across the switch must be lower than V_h (Eq. 6.12) in order for the switch to release. If $V_s \gg V_h$, which is usually the case, then one must wait for the RC discharge to occur before the switch starts to release. For a $1 \text{ M}\Omega$ bias resistor and a down-state capacitance of 2 pF , the RC time constant is $1.7 \mu\text{s}$ and the switch is held down for about $5 \mu\text{s}$ before it starts to release.

6.6.5 Voltage Shaping

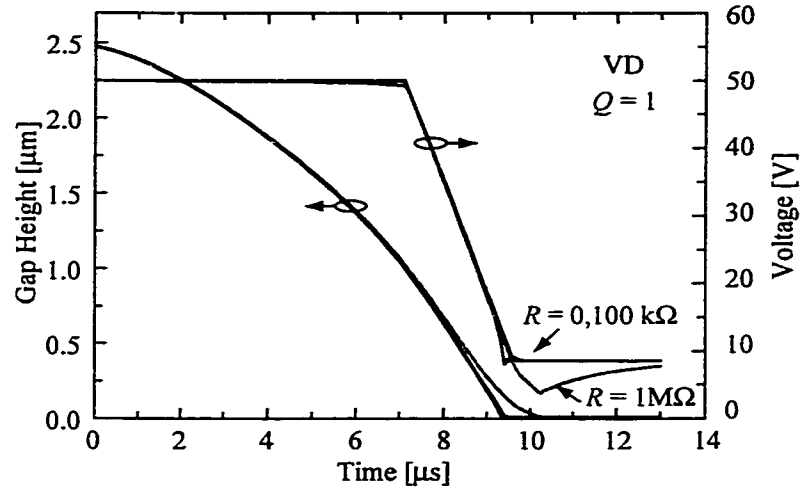
Another way to reduce the impact energy is to reduce the bias voltage, in the last 1/3 of the switching cycle, from a value greater than V_p to a value greater than V_h . This method requires either a very accurate model and understanding of the switching mechanics of the switch or a practical trial and error approach for a given switch. The reduction in the bias voltage near the end of the cycle slightly increases the switching time, but can greatly reduce the impact velocity, switching current and impact energy.

For the simulation shown in Fig. 6.17, the bias voltage is reduced to nearly 10% of the original bias voltage and the bias resistance is taken to be $0\ \Omega$. The velocity near the point of impact is reduced from 3-6 m/s to 0.4-0.8 m/s, resulting in more than a $30\times$ reduction in the impact energy from 1.48 nJ for a constant bias voltage of 50 V to 45 pJ for a shaped voltage function. The impact energy is reduced dramatically because the electro-static forcing function is proportional to the square of the applied bias voltage. The switching current is reduced to 0.46 mA for the 50 V bias voltage function. Combining resistive damping and voltage shaping can further reduce the kinetic energy near the point of impact. The addition of a 100 k to 1 M Ω bias resistor to the shaped function lowers the switching current from 0.46 mA ($R = 0\ \Omega$) to 50-5 μ A, the impact velocity from 0.82 m/s ($R = 0\ \Omega$) to 0.48-0.05 m/s, and the impact energy from 45 pJ to less than 15-1 pJ, respectively.

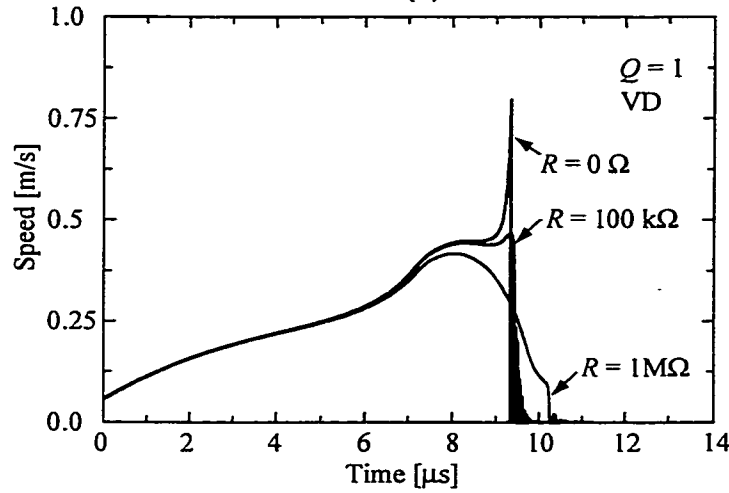
6.6.6 Gap-Stop Measures

For switches with pull-down electrodes that are separate from the RF contact, another way to limit the kinetic energy of the switch at the point of impact is to have a mechanical gap-stop (Fig. 6.18). A gap-stop would prevent the switch from contacting the pull-down electrodes while still allowing a good RF contact. A gap stop therefore does not allow the large increase in the kinetic energy just before the point of impact. There are two ways to realize a gap-stop: 1) using micro-machined dielectric posts underneath the cantilever (Rockwell switch), or 2) using a very thick and rigid cantilever (Analog Devices switch [18]).

A plot of the simulated pull-down dynamics for a cantilever switch with $g_o = 2.5\ \mu\text{m}$,



(a)



(b)

Figure 6.17: Simulated switch position and bias voltage versus time (a) and switch velocity (b) for the gold MEMS switch described in Section 6.6. The initial ($t = 0 \mu\text{s}$) bias voltage is $V_s = 50 \text{ V}$ and is reduced to less than 10 V near the end of the switching cycle.

$Q = 1$, $k = 10 \text{ N/m}$, $f_o = 43 \text{ kHz}$, $V_p = 30 \text{ V}$, and a capacitive area of $80 \times 80 \mu\text{m}^2$ is shown in Fig. 6.18b. The switch velocity is reduced to less than 0.8 m/s as compared to a velocity greater than 4.5 m/s without the stop, resulting in a $25\times$ reduction in the kinetic energy at impact. The switching current is reduced from 11 mA to $7 \mu\text{A}$ since the capacitance does not change much for $g = 0.5 \mu\text{m}$. The impact energy is reduced from 1.48 nJ for a standard

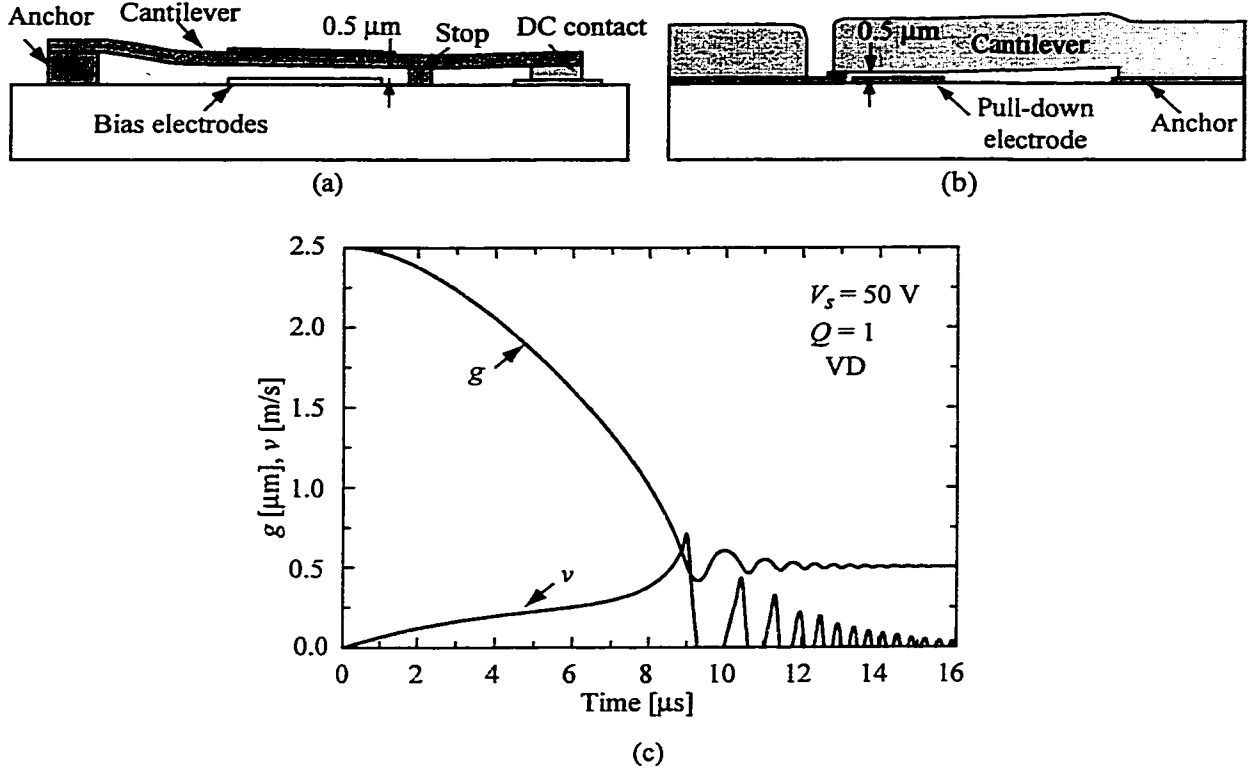


Figure 6.18: Illustration of a gap-stopped cantilever switches (a,b). Simulated pull-down (g) and velocity (v) for a cantilever MEMS series switch with $g_o = 2.5 \mu\text{m}$, $Q = 1$, $k = 10 \text{ N/m}$, $f_o = 43 \text{ kHz}$, $V_p = 30 \text{ V}$, and a capacitive area of $100 \times 60 \mu\text{m}^2$ (c).

switch to 35 pJ for the switch with a stop. The reduction in the impact energy may increase the mechanical life-time of MEMS cantilever switches. The addition of a high impedance bias resistor does not give an additional dramatic reduction in the impact energy, due to the very low switching current at $g = 0 \mu\text{m}$.

The drawback for shunt switches is the inevitable reduction in the RF capacitance ratio because the bridge will not make an intimate a contact as compared to standard switches, such as the Raytheon shunt switch [24]. Therefore, gap-stop measures are useful for series MEMS switches and 2-level MEMS varactors.

6.7 RF Model of MEMS Switches

The presence of an RF signal on a MEMS switch may cause some interesting mechanical and electrical effects. An RF voltage, $V(t) = V \sin(\omega t)$, applied to a MEMS switch induces a force given by

$$F_e(t) = \frac{1}{2} \frac{dC}{dg} V_{RF}^2 = \frac{1}{2} \frac{dC}{dg} \frac{V_{RF}^2}{2} (1 + \cos(2\omega t)) \quad (6.39)$$

where C is the RF capacitance between the switch and the RF line and ω is the frequency of the RF signal. The force given in equation 6.39 has a static and high frequency component at 2ω , which is much higher than the mechanical frequency response of a MEMS switch. Therefore, an equivalent DC voltage due to the RF signal can be defined as:

$$V_{DC} = \frac{1}{\sqrt{2}} V_{RF} = V_{RF} \text{ (rms)} \quad (6.40)$$

and can be incorporated in the the electro-mechanical model of Section 6.2. Because of the traveling-wave nature of an RF voltage signal on a transmission line, the RF voltage across a MEMS switch is a function of the incident, reflected, and transmitted voltage waves and depends on the impedance and configuration of the switch. Two configurations will be discussed: 1) a shunt capacitive MEMS switch, and 2) a series MEMS switch.

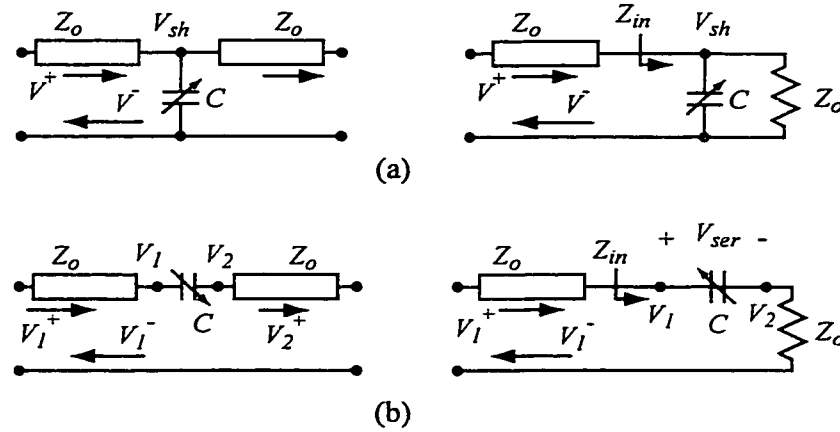


Figure 6.19: RF equivalent circuits for a series (a) and shunt (b) MEMS switch.

6.7.1 RF voltage across a MEMS shunt switch

The equivalent RF circuit model for a shunt capacitive MEMS switch is shown in Fig. 6.19a, and consists of a transmission line loaded by a shunt capacitance. The RF voltage across the shunt capacitance (V) is the addition of the incident (V^+) and reflected (V^-) waves. The reflected wave is related to the incident wave by $V^- = \Gamma V^+$, where Γ the reflection coefficient. The voltage across the MEMS shunt switch can be written as:

$$\begin{aligned} V_{sh} &= V^+ (1 + \Gamma) \\ |V_{sh}| &= |V^+| |1 + \Gamma| \end{aligned} \quad (6.41)$$

The impedance (Z_{in}) as seen from the input is the parallel combination of the shunt capacitance and the output transmission line impedance:

$$Z_{in} = \frac{Z_o}{1 + j\omega C Z_o} \quad (6.42)$$

and the reflection coefficient and $|1 + \Gamma|$ are given by:

$$\begin{aligned} \Gamma &= \frac{Z_{in} - Z_o}{Z_{in} + Z_o} = \frac{-j\omega C Z_o}{2 + j\omega C Z_o} \\ |1 + \Gamma| &= 1 - \frac{\omega^2 C^2 Z_o^2}{4 + \omega^2 C^2 Z_o^2} \end{aligned} \quad (6.43)$$

The voltage across the MEMS shunt switch then becomes:

$$|V_{sh}| = \frac{|V^+|}{\sqrt{1 + \frac{\omega^2 C^2 Z_o^2}{4}}} \quad (6.44)$$

When the MEMS switch is in the up-state position, the shunt capacitance is small ($\omega^2 C_u^2 Z_o^2 \ll 1$) and very little of the incident voltage wave is reflected. Therefore, in the up-state position, the voltage across the switch is approximately equal to the incident voltage. When the switch is in the down-state, the shunt capacitance is much larger ($\omega^2 C_d^2 Z_o^2 \gg 1$) and looks like a short circuit. Therefore, the reflected wave partially cancels the incident voltage wave, greatly reducing the voltage across the switch.

For RF power handling, the incident voltage wave is expressed in terms of the incident power wave by:

$$|V^+| = \sqrt{2Z_o P_{inc}} \quad (6.45)$$

where P_{inc} is the incident power. The above analysis for shunt and series switches can be integrated into the nonlinear mechanical analysis to investigate effects such as two-tone mixing and RF power handling of MEMS switches.

6.7.2 RF voltage across a MEMS series switch

The equivalent RF circuit model for a single gap series capacitive MEMS switch is shown in Figure 6.19b, and consists of a transmission line interrupted by a series capacitance. The voltage across the series capacitance can be derived using simple circuit analysis:

$$V_{ser} = V_1 - V_2 \quad (6.46)$$

The impedance (Z_{in}) looking in from the input is the series combination of the capacitance and the output transmission line impedance:

$$Z_{in} = \frac{1}{j\omega C} + Z_o \quad (6.47)$$

and the reflection coefficient is given by:

$$\Gamma = \frac{1}{1 + j2\omega C Z_o} \quad (6.48)$$

The voltage at the input of the switch (V_1) is given by:

$$V_1 = V_1^+ (1 + \Gamma) \quad (6.49)$$

and the voltage at the output of the switch (V_2) is given by:

$$V_2 = \frac{V_1 Z_o}{Z_{in}} \quad (6.50)$$

The voltage across the MEMS series switch then becomes:

$$|V_{ser}| = |V_2 - V_1| = \frac{2|V^+|}{\sqrt{1 + 4\omega^2 C^2 Z_o^2}} \quad (6.51)$$

When the MEMS switch is in the up-state, the series capacitance is small ($\omega^2 C^2 Z_o^2 \ll 1$) and looks like an open circuit. Therefore, most of the incident voltage wave is reflected and the voltage across the switch is approximately $2\times$ the incident voltage ($V_1 = 2V_1^+$ and $V_2 \simeq 0$). When the switch is near the down-state position, the series capacitance is much

larger ($\omega^2 C^2 Z_o^2 \gg 1$) and looks like a short circuit, greatly reducing the voltage across the switch. In essence, $V_1 \simeq V_2 \simeq V^+$, and the voltage across the switch is nearly zero. For series switches with two gaps, the voltage across each gap is approximately half of the voltage in equation 6.51.

6.7.3 RF Power Handling

The effect of RF power on a MEMS shunt capacitive switch can be included in the simulations by using an equivalent DC voltage given by equation 6.45 and 6.44. The alternative is to use the exact RF voltage magnitude and frequency. The two methods yield identical results. However, the latter case requires substantial simulation capabilities and time.

The RF power handling of MEMS switches can be approximated by substituting equation 6.40 into equations 6.11 or 6.12. The power required to pull down a MEMS shunt or series switch from the up-state to the down-state is:

$$P_p \simeq \begin{cases} \frac{8kg_o^3}{27\epsilon_o AZ_o} & \text{for shunt switches } (V_{sh} \simeq V^+) \\ \frac{2kg_o^3}{27\epsilon_o AZ_o} & \text{for single gap series switches } (V_{ser} \simeq 2V^+) \end{cases} \quad (6.52)$$

where A is the RF capacitive area. For shunt and series MEMS switches with $g_o = 2.5 \mu\text{m}$, $k = 10 \text{ N/m}$, $Z_o = 50 \Omega$, $A = 100 \times 60 \mu\text{m}^2$ (shunt) and $20 \times 20 \mu\text{m}^2$ (series), the pull-down power is 17.4 W and 65 W, respectively. Both of these values are well beyond the thermal power handling capabilities of MEMS switches. However, low k and low height switches have much lower pull-down powers. For the above examples with $g_o = 1.5 \mu\text{m}$ and $k = 2 \text{ N/m}$, the pull-down powers are .75 W and 2.8 W, for the shunt and series switches, respectively. This suggests that MEMS shunt switches might be used as power limiters in some applications, especially low- k designs. The double gap series switch should handle 4× as much power as a single gap for a given capacitive area.

For a MEMS shunt switch, the RF power required to hold the switch in the down-state

is derived using Eqs. 6.40, 6.12, and 6.44, and is:

$$\begin{aligned}
P_h &= \frac{2kg_o(t_d/\epsilon_r)^2}{\epsilon_o AZ_o} \left(1 + \frac{\omega^2 Z_o^2 \epsilon_o^2 A^2}{4(t_d/\epsilon_r)^2} \right) \\
&= \frac{2kg_o(t_d/\epsilon_r)}{C_d Z_o} \left[1 + \left(\frac{\omega C_d Z_o}{2} \right)^2 \right] \\
&\simeq \frac{\epsilon_o A k g_o \omega^2 Z_o}{2} \quad \text{for } \frac{\omega Z_o C_d}{2} \gg 1
\end{aligned} \tag{6.53}$$

where k is the effective spring constant due to load distribution of the RF electrostatic force. For $g_o = 2.5 \mu\text{m}$, $k = 10 \text{ N/m}$, $t_d = 0.2 \mu\text{m}$, $\epsilon_r = 7.6$, and $A = 100 \times 60 \mu\text{m}^2$, $Z_o = 50 \Omega$, and $f = \omega/2\pi$ equals 10 and 30 GHz, the hold-down power is 150 mW and 1.2 W respectively. The reason for a larger power handling at 30 GHz is that the MEMS shunt switch with $C_d = 1.6 \text{ pF}$ is a much better short at 30 GHz than at 10 GHz and this results in a much smaller RF voltage on the switch. For comparison, the hold-down power at 1 GHz is only 22 mW.

The hold-down power for DC-contact MEMS series switches is complicated by the low resistance contact, and the metal-to-metal contact physics in the down-state position. However, once the series switch begins to release, the series capacitance can cause the switch to self-actuate back to the down-state. For a small gap near the down-state in a MEMS single gap series switch, the hold-down power is derived using Eqs. 6.12, 6.40 and 6.51, and is approximately:

$$\begin{aligned}
P_h &= \frac{2k(g_o - g)g^2}{\epsilon_o AZ_o} \left(1 + \frac{4\omega^2 Z_o^2 \epsilon_o^2 A^2}{g^2} \right) \\
P_h &\simeq 8kg_o\omega^2\epsilon_o AZ_o
\end{aligned} \tag{6.54}$$

and for $k = 10 \text{ N/m}$, $g_o = 2.5 \mu\text{m}$, $A = 20 \times 20 \mu\text{m}^2$, $Z_o = 50 \Omega$, and $f = 10 \text{ GHz}$, the hold-down power is approximately 140 mW. For a double gap series switch, the power is $4\times$ larger. Since Eq. 6.54 is a strong function of the gap height g , the roughness of the contact metals and dimpled geometries can greatly affect the calculated hold-down power. An air-gap of 500 \AA raises the hold down-power to 830 mW for the series switch mentioned above.

Figure 6.20 shows RF power pull-down and hold-down simulations of a gold MEMS shunt switch described in section 6.6 with $Q = 1$. These simulations are consistent with, and help support, equations 6.53 and 6.52, developed with static analysis.

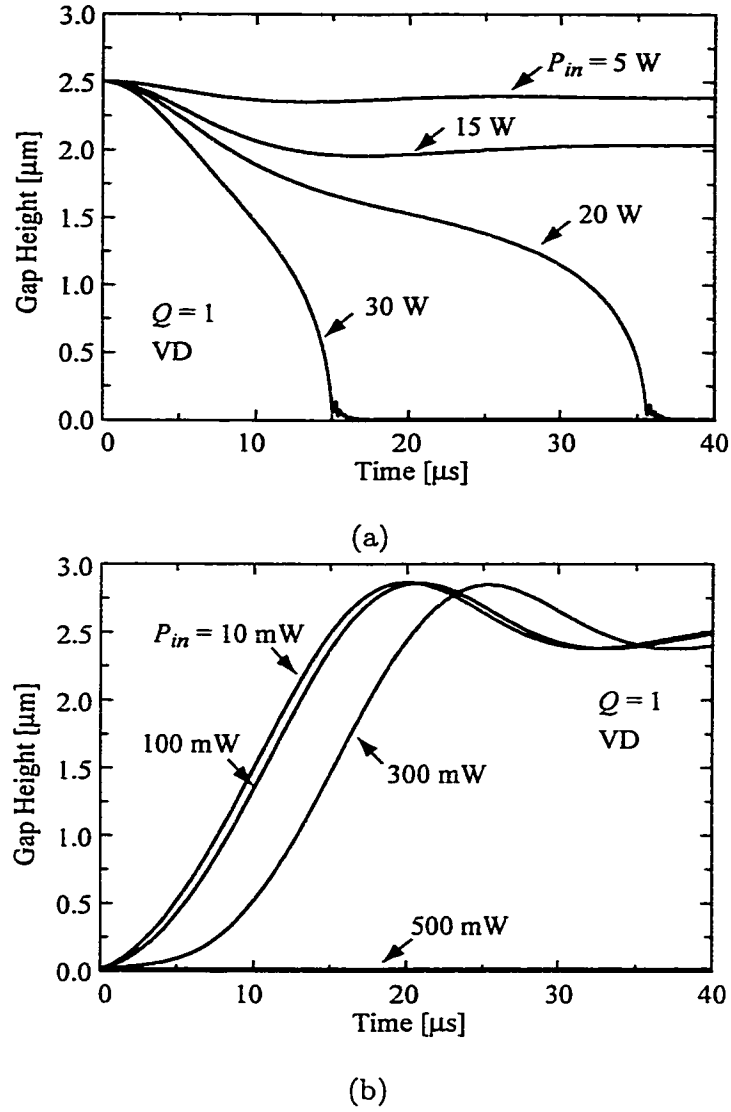


Figure 6.20: Simulated gap height versus times for a different levels of RF power for the shunt capacitive switch described in Section 6.6

6.7.4 Source Voltage Noise, Intermodulation, and Phase Noise

The RF phase noise due to Brownian motion, acoustic sources, vibrations and source voltage noise have been investigated by Gabriel Rebeiz [44]. It was found that phase modulation occurs when the capacitance is changed as the switch vibrates. Let us examine a related source for RF phase noise; RF intermodulation due to a signal with closely spaced frequencies.

Two RF signals on a MEMS shunt switch, $V_1(t) = V_1 \sin(\omega_1 t)$ and $V_2(t) = V_2 \sin(\omega_2 t)$ with a difference in frequency of $\delta\omega = \omega_1 - \omega_2$, can mix together to create an electrostatic forcing function with frequency components at DC, $\delta\omega$, $2\omega_1$, $2\omega_2$, and $(\omega_1 + \omega_2)$, due to the V^2 term in equation 6.4. Since the switch can only respond to the DC and $\delta\omega$ components, the higher frequency terms can be ignored, reducing the simulation time. However, the exact RF voltages and frequencies can be used directly in the forcing function of Eq. 6.4 and yields identical results but with much longer simulation times.

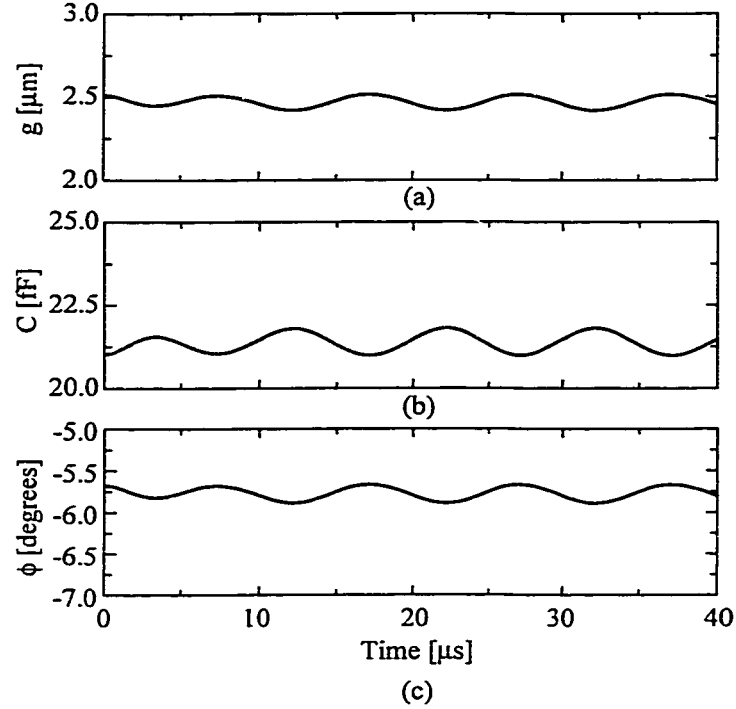


Figure 6.21: Simulated gap height (a), capacitance (b), and RF phase (c) versus time for two 1 W RF signals at 10 GHz with a difference in frequency $\delta f = 100$ kHz for an aluminum shunt capacitive switch described in Section 6.6, with $\omega_o = 114$ kHz and $Q = 1$.

Figure 6.21 shows the effect of two equal power 1 W RF signals ($|V_1| = |V_2| = 10$ V) near 10 GHz separated by 100 kHz. The aluminum MEMS switch is in a shunt topology in the up-state position and has the characteristics described in Section 6.6 with $\omega_o = 114$ kHz and $Q = 1$. It is seen that the RF signals “beat” together to produce a 100 kHz forcing function frequency and thus a $0.125 \mu\text{m}$ peak-to-peak change in the gap height at 100 kHz.

Notice that the switch also self biases due to the DC component of the mixed signals. The phase of an RF signal passing through a MEMS shunt switch in the up-state is [44]:

$$\angle S_{21} = \phi = \frac{-\omega C Z_o}{2} \quad (6.55)$$

and the phase noise is given by [44]:

$$P_{ph} = \frac{1}{2} \frac{1}{(1 + \gamma)^2} \frac{\overline{z_n^2}}{g_o^2} \phi_o^2 \quad / \text{Hz} \quad (6.56)$$

where $\gamma = C_f/C_{pp}$ is the fringing capacitance fraction (in this case $\gamma = 0.4$). From the simulated results, the phase changes by $\pm 0.15^\circ$ and the phase noise is -43 dBc/Hz, for a single MEMS shunt switch. This has implications for high power applications such as phase shifters and tunable filters, resonators, and oscillators.

6.8 Conclusions

This chapter presents an 1-D model of the switching mechanics in MEMS electrostatic switches. The total switching energy is quite low (1-5 nJ) for $Q = 1$ systems. However, the speed of the switch at impact is high (2-4 m/s) and this can affect the switch reliability. Also, the currents involved are substantial and should be taken into account in the design of the DC switching networks. The presence of high impedance bias lines slows down the switch, and reduces the total and kinetic energy of the switch at the moment of impact. Other measures such as voltage shaping or gap-stops will reduce the switching energy and increase the lifetime of the switch. Finally, a detailed study of the self-actuation mechanism of shunt and series switches has been done taking into account the RF voltage across the switch.

CHAPTER 7

FUTURE WORK

This thesis has presented a electro-magnetic and mechanical modelling of MEMS series and shunt switches. Several novel MEMS switch designs were developed, fabricated and tested, including: all-metal DC-contact series switches, capacitive shunt switches, inline capacitive shunt switches, and DC-contact shunt switches. Equivalent circuit models were developed and implemented in tuned circuits for high isolation switching applications.

Many challenges and opportunities for lie ahead for RF MEMS. The most prominent obstacles for commercialization are reliability and packaging. Once these challenges are overcome, RF MEMS may find their way into commercial tunable resonators, filters, and oscillators. These applications require low-loss high-Q MEMS varactors or switched state capacitors. Series DC-contact switches may be used extensively in compact, low-loss phase shifters. The next sections outline future research ares and ideas for such RF MEMS applications.

7.1 All-Metal Series Switch for Microstrip

An all-metal series switch was designed and fabricated at the University of Michigan as a compliment to the all-metal switch developed for CPW geometries (see Fig. 7.1). These switches were to be the building block for single-pole multiple-throw switches and switched line phase shifters. This work is being continued by Guan-Leng Tan at the University of Michigan.

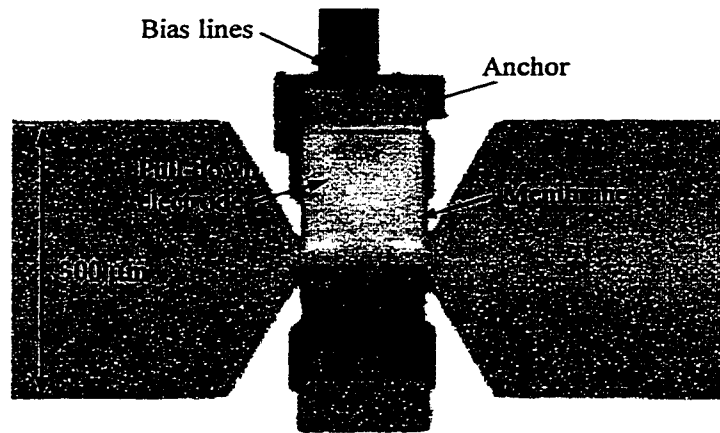


Figure 7.1: Photomicrograph of a MEMS series switch implemented in microstrip.

7.2 Design of Single-Pole Multiple-Throw Series Switches

The near ideal response of MEMS series switches result in a straight-forward implementation of a single-pole multiple-throw switch for the 1-40 GHz frequency range with excellent isolation. A single-pole double-throw (SP2T or SPDT) switch is shown in Fig. 7.2. The most important part of the design is actually the distance between the MEMS switches and the reactive junction, labeled d_s in Fig. 7.2. When S1 is in the up-state position, the short sections of transmission line in the arm of S1 acts as a small capacitance and increases the input reflection coefficient of the SP2T switch. Figure 7.3 shows the return loss of a SP2T with $d_s = 100 \mu\text{m}$ and $d_s = 250 \mu\text{m}$ on a silicon substrate. The input reflection coefficient can be improved by the addition of a short high-impedance section before the reactive junction (Z_h and d_1 in Fig. 7.2 and Fig. 7.3). The same idea applies for SP3T and SPNT (more sensitive to d_s). The insertion loss and isolation are not shown in Fig. 7.3 but are near ideal for the matched SP2T design. The isolation is 6 dB better than a standard series switch due to the presence of the “thru” port.

If higher isolation is required from a single-pole multiple-throw switch, then a series/shunt switch should be used in each arm of the switch. If operation up to 50 GHz is needed, then d_s must be smaller than $150 \mu\text{m}$ for a SPDT design on a silicon substrate.

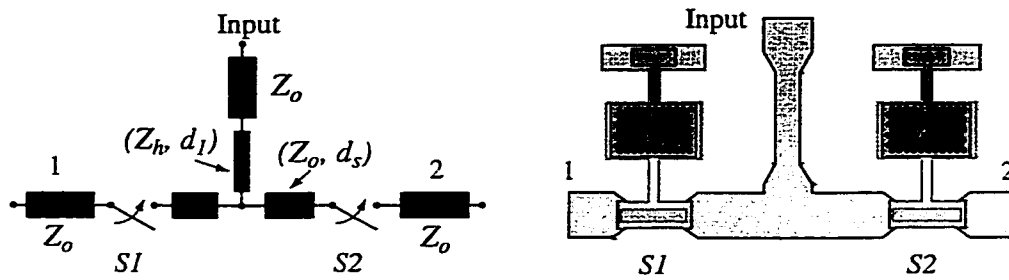


Figure 7.2: Equivalent circuit and microstrip layout for a SP2T series switch.

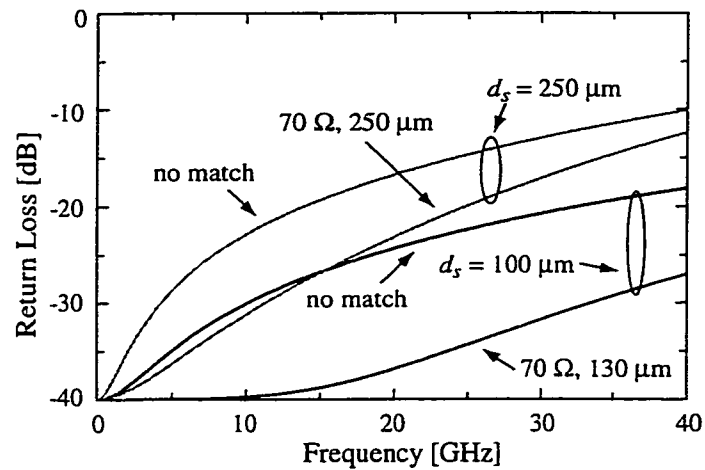


Figure 7.3: Simulated return loss for a SP2T series MEMS switch with $d_s = 100 \mu\text{m}$ and $250 \mu\text{m}$. Also shown is the return loss with a short high-impedance matching section at the input port.

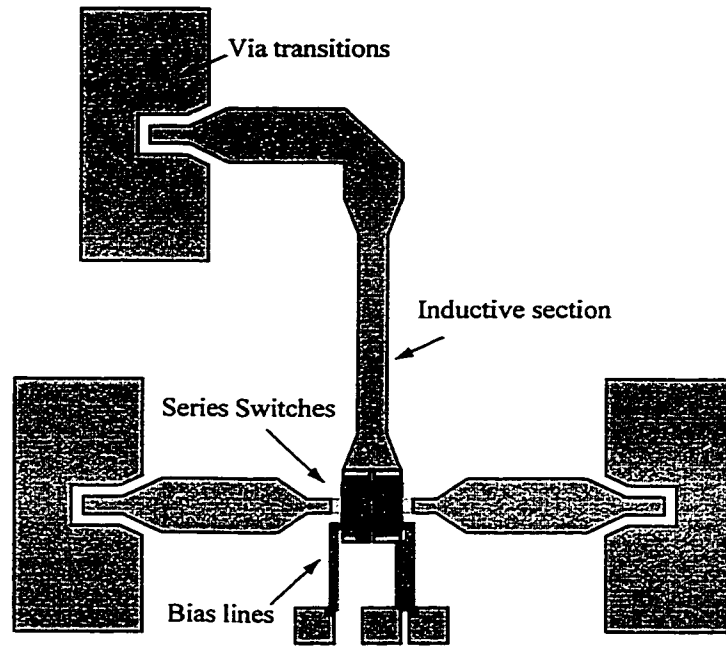


Figure 7.4: Physical layout and simulated S-parameters of a SP2T switch using the All-metal series switch with only one contact.

Also, the reactive T-junction must be modeled using numerical electromagnetic techniques for optimum performance up to 50 GHz. The SP2T switch can also be implemented using capacitive series switches if operation from 4 GHz and higher is required.

A compact implementation of a SP2T switch using the All-metal series switch presented in Chapter 5 is shown in Fig. 7.4. The simulated S-parameters are shown in Fig. 7.4b. In this case, the series switch has only one metal contact, reducing the switch capacitance in the up-state and the contact resistance in the down-state.

A novel switch matrix can be developed using the all-metal series switch modified as above to have only one contact point. A 4-node network implementation is shown in Fig. 7.5. The simulated S-parameters show good performance up to 20 GHz. The isolation between far ports is better than -50 dB at 10 GHz with the other two ports connected. With all the switches up, the isolation between all the ports is better than -45 dB at 10 GHz. The return loss for all connected paths is less than -18 dB up to 20 GHz. Such a switch matrix could be very useful for making compact switched line phase shifters.

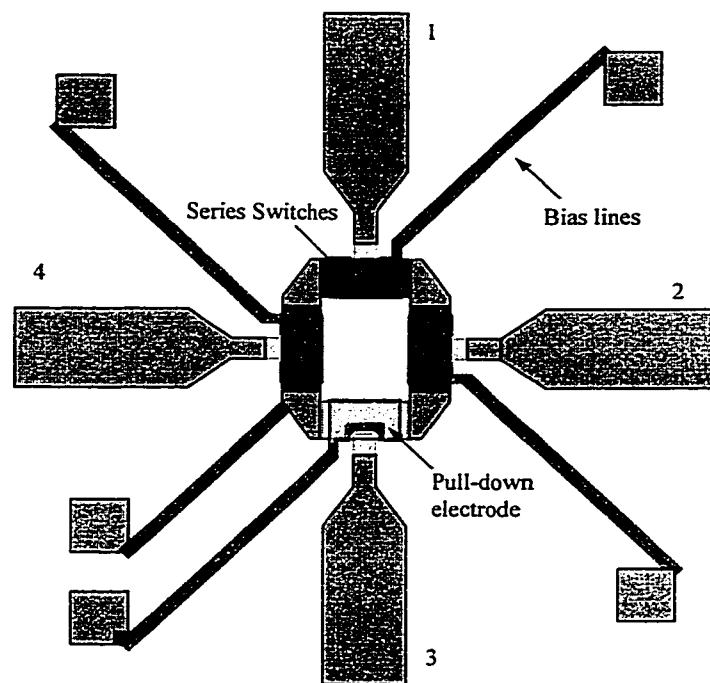


Figure 7.5: Physical layout and simulated S-parameters of a 4-node switch matrix using the All-metal series switch with only one contact.

7.3 76 GHz M/A-COM Switch Examples

Shunt capacitive switches were developed in microstrip and channelized microstrip implementations using the M/A-COM GMIC process. The design and simulation of these switches was completed at the University of Michigan. M/A-COM fabricated the GMIC vias and the first metal layers. The rest of the processing will be completed at the University of Michigan and the measured results will be presented in a future paper.

In our effort to design high isolation switches for automotive radar applications at 76 GHz, we first concentrated on designing and simulating single MEMS switches that are compatible with MACOM's GMIC process. Conventional microstrip designs using pyramidal vias for the ground path were investigated. Equivalent lumped-element circuit models for single switches were implemented in a tuned at 76 GHz. The method tuned approach with equivalent circuit models works well for K-band switches, however at 76 GHz the inductance to ground and the element-to-element interaction becomes significant. Because of this fact, full wave simulations of tuned switches as well as measurement of test structures have been done.

Two basic switch geometries, shown in Fig. 7.6 were investigated for the single bridge switch in the microstrip configuration. The first geometry, Fig. 7.6a, involves the use of two vias placed on either side of the microstrip line and an airbridge suspended over the microstrip line from one via to the other. The second geometry, Fig. 7.6b, involves placing a via directly under an airbridge section of microstrip line. The S-parameters of each geometry were simulated using IE3D and compared to S-parameters derived using lumped element models. The lumped element parameters were obtained using Maxwell 3D and 2D Electrostatic solvers, as well as Simian. The final measurements will be presented in a future paper, pending successful fabrication.

7.4 Increased Tuning Range and Switched State Varactors

One way of obtaining an increased tuning range for MEMS varactors is to have steps in the height of the bridge as shown in Fig. 7.7a. The section of the bridge over the RF

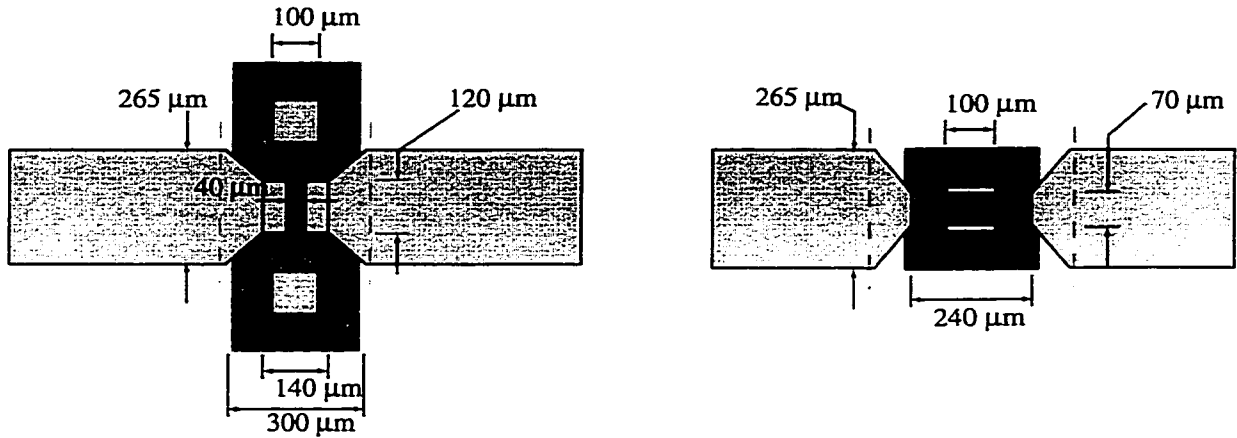


Figure 7.6: The two basic prototype geometries investigated for the shunt MEMS capacitive switches with via-holes implemented in MA-COM's GMIC process.

capacitance is lower than the sections over the actuation portion of the bridge. This allows for a capacitance variation that could be as much as 5 to 1 with correct design before the varactor acts like a switch and collapses to the down-state. Such designs have been fabricated and the measured results will appear in a later paper with Dr. Laurent Dussopt.

A high Q switched state varactor can be obtained using a similar step method discussed above. However the step relationship is inverted (see Fig. 7.7b). The section over actuation electrodes is lower than the section over the RF capacitive portion of the varactor. In this way, the varactor in the down-state has an air gap capacitance with the gap height determined by the difference in the step height of the actuation portion and the RF portion. This type of varactor would be very suitable for switched frequency resonators, oscillators and tunable filters because the quality factor of the varactors in the down-state might be as high as 200-500 at K and X bands.

7.5 Tunable Resonators and Filters

Obtaining a low-loss planar resonator necessitates the use of microstrip t-lines on low loss substrates. High Q microstrip resonators and filter structures have been widely demonstrated [45]. Tunable resonators and filters have also been demonstrated with active varac-

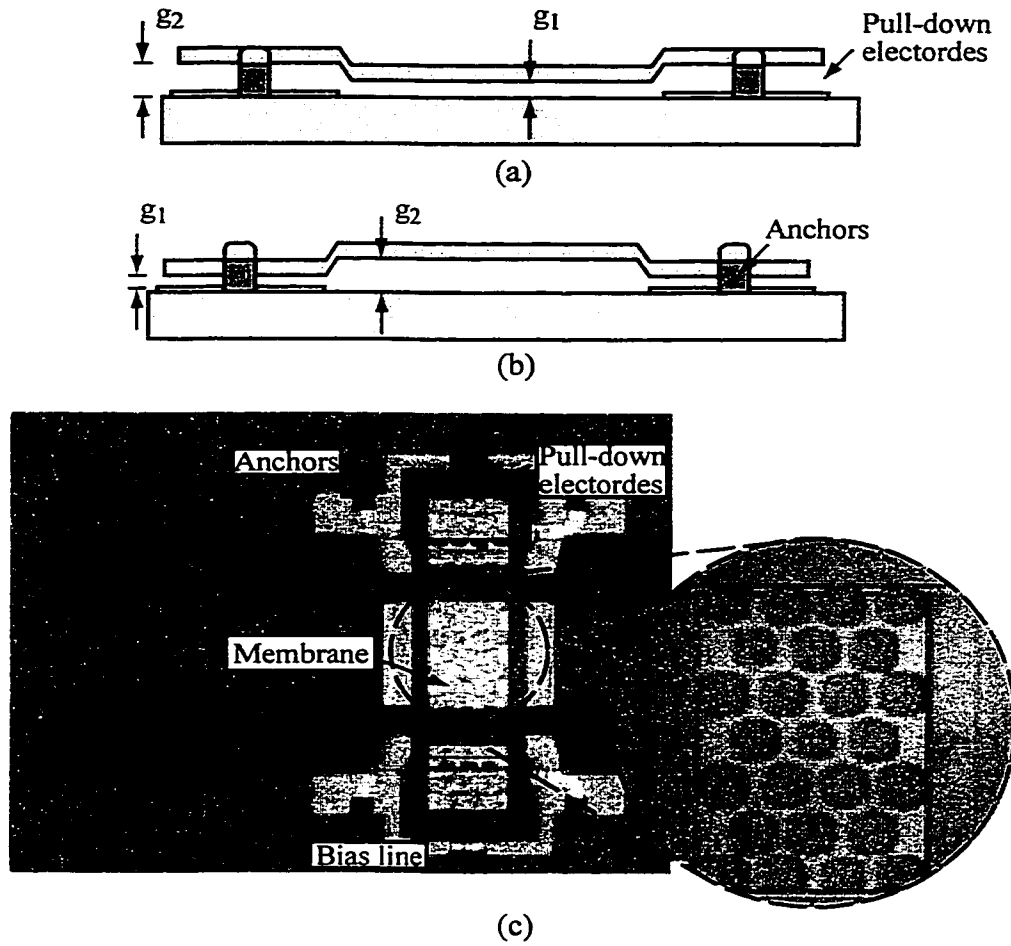


Figure 7.7: Illustration of an increased tuning range varactor (a), a switched state varactor (b), and a photomicrograph of a CPW MEMS varactor with holes for decreased damping.

tors. Loading these types of resonators with MEMS varactors seems to be the next step. The varactors may be connected to the microstrip ground by direct connection through vias or by capacitive coupling.

Channelized microstrip can be fabricated with the use of micro-machining, an example of which is the M/A-COM GMIC process described earlier. I propose the use of inverted microstrip, a variant of the M/A-COM design, in which the microstrip is fabricated on one side of a thin quartz wafer. The wafer is then low-temperature bonded to a metallized silicon wafer with cavities surrounding the microstrip lines as shown in Fig. 7.8. This

implementation allows for a low loss resonator with easy access to the ground planes which are brought up to the circuit layer by the micromachined cavity walls. MEMS devices can be easily fabricated on the thin quartz wafer. If a good low-temperature bond and seal is developed, the metallized cavities may also serve as as mechanical/environmental packaging for the MEMS devices.

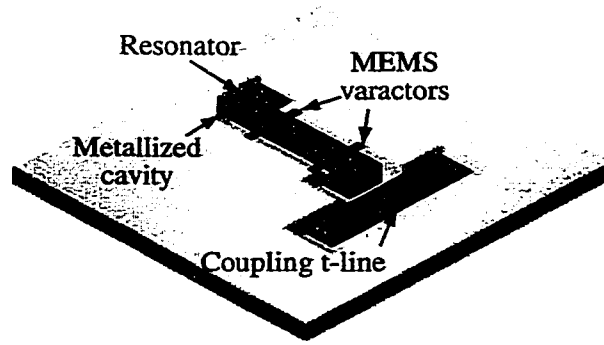


Figure 7.8: Inverted microstrip implementation of a tunable planar resonator. Quartz carrier wafer not shown.

7.5.1 Variable Resonator

A variable resonator can be achieved by loading a transmission line resonator with several MEMS membrane varactors. Microstrip resonators can achieve quality factors of 400-500 around X-Band while CPW resonators have quality factors of 100-200. The CPW resonator is examined here because of the ease of analysis. A typical CPW design is shown in in Fig. 7.9. Simple circuit analysis yields a transcendental equation for the resonant frequency of the loaded resonators,

$$\omega_r = \frac{1 - \tan \beta \ell_1 \tan \beta \ell_2}{Z_o C_u \tan \beta \ell_2} \quad (7.1)$$

where ℓ_1 , and ℓ_2 are defined in Fig. 7.9. The location of the MEMS varactors determines the coupling to the resonator and the associated frequency shift and tunability (Fig. 7.10). Varying the up-state capacitance of the MEMS varactors causes a shift in the resonant frequency of the transmission line resonator as shown in Fig. 7.11. Because the Q of the MEMS varactors is much higher than the transmission line resonator Q and the coupling

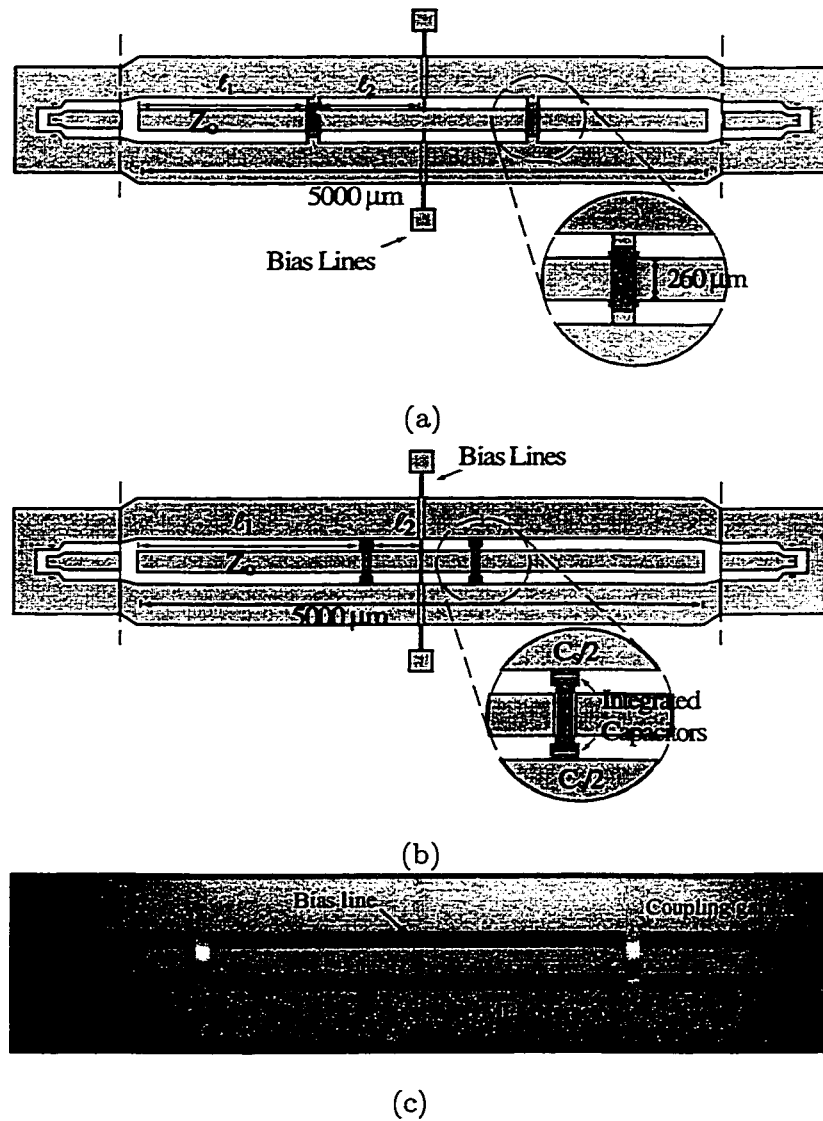


Figure 7.9: Physical implementation of a CPW tunable resonator on silicon(a). The MEMS varactors in the switched mode can be used with integrated capacitors to make a two state resonator(b). Photomicrograph of a fabricated tunable resonator(c).

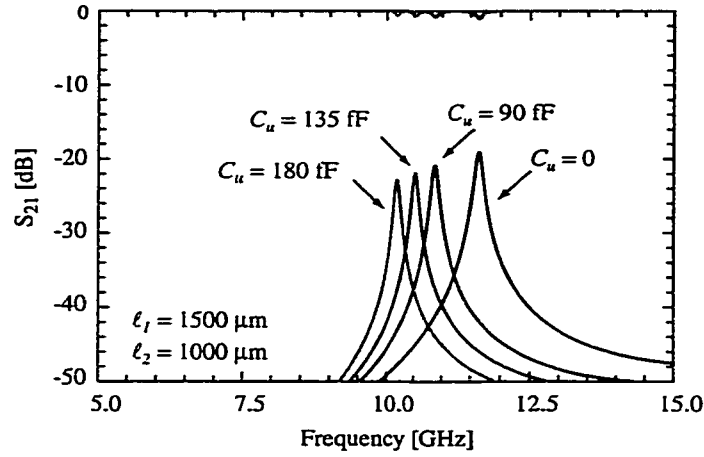


Figure 7.10: Simulated S_{21} for a $5000 \mu\text{m}$ long CPW resonator symmetrically loaded $1500 \mu\text{m}$ from the ends with two MEMS varactors.

to resonator is relatively weak, the Q of the resonator is not altered. Circuits like the one in Fig. 7.9 are under fabrication and the measurements will be presented in a later paper.

7.5.2 Switched Mode Resonator

The variable resonator above can be changed to a switched frequency resonator by using integrated the switched state varactors described above or by using capacitors between the standard MEMS switches and the ground planes. The total capacitance to ground is now the series combination of the MEMS switch capacitance and the integrated capacitors and is given by

$$C_t = \frac{C_b C_s}{C_b + C_s} \quad (7.2)$$

where C_b is C_u or C_d depending on the state of the switch, C_s is the integrated capacitance, and C_t is the total capacitance to ground. For large values of C_d , the total capacitance to ground (C_t) is determined by the value of C_s . This gives precise control over the resonator loading and the corresponding resonant frequency shift. Several designs like this are under fabrication and the measurements will be presented in later publications.

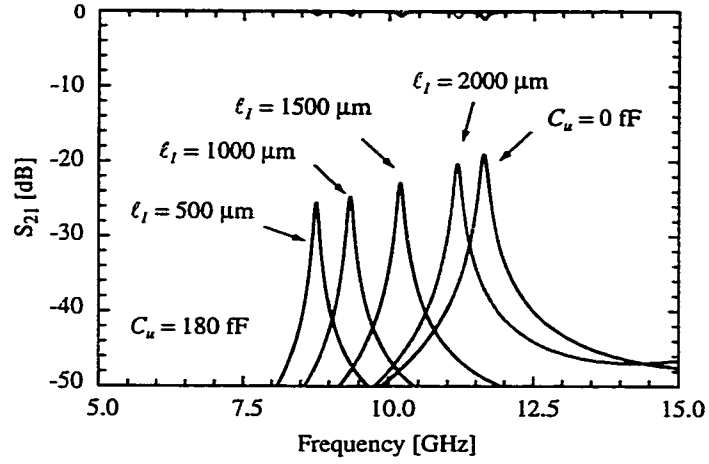


Figure 7.11: The variation in the resonant frequency with loading point is shown for a $5000 \mu\text{m}$ long CPW resonator symmetrically loaded with two MEMS varactors with a capacitance of $C_u = 180 \text{ fF}$.

7.5.3 Inter-resonator Coupling Structures

Designs of sophisticated tunable filters necessitates the variation of the inter-resonator coupling. A simple inter-resonator coupling structure is shown in Fig. 7.12. It is a simple variation of the All-metal series switch, in this case used as a varactor.

7.6 Tunable Oscillators

The tunable varactors and resonators described above can be implemented in tunable and switched state oscillators. Dr. Laurent Dussopt and the author are currently designing, building and testing tunable oscillators using tunable resonators in Section 7.5.2. The some of the resonator designs are similar to the work of Dr. Andy Brown where a reflection type oscillator was designed with planar high-Q resonator loading the gate of the transistor [45]. The planar resonators are loaded with varactors to shift the resonant frequency of the oscillator. Investigations of the noise due to the loading varactors will also be completed.

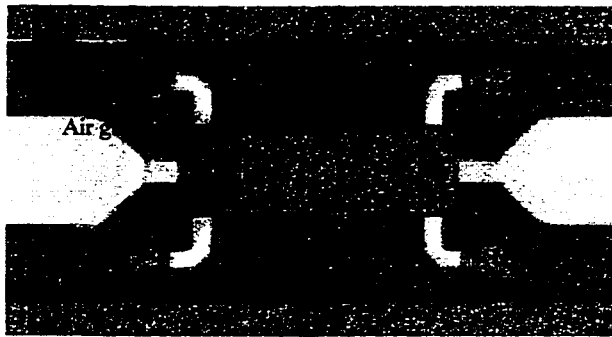


Figure 7.12: Photomicrograph of a proposed inter-resonator MEMS variable coupler.

7.7 Packaging

For RF MEMS devices to become commercially available, packaging techniques that are affordable and reliable must be developed. Because most RF MEMS devices need inert gasses (N_2) and very low moisture environments, near hermetic seals must be maintained for the life of the switch. Many of the current methods use epoxies and other chemicals that will out-gas contaminants and particles into the packaged environment that can adversely effect the performance and reliability of MEMS switches.

APPENDICES

APPENDIX A

FABRICATION PROCESSES

This appendix presents detailed fabrication processes for the series and shunt MEMS switches presented in this thesis. Most of the processing is done on silicon or quartz wafers in a class 100 clean room at the University of Michigan. Most of the devices described in this thesis are fabricated using thin-film metal membranes. The development of stress balanced membranes for MEMS switches has been a coordinated effort of Joseph Hayden, Guan-Leng Tan, and Jeremy Muldavin (author), all at the University of Michigan. The specifics of this development will be covered in the work of Joseph Hayden.

A.1 Description of Terms

While there are numerous techniques and processes involved in micro-fabrication and micro-machining, only the most common techniques used in the fabrication of RF MEMS devices will be outlined here. The following is a list of common terms and techniques, listed under the general categories of patterning, deposition, and etching.

1. Photo-lithographic patterning:

- (a) **mask maker**: a device which selectively exposes small apertures onto the surface of photosensitive masking plate.
- (b) **photo-mask**: a patterned layer of material that is opaque to light and is used to pattern photo-sensitive material on the surface of a wafer. A typical photo-mask consists of a glass plate with a reflective chrome surface and coated with

photoresist.

- (c) **photo-resist:** a light sensitive material that is deposited on the surface of a wafer. Depending on the polarity of the photoresist, when an area of the photoresist is exposed to UV light, it can either be removed or preserved while the unexposed areas are either preserved or removed, respectively, during the developing process. Positive photo-resist is removed after exposure and negative PR remains after exposure.
- (d) **image reversal photo-resist:** a special type of negative photo-resist that reverses its polarity after a second exposure. This process creates a special profile or lip at the edge of the resist pattern that is advantage for use in lift-off techniques.
- (e) **mask aligner:** a device which aligns a photomask to an existing pattern on a wafer. It then exposes the aligned mask and wafer with UV light, transferring the pattern from the mask to the photoresist.
- (f) **developer:** a chemical solution that will selectively remove exposed or unexposed areas of photoresist, depending on the polarity of the resist. These developers are often matched to a specific type and brand of photoresist.
- (g) **acetone:** a strong chemical solvent capable of completely removing or stripping most photoresist materials from a wafer or mask.
- (h) **IPA:** (iso-propoyl alcohol) is a solvent used to clean the surface of a wafer. It is often used to remove traces of acetone and photo-resist after stripping the resist in acetone.
- (i) **soft bake:** heating step to partially remove solvent from photoresist before aligning and exposing a wafer.
- (j) **hard bake:** heating step to solidify photoresist after the it has been developed.

2. Material deposition:

- (a) **electron beam evaporator:** a device which uses a high energy beam to evaporate materials form a source crucible. The evaporated materials are ejected from

the surface of the crucible and deposited in a thin film on the surface of a wafer. Common source materials include: Au, Al, Ti, Cr, Ag, Pt, NiCr, and Cu. These materials are often deposited in a lift-off process where photoresist protects areas of the wafer from direct deposition. The metal deposited on the photoresist is then removed when the photoresist is stripped from the wafer in acetone.

- (b) **sputtering tool:** a device which uses a high energy plasma to eject particles from a source target and then redeposit the particles on the surface of a wafer. The source particles are ejected from the plasma in random directions, ensuring a conformal coating of a surface. The plasma, a mixture of charged particles and electrons, can be excited using a direct current (DC) or a radio frequency (RF) source. DC plasmas are often used to deposit metals such as Au, Al, Ti, Cr, and Cu. RF plasmas are used to deposit metal and dielectric materials such as Si, SiO₂, SiN, SiCr, and TaN.
- (c) **LPCVD:** (low pressure chemical vapor deposition) a technique used to deposit or grow oxide or nitride materials on the surface of a wafer. This often occurs in a high temperature furnace with controlled gaseous environments and is used to create high quality SiO₂ and SiN films.
- (d) **PECVD:** (plasma enhanced chemical vapor deposition) a technique that uses an RF plasma with specific gaseous mixtures to deposit materials on the surface of a wafer. This process is often used to deposit dielectric films such as SiO₂ and SiN.

3. Etching techniques:

- (a) **wet chemical etching:** the use of wet chemical agents to selectively etch a material from the surface of a wafer. Common etchants include Au etchant, copper etchant, Ti etchant, HF and BHF to etch oxide and Ti films.
- (b) **plasma etching:** a technique that uses an RF plasma and chemical etching to remove materials from the surface of a wafer. This technique is often used to etch SiO₂ and SiN films.

4. Release:

- (a) **sacrificial layer:** a layer of material that separates a deposited layer from underlying layers to create vertical gaps between the layers. The sacrificial layer is then removed to release portions of the top layer from the underlying layers.
- (b) **CPD:** (critical point dryer) a device which allows the release of MEMS devices from their sacrificial layers without collapse due to surface tension of wet chemical etchants. This device consists of a chamber that fills with liquid CO₂ which mixes with and purges the wet chemicals from around the MEMS devices. The chamber is pressurized and heated to the critical point of CO₂, in which CO₂ exists as a liquid and a vapor simultaneously. The pressure is then lowered slowly and the liquid is converted directly to a vapor. This eliminates the collapse of the devices due to liquid surface tension.

A.2 Specific Processes

Below are listed specific processes used in the fabrication of the MEM switches in this thesis.

A.2.1 Electroplated Membranes

Wafers are 400 μm thick high-resistivity (3000 $\Omega\text{-cm}$) double-side polished silicon wafers with 6000-8000 \AA SiO₂ on both sides. All processing is single-sided.

1. Wafer clean

- (a) Soak in Acetone for 5 minutes.
- (b) Soak in Isopropyl Alcohol (IPA) for 5 minutes.
- (c) Dry with nitrogen (N₂) air gun.

2. First Metallization layer (lift-off)

- (a) Spin adhesion promoter HMDS for 30 seconds at 2.5 krpm.
- (b) Spin image reversal photoresist AZ 5214 for 30 seconds at 2.5 krpm.

- (c) Softbake 105 °C for 1.5-2 minutes.
- (d) Align to circuit metallization mask and expose for 4.5 seconds at 20 mW/cm².
- (e) Image reversal bake at 130 °C for 1-1.5 minutes.
- (f) Flood expose (no mask) for 1.5 minutes at 20 mW/cm².
- (g) Develop in AZ 327 developer for 40-60 seconds.
- (h) Rinse and dry with nitrogen (N₂) air gun.
- (i) Examine edge profile under microscope.
- (j) Evaporate Cr/Au (500/4000 Å) or Ti/Au.
- (k) Soak samples in Acetone, overnight, for metallization liftoff.
- (l) Soak samples in IPA for clean.
- (m) Dry with nitrogen (N₂) air gun.

3. Sacrificial Layer Deposition

- (a) Spin adhesion promoter HMDS for 30 seconds at 3 krpm.
- (b) Spin positive photoresist 1813 for 30 seconds at 3 krpm.
- (c) Softbake 105 °C for 1 minute.
- (d) Align to circuit metallization mask and expose for 6 seconds at 20 mW/cm².
- (e) Develop in MF 351 developer for 40 seconds.
- (f) Rinse and dry with nitrogen (N₂) air gun.
- (g) Examine circuit pattern under microscope.
- (h) Hard bake 130 °C for 1-1.5 minutes.

4. Bridge and Circuit Metallization (electro-plating)

- (a) Evaporate electro-plating seed layer Cr/Au/Cr (500/1000/500 Å).
- (b) Spin adhesion promoter HMDS for 30 seconds at 3 krpm.
- (c) Spin positive photoresist 1827 for 30 seconds at 3 krpm.
- (d) Softbake 105 °C for 1 minute.

- (e) Align to circuit metallization mask and expose for 12 seconds at 20 mW/cm^2 .
- (f) Develop in MF 351 developer for 40 seconds.
- (g) Rinse and dry with nitrogen (N_2) air gun.
- (h) Examine circuit pattern under microscope.
- (i) Etch Chrome in fresh Chrome etchant for 30 seconds.
- (j) Examine gold circuit profile under microscope
- (k) Electroplate gold (Au) in cyanide-based electroplating solution $1.5\text{--}2 \mu\text{m}$ at low current densities.

5. Sacrificial Layer Removal

- (a) Flood expose sample for 3 minutes at 20 mW/cm^2 to expose resist.
- (b) Develop in MF 351:DI H_2O (1:5) developer for 1 minute.
- (c) Etch Chrome in fresh Chrome etchant for 30 seconds.
- (d) Etch gold (Au) seed layer in fresh TFA gold etchant for 40 seconds.
- (e) Etch Chrome in fresh Chrome etchant for 30 seconds.
- (f) Remove lower layer of photoresist by soaking in hot PRS2000 for 30 minutes.
- (g) Rinse in DI H_2O for 5 minutes.
- (h) Soak in Acetone for 5 minutes.
- (i) Soak in IPA for 5 minutes
- (j) Dry with nitrogen (N_2) air gun.

6. SiO_2 dielectric removal in Slot/Aperture Regions

- (a) Etch oxide in buffered hydrofluoric acid (BHF) for 7.8 minutes (1000 \AA/min etch rate).
- (b) Soak in Acetone for 5 minutes.
- (c) Soak in IPA for 5 minutes
- (d) Dry with nitrogen (N_2) air gun.

A.2.2 Integrated Resistors

1. TaN resistors (More detailed information given in dissertation of Brown [45].) (side 1)
 - (a) Clean sample in Acetone and IPA.
 - (b) Reactively sputter 700 Å of Ta₂N with sputtering pressure of 1 mtorr, a nitrogen ratio of 10%, and 3 Amp current for 2.5 minutes. This should result in 43 Ω/sq sheet resistance.
 - (c) Sputter W/Ti (5%) for 1 minute at 650 W in an Argon ambient at 7 mtorr, which should yield 100 Å.
 - (d) Spin 1813 PR for 30 sec at 3.5 krpm.
 - (e) Softbake 105 °C for 1 minute.
 - (f) Align and expose corners with edge bead removal mask for 30 seconds at 20 mW/cm².
 - (g) Develop in MF 351 developer for 40 seconds.
 - (h) Align TaN mask and expose for 6 sec. at 20 mw/cm².
 - (i) Develop in MF 351 developer for 30 seconds.
 - (j) Rinse and dry with nitrogen (N₂) air gun.
 - (k) Examine circuit pattern under microscope.
 - (l) Descum in plasma asher for 1 minute at 80 W, 250 mT in O₂ plasma.
 - (m) Hardbake 130 °C for 1.5 minutes.
 - (n) Etch exposed W/Ti and Ta₂N in Semi-Group Reactive Ion Etcher (RIE). The etch is in an SF₆:Ar plasma with gas flows of 10 sccm and 5 sccm, respectively. The other etch parameters are 10 mtorr for 5 minutes at 100 W.
 - (o) Etch the top of the photoresist film to remove organic residue in plasma asher for 1 minute at 80 W, 250 mT in O₂ plasma.
 - (p) Soak in ACETONE to remove resist.

- (q) Soak in IPA.
 - (r) Dry with nitrogen (N_2) air gun.
2. NiCr resistors Before depositing NiCr evaporate NiCr on glass slide and measure surface resistance with 4 point probe.
- (a) Spin adhesion promoter HMDS for 30 seconds at 4.5 krpm.
 - (b) Spin image reversal photoresist AZ 5214 for 30 seconds at 4.5 krpm.
 - (c) Softbake 105 °C for 2 minutes.
 - (d) Align edge bead removal mask and expose for 1 minute at 20 mW/cm².
 - (e) Develop in AZ 327 developer for 40 seconds.
 - (f) Dehydrate bake 105 °C for 2 minutes.
 - (g) Align to NiCr resistor mask and expose for 5 seconds at 20 mW/cm².
 - (h) Image reversal bake at 130 °C for 1 minute.
 - (i) Flood expose (no mask) for 1.5 minute at 20 mW/cm².
 - (j) Develop in AZ 327 developer for 40 seconds.
 - (k) Rinse and dry with nitrogen (N_2) air gun.
 - (l) Examine edge profile under microscope.
 - (m) Evaporate NiCr at 42 Ω /square (400 Å).
 - (n) Soak samples in hot PRS2000 for liftoff (10-15 min).
 - (o) Soak samples in DI H2O quench.
 - (p) Soak samples in Acetone for clean.
 - (q) Soak samples in IPA for clean.
 - (r) Dry with nitrogen (N_2) air gun.

A.2.3 SiCr Bias Lines

1. SiCr resistors (about 700-900 Ω per square)
- (a) Spin adhesion promoter HMDS for 30 seconds at 4.5 krpm.

- (b) Spin image reversal photoresist AZ 5214 for 30 seconds at 4.5 krpm.
- (c) Softbake 105 °C for 2 minutes.
- (d) Align edge bead removal mask and expose for 1 minute at 20 mW/cm².
- (e) Develop in AZ 327 developer for 40 seconds.
- (f) Dehydrate bake 105 °C for 2 minutes.
- (g) Align to NiCr resistor mask and expose for 5 seconds at 20 mW/cm².
- (h) Image reversal bake at 130 °C for 1 minute.
- (i) Flood expose (no mask) for 1.5 minute at 20 mW/cm².
- (j) Develop in AZ 327 developer for 40 seconds.
- (k) Rinse and dry with nitrogen (N₂) air gun.
- (l) Examine edge profile under microscope.
- (m) Clean sample in Acetone and IPA.
- (n) Reactively sputter 1000 Å of SiCr with sputtering pressure of 7 mtorr, a nitrogen ratio of 10%, and 3 Amp current for 2.5 minutes. This should result in 700-900 Ω/sq sheet resistance.
- (o) Soak in ACETONE to remove resist and unwanted SiCr.
- (p) Soak in IPA.
- (q) Dry with nitrogen (N₂) air gun.

A.2.4 Sputtered Bridge Process

1. Sacrificial Layer Deposition

- (a) Spin adhesion promoter HMDS for 30 seconds at 3 krpm.
- (b) Spin positive photoresist 1813 for 30 seconds at 3 krpm.
- (c) Softbake 105 °C for 1 minute.
- (d) Align to circuit metallization mask and expose for 6 seconds at 20 mW/cm².
- (e) Develop in MF 351 developer for 40 seconds.

- (f) Rinse and dry with nitrogen (N₂) air gun.
- (g) Examine circuit pattern under microscope.
- (h) 130 °C for 1-1.5 minutes.

2. Bridge and Circuit Metallization (sputtering)

- (a) Sputter Ti/Au/Ti (500/8000/500 Å).

3. Anchor Electroplating

- (a) Spin adhesion promoter HMDS for 30 seconds at 3 krpm.
- (b) Spin positive photoresist 1827 for 30 seconds at 3 krpm.
- (c) Softbake 105 °C for 1 minute.
- (d) Align to circuit metallization mask and expose for 12 seconds at 20 mW/cm².
- (e) Develop in MF 351 developer for 40 seconds.
- (f) Rinse and dry with nitrogen (N₂) air gun.
- (g) Examine circuit pattern under microscope.
- (h) Etch Ti in fresh Chrome etchant for 30 seconds.
- (i) Examine gold circuit profile under microscope
- (j) Electroplate gold (Au) in cyanide-based electroplating solution 1.5-2 μm at low current densities.

4. Bridge Patterning

- (a) Flood expose sample for 3 minutes at 20 mW/cm² to expose resist.
- (b) Develop in MF 351:DI H₂O (1:5) developer for 1 minute.
- (c) Spin adhesion promoter HMDS for 30 seconds at 3 krpm.
- (d) Spin positive photoresist 1827 for 30 seconds at 3 krpm.
- (e) Softbake 105 °C for 1 minute.
- (f) Align to bridge pattern mask and expose for 12 seconds at 20 mW/cm².
- (g) Develop in MF 351 developer for 40 seconds.

- (h) Rinse and dry with nitrogen (N_2) air gun.
- (i) Examine circuit pattern under microscope.
- (j) Etch Ti in fresh BHF for 30 seconds.
- (k) Examine gold circuit profile under microscope
- (l) Etch Chrome in fresh Chrome etchant for 30 seconds.
- (m) Etch gold (Au) seed layer in fresh TFA gold etchant for about 2 minutes.
- (n) Etch Ti in fresh BHF for 30 seconds.
- (o) Remove lower layer of photoresist by soaking in hot PRS2000 for 30 minutes.
- (p) Rinse in DI H_2O for 5 minutes.
- (q) Soak in Acetone for 5 minutes.
- (r) Soak in IPA for 5 minutes.
- (s) Dry with CPD machine.

APPENDIX B

PRELIMINARY WORK

B.1 Micro-machined Tapered Slot Antennas

B.1.1 Introduction

Tapered Slot Antennas (TSA) have been developed by Gibson et. al [46] and Yngvesson et. al [47, 48] for phased array and focal plane imagin systems. The performance of a TSA is sensitive to the thickness and dielectric constant of the antenna substrate. An *effective thickness*, which represents the electrical thickness of the substrate, has been defined as $t_{eff} = t(\sqrt{\epsilon_r} - 1)$. One accepted range of the effective thickness (determined experimentally) for good operation of a TSA is given as $0.005\lambda_o \leq t_{eff} \leq 0.03\lambda_o$ [47]. For substrate thickness above the upper bound of effective thickness, unwanted substrate modes develop which degrade the performance of the tapered slot antenna, while antennas on thinner substrates suffer from decreased directivity.

The upper bound on the effective thickness, $t_{eff} \leq 0.03\lambda_o$, necessitates mechanically thin substrates for mm-wave applications, even if low dielectric constant materials are used. For example, a maximum thickness of 200 μm (8 mils) is allowed for a 94 GHz TSA integrated on an $\epsilon_r = 2.2$ dielectric substrate. This results in a mechanically fragile substrate.

One way of improving the mechanical stability is to increase the thickness of the substrate and then selectively remove parts or nearly all of the underlying dielectric material. If nearly all of the substrate is removed, the TSA can be suspended on a thin dielectric membrane with an effective dielectric constant of $\epsilon_r = 1.05$ [49]. This is easily implemented

at sub mm-wave frequencies (300 GHz-3 THz), but is not as practical at mm-wave frequencies (30-300 GHz) since the membrane dimensions are large and the mechanical stability of the suspended membrane is compromised. Other researchers (Vowinkel et al [50]) have selectively removed large portions of the dielectric inside the slot area of the TSA with good results.

Another method commonly used at mm-wave frequencies is the integration of the radiating antenna on a thin (4-8 mil) low dielectric substrate with $\epsilon_r = 2.2$ backed by a thick foam substrate with a dielectric constant of less than 1.1 [51, 52]. While this is excellent at 20-100 GHz, the thin dielectric substrate will interfere with the radiation patterns of Tapered Slot Antennas at frequencies greater than 100 GHz. Therefore, it is advantageous to develop a technique to further reduce the dielectric constant of the dielectric support substrate.

In this work, an array of closely drilled holes is used to remove a portion of the underlying substrate, thereby resulting in a lower quasi-static (effective) dielectric constant substrate. This technique has been applied successfully using microstrip antennas [53]. The volume of the dielectric removed can be precisely controlled (between 0-100%) and determines the effective dielectric constant of the substrate. In this application, around 40-50% of the substrate is removed to maintain good mechanical properties.

B.1.2 30 GHz Design & Measurements

LTSA Design

A non-optimal linear tapered slot antenna design, shown in figure B.1, was chosen for the 30 GHz experiments. The LTSA was designed to be $4\lambda_o$ long with a 12° taper angle, which results in nearly one λ_o aperture. The slotline feed was 200-300 μm wide. The substrate is 1.27 mm (50 mils) thick RT/duriod, with a relative dielectric constant of $\epsilon_r = 2.2$. Three different substrates were investigated: *solid substrate*, *big hole substrate*, and *small hole substrate*. The big hole and small hole patterns, shown in figure 2, were machined in a 45-degree rotated rectangular lattice with an automated milling machine. The big hole substrate was chosen to be a large fraction of a wavelength with $D = \lambda_o/3$ (3.18 mm) and

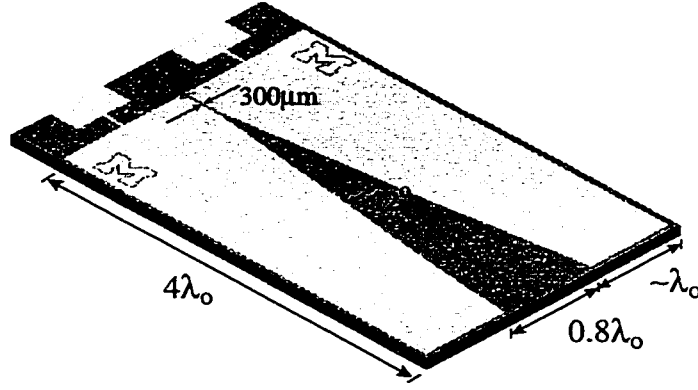


Figure B.1: The linear tapered slot antenna on a 1.27 mm thick RT/durioid ($\epsilon_r = 2.2$) substrate. The pads on the end of the antenna are for low frequency signal pickup.

$W = \lambda_o/2$ (5.08 mm). The small hole pattern was chosen with $D = \lambda_o/8$ (1.27 mm) and $D = \lambda_o/5$ (2.03 mm). Previous measurements at 10 and 30 GHz have shown that the lattice choice (rectangular, hexagonal, etc.) has no effect on the far field patterns for low dielectric constant substrates [54].

The machined substrates were chosen to have the same effective relative dielectric constant. The effective dielectric constant is a quasi-static value, given by the volumetric average dielectric constant of the machined substrate, and is: $\epsilon_{eff} = \frac{\pi}{2}(\frac{D}{W})^2 + \epsilon_r[1 - \frac{\pi}{2}(\frac{D}{W})^2]$, where D and W are defined in figure B.2.

For RT/durioid, with $\epsilon_r = 2.2$, the effective dielectric constant, ϵ_{eff} , is equal to 1.46 for the two machined substrates shown in figure B.2. For a 30 GHz TSA integrated on 1.27 mm (50 mils) thick substrate, this reduction in the effective dielectric constant changes the value of t_{eff}/λ_o from 0.061 for the solid substrate to 0.026 for the machined substrates, placing the effective thickness just within the performance limits of Yngveson et al [47].

30 GHz Measurements

The normalized radiation patterns of the antennas were measured in an anechoic chamber. The thin leads and the pads on the slot end of the antenna (Fig. B.1) were designed to allow pickup of low frequency signals from a zero-bias Schottky diode (Metelics MSS20141-

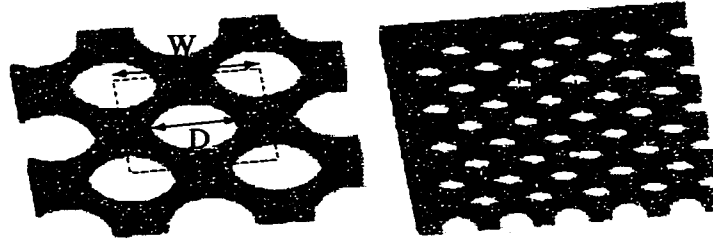
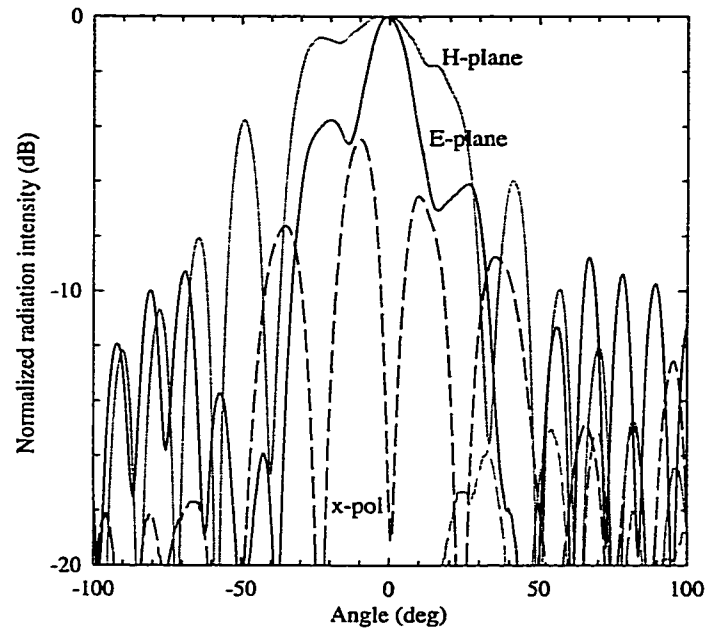


Figure B.2: Hole patterns machined into the substrates of the 30 GHz tapered slot antennas. The larger pattern has a hole diameter, D , of 3.18 mm (125 mils), and a spacing, W , of 5.08 mm (200 mils). The smaller pattern has a hole diameter of 1.27 mm (50 mils), and a spacing of 2.03 mm (80 mils). The dashed box represents the unit cell.

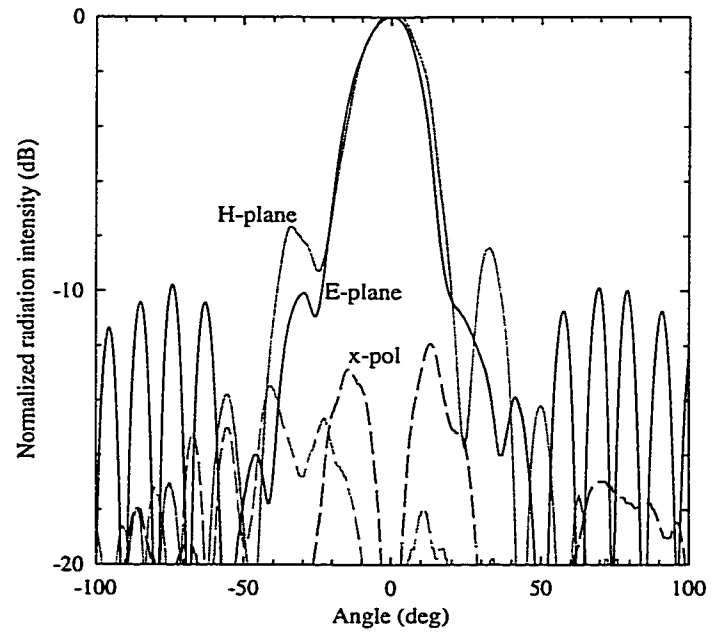
B10D, $C_t = 0.8$ pF) placed over the slot line of the antenna, one quarter of a guided wavelength from a capacitive RF short. The RF source was AM modulated at 5 kHz and radiated by a standard gain horn. The detected low frequency signal (5 kHz) at the diode terminals was delivered to a lock-in amplifier. The amplified signal was then read by a computer, which controlled the antenna mount positioner.

The 30 GHz far field radiation patterns of the solid substrate and the big hole substrate antennas are shown in figure B.3. There was significant improvement in the far field patterns of both the E- and H-plane with the machined substrates. Note the lower cross-polarization levels in the E- and H-plane patterns for the machined big hole antenna. No directivity values are quoted since the 45-plane co- and cross-polarization patterns were not measured. The big hole and the small hole tapered slot antennas gave very similar patterns to within $\pm 1^\circ$ and ± 1 dB (Fig. B.4). This indicates that the improvement in performance is independent of hole geometry even if the holes/periods are a large fraction of a wavelength. This further suggests that the effect is purely a quasi-static reduction of the substrate dielectric constant, and not a mode suppression/photonic bandgap mechanism typically seen in high dielectric constant substrates [55].

The 3-dB and 10-dB beamwidths for all three antennas are summarized in Table B.1. Notice the fine structure (or ripple) in the measured patterns at angles above $\pm 40^\circ$. This is believed to be an interference pattern from the measurement setup and the edge of the

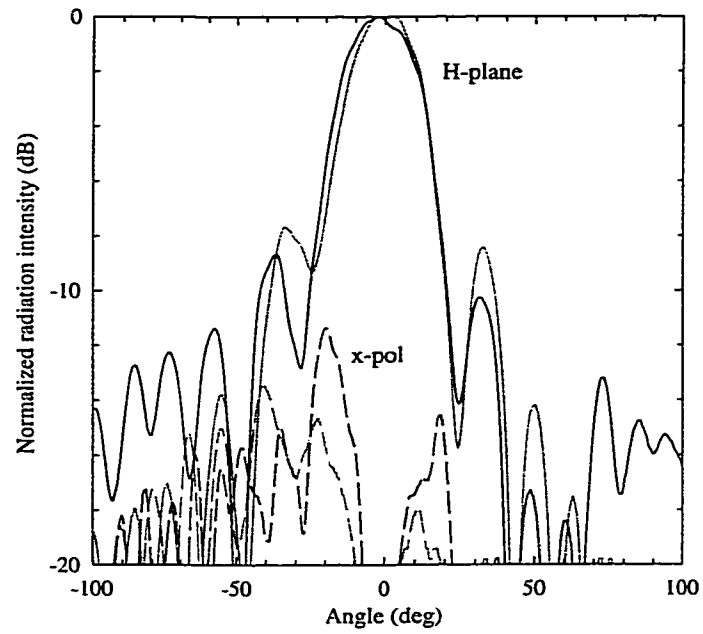


(a)

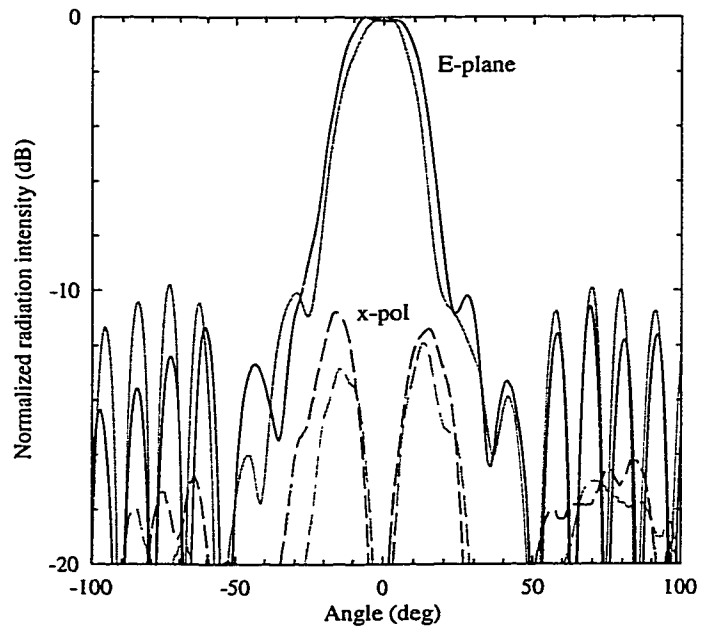


(b)

Figure B.3: Measured 30 GHz far field antenna patterns for the solid substrate (a) and the big hole LTSA(b).

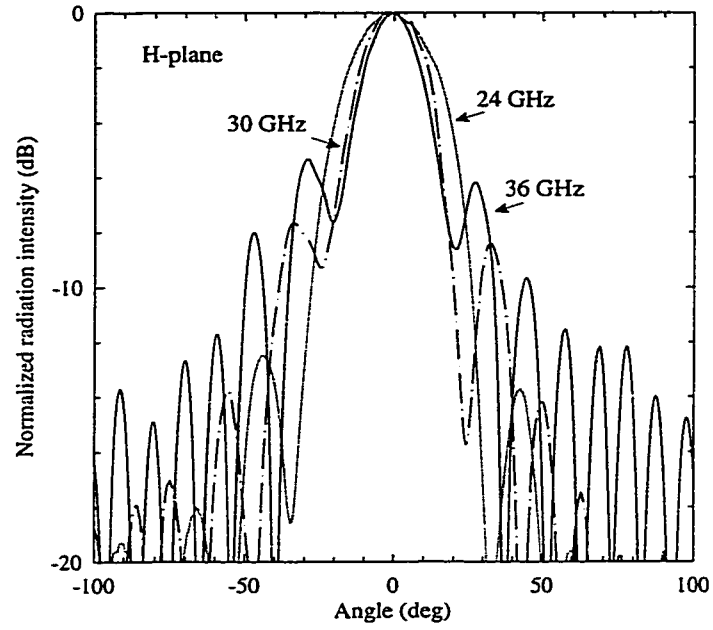


(a)

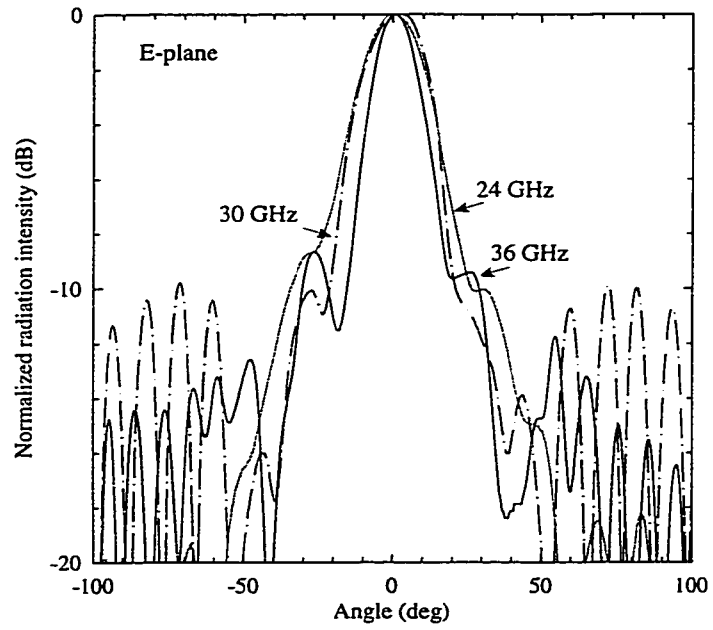


(b)

Figure B.4: Measured 30 GHz H-plane (a) and E-plane (b) far field antenna patterns for the big hole (gray) and small hole LTSA (black).



(a)



(b)

Figure B.5: Measured 24 (gray), 30 (dash-dot) and 36 GHz (solid) H-plane (a) and E-plane (b) far field co-polarization antenna patterns for the big hole LTSA.

Antenna	3-dB		10-dB	
	E-plane	H-plane	E-plane	H-plane
Solid substrate	17	54	66	67
Big/small hole	25	26	42	43

Table B.1: Comparison of the 3-dB and 10-dB beamwidths for three different 30 GHz TSA substrates.

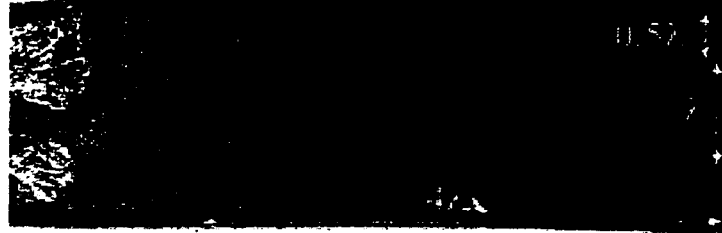
TSA substrate. Recently, Sugawara et al. have shown that TSA patterns are very sensitive to currents induced on the edge of the finite-width substrate. These edge currents are in opposite phase to the slot-antenna currents and result in interference-like patterns at large measurement angles [56]. The big hole antenna results in symmetrical patterns at 30 GHz, and for a 10-dB taper in an imaging lens system, the antenna will fit an $f/1.25$ lens.

A comparison of the measured 24, 30, and 36 GHz far field radiation patterns for the big hole antenna is shown in figure 5. The backside radiation patterns ($|\theta| \geq 90^\circ$) were below -15 dB. The peak cross-polarization levels were below -12.5, -10.5, and -8.5 dB at 24, 30, and 36 GHz, respectively. The corresponding patterns of the small hole LTSA are virtually identical and are not shown. As the frequency increases, the beamwidth decreases, the side lobe levels increase, and the patterns degrade as the effective thickness increases (as expected). Note that even at 36 GHz with $D = \lambda_o/2.5$ and $W = \lambda_o/1.6$, the big hole TSA gave virtually identical patterns to the small hole TSA with $D = \lambda_o/6.3$ and $W = \lambda_o/4$.

B.1.3 94 GHz Design & Measurements

94 GHz Design

A constant width tapered slot antenna design, provided by Dr. Ellen Moore at Millimetrix Corporation, was used for the 94 GHz experiments (Fig. B.6). In order to obtain an effective thickness of $t_{eff} \leq 0.03\lambda_o$ at 94 GHz, the solid substrate thickness must be less than 200 μm , resulting in a mechanically unstable substrate. Increasing the thickness to 380 μm (15 mils) improves the mechanical stability to a practical level. We compared 380 μm thick solid substrate antennas to antennas machined with a hole pattern, shown in



(a)



(b)

Figure B.6: Front-side conductor pattern (a) and back-side hole pattern (b) for the CWSA 94 GHz antenna. The antenna aperture is approximately λ_o , and the length is approximately $4\lambda_o$. The hole diameter is $380 \mu\text{m}$ and the unit cell width is $610 \mu\text{m}$.

figure B.2, having a diameter of $380\text{ }\mu\text{m}$ ($\lambda_o/9$) and a spacing of $610\text{ }\mu\text{m}$ ($\lambda_o/5$). In retrospect, these dimensions were chosen to be unnecessarily small and can easily be enlarged by a factor of 2-3. The machining removes approximately 40% of the substrate and again results in an effective dielectric constant of 1.46. The effective thickness of the antenna is reduced from 0.058 to 0.025, again just within the acceptable limits.

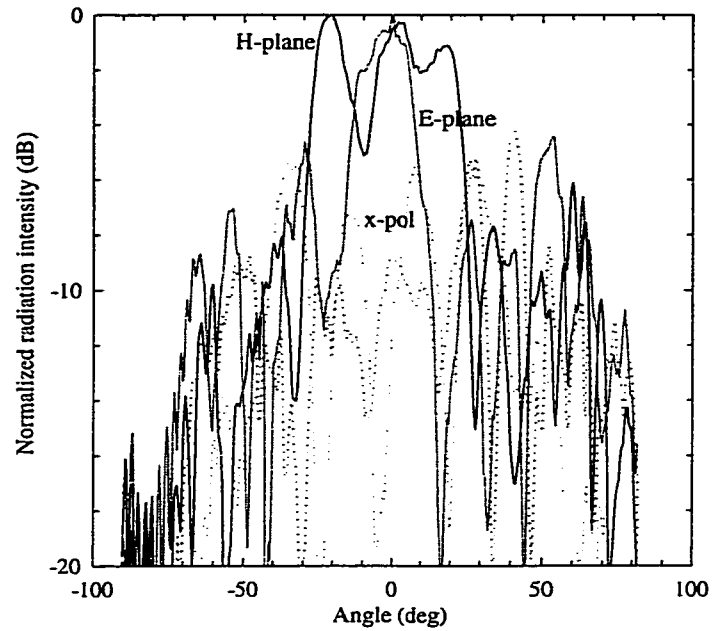
94 GHz Measurements

The 94 GHz measurements were performed on a bench top with absorber placed around the perimeter of the bench. The measurements were performed with an experimental setup similar to the 30 GHz setup, except with an AM modulated 94 GHz Gunn-diode source. An Alpha diode (DMK2784-000, $C_t = 0.04\text{ pF}$), placed across the slot, was used to detect the modulated signal. A signal to noise ratio of greater than 20 dB was achieved.

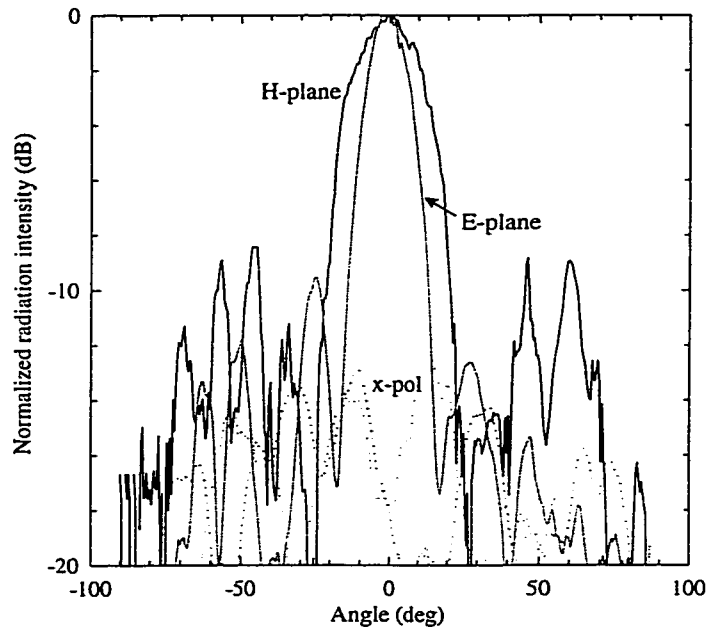
The 94 GHz far field antenna patterns for the solid substrate and the machined CWSA are shown in figure B.7. The CWSA showed excellent pattern improvement for the machined case, with low cross polarization levels (-13 dB). The sharp -10 dB sidelobes are believed to be due to the edge currents on the finite width ($0.5\lambda_o$) conductor half plane. The machined CWSA results in an average -10 dB beamwidth of 35° and fits an $f/1.6$ lens imaging system. It is expected that the antenna patterns will change when placed in a 2-D imaging array, and this is subject to current investigation in our group.

B.1.4 Conclusions

We have shown that selective machining of a thick dielectric substrate results in a simple method for reducing the effective thickness of tapered slot antennas. In contrast to earlier measurements on high-dielectric constant substrates, if low dielectric constant substrates are used, the improved far field radiation patterns are not sensitive to hole geometry or lattice choice (as long as the quasi-static effective thickness remains the same) and can be easily scaled with frequency from 10-94 GHz. A 94 GHz constant width tapered slot antenna on a thick machined substrate ($\epsilon_r = 2.2$) was successfully fabricated, showing mechanical stability and practical radiation performance, for imaging array applications.



(a)



(b)

Figure B.7: Measured 94 GHz solid substrate (a) and machined substrate antenna (b) far field CSWA patterns.

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