RF MEMS DEVICES FOR MULTIFUNCTIONAL INTEGRATED CIRCUITS AND ANTENNAS

by

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This work is dedicated to my family for all their love and sacrifice on my behalf.

Excellence is the result of caring more than others think is wise; risking more than others think is safe; dreaming more than others think is practical and expecting more than others think is possible.

Anonymous

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CHAPTER 1

Introduction

1.1 Motivation

WITH ever-increasing demand for low-cost efficient communications the need for multifunctional, adaptive and low-power systems is on the rise. Furthermore, modern communication networks have to suppress the harmful effects of the interference from other users who share the same channel and the self-interference due to multipath propagation. Additionally, securing the transmitted information from the unintended listeners and alleviating the effects of communication jammers are two equally important issues for the current and the coming generation of the tetherless (terrestrial wireless and satellite) communication systems. All these vital requirements impose significant challenges on the current technology and illustrate the need for new designs and advanced architectures.

Although significant effort has been focused on the development of neoteric modulation techniques and network protocols (spread spectrum channels, CDMA and DSL protocols, new voice over IP protocols, etc.) the RF front-end technology has received significantly less attention up to now [7]. Since the RF front-end is the basic interface between a typical communication system and its environment (see Fig. 1.1), the aforementioned challenges of reconfigurability, spectrum efficiency, security, minia-

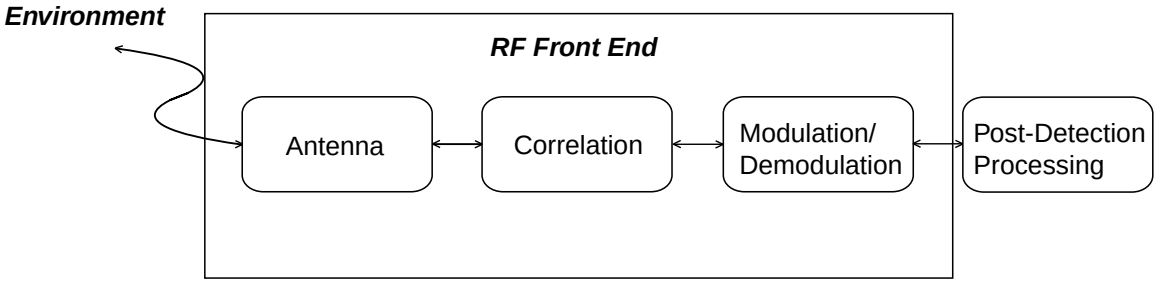


Figure 1.1: RF front-end in a modern communication system architecture.

turization and cost minimization can only be met by ensuring that the RF front-end is comprised of low-energy, low-cost, adaptive and high-performance RF devices. A number of enabling technologies including novel circuit architectures, adaptive and reconfigurable phased antenna arrays, advanced materials and novel integration and packaging methods are required for these type of RF systems. These systems need to be developed for microwave up to sub-millimeter-wave frequencies, since the next generation of the communication networks will be specifically designed in these bands, due to their significant advantages in bandwidth and miniaturization.

The existing technology enables the design and fabrication of all the basic transeiver components (amplifiers, oscillators, mixers, doublers, filters, antennas, switches and so on) on planar substrates. Most of these components that are commercially available are built on the mature well-known semiconductor technology based on diodes and transistors. Although nowadays this technology dominates both analog and digital circuits, a research effort on micromachining and Micro-Electro-Mechanical Systems (MEMS) that could enhance or even replace the existing systems has emerged. Over the past two decades, in particular, MEMS and micromachining have been identified as two of the most significant enabling technologies in developing miniaturized, low-cost and low-energy RF components and systems.

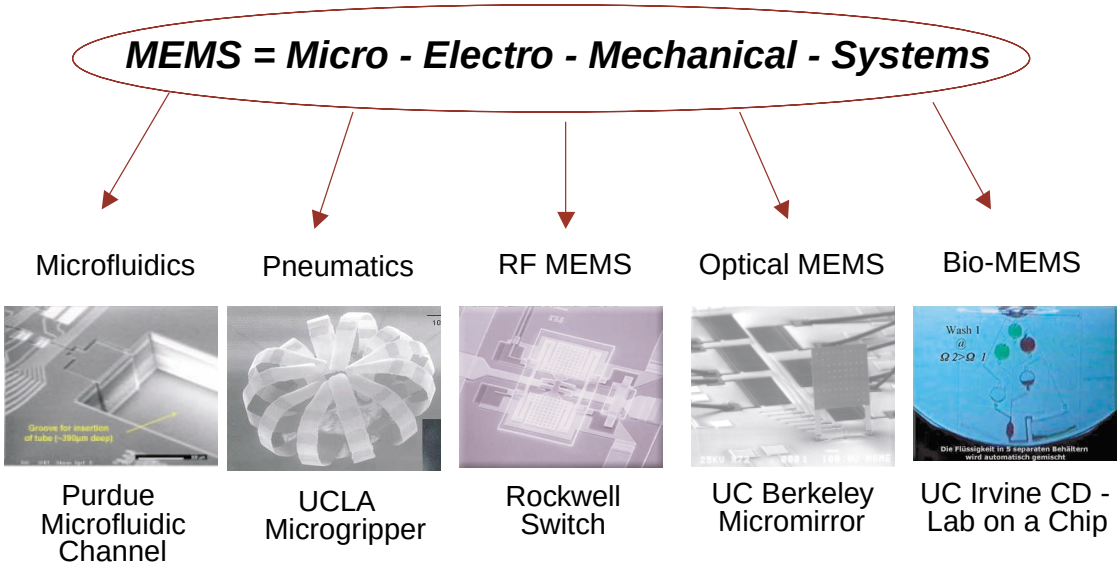


Figure 1.2: Examples of Micro-Electro-Mechanical Systems.

1.2 MEMS Overview

MEMS today is a generic term commonly used in North America[1] to describe microscopic devices that typically involve some sort of mechanical movement. One of the most important aspects of MEMS is that they can be fabricated in large numbers on a single chip (batch fabrication) with processes similar to the ones used in the Integrated Circuits (IC) industry.

MEMS development was initiated in the early 1980s and was based on the well-understood properties of Silicon related to surface and bulk micromachining [8, 9]. The first MEMS structures were primarily relatively simple acceleration, pressure and temperature sensors. Since then, MEMS have been proven to be applicable in almost all areas of engineering systems, such as optical, biological and microwave (Fig. 1.2). MEMS, for example, are already found in commercial applications such as accelerometers in the automotive industry as well as in inkjet printers. The true excitement about MEMS, however, still lies in the Research and Development (R&D)

[1]Microsystems Technology is the most common term in Europe, while Micromachines is preferred in Japan.

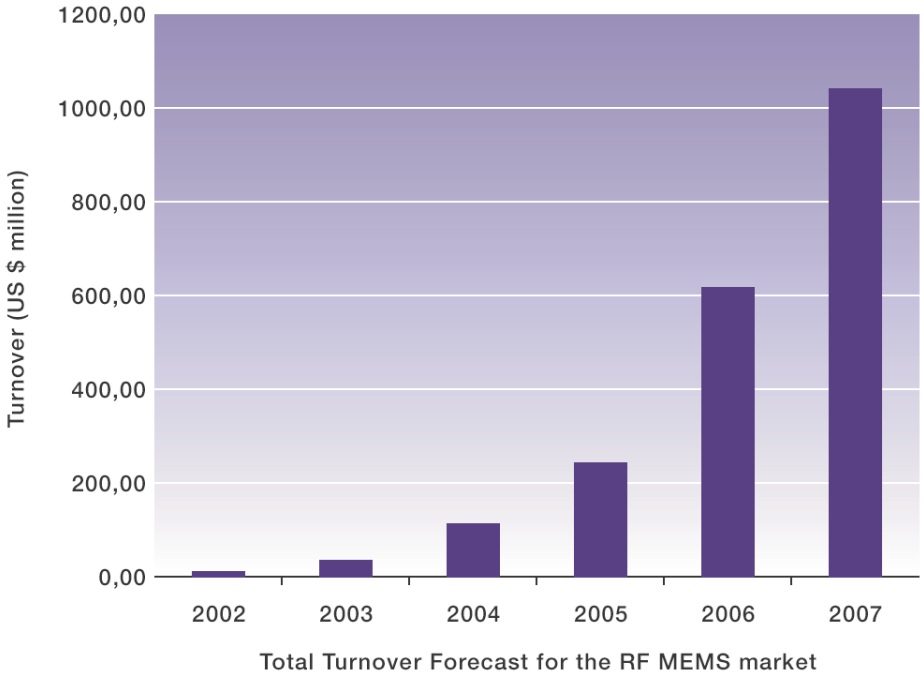


Figure 1.3: Expected RF MEMS market up to 2007 (after [2]).

area and in a number of different applications. Because of their promising unmatched performance, MEMS have already generated very serious interest that has lead several organizations to complete extensive studies estimating their economic impact for the next five years [10, 2]. One of the most recent studies, estimates this market potential of MEMS to exceed $1 billion by 2007 (Fig. 1.3).

Although this dissertation discusses only some aspects of MEMS for microwave systems (commonly called RF MEMS), the interested reader may find useful information about other types of MEMS in many sources. Profs. Senturia's ([11]) and Madou's ([12]) books are excellent sources. Several web pages mentioned in [12] may also serve as good starting points.

1.3 MEMS for High Frequency Electronics

The most important MEMS device in the RF/microwave arena is undeniably the RF MEMS switch. The RF MEMS switch is a component, which through mechanical movement, achieves an open or short circuit on a transmission line (for a given bandwidth). More generally, the physical mechanical movement of an RF MEMS switch controls the impedance of an RF transmission line.

Petersen [8, 9] was the first to demonstrate the ability to build MEMS switches as simple cantilever beams. At first, only low-frequency MEMS devices were of significant interest, because they could be integrated with CMOS circuits. Therefore, many devices were based on polysilicon, which has excellent mechanical properties [13]. However, with the advent of the microwave technology, it became apparent that a high-resistance material, such as polysilicon, could not be included in low-loss circuits that are necessary in the microwave and millimeter-wave region (1–100 GHz). This led to the development of extremely low-loss metallic MEMS components. Au and Al are the most common materials [4, 14] used for that purpose, while Ni, has also been demonstrated as a potential candidate [15].

RF MEMS switches have been developed in both series and shunt configurations and some of these are discussed in this dissertation. Fig. 1.4 shows examples of series and shunt RF MEMS switches along with their simplified equivalent circuits. These equivalent circuits are obviously neither complete representations of the actual switches, nor can they be employed for any series or shunt switch configuration. Nevertheless, they define important switch parameters (on-state resistance and off-state capacitance for instance) that are commonly used to characterize the performance of an RF MEMS switch. A good series switch, for example, is required to have an on-state resistance (R_{ON}) of less than 1 Ω in order for its on-state insertion loss to be less than 0.1 dB. Extensive discussions of modelling, fabrication and experimental characterization of RF MEMS switches can be found in Chapters 3, 4 and 6.

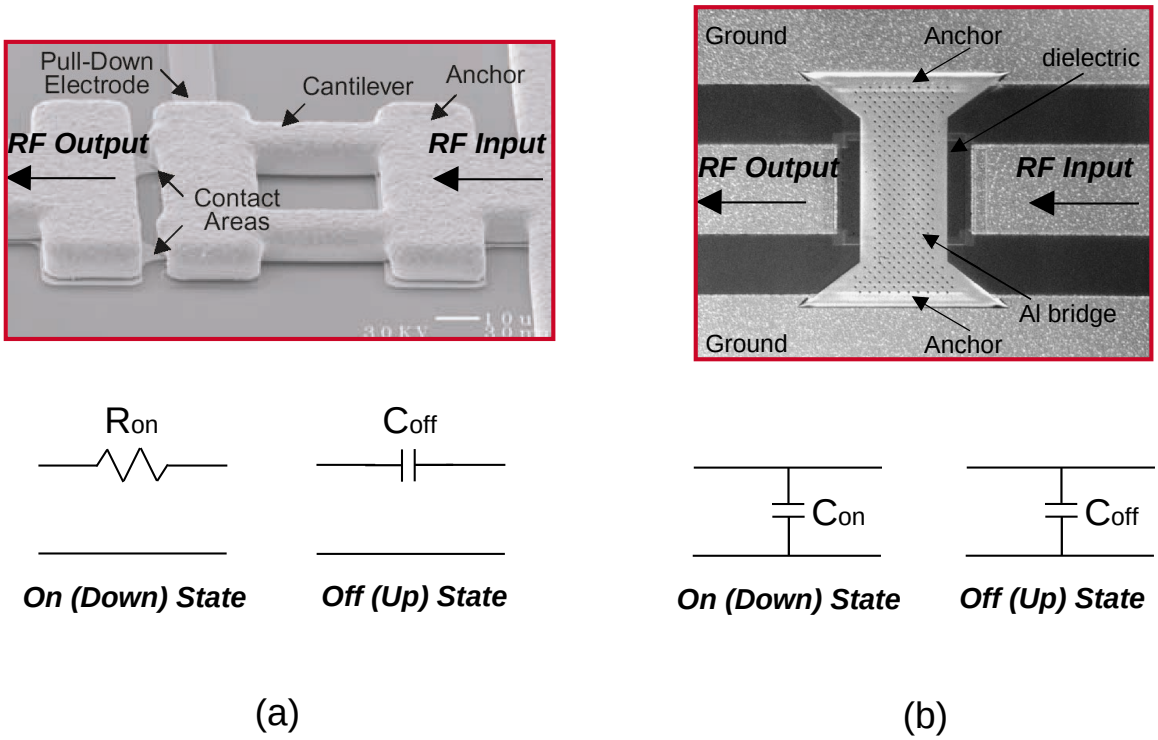


Figure 1.4: (a) Series switch developed by Analog Devices/Northeastern University and a simple equivalent circuit [3]. (b) Shunt switch developed by Raytheon and a simple equivalent circuit [4].

MEMS switches show remarkable advantages over their solid state counterparts (PIN diodes or FET transistors) that make them very attractive for many applications. Table 1.1 [1] compares in a general sense the performance of RF MEMS switches versus common solid-state switches. The first obvious advantage of RF MEMS is that they require very low DC power to operate – except the ones based on thermal actuation mechanisms –, which is in the order of μW as compared to mW for diodes and transistors. However, they typically need higher DC voltage than solid state switches. Moreover, they are characterized by very small series ohmic resistance, on the order of 0.5 to 2 Ω and ultra low series capacitance (less than 10 fF). Their on-state insertion loss is rarely above 0.3 dB and they are capable of providing moderate to high off-state isolation (typically 15–30 dB per switch) even up to 100 GHz. Furthermore, they are much more linear than solid state devices, since they are completely

Table 1.1: Performance comparison of FETs, PIN diodes and RF MEMS electrostatic switches (based on [1]).

Parameter	RF MEMS	PIN	FET
Voltage [V]	20–80[a]	±3–5	3–5
Current [mA]	0	3–20	0
Power Consumption[b] [mW]	0.05–0.1	5–100	0.05–0.1
Switching time	1–300 μsec	1–100 nsec	1-100 nsec
C_{up} (series) [fF]	1–6	40–80	70-140
R_s (series) [Ω]	0.5–2	2–4	4–6
Capacitance ratio[c]	40–500[d]	10	na
Cutoff frequency[e]	20–80	1–4	0.5–2
Isolation (1–10 GHz)	Very high	High	Medium
Isolation (10–40 GHz)	Very high	Medium	Low
Isolation (60–100 GHz)	High	Medium	None
Loss (1–100 GHz) [dB]	0.05–0.3	0.3–1.2	0.4–2.5
Power Handling [W]	<1	<10	<10
Third-order intercept point [dBm]	+66–80	+27–45	+27–45

[a]Actuation voltages as low as 6 V are reported in this work.
[b]Includes voltage upconverter or drive circuitry.
[c]Capacitive switch only
[d]A ratio of 500 is achieved only with very smooth and high-ϵ_r dielectrics
[e]The cutoff frequency f_c is defined as the frequency where the ratio of the off (up-state) capacitance and on (down-state) resistance degrades to unity $f_c = 1/(2\pi C_{up} R_s)$

passive components with no semiconductor junctions. This improves the intermodulation distortion by approximately 30 dB. Since no other technology has been able to match this RF performance, the RF MEMS potential is very promising in a number of commercial (tunable filters, phase shifters, wireless telecommunications switches) and defense (phased arrays, high-performance matching networks) applications.

On the other hand, RF MEMS switches are three orders of magnitude slower than PIN diodes due to inertia. As a result, their switching speed is typically in the order of 1-300 μsec. In addition, special consideration is needed for high power operation. If the RF power is sufficiently high, self actuation of the switch may occur, due to the associated rectified voltage. Chapter 3 discusses these issues in detail. Moreover, MEMS are very sensitive to important environmental factors (humidity, dust, etc.) Consequently, their RF performance, as well as their reliability, can be seriously

degraded in a dirty environment. Packaging, therefore, is essential and it remains an open research area at this day.

1.4 Dissertation Overview

The main objectives of this dissertation are (a) to present the design, fabrication and characterization of novel RF MEMS devices, and (b) to demonstrate neoteric architectures of reconfigurable circuits and antennas suitable for integration with the developed RF MEMS devices. The first MEMS structure, analyzed in Chapters 2 and 3, is a low-voltage switch originally proposed by Pacheco et al. [15]. A significant number of concepts, fabrication techniques, circuits and measurements presented in these chapters have been contributed by Sergio Pacheco and Linda P.B. Katehi. The following is an overview of this thesis chapters that also summarizes the contributions by Sergio Pacheco and Linda P.B. Katehi included in these chapters.

- Chapter 2 reports on the design, fabrication and testing of a low-actuation voltage Micro-Electro-Mechanical switch for high frequency applications. The mechanical design of low spring-constant folded-suspension beams is presented first and switches using these beams are demonstrated with measured actuation voltages of as low as 6 V. Furthermore, common nonidealities such as residual in-plane and gradient stress as well as down-state stiction problems are addressed and possible solutions are discussed. Finally, both experimental and theoretical data for the dynamic behavior of these devices are presented. The results of this chapter clearly underline the need of an integrated design approach for the development of ultra low-voltage RF MEMS switches.

  As already mentioned, the analyzed switch has been first proposed by Sergio Pacheco and Linda P.B. Katehi. Chapter 2 includes several of their findings. In particular, Sergio Pacheco and Linda P.B. Katehi developed the original

switch concept and the required fabrication process (polyimide sacrificial layer, evaporated Ti/Ni seed layer) [15]. Additionally, Sergio Pacheco has fabricated all the MEMS structures used in the actuation voltage and switching speeds measurements and performed all these measurements as well. Part of the in-plane stress analysis included in this chapter (equations (2.12), (2.13), (2.14) and Fig. 2.12) has been also contributed by Sergio Pacheco.

- Chapter 3 presents an experimental and theoretical study of the low-voltage RF MEMS switch discussed in the previous chapter for high power applications. First, the problem of self-actuation due to high RF power is investigated and switches that do not self-actuate or catastrophically fail with a measured RF power of up to 5.5 W are successfully demonstrated. Second, the problem of switch stiction to the down state as a function of the applied RF power is also theoretically and experimentally studied. Finally, a novel switch design with a top electrode is introduced and its advantages with regard to RF power handling capabilities are presented. By applying this technology, we demonstrate hot-switching measurements with a maximum power of 0.8 W. Our results, backed by theory and measurements, illustrate that careful design can significantly improve the power handling capabilities of RF MEMS switches.

  Sergio Pacheco and Linda P.B. Katehi were the first to recognize that the de-coupling of the RF and DC pads significantly increases the switch power handling capabilities [15]. They were also the first to introduce the switch top electrode for increasing the switch's restoring force. Furthermore, the need to extensively study all three scenarios presented in this chapter as well as all the experimental work (MEMS structures and high RF power measurements) have been contributed by Sergio Pacheco.

- Chapter 4 discusses the development of inductively tuned switches and high-isolation switch packets based on the low-voltage switch presented in the previ-

ous chapters. Theoretical and experimental data show that slight modifications in the switch design may result in significant differences in its electrical performance. Measured isolation as high as 30 dB per switch and 2-,3- and 4-switch packets with measured isolation as high as 70 dB are reported.

- Chapter 5 uses the same low-voltage switch as a vehicle to discuss novel techniques of digitally tuning lumped elements that are commonly found in microwave integrated circuits. Examples of tunable shunt capacitors, series inductors and shunt inductors are thoroughly analyzed. This chapter also shows how these tunable lumped elements can be integrated into compact reconfigurable filters with very high tuning ranges. A Chebyshev lowpass filter with 3:1 tuning ratio is demonstrated based on this technique. Furthermore, a novel bandpass filter architecture particularly suited for the switch at hand is introduced. A K-band bandpass filter based on this topology is successfully developed with a measured tuning range of 2:1. Chapter 5 also shows that these results can be further improved if a metal-to-metal contact switch is employed.
- Based on the findings of Chapter 5, Chapter 6 introduces a novel metal-to-metal contact switch architecture with state-of-the-art on-state resistance $R_s = 0.5\ \Omega$ and off-state capacitance $C_s = 10$ fF. This is the first reported RF MEMS switch (DC–40 GHz) whose contact force is based on stress-induced deformation. Two different switch configurations are discussed and experimentally characterized for minimum insertion loss and maximum isolation.
- Chapter 7 uses the knowledge acquired from the previous chapters to introduce microstructures particularly suited for analog rather than digital tuning. Novel RF MEMS varactors are demonstrated with maximum analog capacitance range of 4:1 (300%). This is the highest analog tuning range reported for electrostatically actuated millimeter-wave varactors and is due to their unique electromechanical design. Reliability results from these structures are also pre-

sented in this chapter.

- Chapter 8 focuses on tunable antennas. In particular, the design of a compact, efficient and electronically tunable antenna is presented. A single-fed resonant slot loaded with a series of switches constitute the fundamental structure of the antenna. The antenna tuning is realized by changing its effective electrical length, which is controlled by the bias voltages of the switches along the slot antenna. Although the design is based on a resonant configuration, an effective bandwidth of 1.7:1 is obtained through this tuning without requiring a reconfigurable matching network. Theoretical and experimental behavior of the antenna parameters is presented and it is demonstrated that the radiation pattern, input impedance, efficiency and polarization state of the antenna remain essentially unaffected by the frequency tuning. Although the measurements were performed on an antenna with PIN diode switches, the design techniques presented in this chapter apply equally well for MEMS switches.
- Chapter 9 summarizes the major findings of this work and discusses future challenges for RF MEMS, such as packaging and reliability.

CHAPTER 2

Mechanical Design and Analysis of Low-Voltage Capacitive Switches

2.1 Introduction

MICROMACHINING and MEMS are among the most promising enabling technologies for developing low-power, low-cost, miniaturized RF components for high-frequency applications. Several universities and companies have developed RF MEMS switches in the last decade that can be primarily classified as a) series or shunt, b) fixed-fixed membranes or cantilever beams and c) capacitive or metal-to-metal contact type [16]. The main driving force behind this major research effort is the outstanding demonstrated RF performance of the MEMS switches from DC to 100 GHz compared to PIN diodes or FET transistors. Furthermore, electrostatically driven switches require only a few μW of DC power compared to several mW that their solid state counterparts dissipate. It is for this reason, as well as for the simplicity of their biasing networks that most of the developed switches are electrostatic in nature.

These studies, however, have only limited their focus on the RF performance of MEMS switches and have provided little information on several important phenomena

directly related to the inherent electromechanical characteristics of these structures. Their sheer interdisciplinary nature imposes a very tight coupling between the electrical and mechanical domains. For instance, thin film residual stress and viscous damping may have a far greater influence on the performance of the device than intuitively anticipated. Moreover, the vast majority of the switches in the literature typically require a pull-in and hold-down voltage of $40-100$ V and $15-30$ V respectively. Whereas no difficulty exists in achieving these ranges in a typical laboratory environment, they may be quite challenging for handheld mobile phones, automotive vehicles and similar wireless devices that rely on low-voltage power supplies. In addition, Goldsmith et al. [17] have shown that the lifetime of capacitive switches strongly depends on the applied actuation voltage. In particular, for capacitive switches they experimentally observed a lifetime improvement of a decade for every 5 to 7 V drop on the switch pull-in voltage. Consequently, reducing the actuation voltage of MEMS switches may not only broaden the range of their possible applications, but also significantly enhance their performance. It would seem, therefore, that further investigations are needed in order to provide the MEMS engineer with complete and accurate information on the design and operation of these devices.

It is the purpose of this chapter to present the results of our investigation on these issues. First, in Section 2.2 we focus on the design of the low spring-constant beams that support the main switch structure. We also demonstrate a number of designs that resulted in switches with pull-in voltages of as low as 6 V. Section 2.3 discusses the effects of residual axial and gradient stress on the device performance and shows how minor design and fabrication details may have a significant impact on the final structure. Section 2.4 concludes our study by presenting experimental and theoretical results on the dynamic behavior of the low-voltage MEMS switch. Sergio Pacheco and Linda P.B. Katehi developed the original switch concept and the required fabrication process (polyimide sacrificial layer, evaporated Ti/Ni seed layer) [15]. Additionally,

Sergio Pacheco has fabricated all the MEMS structures used in the actuation voltage and switching speeds measurements and performed all these measurements as well. Part of the in-plane stress analysis included in this chapter (equations (2.12), (2.13), (2.14) and Fig. 2.12) has been also contributed by Sergio Pacheco.

2.2 Spring Constant and Actuation Voltage

2.2.1 Design

The mechanical design of most electrostatically based switches starts with considering the required DC actuation voltage. Equation (2.1) presents a widely cited formula (e.g. [14]) for calculating the pull-in voltage of fixed-fixed beams, or air-bridges

$$V_p = \sqrt{\frac{8K_z{g_0}^3}{27\epsilon_0 A}} \tag{2.1}$$

K_z is the equivalent spring constant of the moving structure in the direction of desired motion (typically z-direction), g_0 is the gap between the switch and the actuation electrode, ϵ_0 is the free space permittivity and A is the switch area where the electrostatic force is applied. Formula (2.1) implies that there are several ways that may decrease the required actuation voltage [18]. For instance, reducing g_0 can significantly lower the pull-in voltage. Although this solution can be partly applied to low-frequency applications ($<$ 10 GHz), it will adversely affect the high-frequency off-state switch performance by compromising the switch isolation (for a series switch), or insertion loss (for a shunt switch). A second approach in lowering the pull-in voltage would be to increase the actuation area A. This area, however, has to stay within reasonable limits, primarily imposed by our desire for miniaturized circuits. The third alternative, which offers the maximum design flexibility for a low to moderate actuation

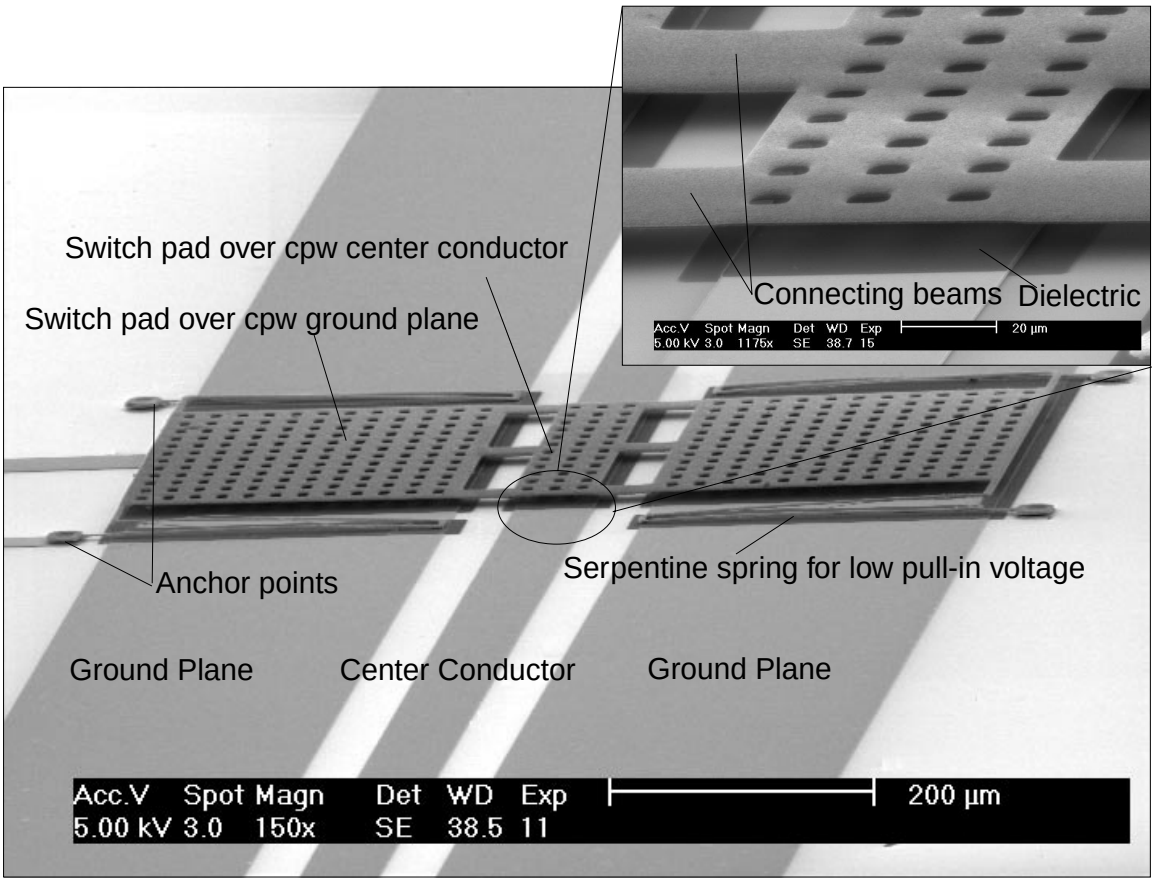


Figure 2.1: SEM picture of the proposed low-voltage capacitive shunt switch over a cpw line.

voltage, is to lower the switch spring constant, hence designing a compliant switch.

Fig. 2.1 shows an SEM picture of our proposed switch in a coplanar waveguide (cpw) configuration. The switch consists of three movable metallic plates, one over each conductor of the cpw line. These plates are connected together with three short beams (connecting beams) and the whole structure is connected to the substrate at four points (anchors) through four beams. Because of their shape, we will call these beams serpentine springs or folded-suspension beams. The switch is typically suspended 4–5 μm above the cpw line and is electrostatically actuated when a DC voltage is applied between the switch and the cpw ground planes.

2.2.2 Fabrication

The fabrication process requires four masks and is described in detail in Appendix A. Fig. 2.2 summarizes the required steps, which were first introduced by Pacheco and Katehi [15]. The cpw line is typically made of Ti/Au (500/9000 $\mathring{A}$) and is defined first through a lift-off process. A Plasma Enhanced Chemical Vapor Deposition (PECVD) of approximately 1200–2000 $\mathring{A}$ Si_3N_4 follows. Since the switch is made of metal (typically Ni) this dielectric layer is primarily needed during the actuation stage to prevent a direct DC contact between the switch and the cpw line. Therefore, a positive photoresist intended to protect the Si_3N_4 underneath the switch is deposited and patterned, while the remaining dielectric layer is etched through an RIE process. After the photoresist removal, the sacrificial layer (polyimide or photoresist) is deposited and the switch anchor points are photolithographically defined. Afterwards, a seed layer (typically Ti/Ni 2000/500 $\mathring{A}$), is deposited, patterned and electroplated. The last step is the removal of the sacrificial layer and the supercritical CO_2 drying of the structure. More details about the fabrication process are available in Appendix B.

2.2.3 Spring Design

Since the mathematical details of the electrostatic actuation (including equation (2.1)) have been extensively analyzed in the past [19, 20], we will just briefly describe the basic principle here. When no DC bias is applied, the switch presents a very small shunt capacitance (typically in the order of 30–50 fF) between the center conductor and the ground planes. This is called the up or off state and the RF signal can propagate with minimal loss (typically with less than 0.1 dB at X-band). On the other hand, if the applied bias exceeds the actuation voltage, the switch collapses on the dielectric layer underneath, resulting in a significant shunt capacitance, which is equivalent to an RF short-circuit. This is called the down or on state and virtually all the incident RF power is reflected back to the source.

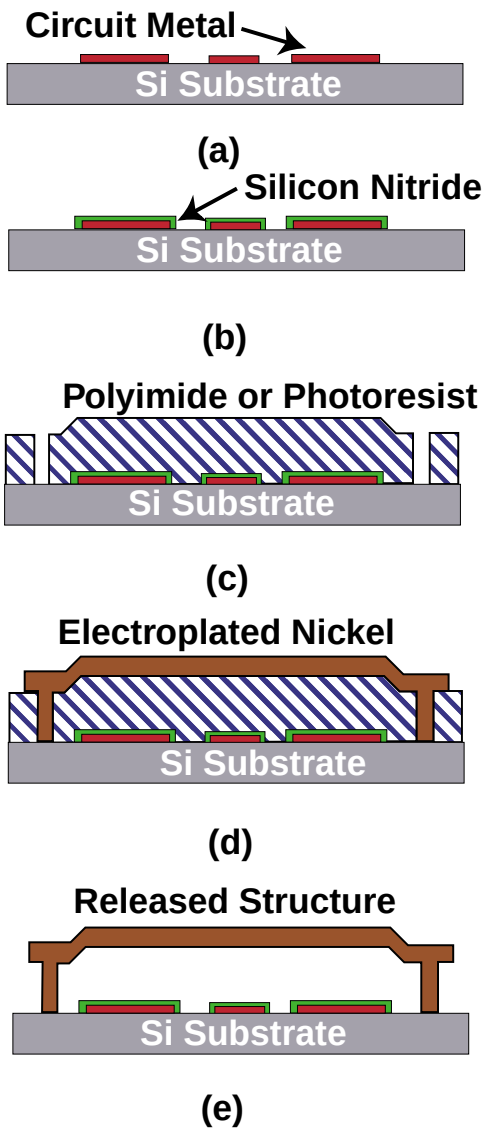
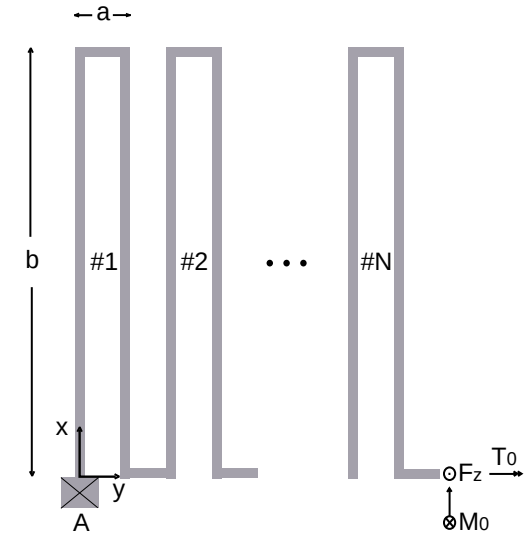


Figure 2.2: Summarized switch fabrication process.

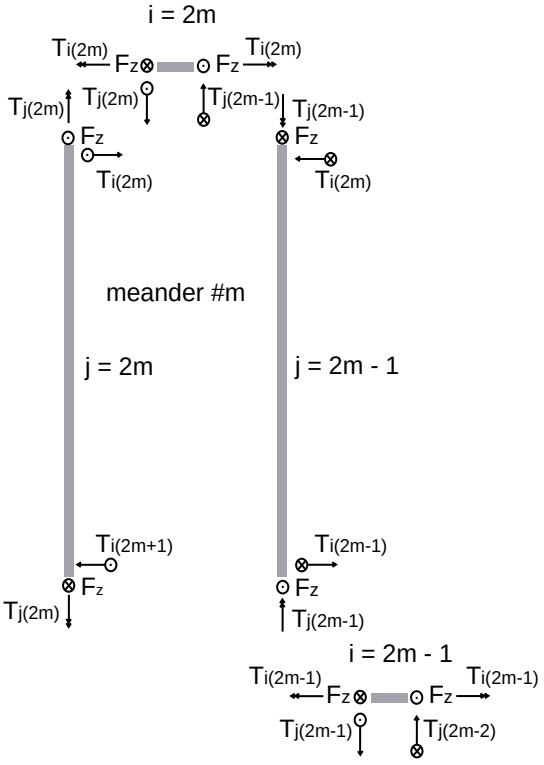
As it was previously mentioned, the switch of Fig. 2.1 is connected to the substrate through four serpentine springs that are used to substantially lower the switch spring constant. If k_z is the z-directed spring constant for each one of the springs, the total switch spring constant, K_z, is given by

$$K_z = 4k_z \tag{2.2}$$

Compared to simple cantilever beams of equal total length, these springs have the



(a)



(b)

Figure 2.3: (a)Schematic (drawn to scale) of an N-meander serpentine spring. (b) Forces, torques, and moments in the mth meander.

Table 2.1: Physical dimensions and material constants for the low-voltage switch.

Primary meander length (a)	20 μm
Secondary meander length (b)	240 μm
Switch thickness (t)	2 μm
Beam width (both beams) (w)	5 μm
Ni Young's modulus (E)	207 GPa
Ni Poisson's ratio (ν)	0.31
Shear modulus (G)	$E/(2(1+\nu))$
x-axis moment of inertia (I_x)	$wt^3/12$
z-axis moment of inertia (I_z)	$tw^3/12$
polar moment of inertia (I_p)	$I_x + I_z$
Torsion constant (J)	$0.413I_p$ (see [22])

additional advantage of occupying considerable less space, but they also show higher spring constant. As it will be shown, however, adding more meanders can significantly lower it without excessively increasing the required space. In the following we calculate the spring constant of an N-section meander (Fig. 2.3a) when a virtual force F_z is applied at its free end. An analytical solution for a similar folded meander has been obtained by Fedder [21] and our analysis is based on his work.

Each meander of the whole spring is defined as the set of four beams: two primary beams of length a and two secondary beams of length b. Therefore, an N-meander spring has $2N$ primary beams and $2N$ secondary beams. The switch shown in Fig. 2.1 for instance, has a single section meander ($N = 1$) with $a = 20$ μm and $b = 240$ μm. All the necessary dimensions and material constants for our switch are given in Table 2.1. For the analytical calculation it is assumed that all six degrees of freedom of the anchor point (point A in Fig. 2.3a) are fixed. Moreover, the guided-end boundary conditions are applied for the free-end point of the spring, since this point is attached to the main switch body. Consequently, a moment M_0 and a torsion T_0 are applied to this point to constrain the rotation angles around the x and y axes. The torsion and moment of each beam are then given by [21] (see Fig. 2.3b)

$$
\begin{aligned}
M_{a,i} &= M_0 - F_z\left[x + (i-1)a\right] \\
T_{a,i} &= T_0 + \left[\frac{1+(-1)^i}{2}\right] F_z b \\
M_{b,j} &= (-1)^j T_0 - F_z x + \left[\frac{1+(-1)^j}{2}\right] F_z b \\
T_{b,j} &= (-1)^j \left(j F_z a - M_0\right)
\end{aligned}
\tag{2.3}
$$

where $M_{a,i}$ and $T_{a,i}$ ($M_{b,j}$ and $T_{b,j}$) are the moment and torsion of the ith primary beam (jth secondary beam) with $i = 1$ to $2N$ ($j = 1$ to $2N$). In these equations, x is the longitudinal dimension along each one of the beams.

Following the virtual work method, the total elastic strain energy of the meander is given by

$$
U = \sum_{i=1}^{2N} \int_0^a \left(\frac{M_{a,i}^2}{2EI_x} + \frac{T_{a,i}^2}{2GJ}\right) dx + \sum_{j=1}^{2N} \int_0^b \left(\frac{M_{b,j}^2}{2EI_x} + \frac{T_{b,j}^2}{2GJ}\right) dx \tag{2.4}
$$

where I_x, I_z, G and J are defined in Table 2.1. Finally, the spring constant is given by

$$
k_z = \frac{F_z}{\delta_z} = \frac{F_z}{\partial U / \partial F_z} \tag{2.5}
$$

along with the boundary conditions

$$
\phi_0 \equiv \frac{\partial U}{\partial M_0} = 0 \quad \text{and} \quad \psi_0 \equiv \frac{\partial U}{\partial T_0} = 0 \tag{2.6}
$$

These equations lead to the following expressions for the reactions M_0 and T_0

$$
M_0 = \frac{\frac{2Na}{EI_x} + \frac{(2N+1)b}{GJ}}{2\left(\frac{a}{EI_x} + \frac{b}{GJ}\right)} a F_z \tag{2.7}
$$

$$
T_0 = -\frac{F_z b}{2} \tag{2.8}
$$

and for the spring constant k_z

$$k_z = \left[\frac{8N^3a^3 + 2Nb^3}{3EI_x} + \frac{abN\left[3b + (2N+1)(4N+1)a\right]}{3GJ} - \frac{Na^2\left[\frac{2Na}{EI_x} + \frac{(2N+1)b}{GJ}\right]^2}{2\left(\frac{a}{EI_x} + \frac{b}{GJ}\right)} - \frac{Nb^2}{2}\left(\frac{a}{GJ} + \frac{b}{EI_x}\right)\right]^{-1} \tag{2.9}$$

Although equation (2.9) is lengthy, it is written in an intuitive way that may facilitate the design of these meanders or similar beams. The first two terms of the denominator represent the percentage of the spring constant that is due to beam bending (first term) and twisting (second term). In other words, these terms depend solely on the meander geometry and the ability of the beam material to bend and twist. The last two terms of the denominator are due to the boundary conditions of the meander moving end and correspond to its inability to rotate around the x- (third term) and y-axis (fourth term). These two terms may have comparable magnitude to the first two and considerably increase the switch spring constant.

Equation (2.9) was verified by a commercially available finite element (FEM) code [23]. The dimensions of Table 2.1 were input in the code and several linear simulations were performed for springs with one to five meanders. For each simulation, a concentrated z-directed force of $F_z^{FEM} = 1$ μN was applied at the tip of the spring along with the necessary guided-end boundary conditions. The resulting deflection Δ_z was then computed and the FEM spring constant was extracted as $k_{mz}^{FEM} = F_z^{FEM}/\Delta_z$. Excellent agreement between the analytically and numerically computed spring constants is observed in Fig. 2.4, which graphically presents the two spring constants as a function of the number of the meanders. This graph also illustrates that the serpentine spring constant is not significantly reduced after including four or five meander sections. Hence, three or four meanders would be a good compromise between low spring constant requirements and space limitations.

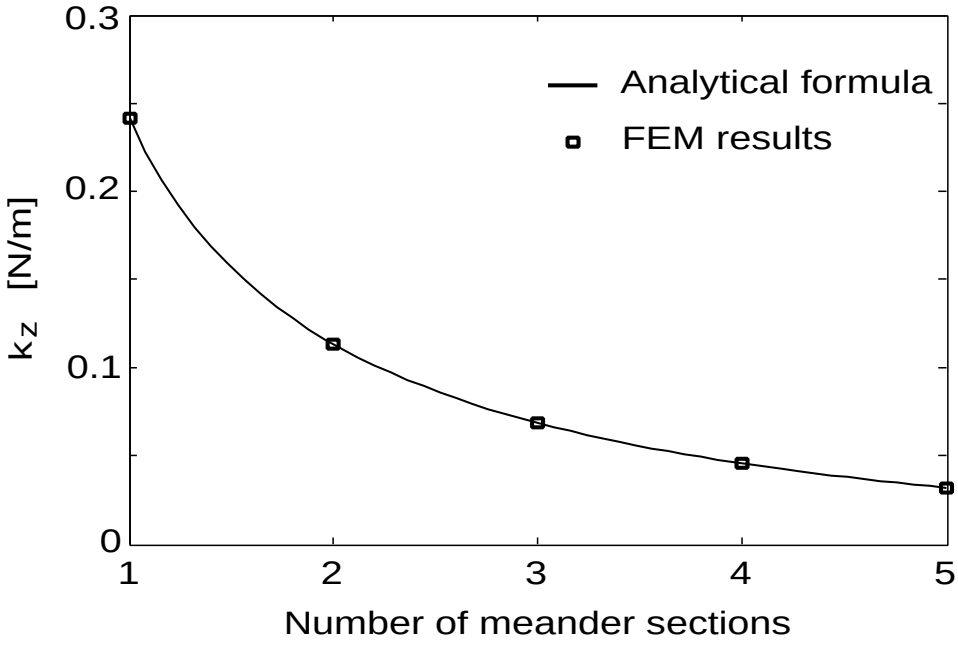


Figure 2.4: Analytically computed and FEM simulated results of the z-directed spring constant of an N-section meander.

2.2.4 Actuation Voltage Measurements

Five switch designs with one, two, three, four, and five meanders in their folded-suspensions were fabricated and measured. Sergio Pacheco fabricated the switches and performed all the measurements in this Section. Except for the serpentine springs, all designs were identical and were fabricated on the same wafer by the same fabrication process. For each design, we measured the pull-in voltage using an HP 4275A multifrequency LCR meter with an internal bias option. These measurements are presented in Table 2.2, which also compares the extracted switch spring constant from the measured pull-in voltage (based on Equation (2.1)) with the corresponding theoretical results. The theoretical values have been calculated for a switch thickness of $t = 2.5$ μm (because of over-plating in the fabricated switches) and an initial gap of $g_0 = 5$ μm. The reason for this higher gap is that, although the sacrificial layer thickness was 4 μm, the induced residual stress across the structure caused a slight out-of-plane deflection, which on average increased the total distance from the sub-

Table 2.2: Actuation voltage measurements for several MEMS switches (courtesy of Sergio Pacheco and Linda P.B. Katehi).

Meanders	Experimental		Theoretical	
	V_p [V]	K_z [N/m]	V_p [V]	K_z [N/m]
1	30	26.9	8.3	2.08
2	22	14.5	5.7	0.97
3	17	8.6	4.4	0.58
4	11	3.6	3.6	0.38
5	6	1.1	3.0	0.27

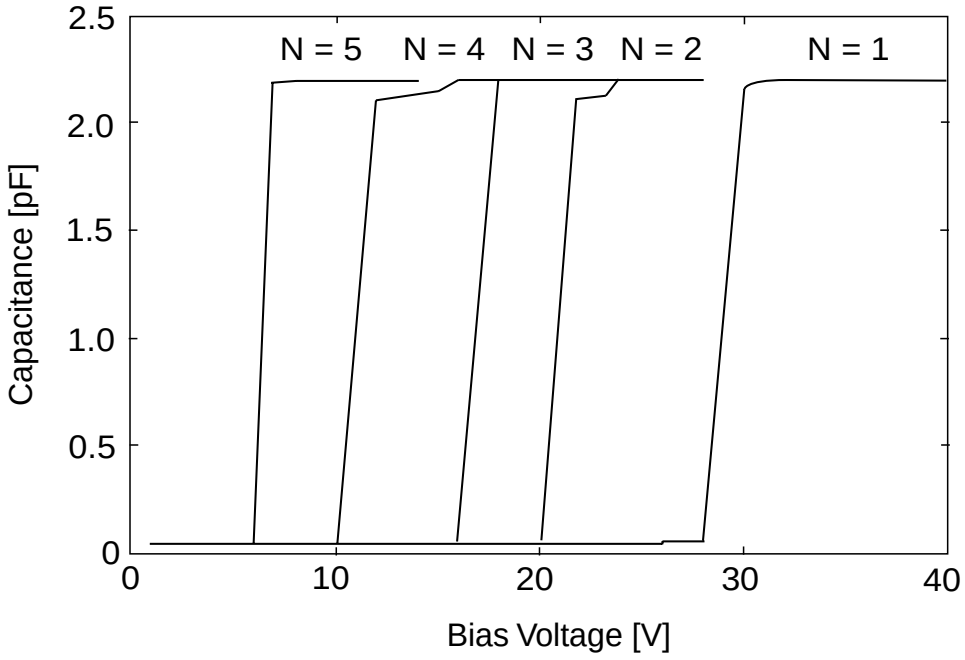


Figure 2.5: Measured DC switch capacitance as a function of the applied bias voltage and the number of meanders (courtesy of Sergio Pacheco and Linda P.B. Katehi.)

strate to 5 μm. We will discuss stress issues in more detail in Section 2.3. Fig. 2.5 also shows the measured DC-capacitance of the switches as a function of the applied bias voltage and the number of meanders.

These data reveal several discrepancies between the simulated and measured results. The first dissimilarity is the fact that the measured pull-in voltages are five to

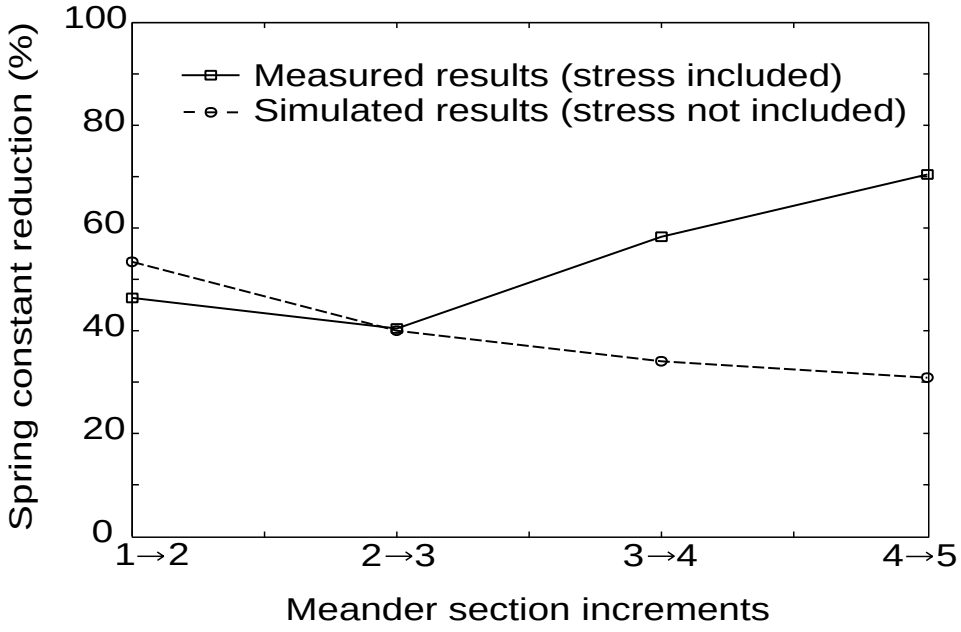


Figure 2.6: Experimental and theoretical percentage change of the switch spring constant as the number of meanders is increased.

ten times higher than the theoretically calculated ones. The second, and most interesting one, is related to the percentage of the spring constant reduction as the number of meanders is increased. For example, when the number of meanders was increased from one to two, the experimentally extracted spring constant was decreased by 46%, while the theoretical calculations predicted 53%. Although these results are in fair agreement, this is not the case for switches with more meanders. The switches with five meanders, for instance, had 70% lower spring constant than the ones with four. According to equation (2.9), however, this number should be close to 30%. Fig. 2.6 graphically illustrates these observations for all cases. All these issues are due to the high intrinsic axial stress built into the Ni layer during the fabrication and are studied in Section 2.3.

2.2.5 Stiction and Top Electrode Design

Although low spring constant is essential in obtaining low-voltage switches, preventing down-state stiction is equally important. A low-voltage switch experiences a relatively weak restoring force while in the down state, which may not be sufficiently high to pull the switch up, particularly in humid or contaminated environments. This drawback of this family of switches can be overcome by including top electrodes. Chapter 3 includes a detailed discussion of the design, fabrication and measurements of a top electrode for our low-voltage switch. Additionally it discusses the advantages of the top electrode switch with regard to its power handling capabilities.

2.3 Intrinsic Residual Stress Issues

Although the previous analysis allows for a first estimate of the switch spring constant and pull-in voltage, it does not account for any intrinsic residual stress on the structure. Residual stress, however, is developed during the fabrication of most microstructures and typically presents most of the major challenges in developing these devices. Under this stress, thin-film structures can experience undesirable deformations, which may be significant, particularly for high-aspect ratio structures. Additionally, many MEMS switches must satisfy very stringent requirements for reliable performance, including being planar over the circuit underneath it. Any undesirable buckling or curling may easily deteriorate the performance of the switch, or lead to the complete failure of the device. A lot of attention, therefore, has to be paid to residual stress and its effects on compliant structures before any successful devices can be developed.

When a thin film is deposited on a sacrificial layer at a temperature lower than its flow temperature, intrinsic stresses develop in the film-sacrificial layer system [24]. A number of studies have been already performed to theoretically explain the mech-

anisms of these stresses [25, 26] and to experimentally measure their effects [27, 28]. Nonetheless, in general thin-film stress is complicated and heavily depends on the specifics of the fabrication process. There is also very little information for metallic microstructures built by thin films depositions and effective ways that can control its stress and/or its effects. This section illuminates the most important stress-related challenges for developing low-voltage switches.

2.3.1 Gradient Residual Stress

A general uniaxial residual stress field in a thin film can be represented as [27]

$$\sigma_{total} = \sum_{k=0}^{\infty} \sigma_k \left(\frac{y}{h/2} \right)^k \tag{2.10}$$

where h is the film thickness and $y \in (-h/2, h/2)$ is the coordinate across the film thickness, with its origin at the mid-plane of the film. For a first order approximation, the total stress can be calculated as

$$\sigma_{total} \simeq \sigma_0 + \sigma_1 \left(\frac{2y}{h} \right) \tag{2.11}$$

This equation implies that the total stress can be expressed as a superposition of the constant mean stress σ_0 (positive or negative depending on whether the film is in tension or compression) and a gradient stress σ_1 about the mid-plane (see Fig. 2.7). The effects of the gradient stress are analyzed in this subsection and those of the mean stress in the following one.

It is widely known that residual gradient stress causes undesirable out-of-plane deformation. Fig. 2.8 shows two examples of extremely warped switches. These switches were 4 μm thick and the maximum deformation, defined as the distance between the higher and lower switch points, was on average 22–24 μm. This deformation was recorded for switches 640 μm long (not counting the length of the meanders) but

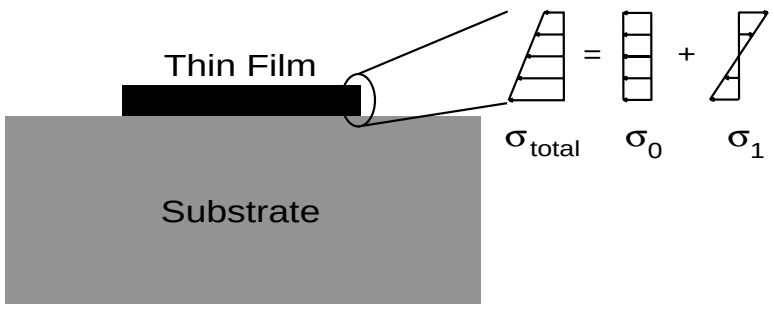


Figure 2.7: Thin film residual stress approximation.

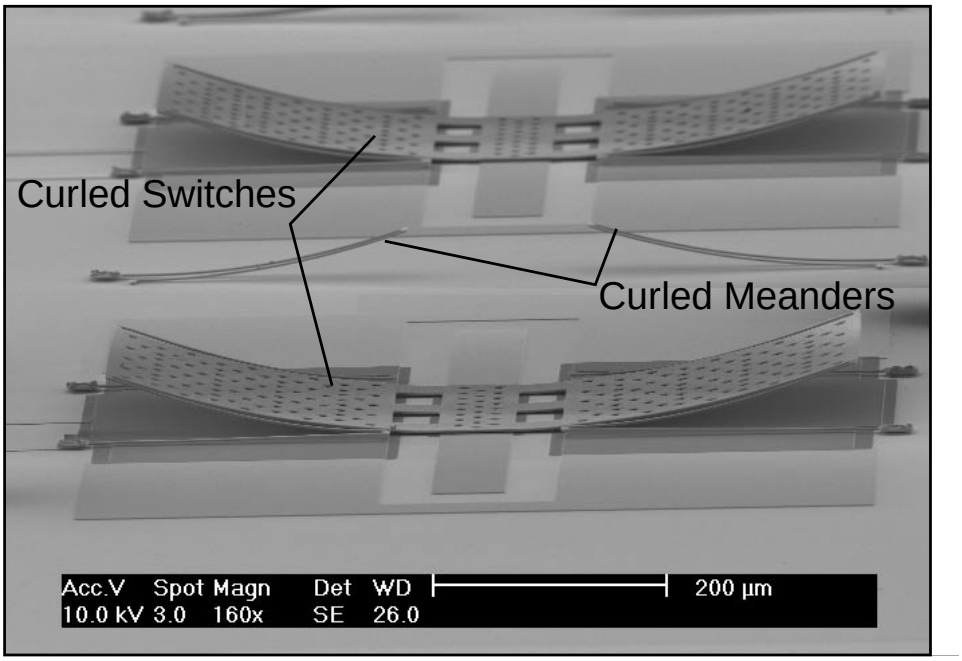


Figure 2.8: Switches with considerable deflection as a result of a poorly designed fabrication process.

increased to 70–80 μm for switches close to 1 mm long. This substantial deformation renders both structures unusable for two reasons: a) the required actuation voltage is much higher than the design value ($>$ 80 V), and b) the up-state switch RF capacitance is considerably higher than anticipated ($C_{up} >$ 150 fF, instead of 50 fF). The sacrificial layer and the seed layer that resulted in such a stress were the polyimide DuPont PI2545 and an evaporated Ti/Ni (1500/500 $\AA$) layer respectively. The switches were then electroplated in a Ni solution (Nickel Sulfamate, Barrett SN by

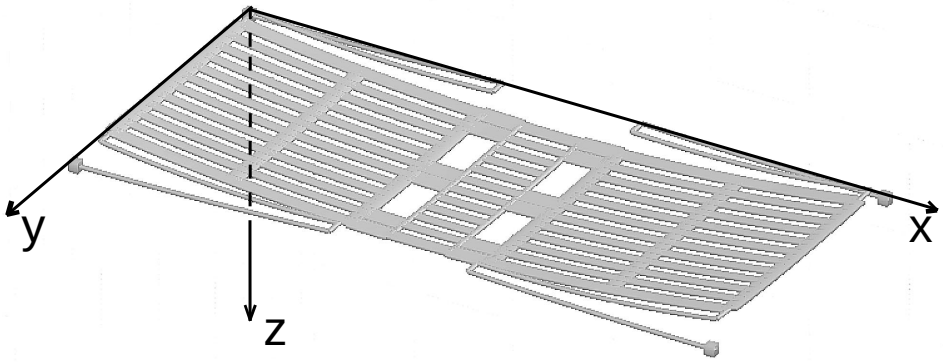


Figure 2.9: Simulated warped switch structure (by SUGAR). The maximum switch deflection is approximately 23 μm.

Mac Dermid) with a steady current density of 4 mA/cm^2 for approximately 30 minutes. The induced stress with this fabrication process was repeatable over a period longer than six months.

This switch shape under residual gradient stress was also theoretically validated using SUGAR [29]. Fig. 2.9 shows the simulated switch shape, which agrees very well with the fabricated switches. The maximum gradient stress value in the software was varied until the measured maximum deflection was obtained.

One way to alleviate this problem without increasing the actuation voltage is to selectively increase the switch thickness [30]. In this technique, the main switch body thickness is increased to 6–8 μm, but the springs remain 2 μm thick (Fig. 2.10a). This process utilizes two electroplating steps: first the switch and the springs are plated, and subsequently the switch main body is plated again until it reaches a thickness of 6–8 μm. Because of some adhesion difficulties between the two plated structures,

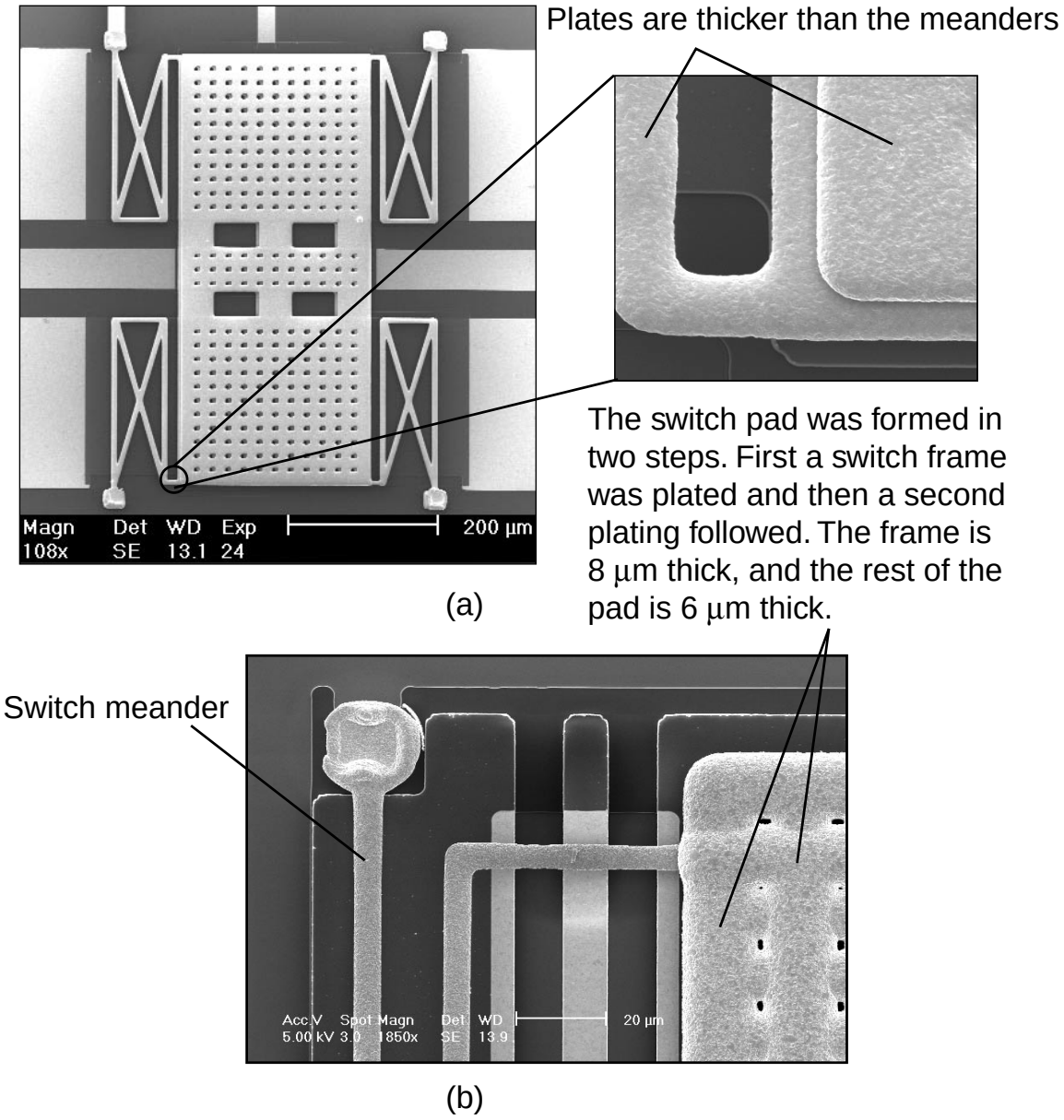


Figure 2.10: Fabricated switches with the selective electroplating process. The adhesion problems of the first switch were solved by increasing the seed layer area that was exposed to the second plating.

the process was slightly changed by plating only a switch frame during the first step instead of the whole switch (Fig. 2.10b). This improvement resulted in a 98% yield.

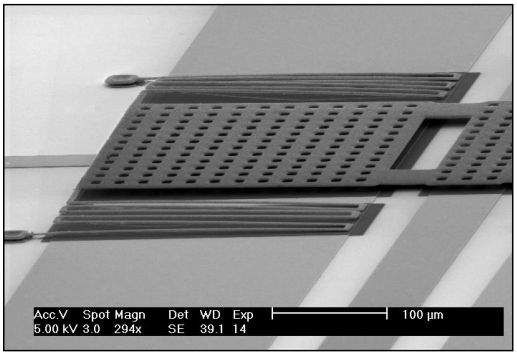
The drawback of this technique, however, is that although it limits the switch warping to 1–3 μm and may prove useful for other types of MEMS devices, it also

results in less conformal switches with lower down-state capacitance than the original structures.

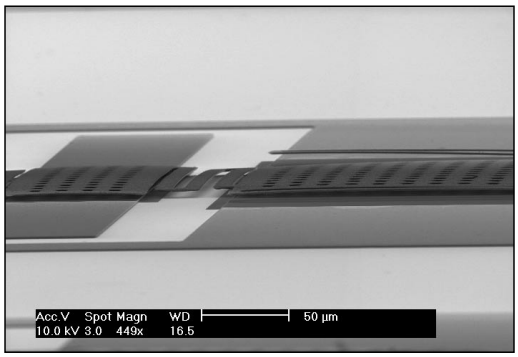
We experimentally found that a better solution is to sputter deposit the Ti layer (instead of evaporating) above the sacrificial layer. More specifically, the Ti sputtering process is performed with The University of Michigan sputtering tool with a DC source calibrated to deposit 90 $\mathring{A}$/min under 7 mT of Ar pressure. The actual deposition is typically done for 25–26 min resulting in a film of 2250–2350 $\mathring{A}$ of Ti. After the sputtering process is completed, the sample is immediately (in order to minimize Ti oxidation) taken to the Ni e-beam evaporator where 500 $\mathring{A}$ of Ni are deposited. It is also very important to point out that nothing else is changed in the process, including the Ni electroplating solution, current density and sacrificial layer etching. Furthermore, this process can be followed with either polyimide or photoresist with negligible differences.

Fig. 2.1 is one example of the plane switches fabricated with this process and Fig. 2.11 shows some details of three more examples. The switches shown in Fig. 2.1 and 2.11a are 2 μm thick and suspended over a 40/60/40 μm cpw line. Although the latter switch was fabricated with three meanders instead of one, no appreciable difference in the warping profile was observed. The maximum measured deflection (as defined in Fig. 2.8) for both of them is approximately 0.5 μm. This corresponds to less than 0.1% of the main switch length (640 μm) and does not affect the RF switch performance, since it is strongly localized at the end of the DC actuation pad.

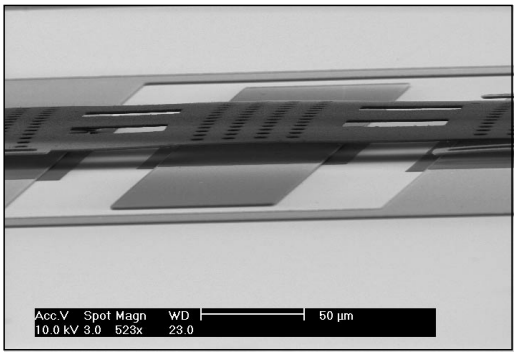
The improved fabrication process was also tested with switches only 1 μm thick, 680 μm long, and 240 μm wide. Two of these switches are shown in Fig. 2.11b and c. Both switches include one meander, but in the first one we have replaced the straight connecting beams with a second meandering beam. Evidently both structures are fairly plane and their residual gradient stress is nearly negligible. The first one, however, exhibits somewhat straighter profile, which is related to the axial residual



(a)



(b)



(c)

Figure 2.11: Planar switches fabricated with sputtered Ti layer instead of evaporated. (a) This three-meander switch is 640 μm long, 2 μm thick, its maximum out-of-plane deformation is less approximately 0.5 μm and the used sacrificial layer was polyimide. (b) and (c) These switches are 680 μm long, 1 μm thick and photoresist was their sacrificial layer. Their warping level is about 3 μm and is mostly along their short dimension.

stress, analyzed in the next section. This meandering connecting beam was originally employed to increase the shunt switch inductance [31], but it also proved useful in releasing the in-plane switch stress. As for the three short connecting beams, the slightly less plane switch may not appear very appealing at first, but it is very useful in limiting the high-frequency up-state insertion loss, because it substantially reduces the up-state capacitance (by 50–70%). Furthermore, the pull-in voltage increase is negligible (both structures actuate with 15–20 V) because most of the electrostatic force is concentrated on the ground plane switch pads. Finally, both structures experienced some warping along their width, but this did not prove to be a problem. The switches were thin enough that were able to conform on the dielectric surface in the down-state.

2.3.2 In-plane Residual Stress

In-plane residual stress primarily increases the switch spring constant and is therefore essential to control it within reasonable limits. It was experimentally found [28] that the induced tensile stress during the fabrication process was in the order of 150 MPa. A first order approximation that shows the impact of this stress on the spring constant is analyzed in [32] where the deflection of a guided-end cantilever is calculated under simultaneous axial tension and concentrated transverse loading. The maximum deflection at the tip of the beam is given by

$$z_{max} = \frac{W}{\gamma P}\left[\frac{(\cosh(\gamma l) - 1)^2}{\sinh(\gamma l)} - (\sinh(\gamma l) - \gamma l)\right] \tag{2.12}$$

where P is the axial tensile load, W is the transverse concentrated load at the tip of the beam, l is the length of the beam and γ is defined by

$$\gamma = \sqrt{\frac{P}{EI_x}} \tag{2.13}$$

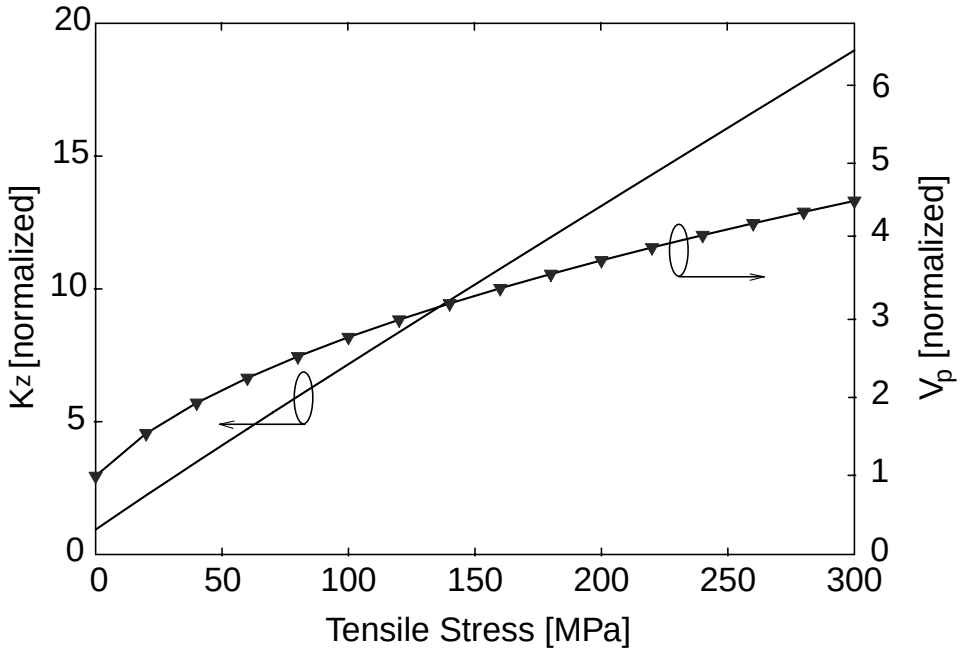


Figure 2.12: Spring constant and pull-in voltage as a function of axial residual stress for a guided-end cantilever with simultaneous axial tension and concentrated transverse loading.

This leads to the following expression for the spring constant

$$K_z^{cant} = \frac{\gamma P \sinh(\gamma l)}{2(1-\cosh(\gamma l)) + \gamma l \sinh(\gamma l)} \tag{2.14}$$

Fig. 2.12 shows the variation of the normalized spring constant and the associated actuation voltage (with respect to the spring constant and actuation voltage of zero axial stress) for an axial tensile stress of 0 to 300 MPa. This figure clearly demonstrates the considerable impact of the axial stress on the switch actuation voltage. For instance, a tensile stress of 150 MPa would increase the pull-in voltage of a switch suspended by four cantilever beams by more than three times.

The serpentine beams shown in Fig. 2.3 exhibit higher flexibility in handling the in-plane mean stress than the simple cantilever beam. In other words, as the number of meanders is increased, not only is the z-directed spring constant reduced, but also the lateral ones. To show this effect, the x- and y-directed spring constants

were calculated with a similar process to that of Section 2.2. The y-directed spring constant can be expressed as

$$k_y = \frac{\frac{2S_{1y}}{Nb^2} EI_z}{2\left(a + \frac{2b}{3}\right) S_{1y} - (a+b) S_{2y} - 3(2N+1)a(a+b)^2} \tag{2.15}$$

where S_{1y} and S_{2y} are calculated by

$$S_{1y} = 4N^2a^2 + \left(4N^2 - 1\right) b^2 + 2\left(4N^2 + 1\right) ab \tag{2.16}$$

$$S_{2y} = 2N(2N-3)a^2 + \left(4N^2 - 1\right) b^2 + \left(8N^2 - 6N - 1\right) ab \tag{2.17}$$

Similarly, the x-directed spring constant is given by

$$k_x = \frac{EI_z}{Na^2 \left[S_{1x} + S_{2x} + \frac{8N^2a + (2N+1)(4N+1)b}{3}\right]} \tag{2.18}$$

where

$$S_{1x} = (2Na + (2N+1)b) \left[-\frac{2N+1}{2} + \frac{a(a+2b/3)}{(a+b)(a+b/3)} \right] \tag{2.19}$$

$$S_{2x} = -(2N+1)(a+b)\frac{a}{2(a+b/3)} \tag{2.20}$$

Linear FEM simulations verified the previous formulas and the results are given in Fig. 2.13. From this figure we clearly observe that the spring constant of the serpentine spring is greatly reduced as the number of meanders is increased. For instance, a spring with three meanders is 177 times more flexible along the x-dimension than a spring with one meander. As a result, such a spring can help release the axial switch stress along its long dimension much more effectively than a spring with one meander. In other words, springs with many meanders are much more effective as stress buffers than springs with only one meander. A similar tendency exists for k_y, which decreases by a factor of 5.2 when the meanders are increased from one to five. These results provide a qualitative explanation for the trends observed in Fig. 2.6.

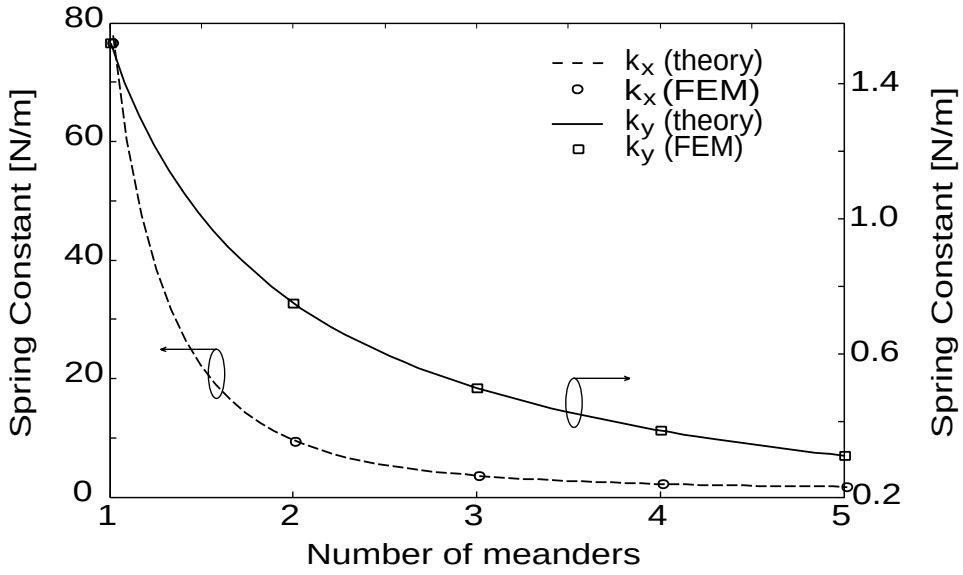


Figure 2.13: In-plane spring constants of the serpentine spring for various number of meanders.

2.4 MEMS Switch Dynamic Behavior

Switching speed is one of the few disadvantages of MEMS components compared to PIN diodes and FET transistors. While their mass is typically very small (in the order of 10^{-11} to 10^{-9} Kgr), inertia due to mechanical movement still limits their speed typically in the order of a few μsec. The fastest switch so far has been developed by researchers at MIT Lincoln Laboratory [33]. It is a very compact cantilever switch (less than 50 μm long) with a speed of approximately 1 μsec. This very low speed is primarily due to its very small dimensions, mass and limited squeeze-film damping. It does require, however, a high pull-in voltage of 50–60 V, while it is typically actuated with 70–80 V. Low voltage switches are generally expected to be slower since they typically have to move a relatively large actuation area. This is particularly true if the switch is expected to operate in air or another gas environment, such as N_2 (for limited humidity).

The switching speed is measured by recording the change in the power transmitted through the switch when a step voltage is applied at the bias of the device

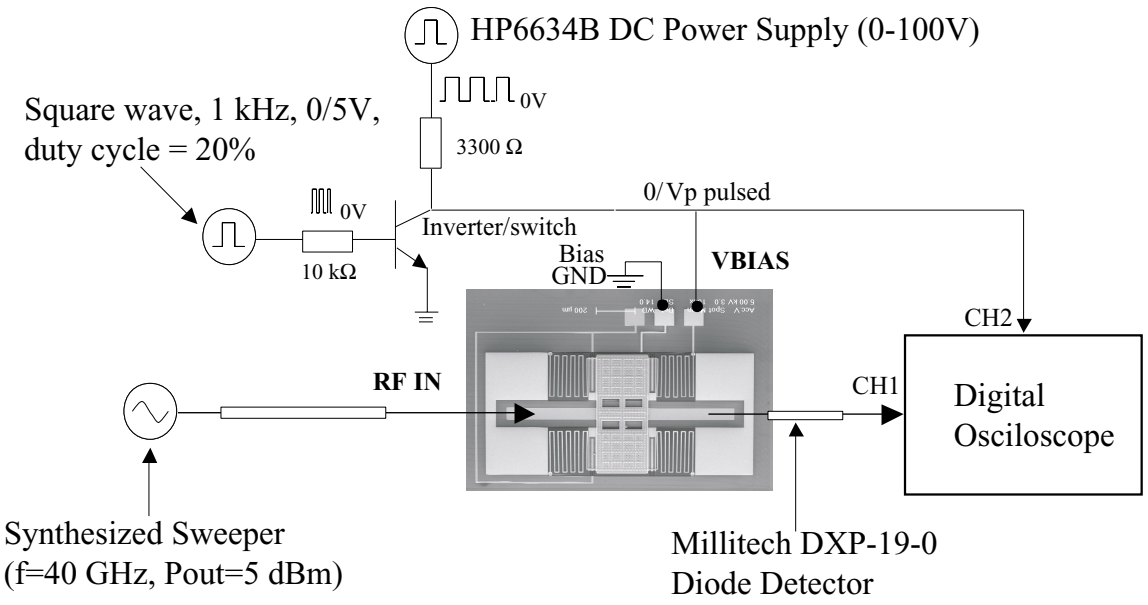


Figure 2.14: Switching speed measurement setup (Courtesy of Prof. Rebeiz, University of Michigan).

(Fig. 2.14 [34]). Sergio Pacheco fabricated the switches and performed all the measurements presented in this Section. The RF input signal at 40 GHz is provided by an RF synthesizer, while the RF output signal is recorded by a high frequency diode detector. The biasing signal is provided by a suitable combination of two DC power supplies and an inverter. Fig. 2.15 presents two typical measurements taken with this set-up for 3-meander switches. The measured switches were suspended a mean distance of 5 μm above the cpw line and the applied bias voltage was only 20–30 % higher than their actuation voltage. Both pull-in and release times were measured for these switches. Pull-in time is the time it takes the switch to touch the dielectric underneath it. On the other hand, the time that is required for the switch to move from the down-state to its original height (or within 5% from this value) is defined as the release time. Fig. 2.15 shows that the actuation and release times are approx-

imately 52 and 213 μsec respectively. However, for the release time measurement, it takes the switch only 25 μsec to reach its normal height, but another 190 μsec are needed to settle within 5% of its original height. It is also interesting to note that during the first 30 μsec of the actuation stage the switch does not move significantly. These effects will be discussed in the remaining of this section.

To explain the experimental results we employed a simple 1-D non-linear model that has been adopted by several researchers [19, 35, 36]. This model treats the switch as a single lumped mass and applies classical Newtonian mechanics to predict its behavior under the applied electrostatic force. A model that would accurately predict the dynamic behavior of the MEMS structure should integrate a good understanding of several different phenomena including electrostatics, mechanics, residual stress, contact forces, compressible squeeze film damping and impact effects on a microscale. A lot of these areas are currently under investigation and there is not a complete model that would account for all of these effects. Furthermore, our switch is a relatively large structure that cannot be perfectly approximated as a lumped mass. Nevertheless, the 1-D model can be used for an at least qualitative explanation of the measured switch behavior and provide reasonable approximations for the switching times.

The following equation of motion if the basic formula for the 1-D model

$$mz'' + bz' + K_z z = F_e + F_c \tag{2.21}$$

where m is the switch mass, b is the damping coefficient, K_z is the switch spring constant in the direction of motion, A is the switch actuation area, g_0 is the initial gap, ϵ_r and t_d are the dielectric layer constant and thickness respectively, V is the applied DC voltage, F_e is the electrostatic force and F_c is the contact force when the switch touches the dielectric. Several approximations may be adopted for calculating the parameters in this model. For instance, although the viscous damping can be considered constant for small displacements, this is not the case when the switch

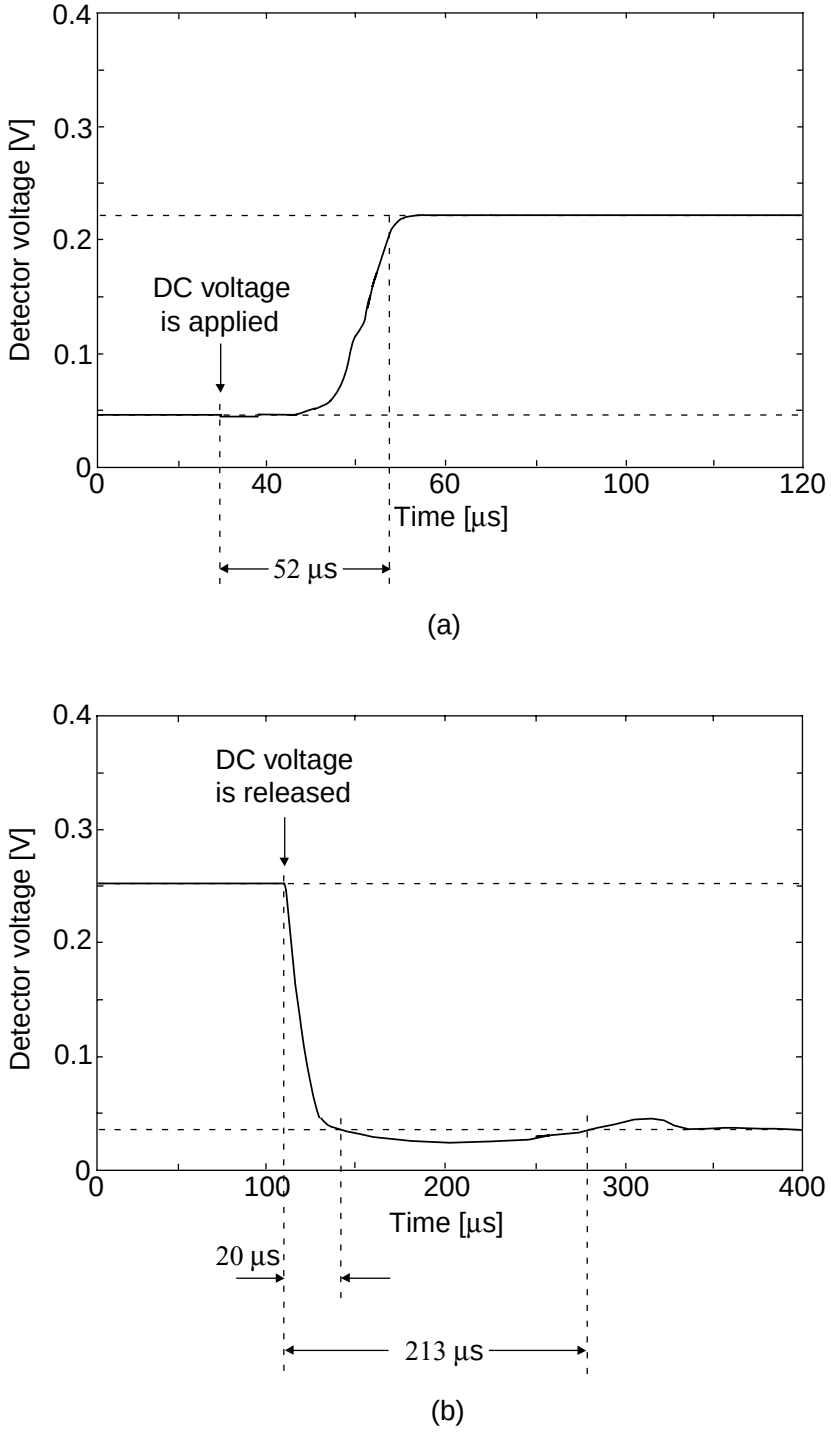


Figure 2.15: Measurements of the switching time for the (a) up-down and (b) down-up movements. Because of the diode detector, high voltage level corresponds to low RF power and vice-versa (courtesy of Sergio Pacheco and Linda P.B. Katehi.

is moving completely towards the substrate. Our model for the switching speed calculations is based on the discussion presented in [35] and [37] where these effects are taken into account. These equations can be summarized as follows

$$F_e = \frac{\epsilon_0 A V^2}{2\left(g_0 + t_d/\epsilon_r - z\right)^2} \tag{2.22}$$

$$b = \frac{K_z}{\omega_0 Q} \quad \text{where} \quad \omega_0 = \sqrt{\frac{K_z}{m}} \tag{2.23}$$

$$Q = Q_0 \left(1 - \left(\frac{z}{g_0}\right)^2\right)^{3/2} \left(1 + 9.638\left(\frac{\lambda}{g_0 - z}\right)^{1.159}\right) \tag{2.24}$$

$$F_c = \frac{m_1 A}{\left(g_0 - z\right)^3} - \frac{m_2 A}{\left(g_0 - z\right)^{10}} \tag{2.25}$$

Equation (2.24) calculates the switch quality factor and takes into account the damping dependence on the switch height. If this is ignored, the second term of the right hand side should be replaced by one. Furthermore, the third term reduces the gas flow resistance underneath the switch because of the slip-effect, were particles can have fewer interactions before escaping [38]. The variable λ of this term is called the mean free path and is approximately 0.1 μm at STP. The damping coefficient, which is related to Q_0 by (2.23), has been derived in [39] for a square plate with area A as

$$b = \frac{3}{2\pi}\frac{\mu A^2}{{g_0}^3} \tag{2.26}$$

where μ is the air viscosity (at STP $\mu = 1.845{\cdot}10^{-5}$ Pa·sec). For the switch dimensions and for a gap of 5 μm $b \simeq 2.5{\cdot}10^{-4}$ Pa·sec and $Q_0 = 0.64$ (for $K_z = 8.6$ N/m). However, the holes included in the switch allow the air underneath to escape more easily, thus reducing the damping coefficient and increasing the Q of the structure. Therefore, this value can be considered as a low bound for the switch quality factor. In fact, our experimental results suggest a quality factor of about two. The final equation of the model (equation (2.25)) was used to provide a stable solution to the

simulation when the switch contacts the dielectric layer.

Fig. 2.16a shows the simulated results for the pull-in and release time. A spring constant of 8.6 N/m (Table 2.2) and an actuation voltage of 25% higher than the pull-in voltage have been used for these simulations. These simulations provide a valuable insight in the measured dynamic behavior of the switch. The pull-in time, for instance, is approximately 50 μsec from which about 30 μsec are needed for the switch to move from 5 to 3.5 μm. The RF capacitance, however, does not change appreciably between this distance and this explains the relatively long period that is required to note any difference between the measured output power level (see Fig. 2.15). On the other hand, during the release stage, the switch reaches its original height within 35 μsec, but 140 additional μsec are required for stabilization within 5% of its original height. We have also plotted in the same figure the simulated release time assuming a constant quality factor $Q = Q_0$. Evidently, taking into account the quality factor variation versus height is of vital importance for meaningful simulations.

The problem of the long stabilization time can be easily corrected by decreasing the quality factor by about one. Fig. 2.16b shows the simulated release time for quality factors of 2, 1.5, and 1. This figure clearly demonstrates that the release time can be decreased by more than three times, if a lower quality factor is achieved. This can be done by optimizing the hole orientation on the main switch structure and by reducing their number per unit area. This change will not appreciably increase the pull-in time, as Fig. 2.16c shows. For example, for $Q = 1.5$, the pull-in time will be increased by only 10%, yet the release time will be reduced by 300%. Consequently, an optimization of the switch holes can lead to a design with switching times in the order of 50–60 μsec.

2.5 Conclusions

Low-voltage RF MEMS switches have been studied in this chapter. The design, fabrication and testing of these structures has been thoroughly discussed and switch designs with as low as 6 V actuation voltages have been measured. Moreover, residual stress issues associated with this family of switches have been addressed and it has been experimentally demonstrated that sputtered seed layer films result in devices with superior performance when compared with evaporated films. Furthermore, the dynamic operation of low-voltage switches has been experimentally and theoretically characterized and adequate switching times in the order of 50 μsec have been achieved.

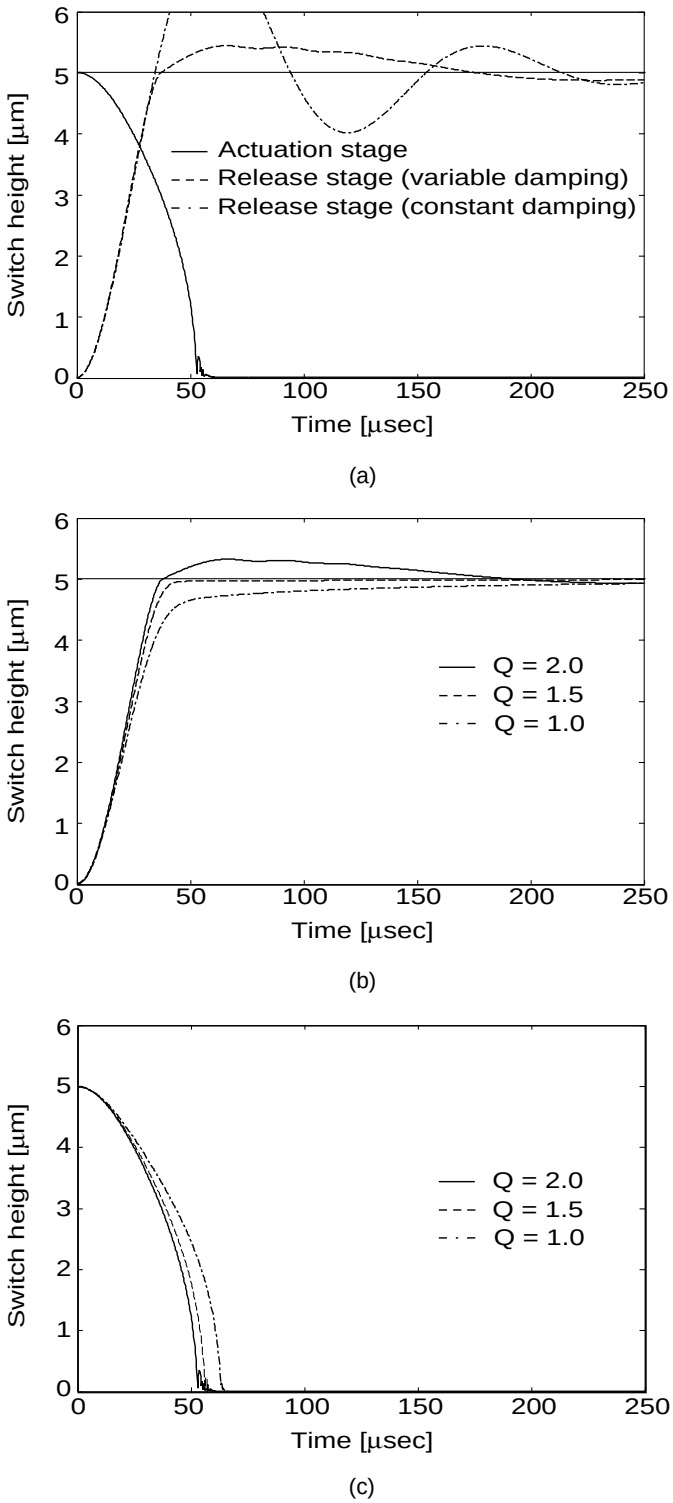


Figure 2.16: (a) Simulated switch pull-in and release times. (b) Comparison of simulated release times for different values of the quality factor. (c) Comparison of simulated pull-in times for different values of the quality factor.

CHAPTER 3

Capacitive MEMS Switches with Enhanced Power Handling Capabilities

3.1 Introduction

THE previous chapter focused on the mechanical design, residual stress and switching speed of a low voltage RF MEMS switch. The maximum RF power that MEMS switches can successfully handle, is an equally important issue for a number of different applications, such as transmitters in satellite and/or earth-based communications stations. Research in this area could initiate a significant effort towards reducing the weight, cost, and power required for these stations.

The main purpose of this chapter is to provide a theoretical and experimental study that addresses the aforementioned issues. In particular, after briefly describing in Section 3.2 the switch RF properties used in our experiments, Sections 3.3 and 3.4 discuss the problems of self-actuation and stiction in the down state due to high RF power. These findings suggest a few guidelines for designing switches specifically suited for high-power applications. We show for example that de-coupling the RF and DC actuation pads can substantially increase the power handling capabilities of the MEMS switch. Finally, Section 3.5 presents a novel switch architecture with a

top electrode above the switch to enhance its behavior during hot switching. All the fabricated switches, measurement techniques and measured results presented in Sections 3.3.2, 3.4.2, 3.5.1 and 3.5.3 reflect Sergio Pacheco's and Linda P.B. Katehi's contributions.

3.2 Switch Geometry and Characteristics

All of the experiments reported in this study have been carried out on the switch described in the previous chapter (see Fig. 2.1). This switch has been specifically designed for low actuation voltage and high power handling capabilities. It consists of three movable metallic plates, one over each conductor of the cpw line. These plates are connected together with three short beams (connecting beams) and the whole structure is connected to the substrate at four points (anchors) through four beams. Because of their shape, we will call these beams serpentine springs or folded-suspension beams. The switch is electrostatically actuated and is typically suspended 4–5 μm above the cpw line. When no DC bias is applied, the switch presents a very small shunt capacitance (typically in the order of 30–50 fF) between the center conductor and the ground planes. This is called the up or off state and the RF signal can propagate with minimal loss (typically with 0.2 dB up to 40 GHz). On the other hand, if the applied bias exceeds the actuation voltage, the switch collapses on the dielectric layer underneath it. The switch then presents a significant shunt capacitance, which is equivalent to an RF short-circuit. This is called the down or on state and virtually all the incident RF power is reflected back to the source. Whereas Fig. 2.1 shows a structure with one meander, switches with one to five meanders have been developed with a minimum measured voltage of 6 V [15].

Fig. 3.1 shows a lumped-element equivalent circuit for this structure [40] that is accurate up to 80 GHz. Typical up and down-state measurements are presented in

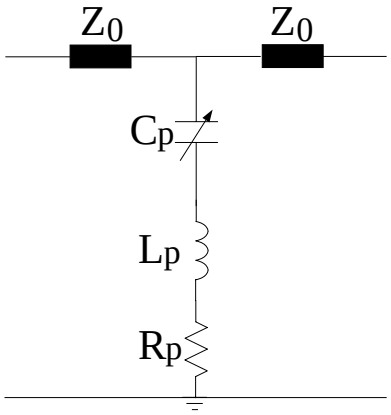


Figure 3.1: Lumped element equivalent model for the low voltage switch of Fig. 2.1

Fig. 3.2 along with the simulated results from this model. The switch presents an up-state insertion loss of 0.04 and 0.17 dB at 20 and 40 GHz respectively. The return loss is less than -12 dB up to 40 GHz. Based on the measured return loss, an up-state capacitance of approximately $C_U = 40$ fF can be extracted. The down-state isolation depends strongly on the switch geometry, the dielectric thickness and roughness [41]. The maximum isolation can be also tuned to the desired frequency by changing the inductance L_p, which depends on the connecting beams of the switch [31]. The switches measured in this study have been fabricated with 2000 $\mathring{A}$ of Si_3N_4, and have the connected beams shown in Fig. 2.1 that result in $L_p = 2 - 3$ pH. These switches exhibit a maximum measured isolation of approximately 15.5 dB at 40 GHz (Fig. 3.2), which corresponds to a down-state capacitance of approximately $C_D = 800$ fF.

3.3 Self-Actuation Due to High RF Power

3.3.1 Design and Modeling

Although a DC voltage is applied to bias electrostatic switches, these structures respond to any voltage with frequency lower than the switch self-resonance, which is typically in the order of a few kHz. For example, a harmonic RF voltage $V(t) =$

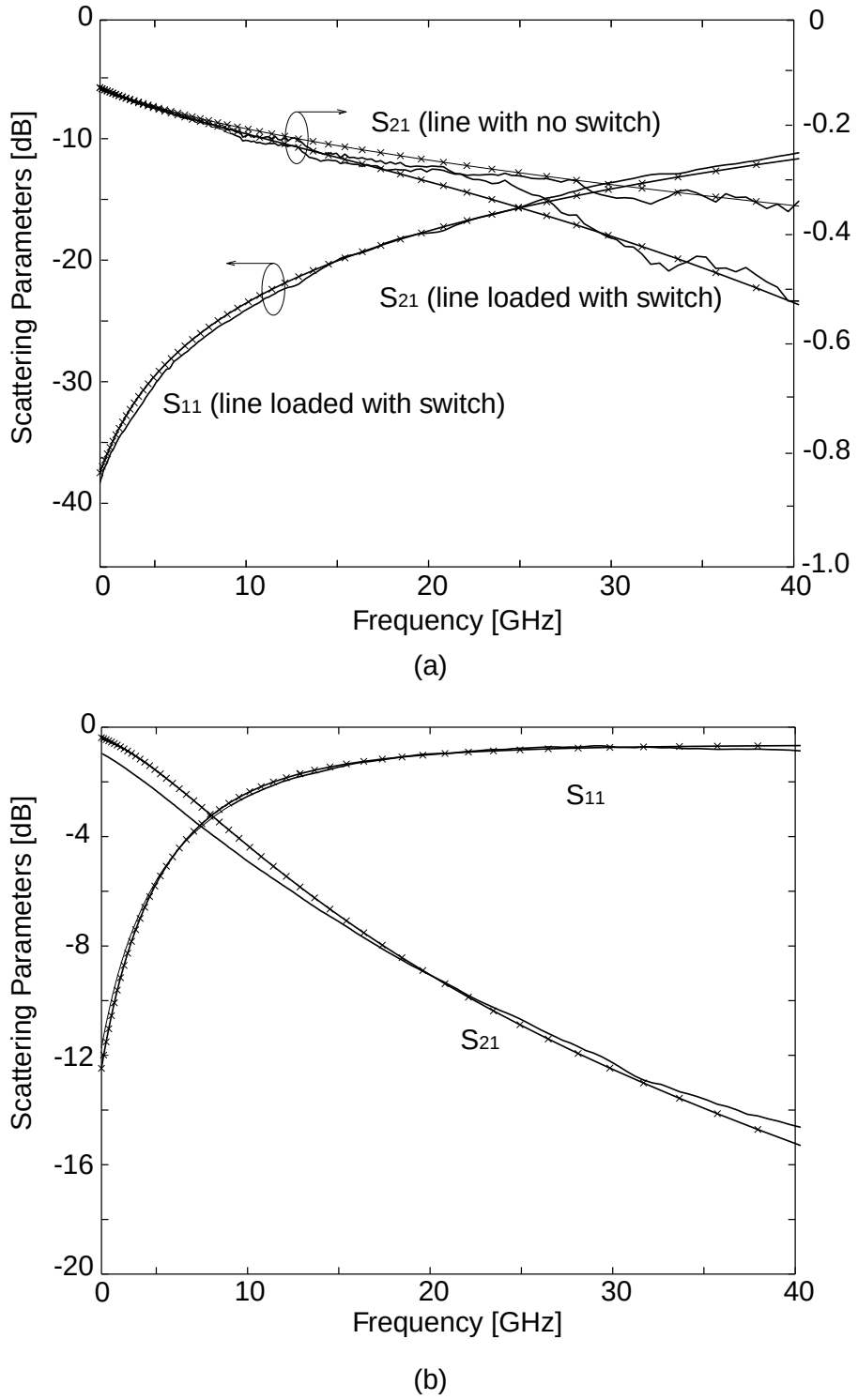


Figure 3.2: Measured and simulated RF performance of the switches used for the high-power measurements in the (a) up and (b) down states (courtesy of Sergio Pacheco and Linda P.B. Katehi.)

$V_0 cos(2\pi ft)$ applied between two parallel metallic plates in air induces an electrostatic force [37]

$$F_{RF} = -\frac{1}{2}\frac{\epsilon_0 A(V_0/\sqrt{2})^2}{g^2}\left(1 + cos(4\pi ft)\right) \tag{3.1}$$

where A is the area of the plates and g the distance between them (fringing capacitance has been ignored). Although the high-frequency component of this force will not cause any significant movement, the low-frequency force is equal to the force that would have been experienced by the metallic plates, if an equivalent DC voltage

$$V_{eq} = V_0/\sqrt{2} = V_{RF}^{rms} \tag{3.2}$$

had been been applied to them. Equation (3.1) implies that if the applied RF power is sufficiently high, the induced force may become sufficiently strong to pull the switch down without any DC bias voltage. Equivalently, the switch will be actuated if the voltage V_{eq} is higher or equal to the pull-in voltage given by

$$V_p = \sqrt{\frac{8K_z {g_0}^3}{27\epsilon_0 A}} \tag{3.3}$$

where K_z is the equivalent spring constant of the moving structure in the direction of desired motion (typically z-direction), g_0 is the gap between the switch and the actuation electrode, ϵ_0 is the free space permittivity and A is the switch area where the electrostatic force is applied. This phenomenon is called self-actuation and is characteristic of high RF power.

To model the self-actuation mechanism, we follow the ideas presented in [37]. Consider an input power

$$P_{in} = \frac{V_0^2}{2Z_0} \tag{3.4}$$

to the cpw line underneath the switch (see Fig. 3.3). Since the switch is in the up-

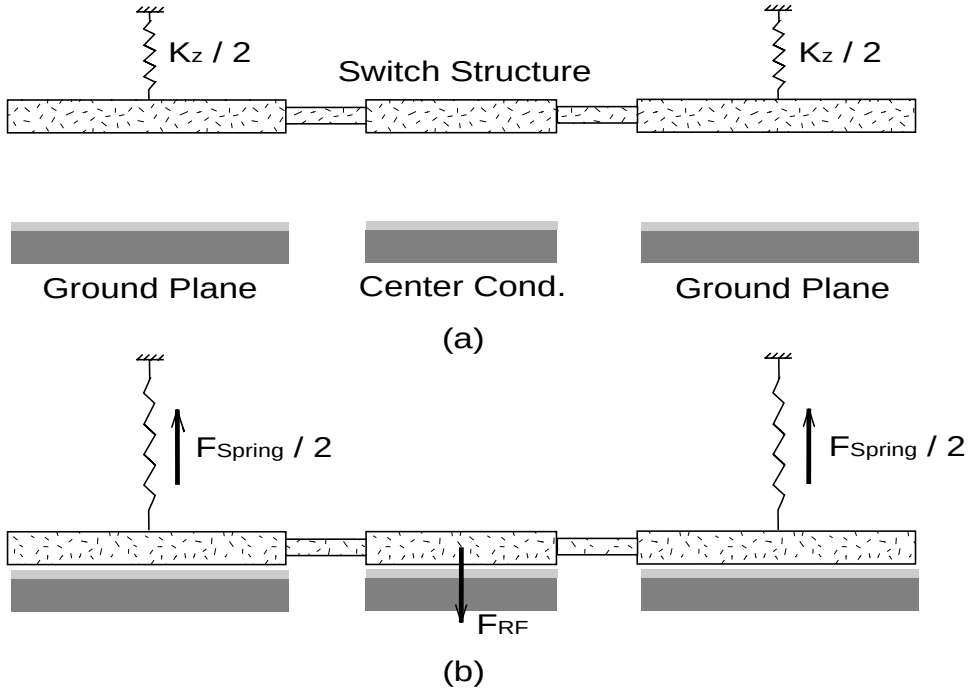


Figure 3.3: Schematic representation of the self-actuation mechanism. (a) The switch is initially in its up state over a cpw line. (b) The incident power on the cpw line is higher than the pull-down power and the switch is actuated with no bias voltage present.

state, almost zero power will be reflected. Equations (3.2), (3.3) and (3.4) readily show that the required power to actuate the switch is

$$P_{act} = \frac{8K_z g_0^3}{27\epsilon_0 A_{RF} Z_0} \tag{3.5}$$

where A_{RF} is the switch area that interacts with the applied RF power. We will refer to this power as the minimum pull-down RF power.

Although for typical air-bridge-type switches [4, 14] A_{RF} can be approximated as the switch area over the center conductor A_{cc} of the cpw line (fringing fields are ignored in this approximation), it is not straightforward that this approximation holds for the switch of Fig. 2.1. Since this switch is not directly connected to the cpw ground planes, part of the total attractive force will be distributed on the switch pads

that are suspended over the cpw ground planes. Whereas this may initially suggest that the value of A_{RF} used in equation (3.5) has to be larger than A_{cc}, this is not necessarily true. The reason lies in the fact that equation (3.5) assumes a potential difference of $V_{eq} = V_0/\sqrt{2}$ between the switch and the center conductor, which is not the case for our switch. Our switch is not anchored to the ground planes and, therefore, its potential is higher than zero. Consequently, the potential difference between the switch and the center conductor will be lower than V_{eq}.

These arguments suggest that an equivalent value of the area A_{RF} – suitable for equation (3.5)– can be calculated by comparing the actual attractive force F_{actual} with the well-known parallel-plate approximation

$$F_{pp} = \frac{1}{2}\frac{\epsilon_0 w V_{eq}^2}{g_0^2} \quad [N/m] \tag{3.6}$$

where w is the width of the cpw center conductor. The actual attractive force can be calculated by using a quasi-static approximation as sketched in Fig. 3.4. The switch beam in this simulation is placed 4 μm above the cpw line and is also treated as a floating conductor with zero total charge. This represents the fact that the switch is not in direct contact with the cpw line. We solved this electrostatics problem numerically by Ansoft's Maxwell code [42]. The cpw line was excited with a total voltage difference of 1 V (see Fig. 3.4) and the resulting attractive force was calculated to be

$$F_{actual} = 16.47\ \mu N/m \tag{3.7}$$

Using the same geometrical parameters and with $V_{eq} = 1$ V equation (3.6) results in

$$F_{pp} = 16.60\ \mu N/m \tag{3.8}$$

Comparing equations (3.7) and (3.8) we conclude that for our switch the following equation

$$A_{RF} \simeq A_{cc} \tag{3.9}$$

is a very good approximation to be used in equation (3.5).

It is also interesting to note that in the design shown in Fig. 2.1 the bias voltage is primarily applied between the cpw ground planes and the switch pads above them. As a result, the switch area responsible for the DC actuation A_{DC} is significantly larger than A_{RF}. In particular, as shown by the geometry of Fig. 2.1,

$$A_{DC} = 2A_{gp} \tag{3.10}$$

where A_{gp} is the area of the switch pad above each of the ground planes. Additionally,

$$A_{gp} = 4A_{cc} \tag{3.11}$$

Consequently, equations (3.9), (3.10) and (3.11) lead to

$$A_{DC} \simeq 8A_{RF} \tag{3.12}$$

This is a significant advantage between this design and traditional cpw fixed-fixed beam switches [4, 14] where

$$A_{DC} \simeq A_{RF} \qquad \text{(fixed-fixed beam cpw switches)} \tag{3.13}$$

Since A_{DC} and A_{RF} control the actuation voltage and pull-down power respectively (see equations (3.3) and (3.5)), de-coupling of these areas significantly improves the design flexibility for this switch. Compared to the fixed-fixed beam geometries, for instance, a much higher RF pull-down power can be achieved for a given actuation

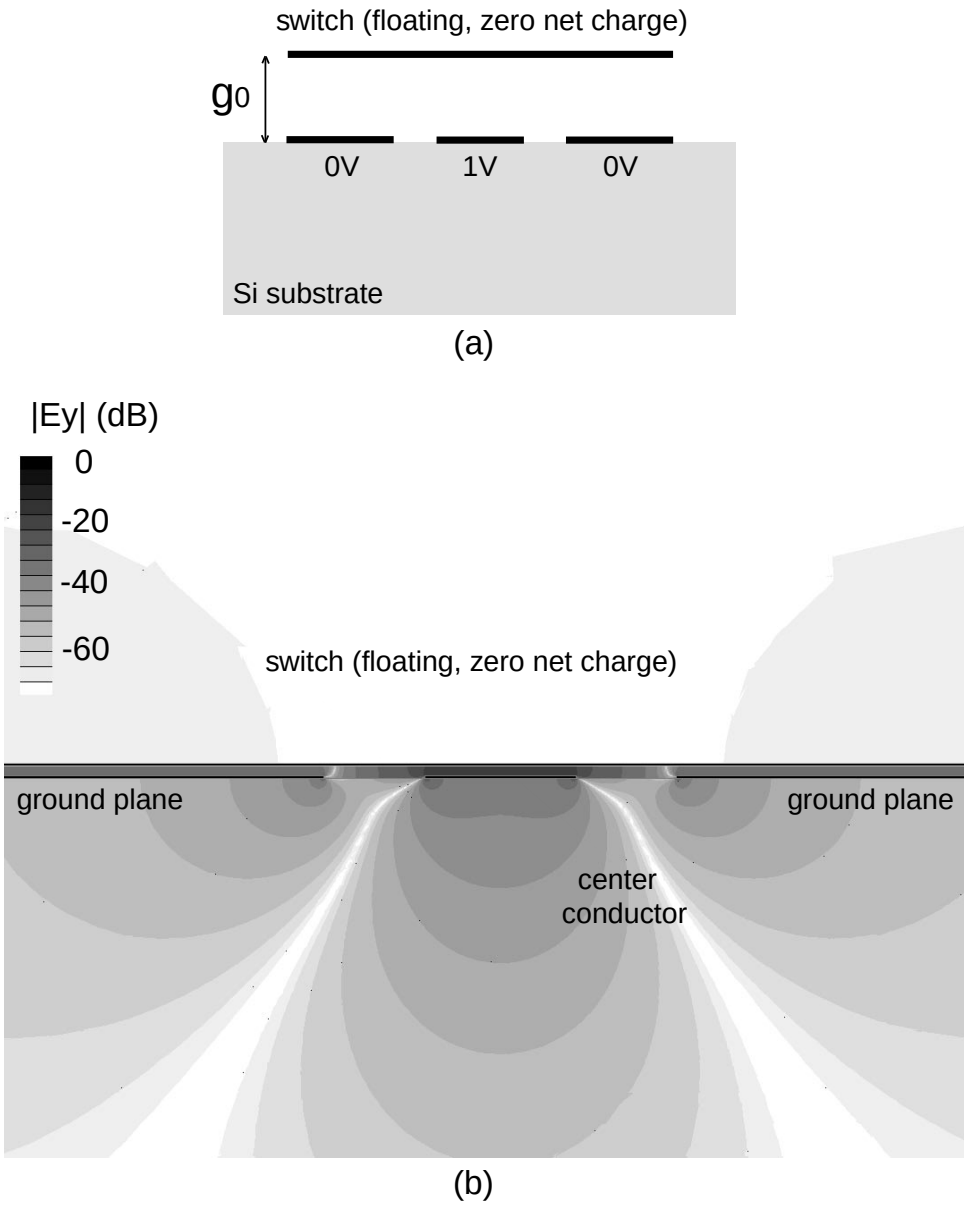


Figure 3.4: (a) 2D quasi-static simulated model (not drawn to scale for clarity) of the switch over the cpw line for field and force calculations. (b) Detail of the simulated magnitude of the electric field vertical component. The results of this simulation were used to calculate the total attractive force between the switch and the cpw line.

voltage. Equivalently, a much lower actuation voltage can be obtained for a given spring constant and pull-down power. Typical values for A_{DC} and A_{RF} as well as for other switch parameters are given in Table 3.1. On the other hand, the drawback of

Table 3.1: Typical parameters for the switches analyzed in this chapter

Center conductor pad (A_{cc})	250×60 μm^2
Ground plane pad A_{gp}	250×250 μm^2
Spring constant[a] – 1 meander (K_{z1})	26.9 N/m
Spring constant – 2 meanders (K_{z2})	14.5 N/m
Spring constant – 3 meanders (K_{z3})	8.6 N/m
Spring constant – 4 meanders (K_{z4})	3.6 N/m
Spring constant – 5 meanders (K_{z5})	1.1 N/m
Mean switch height (g_0)	5 μm
CPW Line impedance (Z_0)	50 Ω
Down-state capacitance	0.8 pF
Dielectric layer thickness (t_d)	2000 $\mathring{A}$
Effective dielectric constant (ϵ_r)	7.5
Extracted air-gap[b] (d_{gap})	600 $\mathring{A}$

[a]All the spring constants are extracted from measurements in [41]. They are also presented in Chapter 2.

[b]Extracted by comparing the down-state capacitance and the capacitance that would have been achieved if the switch had perfect contact with the dielectric layer underneath it.

this approach is that the achieved down-state capacitance is slightly reduced by the series combination of the capacitances C_1 and C_2, where C_1 (C_2) is the capacitance between the center conductor (ground plane) and the switch pad above it. The achieved capacitance is

$$C = \frac{C_1(2C_2)}{C_1 + 2C_2} = 0.89C_1 \tag{3.14}$$

since $C_2 = 4C_1$ for the geometry of Fig. 2.1. This shows that for a 10% reduction in the down-state capacitance, the actuation voltage can be reduced by a factor of $\sqrt{8} = 2.83$ for a given spring constant and maximum sustained RF power.

One more point that needs to be addressed with regard to equation (3.5) is the treatment of the 8 μm holes in the switch structure. These holes facilitate the switch release process, partially relieve the residual stress in the structure and allow the air underneath the switch to escape during actuation [41]. However, they also reduce

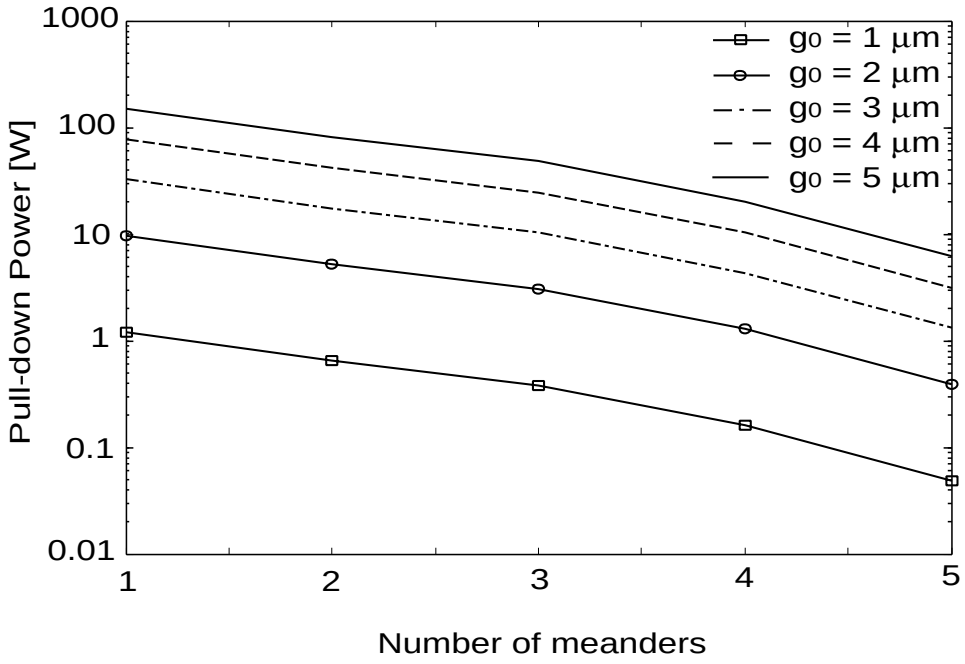


Figure 3.5: Calculated minimum required RF power to cause self-actuation as a function of the number of meanders and gap from the ground planes.

the capacitance between the switch and the cpw line. Their effect is only of minor importance in the up-state, because of the fringing fields that "fill" the area of the holes. Their effect on the down-state capacitance, however, is significant since the dielectric layer thickness is very small and the fringing field negligible. Consequently, the following formulas are used throughout this work for A_{RF}

$$A_{RF} = \begin{cases} 250 \times 60 = 15,000\ \mu m^2 & \text{up state} \\ 8,800\ \mu m^2 & \text{down state} \end{cases} \tag{3.15}$$

Fig. 3.5 shows the minimum calculated RF power required to cause self-actuation for switches with one to five meanders and for various gaps. The parameters used for these calculations are given in Table 3.1. This plot reveals the significance of allowing enough distance between the switch and the RF circuit, particularly for low spring constant switches.

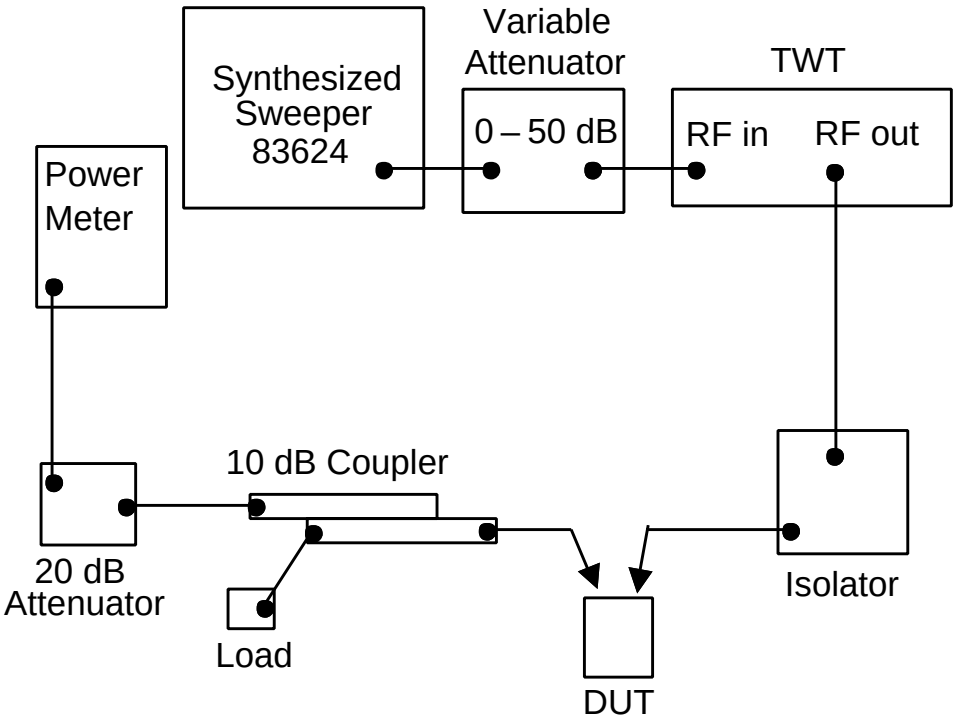


Figure 3.6: X-band power measurement set-up.

3.3.2 Experimental Results and Discussion

The experimental characterization of the switches was performed by the measurement set-up shown in Fig. 3.6. Sergio Pacheco fabricated all the switches used in these measurements, developed the necessary measurement set-up and performed all the measurements. The RF signal in this set-up is produced by an X-band synthesized sweeper. After passing a variable 0–50 dB attenuator, it is amplified by an X-band Travelling Wave Tube (TWT) amplifier that produces a maximum power level of about 7 W. The amplified signal is then guided through an isolator to the switch under test. A portion of the output signal is then recorded to a power meter through a 10 dB coupler and a 20 dB attenuator. The measurements were performed at 10 GHz because of the limitations imposed by the TWT amplifier. Although the switch provides an isolation of only 3–4 dB at this frequency, this isolation is

significantly higher than the measurement error and therefore we were still able to determine any self-actuation problems.

Switches with one to four meanders were tested with this set-up and were actuated with a bias voltage of 10–40 V. The mean gap g_0 was approximately 4.8–5.2 μm for all the switches. All the switches were initially tested in the up-state with an input power of approximately 0.7 mW. Then we slowly increased the power up to a maximum of about 5.5 W by decreasing the attenuation of the variable attenuator. No self-actuation was observed for any of the switches at any stage. The fact that the maximum recorded power was less than 7 W is explained by the losses of the connections and the cables introduced between the TWT and the DUT. We were also limited by the maximum output power of the TWT amplifier (7 W) and therefore we could not experimentally observe any self-actuated switches. The same procedure was repeated when the switch was in the down state. No catastrophic failure of the switch or the dielectric underneath it was observed in these measurements. Only for high power levels (higher than 3 W) slight bending of the switch springs was observed. The springs returned to their original positions when the power was turned off. This is due to the thermal effects associated with the heat generated due to the input power. Fig. 3.7 shows the recorded results for a typical switch with three meanders versus the reading of our variable attenuator. The 3–3.5 dB difference between the power levels of the switch up and down states is explained by the switch isolation at 10 GHz (see Fig. 3.2). These results agree well with our theoretical expectations, since according to equation (3.5) an input power of 48 W would be required for self-actuation.

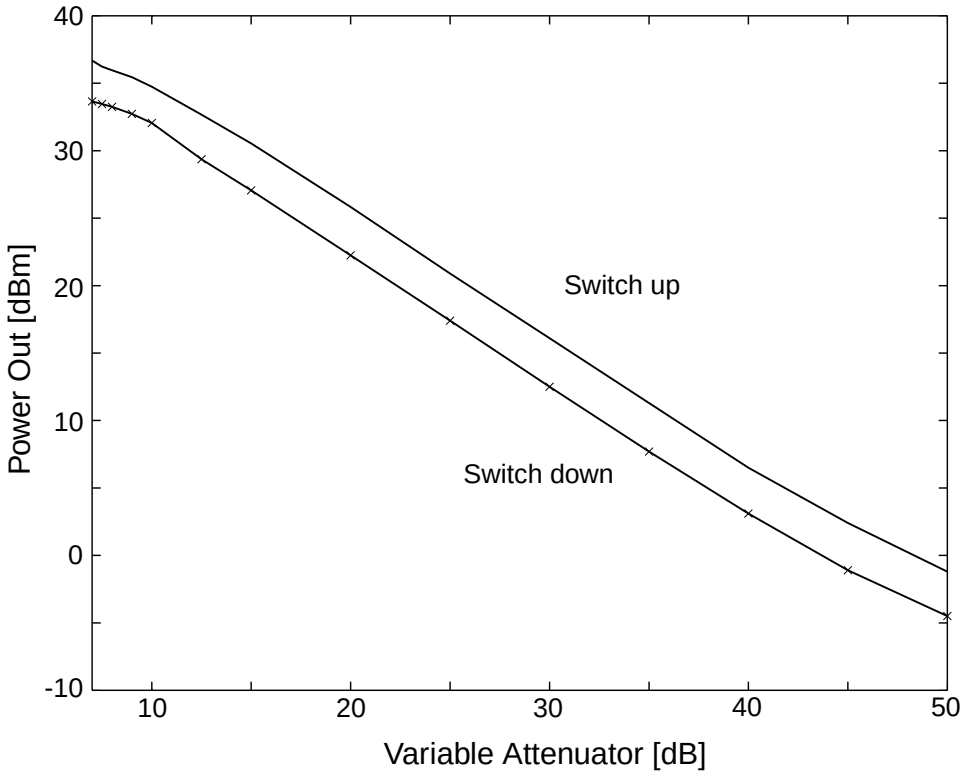


Figure 3.7: Measured power levels for the up and down switch states.

3.4 Switch Stiction Due to High RF Power

3.4.1 Modeling

Although the minimum pull-down power may be in the order of several watts, this is not the case for the hold-down power, i.e. the minimum RF power required to hold a switch in the down position without any bias voltage. A simple schematic for this scenario is shown in Fig. 3.8. Initially it is assumed that the switch is in the up-state and an incident power P_{in} is applied to the cpw line underneath the switch. We also assume that this power is not sufficiently high to cause self-actuation, i.e. $P_{in} < P_{act}$. Then the switch is actuated by a bias voltage higher than the pull-in voltage (Fig. 3.8b). An effective air-gap of d_{gap} has been introduced to model the lack of perfect contact between the switch and the dielectric layer underneath it. This

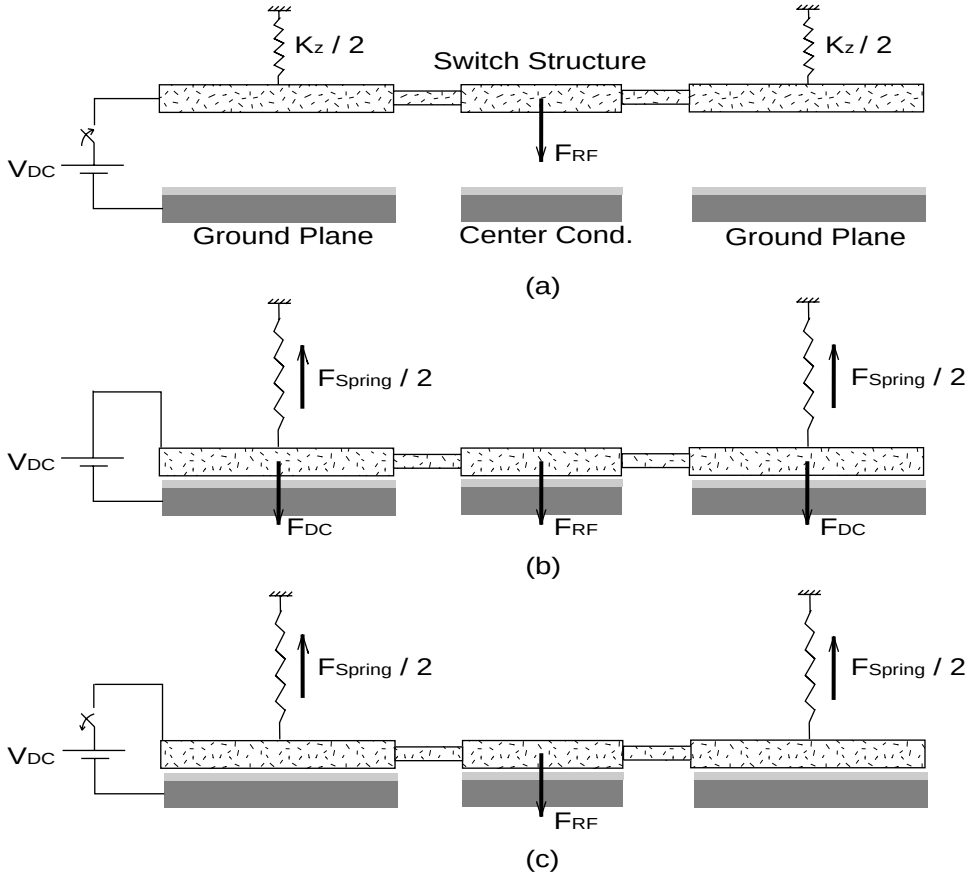


Figure 3.8: Simplified scenario for hold-down power calculations. (a) Initially the switch is in the up-state and an incident RF power (less than the pull-down power) is applied to the line underneath it. (b) At some point a bias voltage (higher than the actuation voltage) is applied and the switch is actuated. (c) The bias voltage is removed afterwards, but the switch remains in the down state since the RF power exerts an RF force on the switch higher than the restoring force.

air-gap is due to the surface roughness between the contact areas and the inability of the switch to conform perfectly on the dielectric layer underneath it. For example, our switches in this study were approximately 3 μm thick and no perfect conforming could be achieved. The relatively low measured isolation (Fig. 3.2b) is mostly due to this factor. By comparing the switch down-state capacitance (0.8 pF) and the capacitance that could have been achieved if the switch had perfect contact with the dielectric layer underneath it (2.6 pF), an effective air gap of about 600 $\mathring{A}$ can be

deduced. The forces applied to the switch when in its down state are given by [37]

$$\begin{aligned} F_{RF} &= -\frac{1}{2}\frac{\epsilon_0 A_{RF}|V_{sw}\,|^2}{\left(d_{gap}+t_d/\epsilon_r\right)^2} \\ F_{Spring} &= K_z g_0 \\ F_{DC} &= \frac{1}{2}\frac{\epsilon_0\left(A_{DC}\right)V_{DC}^2}{\left(d_{gap}+t_d/\epsilon_r\right)^2} \end{aligned} \tag{3.16}$$

where V_{sw} is the switch RF voltage. When the DC voltage vanishes, the switch will return to its initial state unless $|F_{RF}| \geq |F_{Spring}|$, or equivalently,

$$\frac{1}{2}\frac{\epsilon_0 A_{RF}|V_{sw}\,|^2}{\left(d_{gap}+t_d/\epsilon_r\right)^2} \geq K_z g_0 \tag{3.17}$$

Equations (3.2) and (3.4) cannot be applied directly in this case to estimate V_{sw} since they are associated only with the incident power on the switch. The switch being in the down-state, however, generates a reflected voltage, which greatly reduces the total RF voltage across it. Consequently the total voltage can be calculated as $V_{sw} = V_{RF}\left(1+\Gamma\right)$, where V_{RF} is the amplitude of the incident wave and Γ is the reflection coefficient due to the shunt switch capacitance on the line. Standard transmission line theory yields [37]

$$|V_{sw}| = \frac{|V_{RF}|}{\sqrt{1+\left(\pi f C Z_0\right)^2}} \tag{3.18}$$

For all frequencies below 80 GHz this voltage can be considered almost constant along the switch width, since the switch is at least an order of magnitude smaller than the wavelength. Combining (3.2), (3.4),(3.17), and (3.18) we get the following formula for the necessary RF power to hold the switch down

$$P_h = \frac{2K_z g_0\left(d_{air}+t_d/\epsilon_r\right)^2\left[1+\left(\pi f C_D Z_0\right)^2\right]}{\epsilon_0 A_{RF} Z_0} \tag{3.19}$$

Table 3.2: Measured and calculated hold-down RF power for switches with one, three and five meanders

Meanders	P_h [mW] (Calc.)	P_h [mW] (Meas.)
1	1335	—
3	426	500
5	54.6	63

3.4.2 Experimental Results and Discussion

The experimental set-up of Fig. 3.6 was also used to measure the hold-down RF power. Sergio Pacheco fabricated all the switches used in these measurements and performed all the measurements. In this case, however, the maximum incident RF power was limited to 0.8 W. The reason is that we wanted to compare these measurements with the experiments presented in Section 3.5, where the maximum applied power was limited to 0.8 W. We tested switches with one, three, and five meanders with this set-up and the results are shown in Table 3.2. No power-stiction problems were observed with one-meander switches, which is in agreement with our theoretical expectations. Furthermore, the measured and calculated hold-down powers for three- and five-meander switches are also in reasonable agreement with the calculated powers from equation (3.19). The minor discrepancies (in the order of 15%) are due to the variations in height and the down-state capacitance of the measured switches as compared to the nominal values used for the theoretical calculations.

These results indicate that the 1-D model is physically meaningful and can be used for predicting the performance of the same switches at different frequency bands. For instance, equation (3.19) shows that the hold-down RF power is proportional to the square of the operating frequency. Consequently, if the same measurements had been performed at 40 GHz, the hold-down power for switches with one and five meanders would have been 13.6 and 0.55 W respectively. At this frequency the switch presents a much improved short for the RF signal, hence limiting the RF voltage across it to

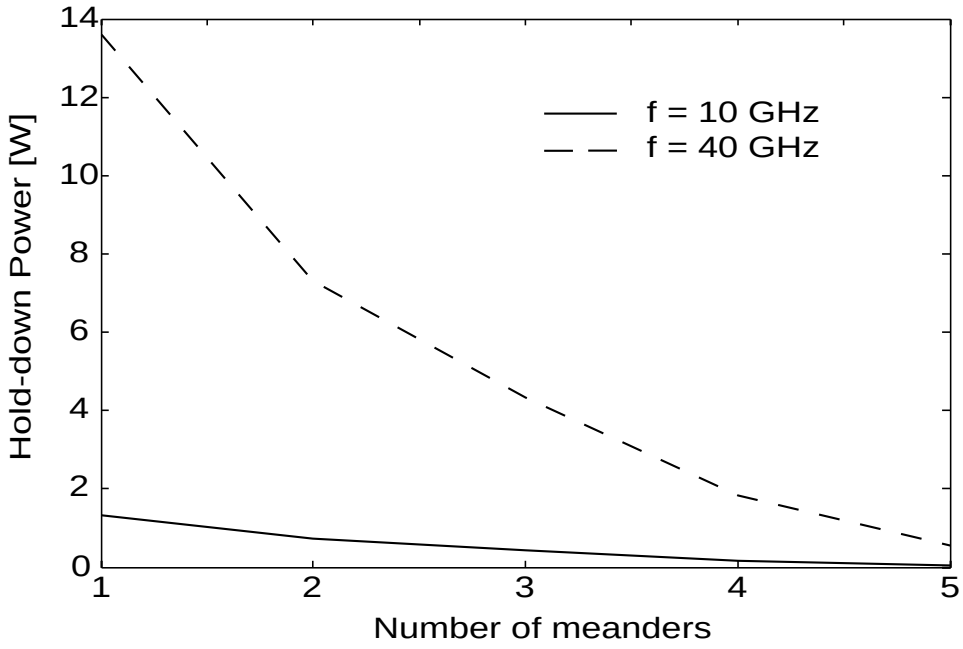


Figure 3.9: Simulated hold-down power for the same switch at two different frequencies. The sustained hold-down power is higher at 40 GHz because the switch presents a better short circuit at that frequency.

a much smaller value than before. Fig. 3.9 graphically illustrates these results. One has to be careful, however, interpreting these simulations. Thermal issues, for example, [43, 44] may cause different problems well before high power levels are reached. Additionally, the dielectric layer underneath the switch is typically a temperature-sensitive material and it may lead to additional stiction problems for sufficiently high temperatures. This particularly applies to the case of non-heat conducive substrates (e.g. quartz). These thermal effects have not been taken into account in our analysis and their study requires a completely different treatment.

One more interesting phenomenon is related to the hold-down power as a function of the switch down-state capacitance. Typically the down-state capacitance is limited by the ability of the switch to conform on the dielectric underneath it and the surface roughness of the dielectric and metals. Both of these factors limit the maximum capacitance by limiting the contact between the switch and the dielectric layer. It

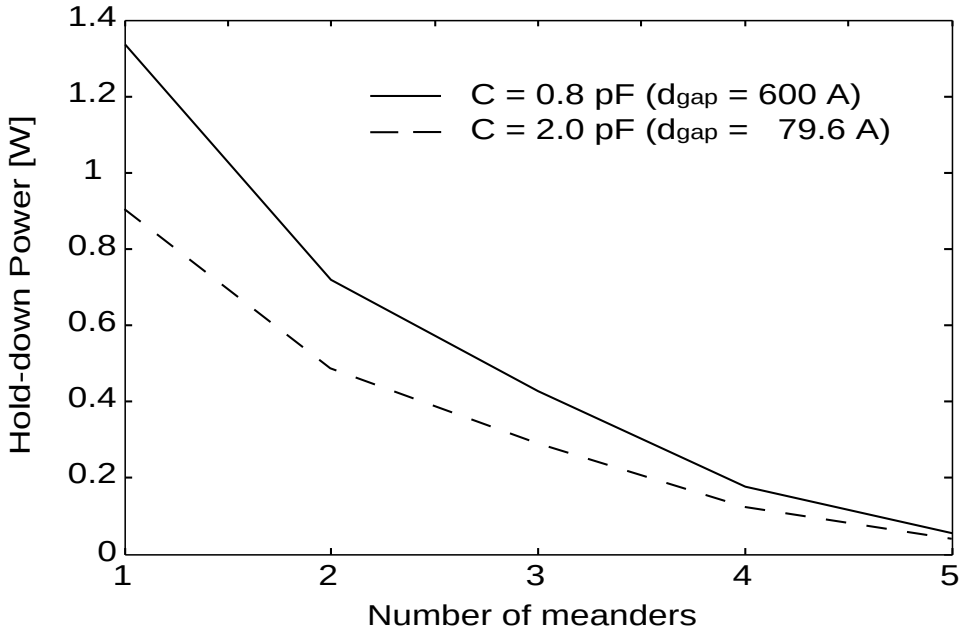


Figure 3.10: Simulated hold-down for different air-gaps. A smaller air gap leads to a higher down-state capacitance but also to a lower hold-down RF power.

has already been mentioned that these effects can be modelled by an equivalent air-gap d_{gap} that typically varies between 50 and 1000 $\mathring{A}$. Higher down-state capacitance, therefore, can be achieved by either increasing the switch area (which will also increase the up-state insertion loss) or by decreasing the equivalent air-gap. If the switch area is increased, but the air-gap remains essentially the same, higher hold-down power can be achieved for reasons described in the previous paragraph. On the other hand, if the switch capacitance is increased by limiting the effective air-gap, a lower hold-down power may actually be obtained. The reason is that although a lower RF voltage exists across the switch, due to its higher capacitance, the equivalent RF force is also higher (see equation (3.16)). Fig. 3.10 shows two examples using the values of Table 6.1 for capacitances of 0.8 and 2 pF. These correspond to air-gaps of 600, and 79.6 $\mathring{A}$ respectively. This figure clearly shows the trade-offs between the maximum down-state isolation and power stiction problems, particularly for switches with spring constant higher than 10 N/m.

3.5 Switch with Top Electrode

3.5.1 Design and Fabrication

The spring-restoring force is the only force that has been considered in the literature so far for returning the switch to its initial state after it has been actuated. This force can be relatively weak for low-voltage switches, especially if the moving distance is limited (less than 2 μm). As a result, it may be insufficient for reliable switching in high-power applications. Sergio Pacheco and Linda P.B. Katehi introduced the idea of having a top electrode fabricated over the switch. The switches and fabrication process presented in this section have been contributed by Sergio Pacheco.

The top electrode is electrically isolated from the switch and the cpw line underneath it and it can be used to pull the switch from the down-state to the up position. Fig. 3.11 shows the fabrication process followed for this electrode after the switch is completed, but before it is released. In particular, in the first stages (the initial process can be found in [15]) the circuit underneath the switch is deposited, followed by the deposition and patterning of the dielectric layer (Si_3N_4). Spinning and patterning of the first polyimide layer (first sacrificial layer) follows and then a seed layer of Ti/Ni is deposited. This seed layer is electroplated to define the switch structure. After the seed layer is removed, a SiO_2 (approximately 5000 $\mathring{A}$ thick) layer is sputtered and patterned with an RIE process on top of the switch. This dielectric layer is introduced to prevent any DC short-circuit between the switch and the top electrode. A new sacrificial layer of polyimide PI2545 is then spun at 3–4 krpm for 30 sec. and cured at 150°C for 15 min. This results in a thickness of approximately 2–2.5 μm. It was experimentally found that layers with smaller thicknesses were particularly difficult to remove afterwards. The thickness of the first sacrificial layer was also adjusted to 1.4–1.6 μm in order to limit the maximum distance between the top-electrode and the cpw line to about 4 μm. The anchor points of the top electrode are then patterned

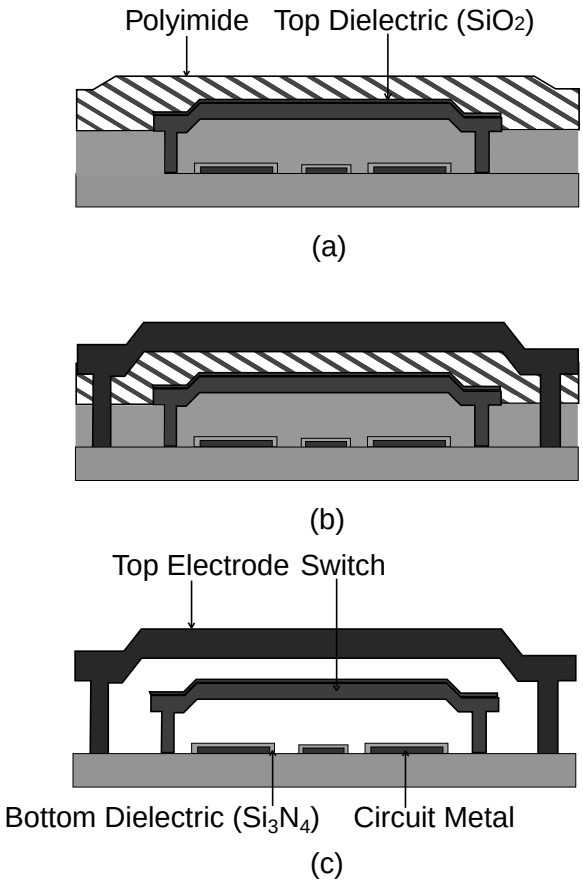
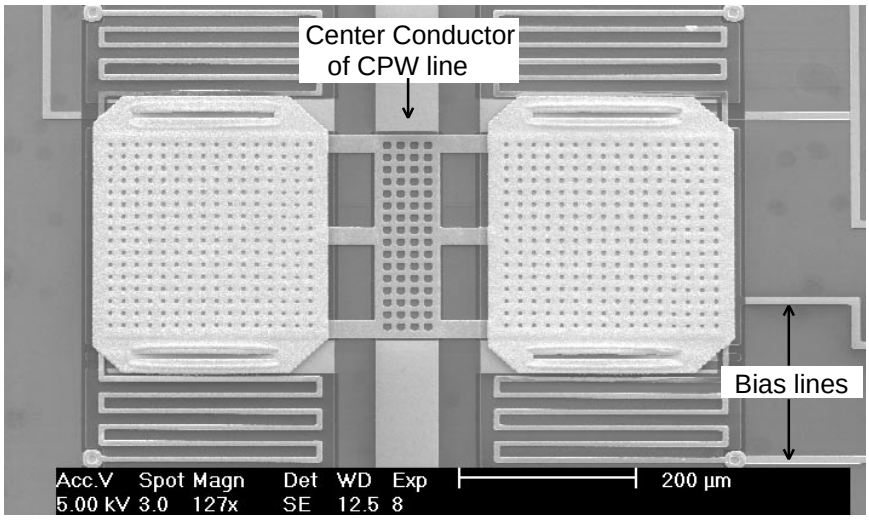


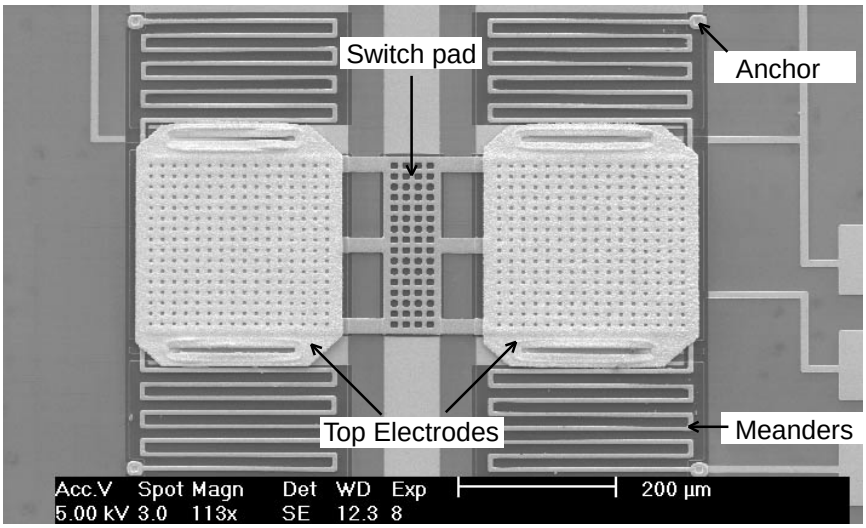
Figure 3.11: Fabrication process of the switch top electrode. (a) A SiO_2 layer is sputter deposited and defined on top of the switch. Then a polyimide layer is spun deposited and serves as a second sacrificial layer. (b) The anchor points of the top electrode are defined. A seed layer of Ti/Au/Ti is then deposited and electroplated to define the top electrode. (c) The polyimide layers are etched and the structure is dried with a CO_2 supercritical process.

with a process very similar to the one followed for the switch anchor points. The next step is to deposit a seed layer of Ti/Au/Ti (500/2000/500 $\AA$). The seed layer is electroplated with Au typically up to 4–5 μm to shape the top-electrode. Eventually the two sacrificial layers are etched in hot PRS2000 and the whole structure is dried with a standard supercritical CO_2 process.

Fig. 3.12 shows two examples of fabricated switches (with three and four meanders) with top electrodes. Due to the switch symmetry, one electrode above each of the



(a)



(b)

Figure 3.12: Two examples of switches with fabricated top electrodes.

switch actuation pad is fabricated. However, no top electrode is placed above the center conductor pad, because such an electrode would deteriorate the RF performance of the switch due to additional parasitic capacitance. This does not significantly reduce the electrostatic force between the top electrodes and the switch, since the center conductor pad is significantly smaller that the other two pads. An additional advantage of the top electrodes is that they are extremely stiff, hence enhancing switch

stabilization. Even without accounting for any axial stresses, the calculated spring constant for each of these electrodes is in the order of 2300 N/m. A DC voltage in excess of 230 V would be, therefore, required for any significant movement.

3.5.2 Modeling

Besides switch stabilization, the main purpose for introducing the top electrodes is to enhance the power handling capabilities of the low-voltage switches. The most useful (and at the same time worst-case) scenario that was theoretically and experimentally investigated is illustrated in Fig. 3.13. It is assumed that the switch is initially in the down-state position, either because of self-actuation, or because of DC biasing. In both cases, the RF power is considered sufficient to counteract the restoring force, forcing the switch to remain down. To move the switch in the up-state, a DC voltage is applied between the switch and the top electrode. If this voltage is sufficiently high, the switch will move upwards and eventually touch the top electrode. For obtaining general force expressions, we assume that the switch has moved by a distance z from the dielectric layer (Fig. 3.13). For the following equations $g_0 = 1.5$ μm is the distance between the circuit and the initial switch state ($F_{spring} = 0$) and $g_{up} = 4$ μm is the distance between the circuit and the top electrode. The forces acting on the switch are then given by

$$\begin{aligned} F_{RF} &= -\frac{1}{2}\frac{\epsilon_0 A_{RF}|V_{sw}|^2}{\left(d_{gap} + t_d/\epsilon_r + z\right)^2} \\ F_{Spring} &= K_z\left(g_0 - z\right) \\ F_{UP} &= \frac{1}{2}\frac{\epsilon_0 A_{DC} V_{up}^2}{\left(g_{up} + t_{d2}/\epsilon_{r2} - z\right)^2} \end{aligned} \tag{3.20}$$

The meaning of the symbols is the same as in formula (3.16), except a) V_{up} is the applied DC voltage between the top electrodes and the switch, and b) t_{d2} and ϵ_{r2}, are the thickness and dielectric constant of the SiO_2 film underneath the top electrodes.

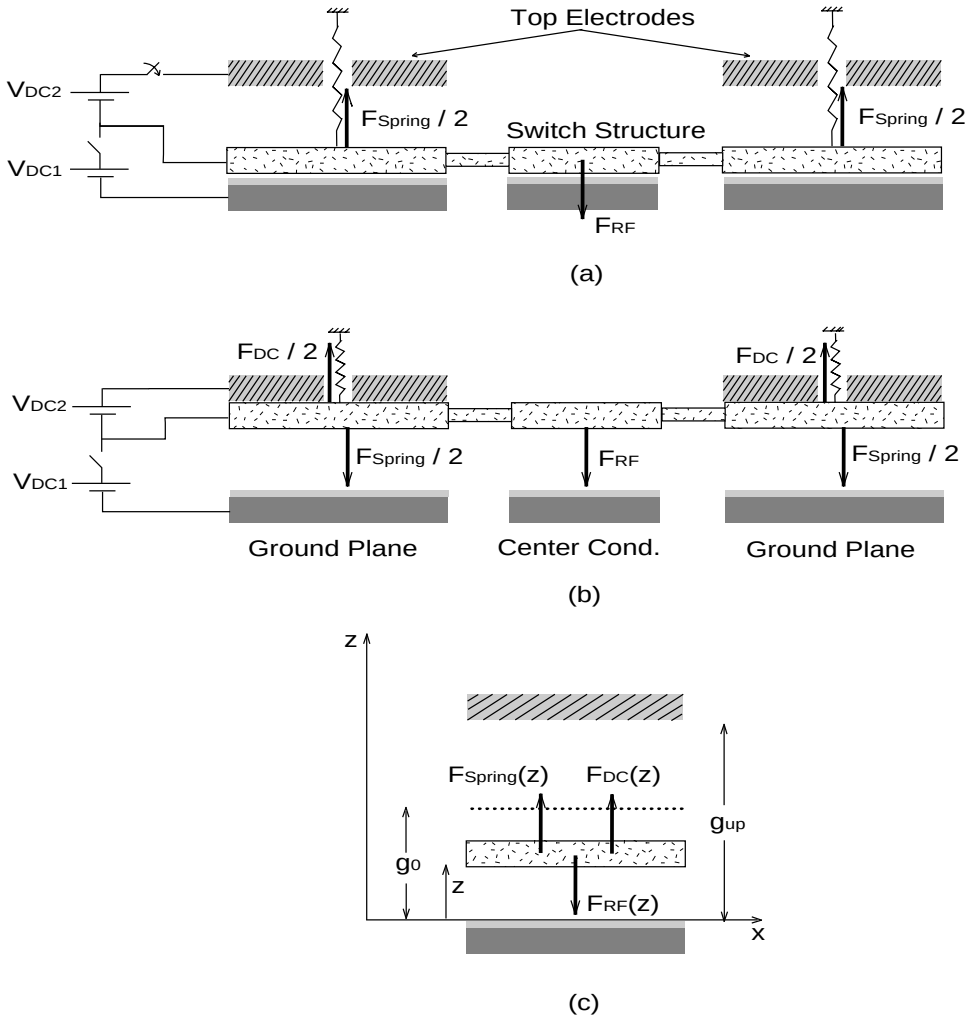


Figure 3.13: Simplified scenario for modelling the top-electrode effect in power-stiction problems. (a) The switch is in the down state either by self-actuation or by DC biasing. (b) A DC voltage is applied between the switch and the top electrode and the switch is moved upwards and stops to the top electrode. (c) Simple 1-D schematic that demonstrates the geometrical details of the switch design

We also have to note that A_{DC} is smaller than $2A_{gp}$ because of the holes that exist in both the switch and the top electrode. Consequently the fringing fields are weak in the areas of the holes and can be ignored. Hence A_{DC} includes only the overlapping area between the top electrodes and the switch and is given by $A_{DC} = 2 \times 38,0000\ \mu m^2 = 76,000\ \mu m^2$.

Based on these equations, a simple 1-D dynamic simulation can be performed,

similar to the one presented in [41] for switching speed calculations. However, for low spring-constant switches, the restoring force can be ignored for high RF power levels. Consequently, an analytical expression for the required top-electrode voltage as a function of the incident RF power and the switch geometry can be obtained. As the following results will show, this is a valid assumption in our case. The minimum required top-electrode DC voltage to pull the switch up is given by the (approximate) requirement $F_{UP} \geq F_{RF}$, or equivalently,

$$V_{up} \geq \frac{g_{up} + t_{d2}/\epsilon_{r2}}{d_{gap} + t_d/\epsilon_r} \sqrt{\frac{A_{RF}}{A_{DC}} \frac{Z_0 P_{in}}{1 + (\pi f C Z_0)^2}} \tag{3.21}$$

This equation underlines the significance of separating the DC from the RF pads. Additionally, it underscores the importance of obtaining a good RF short-circuit in minimizing the required pull-up voltage. For example, if

$$\pi f C Z_0 \gg 1 \tag{3.22}$$

and

$$C = \frac{C_1(2C_2)}{C_2 + 2C_2} \simeq C_1 = \frac{\epsilon_0 A_{RF}}{d_{gap} + t_d/\epsilon_r} \tag{3.23}$$

(where C_1 and C_2 are defined in 5.1), equation (3.21) yields

$$V_{up}^{min} \simeq \frac{1}{\pi f C_{up}} \sqrt{\frac{A_{RF} P_{in}}{A_{DC} Z_0}} \tag{3.24}$$

where

$$C_{up} = \frac{\epsilon_0 A_{RF}}{g_{up} + t_{d2}/\epsilon_{r2}} \tag{3.25}$$

is the fictitious capacitance between the switch center conductor pad and an imaginary electrode at a distance g_{up} from it.

3.5.3 Experimental Results and Discussion

Sergio Pacheco experimentally validated these results by fabricating and testing several switches with top electrodes using the experimental set-up of Fig. 3.6. Although at 10 GHz the switch provides a typical isolation of only 3–4 dB, the advantages of the top electrode can still be exposed. These measurements were done with the RF power continuously on (hot switching) by alternating the bias voltage between the switch/the cpw ground plane, and the switch/top electrode. Mostly switches with five meanders were tested, since these presented the lowest spring constant. Fig. 3.14 shows typical results of the experimentally measured top-electrode voltage that was needed to pull up a five-meander switch with input power of up to 0.8 W. At this power, a voltage of 68 V was required to pull the switch up, which was slightly lower than the break-down voltage of the SiO_2 film underneath the top electrode. This was the limiting factor of applying more power to the system. Fig. 3.14 also shows the theoretically calculated pull-up voltage based on equation (3.21) and on dynamic simulations that included the spring-constant force given in (3.20). In both simulations the dielectric layers underneath (2000 $\mathring{A}$ of Si_3N_4) and above the switch (5000 $\mathring{A}$ of SiO_2) were also taken into account. This figure clearly shows that the theoretical results agree very well with the measured values of the pull-up voltage. Additionally, it validates the assumption of ignoring the switch spring constant for these calculations, as equation (3.21) is obviously an excellent approximation of the pull-up voltage.

It is worth noting that the measured and simulated pull-up voltages are substantially higher than the measured pull-in voltage of 6 V [41]. For instance, for an input power of 0.8 W, the pull-up voltage was measured to be almost 70 V. Although this may initially seem as a contradiction of the low-voltage properties of the switch, it is important to remember that, as equation (3.21) shows, the pull-up voltage depends heavily on the frequency of operation and down-state switch capacitance. The presented low-voltage switch is a high-frequency device and is not well suited for X-band

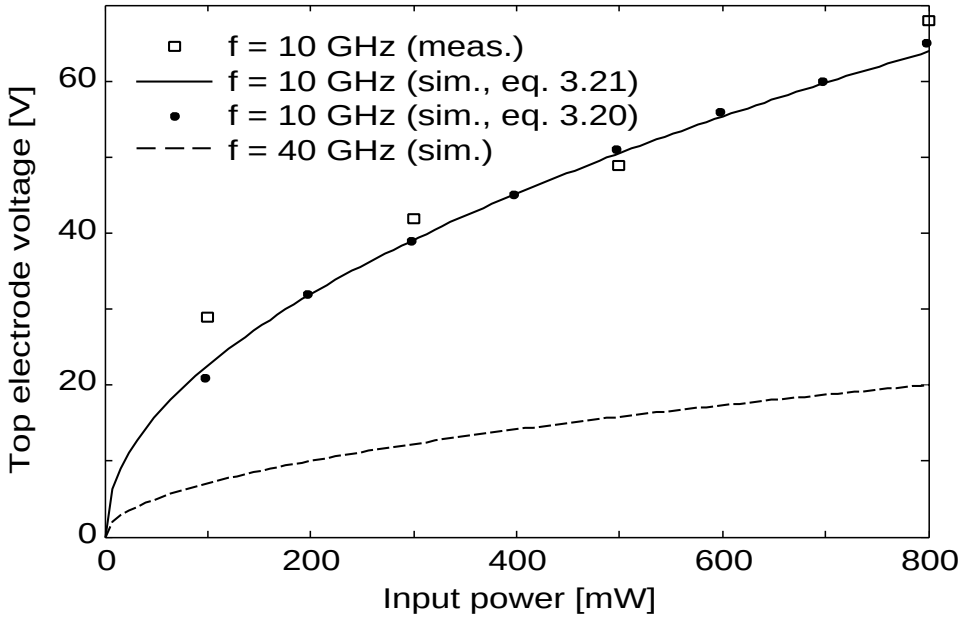


Figure 3.14: Measured and simulated pull-up voltage for switches with five meanders and fabricated top-electrodes. The required pull-up voltage is significantly lower at 40 GHz than at 10 GHz, because the RF voltage across the switch is substantially reduced at 40 GHz.

operation. The switch isolation is only 2–5 dB at this band. However, our measurements had to be performed at 10 GHz, because of the TWT frequency of operation. Despite the low switch isolation at this band, these measurements prove that our 1-D model is physically correct and can be successfully used for predicting the switch performance at different bands. If the same measurements had been performed at 40 GHz, where the switch is more useful with a down-state $S_{21} = -15.5$ dB, the pull-up voltage would have been substantially lower. Fig. 3.14 presents the simulated 40-GHz pull-up voltage for the same switch and under the same conditions. The pull-up voltage is now 10 and 20 V for input powers of 0.2 and 0.8 W respectively. This analysis shows that a number of power handling issues need to be considered during the design process of an RF MEMS switch.

3.6 Conclusions

The power handling capabilities of RF MEMS switches have been presented in this chapter. In particular an experimental and theoretical investigation of three important cases is presented: a) self-actuation, b) stiction in the down state, and c) hot-switching. For all cases we have demonstrated the significance of separating the DC and RF pads for improved performance. Furthermore, a novel switch structure with a top electrode that substantially increases the hot switching RF power range has been discussed.

CHAPTER 4

High-Isolation Capacitive MEMS Switches and Switch Packets

4.1 Introduction

IN the previous two chapters we presented a low-voltage capacitive MEMS switch and discussed several important issues (such as actuation voltage, residual stress, power handling etc.) associated with its performance. One of the most significant advantages of these type of switches is their very low off-state insertion loss, which is typically less than 0.2 dB up to 40 GHz. As shown in the previous chapter, however, their on-state isolation is typically limited by the down-state capacitance C_D. This down-state capacitance depends on the flatness and smoothness of the MEMS switch as well as the dielectric layer underneath it. If perfect contact and smoothness is assumed, this capacitance can reach the value predicted by the parallel plate model

$$C_{D,max} = \epsilon_0 \epsilon_r \frac{A_{RF}}{t_d} \tag{4.1}$$

where A_{RF} is the equivalent switch area interacting with the RF signal (approximately equal to the area of the pad suspended over the cpw center conductor) and ϵ_r and t_d are the relative permittivity and thickness of the dielectric layer underneath it

respectively. In Chapter 3 we discuss these quantities in more detail. This maximum down-state capacitance is rarely achieved in practice. Instead, a lower capacitance is typically measured (see Chapter 3 for example), which can be modeled by assuming an equivalent air-gap d_{gap} that accounts for both the reduced contact area and the roughness between the MEMS structure and the dielectric underneath it. This model results in a more realistic down state capacitance C_D given by

$$C_D = \epsilon_0 \frac{A_{RF}}{d_{gap} + \frac{t_d}{\epsilon_r}} \tag{4.2}$$

Depending on d_{gap}, the down-state capacitance C_D may be up to 2–3$\times$ smaller than $C_{D,max}$. These issues impose significant challenges in achieving high down-state isolation for frequencies lower than 5–10 GHz, while decreasing d_{gap} is a difficult technological problem.

An alternative approach of obtaining high isolation is investigated in this chapter. This approach is based on the idea of changing the mechanical design of the switch to increase the shunt switch inductance L_p (see Fig. 3.1). If properly designed, a resonant behavior to the down-state S_{21} around the frequency of interest can be obtained. This idea was first presented simultaneously by Peroulis et al. [31] and by Muldavin and Rebeiz [45] in June 2000. Inductances that reach almost 90 pH are presented in this chapter, which result in resonant frequencies as low as 15 GHz. This method produces switches with isolation of 25–30 dB, depending on the switch resistance. If higher isolation is desired, switch-packets can be appropriately designed. Broadband (10–30 GHz) switch packets with 2,3 and 4 switches are presented in this chapter with very high isolation that is only limited by substrate surface waves.

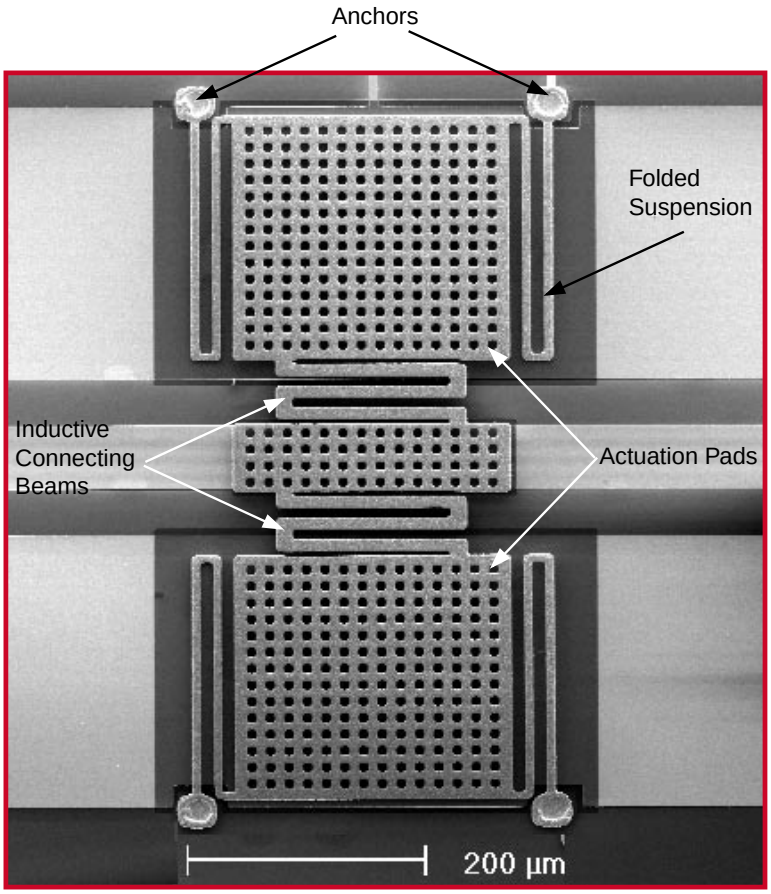


Figure 4.1: Microphotograph of an inductively tuned switch.

4.2 Single Inductively Tuned Switch

The beams connecting the three switch pads (see Fig. 2.1), which we will call inductive connecting beams, play a crucial role in the RF performance of the switch, because they form the path the RF signal has to follow to reach the ground. Consequently, the shunt inductance L_p primarily depends on the geometry of these beams. The six connecting beams, for instance, shown in Fig. 2.1 result in a very low inductance $L_p \simeq 2$ pH. A different design of these beams can significantly increase the value of this inductance. Fig. 4.1 shows an example of such a switch design. This switch was fabricated with the Ti/Ni process described in Chapter 2 with a total thickness of 1.5 μm. The metal of the inductive connecting beams is 10 μm wide and the spacing

is 10 μm as well. To demonstrate the robustness of this design, the switch was also fabricated with 1 μm sputtered Au. The inductive connecting beams in this case had metal width and spacing equal to 8 μm. No catastrophic failure of the switch structure was observed at any point. A number of different meander structures were fabricated and are summarized in Fig. 4.2.

Fig. 4.3 shows the up- and down-state measured and simulated/fitted results for the structure A of Fig. 4.2. The up-state capacitance can be extracted from the up-state reflection coefficient as $C_U = 29$ fF. The down-state capacitance C_D, as well as the inductance L_p and resistance R_p can be found from the down-state measured isolation. The fitted down-state capacitance for this structure is $C_D = 1100$ fF which leads to down/up capacitance ratio of $C_D/C_U = 38$. The fitted inductance is 87 pH, while the resistance R_p is 1.95 Ω. This value is extracted by the maximum achieved isolation of nearly 23 dB at the resonant frequency (16.2 GHz). The fitting of the LCR parameters is best done using an appropriate software (e.g. ADS) and the model shown in Fig. 3.1. It can also be done by simple approximate analytical formulas [37]. Fig. 4.3 also shows the simulated response of the same switch but with $L_p = 2$ pH and $R_p = 0.2$ Ω. The achieved isolation with the inductively tuned design around the resonant frequency is approximately 13 dB higher. Fig. 4.2 shows the extracted results of other fabricated structures. The ability to tune the frequency where the switch presents its maximum isolation is the major advantage of this design.

4.3 Switch Packets: The π-Match

As shown in the previous section, single capacitive shunt switches can typically provide a maximum isolation of 25–30 dB. If a higher total isolation is desired, multiple parallel switches have to be fabricated. Such a technique has been widely adopted in PIN diode reflective switches and phase shifters [46]. The main idea is to use a τ-

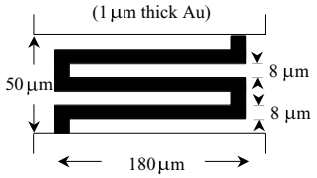
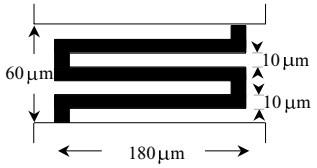
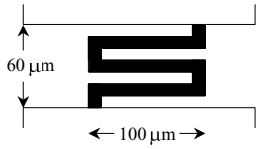
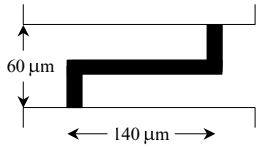
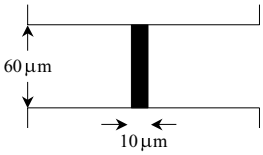
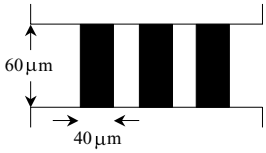
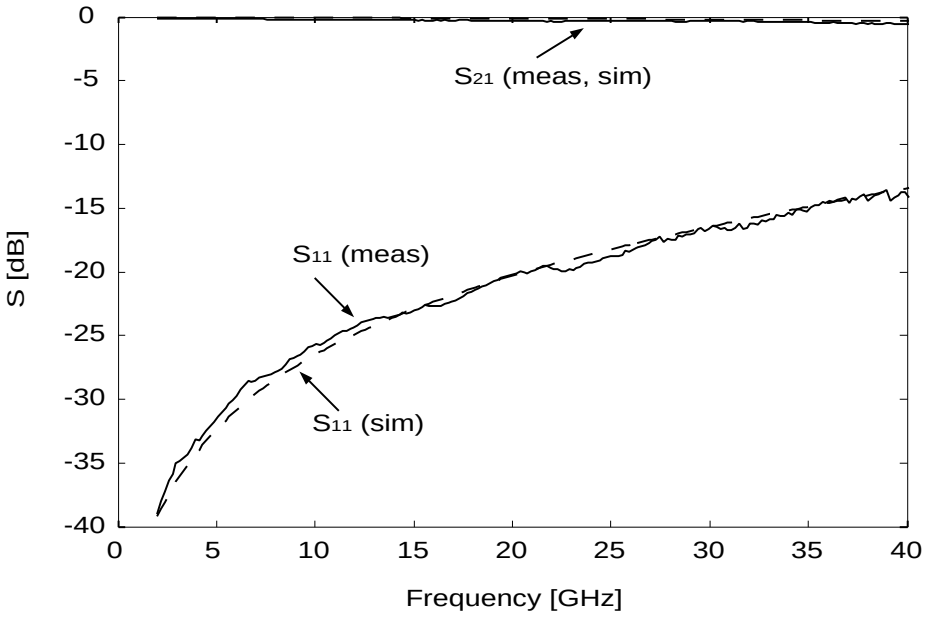
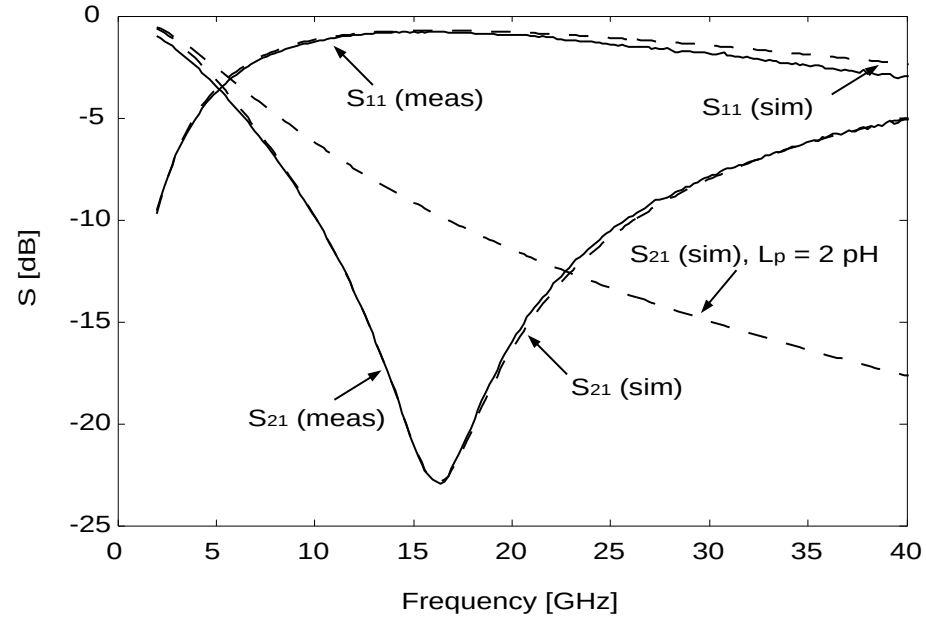
	Inductive Connecting Beam	Resonant Frequency [GHz]	Inductance [pH]	Resistance [Ω]
A		16.3	87	1.95
B		21.5	50	1.7
C		27.3	31	1.1
D		29.8	26	0.9
E		43.8 (simulated)	12	0.6
F		107.3 (simulated)	2	< 0.2

Figure 4.2: Inductive connecting beams and their resonant frequencies ($C_D = 1.1$ pF). The extracted inductances and resistances of these structures are also shown.



(a)



(b)

Figure 4.3: Measured and simulated (a) up- and (b) down-state S-parameters of the switch with the connecting beams A shown in Fig. 4.2. The extracted up-state capacitance is $C_U = 29fF$. The extracted values for the down-state circuit are: $C_D = 1100$ fF, $L_p = 87$ pH and $R_p = 1.95\ \Omega$.

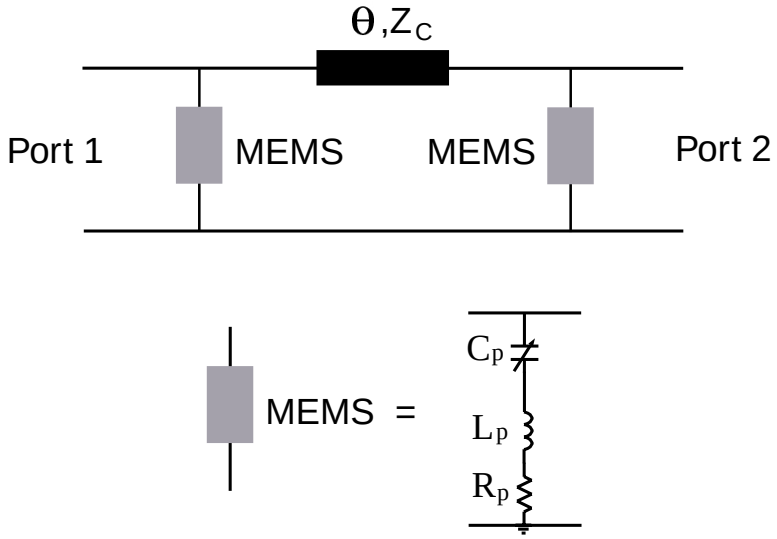


Figure 4.4: The π-match circuit.

or a π-match technique to increase the on-state isolation and minimize the off-state insertion loss. In this section we employ similar techniques for high-isolation switch packets and discuss in detail the trade-offs (bandwidth, compactness and maximum isolation) involved in the design of such circuits.

The simplest high-isolation switch packet is the π-match circuit shown in Fig. 4.4. Each shunt element represents a MEMS switch with admittance Y_{sw}

$$Y_{sw} = Z_{sw}^{-1} = \left[R_p + j\left(\omega L_p - \frac{1}{\omega C_p}\right)\right]^{-1} \equiv G_{sw} + jB_{sw} \tag{4.3}$$

where, as mentioned before, C_p, L_p and R_p are the switch capacitance, inductance and resistance respectively. The scattering parameters of the π-match network are given by [46]

$$S_{11} = S_{22} = \frac{BY_0 - CZ_0}{2A + BY_0 + CZ_0} \tag{4.4}$$

$$S_{21} = S_{12} = \frac{2}{2A + BY_0 + CZ_0} \tag{4.5}$$

where A, B, C and D represent the $ABCD$ parameter matrix of the network given

by

$$A = D = (\cos\theta - B_{sw} Z_C \sin\theta) + jG_{sw} Z_C \sin\theta \tag{4.6}$$

$$B = jZ_C \sin\theta \tag{4.7}$$

$$C = 2G_{sw} (\cos\theta - B_{sw} Z_C \sin\theta) + jZ_C \left[2B_{sw} Y_C \cos\theta + \left(Y_C^2 + G_{sw}^2 - B_{sw}^2\right) \sin\theta\right] \tag{4.8}$$

Although these equations may be lengthy to be used as a design aid, they can be greatly simplified by considering the dominant switch components in the up and down states. In the up state, for instance, the dominant component is the small up-state capacitance. Hence

$$Z_{sw} \simeq -j\frac{1}{\omega C_U} \quad \text{(up-state)} \tag{4.9}$$

On the other hand, in the down-state and at the switch resonant frequency, the complex impedance Z_{sw} is simply equal to R_p

$$Z_{sw} = R_p \quad \text{(down-state resonant frequency)} \tag{4.10}$$

Our design goals for the π-match design can be summarized as follows

- Up State: $S_{11} = 0$. This goal can be exactly true at only one frequency in the design bandwidth. We will refer to this frequency as the cancellation frequency $\omega_{r,up}$ [47]
- Down State: S_{21} =min at the switch resonant frequency $\omega_{r,dn}$

Based on these two requirements, the optimal values for the transmission line electrical length θ and characteristic impedance Z_C can be determined. The optimal value θ_{opt} can be determined from the first goal and by equation (4.4)

$$S_{11} = 0 \Leftrightarrow BY_0 = CZ_0 \tag{4.11}$$

This equation along with (4.9) leads to

$$\theta_{opt} = \tan^{-1}\left(\frac{2C_U\omega_{r,up}Z_C Z_0^2}{Z_C^2 - Z_0^2 + \left(C_U\omega_{r,up}Z_C Z_0\right)^2}\right) \tag{4.12}$$

It is interesting to note that any (practical) value of Z_C can be chosen. The most commonly chosen values are: 1) $Z_C = Z_0$ [14] which leads to the simplified equation

$$\theta_{opt} = \tan^{-1}\frac{2}{C_U Z_0 \omega_{r,up}} \tag{4.13}$$

and 2) $Z_C \gg Z_0$ which leads to minimal electrical length.

Nevertheless, these choices are not necessarily leading to the maximum possible isolation at the switch resonant frequency. The optimum value $Z_{C,opt}$ may, however, be computed from the second goal, namely $S_{21} = 0$ at the switch resonant frequency $\omega_{r,dn}$. By considering (4.5) (4.6), (4.7) and (4.10) we finally get

$$\alpha = \frac{1}{S_{21}} = \frac{\left(1 + \frac{Z_0}{R_p}\right)^2 + Z_C^2 \tan^2\theta_{opt}\left[\frac{1}{R_p} + \frac{1}{2Z_0} + \frac{Z_0}{2}\left(\frac{1}{Z_C^2} + \frac{1}{R_p^2}\right)\right]^2}{1 + \tan^2\theta_{opt}} \tag{4.14}$$

Fig. 4.5 graphically illustrates this equation for C_U = 30, 50 and 70 fF, $R_p = 2\ \Omega$, $Z_0 = 50\ \Omega$ and $f_{r,up} = 15$ GHz. We can clearly observe that the maximum isolation at the switch resonant frequency is achieved for $Z_C = Z_0$, while its sensitivity depends on the value of the up-state switch capacitance.

Equations (4.12) and (4.14) can be successfully employed to design a low-loss and high-isolation switch packet with two shunt capacitive switches. These packets, however, are fairly narrowband since the second design goal has been the maximization of the packet isolation around the switch resonant frequency. If broader bandwidth is desired, the two switches need to have different resonant frequencies. The analysis can be completed in this case in a similar way, but it is more convenient to use a CAD package. Furthermore, a CAD package greatly simplifies the design of switch

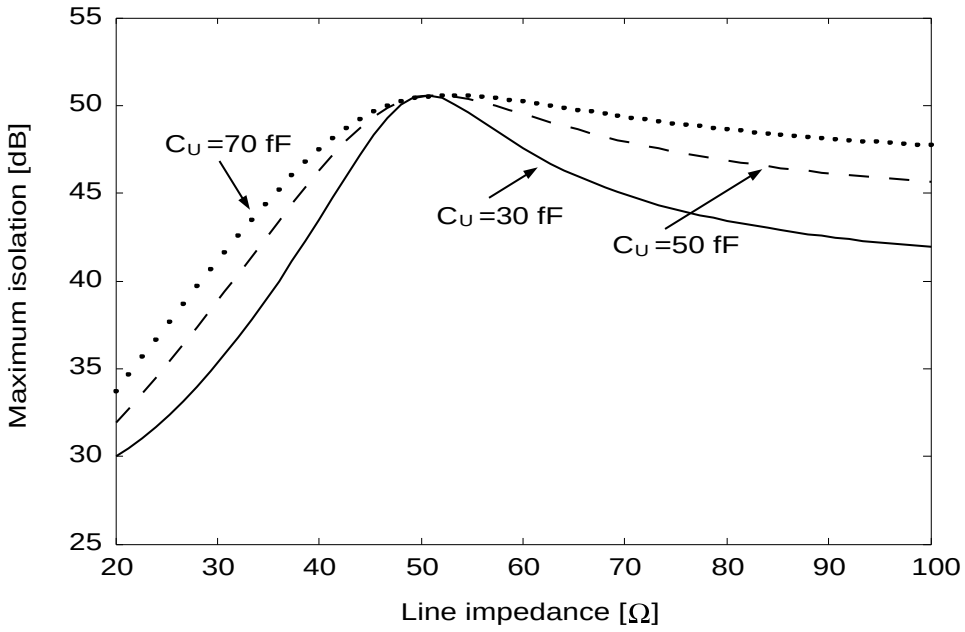


Figure 4.5: Maximum down-state isolation of the π-match circuit at the switch resonant frequency. The following values have been assumed for this graph: $C_U = 30$, 50 and 70 fF, $R_p = 2\ \Omega$, $Z_0 = 50\ \Omega$ and $f_{r,up} = 15$ GHz.

packets with more than two switches, which are particularly suited for applications that require higher isolation over broader bandwidth. The following section presents several examples of switch packets with 2, 3 and 4 shunt switches.

4.4 Switch Packets: Multiple Switches

The previous section discussed the design of simple switch packets for low up-state return loss and high down-state isolation. The main conclusion has been that, depending on the design goals, an optimal characteristic impedance $Z_{C,opt}$ exists for the transmission line section connecting the switches. If compactness is desired, Z_C has to be the highest impedance allowed by the fabrication technology. If, on the other hand, the maximum isolation is desired at the switch resonant frequency, Z_C has to be selected based on equation (4.14). These design considerations are also true for switch packets with more than two switches. Furthermore, the down-state

isolation bandwidth should be also added to the design considerations of the switch packets. Narrowband designs with maximum isolation are possible if switches with identical resonant frequencies are used, while higher bandwidths but with lower (theoretically) isolation are obtained with switches that have significantly spread resonant frequencies. Such design are discussed in detail in this section.

4.4.1 Measured Results with Printed Switches

Fig. 4.6 shows two groups of high-isolation switch packet designs. Group A shows switch packets with 2, 3 and 4 switches connected with $Z_C^A = Z_0 = 50\ \Omega$ transmission line sections. The length of these lines is $l_C^A = 1400\ \mu$m. The major goal of these designs is to achieve maximum isolation. Group B, on the other hand, includes the same designs but with $Z_C^B = 84\ \Omega$, $l_C^B = 250\ \mu$m. The high-impedance line is made of an 80/20/80 μm cpw. These designs are focused on achieving a high-isolation with the minimum possible area.

Switches with two different resonant frequencies were designed to study both broadband and narrowband designs. The networks of Fig. 4.6 were first fabricated with the switches printed in the down position so that only their RF performance would be characterized. (The following section presents the results of the same networks with the switches fabricated 4–5 μm over the cpw lines.) The measured down-state RF performances of the printed single switches are presented in Fig. 4.7. Based on the discussion of Section 4.2, the equivalent circuits of these switches can be easily extracted from these measurements (see Table 4.1).

Fig. 4.8a presents the measured results of the group A high-isolation switch packets. Only the SPS1 switch was used in all the designs in order to obtain the maximum isolation at the lowest possible frequency. Fig. 4.8b shows the measured results from the group B switch packets using the same type of switch. As expected, in both cases, the higher the number of switches used, the higher the obtained isolation is.

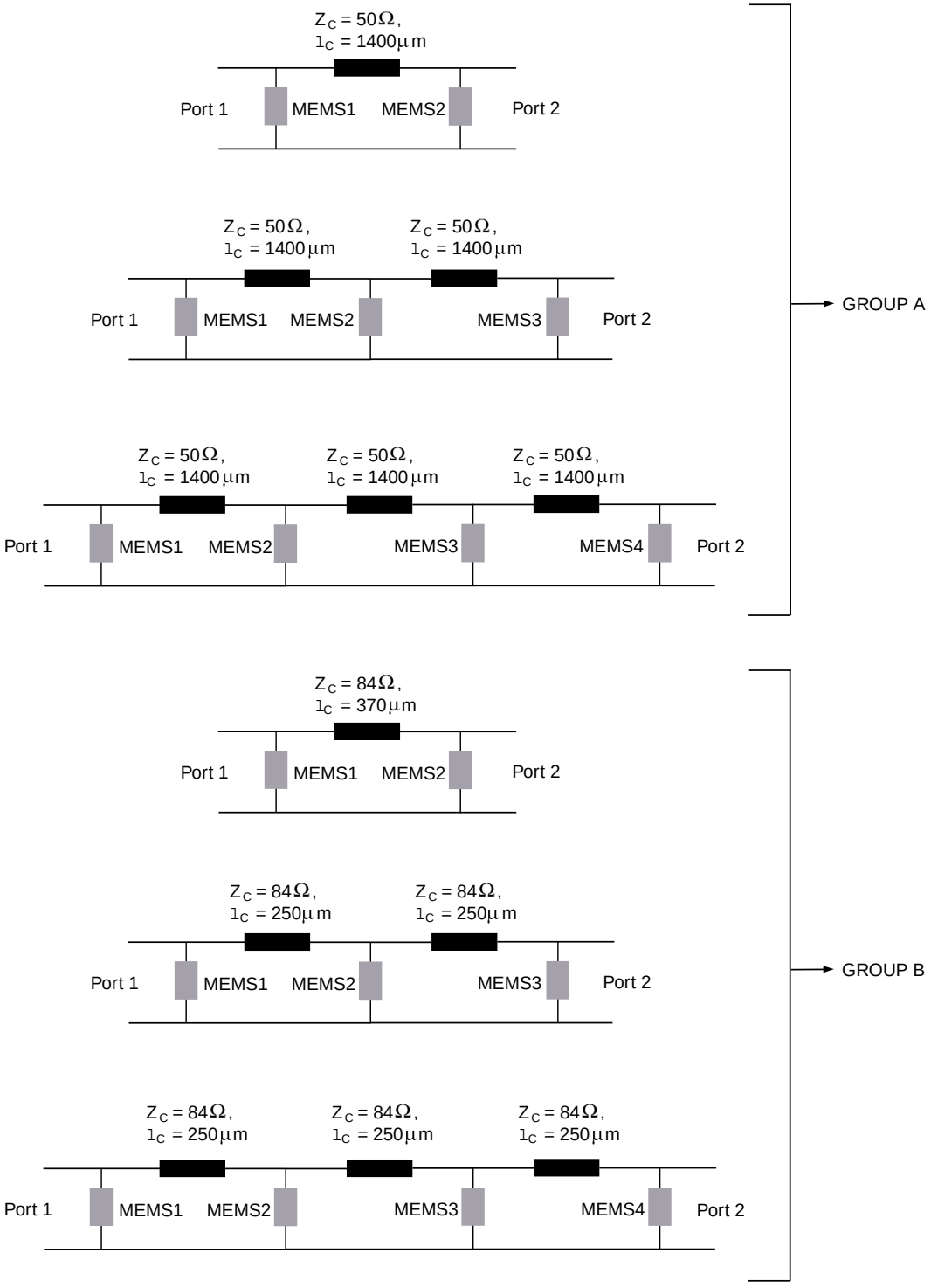


Figure 4.6: High-isolation switch packets. Group A focuses on obtaining the maximum possible isolation, while compactness is the primary goal of group B designs.

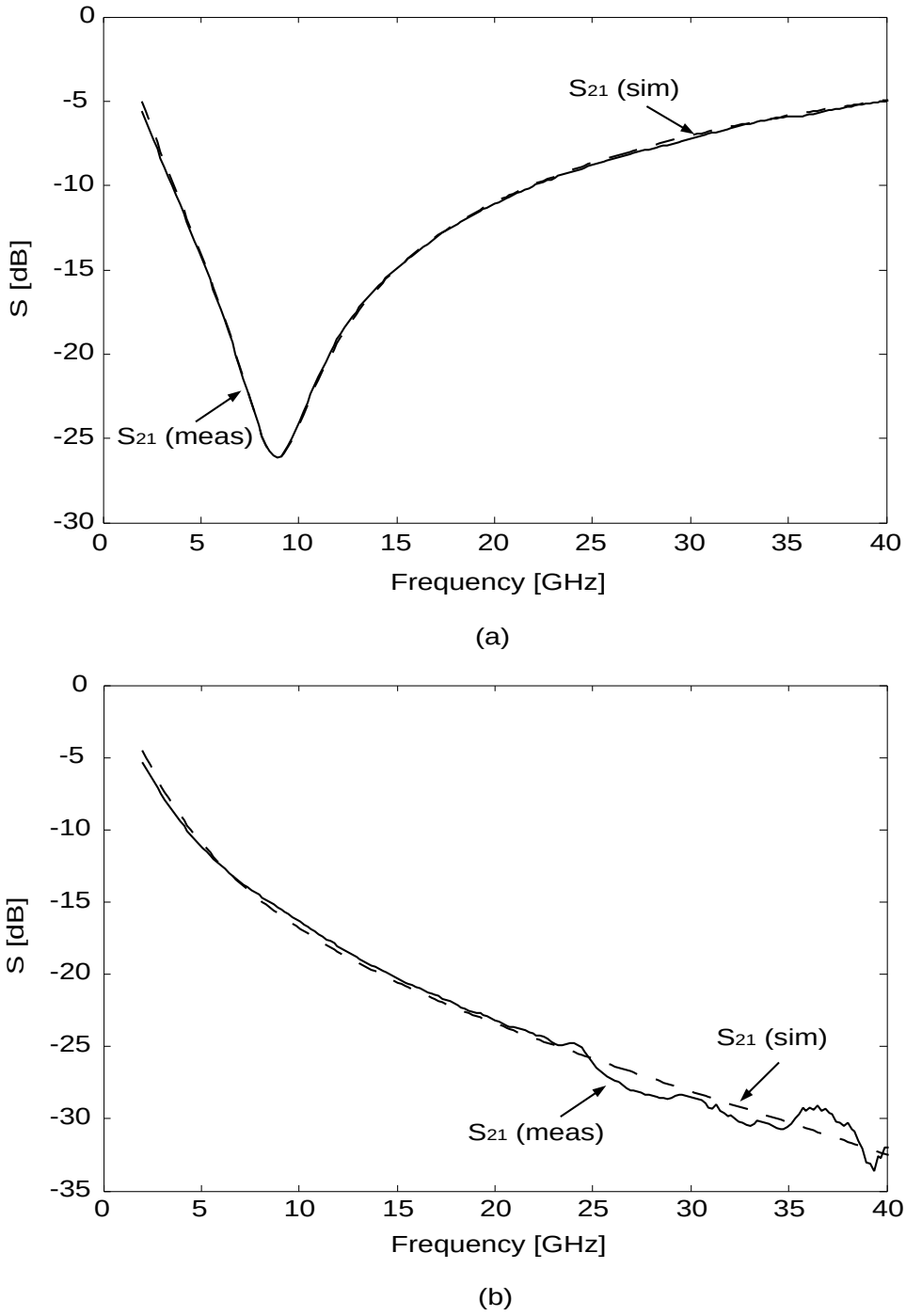


Figure 4.7: Measured down-state S-parameters of two printed switches. (a) Single Printed Switch 1 (SPS1 in Table 4.1) (b) Single Printed Switch 2 (SPS2 in Table 4.1).

Per design goals, group A results in higher isolation in the 5–10 GHz band since it incorporates the optimum line impedance $Z_C = 50\ \Omega$. This advantage, nonetheless,

Table 4.1: RF equivalent down-state capacitance, inductance and resistance for the two different switches used in the high-isolation networks. These values correspond to the switch characteristics when printed in the down position.

Switch type	C_D [pF]	L_p [pH]	R_p [Ω]
SPS1	4.2	76	1.3
SPS2	4.2	1.5	0.2

Table 4.2: Types of switches used in the broadband high-isolation networks (see Fig. 4.6)

Number of Switches	MEMS1	MEMS2	MEMS3	MEMS4
2	SPS1	SPS2	–	–
3	SPS2	SPS1	SPS2	–
4	SPS1	SPS2	SPS2	SPS1

becomes less significant as the number of switches is increased. This is due to the leaking modes in the Si substrate that limit the achieved isolation as the recorded "noise floor" shows. It is also interesting to note that, although both groups have the SPS1 switch, group B is inherently more broadband than group A.

The same networks were designed and fabricated by using both the SPS1 and SPS2 switches in an effort to obtain more broadband networks. Table 4.2 shows the exact configuration of the switches for the high isolation networks. The measured results from these circuits are given in Fig. 4.9 for both group A and group B designs. Both designs are significantly more broadband that the ones using only the SPS1 switch, but the improvement is more dramatic for the designs of group A. We can also easily observe that group A results in approximately 10 dB higher isolation between 7–20 GHz, which is consistent with the analysis of Section 4.4. Group B, however, is still more broadband than group A and maintains an isolation of higher than 40 dB even up to 40 GHz for all designs.

In summary, we have seen that extremely high-isolation switch packets are possible. The design procedure for these packets depends on the number of switches

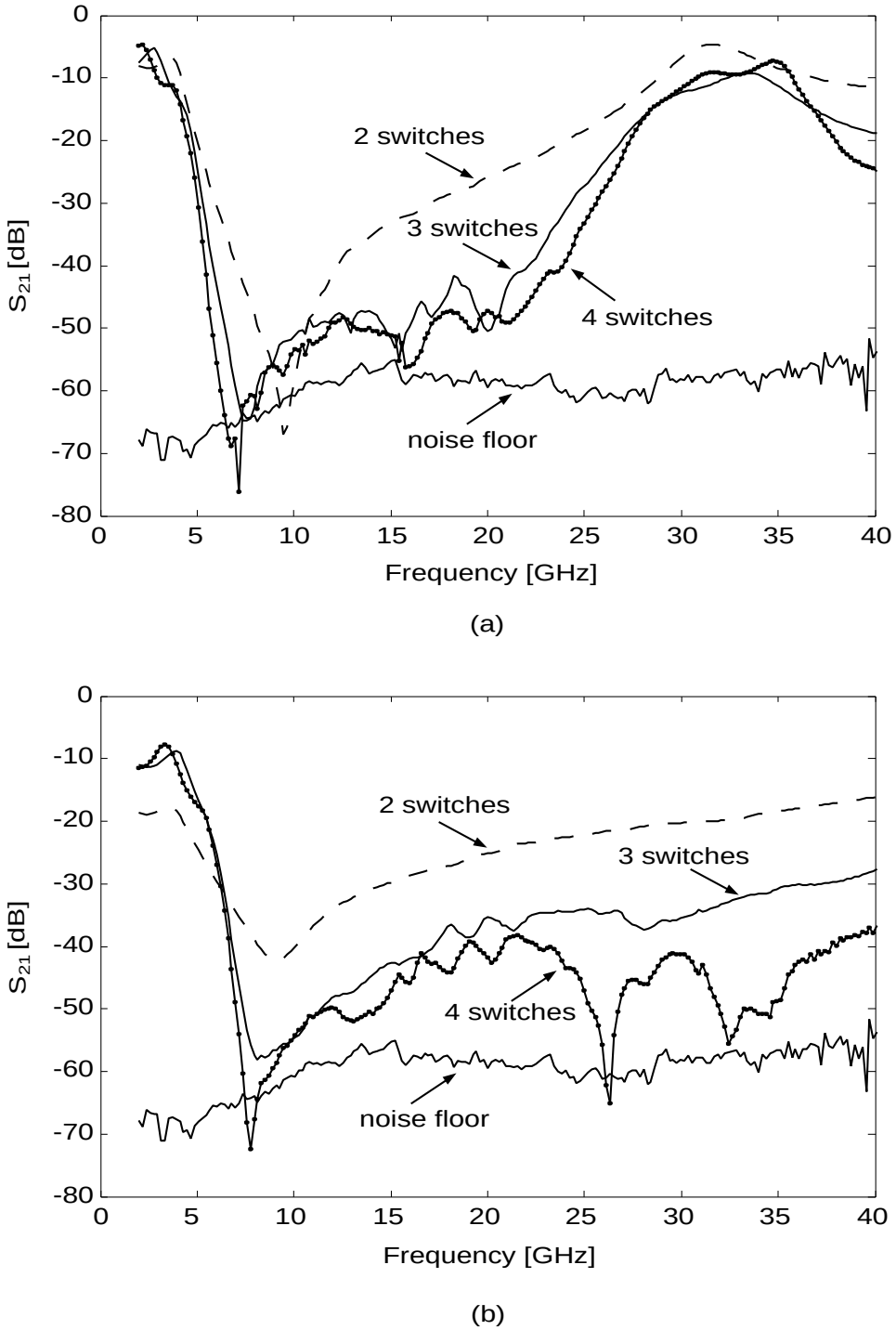


Figure 4.8: Measured down-state isolation of the (a) group A and (b) group B switch packets. All networks use only the SPS1 switch (see Table 4.1).

in the packet and the isolation/bandwidth requirements. If the maximum possible isolation is desired, switch packets with only one switch type and with the optimum

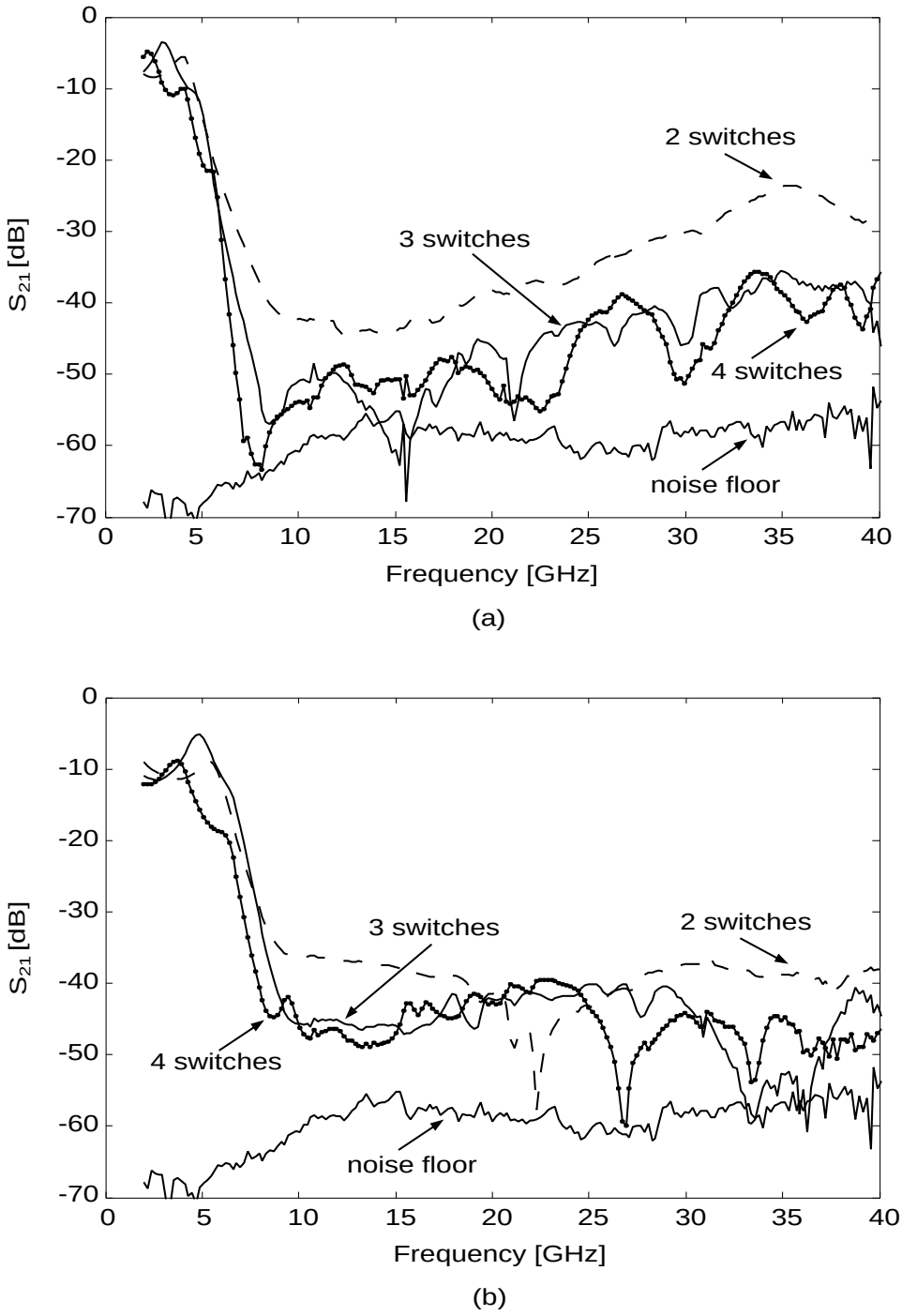


Figure 4.9: Measured down-state isolation of the (a) group A and (b) group B switch packets. All networks use both switch types according to the configuration shown in Table 4.2.

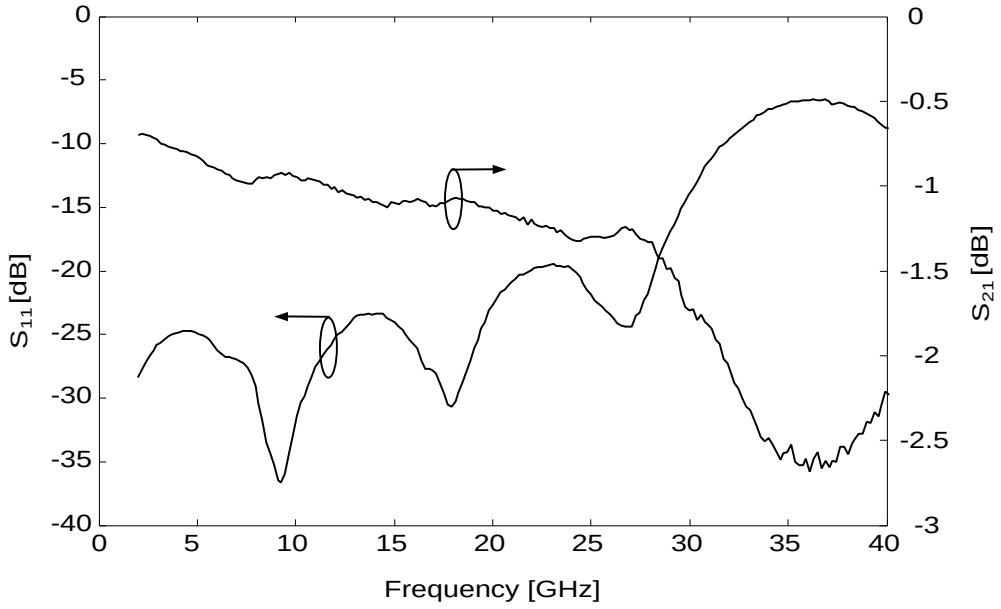
transmission line impedance should be implemented. The measurable isolation of networks with more than 2 switches, however, is typically limited by the surface wave

modes in the Si substrate. Hence, the isolation requirements of the network can be relaxed. The benefits in this case are 1) minimization of circuit real-estate by using high impedance transmission line sections and 2) increased bandwidth by using switches with different resonant frequencies.

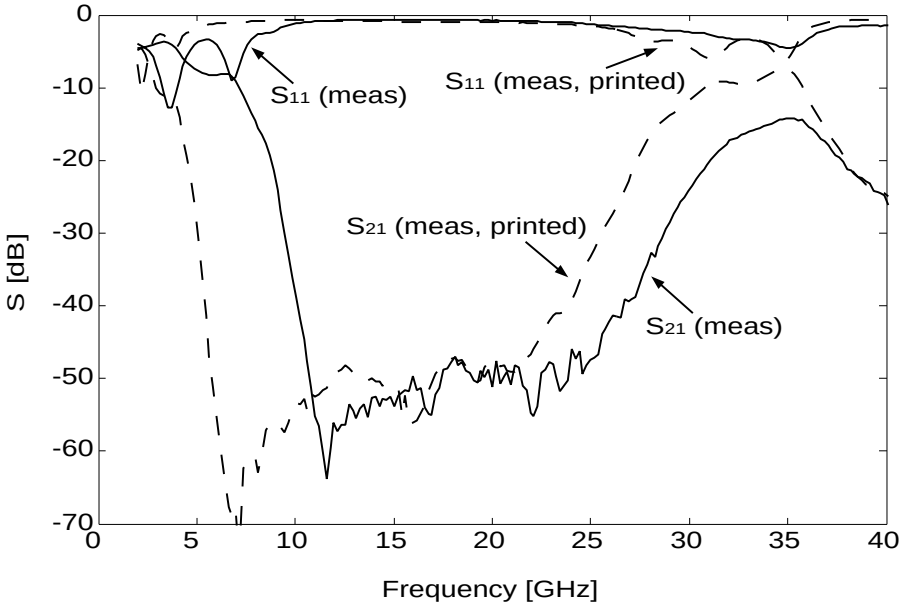
4.4.2 Measured Results with Suspended Switches

In an effort to verify the results with the printed switches and characterize the behavior of the high-isolation networks with suspended switches, we fabricated and measured the most complex 4-switch networks of group A. Fig. 4.10 shows the up and down-state S-parameter of this network. The up-state insertion loss is 0.94 dB at 10 GHz and 1.31 dB at 25 GHz. Based on TRL calibration [48, 49], the loss of the simple thru lines is 1.55 dB/cm at 10 GHz and 1.89 dB/cm at 25 GHz. Consequently, the loss of a thru line with the same length (5250 μm) as the high-isolation network would be 0.81 dB and 1 dB at 10 and 25 GHz respectively. This shows that the total up-state loss of the four switches is only 0.13 dB and 0.31 dB at 10 and 25 GHz respectively. The return loss of the switch packet is less than -13.5 dB up to 30 GHz.

The down-state performance of the network shows an isolation greater than 40 dB from 10 to 26.5 GHz. The measured isolation follows closely the one obtained from the same network with the switches fabricated in the down position (Fig. 4.10b). The only difference is that the achieved down state capacitance is approximately 1.2 pF. This is due to the residual stress in the fabricated switches and the roughness of the contacting surfaces that did not allow the switches to conform perfectly on the dielectric layer underneath them.



(a)



(b)

Figure 4.10: Measured (a) up- and (b) down-state S-parameters of the group A 4-switch high-isolation network. The down-state isolation compares well with the measured isolation of the same network with the switches fabricated in the down position, except that the achieved down state capacitance is about 1.2 pF.

4.5 Conclusions

This chapter has presented several design techniques for achieving high isolation from capacitive MEMS switches. We have demonstrated inductively tuned single switches that present 25–30 dB per switch around their resonant frequency. These switches may also be successfully combined in high-isolation switch packets. A variety of switch packets that address different design goals have been presented. Switch packets with up to four switches show an insertion loss of only 0.03 dB and 0.08 dB at 10 and 25 GHz respectively per switch. They also provide very high isolation that is only limited by the surface wave substrate modes. Theoretical and experimental results of these packets have shown that a compromise between the highest possible isolation, bandwidth and circuit size is typically required for practical circuits.

CHAPTER 5

Tunable Lumped Components with Applications to Reconfigurable MEMS Filters

5.1 Introduction

CHAPTERS 2, 3 and 4 have concentrated on switches and switching circuits, which are undeniably the most significant components of RF MEMS. In particular, we have demonstrated the design of a low-voltage MEMS switch and we have discussed several aspects of its operation, including bias voltage, insertion loss, power handling and dynamic behavior. In chapter 4 we presented improved inductively-tuned switches that presented their maximum isolation at a frequency bandwidth controlled by the switch geometry. Switch packets were also demonstrated with a maximum measured isolation of 50 dB from 10–25 GHz.

The common factor in Chapters 2, 3 and 4 has been that the switching function is the primary goal of any RF MEMS component or collection of components. However, RF MEMS switches are more general devices than relays, since they have the capability to locally change the RF impedance of a transmission line. Several examples that demonstrate the applicability of this property are introduced in this chapter. In particular, we discuss a unique technique of employing MEMS switches

for digitally tuning cpw-based lumped elements and the potential of this technique in reconfigurable compact filter design. Three lumped tunable components for microwave frequencies are first introduced (shunt capacitor, series inductor and shunt inductor) and then used in lowpass and bandpass tunable filters.

5.2 Tunable Shunt Capacitor

The easiest way to implement a digitally tuned capacitor is to use a capacitive MEMS switch. For example, a metallic plate suspended over a cpw line that can be electrostatically actuated and short the line is a well-known technique. The switch in the up state presents a very small capacitance (typically in the order of 20 to 50 fF), while the down state capacitance is in the range of 1 to 4 pF. Therefore, a tuning range of 40 to 80 can be achieved. While this simplistic model of a capacitive MEMS switch may be adequate for switching-network design, it is not sufficient for filter design due to the parasitic components that cannot be neglected in the latter case.

Although the low-voltage switch already discussed in the previous chapters is used in this chapter as a vehicle to demonstrate the previous concepts, the following techniques can be readily applied to most of the capacitive switches with similar properties. Fig. 5.1a illustrates the layout of this switch in a configuration that will be later used for the filter implementation. Fig. 5.1b shows a lumped-element equivalent T-network that can be used to accurately simulate the RF performance of this switch.

The capacitance C_p is given by the series connection of the capacitance C_{ct} and C_{gnd}, where C_{ct} (C_{gnd}) is the capacitance formed between the center conductor (ground plane) of the cpw and the plate on top of it. Following [14], the up and

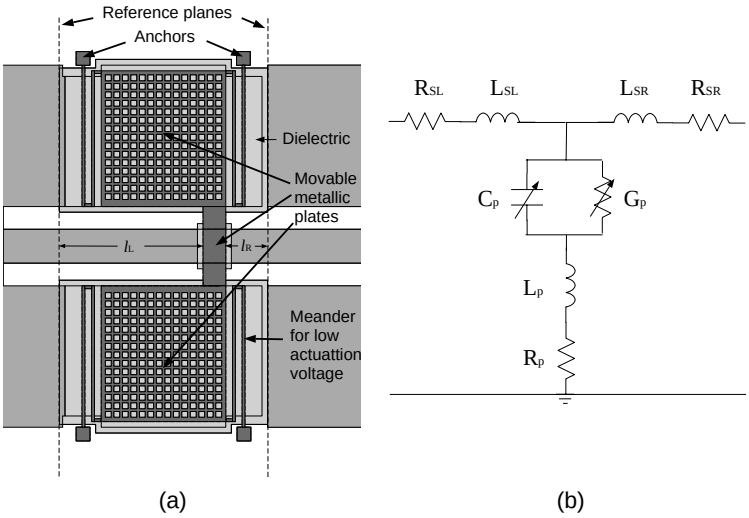


Figure 5.1: (a) Capacitive MEMS switch used as tunable capacitor over a cpw line, and (b) its equivalent circuit.

down-state capacitances can be expressed as

$$C_p = \begin{cases} \varepsilon_0 \frac{A}{d+t_d/\varepsilon_r} + C_{frng} & : \text{ up-state} \\ \varepsilon_0 \varepsilon_r \frac{A}{t_d+d_{gap}} & : \text{ down-state} \end{cases} \tag{5.1}$$

where A is the plate area on top of the center conductor, d is the distance between the switch and the cpw in the up-state ($d \simeq 4-5$ μm for the switches in this work), t_d is the thickness of the dielectric material on top of the cpw line ($t_d = 1200\mathring{A}$), ε_r is the dielectric constant of the material used ($\varepsilon_r \simeq 7.5$ for PECVD Si_3N_4) and C_{frng} is the additional capacitance due to the fringing field effect. Finally, d_{gap} is an effective thickness that models the inability of the switch to achieve a perfect contact with the dielectric layer underneath it. For the geometry shown in Fig. 5.1a, the extracted up and down capacitances from the measured S-parameters are $C_p^{up} = 17$ fF and $C_p^{down} = 920$ fF.

R_p and L_p represent the resistance and inductance of the switch beam and can be modeled with a full wave simulator. Typical values range from 0.1–2 Ω and 1–80 pH for the R_p and L_p respectively. They are primarily dominated by the beams

connecting the switch plates (see Chapter 4). G_p depends on the quality of the dielectric material and can be readily modeled using the formula:

$$G_p = \begin{cases} 0 & : \text{ up-state} \\ \omega C_p \tan\delta & : \text{ down-state} \end{cases} \tag{5.2}$$

where $\tan\delta$ is the loss factor of the dielectric material used as the insulator. The inductive sections L_{SL} and L_{SR} are used to model the short transmission line sections of lengths l_L and l_R respectively (see Fig. 5.1). These inductances are important since their values can be comparable to those of the inductors used in a filter. L_{SL} can be approximated as :

$$L_{SL} \simeq \frac{2Z_0}{\omega} \tan(\beta l_L/2) \simeq Z_0 \beta l_L/\omega \tag{5.3}$$

A similar formula holds for L_{SR}. Alternatively short transmission line sections can be employed to model the finite (but small) switch electrical length. The resistances R_{SL} and R_{SR} represent the ohmic loss of the same transmission line sections and can be modeled as:

$$R_{SL} \simeq 2\alpha Z_0 l_L \quad \text{and} \quad R_{SR} \simeq 2\alpha Z_0 l_R \tag{5.4}$$

where α is the measured attenuation of the transmission line (approximately 1.2 dB/cm for the circuits measured in this work).

5.3 Tunable Series Inductor

It is a well-known fact that a relatively high-Q inductor can be implemented with a short section of a transmission line assuming that the length is less than approximately a tenth of a wavelength [50] (Fig. 5.2). The component values of

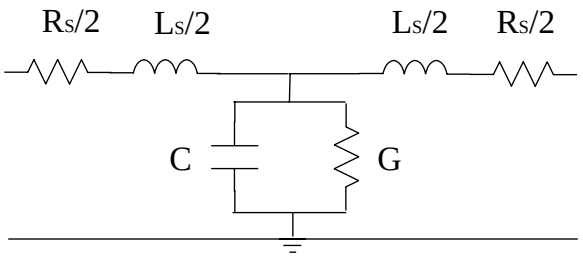


Figure 5.2: Equivalent circuit of a short transmission line

this equivalent circuit can be calculated by formulas similar to the ones given in (5.2),(5.3),(5.4). The quality factor of this inductor can be estimated if the small shunt capacitance and conductance are neglected, as follows :

$$Q_{S,ind} = \frac{\omega L_S}{R_S} = \frac{\tan(\beta l/2)}{\alpha l} \simeq \frac{\beta}{2\alpha} \tag{5.5}$$

This equation results in a quality factor of 19 at 10 GHz with a measured attenuation of 1.2 dB/cm, which is typical for the high resistivity Si wafers (2000 $\Omega\times$cm before the wafer oxidization) used in this work. Higher Q values can be readily achieved by using higher resistivity Si wafers (e.g. 10000 $\Omega\times$cm), high-quality quartz wafer (with a loss tangent of 0.0004) or by employing well-known buck micromachining techniques [51, 52, 53]. Independently of the available technology, the short transmission line section results in a (conventional) inductor with the highest possible quality factor.

The reconfigurability of this element can be achieved in association with the tunable capacitor. The primary goal is to load a short transmission line section with RF MEMS switches and then actuate the appropriate switches in order to get the desired equivalent series inductance between the actuated switches. An example that explains this idea is illustrated in Fig. 5.3, which shows a short transmission line with four capacitive MEMS switches numbered from one to four. Assuming that 1) the up-state capacitance is negligible, and 2) all four switches are identical, the series inductor can be tuned by actuating different sets of switches. For

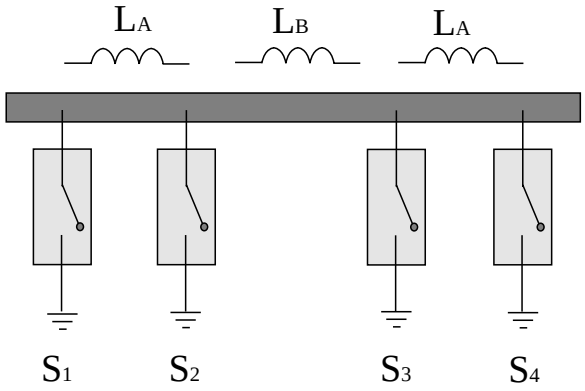


Figure 5.3: Tunable series inductor with four switches.

instance, if S_1 and S_4 are down, then the inductance value between these switches is $L_{ind}^{1,4} = L_B + 2L_A + 3(L_{SL} + L_{SR})$. On the other hand, when S_2 and S_3 are down, this value becomes $L_{ind}^{2,3} = L_B + L_{SL} + L_{SR}$ resulting in a tuning ratio of:

$$\mathcal{R}_{ind} \equiv \frac{L_B + 2L_A + 3\,(L_{SL} + L_{SR})}{L_B + L_{SL} + L_{SR}} = 1 + 2\frac{L_A + L_{SL} + L_{SR}}{L_B + L_{SL} + L_{SR}} \tag{5.6}$$

The major advantage of this technique is that the inductor tuning ratio can be quite high and is totally controlled by the placement of the switches on the transmission line. Moreover, although two switching pairs have been used in this example, more switching pairs can be easily integrated with the transmission line section and the inductor can take more discrete values. The minimum and maximum inductance values are given by.

$$L_{min} = L_{SL} + L_{SR} \quad \text{and} \quad L_{max} = L_B + 2L_A + 3(L_{SL} + L_{SR}). \tag{5.7}$$

5.4 Tunable Shunt Inductor

An inductive cpw stub is usually employed to implement a shunt resonator. Although stubs as long as $\lambda/4$ have been used [54], only short stubs are discussed in

this work. Such short inductive stubs exhibit similar properties (in phase shifting and quality factor) to the series inductors presented in the previous subsection. Therefore, their equivalent circuits are not substantially different from the ones already presented and will not be repeated.

A metallic plate suspended on top of the inductor and the ground plane as shown in Fig. 5.4a can be utilized for tuning this component. The plate covers completely the inductive stub and a part of the ground plane. Furthermore, the holes have been removed from the plate just above the stub in order to achieve a higher capacitance (for clarity in the figure, the metallic plate is transparent). In the up-state, the plate should not substantially affect the value of the inductance. In the down-state, however, the stub is effectively shorted by the capacitively formed RF short and the inductance value changes to an effective inductance L_{eff}.

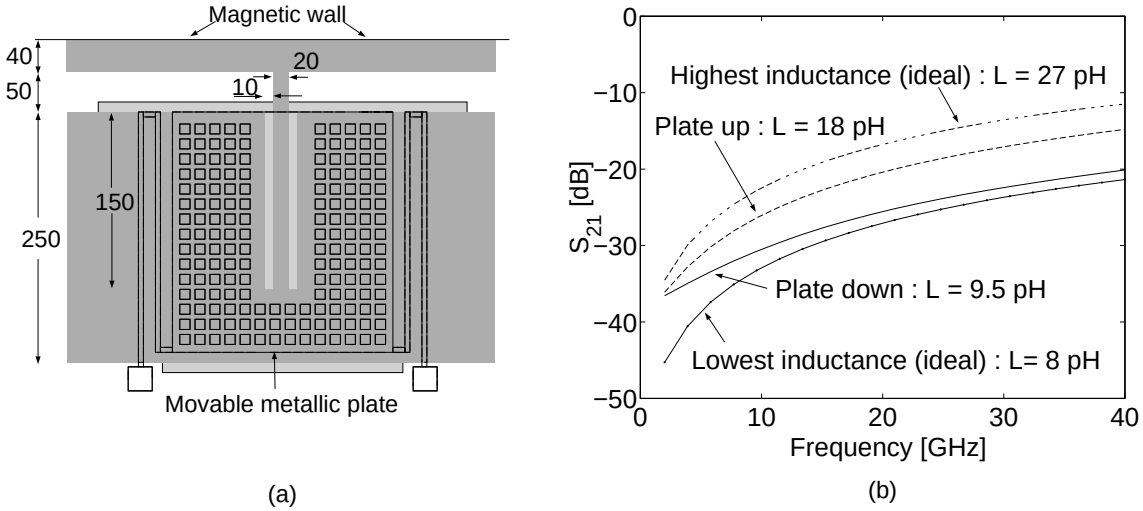


Figure 5.4: (a) Tunable shunt inductor (dimensions are in μm). (b) Simulated response.

IE3D [55] was used to model the inductance in the up and down position and demonstrate this concept. The simulated results are presented in Fig. 5.4b, which clearly indicate that a tuning range of approximately 2:1 can be realized through this technique. Two ideal inductance values are also mentioned in Fig. 5.4, which correspond to the inductances that could be realized if it were possible to perfectly short

the stub in the down state and leave it unaffected in the up state. Obviously, an even higher tuning range could be achieved if these minimum and maximum inductance values could be obtained. A metal-to-metal contact switch could, therefore, provide results closer to the ideal situation. Additionally, the tuning range can be further optimized by changing the geometrical features of the stub.

5.5 Tunable Lowpass Filter

The tunable components analyzed in the previous section can be combined to form potentially useful tunable circuits. To demonstrate this concept, two tunable filters were implemented using these ideas. A 3:1 (digital tuning) lowpass filter is presented in this section where the basic concepts are explained. A more innovative and complex 2:1 bandpass filter design that employs all of the three tunable components in this chapter is discussed in the next section.

5.5.1 Design Approach

Fig. 5.5 shows the well-known LC ladder topology of a prototype lowpass filter. The tunable lumped elements presented in this chapter are adequate for reconfiguring this topology. The basic idea is to implement the shunt capacitors by shunt capacitive MEMS switches and the series inductors of the filters with high-impedance section transmission lines. The filter topology can then be readily altered by appropriately selecting the group of MEMS switches to be actuated.

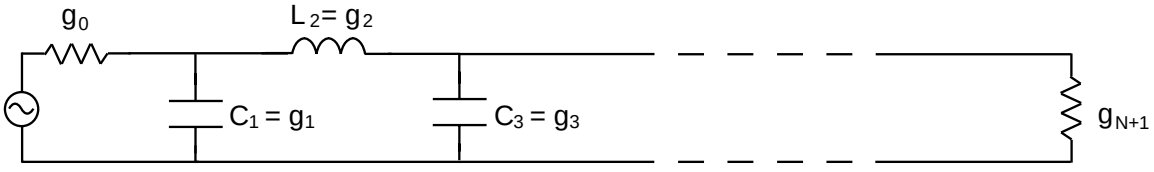


Figure 5.5: Low-pass filter topology.

Fig. 5.6 illustrates an example of this technique. The initial filter topology represents a third order lowpass filter when switches 1 and 5 are activated, while it is transformed to a fifth order filter if switches 2, 3 and 4 become active. The desired bandwidth of the two filters can be achieved by appropriately selecting the capacitance values of the MEMS switches and the length of the transmission lines (equivalent inductors) connecting them. It is interesting to note that this technique allows the tuning of every single element of the filter. This is necessary for a true reconfiguration of the filter.

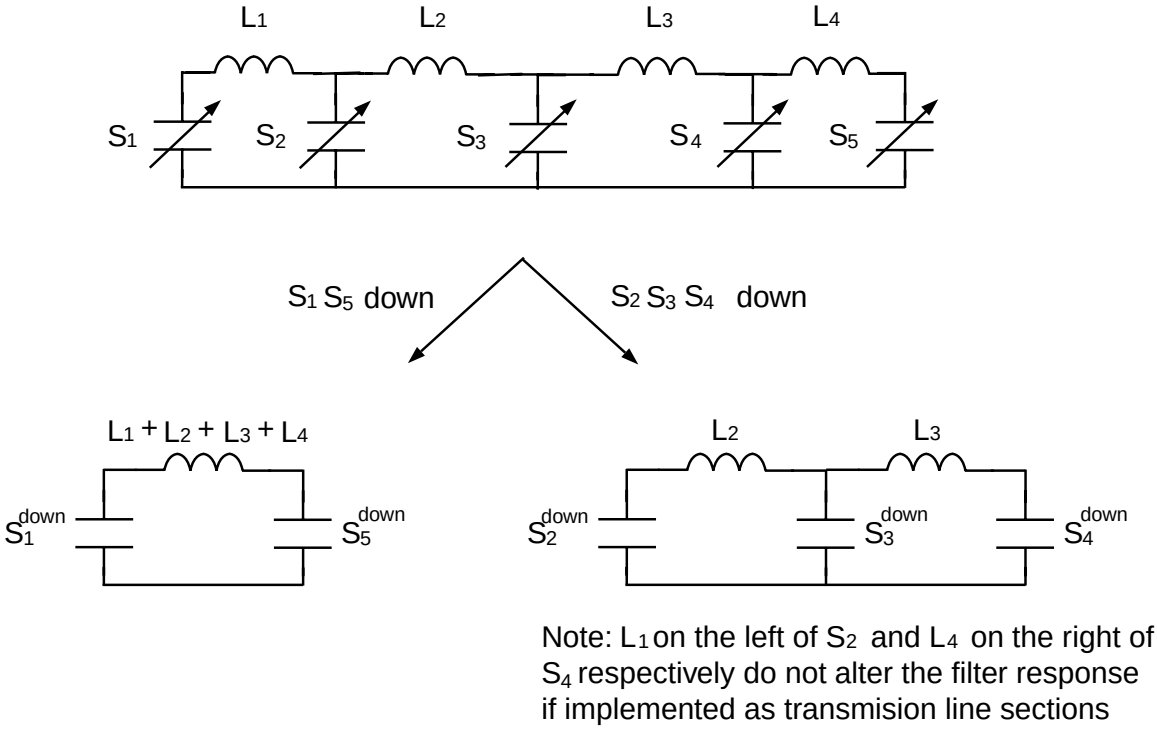


Figure 5.6: Basic concept for the low-pass filter reconfiguration.

5.5.2 Implementation and Results

These techniques were applied to implement a 3:1 Chebyshev tunable lowpass filter. The basic design starts by considering separately the two desired filters. For this implementation two 0.2 dB Chebyshev filters are considered with 10 (third order

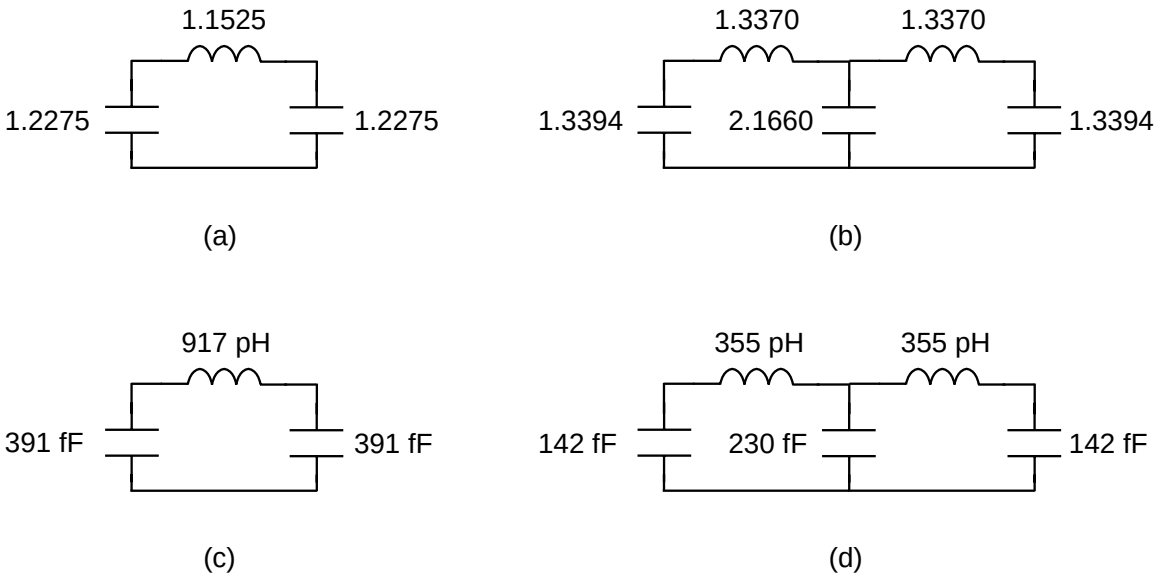
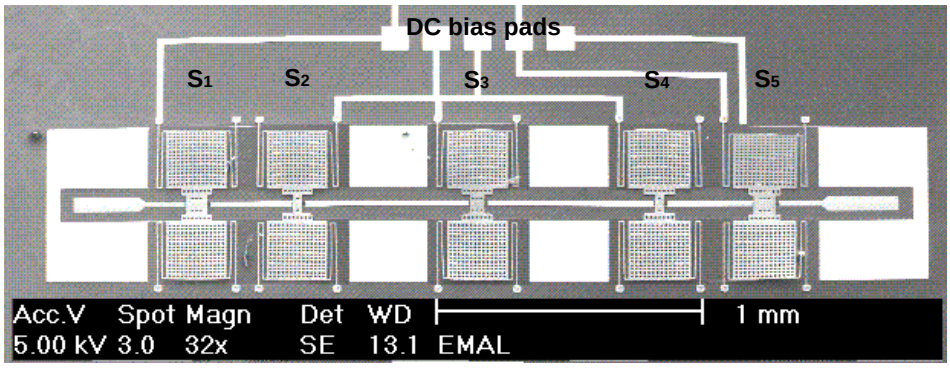


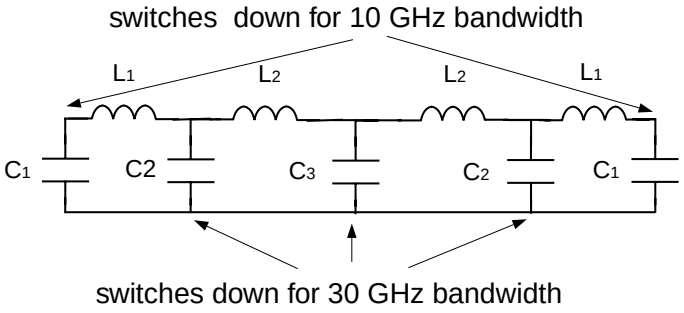
Figure 5.7: (a) Lowpass prototype for 0.2 dB third order Chebyshev filter. (b) Lowpass prototype for 0.2 dB fifth order Chebyshev filter. (c) Lumped-element implementation of (a) with 10 GHz bandwidth in a 50 Ω system. (d) Lumped-element implementation of (b) with 30 GHz bandwidth in a 50 Ω system.

filter) and 30 GHz (fifth order filter) bandwidth respectively. Fig. 5.7 shows the two lowpass prototypes as well as the lumped-element value components for the desired bandwidths assuming a 50 Ω system. These two filters are combined according to the idea illustrated in Fig. 5.6. Each capacitor is then implemented by a shunt MEMS switch and each inductor with a high-impedance transmission line. Fig. 5.8 shows the final fabricated filter, a simple extracted equivalent circuit for the two stages and the final measured and simulated results.

In general the measured results can be well explained by the extracted equivalent circuits. The low frequency filter in particular matches very well with the model. This filter's insertion loss is approximately 1.1 dB at the 10 GHz passband bandwidth with a return loss of less than –15 dB. However, there is an increase of 0.8 dB in the insertion loss at the 30 GHz band. This is partly due to the increased return loss at the level of −8 dB around 20 GHz. This discrepancy can be attributed to the somewhat lower



(a)



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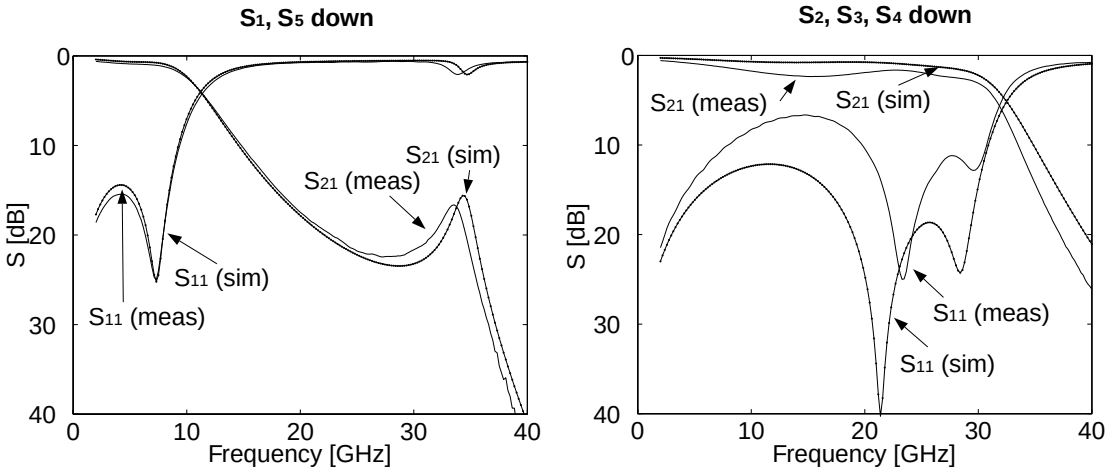


(c)

Figure 5.8: (a) Low-pass filter. (b) Simplified equivalent circuit. (c) Simulated and measured response.

capacitances that were obtained when the switches 2, 3 and 4 were down. One more iteration would tune these capacitor values and result in an optimized design.

5.6 Tunable Bandpass Filter

5.6.1 Design Approach

While a conventional Chebyshev bandpass implementation with an LC ladder is possible, the presence of the small inductors L_{SL} and L_{SR} (see Section 5.2) makes the accurate implementation of the shunt LC resonator difficult (Fig. 5.9). This is particularly true when more than one switches are placed in parallel with the shunt inductor for a multi-band operation. L_{SL} and L_{SR} in such a case can easily become comparable to the inductor of the shunt resonator, leading to a significantly distorted filter response. Consequently, the traditional LC ladder scheme is sub-optimal for the implementation of lumped-element tunable bandpass filters.

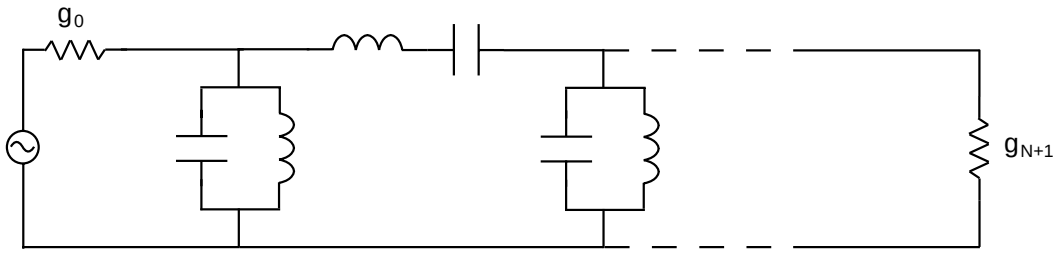


Figure 5.9: Traditional LC-ladder bandpass filter implementation. The switch (shunt capacitor) electrical length significantly complicates the realization of shunt resonators of this filter.

Instead a new network (to the best of the author's knowledge) particularly suited for MEMS switch reconfigurability has been investigated in this work. The major advantages of this network are a) it results in very compact implementations, b) it requires only one mechanically moving device (the shunt capacitive switch) for its reconfiguration, and c) it preserves the absolute bandwidth of the filter as the center frequency is tuned, since every one of its components is tuned.

Fig. 5.10 presents the conceptual steps followed to design this network. The first basic idea relies on the fact that the circuits of Fig. 5.10a and Fig. 5.10b are equivalent

for short transmission line lengths. In other words, for $\beta l < \pi/6$ they result in (almost) the same reflection coefficient. Consequently, by placing different shunt capacitors in various distances from the short circuit of Fig. 5.10b we can obtain different shunt LC resonators. This technique can be used for frequencies that satisfy $\beta l < \pi/6$. Based on these one-port networks, a two-port network can be synthesized as shown in Fig. 5.10c. The shunt inductor L_p is necessary for the desired bandpass response.

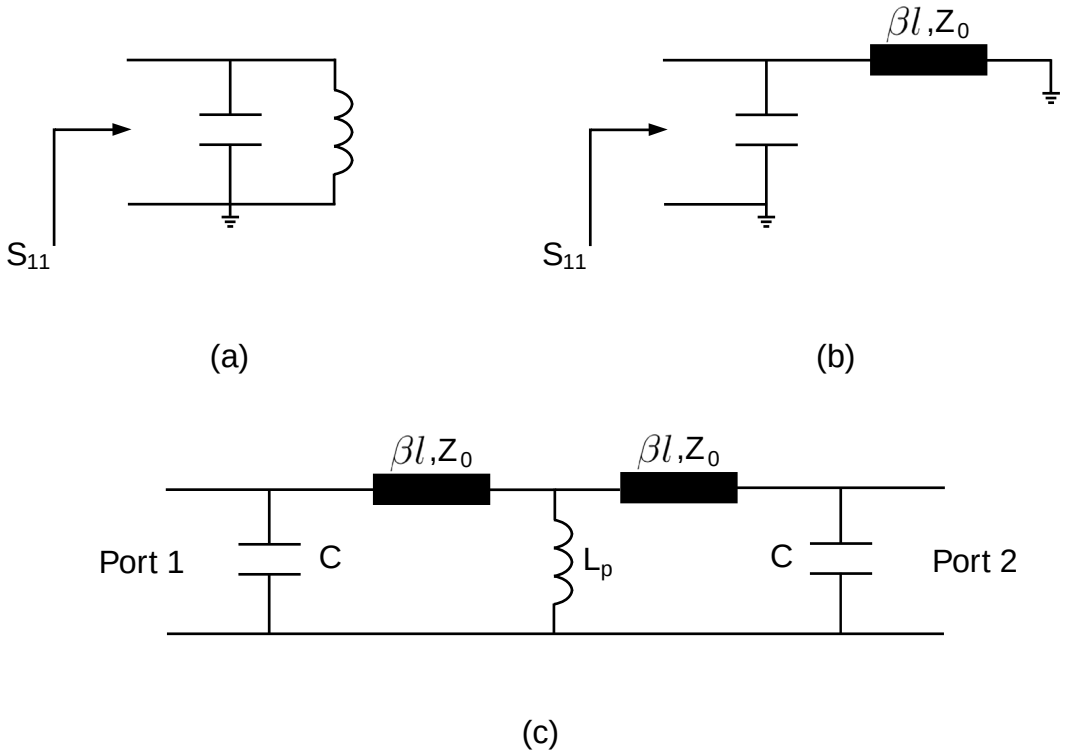


Figure 5.10: Design approach for the synthesis of the bandpass filter topology. The two one-port networks shown as circuits (a) and (b) are (almost) equivalent if $\beta l < \pi/6$. Network (c) is the finally proposed two-port filter.

The frequency response analysis of this filter can be readily obtained by following the well-known even-odd analysis method. Figs. 5.11 and 5.12 graphically illustrate the detailed steps of the analysis.

Even-Odd Mode Analysis

Even-mode. The even-mode excitation is shown in Fig. 5.11b. Because of the symme-

try emphasized in Fig. 5.11d, the circuit is finally transformed to the topology shown in Fig. 5.11e. From this topology we have:

$$V_A^e = \frac{V_g}{2}\frac{C \parallel (L_s + 2L_p)}{Z_0 + C \parallel (L_s + 2L_p)} = \frac{V_g}{2}\frac{s\frac{\omega_{0e}}{Q_e}}{s^2 + s\frac{\omega_{0e}}{Q_e} + \omega_{0e}^2} \tag{5.8}$$

where

$$\omega_{0e} = \frac{1}{\sqrt{C(L_s + 2L_p)}} \quad \text{and} \quad Q_e = \frac{1}{Z_0 C \omega_{0e}} = Z_0\sqrt{\frac{C}{L_s + 2L_p}} \tag{5.9}$$

The voltages V_B and V_C are then readily given by

$$V_B^e = V_A^e\frac{2L_p}{L_s + 2L_p} \quad \text{and} \quad V_C^e = V_A^e \quad \text{(because of symmetry)} \tag{5.10}$$

Odd-mode. The odd-mode excitation is shown in Fig. 5.12. Due to anti-symmetry we have

$$V_A^o = -V_C^o \quad \text{and} \quad V_B^o = 0 \tag{5.11}$$

Additionally, similarly to the even-mode analysis we readily get

$$V_A^o = \frac{V_g}{2}\frac{s\frac{\omega_{0o}}{Q_o}}{s^2 + s\frac{\omega_{0o}}{Q_o} + \omega_{0o}^2} \tag{5.12}$$

where

$$\omega_{0o} = \frac{1}{\sqrt{CL_s}} \quad \text{and} \quad Q_o = \frac{1}{Z_0 C \omega_{0o}} = Z_0\sqrt{\frac{C}{L_s}} \tag{5.13}$$

By applying superposition the total voltages on the filter are given by

$$V_A = V_A^e + V_A^o = \frac{V_g}{2}\left[\frac{s\frac{\omega_{0e}}{Q_e}}{s^2 + s\frac{\omega_{0e}}{Q_e} + \omega_{0e}^2} + \frac{s\frac{\omega_{0o}}{Q_o}}{s^2 + s\frac{\omega_{0o}}{Q_o} + \omega_{0o}^2}\right] \tag{5.14}$$

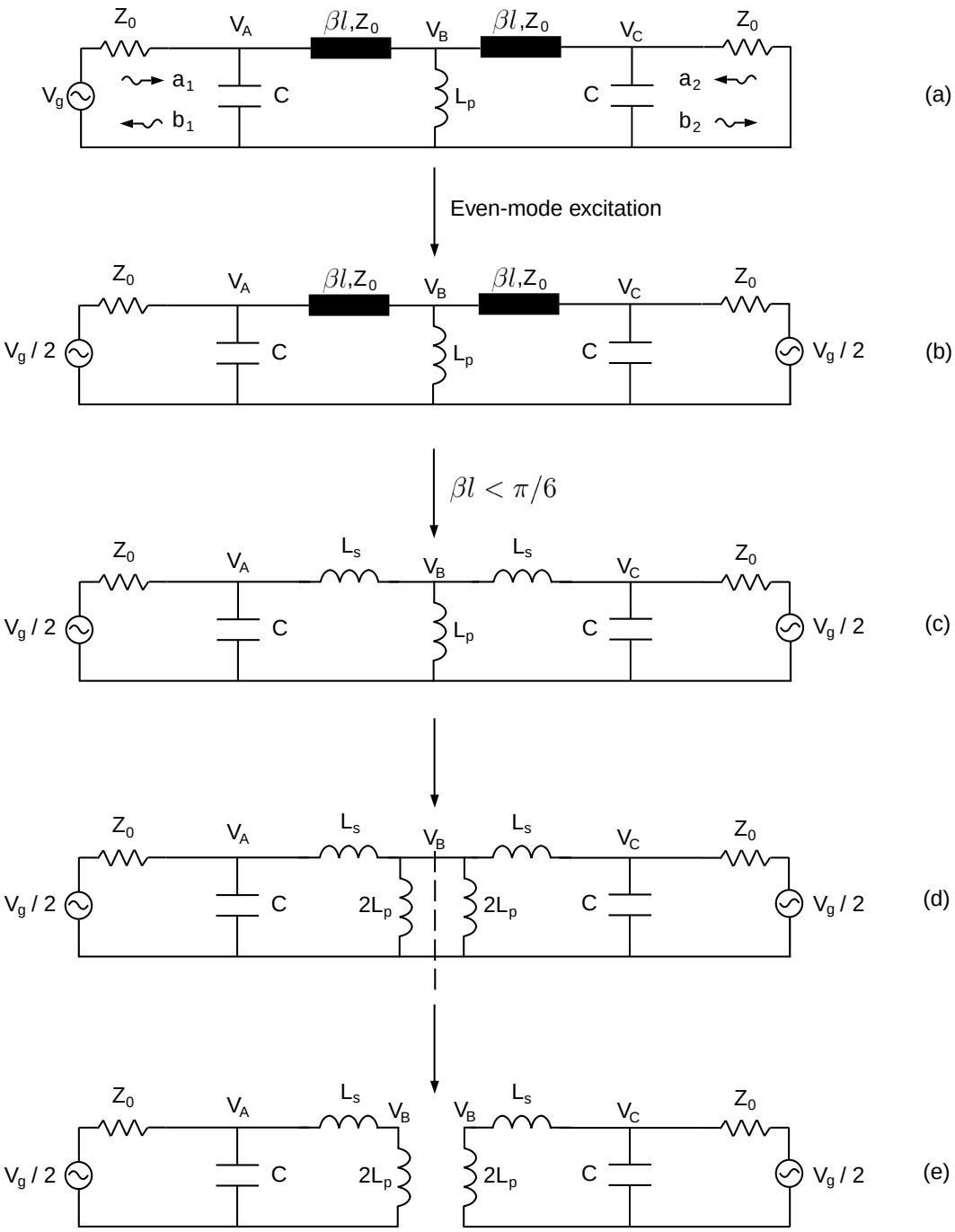


Figure 5.11: (a) Band-pass filter topology with source and load connections. (b) Even-mode excitation (c) Short transmission line sections are replaced by their equivalent inductors (d) Network redrawn to emphasize symmetry. (e) Final topology because of the circuit symmetry.

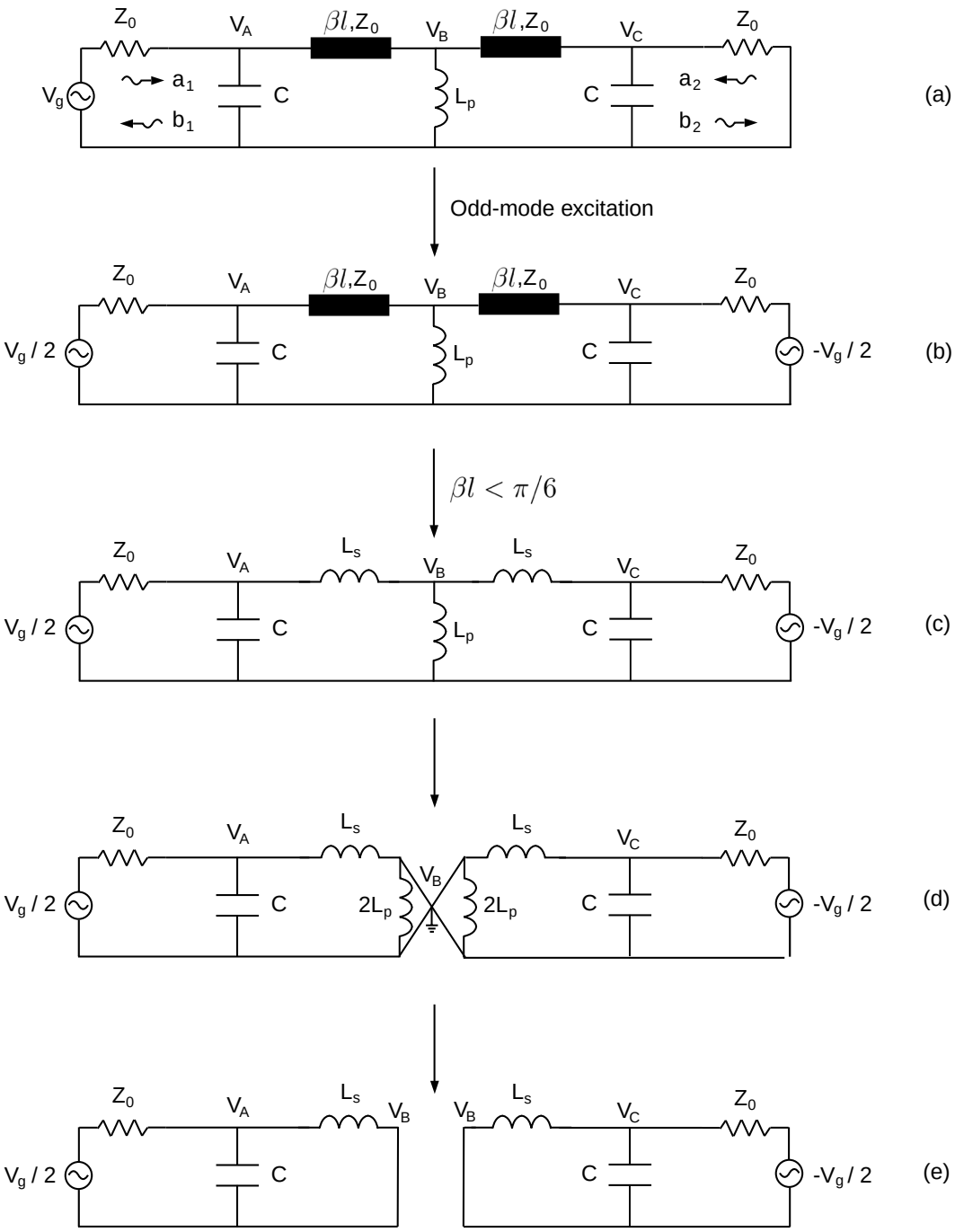


Figure 5.12: (a) Band-pass filter topology with source and load connections. (b) Odd-mode excitation (c) Short transmission line sections are replaced by their equivalent inductors (d) Network redrawn to emphasize symmetry. (e) Final topology because of the circuit symmetry.

$$V_B = V_B^e + V_B^o = \frac{V_g}{2}\frac{2L_p}{L_s + 2L_p}\frac{s\frac{\omega_{0e}}{Q_e}}{s^2 + s\frac{\omega_{0e}}{Q_e} + \omega_{0e}^2} \tag{5.15}$$

$$V_C = V_C^e + V_C^o = \frac{V_g}{2}\left[\frac{s\frac{\omega_{0e}}{Q_e}}{s^2 + s\frac{\omega_{0e}}{Q_e} + \omega_{0e}^2} - \frac{s\frac{\omega_{0o}}{Q_o}}{s^2 + s\frac{\omega_{0o}}{Q_o} + \omega_{0o}^2}\right] \tag{5.16}$$

The return loss of the filter is now calculated as

$$S_{11} = \frac{b_1}{a_1}|_{a_2=0} \tag{5.17}$$

by taking into account that

$$V_A = \sqrt{Z_0}\,(a_1 + b_1) \tag{5.18}$$

The final expression is

$$S_{11} = \frac{s\frac{\omega_{0e}}{Q_e}}{s^2 + s\frac{\omega_{0e}}{Q_e} + \omega_{0e}^2} + \frac{s\frac{\omega_{0o}}{Q_o}}{s^2 + s\frac{\omega_{0o}}{Q_o} + \omega_{0o}^2} - 1 \tag{5.19}$$

Similarly it can be shown that the insertion loss of the filter is

$$S_{21} = \frac{s\frac{\omega_{0e}}{Q_e}}{s^2 + s\frac{\omega_{0e}}{Q_e} + \omega_{0e}^2} - \frac{s\frac{\omega_{0o}}{Q_o}}{s^2 + s\frac{\omega_{0o}}{Q_o} + \omega_{0o}^2} \tag{5.20}$$

or equivalently

$$S_{21} = \frac{s\frac{\omega_0}{Q}\left(\omega_{0o}^2 - \omega_{0e}^2\right)}{\left(s^2 + s\frac{\omega_{0e}}{Q_e} + \omega_{0e}^2\right)\left(s^2 + s\frac{\omega_{0o}}{Q_o} + \omega_{0o}^2\right)} \tag{5.21}$$

where

$$\frac{\omega_0}{Q} = \frac{\omega_{0e}}{Q_e} = \frac{\omega_{0o}}{Q_o} = \frac{1}{CZ_0} \tag{5.22}$$

Evidently, this filter has two second order poles at

$$f_{pe} = \frac{1}{2\pi\sqrt{C(L_s + 2L_p)}} \quad \text{and} \quad f_{po} = \frac{1}{2\pi\sqrt{CL_s}} \tag{5.23}$$

one zero at $s = 0$ and three zeros at infinity.

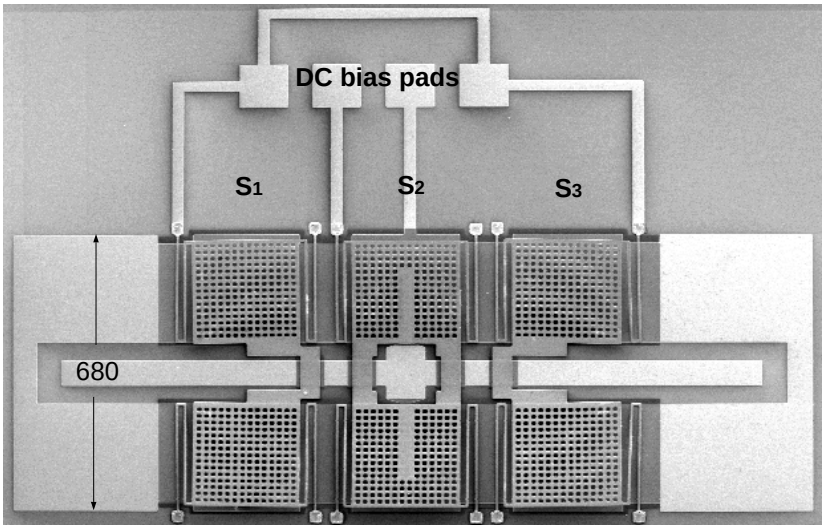
5.6.2 Implementation and Results

Based on the above equations, a bandpass filter with a tunable center frequency at 15 and 30 GHz was designed. This filter is illustrated in Fig. 5.13 along with its equivalent circuit, measured and simulated results. As described before, the filter includes the switched inductor (shunt cpw stub) in its center, which is controlled by the center switch. This inductor is tuned between 16 pH (15 GHz operation) and 9 pH (30 GHz operation). This geometry clearly shows that all elements of the filters (shunt capacitors, series inductors, shunt inductors) are tunable. Because of this key feature, this filter is also capable of preserving its absolute bandwidth even when switched over an octave frequency range. It is worth noting that the total area of this fourth order filter is less than 1 mm^2.

The measured response at 15 GHz shows an insertion loss of 3.5 dB, which agrees very well with the theoretical expectations. Both the center frequency and the bandwidth, are also correctly predicted from the theory. At 30 GHz the measured results show a loss of 4 dB. This band also shows a discrepancy between theoretical and experimental results for frequencies below 30 GHz. The reason for this discrepancy lies in the facts that 1) the tuning range of the shunt inductor is smaller that the one predicted by the theory and 2) the capacitive shorting of the inductor is not sufficient for low frequencies (see Section 5.4). The results can be improved if a metal-to-metal contact switch is used to tune the shunt inductor, particularly for designs at lower frequencies.

5.7 Conclusions

In this chapter we have demonstrated a new design scheme for tuning many circuit elements using MEMS switches. Accurate lumped-element equivalent circuits have been provided for these components and the main salient features have been



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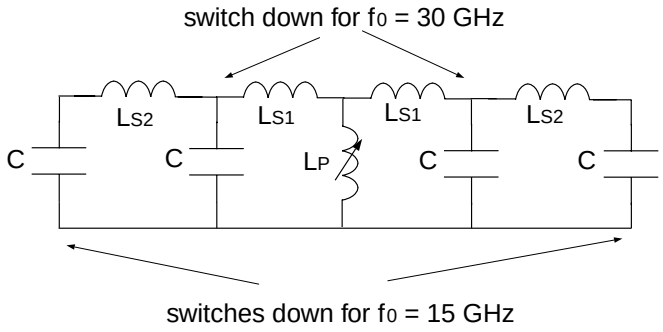

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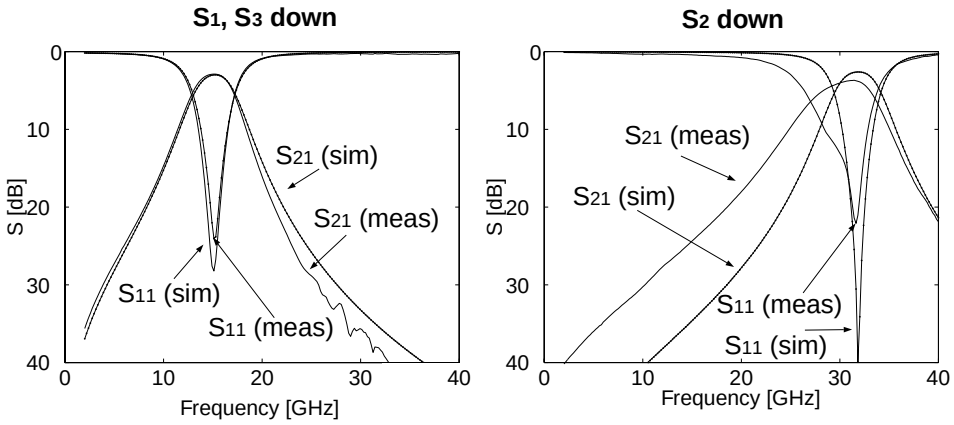


(c)

Figure 5.13: (a) Band-pass filter (dimensions are in μm). (b) Simplified equivalent circuit. (c) Simulated and measured response.

demonstrated. Reconfigurable circuits that follow the proposed techniques tend to be relatively simple, ultra compact and very wideband. This technique has been applied to the design of novel lowpass and bandpass filters that have demonstrated a very high tuning range. Overall, this method has the potential to be applied to many classes of networks where compact, wideband, tunable lumped-element components are required. However, we have observed the limitations of having only a shunt capacitive switch. The next chapter introduces the design of DC-contact switches that can greatly enhance the capabilities of these techniques.

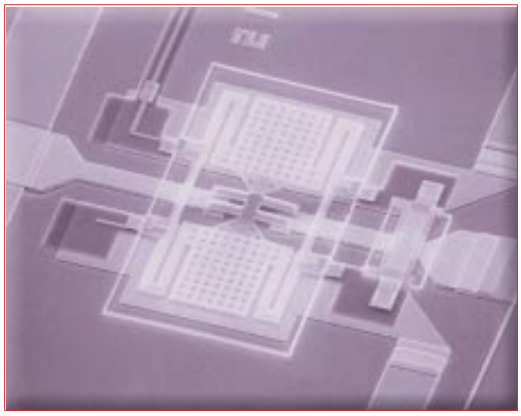
CHAPTER 6

Spring-Loaded DC-Contact Switch

6.1 Introduction

METAL-to-metal contact MEMS switches and micro-relays have received significant attention over the past few years [1] and offer an attractive alternative to capacitive switches. Several different designs with outstanding RF performance have been developed by Rockwell Scientific [56], Analog Devices and Northeastern University [3], the University of Michigan [34, 57], MIT Lincoln Laboratory [33] and others. Fig. 6.1 shows some of these designs.

The aforementioned switches typically rely on electrostatic or (less frequently) on thermal actuation mechanisms. In the typical switch structure (see Fig. 6.2) a movable beam or plate is attracted towards an actuation electrode because of an appropriately applied electric field. In other words, the electrostatically generated force serves as the actuation force for this structure. Moreover, an electric contact is achieved when the movable beam contacts the appropriate metal pad underneath it. The electrostatically generated force, therefore, serves also as the necessary contact force between the two metals. In summary, during electrostatic actuation, the applied force is responsible for 1) actuating the switch structure and 2) forming a low-resistance metal-to-metal contact. These two functions, however, do not necessarily need the same force. For



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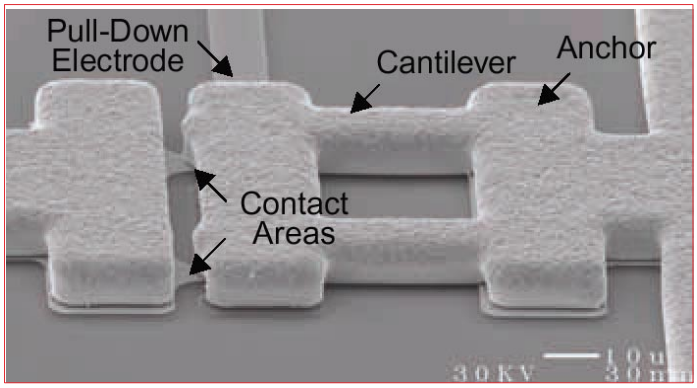

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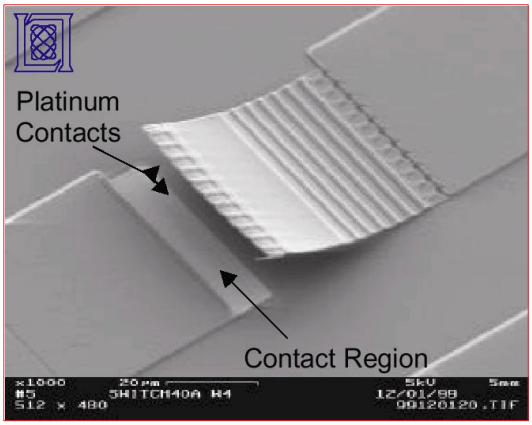


(c)

Figure 6.1: DC-contact (metal-to-metal contact switches developed by (a) Rockwell Scientific, (b) Analog Devices & Northeastern University and (c) MIT Lincoln Laboratory.

instance, although the Lincoln Laboratory switch actuates with a bias voltage of 36 V, 80 V are needed for a contact resistance of less than 1 Ω [33]. However, such a high voltage may severely impact the switch lifetime by increasing the risk of a mechanical or dielectric failure [17]. Furthermore, metal-to-metal contact switches are typically very sensitive to several fabrication parameters, such as intrinsic stress. Minor inaccuracies during the fabrication process may significantly compromise their performance. Residual gradient stress, for example, may substantially deteriorate the metallic contact and substantially increase the required actuation voltage. Similar effects are discussed in detail in Chapter 2.

A different approach of designing DC-contact switches that alleviates the aforementioned problems is introduced in this chapter. This method relies on 1) decoupling the actuation and contact forces, and 2) constructively employing gradient stress effects. Electrostatic actuation is still maintained, since it is relatively fast (switching speed in the order of a few μsec) and has very low power requirements. The metal contact, however, is achieved through a stress-originated force.

6.2 Initial Switch Design

6.2.1 Design Concept

The basic switch concept is illustrated in Fig. 6.3. The moving structure is a cantilever beam, which we will refer to as the movable cantilever beam. This beam is fabricated with a high-gradient-stress process that causes a significant upward deflection when the switch is released (Fig. 6.3a). A second and much stiffer cantilever beam (static beam) is fabricated with a low-stress process above the movable cantilever. Although the two beams are originally separated by a distance determined by the fabrication process, the two cantilevers come into direct contact immediately after the structure is released, because of the movable cantilever deflection. The movable

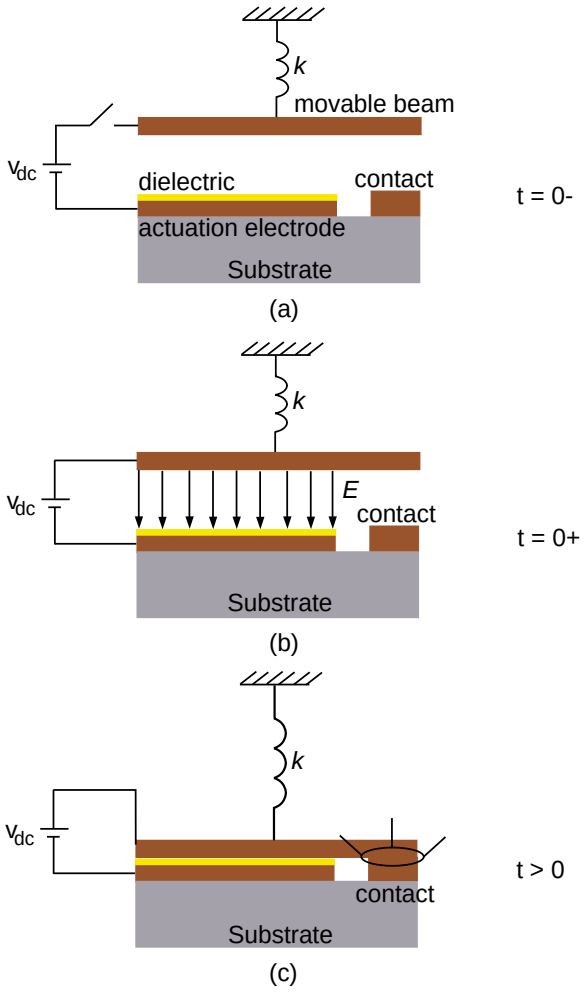


Figure 6.2: Traditional architecture for the development of DC-contact switches. (a) A schematic of the switch structure before the bias voltage is applied (b) An electric field is generated between the movable beam and the actuation electrode immediately after the bias voltage is applied to the structure. This field results in the electrostatic actuation force. (c) After sufficient time (typically in the order of a few μs) the movable beam contacts the designated metal and a short circuit is created. The electrostatically generated force is used as the contact force between the two metals.

and static beams are connected to two RF lines as Fig. 6.3a shows and thus a closed RF contact is achieved. This is the up or on state of the switch. An actuation pad covered by a dielectric layer is also fabricated underneath the cantilevers. The down or off state of the switch is realized when a DC potential is applied between the movable cantilever and the actuation pad. If this potential is higher than the movable

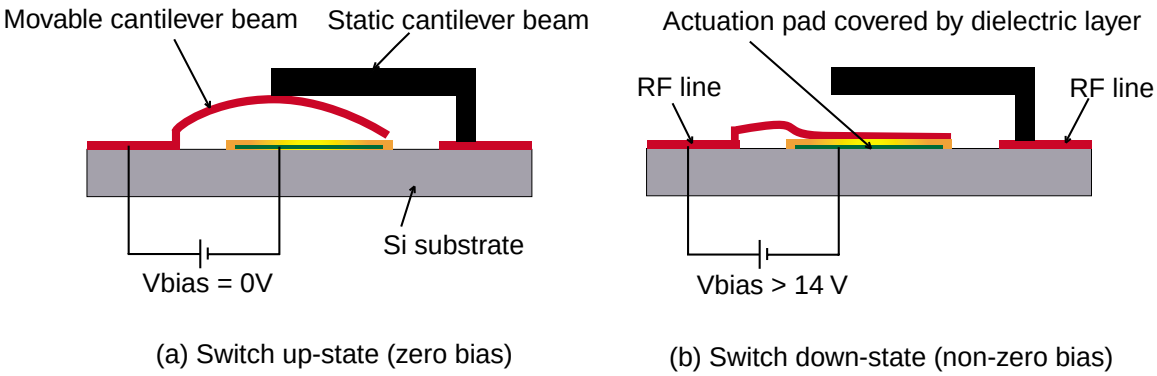


Figure 6.3: Basic switch concept and operation. (a) When no bias is applied, the movable cantilever touches the stiff static beam leading to a metal-to-metal contact. (b) If the DC bias is higher than the actuation voltage of the movable beam, this beam deflects downwards leading to an open circuit.

beam's actuation voltage, this beam deflects and the contact points are separated (Fig. 6.3b). Although the static cantilever is a very stiff beam, as a precaution it is always maintained at the same potential as the actuation pad. Therefore, this beam does not deflect under the influence of the applied DC bias.

Typically a low on-state insertion loss, high off-state isolation, and low actuation voltage are the desired properties of such a switch. The on-state insertion loss is dominated by the contact resistance, which depends on the movable beam geometry, stiffness, and distance from the static beam. It also depends on the fabrication procedure and especially on the types of metals used and their surface smoothness. Sections 6.4 and 6.5 discuss this issue in more detail. On the other hand, the off-state isolation is primarily determined by the distance between the two beams and their overlap area. Finally, because of the movable beam shape and stress, it is difficult to analytically calculate the switch actuation voltage. Nonetheless, a low bound may be obtained assuming that the beam is at a mean distance of D from the actuation

pad. Then the following formula [58] for the actuation voltage may be used:

$$V_{min}^{th} = \frac{8}{3}\left(\frac{EID^3}{3\epsilon_0 AL^3}\right)^{1/2} \tag{6.1}$$

where E=Young's modulus of the movable beam material, I=same beam moment of inertia, ϵ_0=free space dielectric permittivity, A=effective area between the movable beam and the actuation electrode, and L=movable beam length. Although this formula may be useful for a first hand-calculation, it will only yield a low bound since no stress effects are introduced in it.

6.2.2 Fabrication Process

A seven mask process, summarized in Fig. 7.3, is required for the fabrication of the proposed switch.

- The process starts with the preparation of a 400 μm silicon substrate with 2000 $\mathring{A}$ of SiO_2. A lift-off process is first performed to define the bias lines and the actuation pad. These lines are made of a thin SiCr layer (1200 $\mathring{A}$) that is sputtered on top of the negative photoresist [57]. These lines are essential for biasing the switch without affecting the RF signal [34].
- A second lift-off process defines the RF lines, which are made of evaporated Ti and Au layers of 500 and 9000 $\mathring{A}$ respectively.
- The actuation pad and bias lines are covered by 3000 $\mathring{A}$ of Si_3N_4 deposited by a PECVD process and patterned with a dry RIE etch.
- A positive photoresist is then spun and patterned to form the first sacrificial layer. Appendix B presents the details of this patterning. However, it is important to note that an additional hardbaking of 160°C for 3.5 min follows the traditional lithography. This is essential in preventing the photoresist sacrificial layer from bubbling and destroying the switch when hardbaked in subsequent

steps. Also, for low-actuation voltage switches the thickness of this layer is between 0.8–1.2 μm.

- The fifth mask is used to define the movable cantilever beam. 2000 $\mathring{A}$ of Ti followed by 7000 $\mathring{A}$ of Au are evaporated on the whole wafer for this purpose. These layers are subsequently etched except for the locations of the first beam. This is an important step since the induced stress on the beam will determine the deflection magnitude and slope. If the residual gradient stress is not sufficiently high, the movable beam will deflect only a few thousand $\mathring{A}$, resulting in a poor contact. On the other hand, if excessive stress is introduced, adhesion problems between the movable beam and the sacrificial layer will render the rest of the process impossible.
- After this beam is formed, the second sacrificial layer is defined by spinning and soft-baking a 2–2.5 μm layer of polyimide DuPont PI2545. The anchor points for the second beam are then defined similarly to the process reported in [15].
- The seed layer (2000 $\mathring{A}$ of Au) necessary for electroplating the second beam is sputter deposited and patterned. It was experimentally found that there is no need for any adhesion layer between Au and polyimide, especially since this layer is only used as a seed layer. Furthermore, an adhesion layer of Ti or Cr underneath the Au layer would deteriorate the desired metal-to-metal contact.
- The seed layer is then patterned and electroplated to about 6 μm to form a stiff gold beam (static beam).
- Finally, the two sacrificial layers are etched and the structure is dried and released with a standard supercritical CO_2 process.

SEM pictures of three series coplanar waveguide (cpw) switches fabricated with this process can be seen in Fig. 6.5. The first structure (Fig. 6.5a) presents a switch with no static beam fabricated. This picture clearly shows the shape of the movable beam after the switch is released. The fabrication process of this beam induces such

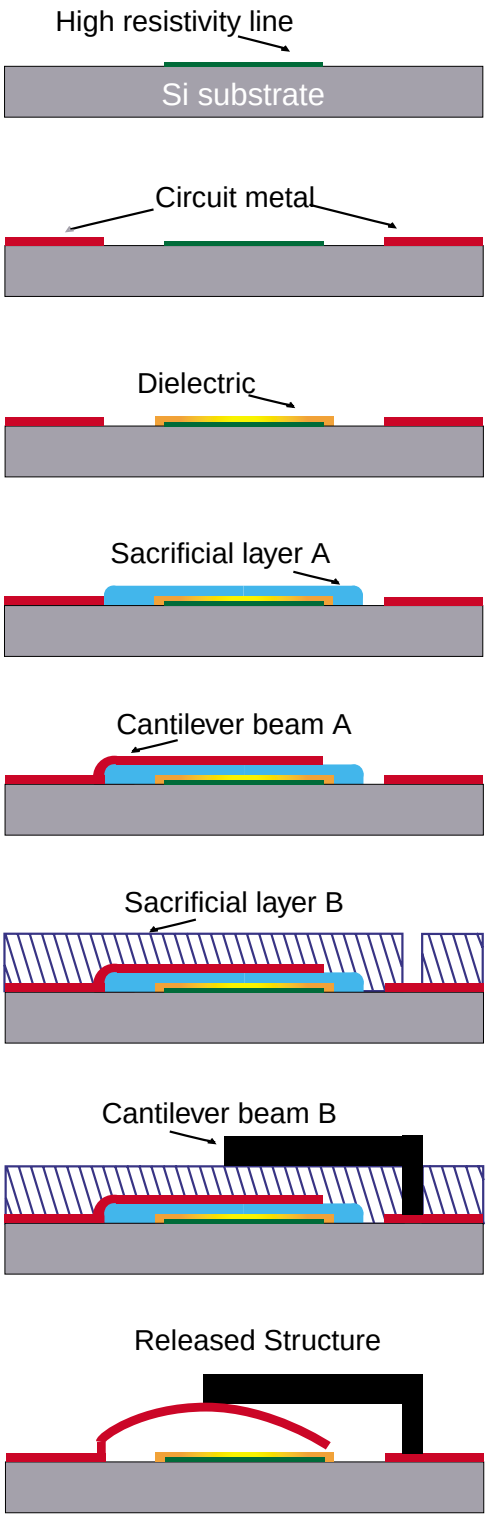
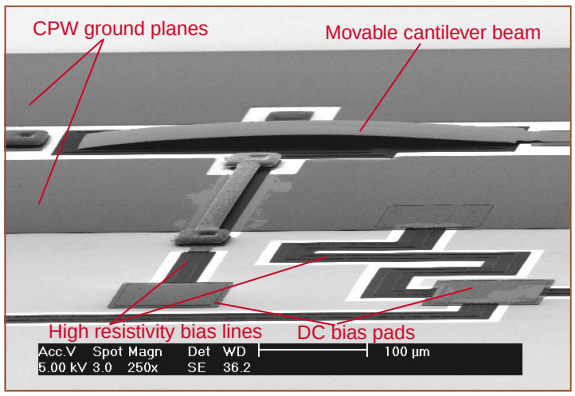
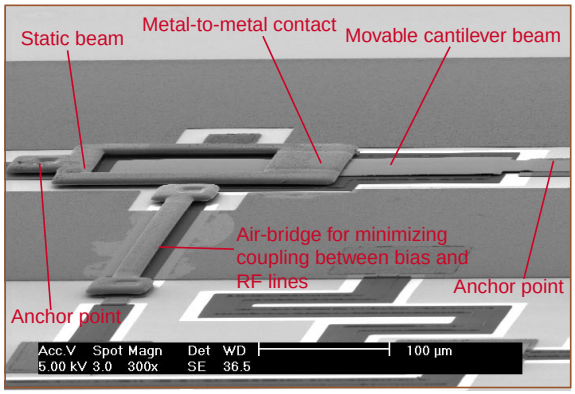


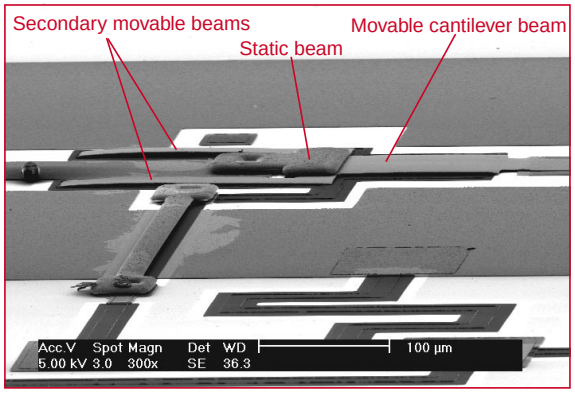
Figure 6.4: Process flow for the fabrication of a MEMS switch.



(a) Switch with 500 µm movable beam and no static beam. The maximum beam deflection is approximately 10 µm and occurs at the center of the beam. The switch is fabricated such that the suitable stress is induced on the movable beam, which deflects with the appropriate slope at its center leading to a successful metallic contact.



(b) Switch with 300 µm movable beam and 160 µm static beam. A rectangular hole has been introduced in the static beam to minimize the down-state capacitance and increase the isolation.



(c) Switch with 300 µm movable beam and 50 µm static beam. The movable beam splits into two parts after the contact with the static beam is made. This results in a short, stiff static beam and shortens the path that the RF signal has to travel out of the cpw.

Figure 6.5: SEM pictures of fabricated switches.

a stress that its center contacts the static cantilever with a zero slope. A completed switch with the static beam included is shown in Fig. 6.5b. The static beam is a low-stress and thick cantilever connected to the left part of the cpw center conductor. A large rectangular hole has been also introduced in this beam in order to minimize the overlap area of the two beams and thus increase the off-state isolation. The movable cantilever is connected to the right part of the center conductor in both structures. Therefore, the two beams become part of the RF circuit in both the up and down states. Finally, the third structure (Fig. 6.5c) is similar to the second one, except for the movable beam geometry. This beam splits into two parts (secondary movable beams) after the contact point with the static beam. This geometry has the advantage of having a short and thus stiffer static beam. Furthermore, the distance that the RF signal is travelling out of the cpw line is now half of that for the structure of Fig. 6.5b, which results in less mismatch loss.

Some of the bias details are also visible in these pictures, which also illustrate the need for high resistance bias lines. In other words, since the bias circuitry comes into direct contact with the RF lines, a strong coupling between the RF and DC signals will occur unless these high resistance lines are introduced.

6.2.3 Results and Discussion

The RF performance of these switches was measured by an 8510C Vector Network Analyzer with the help of an Alessi Probe Station and GGB Picoprobe 150 μm pitch coplanar probes. The effects of the probes and their RF lines to the network analyzer are de-embedded by a standard wideband TRL calibration [48, 49]. Both geometries of Fig. 6.5b and Fig. 6.5c gave similar results, but the last one gave a better on-state performance. Fig. 6.6 presents the measured and simulated RF performance of this geometry.

Fig. 6.6a shows that the switch presents an up-state insertion loss of 0.14 and

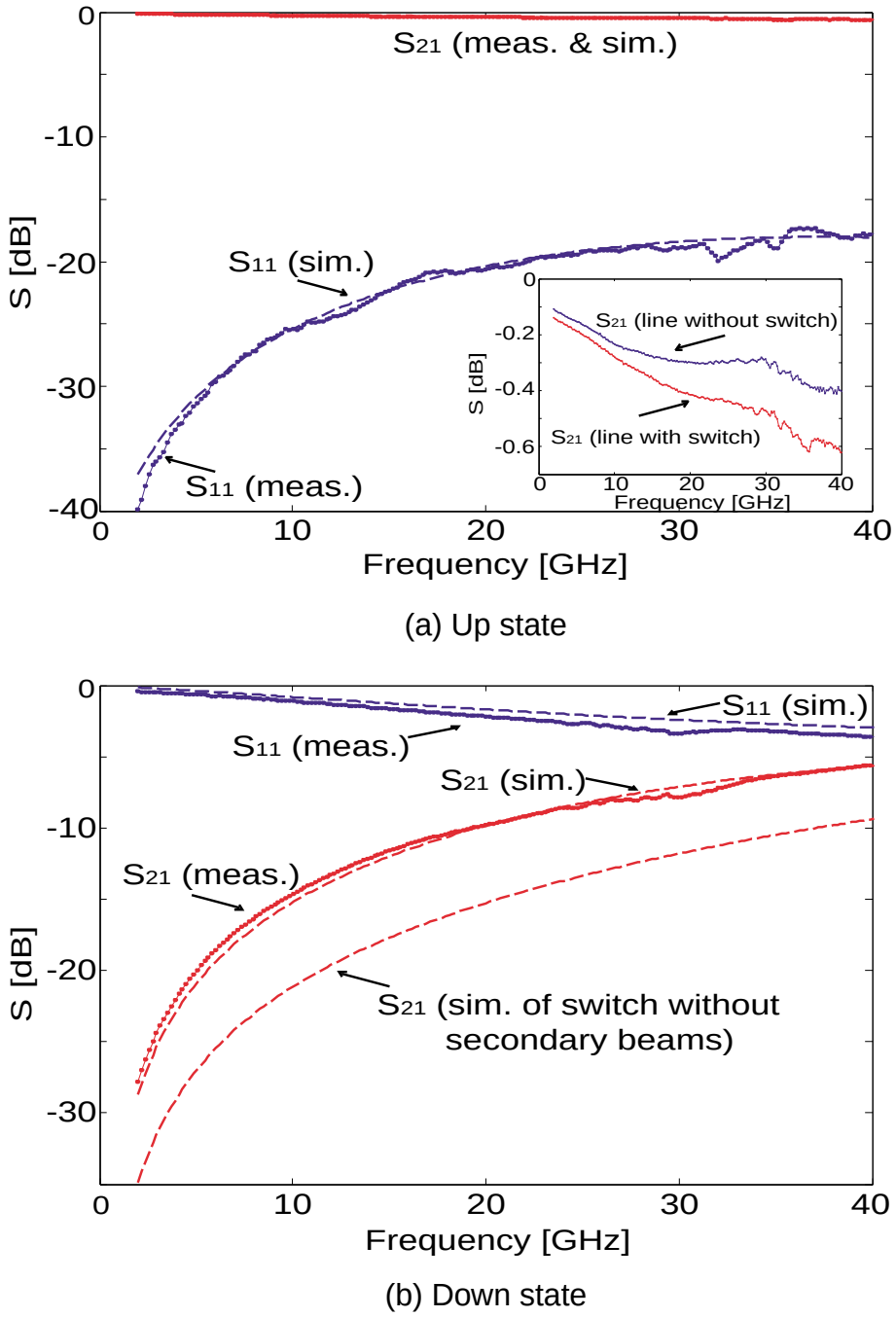
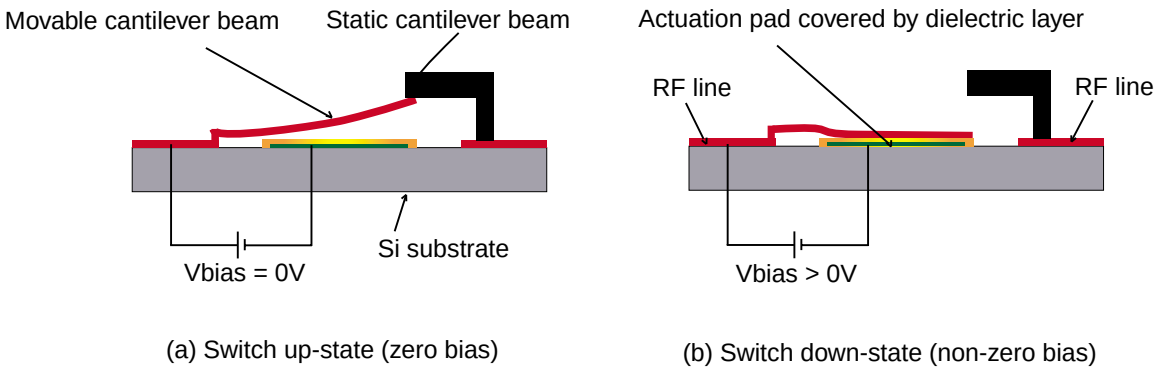


Figure 6.6: Measured and Simulated results of the switch shown in Fig. 6.5c for the (a) up and (b) down state.

0.38 dB at 2 and 20 GHz respectively. Comparing the low-frequency loss values with a cpw line of the same total length (500 μm) and metallization (0.9 μm of Au), a

contact resistance of 0.7 Ω is extracted. Moreover, the measured return loss of the switch is less than −18 dB from 2 to 40 GHz. This slight mismatch is due to the fact that the switch is not at the same level as the cpw line. In other words, although the movable beam is only 3 μm away from the Si substrate at the contact area, it still has a parabolic shape with a mean distance of about 6−7 μm from the substrate. This is the distance that was used in the full wave simulation [55].

Although outstanding up-state results were observed, the down-state measurements reveal an inferior performance. The measured switch isolation is 28 dB at 2 GHz and remains higher than 10 dB up to about 20 GHz. This corresponds to a down-state capacitance of approximately 30 fF. However, the photoresist and polyimide thicknesses were 0.8 and 2 μm respectively and, as a result, the theoretical down-state distance between the movable and the static beams is about $d_{th} = 2.8$ μm. Considering that the overlap area between the two beams is 70×30=2100 μm^2, a down-state capacitance of 6.6 fF is calculated using the well-known quasi-static formula. Even if fringing field capacitance is considered, the down-state switch capacitance is still three times smaller than 30 fF. On the other hand, the simulated results agree very well with the experimental values (Fig. 6.6b) and reveal that the dominant coupling mechanism is not the down-state capacitance, but rather the two secondary beams (Fig. 6.5c). The simulation was repeated for a hypothetical switch without these two beams and the results show a 7 dB improvement in the switch isolation (Fig. 6.6b). However, such a switch would only be possible by altering the stress distribution on the movable beam, thus ensuring that this beam would deflect the same way without the secondary beams. Such a switch is presented in the next section.



(a) Switch up-state (zero bias)

(b) Switch down-state (non-zero bias)

Figure 6.7: Optimized switch design. The coupling between the input and output RF lines is minimized with this design.

6.3 Optimized Switch

The switch design illustrated in Fig. 6.7 does not suffer from the high coupling between the secondary beams and the cpw line. This design is possible provided that the required deflection of the movable beam can be achieved. This deflection, which depends of course on the stress distribution of this beam, is typical of metals with mismatched thermal expansion coefficients (see Chapter 2 and [59]).

This stress distribution was successfully achieved by sputtering a layer of Ti/Au 2500/7500 $\mathring{A}$ at 7mT Ar pressure. This step replaces the evaporation of the Ti/Au used in the initial switch implementation. The difference between the two stress distributions is caused by the different deposition processes. Fig. 6.8a shows a switch without the top static beam. The movable beam is 230 μm long and its tip deflection is approximately 75 μm. This is the average tip deflection among 5 measured beams. Furthermore its deflection profile follows closely the one of Fig. 6.7.

One more improvement of this design has been the fabrication of beam stoppers underneath the movable beam as shown in Fig. 6.8b. These stoppers are fabricated by introducing an additional lift-off process (Ti/Au 500/500 $\mathring{A}$) immediately after the formation of the high-resistivity lines and actuation pads. They are later protected by the PECVD Si_3N_4. The major advantage of these stoppers appears in the

switch down state as they considerably limit the contact area (and therefore adhesion force) between the movable beam and the Si_3N_4 layer. This improvement significantly alleviated several stiction problems observed in the previous design.

As discussed in the introduction of this chapter a low contact resistance requires a high contact force. This force is typically in the order of tens of μN [60, 61] but it heavily depends on the surface profile and cleanliness. A first-order calculation of this force in the pre-stressed cantilever beam with the top beam is necessary in estimating the required residual stress. Two methods –one analytical and one experimental– were employed to compute this force. The first method follows the analysis found in [62, 63, 64] and is based on the theory of bimorph cantilevers. The second one, is based on some tests structures specifically fabricated to measure the contact force. As shown in the next two sections, the combination of these methods provides a good estimate of the contact force.

6.4 Bimorph Cantilever Model

Fig. 6.9 shows a schematic of the Ti/Au bimorph cantilever and the forces and moments acting on a cross section along the length of the cantilever. The variables used as well as their values can be found in Table 6.1. Because of the common interface between the two different materials, the forces and moments must balance.

$$P_1 = P_2 = P \tag{6.2}$$

$$P\frac{t_1 + t_2}{2} = M_1 + M_2 = \frac{E_1 I_1}{r} + \frac{E_2 I_2}{r} \tag{6.3}$$

since beam theory yields

$$M_1 = \frac{E_1 I_1}{r} \quad , \quad M_2 = \frac{E_2 I_2}{r} \tag{6.4}$$

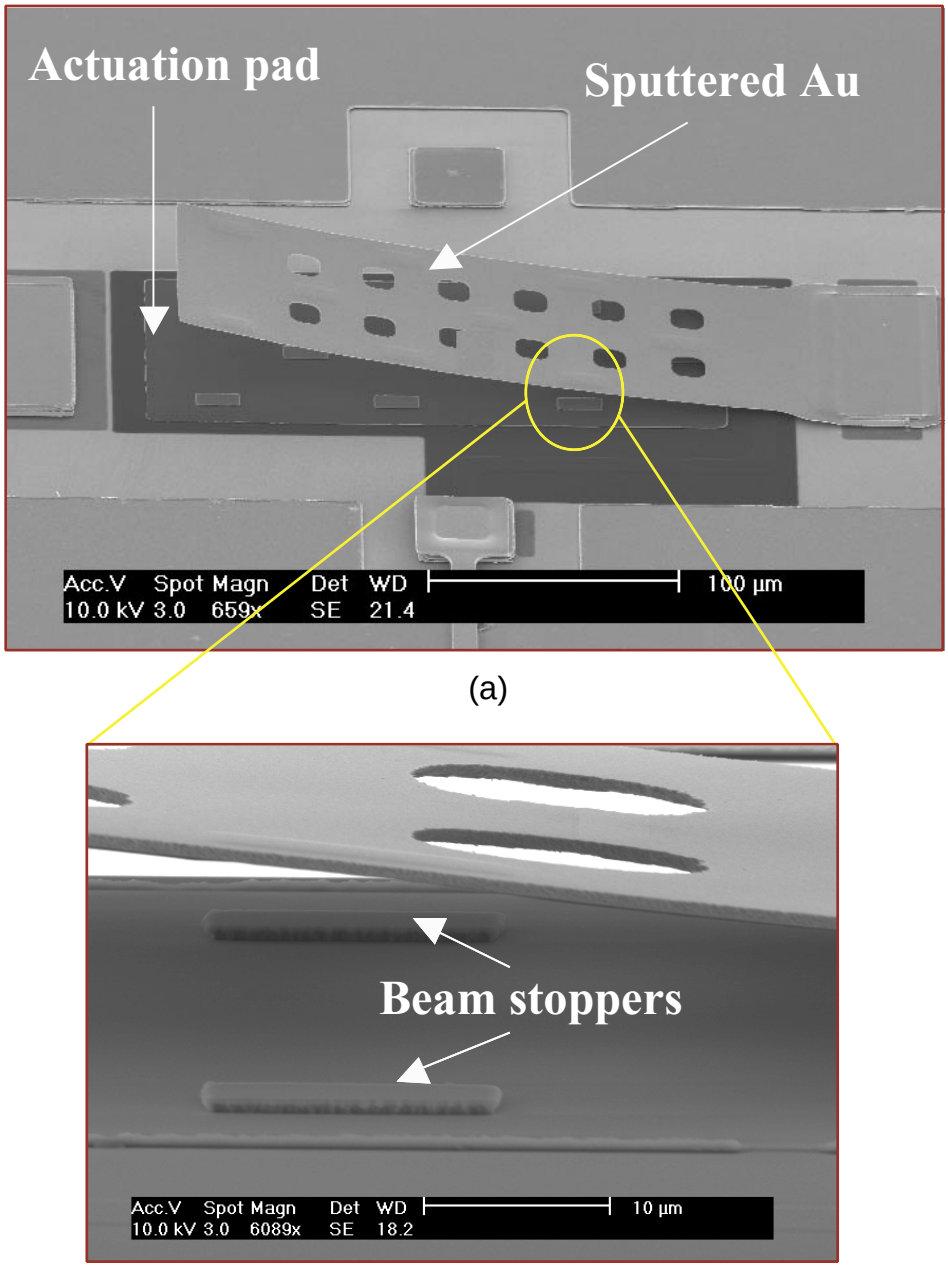
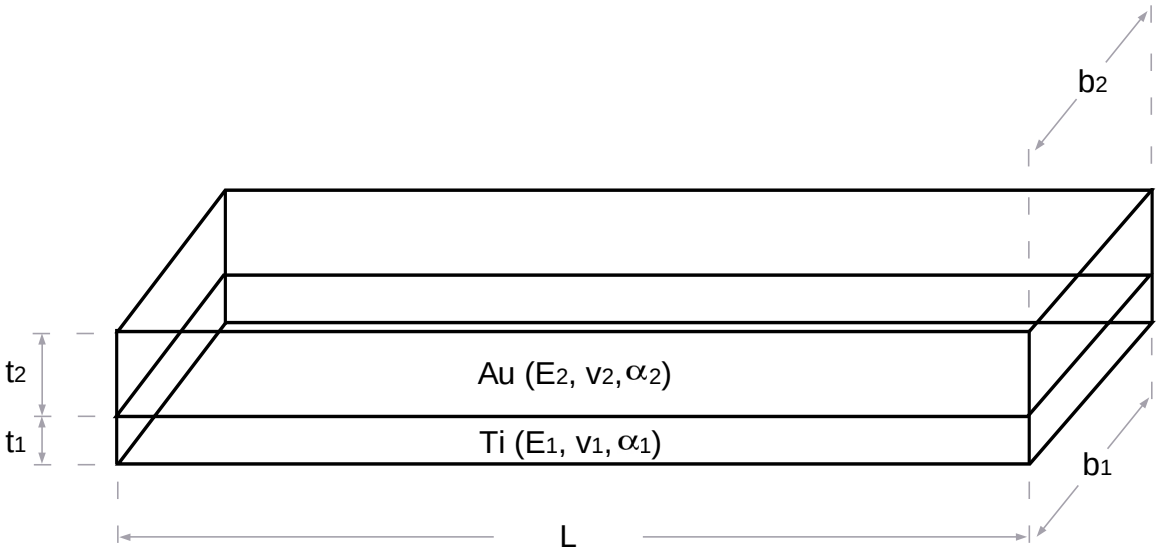
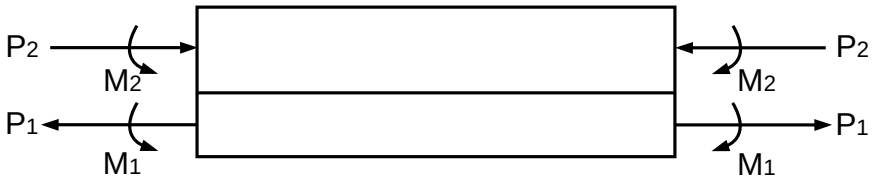


Figure 6.8: (a) SEM picture of the fabricated switch without the top static beam using the optimized process. (b) This detail shows two of the fabricated beam stoppers underneath the movable beam. These stoppers are important in the down state because they limit the contact area (and therefore adhesion force) between the movable beam and the Si_3N_4 layer underneath it.

r is the radius of curvature of the cantilever beam and I_1, I_2 are the moments of inertia for the Ti and Au layer respectively. It is important to underline that the



(a)



(b)

Figure 6.9: (a) Schematic of the bimorph movable cantilever (b) Force and moments acting on the cross section of a segment along the length of the bimorph cantilever.

bi-axial modulus of elasticity has to be used in all analytical formulas about the bimorph beam. The thermal mismatch between the two layers of the cantilever beam is uniform across all directions, causing the beam to deform along its length as well as along its width. This plate-like behavior increases the beam's stiffness and its

Table 6.1: Variables used in the bimorph cantilever model and their respective values

Variable	Description	Value	Dimension
E_1	Ti Young's Modulus of Elasticity	116	GPa
E_2	Au Young's Modulus of Elasticity	80	GPa
ν_1	Ti Poisson's Ratio	0.34	none
ν_2	Au Poisson's Ratio	0.42	none
$E_{1,b}$	Ti Bi-axial Modulus of Elasticity	$E_1/(1-\nu_1)$	GPa
$E_{2,b}$	Au Bi-axial Modulus of Elasticity	$E_2/(1-\nu_2)$	GPa
α_1	Ti Coefficient of Thermal Expansion (20 °C)	8.9	μm/m-°C
α_2	Au Coefficient of Thermal Expansion (20 °C)	14.4	μm/m-°C
L	Bimorph Cantilever Length	230	μm
b_1	Ti Layer Width	80	μm
b_2	Au Layer Width	80	μm
t_1	Ti Layer Thickness	0.25	μm
t_2	Au Layer Thickness	0.75	μm

characterized by the biaxial modulus of elasticity defined as [65]:

$$E_b = \frac{E}{1-\nu} \tag{6.5}$$

Although this will not be made explicit in the following, the biaxial modulus of elasticity will be used whenever the symbol of modulus of elasticity E is written.

The normal strain of Ti and Au also has to be the same at their interface. Hence:

$$\alpha_1 \Delta T + \frac{P}{E_1 t_1 b_1} + \frac{t_1}{2r} = \alpha_2 \Delta T - \frac{P}{E_2 t_2 b_2} + \frac{t_2}{2r} \tag{6.6}$$

where ΔT is the equivalent temperature difference that would result in the radius of curvature r.

By equations (6.3) and (6.6) the radius of curvature can be found:

$$k = \frac{1}{r} = \frac{6 b_1 b_2 E_1 E_2 t_1 t_2 (t_1 + t_2)(\alpha_2 - \alpha_1)\Delta T}{(b_1 E_1 t_1^2)^2 + (b_2 E_2 t_2^2)^2 + 2 b_1 b_2 E_1 E_2 t_1 t_2 (2t_1^2 + 3t_1 t_2 + 2t_2^2)} \tag{6.7}$$

The radius of curvature is related to the beam's maximum deflection d_{max} (at the tip) with the following formula [62]

$$d_{max} = 2r\left(\sin\frac{L}{2r}\right)^2 \tag{6.8}$$

The force of a bimorph cantilever is distributed linearly along its length. An equivalent force F_{eq} at the tip can be defined, however, as the necessary force to counteract the thermally induced force. This force will be given by

$$F_{eq} = K_{eq} d_{max} \tag{6.9}$$

where K_{eq} is the equivalent spring constant of the cantilever. In order to calculate K_{eq} the equivalent flexural rigidity $(EI)_{eq}$ of the beam needs to be known. This quantity is given by [66, 64]

$$(EI)_{eq} = \frac{(b_1 E_1 t_1^2)^2 + (b_2 E_2 t_2^2)^2 + 2b_1 b_2 E_1 E_2 t_1 t_2 (2t_1^2 + 3t_1 t_2 + 2t_2^2)}{12(b_1 E_1 t_1 + b_2 E_2 t_2)} \tag{6.10}$$

Thus the equivalent force at the tip of the cantilever can be calculated by

$$F_{eq} = \frac{3(EI)_{eq} d_{max}}{L^3} \tag{6.11}$$

Based on the values given in Table 6.1 the equivalent contact force is calculated to be

$$F_{eq} = 16.4\ \mu\text{N} \tag{6.12}$$

The next section presents a number of test structures fabricated to experimentally validate this model.

6.5 Test Structures for Contact Force Estimation

Fig. 6.10 shows a schematic diagram of a test structure suitable for measuring stress-induced contact forces. The structure consists of two cantilever beams C_b and C_s. C_b is the Ti/Au cantilever beam used in the DC-contact switch as the movable beam. C_s is a stress-free Au cantilever beam that deflects upwards under the force applied by C_b. The contact force between the two beams may be extracted by measuring the final deflection δ of the stress-free beam and the following equation:

$$F_s = \frac{3E_s I_s \delta}{L_s^3} = \frac{E_s w_s t_s^3 \delta}{4L_s^3} \tag{6.13}$$

where E_s, $I_s = w_s t_s^3/12$, and L_s are the Young's modulus (not bi-axial), moment of inertia and length of the stress-free cantilever C_s. It should be noted that since C_s has a finite stiffness and deflection, F_s will be always smaller than F_{eq} calculated in the previous section. The accuracy of this method depends on 1) the ability to fabricate stress-free cantilever beams with zero out-plane deflection and 2) the ability to accurately measure δ. Low-stress cantilever beams with zero out-of-plane deflection were fabricated by sputtering 2 μm of Au with a low-stress process (10 mT Ar sputtering pressure). The out-of-plane deflection of these beams was measured with an optical microscope with a measurement accuracy of ± 1 μm.

Fig. 6.11 shows a microphotograph of a test structure fabricated for measuring the contact force F_s. Three different types of these test structures were fabricated. Each of these structures included an $L = 230$-μm long Ti/Au (0.25/0.75 μm) bimorph cantilever beam fabricated underneath an $L_s = 140$ μm long and $t_s = 2$ μm thick stress-free cantilever. The width w of the stress-free cantilever was varied between 40 and 10 μm. Table 6.2 summarizes the measured results of these test structures. Each deflection on this table is the average deflection obtained from three identical beams. Based on the measured deflections and equation (6.13) the calculated contact

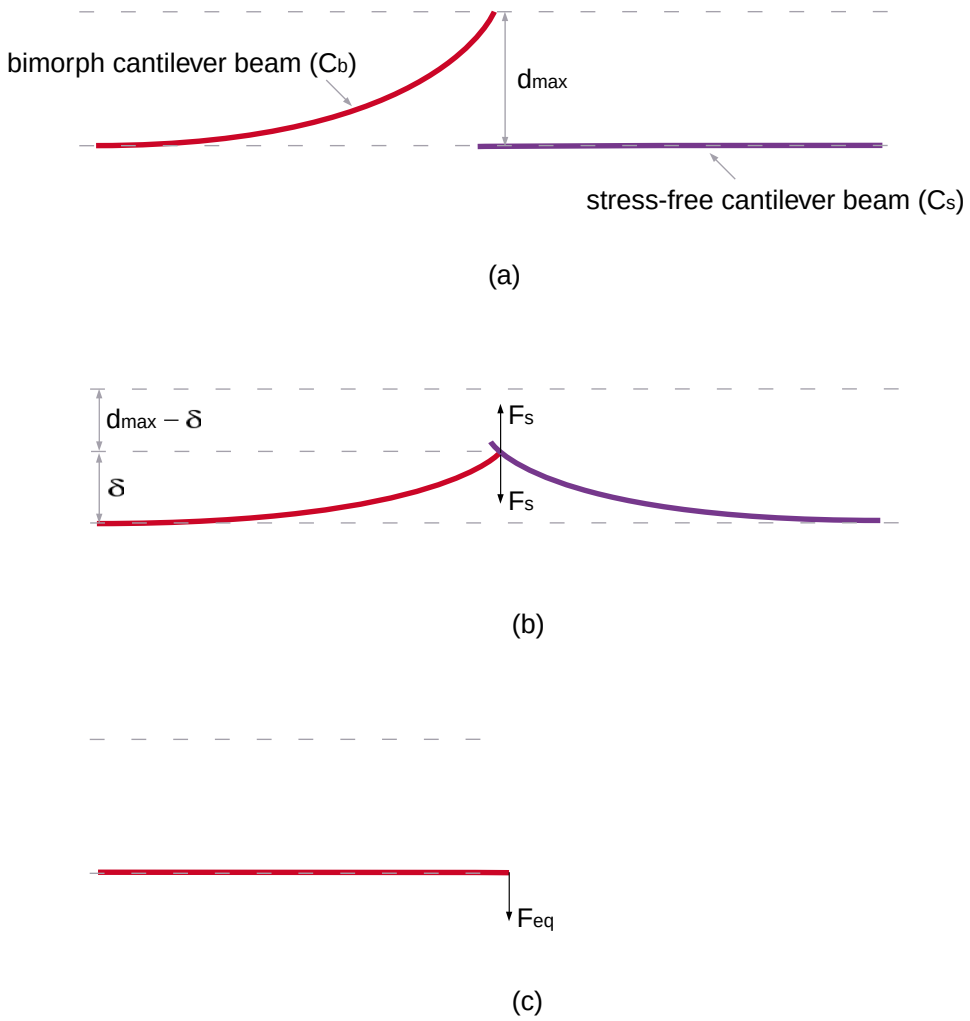


Figure 6.10: (a) Schematic of the bimorph cantilever beam (C_b) and the stress-free cantilever beam (C_s). Under no external forces the maximum deflections for C_b and C_s are d_{max} and 0 respectively (b) The stress-free beam C_s deflects upwards by δ under the force applied by C_b. The contact force of the two beams is F_s. (c) The bimorph cantilever C_b experiences zero deflection under the influence of an external force F_{eq} applied to its tip. This is the maximum possible contact force.

force varies between 11.7 (for $w_s = 10$ μm) and 17.5 μN (for $w_s = 10$ μm). These extracted force values compare well with the analysis of the previous section. This can be verified if equation (6.11) is used to calculate F_{eq}. In this case d_{max} has to be replaced by $d_{max} - \delta$ in order to account for the finite stiffness of the stress-free cantilever beam. Based on the results of these sections and the stiffness of the top

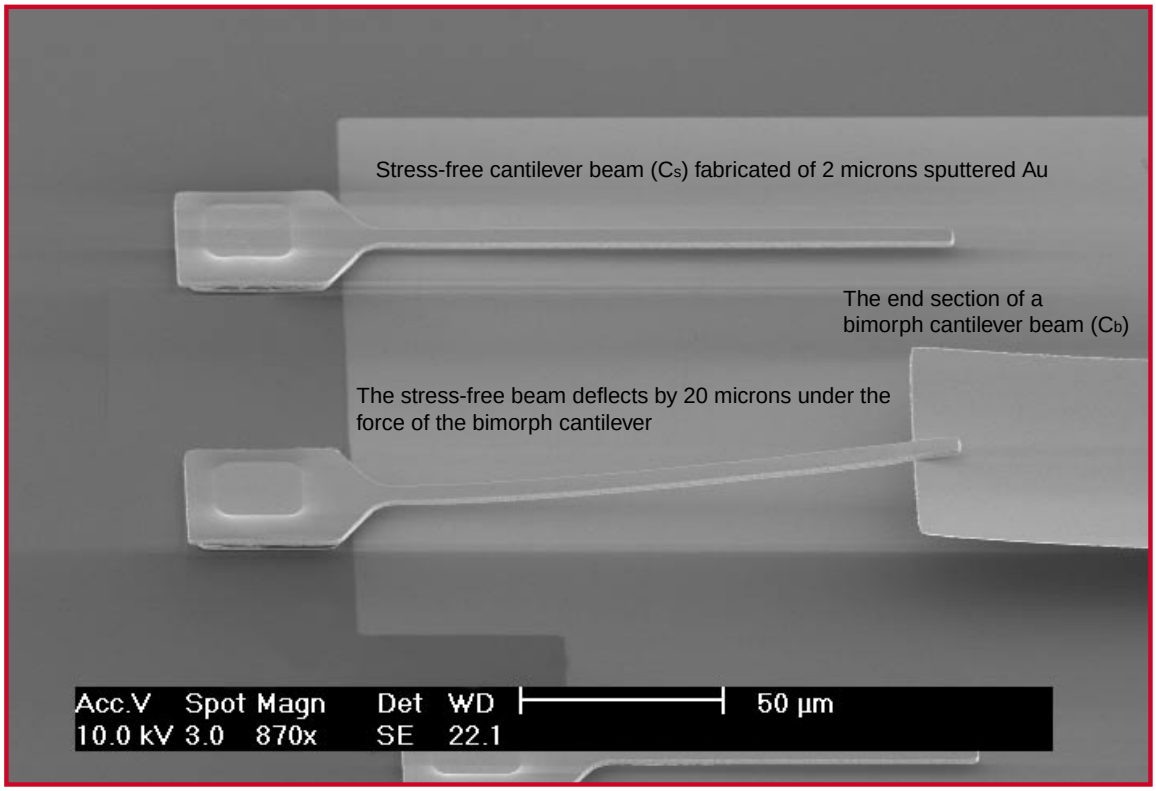


Figure 6.11: Microphotograph of a fabricated test structure for measuring the contact force between a bimorph cantilever and a stress-free cantilever beam.

beam of the switch, the contact force between the two beams in the actual switch structure is estimated to be approximately 19–20 μN. The next section presents the measured switch contact resistance and isolation.

6.6 Measured Results and Discussion

Fig. 6.12 shows a microphotograph of a fabricated switch. The movable and stiff cantilever beams can be clearly seen in this figure. An optical interferometric image of this switch was also acquired and is presented in Fig. 6.13. This image shows that the movable beam, despite the pressure, remains reasonably flat and close to the actuation pad underneath it.

Six identical switches were measured and their average actuation voltage was 50-

Table 6.2: Measured results of the fabricated structures for measuring the contact force F_s

W^a [μm]	δ^b [μm]	${F_s}^c$ [μN]	$F_{eq}^{\delta\ d}$ [μN]
40	7.5	17.5	14.5
20	11	12.8	13.6
10	20	11.7	11.3

[a]Width of cantilever C_s

[b]Measured deflection of cantilever C_s caused by the force F_s

[c]Contact force between cantilevers C_b and C_s (see Fig. 6.11)

[d]Force applied to the tip of the bimorph cantilever necessary to reduce its tip deflection from d_{max} to δ. This force can be computed from equation (6.11) if d_{max} is replaced by $d_{max} - \delta$

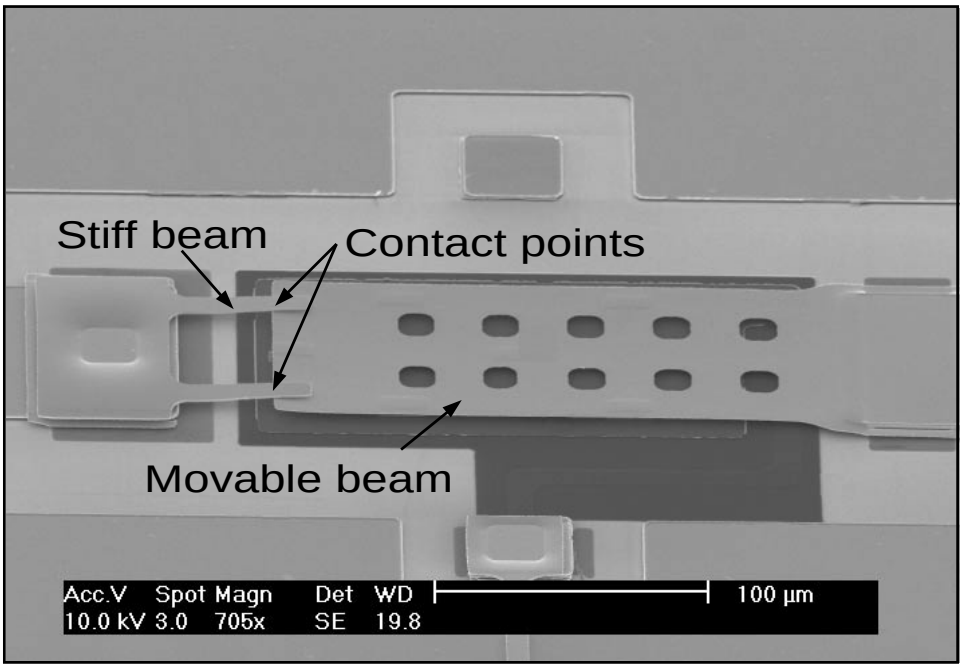


Figure 6.12: Microphotograph of a fabricated optimized spring-loaded DC-contact switch.

60 V. Fig. 6.14 shows the de-embedded on-state measured S-parameters from these switches. The term "de-embedded" refers to calibrated measurements that do not include the loss of any transmission lines connecting the switch to the measurements set-up. The on-state switch loss is on average 0.05 and 0.14 dB at 2 and 40 GHz respectively. The observed slope in the measurements is due to the fact that the

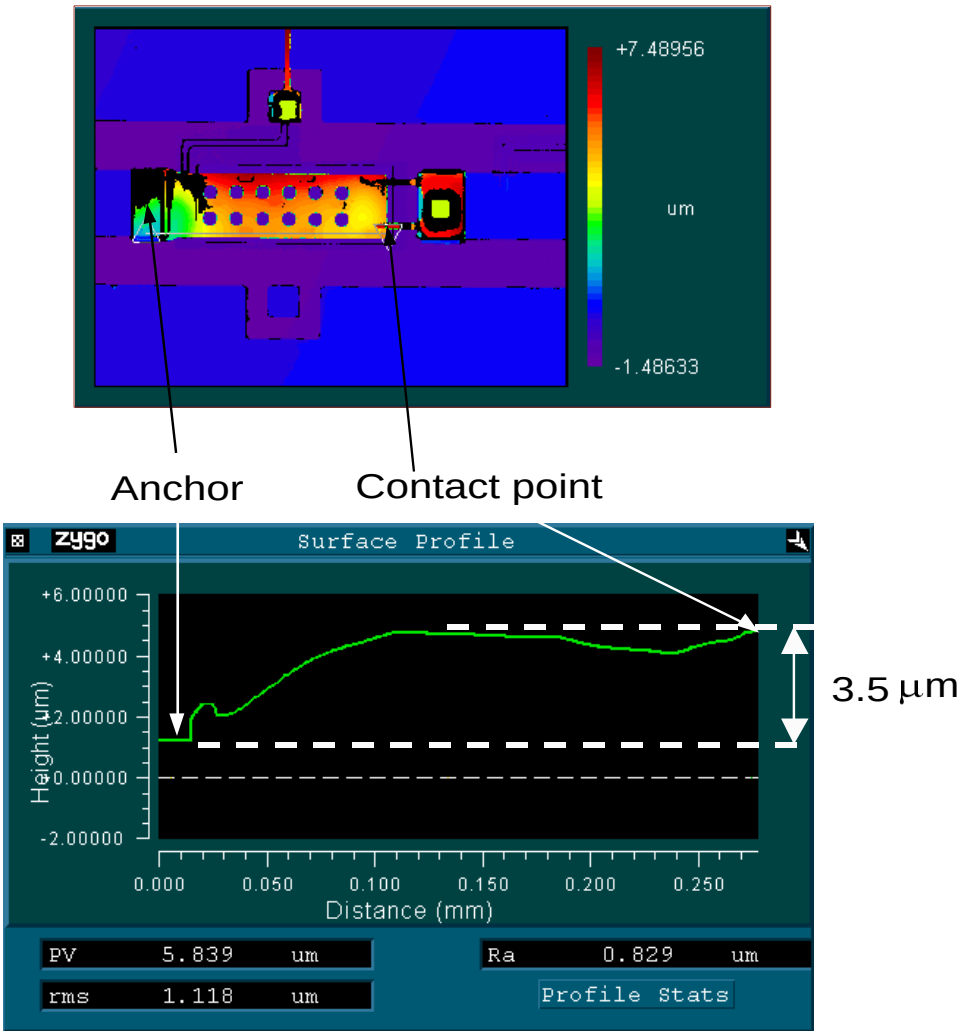


Figure 6.13: Interferometric image of the switch shown in Fig. 6.12.

switch is a 1-μm thick, 80-μm wide and 230-μm long Au beam that introduces an additional small loss versus frequency. The switch return loss is below -19 dB up to 40 GHz. This slight mismatch is due to the fact that the movable beam is approximately 3.5 μm higher than the cpw line. Fig. 6.15a shows the switch equivalent circuit whose component values can be fit to the measured data. This fitting results in an on-state contact resistance of $R_s = 0.5\ \Omega$. This contact resistance is among the lowest that have been reported in the literature and shows that stress-induced forces are sufficiently high to result in very low contact resistance. It is also interesting to note that the impedance of the line in the model is approximately 62 Ω to match the

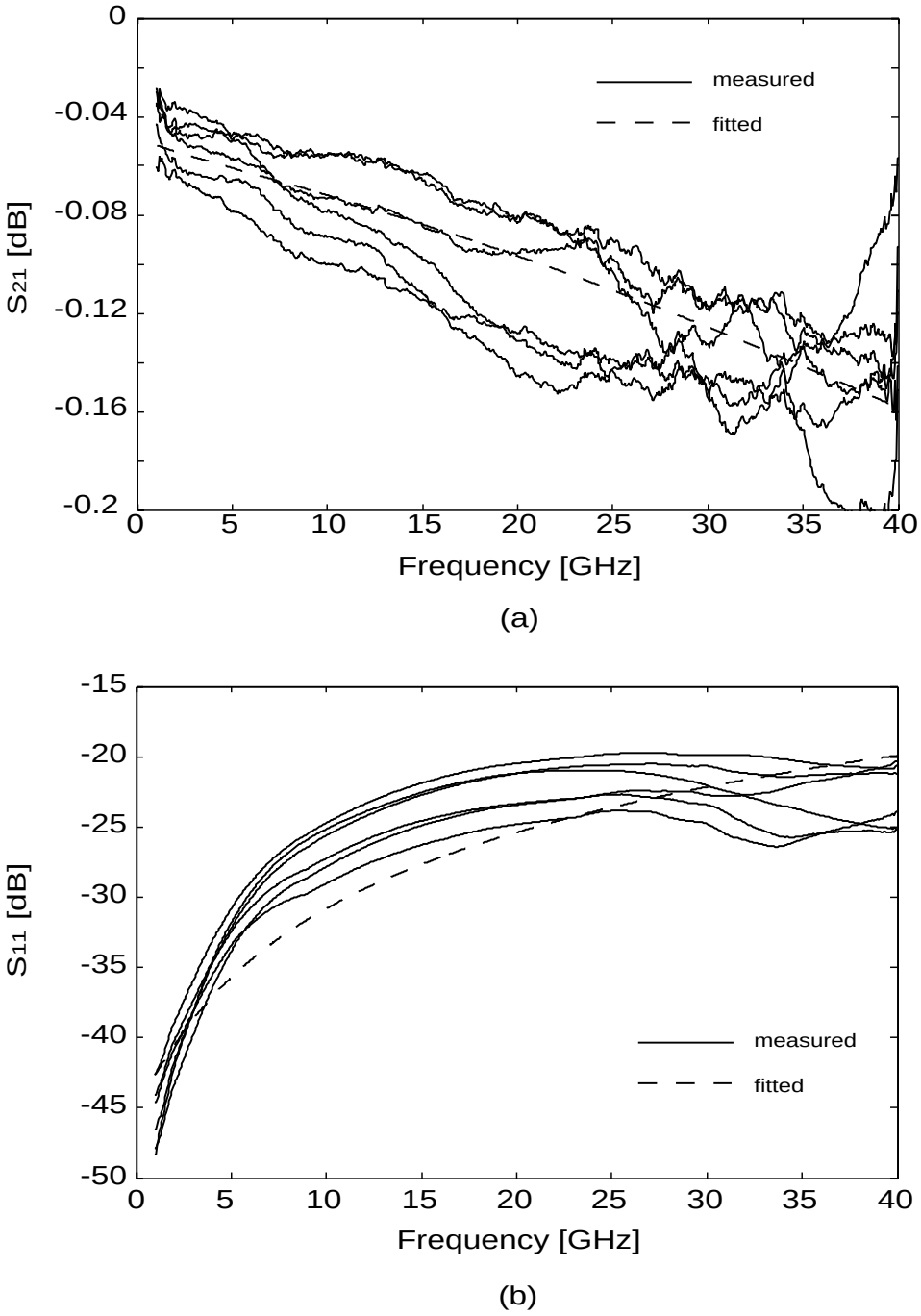


Figure 6.14: On-state measured (a) insertion loss and (b) return loss of six identical spring-loaded switches. The fitted S-parameters that are based on the equivalent circuit of Fig. 6.15a are also presented.

measured return loss.

Fig. 6.16 presents the off-state switch isolation versus frequency. On average,

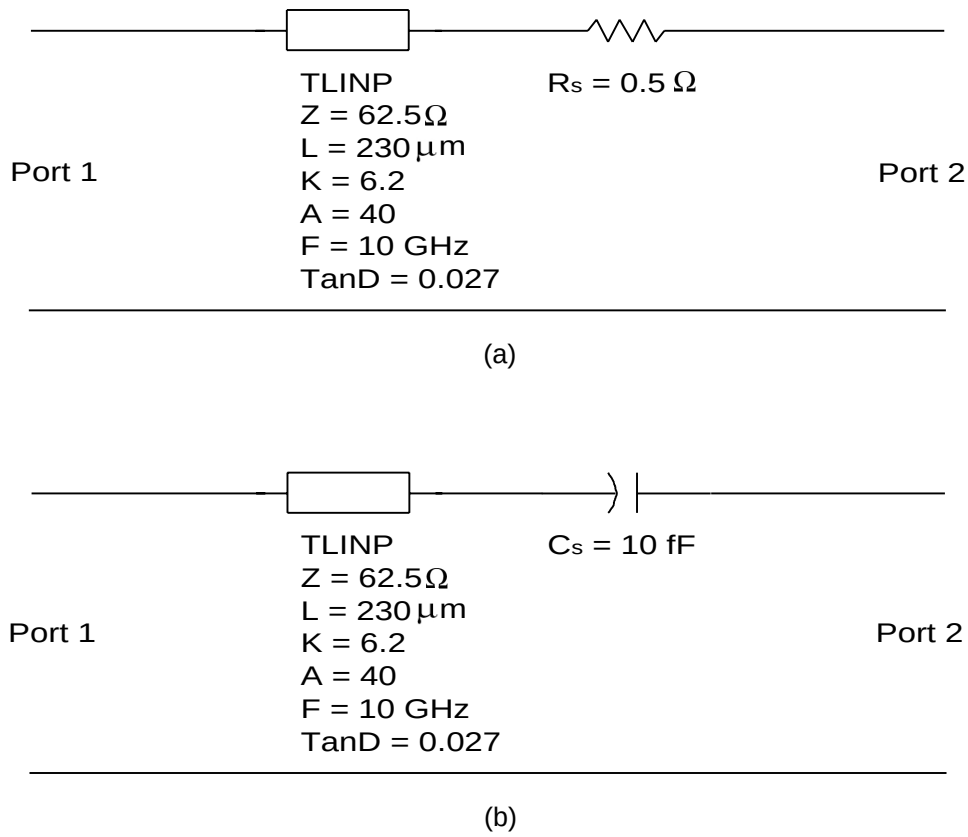


Figure 6.15: (a) On- and (b) off-state extracted ADS equivalent circuit of the spring-loaded DC-contact switch.

the measured isolation is 38 and 13 dB at 2 and 40 GHz respectively. This is a substantially improved performance compared to the initially obtained results of Section 6.2.3. Based on the measured isolation, the switch off-state series capacitance is C_s = 10 fF on average. The simulated switch performance based on this fitted capacitance is also plotted in Fig. 6.16.

6.7 Conclusions

A novel design scheme for metal-to-metal contact RF MEMS switches has been introduced. These switches are electrostatically actuated, but the DC-contact is achieved through a stress-originated force. The contact resistance is not related to

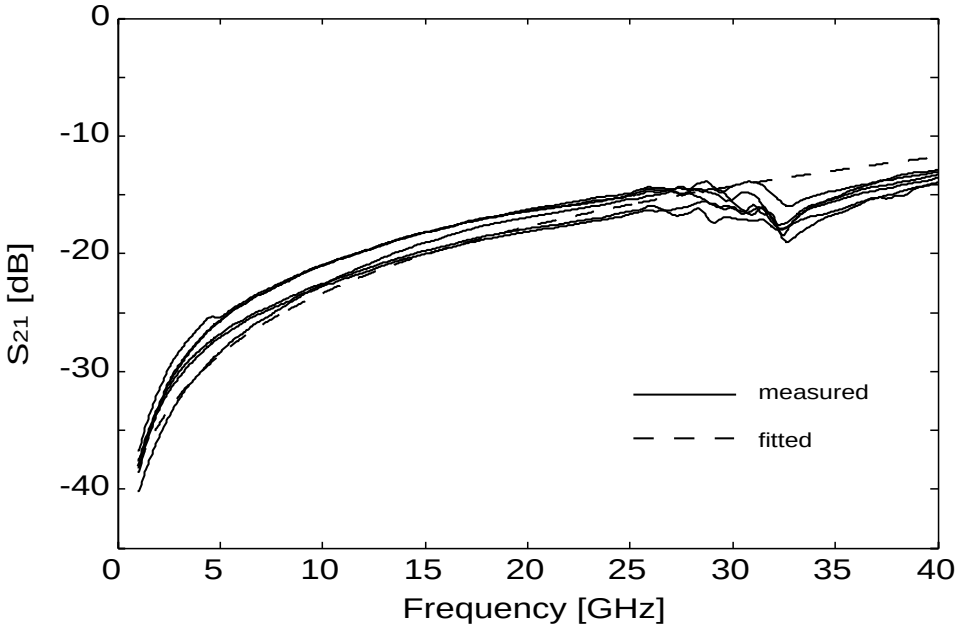


Figure 6.16: Off-state measured and fitted isolation of six identical spring-loaded DC-contact switches.

the actuation force and only depends on the residual stress in the switch. We have demonstrated state-of-the-art results with this switch for both its on and off states. The switch insertion loss has been measured to 0.05 dB at 2 GHz, which corresponds to an on-state contact resistance of 0.5 Ω. Additionally, the switch provides an off-state isolation of 38 and 13 dB at 2 and 40 GHz respectively. The extracted off-state series switch capacitance is 10 fF.

CHAPTER 7

Electrostatically-Tunable Analog RF MEMS Varactors with Ultra High Capacitance Range

7.1 Introduction

A number of different high-frequency switches and their applications have been presented in the previous chapters. These devices and their associated circuit designs rely on electrostatic actuation because of its simplicity and its very low biasing power requirements. This actuation mechanism, however, results in the well-known pull-in effect that forces the micro-switch to collapse when it moves (approximately) one third of its initial height. Although this effect does not significantly impair the switching operation, it can be a serious limitation to MEMS variable capacitors and applications that require analog rather than digital tuning. Voltage control oscillators, tunable filters and matching networks are a few examples where analog tuning can be particularly beneficial.

Two main approaches have been proposed in the literature to overcome this issue. The first one relies on digital MEMS variable varactors that are typically implemented by a bank of MEMS switches [67]. In the second approach the value of a MEMS capacitor is changed in a continuous way by tuning the gap between two parallel plates

[5, 68, 69]. The main advantage of the digital tuning technique is the ability to achieve very high tuning ranges, similar to the on/off capacitance ratios of MEMS switches. Furthermore, the digital approach leads to components with relatively low sensitivity to fabrication process variabilities and vibration. Nevertheless, the required switch bank can occupy a large space and the interconnecting lines typically result in high losses and low self-resonant frequencies. On the other hand, the analog MEMS varactors have low losses, occupy less space and are relatively easy to implement. Their tuning range, however, is relatively limited and can be sensitive to vibration, residual stress and temperature. A further advantage of the analog MEMS varactors is that they are typically non-contact MEMS devices and are, therefore, inherently more reliable than contact type of MEMS (digital varactors or switches).

This chapter focuses on presenting a new analog MEMS varactor with ultra high tuning range, up to 4:1 (300%). This technique is based on the idea of an extended tuning range varactor proposed by Zou et al. in 2001 [5]. Fig. 7.1 shows the traditional analog MEMS varactor as well as the extended tuning range varactor presented by Zou. In the conventional design the RF capacitance is sensed between two parallel plates with an overlap area A and initial spacing x_0. When a DC voltage is applied between them the spacing is decreased up to a minimum (theoretical) value of $2x_0/3$. If the bias voltage is increased beyond this limit, the top plate will snap on the bottom one and the ability to smoothly tune the gap x will be lost. This is the well-known pull-in effect and limits the tuning range of this varactor to a maximum value of 50%. This value is a theoretical limit and rarely achieved in practice because of residual stress in the beam. Practical circuits based on this approach typically achieve a tuning range of approximately 20–30% [70].

One way to increase the tuning range of the parallel-plate varactor is to allow the gap x to be varied beyond the pull-in point. This is achieved by the extended tuning-range varactor, schematically illustrated in Fig. 7.1b. The key idea in this

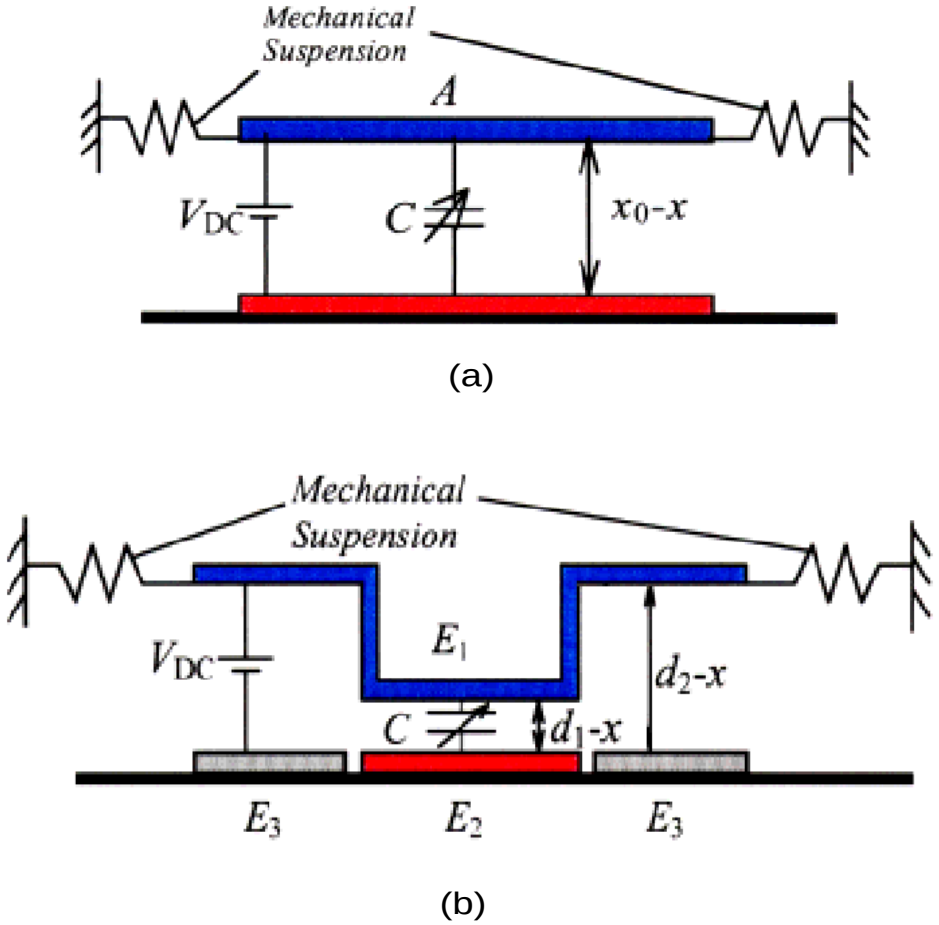


Figure 7.1: (a) Schematic of the traditional analog MEMS varactor based on tuning the gap between two parallel plates or beams in a continuous way. (b) Extended tuning range analog MEMS variable capacitor as presented by Zou [5].

design is to separate the DC biasing plates (E_1 and E_3) from the RF capacitive plate (E_2). The initial spacing d_2 between the movable structure and plates E_1 and E_3, in particular, is designed to be larger than the gap d_1 that controls the RF capacitance. By taking into account that when a bias voltage V_{DC} is applied, all plates are pulled down by a distance x, the tuning range TR of the structure can be calculated as

$$TR = \frac{C - C_0}{C_0} = \frac{\frac{\epsilon A}{d_1 - x} - \frac{\epsilon A}{d_1}}{\frac{\epsilon A}{d_1}} = \frac{x}{d_1 - x} \tag{7.1}$$

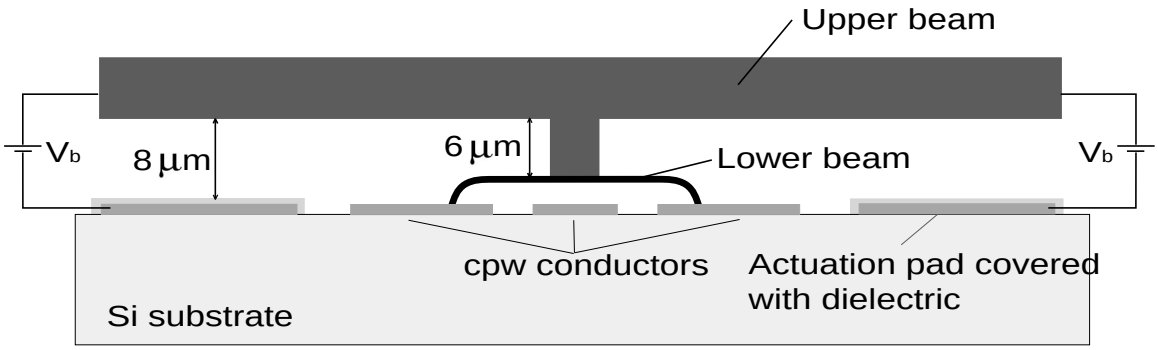
As long as $x < d_2/3$ the structure will not suffer any pull-in effect and the movable beam can be pulled infinitely close to the plate E_2, resulting in a (theoretically) infinite tuning range.

Despite this encouraging theoretical result, practical circuits are still limited by the residual stress in the structure. Zou et al. achieved a measured tuning range of 70%, while Dussopt and Rebeiz measured 46% out of a very similar device [68]. The main reason behind this is the non-uniform movement of the movable beam or plate because of the residual stress in it. Other researchers have focused on a three-plate structure to balance the pull-in effect [71]. The maximum measured tuning range in this case was 86%. Of course the pull-in effect can be completely eliminated by considering other actuation mechanisms. Feng et al., for example, designed a variable capacitor based on thermal actuation with a measured capacitance range of 270% (3.7:1). This extended range, however, comes at a price of considerably higher power consumption (in the order of mW) and slower speed (response time is in the order of msec for thermally driven devices).

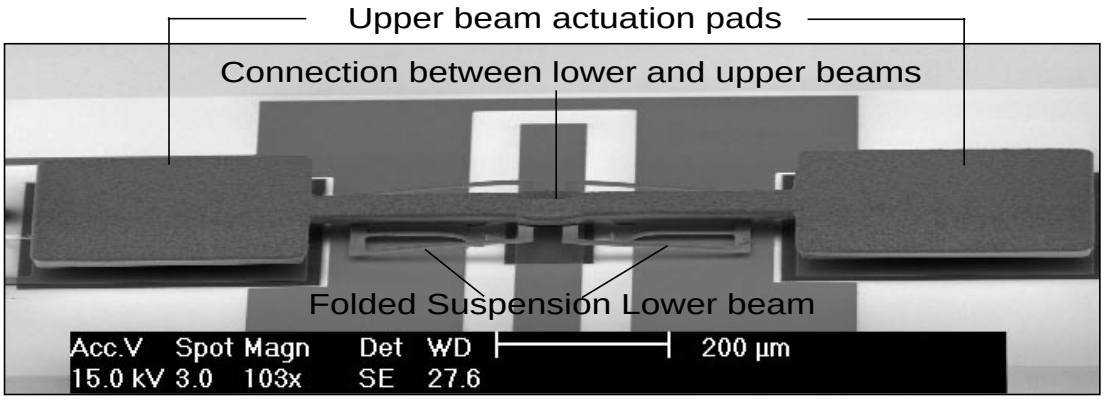
Our proposed varactor also follows the extended tuning range approach, but it is based on a two-metal, two-sacrificial-layer process and results in a measured tuning range of nearly 4:1 (300%). Furthermore, it still uses electrostatic actuation, thus preserving the advantage of low DC power consumption. Section 7.2 discusses the design of this varactor. The fabrication process follows in Section 7.3, while our RF experimental results are reported in Section 7.4. Some reliability results from this device are also presented in Section 7.5.

7.2 RF MEMS Varactor Design

Fig. 7.2a shows a schematic of the proposed device. This device is composed of two Au beams. The first beam (lower beam) is a 0.7-μm thick beam that is suspended



(a)



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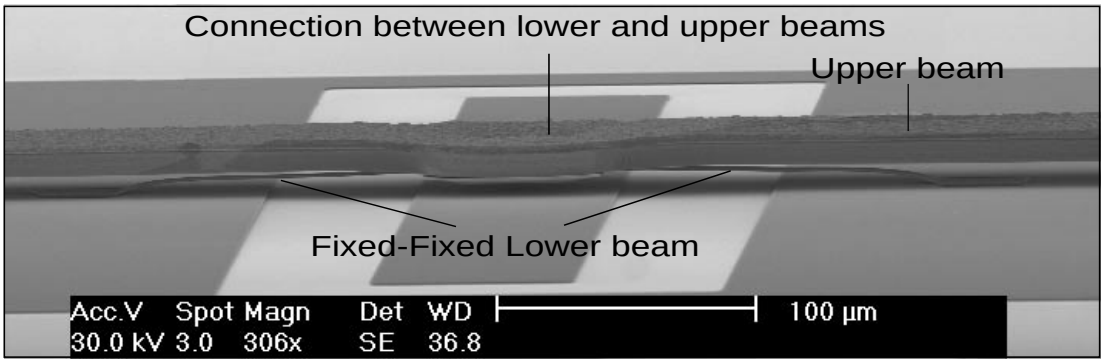


(c)

Figure 7.2: (a) Schematic diagram of the proposed analog MEMS varactor. (b) First implementation of the analog MEMS varactor. This varactor uses a folded-suspension lower beam (FSLB) and a dielectric layer underneath the lower beam. (c) Second implementation of the analog MEMS varactor This varactor uses a fixed-fixed lower beam (FFLB) and it does not have any dielectric layer that could prevent a DC-contact between the lower beam and the center conductor of the cpw.

$g_1 = 2$ μm above a 50/80/50-μm coplanar waveguide (cpw) line, while the second one (upper beam) is 13-μm thick and is suspended $g_2 = 6$ μm above the lower beam. Figs. 7.2b and c illustrate two possible implementations of the lower beam. The first one (Fig. 7.2b) shows a folded-suspension lower beam design (FSLB design), while the second one (Fig. 7.2c) shows a fixed-fixed lower beam design (FFLB design). The second difference between the two implementations is the fact that in the FSLB design a dielectric layer covering the cpw line prevents direct metal contact between the lower beam and the center conductor of the cpw, while this is not the case in the FFLB design. Both implementations are based on the same design principles but they yielded slightly different experimental results.

In both designs the anchor points of the lower beam are connected to the ground planes of the cpw line. Furthermore, in both designs the upper beam (which is suspended $g_2 = 6$ μm above the lower beam) has no anchor points, but is connected to the middle of the lower beam. Although the upper beam is almost 1-mm long, it is very stiff, because it is made of 13 μm of low-stress electroplated Au. The upper beam also forms two 360×300-μm^2 pads (upper pads) that are suspended a total distance of $g_{tot} = g_1 + g_2 = 8$ μm above the two electrostatic actuation pads covered with a dielectric layer as shown in Fig. 7.2a.

When an electrostatic potential V_b is applied between the upper beam and the two actuation pads, the lower beam deflects, because its spring constant is three orders of magnitude lower than the upper beam's. Additionally, because of the height difference between the two beams, the pull-in instability for the upper beam does not occur until it moves by approximately 2.5 μm downwards. This means that the upper beam does not collapse before the lower beam touches the center conductor of the cpw line (in the FFLB case) or the dielectric layer covering it (in the FSLB case). When this happens (at $V_b = V_{ct}$), both beams have moved by about 2 μm, which is the maximum allowable distance the lower beam can travel. Consequently, in both cases

the tuning range of the varactor can be designed to be very high and is limited only by fabrication issues, such as residual stress, thickness and roughness of the dielectric layer.

7.3 Fabrication Process

Fig. 7.3 summarizes the six-mask process that is necessary for the fabrication of the varactor. The fabrication is only briefly presented here since it is similar to the one of Chapter 6. The varactors are fabricated on a high-resistivity Silicon substrate (approximately 2000 Ω-cm) with 2000 $\mathring{A}$ of thermally grown SiO_2. The fabrication starts with a lift-off process of Ti/Au 250/9000 $\mathring{A}$ that is performed to define the 50/80/50 cpw lines and the actuation pads. PECVD deposition of 3000 $\mathring{A}$ Si_3N_4 follows, which is patterned with a dry RIE process. This dielectric layer is mainly deposited to protect the actuation pads from potential direct contact with the upper beam. The first sacrificial layer (photoresist SC1827 by Shipley) is subsequently spun at 3.5 krpm and patterned. This sacrificial layer is post-baked at a 180°C hotplate for 3.5 min to avoid any out-gasing in the remaining of the process. The lower beam deposition and patterning follows. This beam is made of low-stress 0.7 μm Au and is anchored at two or four points, depending on the design (see Fig. 7.2). A second sacrificial layer (photoresist AZ 9260 by Clariant) is spun at 4 krpm and patterned. This photoresist results in a 6-μm layer after being post-baked in a 150°C oven for 1h. A thin layer (1000 $\mathring{A}$) of low-stress Au is subsequently sputter deposited on top of the second sacrificial layer. This layer is electroplated to 12-13 μm to create the very stiff upper beam described in Section II. The final steps are the etching of the sacrificial layer and drying of the varactors with a conventional supercritical CO_2 process. It is worth noting that no adhesion layer is required between the sputtered Au and the photoresist in both depositions described in this process. Such an adhesion layer (e.g.

Ti or Cr) could easily create a significant mismatch between the two metals (Ti/Au or Cr/Au) and result in a significant warping of the structure.

7.4 Results and Discussion

7.4.1 FSLB Tuning Range

The RF performance of these varactors was measured from 2–40 GHz by an 8510C Vector Network Analyzer with the help of an Alessi Probe Station and GGB Picoprobe 150 μm pitch coplanar probes. The effects of the probes and their RF lines to the network analyzer are de-embedded by a standard wideband TRL calibration [48, 49]. The RF shunt capacitance of each of the varactors was extracted by fitting the RF results to the model shown in Fig. 7.5. Fig. 7.4a presents the measured reflection coefficient of a typical varactor following the geometry of Fig. 7.2b.

These measurements prove the almost ideal capacitive response of the varactor for the various bias voltages. The capacitance, however, does not vary smoothly with voltage, but it shows a deviation from the theoretically expected curve at bias voltages of 22–23 V. This intermediate discontinuity becomes more obvious in Fig. 7.4b where the extracted capacitance is plotted as a function of the bias voltage. Varactor C in this plot is the varactor whose results are shown in Fig. 7.4a, while the three other curves represent the extracted capacitances from three more varactors with similar geometries.

Fig. 7.4 clearly demonstrates that the tuning range for all varactors is between 160–213% and the maximum and minimum capacitance values do not vary more than 12% and 20% respectively. Table 7.1 summarizes these results and also provides the measured pull-in voltage and respective capacitance for each one of these varactors. This table shows that the maximum possible capacitance could not be achieved in an analog way. This was due to the residual stress in the lower beam that forced

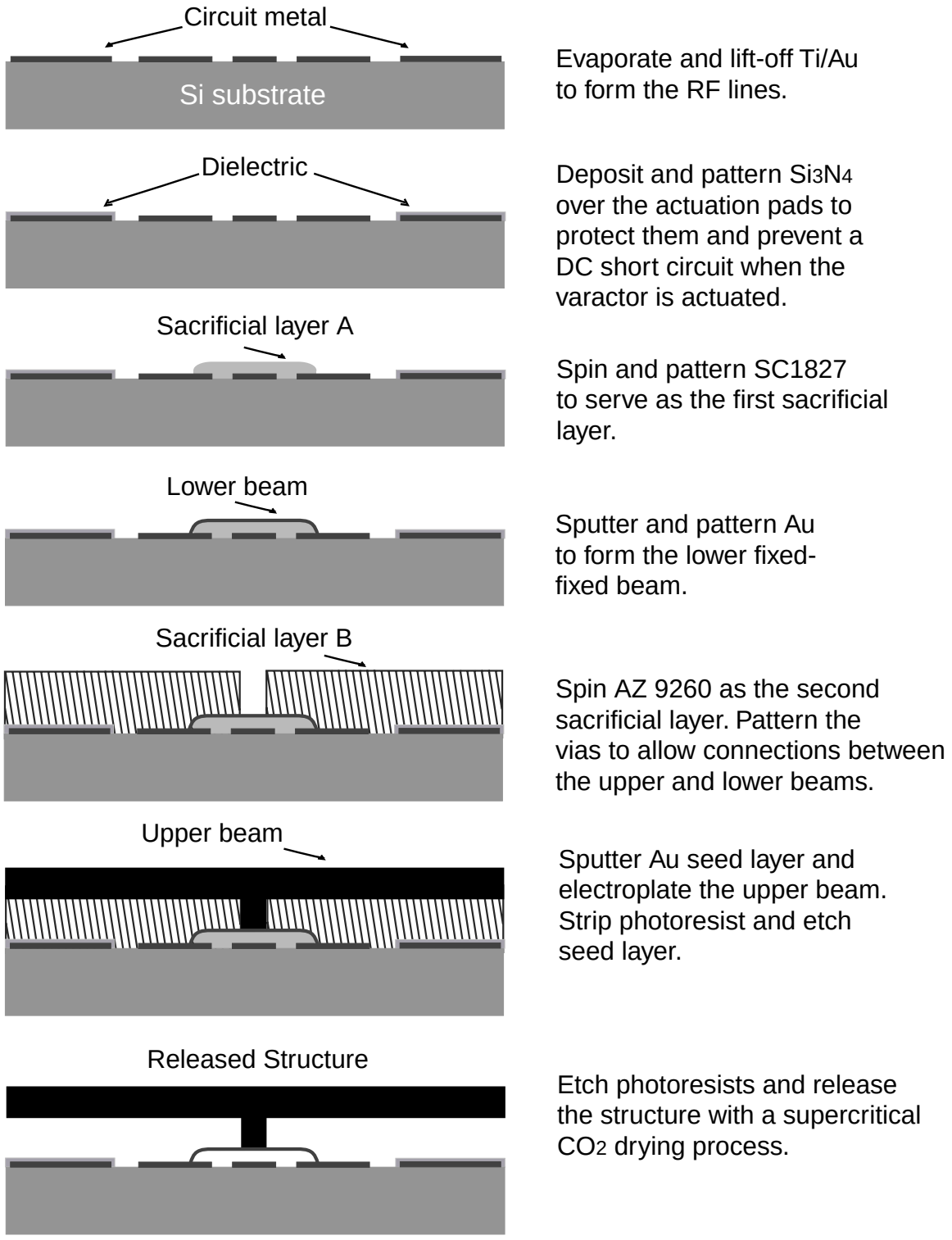


Figure 7.3: Process flow for the fabrication of the proposed MEMS varactor.

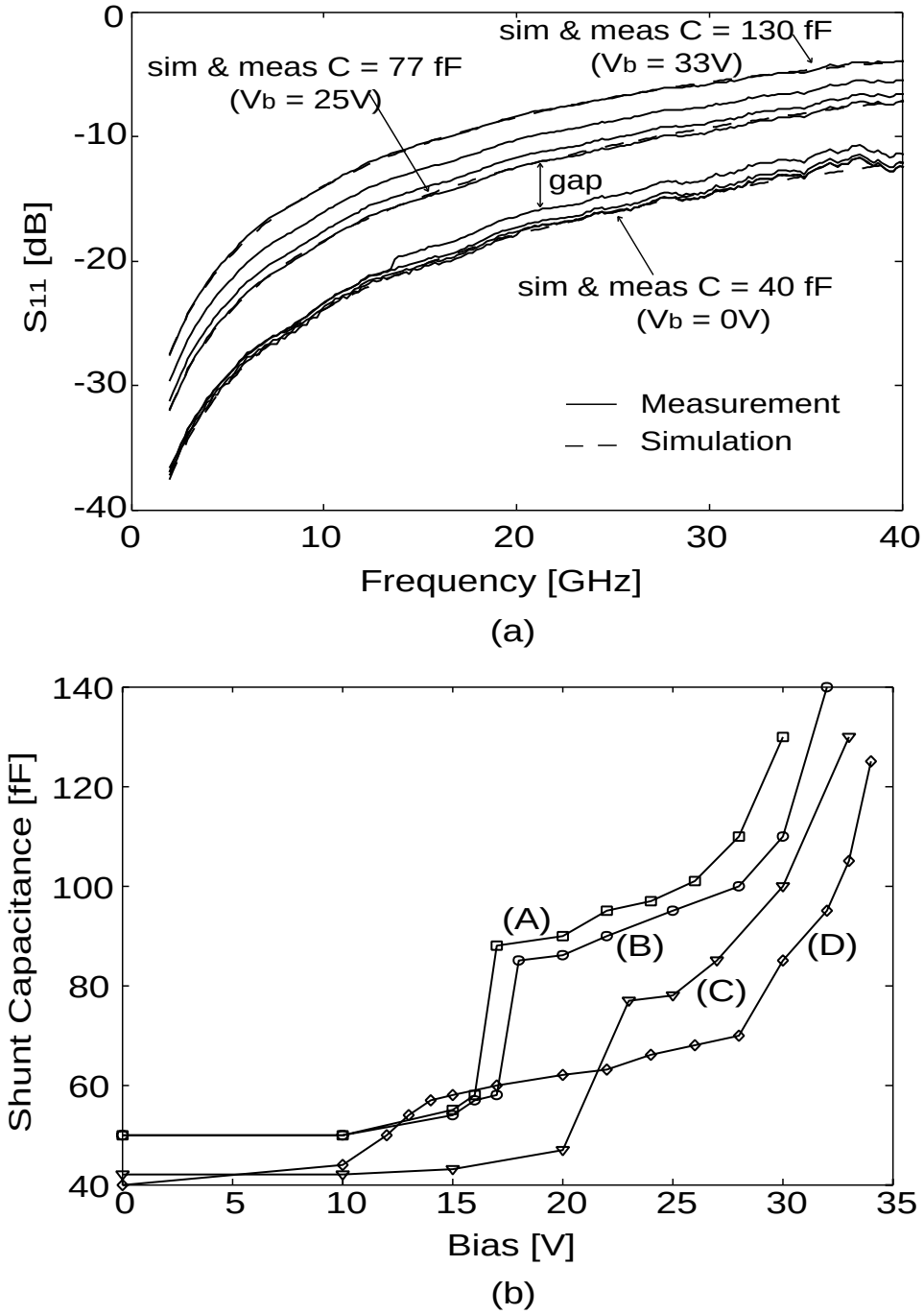
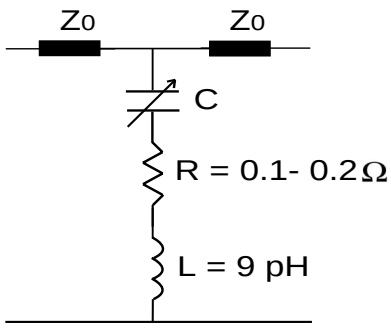


Figure 7.4: (a) Typical measured and simulated reflection coefficient of the varactor shown in Fig. 7.2b. (b) Shunt capacitance presented by several varactors as a function of the applied bias voltage. Varactor C is the varactor whose reflection measurements are shown in the first part of this figure. It is interesting to note the discontinuity for each varactor that occurs at different voltage levels.



(c)

Figure 7.5: Equivalent circuit used to extract the capacitance values vs. bias voltage.

Table 7.1: Summarized results for the varactors presented in Fig. 7.4.

Varactor	A	B	C	D
Min. measured cap. value (fF)	50	51	42	40
Max. measured cap. value (fF)	130	140	130	125
Pull-in voltage (V) (± 1 V)	31	33	34	34
Pull-in capacitance (fF)	270	265	230	240
Measured tuning range (%)	160	175	210	213

it to warp upwards and thus increase g_1, g_2, or equivalently decrease $(g_2 - g_1)/g_1$. It is worth noting, however, that although the maximum tuning range could not be achieved because of residual stress, the device still demonstrated a significantly improved tuning range compared to previous designs.

It is also worth noting that the intermediate discontinuity was observed for all varactors but at different voltage levels. Fig. 7.4b shows that the voltage level where this discontinuity is observed varies by about 50%. Due to this effect it will be very difficult to realize some capacitance values close to the discontinuity region. Varactor C, for instance, cannot easily provide the values from 47 to 77 fF. More studies need to be performed to explain this effect, but it is believed that it is due to residual compressive stress and the upward initial curling of the lower beam. As the biasing voltage is slowly increased, the device starts moving downwards, which increases the

compressive stress in the structure. As the compressive stress is increased, buckling of the structure occurs at some point. This abrupt movement of the device is observed as the discontinuity shown in Fig. 7.4. After buckling, the device's movement continues uninterrupted until pull-in occurs. Devices with tensile residual stress would not experience this problem.

The measurements presented in Fig. 7.4 were performed by slowly increasing the biasing voltage from 0 V to a value slightly less than the pull-in voltage. The reverse measurements were performed by decreasing the voltage from its maximum value to 0 V. Fig. 7.6 shows an example of such a measurement. This figure shows that a hysteresis loop exists in the operation of the varactor and that the observed intermediate discontinuity appears at different voltage levels in the forward and backward biasing schemes. This hysteresis loop is repeatable and very similar for all the varactors of Fig. 7.4. Section 7.5 discusses this in more detail. Although more investigation is necessary to explain this hysteresis loop, we believe that it is a direct result of the existence of the intermediate discontinuity.

7.4.2 FFLB Tuning Range

The measurements presented in the previous subsection were repeated for the FFLB varactors. The results were in general similar, but the achieved tuning range was higher and reached nearly 300%. This improved tuning range was due to the fact that the fixed-fixed lower beam did not significantly deflect due to the process residual stress as it was the case for the FSLB designs. As a result, the lower beam could move almost the total distance of $g_1 = 2$ μm without collapsing due to the pull-in effect of the upper beam. In order to verify this, we did not include any dielectric layer between the lower beam and the center conductor of the cpw for the FFLB design. As a result, if the voltage was increased past the pull-in voltage, a direct metal contact would be observed and a low contact resistance would be recorded.

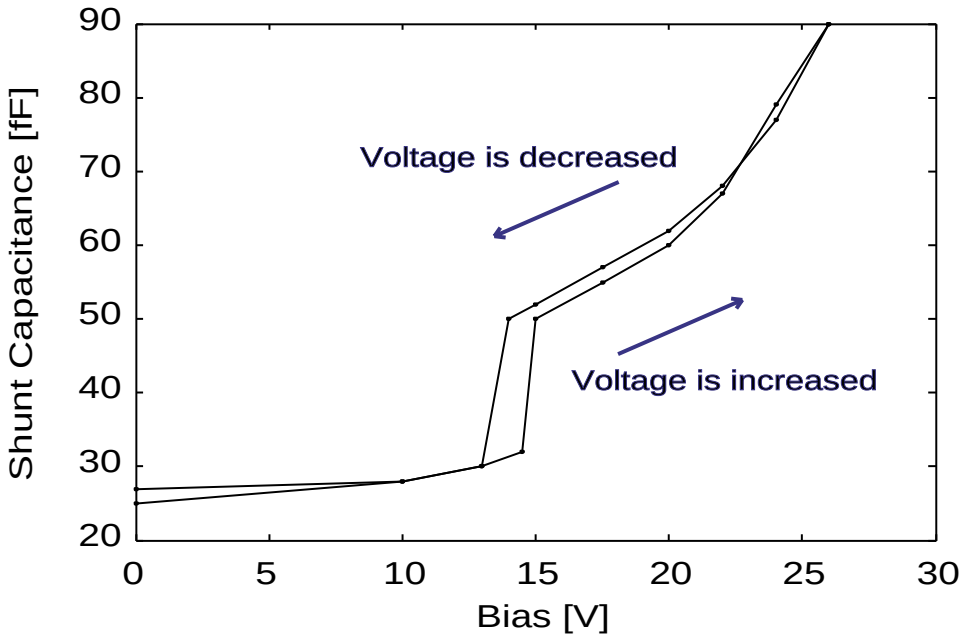


Figure 7.6: Hysteresis loop for a varactor when the bias voltage is increased from zero to a value close to the pull-in voltage and is subsequently decreased back to zero.

Fig. 7.7a presents the reflection coefficient measurements for a typical varactor of the geometry shown in Fig. 7.2c. The measurements demonstrate that the lower beam does not contact the center conductor of the cpw line even with a voltage of 22.5 V. However, when the voltage is increased to 22.8 V, a weak metal contact occurs, as the measured reflection coefficient at this biasing voltage indicates. The extracted capacitance values (except for $V_b = 22.8$ V) are presented in Fig. 7.7b. Based on the parallel plate model approximation, and these capacitance values, the gap between the lower beam and the center conductor at 22.5 V is approximately 0.36 μm. The fact that the upper beam does not collapse before the lower beam touches the cpw center conductor is also proven by the fact that the contact resistance can be precisely controlled by the bias voltage as shown in [72].

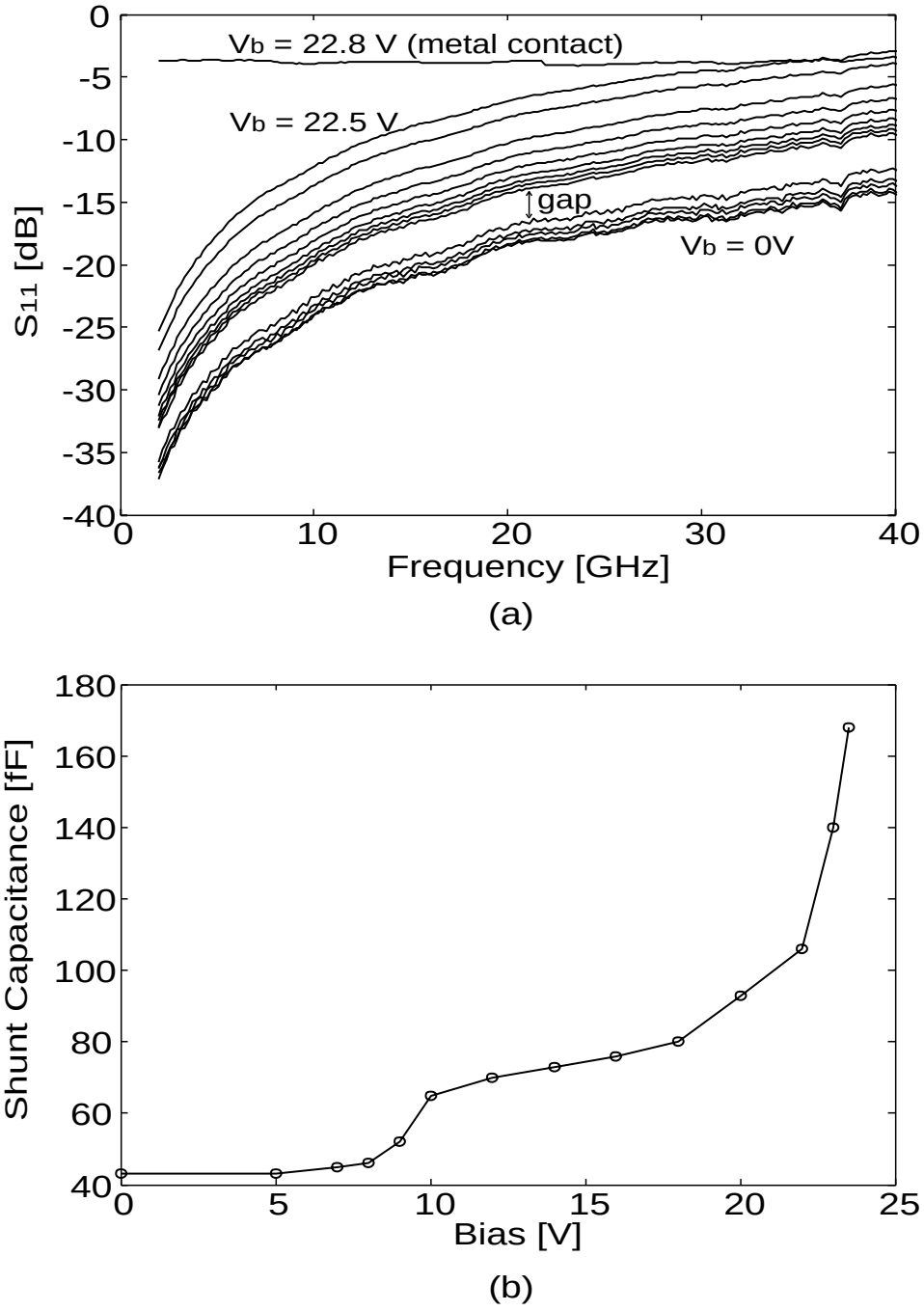


Figure 7.7: (a) Typical measured reflection coefficient of the varactor showed in Fig. 7.2c. (b) Extracted shunt capacitance of the MEMS varactor as a function of the applied bias voltage. The tuning range of this capacitor is nearly 300%. Although the intermediate discontinuity is present in this varactor too, its effect is in general milder than the ones under the FSLB design.

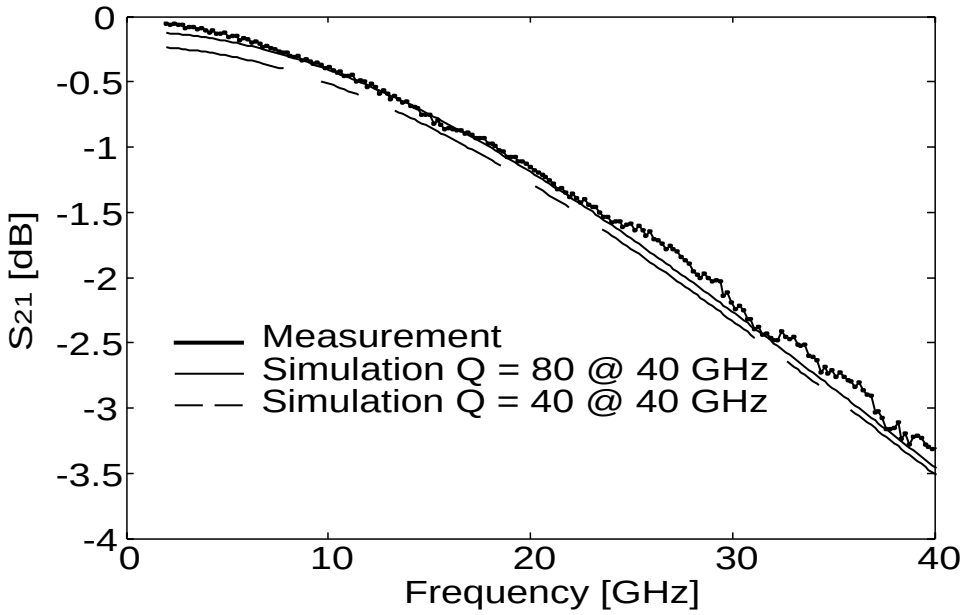


Figure 7.8: Measured and simulated insertion loss of the varactor showed in Fig. 7.2c for $C = 168$ fF. The simulations were performed for various quality factors and two examples are presented in this Figure. These simulations indicate that the quality factor is at least 80 at 40 GHz.

7.4.3 Resonant Frequency and Quality Factor

The resonant frequency of both FSLB and FFLB designs are very high and are dominated by the highest capacitance value and the parasitic inductance of the designs. The parasitic inductance depends on the springs of the lower beam and is in the order of 10 pH for both designs [72]. Consequently the resonant frequency of these varactors is very high (> 100 GHz) and could not be determined by the measurement techniques presented in this work.

The quality factor of these devices is also very high and is dominated by the resistive losses of the cpw line and the lower beam. Fig. 7.8 shows the insertion loss of a FFLB varactor with 168 fF capacitance and the simulated insertion loss for various quality factors at 40 GHz. This figure demonstrates that the quality factor is higher than 80 at 40 GHz.

7.5 Hysteresis Experimental Characterization

It is interesting to see how the hysteresis loop shown in Fig. 7.6 varies over time. In this characterization, the varactor was driven by a 100 Hz bipolar square wave. The measurements were performed under low RF input power (10 mW) and the varactor capacitance value was extracted from the recorded return loss. The test was performed in a regular laboratory environment.

During the first few hundreds of cycles, the varactor under test (VUT) was following exactly the same hysteresis loop. However, after a few thousand cycles, we observed a tendency of the hysteresis loop to shift towards lower voltages. This trend has been recorded for both branches of the hysteresis loop. Figs. 7.9 and 7.10 present the measured results for the forward (varactor moves downwards) and return (varactor moves upwards) branches respectively. Both branches show similar trends. In particular, after 30,000 cycles, the intermediate discontinuity recorded in the forward branch shifted from 15 to 13.5 V, while this shift was also measured to be 1.5 V (from 14 to 12.5 V) for the return branch. After cycling the varactor for an additional 170,000 cycles, we recorded a further shift of 1 and 0.7 V for the forward and return branches respectively. The test was continued until a total of 6 million cycles. As Figs. 7.9 and 7.10 show, the hysteresis loop again shifted slightly to lower voltages. Based on these measured performance, it can be also seen that the varactor spring constant is reduced with cycling. For example, Figs. 7.9b and 7.10b show that the varactor's capacitance values at a specific voltage (20 V for instance) is increased with cycling. In other words, a higher deflection is achieved for the same applied voltage. The varactor was still operational after this cycling. The presented results are typical among several tested varactors.

Although more studies are necessary for a quantitative characterization of these results, a qualitative explanation can be based on the phenomenon of creep. Whereas creep is often observed, it is not widely reported in the literature. However, it is

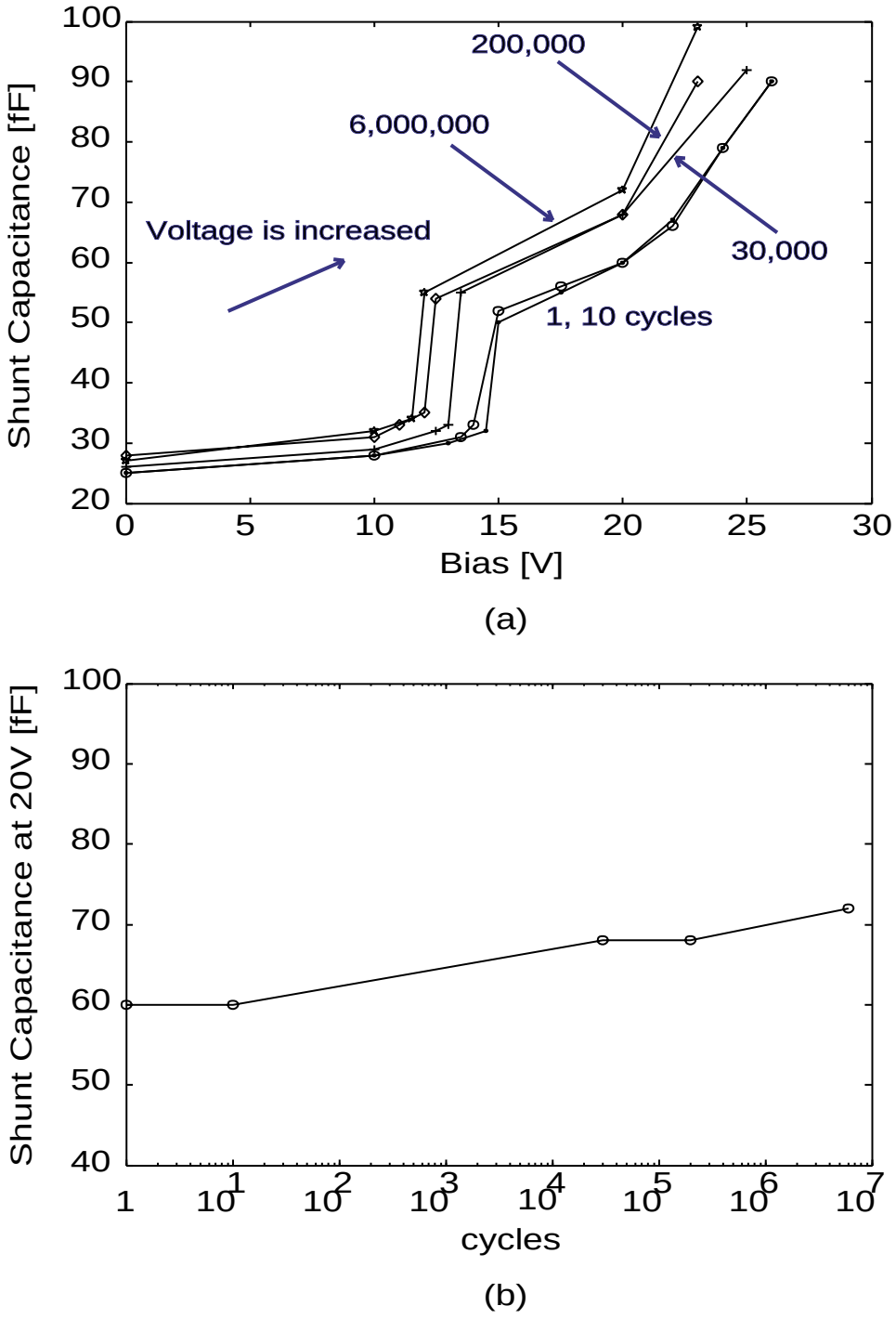


Figure 7.9: (a) Measured forward (varactor moves downwards) branch of a typical varactor hysteresis loop up to 6 million cycles. (b) Measured varactor capacitance at 20 V recorded in the downward movement.

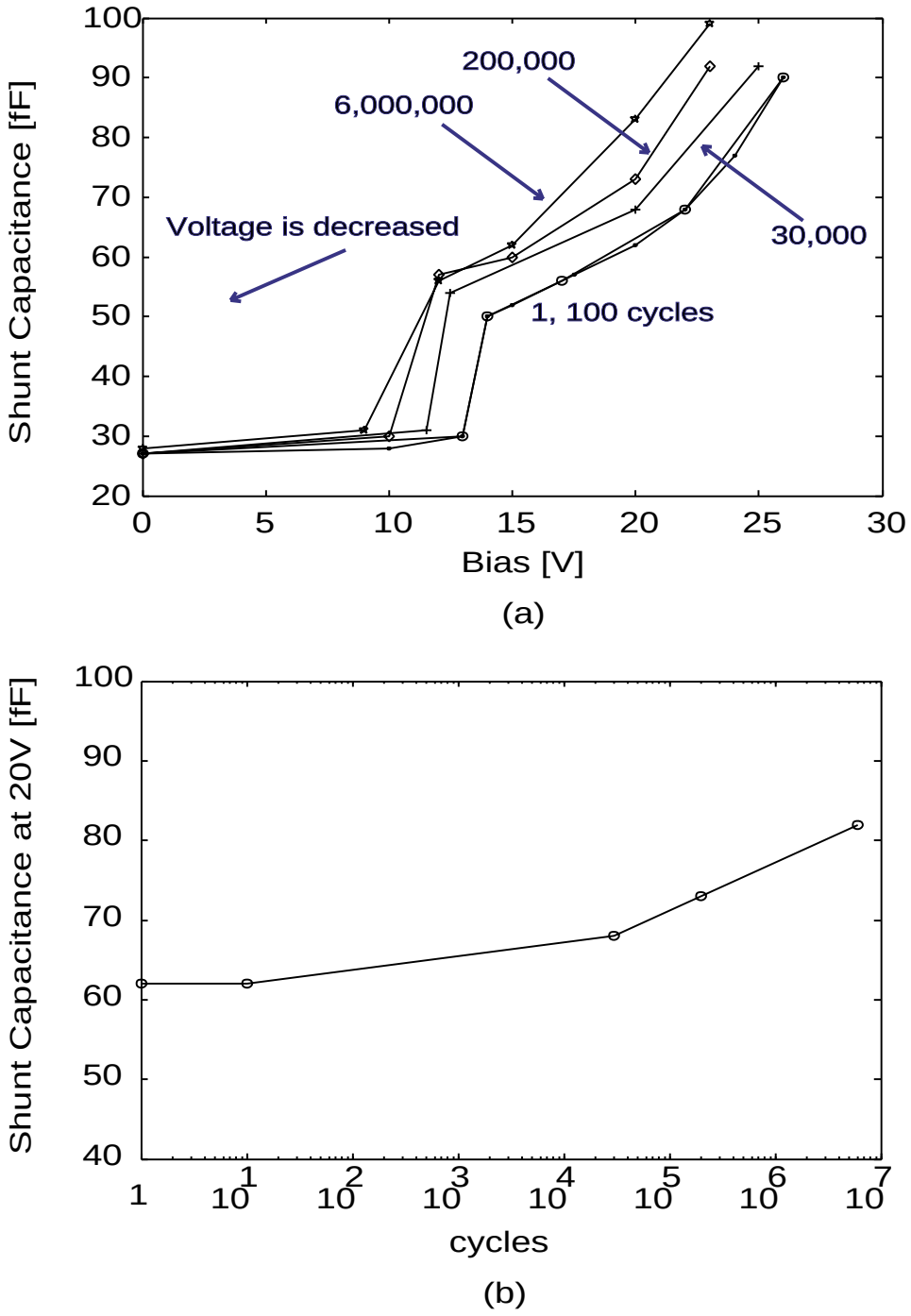


Figure 7.10: (a) Measured return (varactor moves upwards) branch of a typical varactor hysteresis loop up to 6 million cycles. (b) Measured varactor capacitance at 20 V recorded in the upward movement.

known as memory effect in micromirrors [73] and it has been also observed in thin metal plated cantilevers [6]. More specifically, Vickers-Kirby et al. [6] developed an

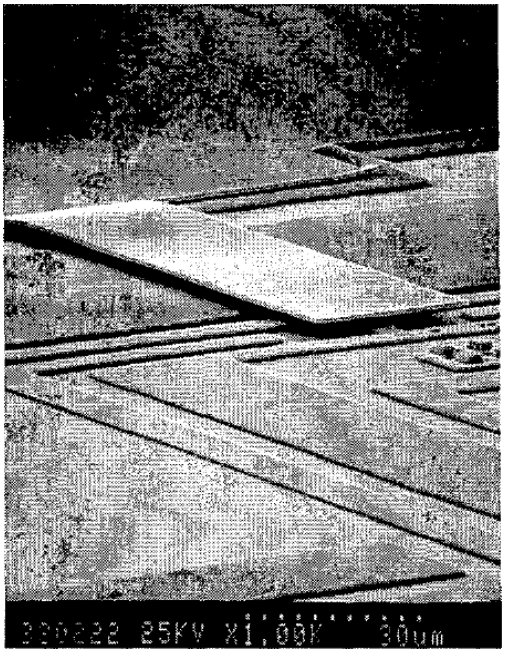
apparatus to experimentally characterize over time the voltage required for a constant deflection of MEMS cantilevers. A number of different materials were studied and it was found that Au was the softest and most sensitive material to creep. Fig. 7.11 presents the obtained results for 100-μm long cantilevers [6]. The observed creep behavior can be attributed to defect hoping, dislocation motion and grain boundary sliding that are caused by mechanical stress. Since creep is of mechanical origin, harder materials are less sensitive to creep. Si was the hardest material in this study and Si devices showed the least voltage drop over time (< 0.4 V). On the other hand, Au was the softest material and exhibited the greatest voltage drop (almost 5 V).

The behavior of our structure can be also explained on the basis of creep of a different kind. Creep is not necessarily associated only with constant deflections, but may be also developed in a structure during cycling even at room temperature [74]. As it has been observed in other structures, residual stress can be partially relieved by creep or plastic strain [74]. Since the spring constant of our varactor is dominated by stress, any relief of the stress in the structure will reduce the spring constant of the varactor and equivalently the required pull-in voltage. This is indeed observed in our varactors made of Au (see Figs. 7.9 and 7.10). This issue can be alleviated by using harder metals (e.g. Ni) for the lower beam of the varactor and by reducing the residual stress.

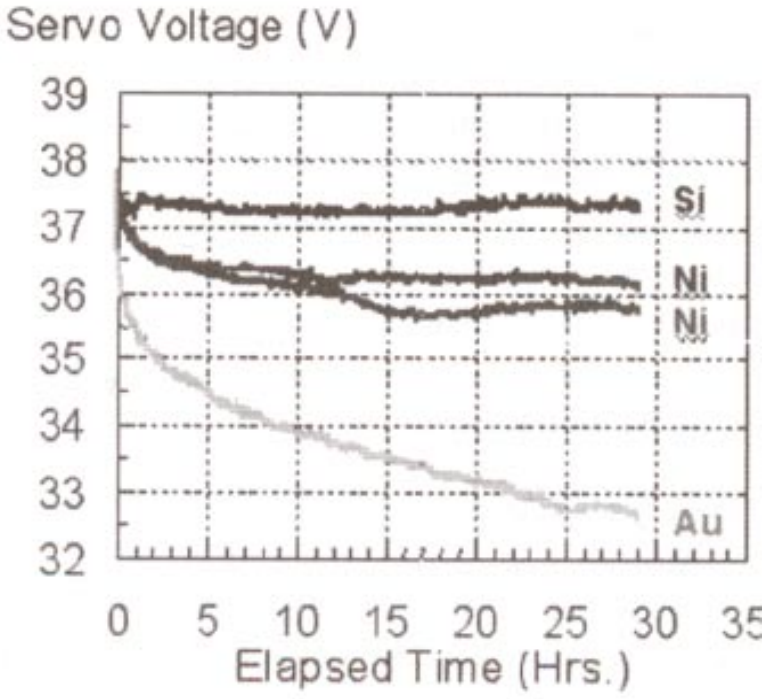
7.6 Conclusions

In this chapter we have presented a novel analog MEMS varactor design with a capacitance tuning ratio of 4:1 or 300%. The capacitance value is electronically controlled by a bias voltage in the range of 20–34 V. These MEMS varactors also show the additional advantages of resonant frequency and quality factor in excess of 100 GHz (for $C = 168$ fF) and 80 at 40 GHz respectively. We have also characterized

these varactors over time and show that creep reduces the required biasing voltage by about 15% over 6 million cycles.



(a)



(b)

Figure 7.11: (a) SEM picture of an electroplated nickel MEMS tunneling accelerometer used in [6] to characterize the required bias voltage to sustain a certain beam deflection over time. (b) Long term bias stability versus time for different cantilever materials in air (after [6]).

CHAPTER 8

Tunable Slot Antenna

8.1 Introduction

IN the previous chapters we have considered a variety for architectures for switches and tunable circuits. MEMS, however, can be also particularly beneficial for tunable antennas since with the ever-increasing demand for reliable wireless communications, the need for efficient use of electromagnetic spectrum is on the rise. In modern wireless systems spread spectrum signals are used to suppress the harmful effects of the interference from other users who share the same channel (bandwidth) in a multiple-access communication system and the self-interference due to multipath propagation. Also spread spectrum signals are used for securing the message in the presence of unintended listeners and alleviating the effects of communication jammers. One common feature of spread spectrum signals is their relatively high bandwidth. This is specifically true for frequency-hopped spread spectrum communications system. In a frequency-hopped spread spectrum system a relatively large number of contiguous frequency slots spread over a relatively wide bandwidth are used to transmit intervals of the information signal. The selection of the frequency slots for each signal interval is according to a pseudo-random pattern known to the receiver.

Signal propagation over large distances and in urban and forested environment can take place at UHF and lower frequencies. At these frequencies, the size of broadband and efficient antennas is considerable. Techniques used to make the antenna size small, usually renders narrow-band antennas. To make miniature size antennas compatible for a frequency-hopped spread spectrum system, we may consider a reconfigurable narrow-band antenna that follows the pseudo-random pattern of the frequency-hopped modulation. In this chapter the design aspects of compact, planar, and reconfigurable antennas are considered and the feasibility of such designs is demonstrated by constructing and testing a planar reconfigurable slot antenna operating at UHF.

Compared to broadband antennas, reconfigurable antennas offer the following advantages: 1) compact size, 2) similar radiation pattern and gain for all designed frequency bands, and 3) frequency selectivity useful for reducing the adverse effects of co-site interference and jamming.

In recent years, reconfigurable antennas have received significant attention for their applications in communications, electronic surveillance and countermeasures by adapting their properties to achieve selectivity in frequency, bandwidth, polarization and gain. In particular, preliminary studies have been carried out to demonstrate electronic tunability for different antenna structures [75-85]. It has been shown that the operating frequency or bandwidth of resonant antennas can be varied when a tuning mechanism is introduced. Several interesting approaches are presented by Sengupta [75, 76] and Guney [77]. In the literature, tuning is accomplished using varactor diodes [78, 79], or by the application of electrically [80] and magnetically tunable substrates [81, 82] with the use of barium strontium titanate (BST) and ferrite materials respectively.

Tuning of printed dipole or slot antennas has also been considered since they share the same advantages of portability, low profile and compatibility in integration

with other monolithic microwave integrated circuits (MMICs). Kawasaki and Itoh [83] presented a 1 λ slot tunable antenna loaded with reactive FET components. Although the radiation pattern properties were preserved in all resonant frequencies, the tuning range of the resulting antenna was very limited. Second-resonance cross slot antennas were also presented by Forman et. al. [84] in a mixer/phase detector system. A varactor diode was used in the microstrip feed-line and the resonance could be electronically tuned over a 10% bandwidth. The bandwidth was increased to 45% when mechanical tuning was used by varying the feed-line length. Dipole tunable antennas were proposed by Roscoe et. al. [85] where printed dipoles in series with PIN diodes were studied. The dipole length was varied from $\lambda/2$ to 1λ depending on whether the diodes were off or on. The operating frequencies were selected from 5.2 to 5.8 GHz, while matching of only 4–5 dB was achieved.

The slot antenna proposed in this chapter utilizes shunt switches that effectively change its electrical length over a very wide bandwidth. To demonstrate the technique a reconfigurable slot antenna capable of operating at four different resonant frequencies over a bandwidth of 1.7:1 is designed and tested. Measurements of the return loss indicate that excellent impedance match can be obtained for all selected resonant frequencies. No especial matching network is used and the matching properties are solely determined by the placement of the switches. The loading effect of the PIN diodes in the antenna is also characterized by a full wave analysis and transmission line theory and comparisons between the real and ideal switches are also studied. Per design goals, it is demonstrated that the reconfigurable slot antenna has the same radiation pattern at all frequencies. Also, the measured radiation patterns agree with the theoretical ones. The polarization characteristics and the efficiency behavior of the antenna as a function of frequency are investigated using both theoretical and experimental data. Finally, some design guidelines are provided and possible design improvements are discussed.

The strict requirements of a constant input impedance, gain, radiation pattern and polarization can only be met, if both the passive structure and the tuning mechanism are carefully designed and effectively integrated into the final design. Therefore, these issues are discussed separately. Section 8.2 focuses on the passive antenna structure and its properties. The switching mechanism, its loading effect on the antenna and the final reconfigurable antenna are discussed in Section 8.3. Finally, the measured results are presented in section 8.4.

8.2 Passive Antenna Design

The antenna size at UHF and lower becomes critical and therefore special consideration is required. A compact planar geometry is best suited since three-dimensional large and bulky structures are in general undesirable, especially for military applications. Furthermore, some miniaturization techniques have been applied to reduce the size. This section focuses on the passive slot antenna design issues emanating from the above principles.

First, the miniaturization capabilities provided by a high dielectric constant substrate were investigated. Inasmuch as an accurate characterization of its effect is needed, a commercially available moment method code [55] was employed. First, simple slot antennas were simulated at 600 MHz and their resonant lengths were determined as a function of the substrate thickness and dielectric constant (Fig. 8.1). This analysis suggests that even at low frequencies where the substrate is very thin compared to the wavelength, a miniaturization factor of about 2:1 is possible, if a high dielectric constant substrate is employed. However, the standard commercially available substrates are electrically thin at UHF and below and therefore the 2:1 factor seems to be a limit difficult to exceed even for substrate permittivities as high as 10.

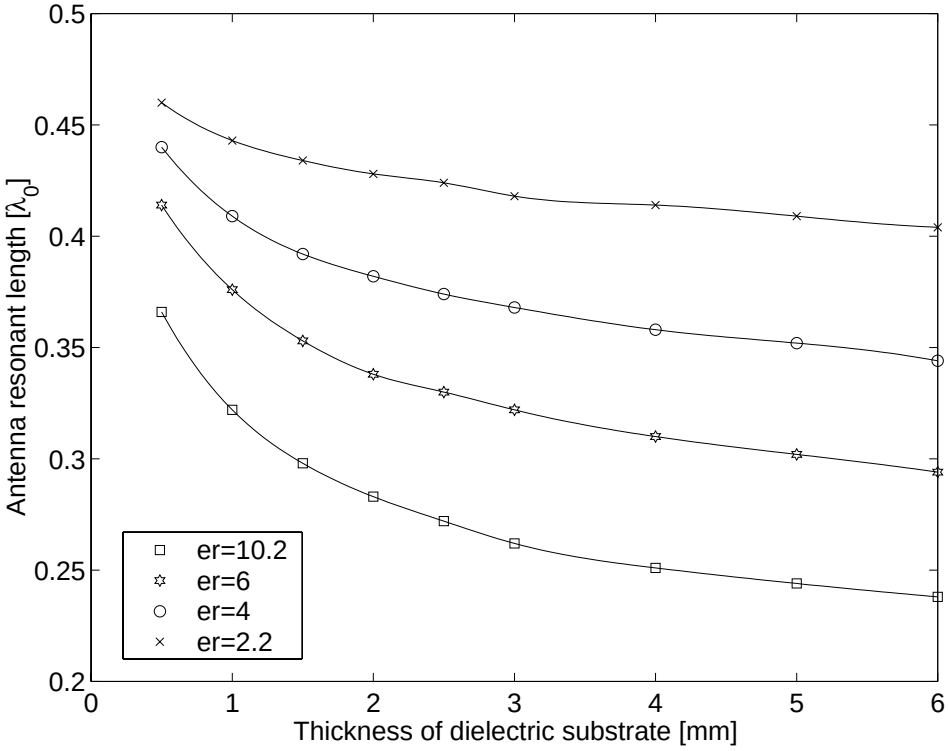


Figure 8.1: Resonant length at 600 MHz for straight slot antenna (in free-space wavelength) as a function of substrate thickness and dielectric constant.

In an effort to further decrease the total area occupied by the antenna, the slot configuration was altered from its standard straight form to an S-shape. From the simulated equivalent magnetic current distribution on the straight and S-shape slots (Fig. 8.2, antennas (a) and (b)), it is obvious that they both closely follow a sinusoidal pattern with the maximum current concentrated in the middle of the slot. As a result, the two antennas share very similar properties and they only differ in their polarization orientation. Antenna (a) is horizontally polarized, while antenna (b) slant linear polarized. Other more complicated geometrical shapes can also be used, but the S-shape slot does not contain any segments supporting opposing currents, which would considerably deteriorate the radiation efficiency. It should also be mentioned that, although the total area of the antenna is greatly reduced by this geometrical change, the resonant length remains almost unchanged. For example, a resonant length of

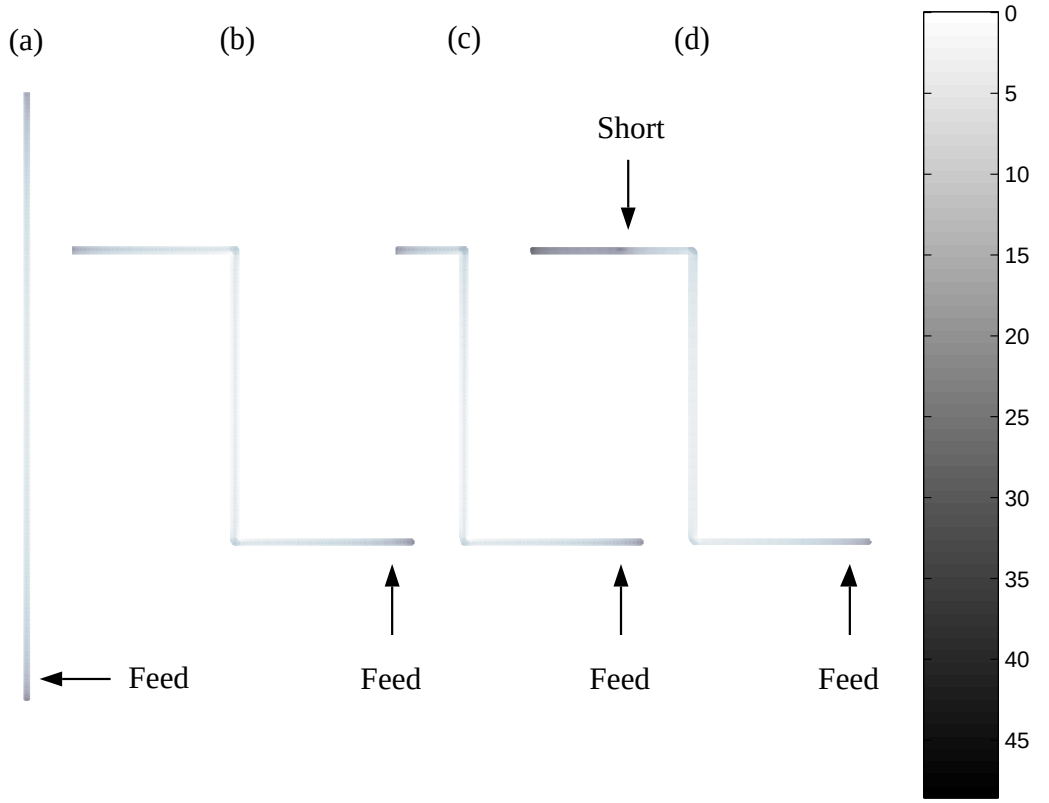
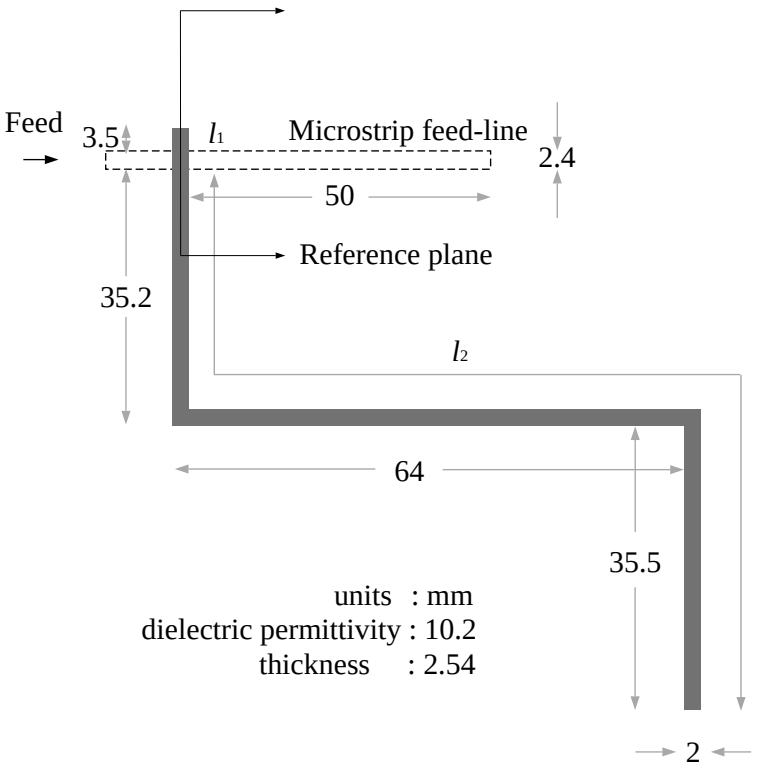


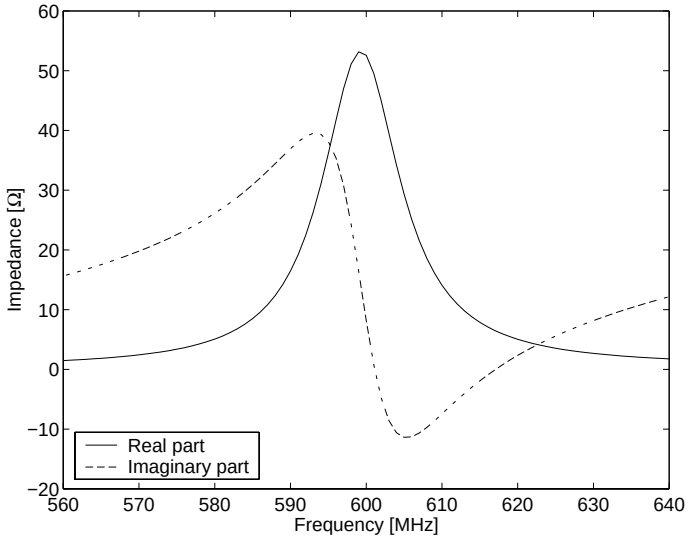
Figure 8.2: Computed magnetic current distribution on (a) 600 MHz straight slot antenna, (b) 600 MHz S-shape slot antenna, (c) 700 MHz S-slot, and (d) 600 MHz S-slot with a short-circuit 21 mm above its bottom edge.

136 mm for a straight slot is slightly increased to 139 mm for S-slot at 600 MHz for a substrate with $\epsilon_r = 10.2$ and thickness of 2.54 mm.

The standard microstrip feed for the simple slot can also be used for the S-shape slot. Fig. 8.3a shows the slot antenna with its feed-line, while Fig. 8.3b presents the input impedance at the feeding point as a function of frequency. To achieve a good match to a 50 Ω line, the microstrip feed-line has to be moved close to one end of the slot antenna. This implies that the antenna input impedance is not very sensitive to small changes in the length of the longer segment (l_2, see Fig. 8.3a). This property will greatly simplify the design of the tunable slot and its feeding network and will result in minimum complexity and maximum reliability for the final antenna. More



(a)



(b)

Figure 8.3: (a) S-slot antenna with microstrip feed-line and (b) the real and imaginary parts of the input impedance as a function of frequency.

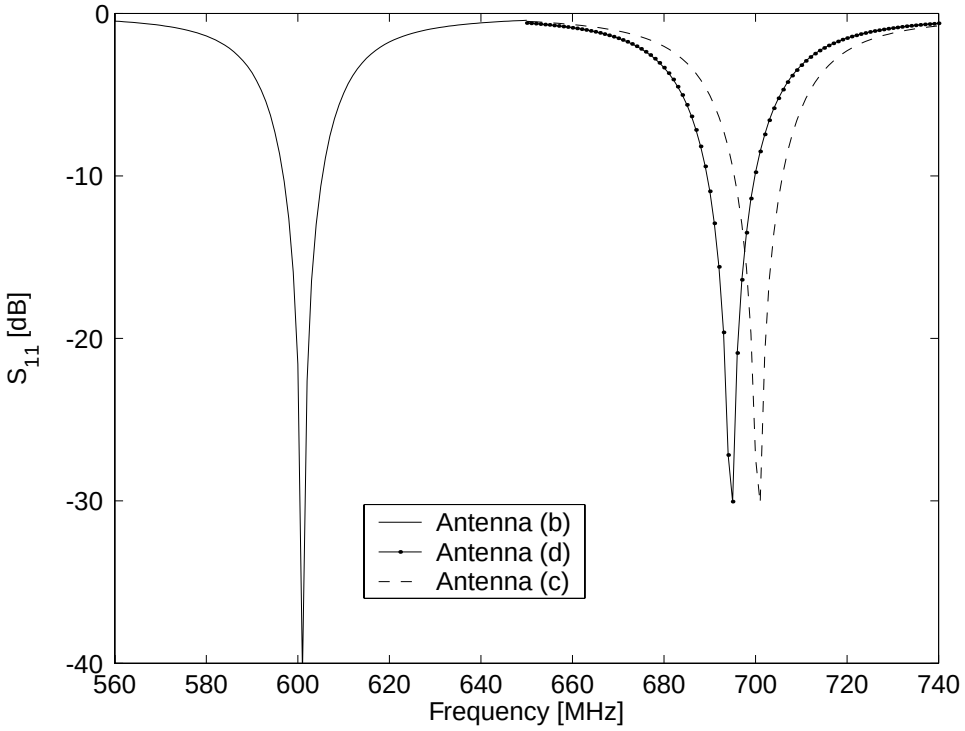


Figure 8.4: Simulated results for the return loss of the S-shape slot antennas presented in Fig. 8.2.

details on this issue can be found in Section 8.3. This property of the slot antenna makes it an attractive choice as a reconfigurable structure, since most other antennas (such as dipoles) would require a specially designed matching network.

The resonant frequency of the above structure can be tuned by changing the electrical length of the slot. This may be readily accomplished by introducing a short circuit at a specific location. Then the slot will appear to be shorter and therefore the antenna will resonate at a higher frequency. The three S-shape slots in Fig. 8.2 demonstrate these concepts. Slot antenna (b) resonates at 600 MHz with a resonant length of 139 mm. Antenna (c) is 21 mm shorter and is designed to resonate at 700 MHz. Finally, antenna (d) is obtained by modifying (b). In particular, antenna (b) is short circuited at 21 mm above its lower end. The simulated return losses for these three slots are shown in Fig. 8.4. It is also important to note that the microstrip feed-line remains unchanged in all three cases. That is, the distance between the top

end of the slot and the feed line cross point remains constant and is equal to 3.2 mm. This means that, although the resonant frequency is shifted by 100 MHz, very good matching is achieved for both (c) and (d) slot antennas without the need for modifying the feeding network. In addition, slot antennas (c) and (d) have almost identical resonant frequencies. The small difference in the resonant frequency comes from the fact that antenna (d) appears somewhat electrically longer than (c) due to the parasitic effects of the short circuit. Therefore, tunability is possible by introducing these short circuits with no special matching network. Although Fig. 8.2 illustrates the basic concept of reconfigurability on a dual band antenna, it is obvious that it can be extended to antennas with several bands of operation. The number of these bands depends on the number of switches on the antenna. For example, a four band antenna is presented in Section 8.3.3 and it is demonstrated that the resonant frequency can be digitally controlled by an array of four switches.

8.3 Modeling and Design of Active Antennas

In the previous section we presented the basic principle of controlling the antenna resonant frequency. It was also shown that even when a perfect short circuit is used, the parasitic effects of the short can slightly affect the antenna performance and particularly the resonant frequency. The parasitic effects become worse when a switch with finite isolation is used. This section addresses the issues related to the design of a suitable solid state switch and on the characterization of its effects on the antenna performance. Finally, the complete reconfigurable antenna design is presented at the end of the section together with its theoretical performance.

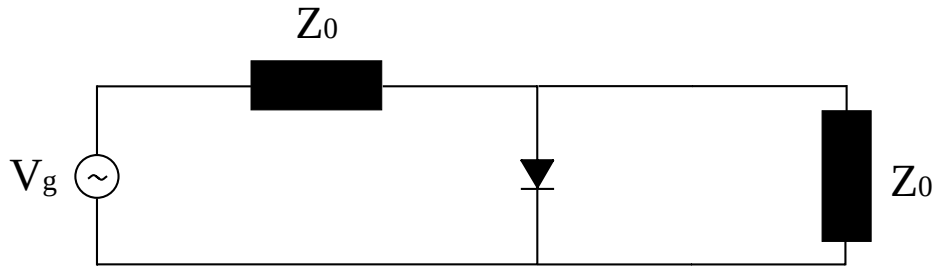
8.3.1 Switch Design

To implement the electronic reconfigurability, the ideal shunt switches must be replaced with PIN diodes. This antenna was intended for usage in an open uncontrolled environment. Therefore, PIN diode's reliability and high switching speed made it most appropriate for the application at hand. Packaged RF MEMS switches, however, could also be used without changing any of the design principles presented in this chapter. The RF equivalent circuit of the diode is shown in Fig. 8.5b for both the on and off states. The reactive components C_p and L_p model the packaging effect, while the others come from the electric properties of the diode junction in the on and off positions [86]. Typical values are also given for the HSMP-3860 diode [87] used in this chapter. The computed isolation (defined as $1/|S_{21}|^2$) for the circuit shown in Fig. 8.5a is given by [87]:

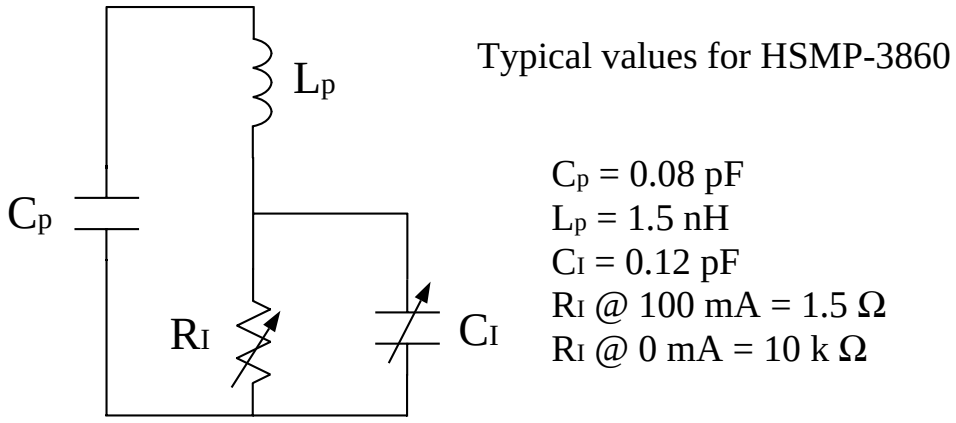
$$\alpha = 10 \log \left[\frac{\left(\frac{R_d Z_0}{R_d^2 + X_d^2} + 2 \right)^2 + \left(\frac{X_d Z_0}{R_d^2 + X_d^2} \right)^2}{4} \right] \tag{8.1}$$

where $Z_d = R_d + jX_d$ is the equivalent impedance of the diode and Z_0 is the characteristic impedance of the line. In the example considered here, the characteristic impedance of the line is approximately equal to 60 Ω, which is calculated by the moment method code [55] for a slotline with a width of 2 mm, a finite ground plane of 60 mm (on both sides of the slot) and a substrate permittivity $\epsilon_r = 10.2$ (RT/Duroid) [88].

The switch bias network is presented in Fig. 8.6. An inductor of 470 nH and three 10 pF capacitors are used to improve the RF-DC signal isolation. These values were chosen based on the bias network RF equivalent circuit shown in Fig. 8.6b. The simulated performance for the on and off states is presented in Fig. 8.6c. The RF-DC isolation is better than 30 dB for both states and the return loss is less than –20 dB



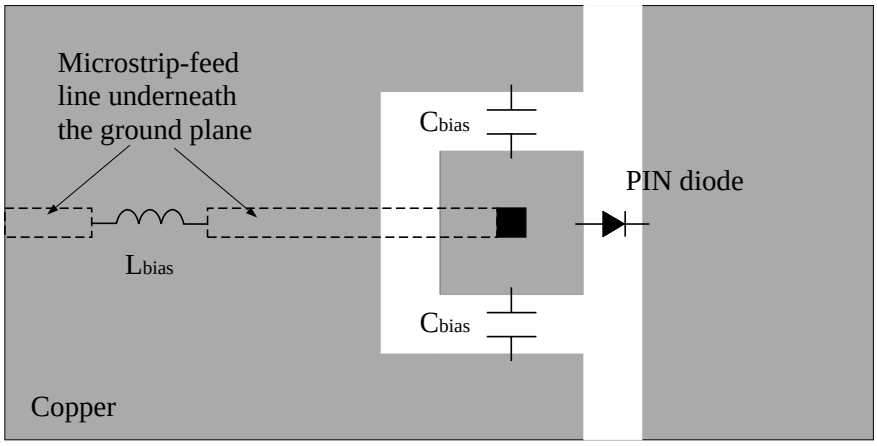
(a)



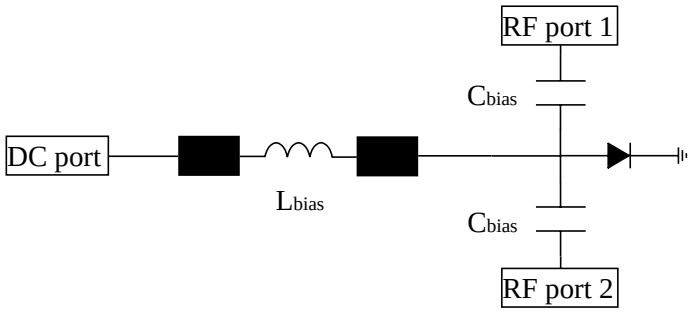
(b)

Figure 8.5: (a) PIN diode connected as a shunt switch in a transmission line. (b) RF equivalent circuit for PIN diode including packaging effects.

for the off state. Finally, the RF-RF isolation is greater than 16 dB for frequencies lower than 500 MHz and degrades to 11 dB at 1 GHz due to the diode parasitic elements.



(a)



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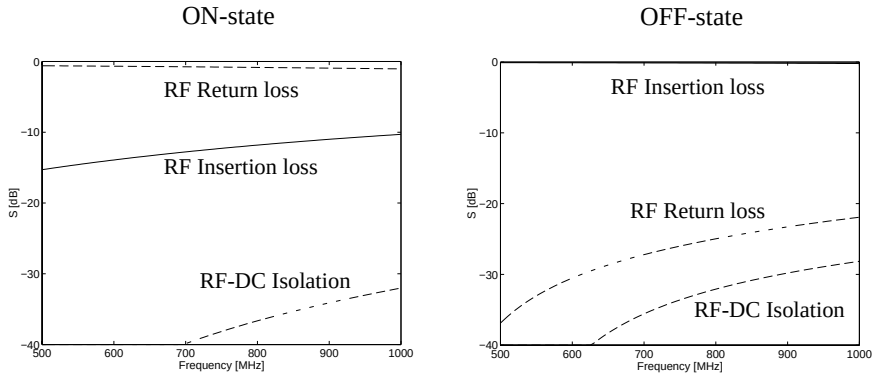


(c)

Figure 8.6: (a) Layout of switch biasing network. (b) RF equivalent circuit. (c) On and Off-state simulated RF performance

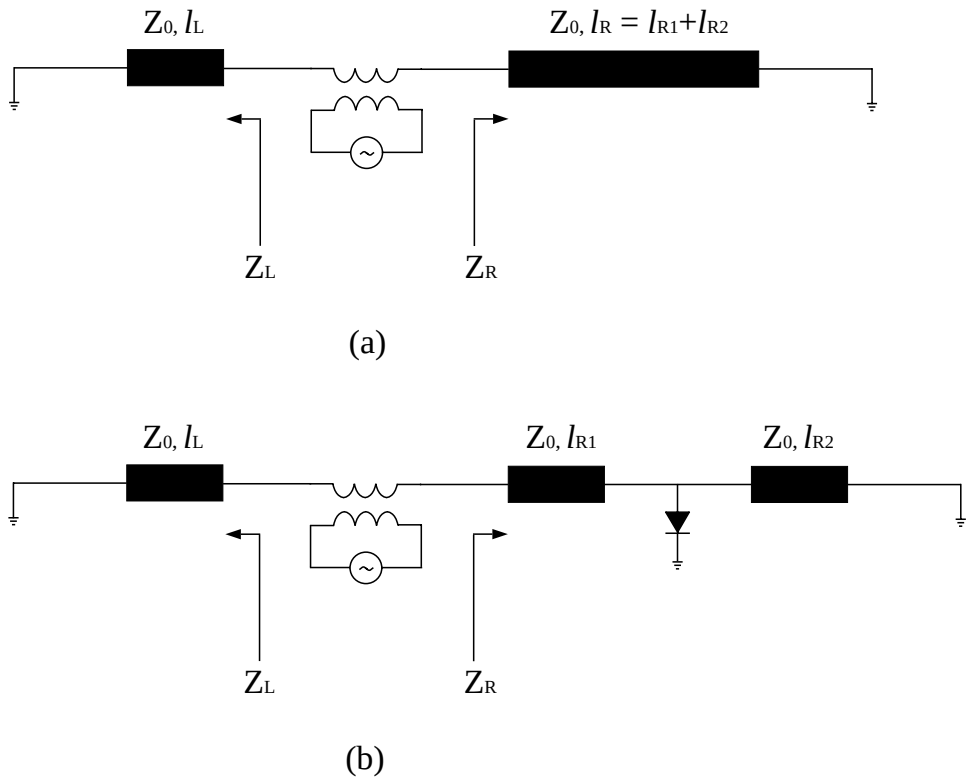


Figure 8.7: RF equivalent circuits for determining the resonant frequency of (a) unloaded and (b) loaded with a single switch slot antenna.

8.3.2 Switch loading on the Antenna

Although the switch isolation is important since it determines the frequency selectivity of the antenna, the switch loading on the antenna is equally important inasmuch as it affects its resonant frequency and input impedance. The loading effects must be taken into account for an accurate prediction of the antenna resonant frequency and input impedance, especially when more than one switch is used for multi-frequency operation.

A transmission line equivalent circuit that models the loading effect of one diode on the antenna is shown in Fig. 8.7. The transverse resonant technique [89] states that:

$$Z_R(z') + Z_L(z') = 0 \tag{8.2}$$

where $Z_R(z')$ and $Z_L(z')$ are the input impedances on the right and left of the reference point respectively. For the unloaded transmission line in Fig. 8.7a equation (8.2) simplifies to:

$$\tan(\beta l_L) + \tan(\beta l_R) = 0 \tag{8.3}$$

or

$$\beta(l_L + l_R) = n\frac{\pi}{2}, \quad n = 1, 2, 3\ldots \tag{8.4}$$

which is the well known formula for these resonant antennas. Now it is important to see what happens in the simplest case of having one switch on the antenna. Fig. 8.7b shows the equivalent circuit of a transmission line loaded with one switch in the off position. Equation (8.2) then becomes:

$$[Z_0\omega_R C - \cot(\beta l_{R2})][\tan(\beta l_L) + \tan(\beta l_{R1})] = 1 + \tan(\beta l_L)\tan(\beta l_{R1}) \tag{8.5}$$

Equation (8.5) can of course be solved numerically and an iterative method can be employed for finding the unknown lengths until the desired resonant frequency (f_R) has been achieved. A similar procedure can be followed if more than one switch is used on the slot, but the process becomes a little more complicated if all resonant frequencies are to be specified. We also need to note that equation (8.5) does not include any packaging effects, but these can be readily incorporated in the model, resulting in a more accurate computation.

Only the loading effects when the switch is in its off state have been discussed up to now. Nevertheless, the small on-state resistance also affects the antenna performance and particularly its input impedance. Full wave analysis was used to model these effects. For a first order approximation, the resistance was modeled as a thin film resistor on top of the slot and the packaging parasitic elements were neglected in this analysis. The parasitic element effects in the on-state can be important especially at the highest frequencies (see Fig. 8.6c). Fig. 8.8a shows the simulated geometry of an

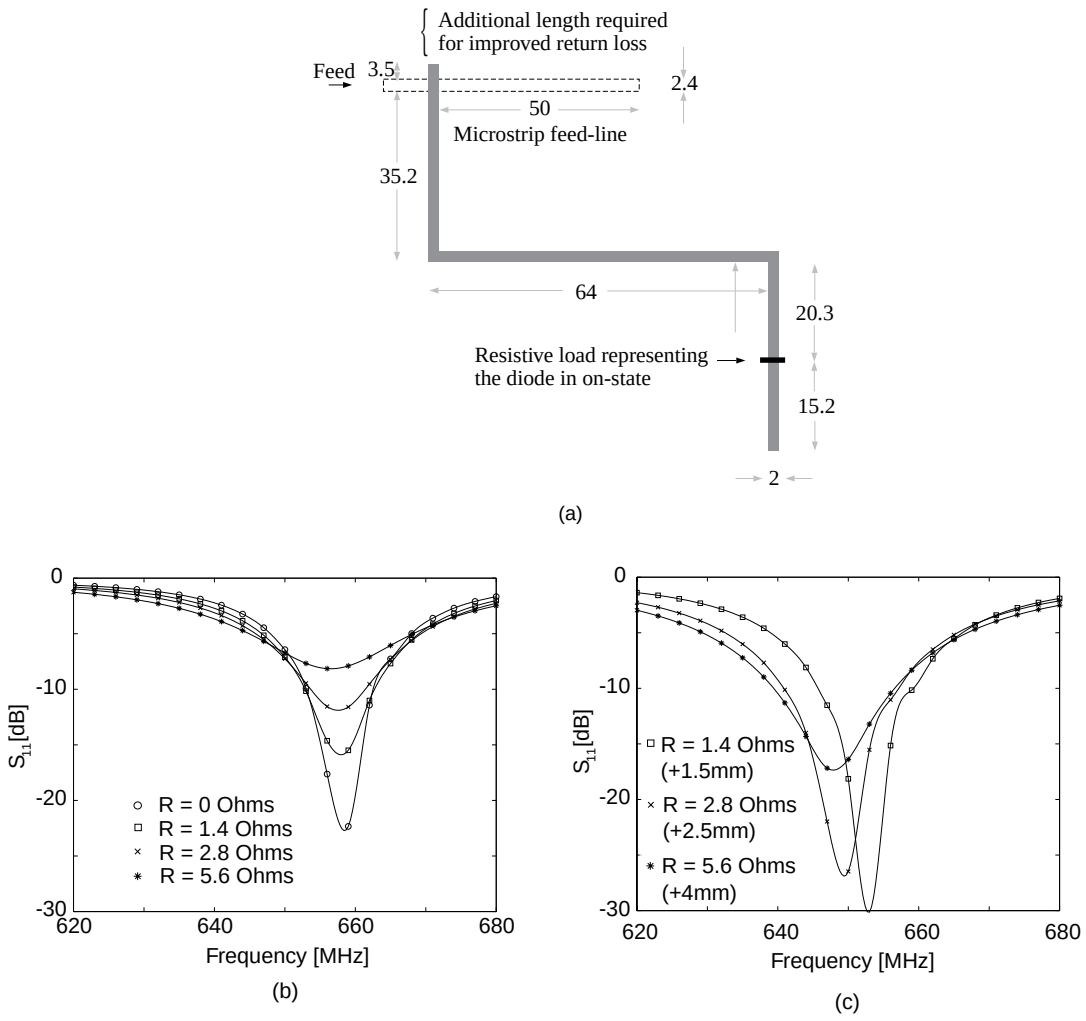


Figure 8.8: (a) Slot antenna with resistive load representing actuated switch (units are in mm). (b) Return loss for different values of switch resistance. (c) Improved return loss with minor adjustments (< 4 mm) in the slot length above the feeding point.

S-shape slot antenna loaded with a resistive film, which is fed by a microstrip line and Fig. 8.8b shows the simulated return loss versus the switch on-state resistance for four different cases between 0 to 5.6 Ω. In all four cases the position of the 50 Ω feed-line was kept unchanged. It is obvious that the matching level deteriorates rapidly as the resistance value increases, and for resistance values above 1.5 Ω the matching level becomes unacceptable.

However, this degradation can be avoided to some extent by elongating the upper

Table 8.1: Computed efficiency for slot antennas with a single switch versus on-state resistance value

R [Ω]	0	1.4	2.8	5.6
Efficiency [%]	71.8	55.6	45.6	33.9

end of the slot as the resistance is increased. Fig. 8.8c shows the improvement on the antenna matching when the slot length is adjusted. It is found that, in all three cases, only a very small line segment length needs to be added in order to improve the input impedance of the antenna. Even for a resistance value of 5.6 Ω the required line segment length is less than 3% of the total slot length, resulting in only a small change in the resonant frequency. This method of maintaining a good impedance match will be utilized later for the design of the reconfigurable antenna by placing additional switches (matching-switches) on the slot above the feed-line and synchronizing them together with the switches at the other end of the slot (frequency-switches). However, it should be noted that the matching switches will not represent perfect shorts and they will introduce an extra loading effect. Nonetheless, this effect is negligible and matching levels of better than –20 dB can be achieved, as will be seen next. Therefore, the matching properties of the reconfigurable antenna will solely depend on the position of an array of switches on the slot and no matching network will be necessary as frequency changes.

Having discussed the loading effects of the switches on the matching properties of the antenna, their effects on the radiation characteristics of the antenna need to be found as well. Ideally, the radiation efficiency should be that of the half-wavelength dipole, since the antenna behaves effectively as a $\lambda/2$ resonant slot at each of its operating frequencies. However, the on-state resistance of the switches will obviously result in power dissipation and finally degradation in the antenna efficiency. The dissipated power obviously depends on the diode's on-resistance and on the number of the switches on the antenna. Table 8.1 shows the computed efficiency for the

Table 8.2: Theoretically calculated resonant frequencies using full wave analysis and transmission line model

f_R [MHz] (TLN)[a]	f_R [MHz] (MM)[b]	Switch Configuration
542	561	4 = ON 1,2,3 = OFF
596	627	1,4 = ON 2,3 = OFF
688	711	2,4 = ON 1,3 = OFF
1002	950	3 = ON 1,2,4 = OFF

[a]Transmission Line Model
[b]Moment Method

antennas previously discussed in Fig. 8.8. Dielectric loss has been included in all cases. This explains the non-ideal efficiency when $R = 0\ \Omega$.

The above antenna efficiency analysis shows that even for a small series resistance of $R = 1.4\ \Omega$ the antenna gain will be approximately 2.5 dB lower than that of an ideal half-wavelength dipole. This is an inherent drawback of using PIN diode switches. However, micro-electro-mechanical (MEMS) switches are becoming increasingly important and are now a viable alternative as they offer very low power consumption and they come even in smaller packages. It has also be shown that capacitive type MEMS switches exhibit very low ohmic losses and therefore can be used for maximized antenna efficiency. However, the required on-capacitance values renders them impractical for UHF frequencies. Hence metal-to-metal contact switches, which have no cut-off frequency should be considered in such a design.

8.3.3 Final Reconfigurable Antenna Design and Properties

Based on the previously discussed design principles, a reconfigurable slot antenna design (shown in Fig. 8.9a) is presented here. Four switches are used in order to tune the antenna over a range of 540 to 900 MHz. Both full wave analysis and the transmission line model were used in the design process. In this design three

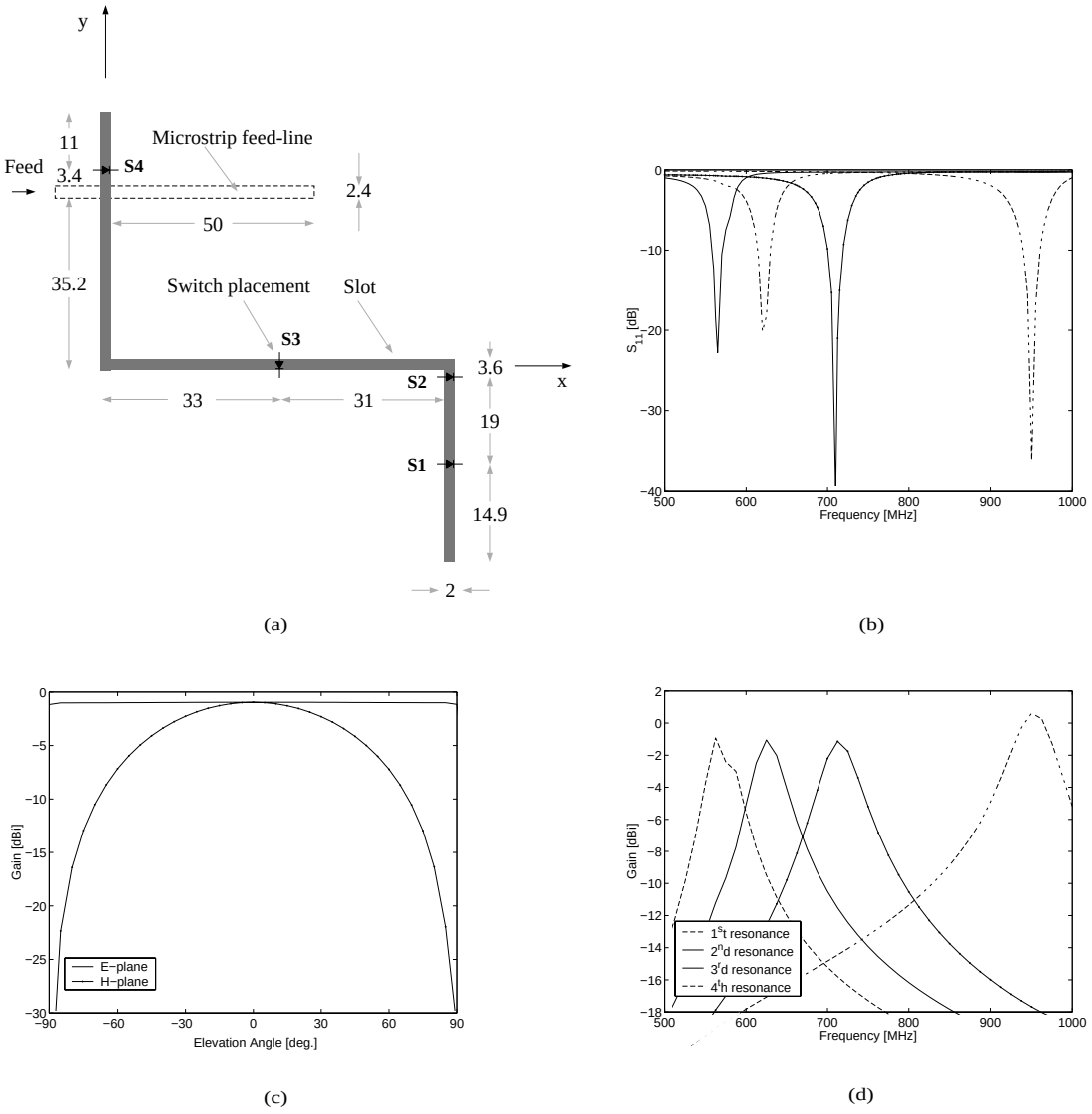


Figure 8.9: (a) Reconfigurable slot antenna (units are in mm) (b) Simulated return loss for the four resonant frequencies. (c) Typical radiation pattern. (d) Simulated gain the four resonant frequencies.

frequency-switches and a single matching-switch are used. Table 8.2 summarizes the calculated resonant frequencies and the conditions of all four switches for each resonant frequency. The transmission line model has the advantage of allowing fast and accurate (as will be proven later) computation of the resonant frequencies and can easily incorporate the diode parasitics. However, the full wave analysis is essential when an accurate prediction of the antenna input impedance is needed. In the moment

method code, the diodes were simulated as metal-insulator-metal (MIM) capacitors and as thin film resistors in the off and on states respectively and as a result the packaging parasitics were ignored. This explains the 5% differences observed in the computed resonances between the two models. Fig. 8.9b shows the calculated return loss where a matching level of better than –20 dB has been achieved for all the operating frequencies.

Since at every operating frequency the antenna radiates as a $\lambda/2$ slot, the radiation pattern remains unchanged when the frequency is shifted. The same holds for the antenna directivity. The E and H-planes of a typical calculated pattern are shown in Fig. 8.9c. Since the antenna has been designed on a electrically thin substrate (at UHF) the radiation pattern is symmetric on the two sides of the slot. However, the efficiency and the gain will be reduced compared to a half-wavelength dipole due to the resistive losses caused by the diodes. Fig. 8.9d shows the calculated gain using the moment method analysis [55]. The gain is approximately –1 dB for the lowest frequencies and increases to about 0.7 dB for the highest one. Similar results hold for the antenna efficiency.

The reference angle of 0° in the previous graphs represents the direction normal to the antenna ground plane. Although the S-shape pattern considerably reduces the antenna occupied area, it has the inherent drawback that the polarization does not remain constant as the frequency is changed. However, as Table 8.3 shows, the polarization does not change considerably (variation of about 30°). This is due to the fact that the antenna polarization (always slant linear) is dominated by the orientation of the middle segment of the slot where most radiated field is emanated from. Therefore, if the orientation of the receiving antenna does not follow that of the transmitter as the frequency is changed, a maximum polarization mismatch of 25% will be incurred. The orientation of linear polarization reported in Table 8.3 is with respect to the x-axis (see Fig. 8.9a).

Table 8.3: Calculated polarization for the reconfigurable antenna

f_R [MHz]	561	627	711	950
Angle (°)	60	70	60	40

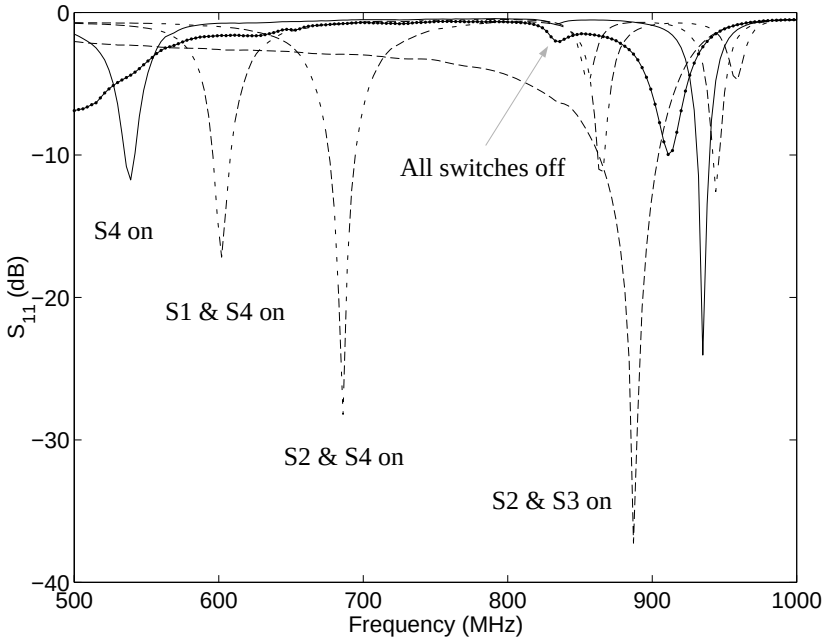


Figure 8.10: Measured resonant frequencies of the reconfigurable antenna.

8.4 Measurements and Discussion

The reconfigurable antenna designed in the previous section was fabricated on a 100 mil thick RT/Duroid substrate ($\epsilon_r = 10.2$). The size of the ground plane was 5×5 in^2.

The first task was to measure the resonances and an HP8753D vector network analyzer was used for the S-parameter measurements. The biasing voltage for the switches was provided by a DC voltage source. After calibrating the network analyzer the antenna return loss was measured when different combinations of the switches were activated. The measured data are presented in Fig. 8.10, where a return loss of

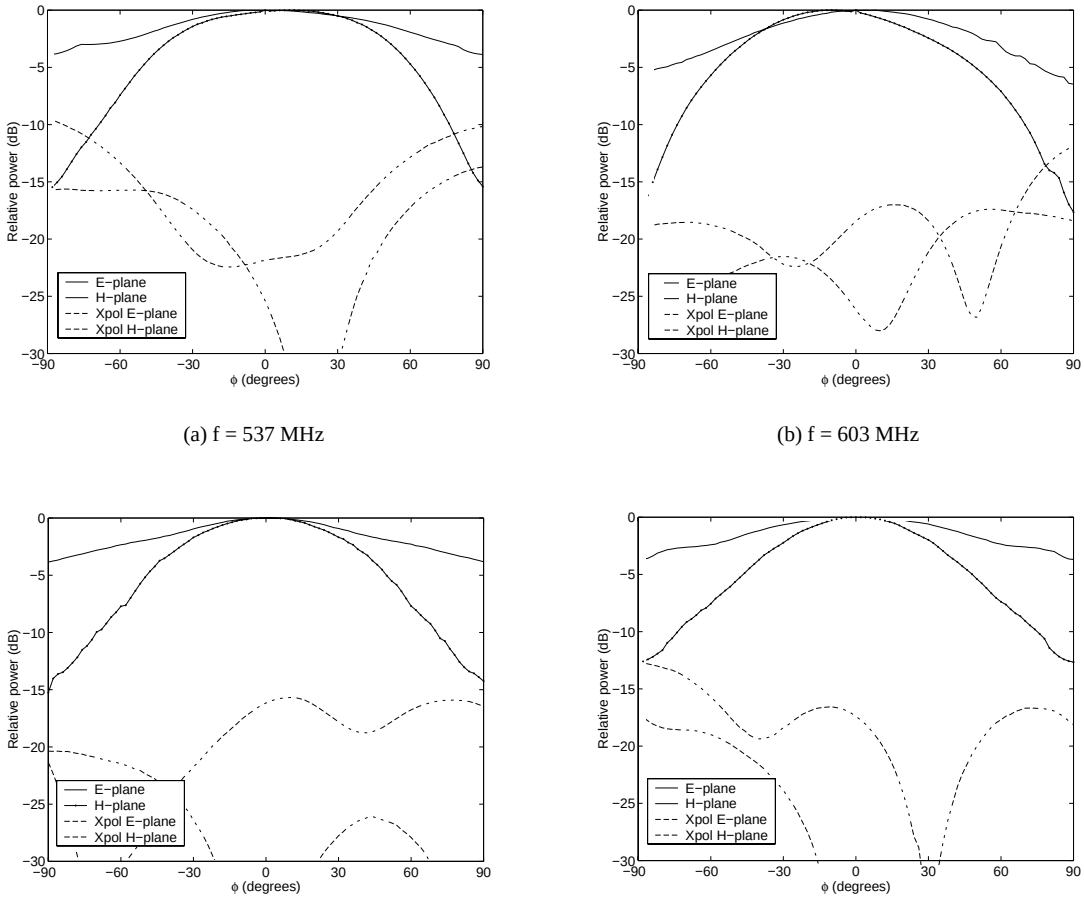
Table 8.4: Measured resonant frequencies and the necessary bias voltages for the switches

f_R [MHz]	Bias Voltage [V]			
	S1	S2	S3	S4
537	-20	-20	-20	1.1
603	1.1	-20	-20	1.1
684	0	1.1	-20	1.1
887	0	1.1	1.1	0.2

better than –13 dB is observed at all resonances. The measured resonances are shown in Table 8.4 together with the necessary biasing conditions. Satisfactory agreement between theoretical, Table 8.2, and experimental ,Table 8.4, data is observed. In addition, the transmission line model gives slightly better results — except the highest frequency — mainly because the parasitic reactive elements have been included in this model and not in the moment method technique. However, this is not true for the highest resonant frequency where an error of 13% exist between the transmission line model and the measurement. This discrepancy can be attributed to the fact that the properties of the diodes, and particularly the element values of its equivalent circuit, cannot be assumed constant up to 1 GHz.

A reverse voltage of –20 V was applied to maintain the switches in the off position and by doing so a better matching level was achieved. This is an important issue particularly when the antenna is used as the transmitter. Since the structure is a resonant structure strong electric fields are established that can turn the diodes on and off at the RF frequency and ruin the small signal design. This effect was clearly observed at the lowest resonance with an input power of 0 dBm. In this case an improvement of about 5 dB was achieved by changing 0 V bias to –20 V.

One more interesting effect was observed for the highest resonance. We noticed that better matching level would occur, if not only S3 but also S2 was forward biased. This is due to the relatively low isolation that each diode provides at these relatively



(a) f = 537 MHz

(b) f = 603 MHz

(c) f = 684 MHz

(d) f = 887 MHz

Figure 8.11: Measured radiation patterns for the four resonant frequencies

high frequencies (see Fig. 8.5c). Therefore, biasing S2 results in higher isolation and reduces the effect of leaked magnetic current in the area after the switch. The improvement in the return loss was approximately 10 dB compared to leaving S2 unbiased for this frequency.

Next, far field patterns were measured in the University of Michigan's anechoic chamber. The E and H-plane were measured as well as the corresponding cross-polarization for each operating frequency. An RF signal and a DC voltage source were used with the reconfigurable antenna and a dipole with adjustable length was employed as the receiving antenna. The dipole length was appropriately adjusted for

each operating frequency of the transmitting antenna until maximum received power was recorded. In order to find the E-plane, the transmitting antenna was rotated until the electric field was vertically polarized. Then the transmitter, placed on a turn table, was azimuthally rotated for measuring E-plane cuts. The cross-polarized pattern was measured by rotating the receiver antenna by 90°. H-plane pattern measurements were conducted in a similar manner.

Although for slot antennas printed on a substrate it is expected that the radiated power be higher in the half-space that include the dielectric substrate, no appreciable difference was observed experimentally. This is easily explained since in this case the dielectric thickness is about $\lambda/200$ at 600 MHz and the size of the ground plane is small (approximately $\lambda/3$) at the same frequency. Therefore the antenna is almost bi-directional and equivalent to a dipole in free space.

The measured data are presented in Fig. 8.11 for each resonant frequency. In these plots 0° denote the direction of maximum radiated power. These measurements show that the H-plane closely follows the expected sinusoidal pattern. However, some slight asymmetries near ±90° exist for almost all frequencies. These discrepancies originate primarily from two sources. First, parasitic radiation from the cables and the feeding network and second, radiation from the edges of the dielectric. These sources of radiation also affected the E-plane pattern measurements and they caused a difference of 3–4 dB between the minimum and maximum measured value. (see Fig. 8.11). Despite these discrepancies, it is clear that the far-field pattern remains unchanged versus the frequency tuning.

Gain measurements are accomplished using the comparison method [90]. A log-periodic antenna with 6 dBi gain at 600 MHz was used as a reference antenna for these measurements. The second resonance at 593 MHz was chosen as the operating frequency of the reconfigurable antenna, so that to make direct comparisons with the reference antenna possible. To measure the gain, the power received by the receiver

Table 8.5: Measured polarization for the reconfigurable antenna

f_R [MHz]	537	603	684	887
Angle (°)	57	70	55	33

dipole at 593 MHz was recorded when both the reference and the reconfigurable antennas were used in the transmitting mode inside the anechoic chamber under the same conditions. The measured gain was found –1.1 dBi, which corresponds to an efficiency of 47%. These results closely resemble the calculated data. It should also be pointed out that the gain of the slot antenna is reduced not only from the forward-biased diode resistance, but also from the small ground plane size. However, a comparison between the measured and calculated data reveals that the dominant degrading factor in gain is the dissipated power on the diodes rather the ground plane size.

Finally, the antenna polarization was measured and the method previously described for the pattern measurement was employed. The measured polarization orientation at each frequency is provided in Table 8.5. As discussed before, although the polarization does not remain absolutely constant as the frequency is changed, the variation range is small and comparable to the theoretical data (see Table 8.3).

8.5 Conclusions

A novel method for designing affordable, compact, reconfigurable antennas is proposed in this chapter. This method relies on changing the effective length of a resonant slot antenna by controlling combinations of electronic RF switches. Theoretical results for significant antenna parameters were validated experimentally. Important issues involved in the design of such antennas and guidelines were also discussed. Based on the proposed method, a compact planar reconfigurable slot antenna was

designed, fabricated and measured and a tuning range of 1.7:1 in the operating frequency was demonstrated. Although such a broad range was achieved, no matching network was required for the antenna. Another salient feature of this design, backed by theory and experiments, is that the radiation characteristics of this antenna remain essentially unaffected by the frequency tuning. The design procedure is general enough and allows even wider tuning ranges to be achieved. By employing suitable switches it can be also readily extended to higher frequency commercial and military applications.

CHAPTER 9

Future Directions

9.1 Thesis Summary

MICROMACHINING and RF Micro-Electro-Mechanical Systems (RF MEMS) have been identified as two of the most significant enabling technologies in developing miniaturized low-cost communications systems and sensor networks. The key components in these MEMS-based architectures are the RF MEMS switches and varactors. The first part of this thesis has focused on three novel RF MEMS components with state-of-the-art performance. In particular, a broadband 6 V capacitive MEMS switch is presented with insertion loss of only 0.04 and 0.17 dB at 10 and 40 GHz respectively. Special consideration has been given to particularly challenging issues, such as residual stress, planarity, power handling capability and switching speed. The need for switches operating below 1 GHz has been also identified and a spring-loaded metal-to-metal contact switch has been developed. The measured on-state contact resistance and off-state series capacitance are 0.5 Ω and 10 fF respectively for this switch. An analog millimeter-wave variable capacitor is the third MEMS component presented in this thesis. This variable capacitor shows an ultra high measured tuning range of nearly 4:1, which is the highest reported value for the millimeter-wave region.

The second part of this work has primarily concentrated on MEMS-based reconfigurable systems and their potential to revolutionize the design of future RF/microwave multifunctional systems. High-isolation switches and switch packets with isolations of more than 60 dB have been designed and implemented. Furthermore, lowpass and bandpass tunable filters with 3:1 and 2:1 tuning ratios respectively have been demonstrated. Similar techniques have been also applied to the field of slot antennas and a novel design technique for compact reconfigurable antennas has been developed. We have demonstrated that the key advantage of these antennas is that they essentially preserve their impedance, radiation pattern, polarization, gain and efficiency for all operating frequencies.

9.2 Contributions

A number of unique contributions have been made during this work. These can be summarized as follows:

- **Chapter 2:** Challenging issues in the implementation of ultra low-voltage have been successfully addressed. A significant portion of our effort has been focused on developing techniques that alleviate the adverse stress effects of residual stress. For example, we have experimentally proved that (appropriately characterized) sputtering may result in significantly less residual stress than evaporation. Furthermore, we have derived analytical formulas that aid the static and dynamic analysis of these switches. These formulas agree well with experimental data.
- **Chapter 3:** The power handling capabilities of the Chapter 2 low-voltage switch have been characterized. Simple but accurate analytical models that agree very well with the measured switch response under three scenarios have been developed. In particular we have presented theoretical and experimental

data (the experiments have been performed by Sergio Pacheco) for the three most significant cases: 1) self-actuation due to high RF power, 2) stiction due to high RF power, and 3) top-electrode pull-up voltage, which is particularly necessary for low-spring constant switches.

- **Chapter 4:** High-isolation single switches have been presented. We have demonstrated that slight modifications of the switch geometry can significantly affect the maximum switch isolation and bandwidth. Switches with 25–30 dB of isolation have been demonstrated and the trade-offs between bandwidth and maximum isolation have been also explored. These techniques have been extended to very high-isolation switch packets with measured isolation of nearly 70 dB. The performance of these networks is only limited by the substrate surface waves. The systematic study of these switch packets is supported by ample measured results that provide significant insight on the practically achieved bandwidth, loss and isolation characteristics.
- **Chapter 5:** Novel tunable lumped components have been successfully developed. In particular, we have demonstrated the capability of realizing compact tunable lumped shunt capacitors, series and shunt inductors. The values of these components are digitally controlled and tuning ranges as high as 3:1 have been presented. We have also discussed the integration of these components into tunable filters. For example, a Chebyshev low-pass filter with a tuning ratio of 3:1 has been implemented. Furthermore, to the best of the author's knowledge, a new bandpass filter topology has been proposed. This topology has been specifically derived for MEMS-based implementation and maximum reconfigurability (2:1 tuning ratio has been measured).
- **Chapter 6:** A novel spring-loaded DC-contact series switch has been designed, fabricated and characterized. We have successfully demonstrated that stress-induced forces between Au contacting surfaces yield low contact resistance and

low insertion loss of better than 0.2 dB up to 40 GHz. Several switches have been tested and the extracted on-state contact resistance and off-state series capacitance have been on average 0.5 Ω and 10 fF respectively. The on-state contact resistance is approximately half of what has been reported in the literature, while the off-state series capacitance compares well to the best reported values.

- **Chapter 7:** An ultra high-tuning range millimeter-wave analog MEMS variable capacitor has been developed. This component is based on continuous tuning of the gap between two parallel plates. Two different designs have been demonstrated with a maximum measured tuning range of 4:1. To the best of the author's knowledge, this is the highest reported capacitance range in the millimeter-wave region. The parasitic series inductance is only 9 pH and the quality factor is higher than 80 at 40 GHz. Furthermore we have characterized the operation of this device over millions of cycles of operation in a regular laboratory environment.
- **Chapter 8:** A novel design technique for compact broadband tunable slot antennas has been proposed. This method has been validated by fabricating and measuring a UHF reconfigurable antenna. The operating frequency of the antenna is tuned between four bands from 580 to almost 900 MHz. The key advantage of this method is that contrary to the already developed reconfigurable antennas, the input impedance, radiation pattern, gain, efficiency and polarization remain essentially unaffected by the tuning of the operating frequency. These properties make the antenna an ideal candidate for low-profile, low-cost and low-size commercial and military systems.

9.3 Future Directions

The RF performance of MEMS devices has been adequately analyzed by several researchers. It has also been demonstrated that a number of applications (antenna arrays, filters, phase shifters, matching networks, etc.) could benefit enormously from RF MEMS's low-loss, high linearity and low power requirements. Nevertheless, RF MEMS are still not available commercially, because some of the topics associated with their development have not been adequately addressed yet. The most important of these topis are reliability, packaging and modeling.

9.3.1 Reliability

Although some studies have been already initiated towards characterizing and improving RF MEMS reliability, there is still a lot of work that needs to be done in this area. The reliability of capacitive switches, for instance, is known to be limited by dielectric charging [17], but the exact mechanisms are not understood well. Additionally, handling of medium to high RF power has not been completely characterized yet. Similarly, metal-to-metal contact switches are currently limited to low power levels because of welding and stiction. The contact resistance of these type of switches degrades over time because of damage in the contact area. Research in materials suitable to be used in these applications needs to be aggressively pursued in the next coming years in order to reach reliability levels that will allow operation in excess of 100 billion cycles under medium RF power. It is also important to realize that a fairly limited family of structures has been investigated so far and that there is room for innovative structures that may eventually help in achieving this kind of performance.

9.3.2 Packaging

It is widely known that RF MEMS are very sensitive to humidity and contaminants. A humidity level as low as 20%, for example, is sufficient to lead to stiction, particularly in capacitive switches where a relatively large contact area is necessary. Additionally, the contact resistance of metal-to-metal contact switches depends heavily on the cleanliness of the contact areas. It is very important, consequently, to operate RF MEMS devices in an ultra clean environment. Today, however, it is not clear what environment is best for these components. Vacuum is not necessarily the best choice since it eliminates dumping, which leads to higher phase noise and more severe up-state ringing. Complete absence of water also results in higher friction coefficients and accelerated surface damage upon contact. As a result, more work is needed in identifying the best possible environment. Developing the necessary package for controlling this microenvironment is also of equal importance. Most researchers believe that a hermetic package will be necessary and work on this issues has been already initiated (see for example [91]). Besides being hermetic, the package has to also be mechanically and thermally stable and present a very low RF loss, comparable to that of the MEMS device itself. The necessity of low cost will most likely lead researchers to wafer-scale packaging solutions.

9.3.3 Modeling

Modeling plays a very significant role in understanding MEMS performance and failure mechanisms. Today's tools, however, do not sufficiently cover this need. Two primary groups of software packages are available now. The first groups includes mostly simple 1-D (e.g. mass-spring model) or SPICE-type models (e.g. SUGAR [29]). These models typically offer useful and fast information in calculating some important design parameters, such as actuation voltage, power handling and switching speed. They are not capable, however, of accurately modeling complex phenomena, such as

partial actuation [92], or phenomena related to MEMS lifetime (e.g. contact resistance degradation). Consequently, the simplicity and speed of these models make them particularly useful as initial design tools, but significantly more information is needed for complete and full physical understanding. On the other hand, more complete 3-D models have become available from ANSYS [93], Coventor [94], MEMSCAP [95] and others. Although these software packages are capable of modeling the true MEMS structure, useful results are extracted only when the process parameters are precisely known. When these parameters are known, accurate results may be obtained from these packages in static, small signal dynamic, thermal and electromagnetic analysis. Nevertheless, significant time is required to obtain these results and it is, therefore, difficult to use these packages as design aids. Furthermore, the mathematical equations used by these packages typically originate from traditional mechanical/materials engineering models that focus on bulk structures rather than thin films. In order to resolve several of the existing reliability issues (dielectric charging, contact surface damage, RF welding), however, new models that focus on interatomic interactions (1,000-100,000 atoms) under conditions that typically occur during the operation of conventional MEMS devices will be required. This is a wide-open research area where a lot of work will be needed in the future.

APPENDICES

Appendix A

Useful Chemicals for the RF MEMS Devices Fabrication

Table A.1 list the most important chemicals that have been utilized in the course of this work for fabricating the presented devices. Almost all of them are classified as hazardous materials, so the appropriate Material Safety Date Sheets (MSDS's) have to be carefully read before these materials are used. Additional information about safe handling may be found at the Occupational Safety and Health Administration website (http://www.osha.gov).

Table A.1: Needed chemicals for the fabrication of the devices presented in this thesis.

Chemical	**Type**	**Purpose**
SC1813	Positive photoresist (Shipley)	Pattern, sacrificial layer
SC1827	Positive photoresist (Shipley)	Sacrificial layer, plating
AZ5214	Negative photoresist (Clariant)	Metal lift-off
AZ9260	Positive photoresist (Clariant)	Sacrificial layer, plating
PI2545	Polyimide (Dupont)	Sacrificial layer
VM651 (diluted)	Adhesion promoter	spin before PI2545
MF351:H_2O (1:5)	Positive developer (Base)	Develop SC1813, SC1827
AZ327	Negative developer (Base)	Develop AZ5214
AZ400:H_2O (1:5)	Positive developer (Base)	Develop AZ9260
HMDS[a] (diluted)	Adhesion promoter	spin before photoresist
H_2SO_4:H_2O_2 (1:1)	Acid in hydrogen peroxide	Piranha clean
HF:H_2O (1:10)	Strong acid diluted in water	Ti etch
HCl:H_2O (1:1)	Acid diluted in water	Ni etch
BHF[b]	Acid	SiO_2 etch
TFA	Acid	Au etch
CR14	Cr etchant (acid)	Etch mask Cr
Acetone[c]	Organic	Wafer clean
IPA[d]	Organic	Wafer clean
Ethyl alcohol[e]	Organic	use in CPD chamber
PRS2000	Photoresist stripper	Etch sacrificial layer (hot)
Barrett SN	Ni plating solution (MacDermid)	Ni plating
H_3BO_3	Acid	Add to Barrett SN (30g/l)
Orotemp 24	Au plating solution (Technic)	Au plating

[a] Hexamethyldisilazane — $C_6H_{19}NSi_2$
[b] Buffer HF
[c] CH_3COCH_3
[d] Isopropyl alcohol — $CH_3CHOHCH_3$
[e] 200 proof — CH_3CH_2OH

Appendix B

Fabrication Processes

B.1 Introduction

THIS appendix covers the fabrication processes of the MEMS switches and varactor presented in this thesis. All of the devices have been fabricated by the author (except those mentioned in Chapter 1) at The University of Michigan clean room maintained by the Solid State Electronics Laboratory (SSEL). The processing has been almost exclusively performed on high-resistivity silicon wafers (resistivity was higher than 2000 Ω-cm before the oxidization step) with 2000-3000 $\mathring{A}$ of SiO_2.However, it can be equally well applied to almost any optically smooth substrate (glass, GaAs, etc.). The size of the processed wafers has typically been approximately 3.5×3.5 cm^2 coming from 4-in high resistivity silicon wafers.

B.2 Equipment

The following is a list of the most commonly utilized equipment for fabricating the MEMS devices in this thesis. They are available at the SSEL of The University of Michigan (http://www.eecs.umich.edu/ssel). The provided description is partly based on [37]. Additional information may be found in [96].

1. **Mask maker (Interserv, model 122135):** a piece of equipment used to selectively expose (UV light) small apertures onto the surface of a photosensitive masking plate (photomask). 4×4 glass plates have been used in this work. The plate is typically covered by a thin Cr film coated with positive photoresist. The exposed photoresist is etched, followed by the Cr layer underneath it. Finally, the remaining photoresist is removed leaving the mask with the desired pattern.
2. **Mask aligner (MJB3 K. Suss):** a device used to precisely align a photomask to a wafer. The MJB3 mask aligner may potentially achieve sub-micron level alignment tolerances, but the devices in this thesis have been fabricated with a maximum misalignment of ± 1 μm. After the alignment is complete, the wafer is exposed to UV light (light intensity is typically 20 mW/cm^2) through the photomask. Thus the mask pattern is transferred the wafer. The process is completed by etching of the exposed photoresist.
3. **Electron Beam Evaporators (Enerjet and SJ-20):** tools which utilize a high-energy beam to evaporate materials from a source crucible. Although a variety of materials (both metals and dielectrics) can be evaporated, Ti, Cr, Au and Ni are the metals that have been evaporated during the course of this work. The deposition rate for these materials typically varies between 5 and 15 $\mathring{A}$/sec.
4. **Sputter coater (Enerjet):** a useful tool particularly suited for conformal coatings. A high energy Ar plasma is formed to etch particles from a source target and then redeposit them on the wafer. Because of the randomness involved in the etching and redeposition, a high-quality conformal coating can be achieved. The plasma can be excited by either a DC or an RF source, depending on the source target. A large number of metals and dielectrics can be sputtered. DC sputtering is typically used for metals, while dielectrics

require an RF source. The major advantage of sputter-deposited materials is that they typically exhibit less residual stress due to the randomness of the deposition process. Furthermore, appropriate adjustments of the deposition rate and sputtering pressure can lead to thin films with very low residual stress [97]. The techniques developed in [97] have been also applied here for low-stress Au films. The random nature of the etching and redeposition also allows a high-quality conformal coating of surfaces with large aspect ratio. Examples of sputtered materials used in this thesis include Ti, Cr, Au, SiCr and SiO_2.

5. **Low Pressure Chemical Vapor Deposition (LPCVD) machine (Oxidization furnace):** A tool used to grow thin oxide and nitride films on wafers. The deposition takes place in high temperatures (e.g. 1100°C for SiO_2) and results in high quality thin films. The wafers mentioned in this thesis have been oxidized by this machine based on recipes that can be found in detail in [98].
6. **Plasma-Enhanced Chemical Vapor Deposition (PECVD) machine (Semi-Group PECVD):** A tool that achieves thin film growth on a wafer surface by using an RF plasma at relatively low temperatures (200–400°C). Although the obtained films are inferior to the ones obtained by LPCVD deposition, this process allows thin films such as Si_3N_4 and SiO_2 to be grown on wafers that are sensitive to high temperatures. Si_3N_4 over Au surfaces, for example, has been extensively utilized in this work.
7. **Reactive Ion Etch (RIE) machine (Semi-Group RIE and Technics Asher):** A tool that removes materials from a wafer surface. The etch is enabled by an RF plasma and the appropriate chemicals. Si_3N_4 etch has been accomplished in this thesis by using this tool. The Technics Asher is a tool almost exclusively used to clean a wafer surface by organic residues

(e.g. photoresist residue) after a wet or dry etch. It uses a weak plasma and low RF power to accomplish that.

8. **Critical Point Drying (CPD) machine (Tousimis Autosamdri-815B series):** A tool that allows drying of MEMS devices after their sacrificial layers have been etched by a wet process. Traditional drying (N_2 blowing for example) can not be used because the surface tension of the liquid underneath the MEMS causes the structure to collapse and stick to the substrate. The CPD machine replaces the liquid surrounding the MEMS structure by liquid CO_2. It then brings the CO_2 at its critical point (31°C, 1072 psi) where there is no difference between the liquid and gas state of the medium. At this point the surface tension of CO_2 is (theoretically) zero. The pressure is then slowly released and the MEMS devices is dried without any damage.

   Before applied to the MEMS field, this technique had been extensively used for cleaning bio-samples. In theory any medium can be used, but the critical point of many materials is not easily achieved in the lab. For example, water's critical point requires a temperature of 374°C at 3212 psi. Consequently CO_2 tends to be a convenient choice. However, CO_2 is not miscible with water, so the wafers with MEMS devices have to be immersed in an organic liquid (e.g. isopropylic alcohol or acetone) before they are place in the CPD machine.

B.3 Photolithographic processes

This section presents the details of the photolithographic processes commonly found in the fabrication procedures of the MEMS devices in this thesis.

B.3.1 Lithography with Negative Photoresist (AZ5214)

1. Spin HMDS at 3.5 krpm for 30 sec.

2. Wait 10 sec.
3. Spin AZ5214 at 3.5 krpm for 30 sec.
4. Softbake the wafer at a 105°C hotplate for 1 min.
5. Align wafer to mask and expose for 4.5 sec at 20 mW/cm^2.
6. Hardbake at a 130°C hotplate for 1 min.
7. Expose wafer (flood exposure) for 1.5 min at 20 mW/cm^2.
8. Develop in AZ327 for 35 sec.
9. Rinse in DI H_2O and dry with nitrogen gun.
10. Inspect wafer under microscope.
11. Clean wafer in the plasma asher (O_2) at 100 W, 250 mT for 1 min.

The final photoresist thickness is approximately 1.5 μm.

B.3.2 Lithography with Positive Photoresist (AZ1813)

1. Spin HMDS at 3.5 krpm for 30 sec.
2. Wait 10 sec.
3. Spin SC1813 at 3.5 krpm for 30 sec.
4. Softbake the wafer at a 105°C hotplate for 1 min.
5. Align wafer to mask and expose for 6 sec at 20 mW/cm^2.
6. Develop in MF351:H_2O (1:5) for 20 sec.
7. Rinse in DI H_2O and dry with nitrogen gun.
8. Inspect wafer under microscope.
9. Hardbake at a 130°C hotplate for 1 min.
10. Clean wafer in the plasma asher (O_2) at 100 W, 250 mT for 1 min.

The final photoresist thickness is approximately 1.5 μm.

B.3.3 Lithography with Positive Photoresist (AZ1827)

1. Spin HMDS at 3.5 krpm for 30 sec.
2. Wait 10 sec.
3. Spin SC1827 at 3.5 krpm for 30 sec.
4. Softbake the wafer at a 105°C hotplate for 1 min.
5. Align wafer to mask and expose for 15 sec at 20 mW/cm^2.
6. Develop in MF351:H_2O (1:5) for 30 sec.
7. Rinse in DI H_2O and dry with nitrogen gun.
8. Inspect wafer under microscope.
9. Hardbake at a 130°C hotplate for 1 min.
10. Clean wafer in the plasma asher (O_2) at 100 W, 250 mT for 1 min.

The final photoresist thickness is approximately 3 μm.

B.3.4 Lithography with Positive Photoresist (AZ9260)

The following recipe is provided for two spinning speeds (2 and 4 krpm).

1. Spin HMDS at 2 or 4 krpm for 30 sec.
2. Wait 10 sec.
3. Spin AZ9260 for 5 sec "spread" followed by 2 or 4 krpm for 30 sec.
4. if spun at 2krpm, rest wafer horizontally in closed wafer carrier for 20 min (retains solvents).
5. Softbake the wafer at a 110°C hotplate for 4.5 min (2 krpm) or 2.5 min (4 krpm).
6. Rest wafer horizontally for 20 min.
7. Align wafer to mask and expose for 2 min (2 krpm) or 45 sec (4 krpm) at 20 mW/cm^2.
8. Develop in AZ400K:H_2O (1:3) for 1-2 min.

9. Rinse in DI H_2O and dry with nitrogen gun.
10. Inspect wafer under microscope.
11. Clean wafer in the plasma asher (O_2) at 100 W, 250 mT for 1 min.

    The final photoresist thickness is approximately 10 μm (2 krpm) or 7 μm (4 krpm).

B.4 Wafer Cleaning Processes

The yield of the process is significantly improved by frequent wafer cleaning. Two processes have been found particularly useful: Piranha clean and Acetone/IPA clean.

B.4.1 Piranha Clean

Mix (1:1 ratio) sulfuric acid (H_2SO_4) with hydrogen peroxide (always add the acid to the H_2O_2). Place the wafer in the solution for 10 min. The ozone (O_3) that is released (equation B.1) cleans the wafer from organic contaminants. Rinse in DI H_2O.

$$3H_2O_2 + H_2SO_4 \longrightarrow 3H_2O + 2H^+ + SO_4^{--} + O_3 \uparrow + \text{heat} \tag{B.1}$$

B.4.2 Acetone/IPA clean

Place the wafer in a beaker with Acetone for 2 min followed by 2 min in IPA. Dry with nitrogen gun and dehydrate bake at a 130°C hotplate. Clean wafer in the plasma asher (O_2) at 150 W, 250 mT for 3 min.

B.5 Low-Voltage Switch Fabrication Process

The first fabrication process for the switch was introduced by Sergio Pacheco [15]. The process described here is an optimized one using 1) SC1827 (instead of

polyimide) for sacrificial layer and 2) sputtered (instead of evaporated) seed layer. The top electrode fabrication is described in detail in Sergio Pacheco's dissertation.

1. Clean the wafer according to the piranha clean process.
2. First Metallization (lift-off)
   (a) Perform the AZ5214 lithography with the circuit-layer mask.
   (b) Evaporate Ti/Au 500/9000 $\mathring{A}$.
   (c) Soak samples in hot PRS2000 for at least 2 hours (preferably overnight) for metal lift-off.
   (d) Lightly swab with PRS2000 to complete metal lift-off.
   (e) Rinse in DI H_2O for 15 min.
   (f) Perform Acetone/IPA clean.
3. Dielectric Layer Deposition and Patterning
   (a) PECVD deposit 1000-2000 $\mathring{A}$ of Si_3N_4 depending on the desired down-state switch capacitance. The following recipe results in a deposition rate of approximately 170-180 $\mathring{A}$/min.
   gas 1: SiH_4 100 sccm
   gas 2: NH_3 10 sccm
   gas 3: He 900 sccm
   gas 4: N_2 990 sccm
   deposition temperature: 400°C
   deposition pressure: 700 mT
   RF power: 100 W
   (b) Perform Acetone/IPA clean
   (c) Perform SC1813 lithography with the dielectric-layer mask.
   (d) RIE etch dielectric. The following recipe results in an etch rate of approximately 450-500 $\mathring{A}$/min.
   gas 1: CF_4 40 sccm

gas 2: O_2 1 sccm

plasma pressure: 100 mT

RF power: 100 W

(e) Soak sample in hot PRS2000 to remove the SC1813.

(f) Rinse in DI H_2O for 15 min.

(g) Dry with nitrogen gun.

4. Sacrificial Layer

   (a) Perform the SC1827 lithography with the sacrificial-layer mask.

   (b) Hardbake at a 160°C hotplate for 3.5 min. This step prevents the sacrificial layer from "bubbling" during subsequent soft- and hardbakes.

5. Switch Formation

   (a) Sputter (DC source) 2000 $\mathring{A}$ of Ti, 7 mT Ar pressure, 550 W DC power for a deposition rate of 47 $\mathring{A}$/min.

   (b) Evaporate 500 $\mathring{A}$ of Ni.

   (c) Perform the SC1827 lithography with the switch-layer mask.

   (d) Electroplate 1.5-2 μm of Ni at low current density.

6. Switch Release

   (a) Flood expose the wafer at 20 mW/cm^2 for 1.5 min.

   (b) Develop the exposed SC1827 (plating mold) in MF351:H_2O (1:5) for 1 min.

   (c) Rinse in DI H_2O.

   (d) Clean wafer in the plasma asher (O_2) at 100 W, 250 mT for 1 min.

   (e) Wet etch the Ni seed layer in HCl:H_2O (1:1) for 3 min.

   (f) Rinse in DI H_2O.

   (g) Wet etch the Ti seed layer in HF:H_2O (1:10) for 3-4 sec.

   (h) Rinse in DI H_2O.

   (i) Soak the wafer in hot PRS2000 for at least 2 hours.

(j) Let the beaker with the hot PRS2000 cool to room temperature.

(k) Rinse in DI H_2O for 15 min.

(l) Soak wafer in IPA for 5 min.

(m) Dry the wafer in CPD.

B.6 DC-Contact Switch Fabrication Process

1. Clean the wafer according to the piranha clean process
2. Bias Lines
   (a) Perform the AZ5214 lithography with the bias-layer mask.
   (b) Sputter 1200 $\mathring{A}$ (RF source) of SiCr, 7 mT Ar pressure, 700 W RF power. The deposition rate is approximately 70 $\mathring{A}$/min and the resulted film has a resistivity of approximately 500-700 $\Omega/\square$.
   (c) Soak samples in hot PRS2000 for at least 2 hours (preferably overnight) for SiCr lift-off.
   (d) Lightly swab with PRS2000 to complete metal lift-off.
   (e) Rinse in DI H_2O for 15 min.
   (f) Perform Acetone/IPA clean.
3. First Metallization (lift-off)
   (a) Perform the AZ5214 lithography with the circuit-layer mask.
   (b) Evaporate Ti/Au 500/9000 $\mathring{A}$.
   (c) Soak samples in hot PRS2000 for at least 2 hours (preferably overnight) for metal lift-off.
   (d) Lightly swab with PRS2000 to complete metal lift-off.
   (e) Rinse in DI H_2O for 15 min.
   (f) Perform Acetone/IPA clean.
4. Dielectric Layer Deposition and Patterning

(a) PECVD deposit 3000 $\mathring{A}$ of Si_3N_4. The following recipe results in a deposition rate of approximately 170-180 $\mathring{A}$/min.

gas 1: SiH_4 100 sccm

gas 2: NH_3 10 sccm

gas 3: He 900 sccm

gas 4: N_2 990 sccm

deposition temperature: 400°C

deposition pressure: 700 mT

RF power: 100 W

(b) Perform Acetone/IPA clean.

(c) Perform SC1813 lithography with the dielectric-layer mask.

(d) RIE etch dielectric. The following recipe results in an etch rate of approximately 450-500 $\mathring{A}$/min.

gas 1: CF_4 40 sccm

gas 2: O_2 1 sccm

plasma pressure: 100 mT

RF power: 100 W

(e) Soak sample in hot PRS2000 to remove the SC1813.

(f) Rinse in DI H_2O for 15 min.

(g) Dry with nitrogen gun.

5. First Sacrificial Layer

(a) Perform the SC1827 lithography with the sacrificial-layer mask.

(b) Hardbake at a 160°C hotplate for 3.5 min. This step prevents the sacrificial layer from "bubbling" during subsequent soft- and hardbakes.

6. Movable Beam Formation

(a) Sputter (DC source) 2000 $\mathring{A}$ of Ti, 7 mT Ar pressure, 550 W for a deposition rate of 47 $\mathring{A}$/min.

(b) Sputter (DC source) 7000 $\mathring{A}$ of Au, 7 mT Ar pressure, 0.5 A for a deposition rate of 280 $\mathring{A}$/min.

(c) Perform the SC1813 lithography with the movable beam-layer mask.

(d) Wet etch Au in TFA solution for 1.5–2 min.

(e) Rinse in DI H_2O.

(f) Wet etch Ti in HF:H_2O (1:10) for 4–5 sec.

(g) Rinse in DI H_2O.

(h) Flood expose the wafer at 20 mW/cm^2 for 1.5 min

(i) Develop the exposed SC1827 in MF351:H_2O (1:5) for 1 min.

(j) Rinse in DI H_2O.

(k) Clean wafer in the plasma asher (O_2) at 100 W, 250 mT for 1 min.

7. Second Sacrificial Layer

(a) Spin VM651 at 2.5 krpm for 30 sec.

(b) Wait 20 sec.

(c) Spin polyimide PI2545 at 2.5 krpm for 30 sec.

(d) Softbake the wafer at a 150°C oven for 30 min.

(e) Evaporate 500 $\mathring{A}$ of Ti.

(f) Perform the SC1813 lithography with the second sacrificial-layer mask.

(g) Wet etch Ti in HF:H_2O (1:10) for 3–4 sec.

(h) Rinse in DI H_2O and dry with nitrogen gun.

(i) Etch polyimide PI2545 in MF351:H_2O (1:5) for 3 min.

(j) Rinse in DI H_2O and dry with nitrogen gun.

(k) Remove SC1813 in Acetone/IPA (30 sec each).

(l) Clean wafer in the plasma asher (O_2) at 100 W, 250 mT for 1 min.

(m) Remove Ti in HF:H_2O (1:10) for 3–4 sec.

(n) Rinse in DI H_2O and dry with nitrogen gun.

8. Static Beam Formation

(a) Sputter (DC source) 2000 $\mathring{A}$ of Au, 10 mT Ar pressure, 0.5 A for a deposition rate of 280 $\mathring{A}$/min.

(b) Perform the SC1827 lithography with the static beam-layer mask.

(c) Electroplate 5–6 μm of Au at low current density.

9. Switch Release

(a) Flood expose the wafer at 20 mW/cm^2 for 1.5 min.

(b) Develop the exposed SC1827 (plating mold) in MF351:H_2O (1:5) for 1 min.

(c) Rinse in DI H_2O.

(d) Clean wafer in the plasma asher (O_2) at 100 W, 250 mT for 1 min.

(e) Wet etch the Au seed layer in TFA solution for 30 sec.

(f) Rinse in DI H_2O.

(g) Soak the wafer in hot PRS2000 for at least 2 hours.

(h) Let the beaker with the hot PRS2000 cool to room temperature.

(i) Rinse in DI H_2O for 15 min.

(j) Soak wafer in IPA for 5 min.

(k) Dry the wafer in CPD.

B.7 Analog Varactor Fabrication Process

1. Clean the wafer according to the piranha clean process
2. First Metallization (lift-off)

(a) Perform the AZ5214 lithography with the circuit-layer mask.

(b) Evaporate Ti/Au 500/9000 $\mathring{A}$.

(c) Soak samples in hot PRS2000 for at least 2 hours (preferably overnight) for metal lift-off.

(d) Lightly swab with PRS2000 to complete metal lift-off.

(e) Rinse in DI H_2O for 15 min.

(f) Perform Acetone/IPA clean.

3. Dielectric Layer Deposition and Patterning

(a) PECVD deposit 2000 $\mathring{A}$ of Si_3N_4. The following recipe results in a deposition rate of approximately 170-180 $\mathring{A}$/min.

gas 1: SiH_4 100 sccm

gas 2: NH_3 10 sccm

gas 3: He 900 sccm

gas 4: N_2 990 sccm

deposition temperature: 400°C

deposition pressure: 700 mT

RF power: 100 W

(b) Perform Acetone/IPA clean

(c) Perform SC1813 lithography with the dielectric-layer mask.

(d) RIE etch dielectric. The following recipe results in an etch rate of approximately 450-500 $\mathring{A}$/min.

gas 1: CF_4 40 sccm

gas 2: O_2 1 sccm

plasma pressure: 100 mT

RF power: 100 W

(e) Soak sample in hot PRS2000 to remove the SC1813.

(f) Rinse in DI H_2O for 15 min.

(g) Dry with nitrogen gun.

4. First Sacrificial Layer

(a) Perform the SC1827 lithography with the sacrificial-layer mask.

(b) Hardbake at a 180°C hotplate for 3.5 min. This step prevents the sacrificial layer from "bubbling" during subsequent soft- and hardbakes.

5. Lower Beam Formation
    (a) Sputter (DC source) 7000 $\mathring{A}$ of Au, 10 mT Ar pressure, 0.5 A for a deposition rate of 280 $\mathring{A}$/min.
    (b) Perform the SC1813 lithography with the movable beam-layer mask.
    (c) Wet etch Au in TFA solution for 1.5–2 min.
    (d) Rinse in DI H_2O.
    (e) Flood expose the wafer at 20 mW/cm^2 for 1.5 min
    (f) Develop the exposed SC1827 in MF351:H_2O (1:5) for 1 min.
    (g) Rinse in DI H_2O.
    (h) Clean wafer in the plasma asher (O_2) at 100 W, 250 mT for 1 min.
6. Second Sacrificial Layer
    (a) Perform the AZ9260 lithography with the second sacrificial-layer mask. The spinning speed is 4 krpm for a thickness of about 7 μm (is reduced to about 6 μm after the subsequent step).
    (b) Hardbake at a 150°C oven for 1 hour. This step prevents the sacrificial layer from "bubbling" during subsequent soft- and hardbakes.
7. Upper Beam Formation
    (a) Sputter (DC source) 1000 $\mathring{A}$ of Au, 10 mT Ar pressure, 0.5 A for a deposition rate of 280 $\mathring{A}$/min.
    (b) Perform the AZ9260 lithography with the upper beam-layer mask.
    (c) Electroplate 10–13 μm of Au.
8. Varactor Release
    (a) Flood expose the wafer at 20 mW/cm^2 for 5 min.
    (b) Develop the exposed AZ9260 (plating mold) in AZ400K:H_2O (1:3) for 2 min.
    (c) Rinse in DI H_2O.
    (d) Clean wafer in the plasma asher (O_2) at 150 W, 250 mT for 3 min.

(e) Wet etch the Au seed layer in TFA solution for 30 sec.

(f) Rinse in DI H_2O.

(g) Soak the wafer in hot PRS2000 for at least 2 hours.

(h) Let the beaker with the hot PRS2000 cool to room temperature.

(i) Rinse in DI H_2O for 15 min.

(j) Soak wafer in IPA for 5 min.

(k) Dry the wafer in CPD.

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