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# **MICROMACHINED W-BAND CIRCUITS**

**by**

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A dissertation submitted in partial fulfillment of the  
requirements for the degree of  
Doctor of Philosophy  
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To my parents, John and Martha Robertson, and  
In memory of my grandmother, Hazel Johnson Moss.

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## **PREFACE**

The goal of this dissertation is to present the work which has been done to demonstrate the successful application of micromachining technologies to high frequency microwave circuits. Through a marriage of silicon micromachining technology with microwave circuit development, new transmission lines and circuit structures have been realized. It is the intention of this document to show that these new micromachined structures represent a powerful solution to the problems encountered by conventional microwave circuits at millimeter-wave frequencies.

The main focus of the work presented is an experimental study of micromachined circuits for *W*-band applications. Methods for fabrication are developed and optimized, leading to the construction of various filters, resonators, and directional couplers. Measurements of these circuits show performance levels that clearly indicate the efficacy of membrane-supported structures for *W*-band applications.

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# microwaves

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# **CHAPTER I**

## **INTRODUCTION**

### **1.1 Motivation**

Historically, technological advancements in the development of microwave circuits have been driven by the desire to either elevate the performance levels or increase the operating frequency of a given component or circuit. The motivation to increase operating frequencies, in many instances, stems from the need to reduce the size and weight of the microwave circuits employed in communications, radar, and remote sensing systems. The overriding factor which dictates the size of microwave circuits is, of course, the wavelength; the smaller the wavelength, the smaller the circuit dimensions. The push to reduce size and weight, then, translates to a need for higher and higher operating frequencies. This is the case especially for atmospheric or space-based applications where deployment costs are dictated by the volume and mass of the systems mounted on a particular platform. Recently, miniaturization has also received attention in the development of collision-avoidance radars and “smart” cruise control systems in automotive applications [1].

For space based systems which are designed to communicate through or observe the earth’s atmosphere, atmospheric absorption plays a major role in determining which frequency range will be selected for the operation of the microwave equipment. In general, the absorption of microwave energy in the

atmosphere increases with frequency, but there are several peaks due to gaseous oxygen and water vapor that should be avoided [2]. A local minimum in the absorption spectrum at approximately 94 GHz makes W-band (75-110 GHz) a convenient choice for communications applications. Additionally, millimeter-wave imaging systems at 94 GHz have the ability to permeate fog, unlike infrared imaging systems [3].

The size and weight of many of these systems can be further reduced by utilizing planar microwave circuit architectures such as microstrip and coplanar waveguide (CPW), depicted in Figure 1.1. These technologies offer significant weight and cost reductions over rectangular waveguide. First, waveguide sys-

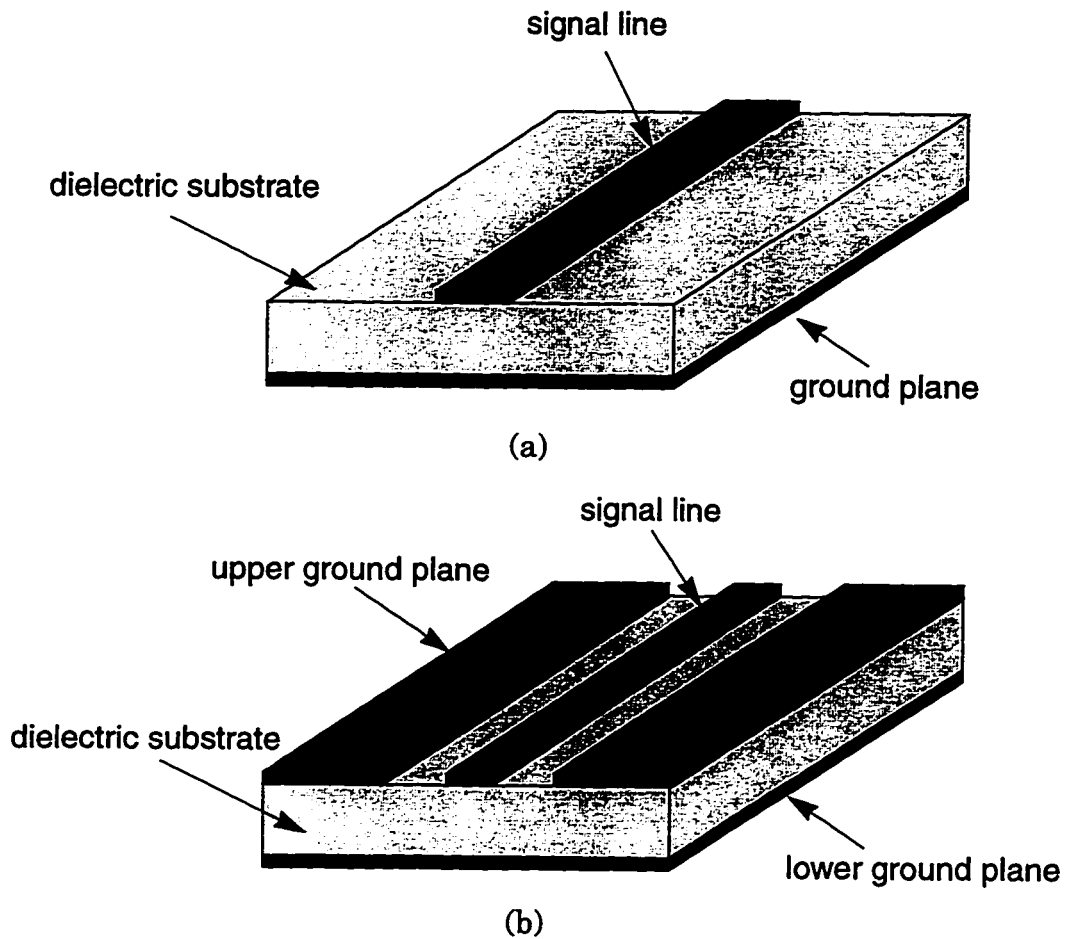


Figure 1.1: Conventional planar transmission line geometries: (a) microstrip line. (b) coplanar-waveguide (CPW).



tems must be precision machined one at a time, while planar microwave circuits can be batch fabricated using monolithic processing techniques adapted from integrated circuit fabrication. Second, waveguide circuit implementations are strictly limited to the operational bandwidth of the waveguide, but planar circuits can be optimized for broad band operation if desired. Finally, integration of active devices such as transistors and diodes is far more feasible with planar circuits, and this allows multiple system functions to be integrated into a single planar substrate. As described in Appendix A, uniplanar circuit structures such as coplanar-waveguide (CPW) and slotline are especially useful since they eliminate the need for via holes or backside metallization and can be integrated with solid-state devices on a single surface [4].

Challenges arise with planar circuit technologies when they are scaled to W-band, however, since the air-dielectric interface introduces parasitic effects such as dispersion, substrate moding, and dielectric loss, which increases with frequency. Usually, these problems are palliated by extra processing steps such as via holes and substrate thinning, but this may not completely eliminate the parasitics, and it may even reverse the production cost benefits which motivated the choice of planar circuits in the first place.

An alternate solution to the frequency limitations of conventional planar circuits employs micromachining techniques. This technology, which is widely used in the area of monolithic integrated sensors [5], was first applied to microwave circuits in the form of membrane supported antennas for millimeter-wave applications [6]. It was later adapted to microwave transmission lines in the form of the microshield line [7]. This transmission line structure, as shown in Figure 1.2, relies on selective silicon etching and membrane supported conductors and can be likened to a CPW line with an air dielectric. Development of the microshield line has opened the doors for a whole new way

of thinking about planar transmission line geometries. Removal of the dielectric substrate provides new opportunities for solving the problems associated with conventional planar transmission lines at millimeter-wave frequencies.

Radiation loss into parasitic modes (surface waves) in CPW [8] has been shown to be a function of both  $f^3$  and  $(\epsilon_r - 1)^2$ , where  $f$  is the frequency and  $\epsilon_r$  is the relative dielectric constant of the substrate [9]. Thus, although radiation loss increases rapidly with frequency, it can be eliminated by using an air dielectric. In addition, removal of the silicon substrate eliminates any loss associated directly with the dielectric, and any dispersion related to the dielectric/air interface. Passive microwave circuit components based on microshield line technology have demonstrated excellent performance up to 40 GHz [10]. In addition, membrane supported bolometers from microwave and millimeter-wave power detection have been reported [11],[12]. Recently, a sub-millimeter wave planar band-pass filter was demonstrated using microshield line [13], and time-domain electro-optic sampling of a CPW line on a membrane has indicated the successful propagation of signals at frequencies as high as 1000 GHz with low loss and low dispersion [14]. Other planar microwave circuits have employed membrane technology with excellent results, and these include a 33 GHz air-microstrip Wilkinson power divider [15] and air-stripline interdigitated band-pass filters at 15 GHz [16]. Micromachining was also applied in the development of a completely shielded CPW line [17].

The successes of membrane supported circuits between 5 and 40 GHz provided the foundation for the application of microshield line to *W*-band circuits. This was accomplished not only with the microshield line, but also with a new type of micromachined structure - the shielded membrane microstrip (SMM) line.

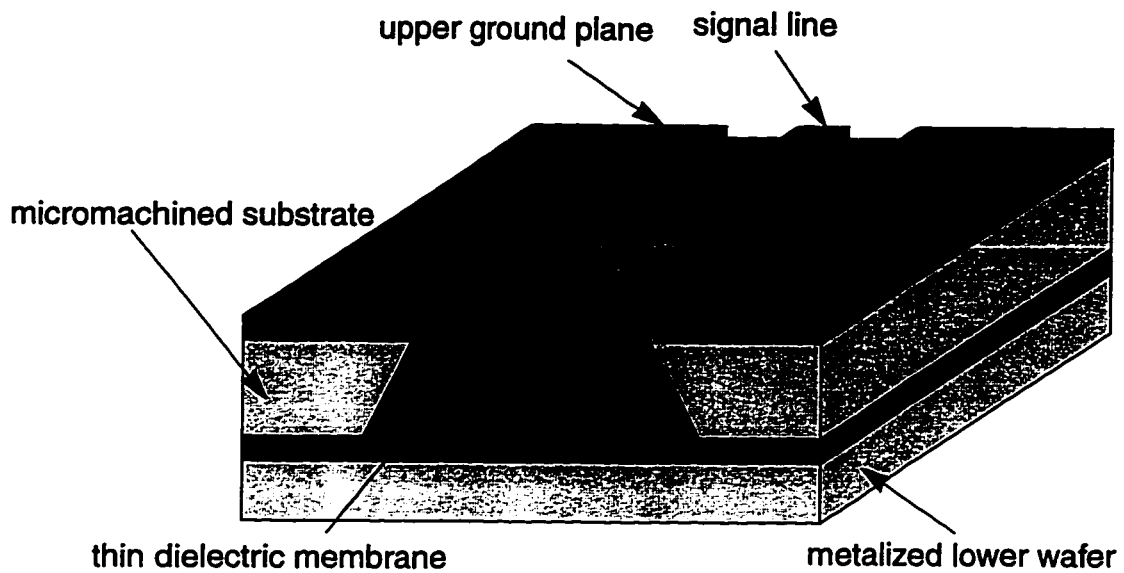


Figure 1.2: The microshield transmission line.

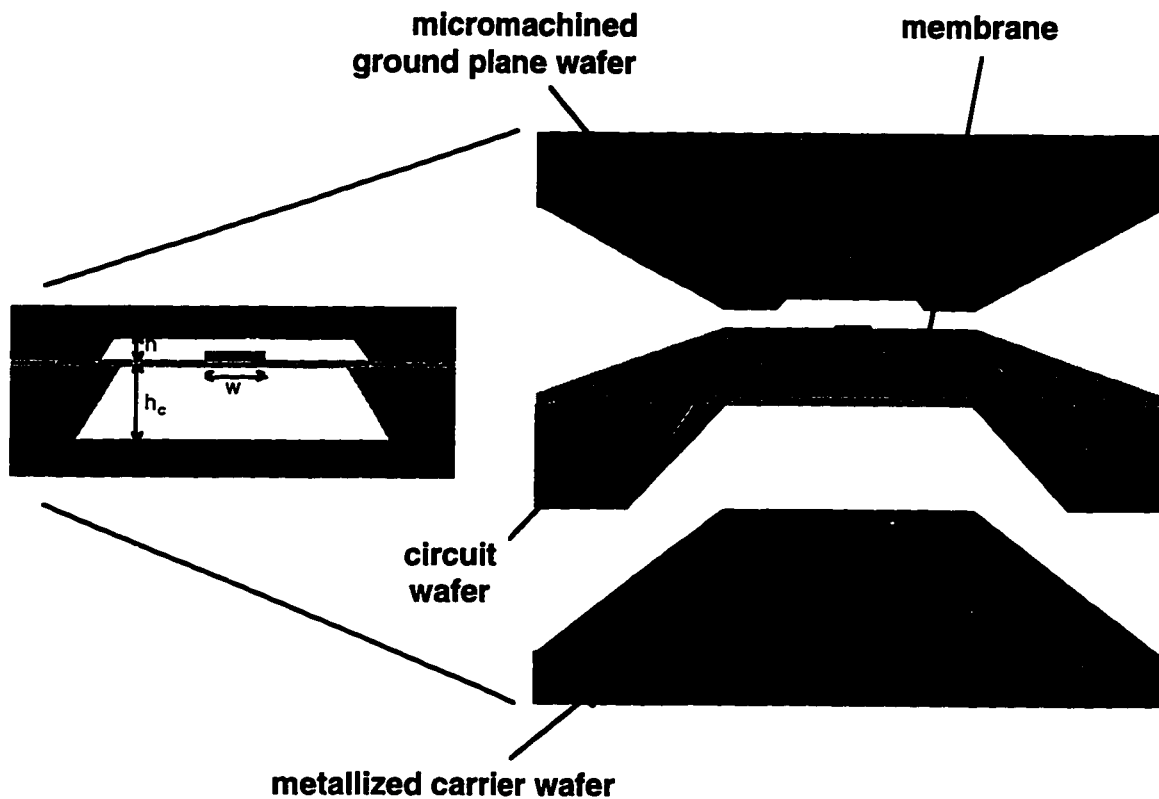


Figure 1.3: Geometry of shielded membrane microstrip (SMM). Two separate wafers are micromachined.

## 1.2 Summary

Chapter II of this thesis provides a detailed description of the technology associated with micromachined circuits and transmission lines. This includes a detailed discussion of the thin dielectric membranes and the micromachining process technologies associated with the fabrication of the membrane-supported circuits. In addition, treatment is given to the methods used for circuit design and testing. Then, a comprehensive treatment of the microshield line and the shielded membrane microstrip line architectures is given.

The membrane supported transmission line circuit elements which were experimentally studied are presented in Chapters III & IV. Chapter III discusses the circuits which can be classified as filters or filter elements, while Chapter IV outlines the results obtained for a high-pass directional coupler. Throughout these chapters, comparisons between the membrane supported components and equivalent substrate supported elements are provided with the use of theoretical studies. These studies demonstrate the success with which membrane-supported structures alleviate the problems associated with dielectric substrates.

Chapter V presents the results of a study into the application of micromachining to integrated packaging concepts. In particular, an existing low noise amplifier design based on a flip-chip InP HEMT is adapted to a shielded CPW environment, and tested for *K*-band operation. Results of these tests demonstrate the viability of the integrated packaging approach, especially with the use of flip-chip devices. This combination of integrated packaging and flip-chip devices represents a powerful method for MMIC cost reduction in terms of both design and fabrication expenses. These techniques will be even more advantageous when applied to *W*-band MMIC development.

The conclusions reached as a result of the body of work on micromachined circuits in *W*-band are summarized in Chapter VI. Also presented are several areas which will need attention in the future study of micromachined *W*-band circuits.

## **CHAPTER II**

# **MICROMACHINED TRANSMISSION LINES**

## **2.1 Introduction**

This chapter will present the basic background of micromachined transmission lines for *W*-band applications. There are two membrane supported lines which are discussed in detail: the microshield line and the shielded membrane microstrip line. Details of the design, fabrication, and testing of these lines, as well as some preliminary results concerning their *W*-band propagation characteristics is presented.

### **2.1.1 Fabrication of Membrane Supported Structures**

Development of membrane-supported transmission line structures is based on two major components: the thin dielectric layers that comprise the membranes and the bulk Si micromachining used to selectively remove Si underneath the membranes. These technologies rely on standard processing techniques that are common to most microelectronics fabrication laboratories. This is true even for the micromachining aspects of the fabrication process. Technology advancement in the microelectromechanical systems (MEMS) community has driven the optimization of many micromachining process techniques, and these procedures are now well developed and widely used.

### Thin Dielectric Membranes

The dielectric membrane employed in membrane-supported transmission lines and circuits is a very thin three layer  $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2$  composite structure that is grown/deposited on silicon wafers before any other processing is initiated. Typically, a batch of 25 wafers is thoroughly cleaned and then placed in a thermal oxidation furnace for growth of the base layer of 7500 Å thick silicon dioxide. The  $\text{SiO}_2$  is grown at a temperature of 1100°C in three steps. First, a few hundred Ångstroms of “dry” oxide is grown by flowing oxygen ( $\text{O}_2$ ) in the furnace for five minutes. Then, a hydrogen ( $\text{H}_2$ ) flow is added to the oxygen to begin the “wet” oxidation step, which grows the bulk of the film to a target thickness of 7500 Å. The wet oxide grows much more rapidly than the dry oxide, and it is also a more porous film. Total process time is determined by furnace characterization, and the 7500 Å film can typically be grown with about 90 to 100 minutes of wet oxidation. Finally, the hydrogen flow is discontinued, and a five minute dry oxidation step completes the film growth.

After the wafers have been oxidized, they are removed from the furnace and transferred to a Low Pressure Chemical Vapor Deposition (LPCVD) furnace, where they undergo a silicon nitride ( $\text{Si}_3\text{N}_4$ ) deposition followed by an oxide deposition. The silicon nitride film is deposited at a pressure of approximately 100-200 mTorr and tilt zone temperatures of 810/820/830°C. The constituent materials are provided by gaseous flows of dichlorosilane (DCS,  $\text{SiCl}_2\text{H}_2$ ) and ammonia ( $\text{NH}_3$ ). After the nitride deposition, the furnace zone temperatures are raised to 910/920/930°C and the final oxide film is deposited by flowing DCS with nitrous oxide ( $\text{N}_2\text{O}$ ) and an  $\text{N}_2$  (dilute) at a pressure of 400-600 mTorr. The target thicknesses for the nitride and oxide layers are 3500 Å and 4500 Å, respectively.

Once the tri-layer dielectric film has been deposited on the wafers, they are ready to undergo further processing to define the circuit metallization patterns and any other electrical elements required for the desired components. Typically, a single wafer is cleaved or diced into smaller pieces which can be processed individually. Once all front-side circuit processing has been completed, the final step of selective silicon removal can be performed. This is preceded by patterning the back side dielectrics to expose the silicon surface. An infrared (IR) alignment is used to align the backside patterns to the front surface and the backside dielectrics are then etched. This can be accomplished with a photoresist mask and a combination of dry and wet etches (note that the front side of the wafer must also be protected with photoresist to insure that the membrane dielectrics are not harmed by the back side processing). The silicon nitride layer must be etched using a  $\text{CF}_4/\text{O}_2$  plasma, while the oxide layers can be either wet-etched in a commercial Buffer HF (BHF) solution or dry-etched in a  $\text{CHF}_3/\text{CF}_4$  plasma. Perhaps the simplest way to etch the dielectrics is to use a plasma etching system that can be programmed to etch all three layers sequentially. Table 2.1 details the process parameters that have been used to etch the dielectric films in an automated plasma etching system.

The micromachining step occurs last in the fabrication sequence, since it is the “dirtiest” step and occurs outside of the clean fabrication facility. In addition, this prevents any post-processing on the suspended membranes. Although the membranes are rigorous enough to withstand further processing, special precautions must be taken to prevent their rupture, such as mounting the membrane wafer on a support wafer or glass slide [18], and the process can be simplified by performing the Si micromachining step last.



Etch film	(descum)	LPCVD Oxide	LPCVD Nitride	Thermal Oxide
Thickness (Å)	–	4500	3500	7500
O <sub>2</sub> rate (sccm)	50	–	1	–
CF <sub>4</sub> rate (sccm)	–	15	20	15
CHF <sub>3</sub> rate (sccm)	–	15	–	15
Pressure (mTorr)	300	40	100	40
Power (Watts)	50	100	80	100
Time (min)	1	23	35	38

Table 2.1: Process parameters for etching the three layers of the dielectric membrane in an automated plasma etching system.

### Bulk Si Micromachining

Development of chemical systems to etch silicon continues, but there are some very well known and well characterized wet-chemical solutions which can be applied to micromachining. These include Hydrofluoric-Nitric-Acetic Acids in water (HF-Nitric), Ethylene diamine-Pyrocatechol in water (EDP), Potassium Hydroxide in water (KOH), and Tetramethyl Ammonium Hydroxide in water (TMAH), among others [19],[20]. With the exception of HF-Nitric, all of these etching systems exhibit a strong dependence of the etch rate on crystal lattice of the Si wafer.

The crystalline structure of Si wafers can be described with *Miller indices*, which express directions and planes within the crystal lattice using a set of three integers [21]. Figure 2.1 (a) illustrates the crystal planes and directions which are of importance in the etching of Si. The anisotropic nature of the EDP, KOH, and TMAH etchants (among others) results from the fact that the {111} crystal planes etch much slower than all others. When a standard (100) silicon wafer is used in micromachining applications, the etchant will proceed rapidly in directions that are perpendicular and parallel to the surface of the

wafer. When a  $\{111\}$  crystal plane becomes exposed, however, the etchant effectively stops, leaving a sloping side wall in the etch profile. For randomly oriented shapes in the backside masking layers, the etchant will quickly undercut the mask until it reaches one of the four  $\{111\}$  planes that will stop the etch in a (100) wafer (see Figure 2.1 (b)).

To effectively utilize anisotropic etchants, etching patterns should be limited to rectangular shapes that are aligned with the  $\langle 110 \rangle$  directions (e.g. the major flat) of a silicon wafer. The final size and shape of a membrane suspended over a cavity can be determined by projecting the dimensions in the back side pattern to the front side along the  $54.74^\circ$  slope of the cavity side wall. When doing this, however, it is important to maintain good alignment of the etch mask with the  $\langle 110 \rangle$  directions, otherwise significant undercutting may occur, as in Figure 2.1 (c). If the back side etch patterns are to be aligned to the front side metallization features, then this requires that the front side patterns be aligned to the  $\langle 110 \rangle$  directions.

Among the anisotropic etchants available, only a few are acceptable for use in creating membrane supported circuits. The criterion which drives the selection of the anisotropic etchant is, in the end, the ability of the membrane structure itself to resist the silicon etchant so that it can serve as a backside etch mask to permit selective etching, and so that it will remain intact after the etch is complete. Note that the metallization system used for circuit realization must be resistant to the silicon etchant, since there is no way to mask the circuits during the micromachining step. In the case of the membrane-supported circuits used here, the LPCVD oxide which forms the outer membrane layer and the Ti/Au circuit metal must provide resistance to the silicon etchant.

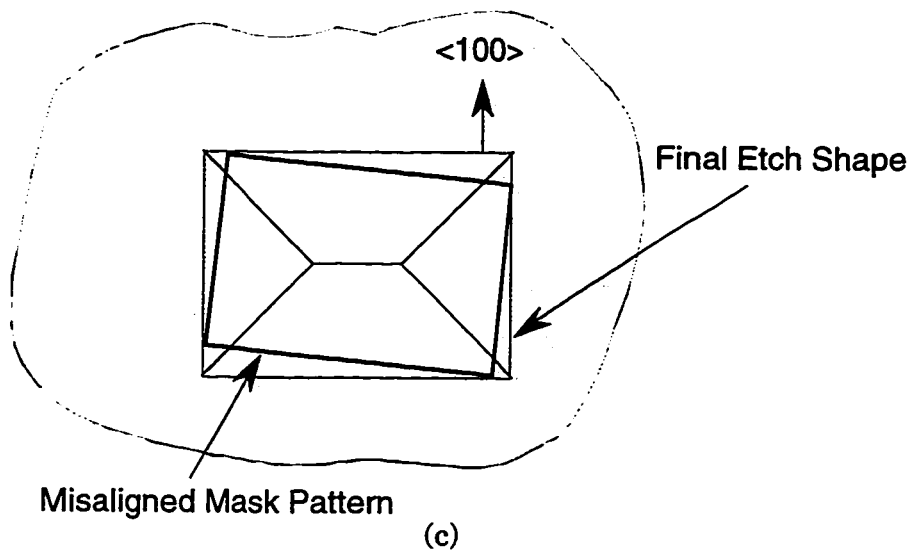
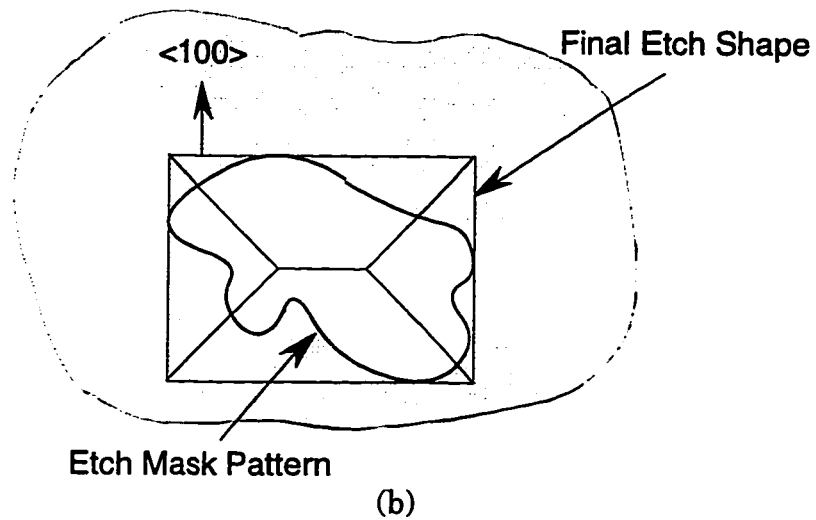
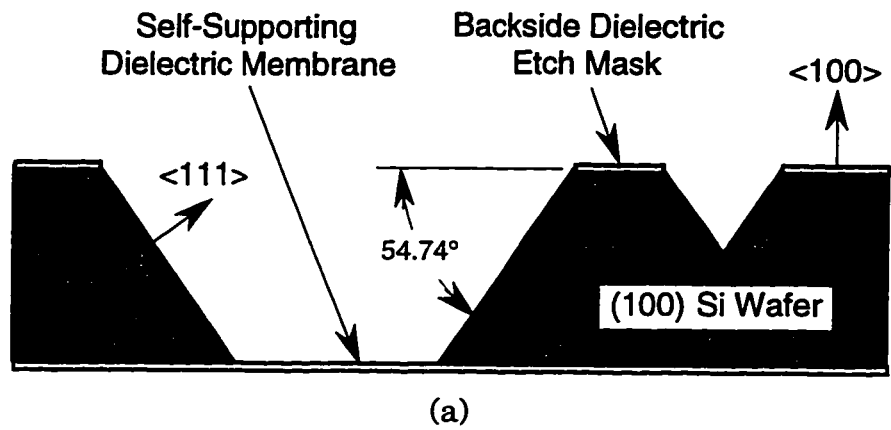


Figure 2.1: Characteristics of anisotropic silicon etchants. (a) Orientation of important crystal planes in the Si wafer. (b) Undercutting of an arbitrary pattern in the etch mask. (c) Undercutting due to misalignment of the etch mask to the <110> direction.

The EDP etchant system has shown very good selectivity to  $\text{SiO}_2$ , Ti, Au, and most refractory metals, and has been used exclusively for the micromachining steps described here. The etching solution is prepared according to the following recipe: 48 mL deionized water ( $\text{DI H}_2\text{O}$ ), 48 g Catechol, 0.9 g Pyrazine, and 150 mL Ethylene Diamine. The (100) silicon etch rate of this solution has been experimentally determined to be approximately  $1.2 \mu\text{m}/\text{minute}$  when the solution is kept between  $105^\circ\text{C}$  and  $110^\circ\text{C}$ , and it etches the LPCVD  $\text{SiO}_2$  film at a rate of approximately  $5 \text{ \AA}/\text{minute}$  [18]. It should also be noted that TMAH has been shown to etch  $\text{SiO}_2$  as much as four orders of magnitude slower than (100) silicon, depending on solution concentration and temperature [22], suggesting that it, too, could be used to etch silicon in membrane supported applications.

### 2.1.2 Membrane Properties

It is important to recognize that the thicknesses of the constituent dielectric layers in the thin membrane are very critical. In order for the membranes to remain rigid and self-supporting after the silicon has been removed underneath them, they must contain some amount of internal tensile stress. The correct amount of stress is not precisely known, but can be determined experimentally. If the membranes have too much tensile stress then they will crack under the pressure. If there is not enough tensile stress, or even some amount of compressive stress, the membranes will buckle.

The stresses that exist in the individual dielectric layers combine to generate the overall stress in the membrane, so they can be examined individually. The primary cause of residual stress in the thermal oxide film is the difference between the thermal expansion coefficients of the oxide layer and the silicon substrate. The linear coefficients of thermal expansion for Si and  $\text{SiO}_2$  are,

respectively,  $4.2 \times 10^{-6} \text{ }^\circ\text{C}^{-1}$  [23] and  $5 \times 10^{-7} \text{ }^\circ\text{C}^{-1}$  [24]. As a silicon wafer is cooled to room temperature after thermal oxidation, the wafer and the oxide film begin to shrink. The oxide film shrinks less than the wafer, and a compressive stress builds up in the film. Some of this stress is alleviated by reflowing while the oxide is still warm enough, but not all of it. Typically, the amount of compressive stress that remains in the oxide film is approximately  $3 \times 10^8 \text{ N/m}^2$  [25]. This value is largely independent of film thickness since the film is so much thinner than the silicon substrate and, as mentioned, some amount of reflowing occurs.

The stresses in LPCVD silicon nitride films have been measured to be approximately  $10 \times 10^8 \text{ N/m}^2$ , tensile [25]. The sources of this large tensile stress are not fully understood, since they are not simply explained by thermal expansion differences ( $\text{Si}_3\text{N}_4$  has a linear coefficient of thermal expansion of  $4 \times 10^{-6} \text{ }^\circ\text{C}^{-1}$  [25]).

The residual stress in LPCVD oxide films is more dependent on the deposition conditions than the stress in the nitride film. It is possible for the layer to have a tensile stress of up to  $3 \times 10^8 \text{ N/m}^2$  [25], but it is apparent from experimental data that the LPCVD film used in these experiments more closely resembles the thermal oxide [26] and adds some amount of compressive stress to the membrane.

The membrane dielectric thicknesses of 7500, 3500, and 4500 Å for the thermal oxide, LPCVD nitride, and LPCVD oxide, respectively, were chosen based on empirical observations. Depending on the stress level and final thickness of the LPCVD layer after Si etching, the three layer composite should achieve a low level of tensile stress, thereby producing reliable thin membranes.

The constituent  $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2$  layers of the membrane also possess relative permittivities of 3.9/7.5/3.9 [24], respectively, and they will therefore contribute to slight changes in the performance of membrane supported microwave circuits. These changes are significant enough to invalidate the assumption that the transmission line is operating entirely in an air environment at millimeter-wave frequencies, and techniques for including membrane effects in circuit simulations will be discussed shortly.

In summary, a listing of the known properties of the dielectric films used to construct the thin membranes appears in Table 2.2.

Layer	Thermal $\text{SiO}_2$	LPCVD $\text{Si}_3\text{N}_4$	LPCVD $\text{SiO}_2$
Thickness ( $\text{\AA}$ )	7500	3500	4500
Process Temp. ( $^\circ\text{C}$ ) <sup>a</sup>	1100	810,820,830	910,920,930
Process Pressure	Atm.	100-200 mTorr	400-600 mTorr
Process Reactants	$\text{O}_2, \text{H}_2$	$\text{SiCl}_2\text{H}_2, \text{NH}_3$	$\text{SiCl}_2\text{H}_2, \text{N}_2\text{O}, \text{N}_2(\text{dilute})$
Linear Coefficient of Thermal Expansion ( $\times 10^{-6}^\circ\text{C}^{-1}$ )	0.5 [24]	4 [25]	N/A
Stress ( $\times 10^8 \text{ N/m}^2$ )	3, compressive	10, tensile	3 to -3, comp.
Relative Dielectric Constant [24]	3.9	7.5	3.9
Etch Rate in EDP ( $\text{\AA}/\text{min}$ )	2 [19]	negl.	5 [18]

Table 2.2: Deposition parameters and properties of the dielectric thin films at 300°C.

a. Tilt zone temperatures are given for LPCVD films.

Survivability of the thin dielectric membranes is a concern if micromachined transmission lines and circuits are to be utilized in space, since the harsh conditions of launch must be endured. Preliminary results have indicated that the membranes are indeed strong enough to withstand the intense heat and vibration encountered during a space launch [27]. Further testing is needed to fully space qualify membrane-supported circuits, including radiation hardness characterization. In general, precautions such as pressure relief venting of micromachined cavities and careful handling practices must be used, but initial testing results demonstrate the robustness of the dielectric membranes.

### 2.1.3 Measurement Techniques

Microwave and millimeter-wave measurements of micromachined transmission lines and circuit elements are carried out using an HP 8510C Vector Network Analyzer (VNA) [28]. The network analyzer can be configured to measure the scattering parameters of a device or network from 2 to 118 GHz using three separate test sets. From 2 to 40 GHz, an 8516A *S*-Parameter Test Set is used with 3.5 mm coaxial cables which connect to Model 40A Picoprobes from GGB Industries [29] for on-wafer measurements. For measurements above 40 GHz, an 85105A Millimeter Wave Controller is used with either a *U*- or *W*-band test set. The *U*-band test set allows measurements from 40 to 60 GHz and employs an 83556A mm-Wave Source Module in addition to the directional couplers and harmonic mixers required to convert the measured signals to the 1.2 MHz baseband of the 85105A. On-wafer measurements are carried out with Model 67A Picoprobes which are connected to the WR-19 output of the *U*-band test set via 1.89 mm coaxial cables and WR-19 to 1.89 mm coax adaptors. At *W*-band, W85104A test set modules supply a measurement

signal from 70 to 118 GHz through WR-10 waveguide, and Model 120A-BT Picoprobes allow on-wafer measurements. Figure 2.2 contains a photograph of the network analyzer configured for *W*-band measurements, with the WR-10 modules placed on either side of the probe station. In all three measurement bands, the Picoprobes have a probe finger spacing (“pitch”) of 150  $\mu\text{m}$ , and are of the ground-signal-ground type. They are best suited for launching CPW type modes in planar circuits.

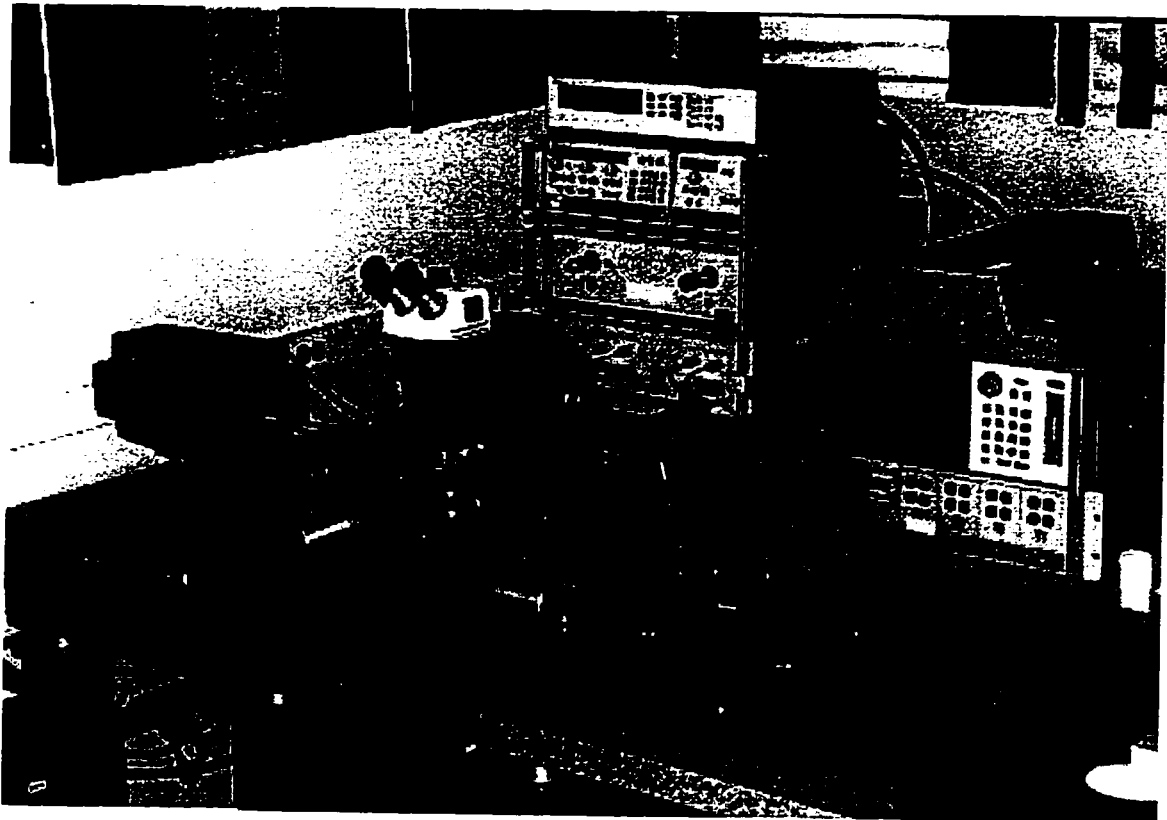


Figure 2.2: Photograph of the HP 8510C Network Analyzer configured for *W*-band measurements.



Calibration of the network analyzer can be accomplished in a variety of ways, with most methods providing satisfactory results in any of the three measurement bands. The two calibration methods most commonly used with micromachined circuits are the SOLT, or Short-Open-Load-Thru, method and the TRL, or Thru-Reflect-Line, method. The SOLT calibration establishes a reference plane at the end of the measurement probe tips where they contact the circuit or device under test. This is accomplished with a set of calibration standards (the open circuit, short circuit, load, and thru elements) which has been designed for use with a particular type of measurement probe. For the 150  $\mu\text{m}$  pitch Picoprobes, the CS-5 calibration substrate is available from GGB Industries [29]. The SOLT calibration software is built in to the HP 8510C network analyzer and can be adapted for any set of standards using a software “kit” which contains the appropriate information for the calibration set being used.

The TRL calibration method [30],[31] was developed to provide an on-wafer reference plane for microwave measurements. Using standards which can be fabricated in conjunction with the devices or circuits to be tested, all effects from the measurement probes and even the transmission line used to connect to the DUT can be de-embedded from the measurements. The calibration requires a minimum of three on-wafer standards: a thru line (the “Thru”), a delay line (the “Line”), and a short or open circuit to be used as the “Reflect” standard. After calibration, the measurement reference plane exists at the center of the standard defined as the “Thru.” All of the other standards are designed based on this reference point. The length of the thru line is not especially critical, but a good rule of thumb is to set the length equal to approximately half of a guided wavelength at the measurement frequency of interest.

Once the length of the thru-line has been determined, the reflect standard is selected to be either an open or short circuit. Usually this is based on the geometry of the transmission line being de-embedded. For microstrip type circuits, it is generally easier to use an open-circuited line, while for CPW-type circuits a short circuited line is preferred. The length of line between the probe contact point and the open or short circuit should be half the length of the thru line.

To complete the calibration set, only one more standard is required: the delay line. The length of the delay line must be chosen so that it provides the necessary information over the correct frequency range. The standard will be effective as long as the phase difference between it and the thru line is between  $50^\circ$  and  $140^\circ$ . If one delay line cannot be designed to apply over a desired range of calibration frequencies, then multiple delay lines can be used to provide complete coverage.

The National Institute for Standards and Technology (NIST) has developed an automated program called MultiCal [32] (formerly called DEEMBED) which was used to implement the TRL calibration method for the on-wafer measurement of micromachined transmission lines and circuits. The program runs in the HP Basic environment, and has been configured to communicate remotely with the VNA from a host computer. When using MultiCal, it is recommended that the calibration set include multiple delay line standards of various lengths. The program has the ability to determine which delay standard provides the most accurate and consistent data on a point-by-point basis, and automatically generates the best set of calibration coefficients and sends them to the VNA. In addition, by comparing the measured data to the user-specified physical line lengths, MultiCal is able to generate data on the attenuation constant and relative effective permittivity of the transmission line

architecture being used for the calibration [33]. As a result, the program can be a very effective diagnostic tool when experimenting with new transmission line geometries.

#### **2.1.4 Theoretical Methods**

The design and simulation of micromachined microwave circuits requires the use of various computational tools. Many commercial software applications have been developed to treat the needs of microwave circuit design in general, and many of these are applicable in the special case of membrane supported circuits. As will be demonstrated, the use of membrane supported structures to achieve air dielectrics often allows the use of simple theoretical models to predict micromachined circuit performance. In some cases, however, it becomes necessary to include the effects of the dielectric membrane in the analysis, and this can present some difficulties due to the extremely small dimensions associated with the membrane dielectrics.

Theoretical tools can be classified as either two-dimensional (2-D) or three-dimensional (3-D) simulators. Those in the 2-D grouping are generally used to predict the characteristic impedance and effective relative permittivity of a given transmission line structure by considering only a cross-section of the geometry. This is done based on the approximation that the capacitance per unit length of the line can be determined from the cross-section alone. The capacitance of the line can be found using a variety of different algorithms, but for coplanar type transmission lines, the conformal mapping method [34] and point matching method [35] have proven to be quite efficient and accurate. In addition, *LineCalc* [28] is a commercially available program that is capable of solving 2-D geometries for a variety of transmission line structures, and can be used for synthesis as well as analysis.

In order to design complete microwave circuits, it is necessary to study the interaction of multiple components which are designed to produce a desired result. This can be done with the 3-D simulators, which take into account the lengths of the components in addition to their height and width. These 3-D simulators can be further classified based on the type of analysis they perform: quasi-static analysis or full-wave analysis.

Quasi-static simulators apply ideal transmission line theory to the problem, with the assumption that there will be very few parasitic or non-ideal effects. In some cases, parasitic effects can be incorporated to the simulation in the form of dimension corrections which mimic the overall effect of a known discontinuity. For example, an open-circuited transmission line can be lengthened during a simulation to include the effects of fringing electric fields, which make the stub appear longer. Additionally, quasi-static simulators can often predict the effects of ohmic and dielectric loss by applying known rules to the geometries being considered. Quasi-static simulators range in complexity from the simple, PC-based microstrip circuit simulator known as *Puff* [36], to the Unix-based *Touchstone/Libra* [28], which incorporates circuit layout functions as well as non-linear device simulation and circuit optimization routines. There are also quasi-static simulators such as PARFIL [37] which are intended for only a specific class of microwave circuits. PARFIL is a PC-based program designed to predict the performance of bandpass and low-pass filters in many different planar and non-planar circuit architectures.

Finally, there is the class of 3-D circuit simulators that apply full-wave analysis to the microwave circuit problem. The term “full-wave analysis” implies that the solution algorithm is derived from the three dimensional Maxwell’s equations, and calculates all six components of the electric and magnetic fields at each point in the simulation space. This gives the simula-

tion the ability to predict all types of non-ideal effects, including dispersion, radiation into substrate modes, and parasitic coupling. Typically, full-wave analysis algorithms solve the problem in the context of a grid, or mesh, which limits the solution to discrete points in the simulation space. The size of the mesh often restricts the dimensions of the circuit features which can be effectively analyzed, and also determines the amount of computation time necessary to reach a solution. Full-wave analysis tools are very computationally intensive, and therefore do not make good candidates for circuit synthesis or circuit design, due to the need for repeated analysis iterations in a circuit design procedure. Sometimes, however, full-wave analysis techniques are the only means by which a particular circuit structure can be analyzed accurately. One technique that has been applied to many of micromachined microwave circuits is the finite-difference time-domain, or FDTD, algorithm [38]. The FDTD simulation provides several advantages for the study of micromachined structures. The fact that the solution occurs in the time domain means that a simple fast fourier transform (FFT) can be utilized to convert the results from a single simulation into data that cover a very wide frequency range. In addition, the use of advanced absorbing boundary conditions prevents problems that may be caused by the metallic walls surrounding the simulation space [39].

## 2.2 Microshield Line

The microshield line was proposed in 1991 [7] as the first application of micromachining techniques to a planar microwave transmission line geometry. The line can best be described as a coplanar waveguide (CPW) structure suspended in air above a metallized cavity (Figure 1.2). Excellent results have been reported for this structure in applications up to 40 GHz [10],[40], show-

ing that a definite performance advantage is achieved by the use of the thin dielectric membranes.

Characteristic impedances for microshield lines structures are primarily dependent on the geometric parameters  $s$  (signal conductor width),  $w$  (slot width) and  $h$  (cavity height), as is the case for substrate supported CPW structures. In addition, the lower cavity width plays a small role in determining the characteristic impedance, and must be considered.

Conformal mapping method (CMM) algorithms are readily applicable to the problem of solving the characteristic impedance of microshield lines, and are quite accurate [35]. Another method for calculating microshield impedances is the point matching method (PMM), which is more computationally intensive and places a metal shielding cavity around both upper and lower halves of the microshield structure. Whichever method is used, it is generally accepted that the cavity side walls may be approximated as vertical walls, rather than the sloping walls that are actually produced by the anisotropic etch used to fabricate the structure.

Also, when performing 2-D analysis of the microshield geometry, it is not computationally effective to attempt to directly consider the presence of the membrane. Since the thickness of the membrane ( $\sim 1.5 \mu\text{m}$ ) is a very small fraction of the total thickness of the structure, it is very difficult to include in an analytical solution. Instead, the effects of the membrane can be modeled in one of two ways. First, there is the option of filling the lower cavity of the microshield line with a very low dielectric constant material [10]. If the relative permittivity of this dielectric is adjusted until the computed effective relative permittivity closely matches the measured value, it can be assumed that the calculated impedance of this structure will more accurately represent the real value. Second, if the analytical method permits, a “thick” membrane can

be inserted into the computation [41]. The thickness of the thick membrane should be chosen as the smallest reasonable dimension that can be included in the analysis, while the total cavity height should remain unchanged. This can also be thought of as only partially filling the microshield cavity with a very low dielectric constant material. Once again, the dielectric constant of the layer must be adjusted until the computed  $\epsilon_{r, \text{eff}}$  matches a measured value. Note that whichever method is chosen, the procedure to arrive at the correct value for the dielectric constant of the filling material should be repeated for each geometry being studied. The  $\epsilon_{r, \text{eff}}$  of microshield lines is highly dependent on the aspect ratio of the conducting lines and a line with a different  $s/(s + 2w)$  ratio will require a different dielectric filler material.

Microshield lines can be designed to realize characteristic impedances ranging from around  $50 \Omega$  to as high as  $300 \Omega$ . For filter and other planar circuit applications, it is more logical to work with a higher central impedance than the nominal  $50 \Omega$  probe impedance, since this falls at the lower end of the possible impedance range.

The successful performance of the microshield line at *W*-band frequencies is validated by the results of the MultiCal calibration software. The measured effective relative permittivity for a  $92 \Omega$  microshield line with a slot separation of  $220 \mu\text{m}$ , a slot width of  $50 \mu\text{m}$ , and a cavity height and width of  $350 \mu\text{m}$  and  $1.2 \text{ mm}$ , respectively, is plotted in Figure 2.3. This curve shows that the membrane dielectrics do have some effect on the performance of the line, since the measured value of  $\epsilon_{r, \text{eff}}$  is not unity, but 1.08. The effective permittivity curve also remains very nearly constant over the measurement band. This indicates the low-loss, low-dispersion characteristics of the line, and establishes the efficacy of the microshield line for use in planar *W*-band applications.

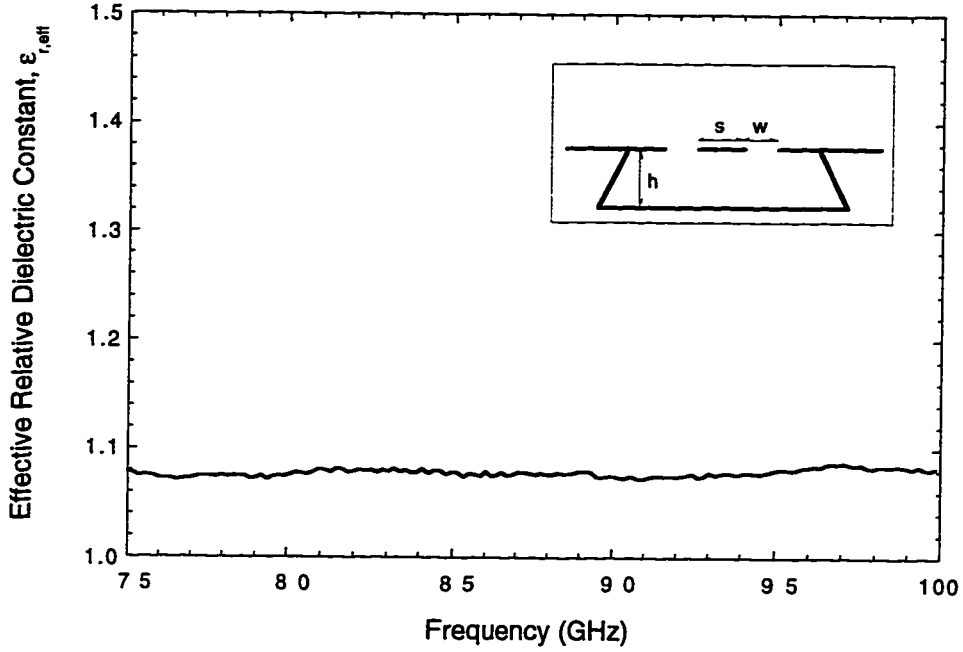


Figure 2.3: Measured effective relative permittivity of a microshield line in W-band. Dimensions in  $\mu\text{m}$  are:  $s = 220$ ,  $w = 45$ ,  $h = 355$ . Data obtained using NIST's MultiCal (DEEMBEd).

### 2.2.1 Fabrication

Fabrication of the membrane supported microshield line can be accomplished using the methods presented in Section 2.1.1, with the addition of an extra step that produces the metallized cavity underneath the line. When metallizing the cavity, it is desirable to allow the top surface ground metallization to overlap with the lower ground metallization in order to form a capacitive short across the membrane between the two metal films. However, this same capacitive short must not be allowed to occur between the lower ground metal and the signal line of the microshield. To avoid this, the lower metal must be patterned so that it is only deposited on the sides of the cavity. The metallization must occur after the cavity has been etched, so no photolithographic methods can be applied. Instead, a mechanical “shadow” mask must be placed



over the cavity opening during electron beam evaporation of the metal [18]. This method is not entirely precise, however, so dimensional allowances must be included between the edge of the cavity and the edge of the lower ground plane. As illustrated in Figure 2.4, an overlap of 200-300  $\mu\text{m}$  is usually sufficient to allow the mechanical shadow mask to perform its task. Final enclosure of the lower cavity may be accomplished by attaching the microshield line wafer to a second metallized wafer using silver epoxy or some other adhesive.

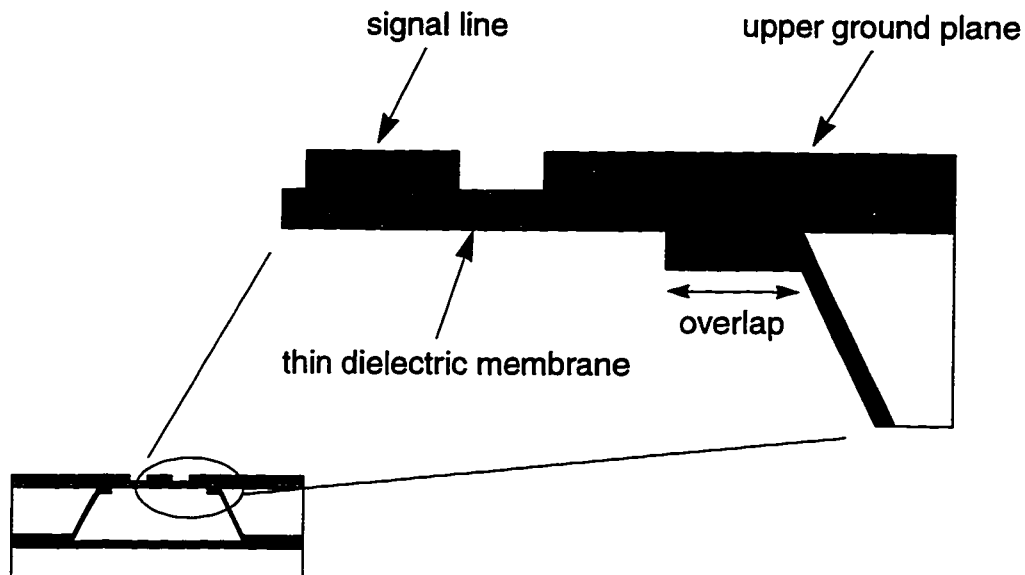


Figure 2.4: Detail of the metallization pattern inside the micromachined cavity. Note the overlap of the upper and lower metallization patterns. This allows a capacitive short to form across the thin dielectric membrane between the two ground planes.

### 2.2.2 Grounded-CPW to Microshield Transitions

The membranes are not strong enough to withstand the pressure of repeated on-wafer probing, so wafer probes must be placed on the silicon support rim of the membrane structure. For *W*-band measurements, it was found that the best results were achieved when the wafer probes were set as close as

possible to the membrane edge. Furthermore, an impedance transformer must be used to reduce the matching problems between the high-impedance membrane circuits and the  $50\ \Omega$  test system impedance. For  $92\ \Omega$  microshield line, a simple quarter-wavelength matching transformer with an impedance of  $68\ \Omega$  provides a suitable solution.

## 2.3 Shielded Membrane Microstrip

### 2.3.1 Description

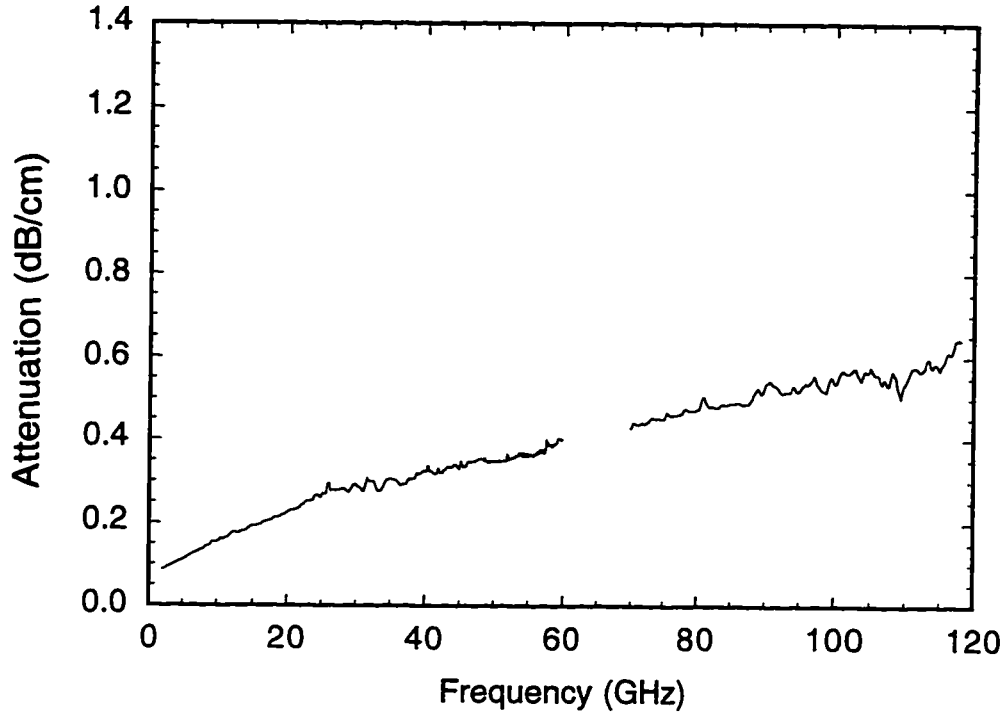
Thin dielectric membranes provide the foundation for shielded membrane microstrip (SMM) lines. The SMM line is a shielded microstrip line with an air dielectric, and possesses the low dispersion and low dielectric loss characteristic of the microshield line. The geometry of SMM resembles that of an air-stripline, but the conducting strip is not positioned symmetrically between the two ground planes. Assembly of the SMM lines requires multiple micromachining steps, including the incorporation of a second micromachined wafer to form a shield. This type of micromachined shielding cavity has been used with completely shielded CPW structures on silicon substrates [17], and with membrane-supported air-stripline geometries [16]. For SMM, the micromachined cavity actually provides the ground plane for the microstrip signal, as seen in the three-wafer assembly illustrated in Figure 1.3. The middle circuit wafer rests on a metallized carrier wafer which acts to provide a shielding cover for the microstrip. The ground plane, then, resides *above* the signal line since the micromachined cavity wafer rests on top of the entire structure. The cover height,  $h_c$ , is determined by the thickness of the circuit wafer, and the signal-to-ground separation,  $h$ , is determined by the etched depth of the micromachined cavity in the ground plane wafer. As with conventional microstrip lines,

the width,  $w$ , of the central conducting strip can be varied to realize the desired characteristic impedance.

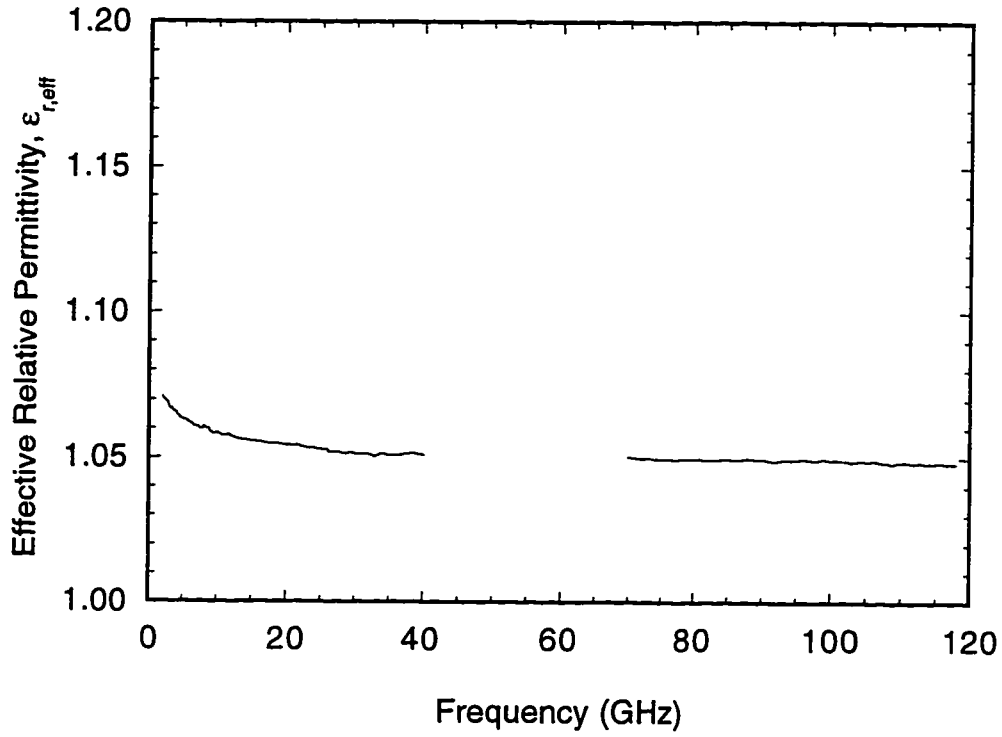
Figure 2.5(a) shows the data extracted from MultiCal for the attenuation constant of an SMM line with a 50  $\mu\text{m}$  ground height and a conductor width of 98  $\mu\text{m}$ . The characteristic impedance of this structure is calculated to be 90  $\Omega$ , and, as the plot shows, the attenuation in this line is very low, reaching a maximum value of only 0.6 dB/cm at 120 GHz. In addition, as Figure 2.5(b) illustrates, the line has extremely low dispersion, with an  $\epsilon_{r,\text{eff}}$  of only 1.05 that remains nearly constant over the measurement band. (The gap in the data between 60 and 70 GHz results from limitations of the measurement apparatus, as discussed in Section 2.1.3.) The slightly elevated values seen below 20 GHz are non-physical; they reflect the assumption that the propagation constant of the line is entirely real. This assumption becomes invalid at low frequencies, where the losses in the measurement apparatus are more significant compared to the wavelength of propagation.

### 2.3.2 2-D Analysis of SMM line

Impedance calculations for the SMM line can be done easily with 2-D static methods, but must take into account both metallized shielding surfaces and the membrane. As with the microshield line, it is useful to also consider the effects of the membrane by using a thick membrane or a low- $\epsilon_r$  substrate. When using *LineCalc* to synthesize SMM lines, there are several built-in models which can be adapted to accurately predict characteristic impedances. The simplest, perhaps, is the basic MLIN microstrip model. When using the MLIN element, a substrate dielectric constant value of around 1.1 is usually required, and the MCOVER option should be set to reflect the shielding height of the SMM cavity. In addition to the MLIN model, *LineCalc* also maintains a



(a)



(b)

Figure 2.5: Measured (a) attenuation constant and (b) effective relative permittivity of SMM line ( $w = 98 \mu\text{m}$ ,  $h = 50 \mu\text{m}$ ,  $h_c = 550 \mu\text{m}$ ).

suspended substrate model (SSSUB) and an offset stripline model (SSUBO). Both of these elements have the advantage of placing the dielectric in the correct position relative to the conducting strip; whereas the MLIN model places the substrate between the signal line and the ground plane, the others can be configured place the substrate between the signal line and the shielding plane. The SSSUB element most closely resembles the actual SMM structure, since a thick membrane can be included, rather than a full-thickness dielectric substrate.

### **2.3.3 Fabrication**

Fabrication of the circuit wafer in the SMM structure can be achieved using the basic micromachining techniques already described. Formation of the ground plane wafer requires specific attention, though, since the issues of ground plane height and wafer probe access must be addressed.

#### **Micromachined Ground Plane Cavities**

To achieve the desired SMM characteristic impedance, the depth of the cavity must be controlled precisely, and this is done by timing the etch. As discussed in Section 2.1.1, the silicon etch rate for the EDP process has been experimentally determined to be approximately 1.2  $\mu\text{m}/\text{min}$ . Rate dependencies on temperature and etch area create difficulties in precise control of the depth of the shielding cavity, but it is believed that an accuracy of  $\pm 5 \mu\text{m}$  can be obtained. For a nominal cavity depth of 100  $\mu\text{m}$ , FDTD analysis shows that a variation in etch depth of  $\pm 5\%$  will cause less than 1% deviances in the center frequency and bandwidth of a 4.3% bandwidth filter centered at 94 GHz. For future applications, it may be possible to optimize an etching process using KOH or TMAH as the ground plane cavity etchant. Both of these

etchants provide very smooth surface finishes (even smoother than EDP many cases) and they proceed at slower rates, which can make it easier to control timed etch steps. The TMAH system is preferred, since a silicon dioxide film can be used to mask the etchant. Difficulties in maintaining uniform etch rates across the sample must be addressed, however.

### Wafer Probe Access Windows

Formation of windows for on-wafer probing access to the circuits can be accomplished by a two-step process which etches the ground plane wafer from both sides and simultaneously forms both the ground plane cavities and the probe windows [17]. This process is outlined in Figure 2.6 and can be applied using a standard thickness, single-side polished silicon wafer with silicon dioxide masking layers on both sides. It begins with the deposition of a Cr/Au 250/2000 Å metal layer on the front (polished) side of the wafer. The shielding cavity patterns are defined on the front side using a photoresist mask and the appropriate metal etchants to remove the Au and Cr. Then, with the back side of the wafer protected by photoresist, the wafer is placed in a BHF solution and half of the front side oxide is removed (Figure 2.6(a)). Next, an IR alignment is used to define the probe window pattern on the unpolished (back) side of the wafer. With the front side now protected by photoresist, the back side oxide is removed in BHF to expose the silicon surface (Figure 2.6(b)). The wafer is then placed in EDP, and the probe windows are selectively etched from the backside first. For this first etch step, the etching time must be chosen such that the probe windows etch to a depth corresponding to the wafer thickness minus twice the desired ground plane cavity height (Figure 2.6(c)). After etching for the appropriate amount of time, the wafer is removed from EDP, cleaned, and placed in the BHF. At this point, the front side oxide will be

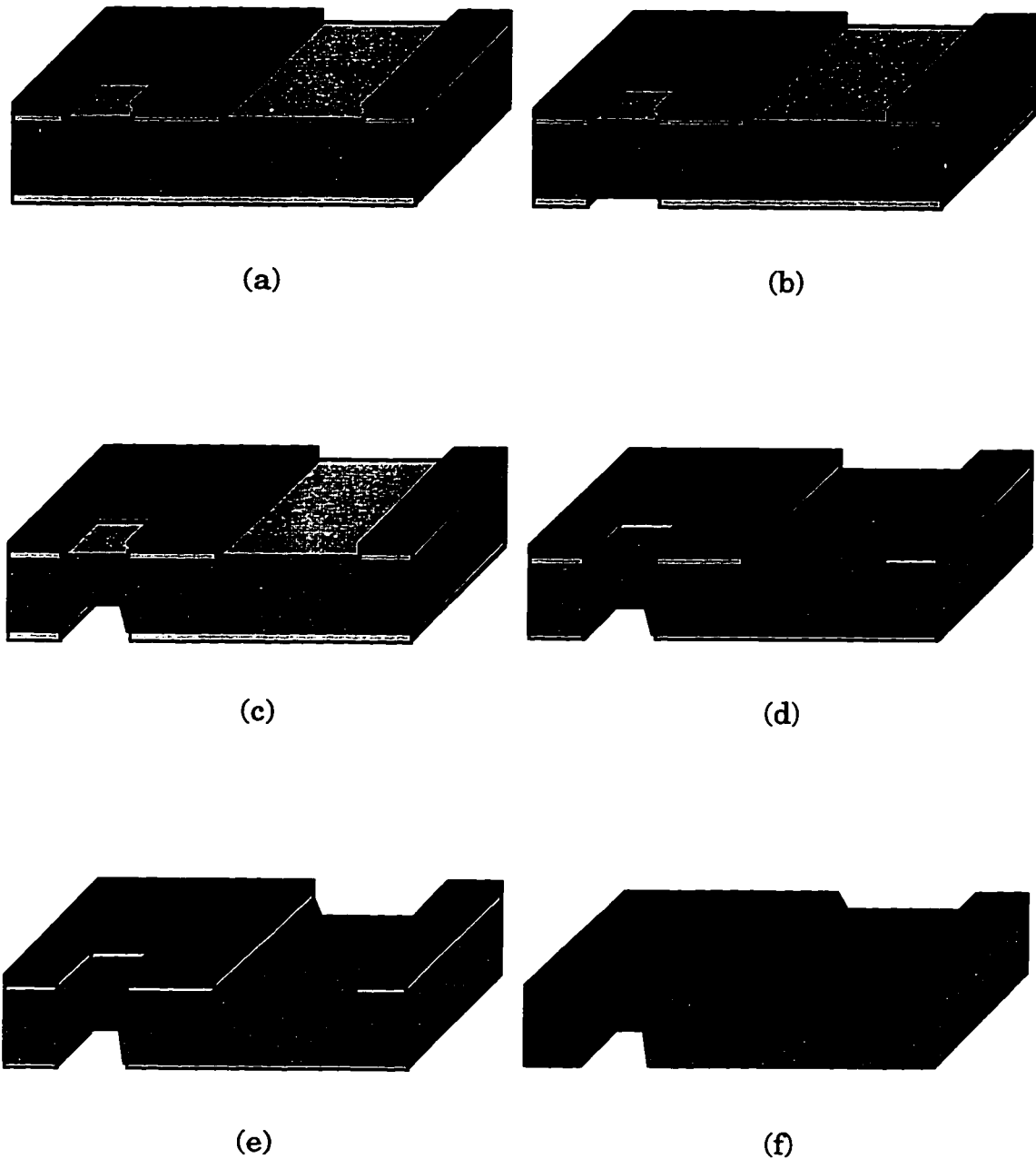


Figure 2.6: Fabrication sequence for the two-sided etch of the micromachined ground plane wafer. (a) Pattern front side metallization and etch half of oxide. (b) Etch back side oxide patterns. (c) Etch Si from back side only. (d) Remove remaining front side oxide. (e) Etch Si from front and back simultaneously. (f) Remove masking layers and metallize.

removed, and, since it is only half as thick as the back side oxide, the probe window pattern on the back side of the wafer will remain intact (Figure 2.6(d)). When the wafer is returned to the EDP etchant, both sides will etch simultaneously. The etching time for this step determines the final ground plane height for the SMM line, and must be controlled precisely (to within  $\pm 1$  minute) to achieve the desired result (Figure 2.6(e)).

After completion of the second etch step, the ground plane wafer must be stripped of all masking layers, cleaned in a “piranha etch” solution ( $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$  1.2:1) for 20 minutes, and then re-metallized with a Ti/Al/Ti/Au 500/10000/500/4000 Å sequence in an electron beam evaporator (Figure 2.6(f)). The ground plane wafer is now ready for attachment to the circuit wafer. Alignment of the ground plane wafer to the circuit wafer is required, so that the etched windows permit access to the GCPW probe pads, and the micromachined ground plane cavities correspond to the appropriate SMM signal lines. The alignment can be accomplished by etching windows in the ground plane wafer that correspond to alignment markings printed on the circuit wafer. The alignment is then performed manually, and can be tedious and difficult to accomplish accurately. Significant improvement in alignment accuracy and ease of alignment can be realized by applying the microsphere self-alignment technique described in Appendix B. For completion of the circuit fabrication, the two-wafer assembly must be placed on a metallized carrier wafer to provide the lower shielding plane.

### 2.3.4 Grounded-CPW to SMM Transitions

For on-wafer probing of SMM line structures, consideration must be given to the manner in which the grounded-CPW (GCPW) geometry of the probe pad can be transformed to provide a field distribution compatible with the SMM



line. The propagating mode of the SMM line is characterized by an electric field orientation which is primarily vertical with respect to the plane of the signal line. Conversely, a horizontally opposed electric field orientation prevails in a CPW-style wafer probe. One possible candidate for a transition between these two modes is the microshield line, which has shown the ability to support both CPW-like and a microstrip-like modes [40]. The ratio of slot width to ground plane height determines whether a microstrip mode or a CPW mode is excited on the line. When the slot width is large compared to the ground plane height, the propagating electric fields tend to concentrate under the center conductor of the structure with a vertical orientation which is very similar to the dominant mode of microstrip propagation. Conversely, when the slots are narrow with respect to the ground plane height, the electric fields adopt a horizontally opposed orientation which is characteristic of the odd mode in CPW lines. This is exemplified in Figure 2.7 by the plot of the microshield line characteristic impedance versus normalized slot width. For smaller  $w/h$  ratios, the impedance is very sensitive to changes in the slot width, indicating a strong horizontal component in the electric field and a CPW-like mode of propagation. As  $w/h$  increases, however, the dependence on the slot width decreases, and the impedance gradually approaches that of a microstrip line with the same  $s/h$  ratio.

A tapered section of microshield line was designed to implement a transition between the two different modes of the CPW wafer probe and the SMM line. The design solves the impedance mismatch between the  $50\ \Omega$  wafer probe and the  $92\ \Omega$  SMM line by incorporating a Klopfenstein impedance matching function into the taper. The Klopfenstein impedance taper is widely used since it is an approximation to an infinite order Chebyshev matching transformer that achieves a desired level of matching in the shortest possible distance [42].

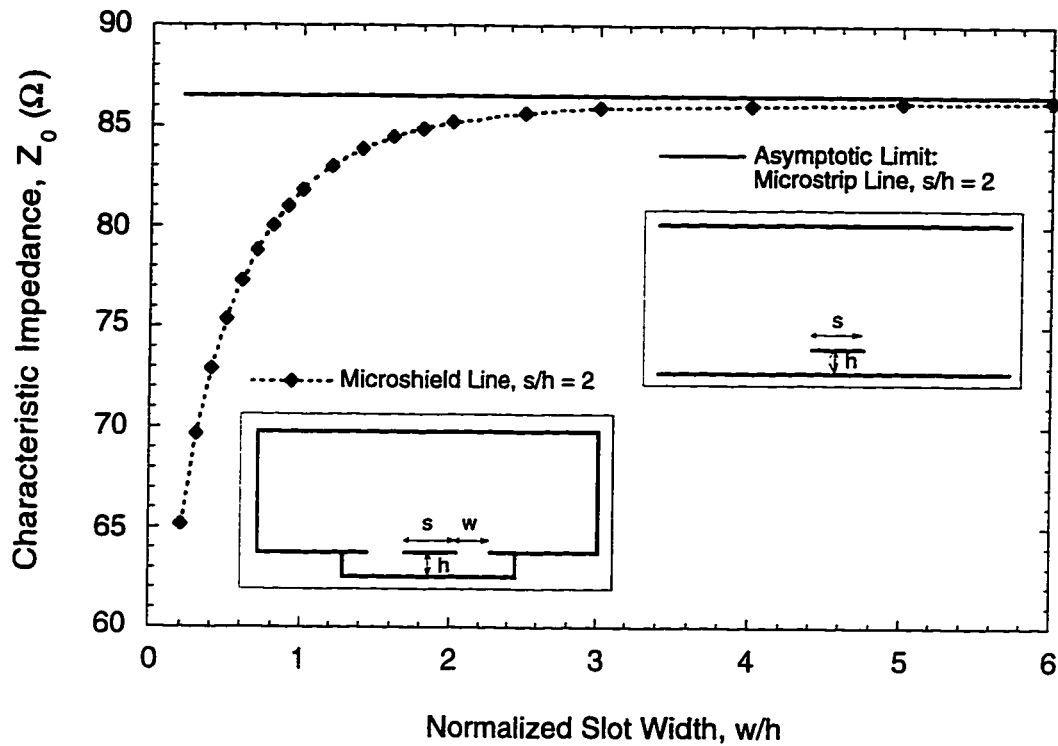


Figure 2.7: Calculated impedances for a microshield line with an upper shield. The solid line indicates the calculated impedance of a microstrip line with an equivalent  $s/h$  ratio.

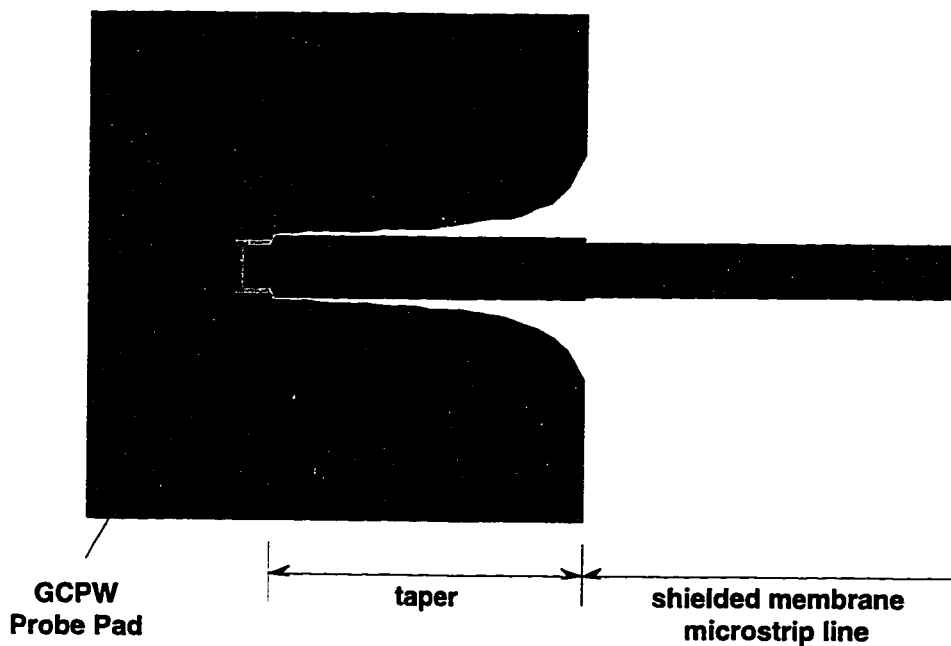


Figure 2.8: Layout of the Klopfenstein taper used as a transition from the GCPW probe pad to SMM line. Only the probing area is supported the silicon support rim.

A published algorithm was used to calculate the necessary impedance distribution at discrete points along the taper [43], and data from Figure 2.7 were used to choose the width of the microshield line center conductor to be very close to the width of the desired SMM line. The slot widths of the microshield line were varied to realize the tapering function. A schematic of the microshield taper is shown in Figure 2.8, including the GCPW probe pad and the SMM line. At each end of the taper, the geometry of the microshield line provides an electric field distribution that is compatible with the appropriate type of transmission line.

## 2.4 Conclusions

Microshield line and shielded membrane microstrip represent two types of membrane-supported transmission line geometries that show promise for use as *W*-band waveguiding structures. The lines are realized using bulk Si micro-machining techniques which are easily incorporated into the fabrication process. Thin dielectric membranes provide the means to support the lines in air, without the need for conventional microwave circuit substrates. The removal of the dielectric substrate produces low-loss, low-dispersion propagation characteristics which are necessary for the development of *W*-band circuits.

## **CHAPTER III**

# **MICROMACHINED W-BAND FILTERS AND FILTER ELEMENTS**

### **3.1 Introduction**

The utility of a transmission line structure is judged not simply by its ability to propagate electromagnetic waves from point A to point B. This is especially true for planar architectures, where the transmission line becomes an important circuit design tool. Microwave circuits based on transmission line discontinuities, resonators, and coupling elements form the basis for communications, radar, and remote sensing systems. The performance of the transmission line ultimately dictates the performance of the overall system.

Fabrication of microwave filters using micromachining technologies and membrane-supported transmission lines has been very successful [10],[52]. There has even been a report of the first ever planar filter at submillimeter-wave frequencies [13]. In order to demonstrate the capabilities of membrane-supported lines at W-band frequencies, several filters and filter elements were fabricated and studied. The design of these circuits was accomplished primarily with ideal transmission line theory and quasi-static methods, with full-wave analysis techniques employed where necessary to ensure the accuracy of the designs [17],[44]. First, 90 GHz low-pass filters were implemented using

the microshield line geometry. Comparison of these filters to conventional substrate supported filters was achieved through the use of FDTD simulations.

Second, several structures were designed using the SMM transmission line structure. An end-coupled half-wavelength resonator was designed for 25 GHz operation, and showed excellent broad band performance all the way through the fourth resonance at 100 GHz. Extracted quality factors of this resonator show that the SMM line is limited only by conductor losses, and maintains very uniform propagation quality through a very wide bandwidth.

Finally, the SMM structure was also applied to the design of several coupled line band-pass filters. These filters, centered at 94 GHz, show some of the first planar filter results in *W*-band, and they perform at levels approaching those of rectangular waveguide band-pass filters.

Theoretical validation of the measurements is provided by the FDTD analysis technique. This method shows great flexibility and accuracy for *W*-band circuit analysis, and is used to simulate structures which are supported by both conventional GaAs substrates and the thin dielectric membranes. Results of these simulations allow for a direct comparison between membrane supported circuits and conventional planar circuits.

## **3.2 Low Pass Filters**

### **3.2.1 Circuit Design**

A low-pass filter designed using a stepped impedance implementation of a 7-section 0.5 dB equal ripple Chebyshev filter prototype is shown in Figure 3.1 [45]. The high and low impedance sections of the filter correspond to 277  $\Omega$  and 63  $\Omega$ , respectively, while the feed line and filter center impedance are designed to be 92  $\Omega$ . The filter section lengths were initially approximated

by means of equivalent circuit models for short transmission line sections [46]. At this point, these values for the filter sections are very rough estimates, and an accurate simulation of the filter response needs to be performed in order to select the final dimensions of the filter stages.

A quasi-static simulation was performed using *Puff* [36], but it was found that the microstrip models available in *Puff* did not adequately predict the parasitic effects of the step-changes in the microshield center conductor. Even though the ideal transmission line theory is the same for both mediums, the parasitics associated with a microstrip step-in-width are very different from those in the case of a microshield transmission line (especially at higher frequencies). Primarily, the difference lies in the proximity of the microshield upper ground planes to the edges of the wide transmission line sections, but there is also the effect of the air dielectric in the microshield line to consider. The air dielectric does not act to confine the propagating fields below the conductor lines as is the case for a microstrip line on a higher dielectric substrate, and this creates the possibility that the parasitics at the junction will be almost entirely due to the upper ground planes, with very little effect from the lower ground plane.

As a result of these complications, a full-wave analysis of the filter was required for the final step in the design sequence, and this was accomplished with FDTD simulations. These revealed that the filter cutoff frequency was lower than the desired 90 GHz value, so the filter section lengths were scaled appropriately to achieve the correct response.

### 3.2.2 Measurements

The measured response of the low-pass filter from 75-110 GHz is plotted in Figure 3.2 with results of the final FDTD analysis from 40-140 GHz. The filter

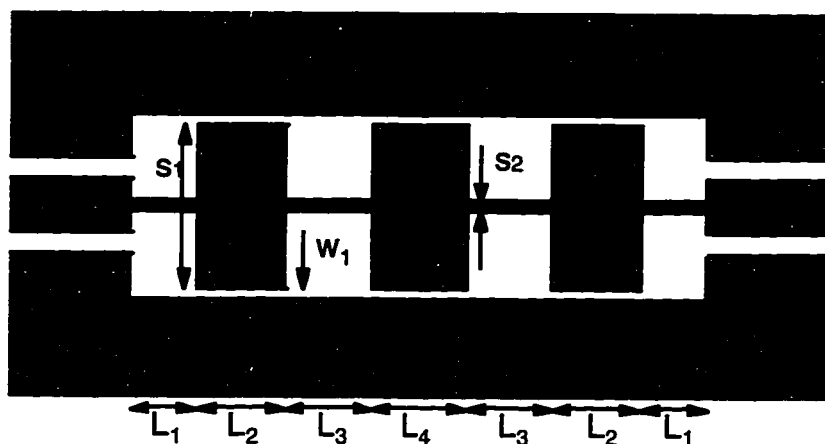


Figure 3.1: Circuit realization of a 7-section stepped-impedance low-pass filter in microshield line.

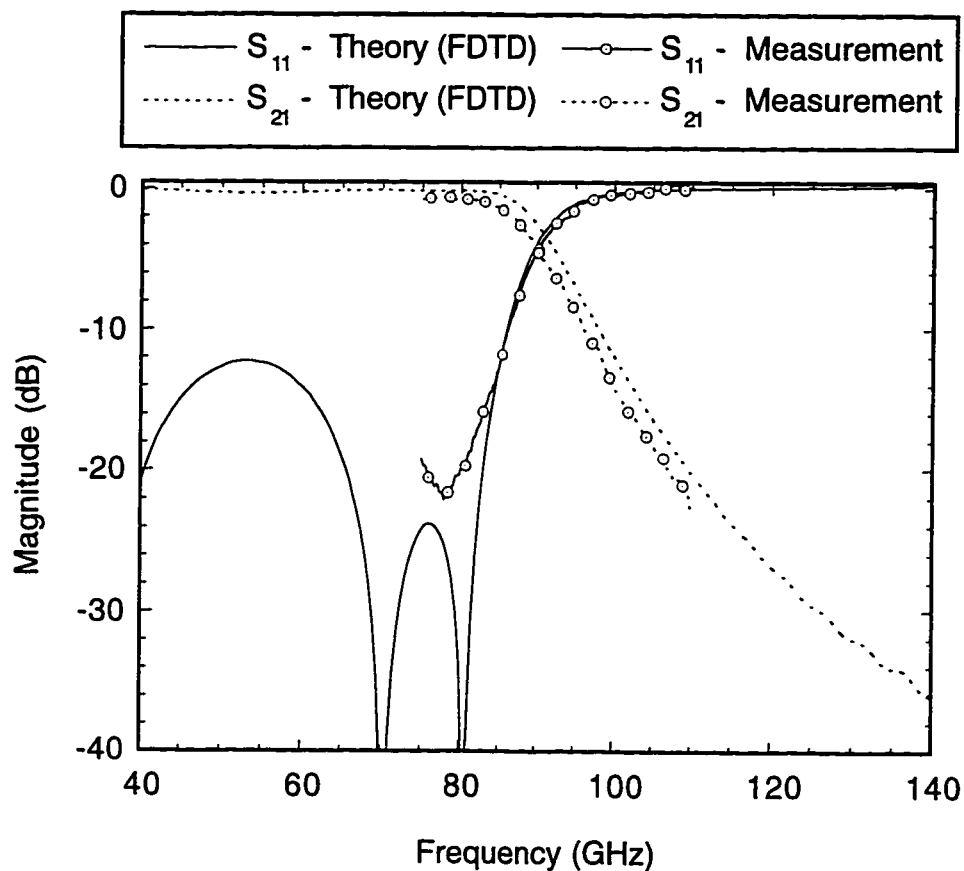


Figure 3.2: Measured results of a 90 GHz microshield line low-pass filter from 75 to 110 GHz compared to FDTD analysis from 40 to 140 GHz.

achieves a cutoff frequency of approximately 90 GHz, with 0.7 dB insertion loss at 80 GHz, and the FDTD technique accurately predicts the filter performance. The presence of the membrane is incorporated into the FDTD analysis using the thick membrane technique. A sheet of dielectric with a thickness of 44  $\mu\text{m}$  (the mesh subsection size in the vertical direction) is placed underneath the conducting lines of the structure. The relative dielectric constant of the thick membrane is set to 1.16, so that the effective dielectric constant predicted by the FDTD analysis corresponds to the measured value of 1.08.

### 3.2.3 A Low-Pass Filter on GaAs

An FDTD analysis was also performed for an equivalent low-pass filter designed using grounded-CPW (GCPW) on a 100  $\mu\text{m}$  thick GaAs substrate ( $\epsilon_r = 12.7$ ). This filter was synthesized using the same Chebyshev prototype values and short transmission line models as used in the design of the microshield line filter, and impedances for the GCPW lines were found from a conformal mapping method calculation [34]. FDTD simulations were performed to scale the filter response to the desired 90 GHz cutoff frequency, but no further design optimizations were attempted. Dimensions are given for both low-pass filters in Table 3.1.

The microshield line filter provides 20 dB more out-of-band attenuation than the GCPW filter, and the return loss of the GCPW filter degrades with

Filter Type	$s_1$	$w_1$	$s_2$	$L_1$	$L_2$	$L_3$	$L_4$
Microshield	540	20	20	220	340	360	420
GCPW on GaAs	230	20	10	120	80	200	80

Table 3.1: Dimensions (in  $\mu\text{m}$ ) for the microshield low-pass filter and the low-pass filter on GaAs.



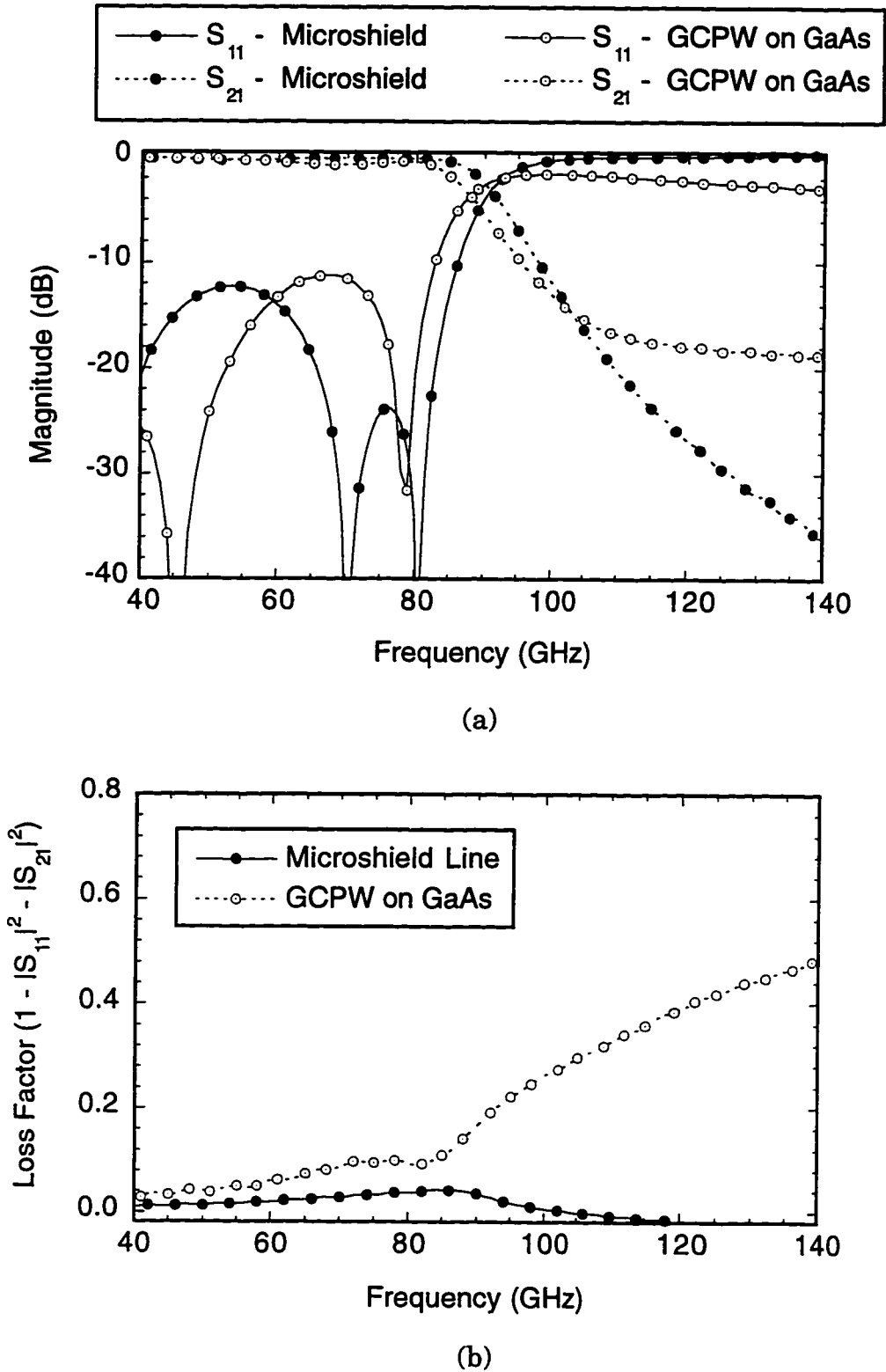


Figure 3.3: (a) Theoretical performance of a low-pass filter fabricated using both microshield line and GCPW on GaAs. (b) Comparison of radiation losses in the low pass filters of (a).

increasing frequency, while the microshield filter return loss remains high (See Figure 3.3(a)). The graph in Figure 3.3(b) explains that the poor performance of the GCPW filter above the cutoff frequency can be attributed to increased radiation losses, since the calculated loss factors do not include conductor or dielectric losses. Above 100 GHz the data for the microshield filter becomes negative due to numerical error in the FDTD simulation. It should be noted that while it is possible to improve the performance of the GCPW filter on GaAs, this requires extensive design iteration that was not performed for the purposes of this comparison. The GCPW filter shown here demonstrates the typical problems encountered when using traditional dielectric substrates such as GaAs.

### 3.3 An End-Coupled Half-Wavelength Resonator

#### 3.3.1 Introduction

A useful demonstration of the propagation characteristics of a transmission line can be accomplished by studying the measured performance of a resonator circuit. For planar transmission line geometries, it is very convenient to couple in and out of the resonator with a capacitive gap at each end of the structure. Accurate data on attenuation in the line can be obtained by measuring the quality factor of the resonator [47],[48].

The layout of a typical gap-coupled microstrip resonator is shown in Figure 3.4. The length of the resonator is chosen to be  $\lambda_g/2$  at the frequency of the desired first resonance, and the gaps are narrow enough that the peaks in the  $S_{21}$  response of the resonator are clearly detectable on the measurement apparatus to be used. In addition, the gaps should be wide enough to

keep the resonator lightly coupled to the input and output feed lines and reduce external loading.

Microwave resonators are described by the *quality factor*, or  $Q$ . The  $Q$  of a resonator is defined as the average amount of energy that is stored in the resonator divided by the amount of energy that is lost per second in the resonator. The quality factor, then, gives an indication of the internal losses in the resonator, and the  $Q$  of any resonant response of a transmission line structure can be found by measuring the insertion loss and 3 dB bandwidth of that resonance. When making microwave measurements, however, the resonator must be coupled to some external circuitry. When this is done, the apparatus that couples to the resonator “loads” down the structure by introducing external losses into the measurement. Therefore, the measurement results in the “loaded”  $Q$ , or  $Q_L$ , which includes both the unloaded  $Q$  and the “external”  $Q$ , or  $Q_e$ . The loaded  $Q$  is expressed in terms of the unloaded and external  $Q$ ’s as:

$$\frac{1}{Q_L} = \frac{1}{Q_e} + \frac{1}{Q} \quad (3.1)$$

In the case of the end-coupled resonator, the  $Q_L$  can be determined simply by measuring the 3 dB bandwidth of the  $S_{21}$  response at the resonant frequency and applying Eqn. 3.2.

$$Q_L = \frac{f_0}{\Delta f_{3 \text{ dB}}} \quad (3.2)$$

Finally, the  $Q_e$  can be determined by the measured loss in the resonator:

$$S_{21}(\text{dB}) = 10 \cdot \log_{10} \left( \frac{Q_L^2}{Q_e^2} \right) \quad (3.3)$$

### 3.3.2 Circuit Fabrication and Measurement

In order to study the performance of the shielded membrane microstrip line, a capacitively coupled section of line was designed to resonate at 25 GHz. The impedances of the resonator and the input/output feed lines were chosen to be  $90\ \Omega$ , and dimensions of the transmission line were selected using the suspended substrate line model available in *LineCalc*. The actual resonator is supported on a membrane with a  $50\ \mu\text{m}$  ground plane spacing and a  $500\ \mu\text{m}$  shielding cover. The suspended substrate line model used a  $10\ \mu\text{m}$  thick dielectric layer with  $\epsilon_r = 7$  to represent the membrane, and predicted that a  $140\ \mu\text{m}$  wide line has a characteristic impedance of  $90\ \Omega$ , and an effective relative dielectric constant of 1.06. The resonator length was therefore chosen to be 5.7 mm and the coupling gap widths were set to  $15\ \mu\text{m}$ .

The SMM resonator was characterized with the help of the TRL calibration scheme and wideband Klopfenstein matching tapers. Measurements were taken from 2-60 GHz and from 70-118 GHz as shown in Figure 3.5. The four resonances occur at 25.05 GHz, 50.17 GHz, 75.32 GHz, and 100.46 GHz.

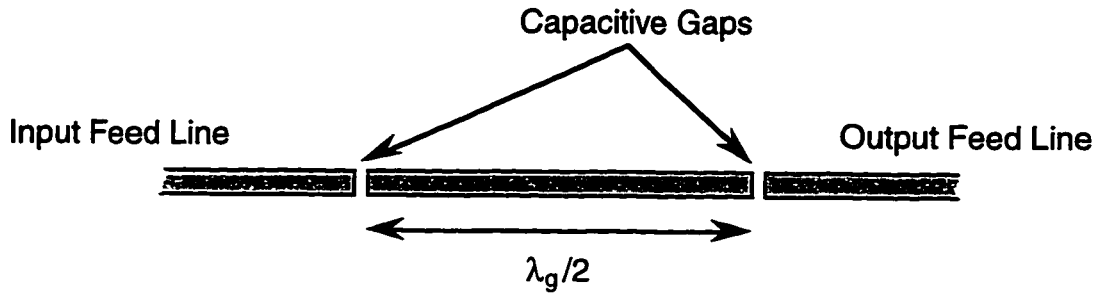


Figure 3.4: A capacitively coupled half-wavelength transmission line resonator.

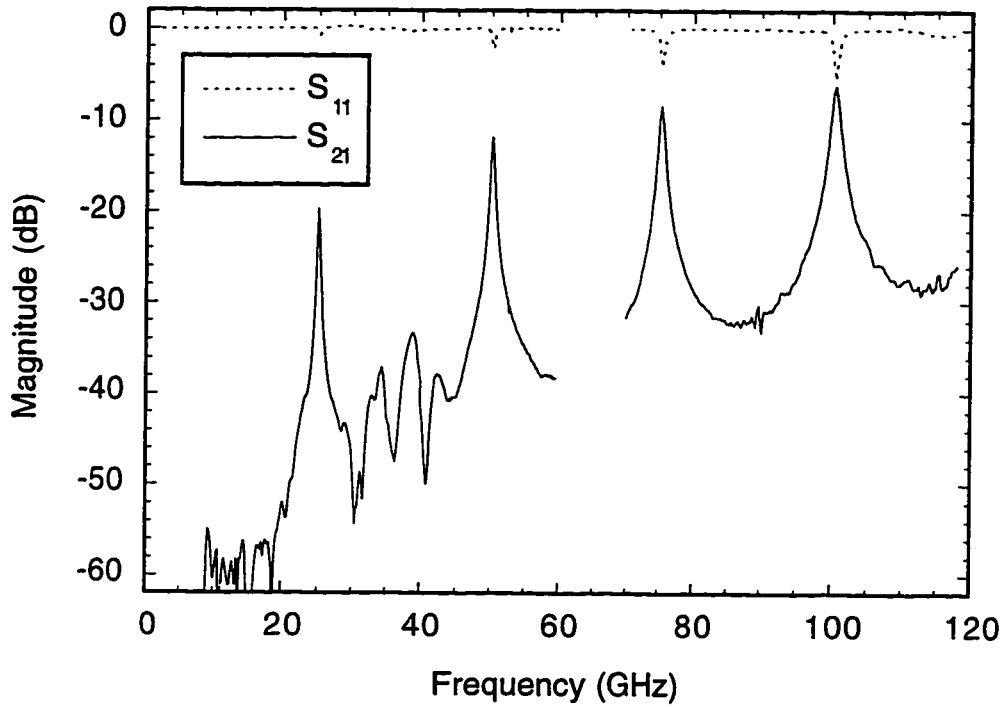


Figure 3.5: Measured response of a capacitively coupled half-wavelength SMM resonator from 2-118 GHz.

### 3.3.3 Quasi-Static Model of the Resonator Circuit

To obtain a more complete understanding of the gap-coupled resonator circuit, a quasi-static model was constructed using the *Touchstone/Libra* software. The model employed a microstrip model for the SMM transmission line. The suspended substrate model similar to the one used in *Linecalc* was not used since it does not incorporate conductor losses into the simulation. Conductor losses are an important part of the resonator's performance, since they determine the value of the  $Q$  for each resonance. An accurate simulation of the losses and phase delay in the SMM resonator was constructed by using a microstrip line of the same width as the actual SMM line (140  $\mu\text{m}$ ) and a 50  $\mu\text{m}$  thick substrate with a dielectric constant equal to 1.08. The microstrip model also included a 500  $\mu\text{m}$  shielding cover, and this resulted in a line with  $\epsilon_{r,\text{eff}} = 1.05$ , which is similar to what was measured for the SMM line in this configuration.

The next component of the gap-coupled resonator model involved constructing an equivalent circuit representation of the capacitive gaps at the ends of the resonator. In this case, the available *Libra* model for a microstrip gap did not provide an accurate simulation of the SMM gaps used in the measurement for two reasons. First, there is no way to incorporate the capacitance of the shielding cover in the gap model available in *Libra*. Second, the capacitance of the gap is affected to a large degree by the location and permittivity of the membrane. The second cause for failure was the more significant of the two, and the reasons for this can be understood by studying the equivalent circuit model seen in Figure 3.6. The model employs the classic  $\Pi$ -equivalent circuit that can be applied to any ideal, lossless, reciprocal, 2-port network. In the case of the gap model, capacitors have been used for all three of the impedance elements [49],[50]. The gap capacitance  $C_g$  can be thought of as the cou-

pling directly between the two open ends of the SMM lines. Similarly, the stray capacitances  $C_s$  can be thought of as representing the “length extension” effect commonly seen in microstrip open circuits as a result of the fringing capacitances from the end of the line to the ground plane and shielding cover.

For the SMM gap, the values of the three capacitances in the equivalent circuit are quite different from those calculated for the microstrip gap model [51]. Even when the dielectric constant of the substrate is selected to give the same  $\epsilon_{r,\text{eff}}$  as the measured value, the differing positions and values of the dielectric layers in the two geometries are significant enough to produce very different equivalent circuit values in the gap model.

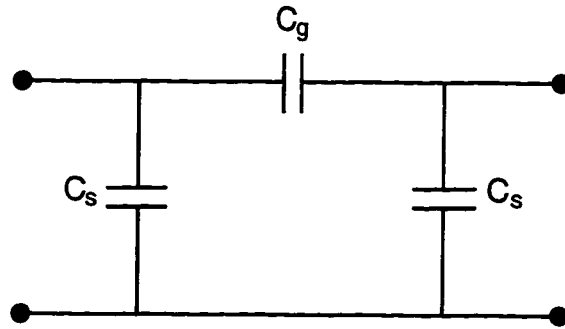


Figure 3.6: The  $\Pi$ -equivalent circuit used to model the capacitive gaps in the SMM resonator circuit.

	Gap Capacitance $C_g$ (pF)	Stray Capacitance $C_s$ (pF)
Microstrip Gap (fit to Libra data)	$1.47 \times 10^{-3}$	$1.94 \times 10^{-4}$
SMM Gap (fit to measured data)	$2.51 \times 10^{-3}$	$6.45 \times 10^{-4}$

Table 3.2: Extracted capacitance values for the  $\Pi$ -equivalent circuit elements of the microstrip gap and the SMM gap.

As an example of this, a circuit using the microstrip gap element from *Libra* was constructed and then the capacitive components of a corresponding  $\Pi$ -equivalent circuit were determined through the optimization routines in *Libra*. Then, the capacitance values in the  $\Pi$ -equivalent circuit were varied to allow the quasi-static model to produce the same response as the fabricated SMM resonator. The capacitance values extracted for each case are listed in Table 3.2 and the simulation results of the final equivalent circuit are shown compared to the measurements of the SMM resonator in Figure 3.7. It should

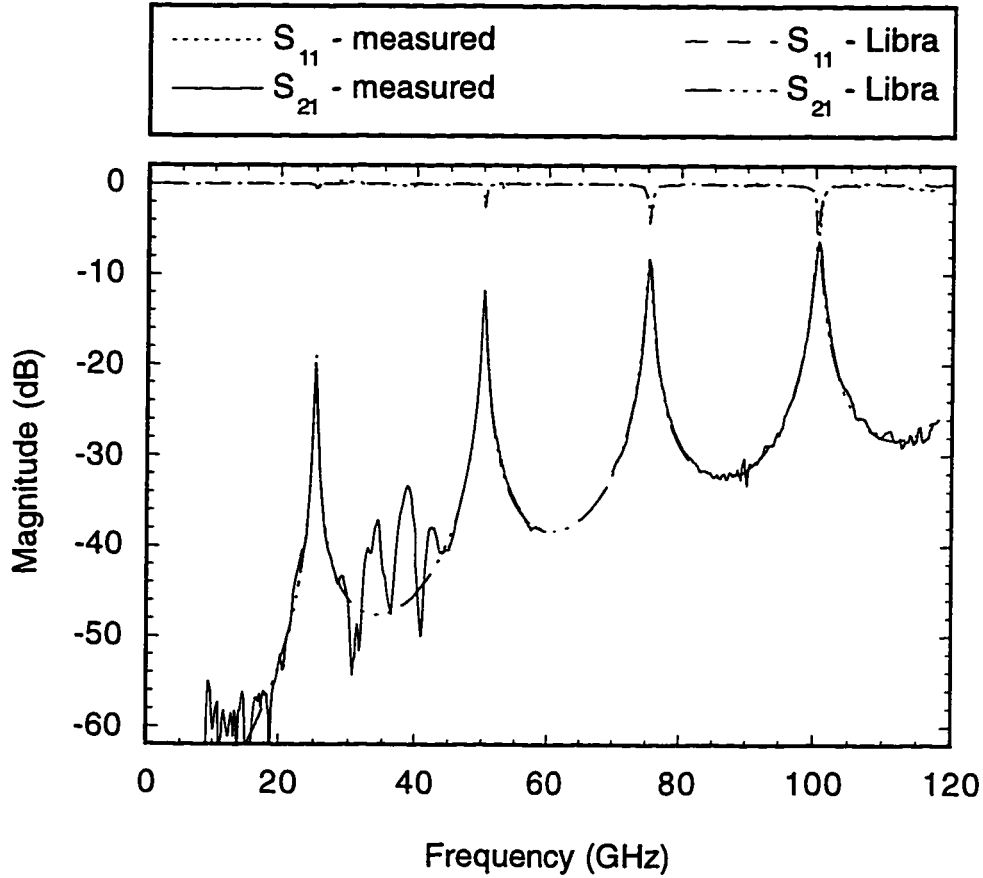


Figure 3.7: *Libra* simulation of the end-coupled resonator using the  $\Pi$ -equivalent circuit to represent the capacitive gaps in the SMM center conductor.



be noted that the values for the stray capacitance ( $C_s$ ) are extremely small, and quite sensitive to changes in the geometry. A small shift in resonant frequency related to a change in stray capacitance could be easily represented by a small change in the length of the resonator. The calculated  $C_s$  values are based on the microstrip line model used in the *Libra* simulation, and any errors in the phase length of the model will result in differing  $C_s$  values.

### 3.3.4 Analysis

More information can be extracted from the measured results by calculating the quality factors, or  $Q$ 's, associated with each resonance. For each resonance, the measurement was repeated with only a 4 GHz bandwidth to allow accurate determination of the minimum insertion loss and 3-dB bandwidth (Figure 3.8). Then, Eqn. 3.1 - Eqn. 3.3 were applied to find the values for the  $Q_L$ ,  $Q$ , and  $Q_e$  of each resonance, and these are listed in Table 3.3. Also included in Table 3.3 are the computed ratios for  $Q/Q_1$  and  $\sqrt{f_0/f_{0,1}}$ . Comparison of these ratios shows that the  $Q$  value of the resonator increases as  $\sqrt{f}$  for all four resonances. The expression for the  $Q$  of a transmission line resonator can be simplified, in the case of a low-loss transmission line, to the following relation:

$$Q = \frac{\beta}{2\alpha} = \frac{\pi}{\lambda\alpha} \quad (3.4)$$

From Eqn. 3.4 it can be seen that the  $Q$  of the resonator is inversely proportional to the loss and the guided wavelength in the transmission line. Since conductor losses increase as  $\sqrt{f}$ , and wavelength decreases linearly with  $f$ , the resonator  $Q$  itself will increase with  $\sqrt{f}$ , as long as there are no other loss mechanisms present in the circuit. Since the results of the SMM resonator measurements obey this trend, it can be concluded that the SMM transmis-

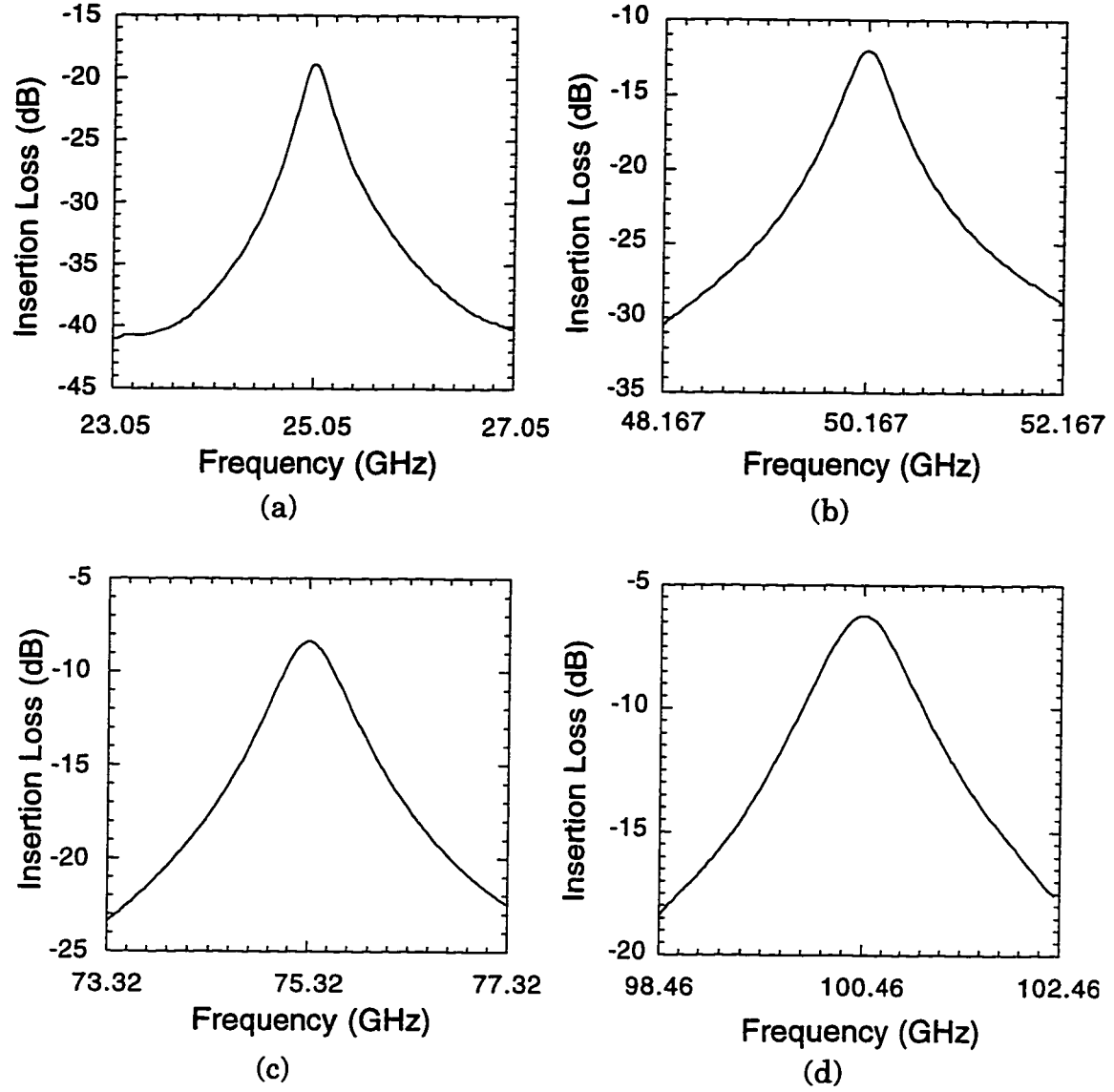


Figure 3.8: Individual measurements of the four resonances of the gap coupled half-wavelength SMM resonator.

$f_0$ (GHz)	$S_{21}$ (dB)	$Q_L$	$Q_e$	$Q$	$Q/Q_1$	$\sqrt{f_0/f_{0,1}}$
25.05	-18.86	83.5	732.296	94.246	1.00	1.00
50.17	-12.03	98.949	395.285	131.988	1.40	1.41
75.32	-8.36	100.830	263.991	163.141	1.73	1.73
100.46	-6.2	98.299	200.702	192.660	2.04	2.00

Table 3.3: Extracted data for the four resonances of the gap-coupled resonator.

sion line performs with virtually zero dielectric loss, and is limited by conductor loss only. This agrees with previously reported results for an air-stripline gap-coupled resonator [52].

### 3.4 Band-Pass Filters

#### 3.4.1 Circuit Design

The design of the band-pass filters begins with coupled-line resonator circuits derived from equal ripple Chebyshev prototypes [47]. Both three- and five-element filters of various bandwidths were designed based on a filter impedance of  $90\ \Omega$  [53]. A commercially available software package, PARFIL [37], was used to synthesize the filter geometry, using a ground plane separation and an upper shield separation of  $100\ \mu\text{m}$  and  $500\ \mu\text{m}$ , respectively. The PARFIL designs were verified by constructing a 2 GHz 47:1 scale model of a 4.3% bandwidth 5-element filter. The dielectric membrane was simulated by a  $76\ \mu\text{m}$  thick polyethylene sheet and the filter metallization patterns were defined using copper tape. Measurements of the 2 GHz filter revealed that the filter center frequency was not accurately predicted by PARFIL, but the measured bandwidth agreed well with the PARFIL data. The PARFIL design values for line widths and gap spacings were therefore used in the *W*-band implementation, but the resonator lengths were determined through experimental iteration on the low-frequency model (for dimensions, see Table 3.6). The desired filter center frequency was achieved when the resonator lengths were scaled to 94.7% of the original design lengths ( $710\ \mu\text{m}$  instead of  $750\ \mu\text{m}$ ), and this was confirmed with FDTD simulations at 94 GHz. The effect of the upper shielding cavity was also investigated using the microwave model, and the measured response of the filter changed significantly

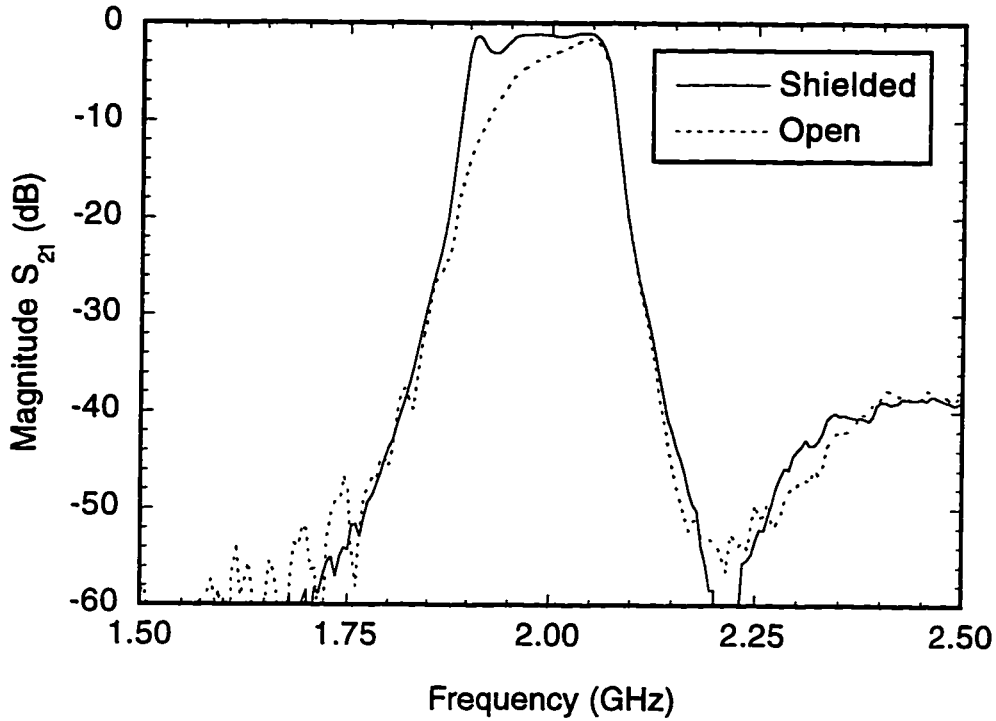


Figure 3.9: Measurements of a 47:1 scale model of a SMM band-pass filter. Comparison between shielded and open geometries shows the detrimental performance of the unshielded filter caused by radiation losses in the filter.

when the upper shielding surface was removed. Figure 3.9 shows that the low-frequency corner of the band-pass response became severely degraded due to radiation losses in the case of the open structure.

### 3.4.2 Measurements

Figure 3.10 shows a fabricated coupled-line band-pass filter. Three such filters were tested, and the measured results for all of them show low passband insertion loss, sharp roll-off, and high out-of-band attenuation. A filter designed for 4.25% bandwidth (pictured in Figure 3.10) achieves a passband insertion loss of 3.6 dB and a bandwidth of 6.1% at a center frequency of

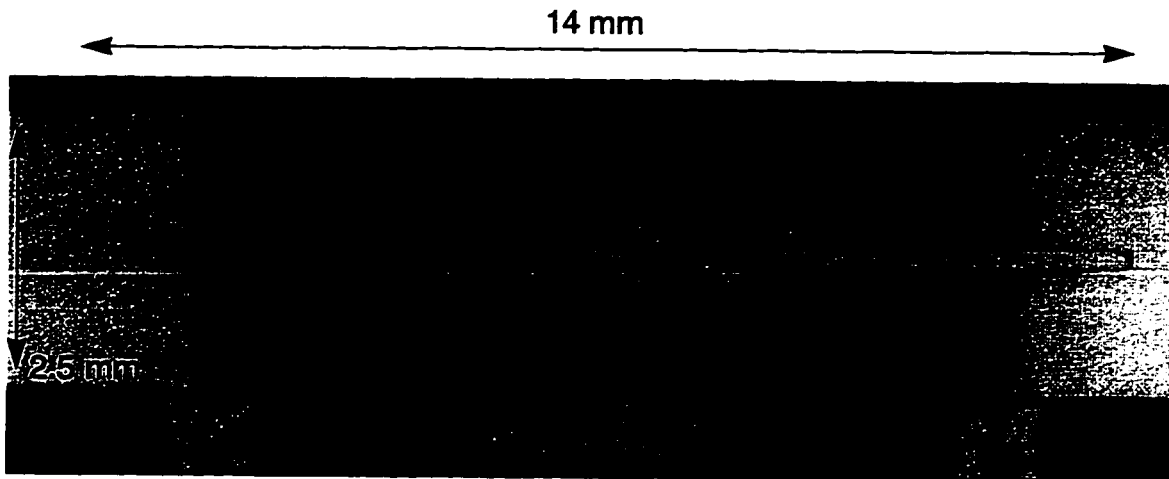
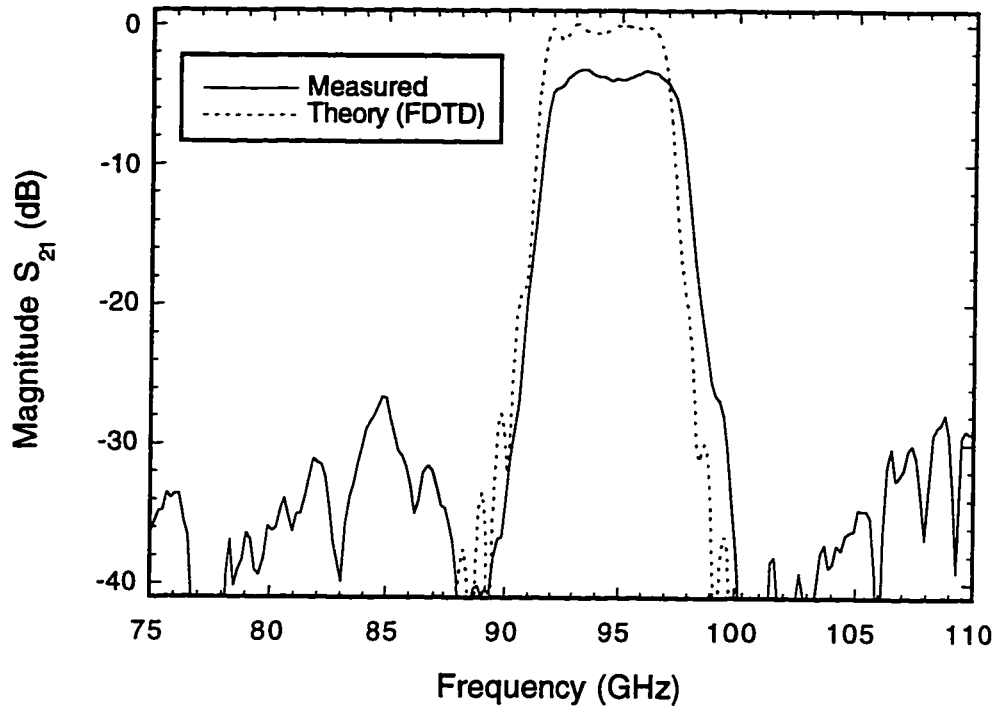


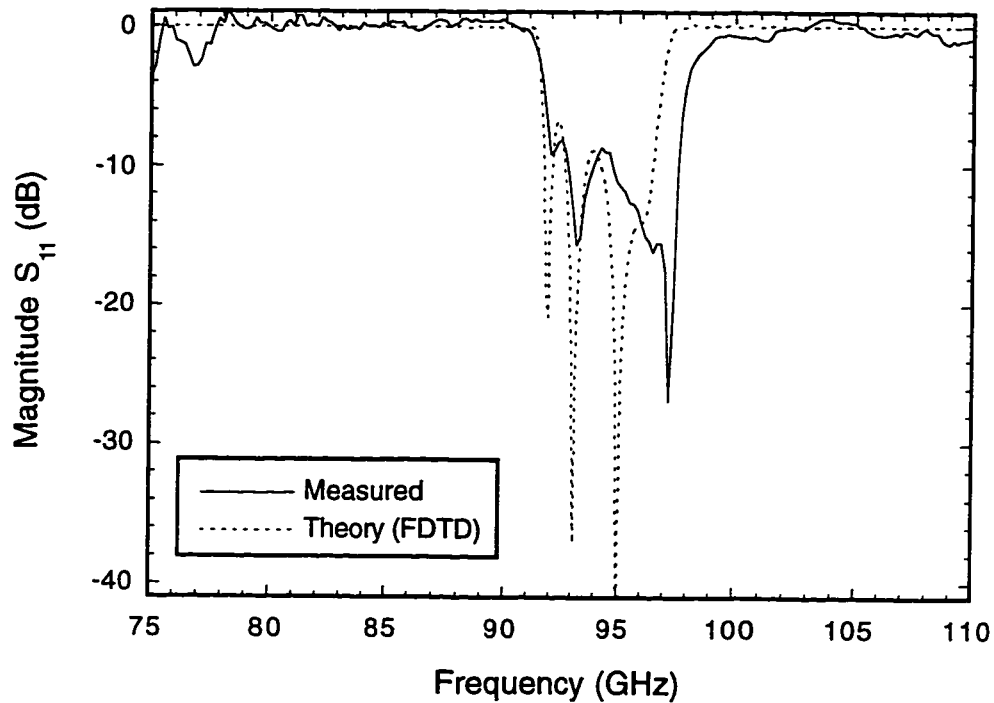
Figure 3.10: Photograph of a 5-section band-pass filter in shielded membrane microstrip (SMM). The ground plane cavity wafer has been removed for viewing, and the membrane portions of the circuit are visible as darkened regions compared to the lighter gray silicon support rim.

94.7 GHz (see Figure 3.11). Figure 3.12 shows the response of a 5-element filter designed for 8.5% bandwidth with a measured insertion loss of 2.2 dB and a 12.5% bandwidth centered at 95 GHz. Measurements of a 3-element, 12.8% bandwidth filter are shown in Figure 3.13. This filter has a measured insertion loss of 1.4 dB, a center frequency of 94.9 GHz, and a bandwidth of 17.7%. Dimensions of all three band-pass filters are listed for reference in Table 3.4.

Measured  $S$ -parameters of the band-pass filters reveal bandwidths which are wider than expected, due to the manner in which the SMM circuits were assembled. The attachment of the lower ground cavity wafer was accomplished by using small beads of photoresist as adhesive. These beads possessed non-zero thicknesses, however, and caused the distance from the signal line to the ground plane to be approximately  $20\text{ }\mu\text{m}$  farther than the  $100\text{ }\mu\text{m}$  depth of the ground cavity. This is verified by the good agreement with the FDTD analysis shown in Figure 3.11, which was performed using a ground



(a)



(b)

Figure 3.11: Measured S-parameters of an SMM coupled-line band-pass filter compared to FDTD results. The filter achieves 3.4 dB insertion loss and 6.1% bandwidth at 94.7 GHz. A 15  $\mu\text{m}$  thick dielectric sheet with  $\epsilon_r = 1.1$  is used in the FDTD analysis.

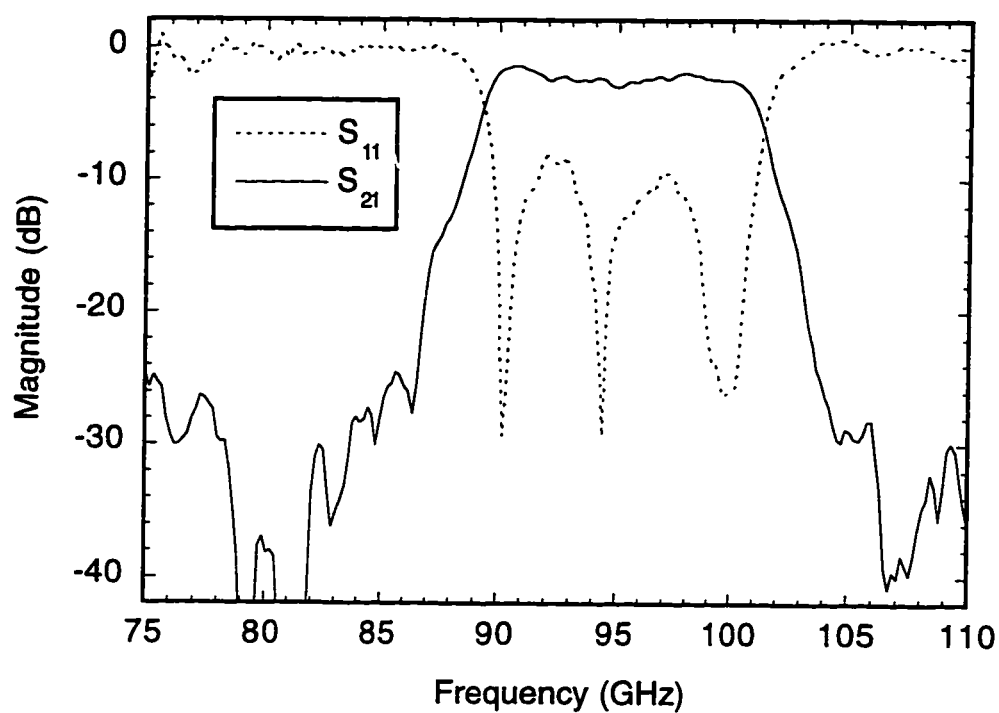


Figure 3.12: Measured S-parameters of an SMM band-pass filter with 2.2 dB insertion loss and 12.5% bandwidth at 95 GHz.

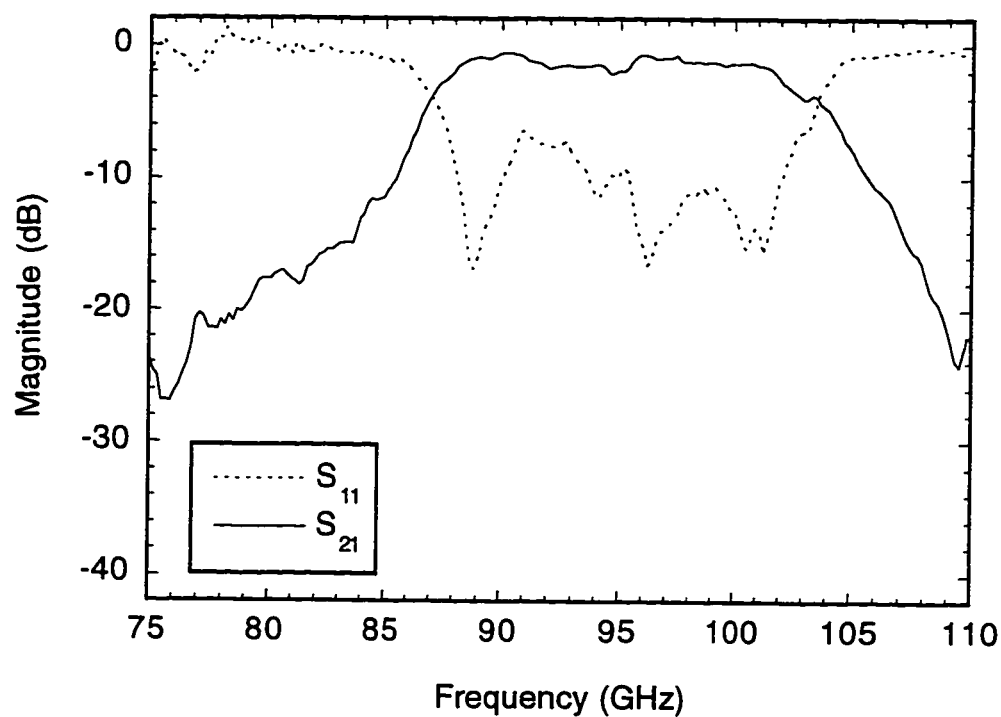


Figure 3.13: Measured S-parameters of an SMM band-pass filter with 1.4 dB insertion loss and 17.7% bandwidth at 94.9 GHz.

plane separation of 120  $\mu\text{m}$ . For this analysis, a dielectric sheet with a thickness of 15  $\mu\text{m}$  and a relative permittivity of 1.1 was used to simulate the effects of the membrane (again, the relative dielectric constant of the thick membrane was chosen to give close agreement between measured and FDTD values of  $\epsilon_{r, \text{eff}}$ ).

The losses in the measured filter responses are assumed to be entirely due to conductor losses within the filter, as was observed for the half-wavelength resonator in Section 3.3. This is verified by PARFIL analysis, which predicts a passband insertion loss of 3.4 dB for the narrow-band (6.1%) filter when only conductor losses are included (metallization is 4000  $\text{\AA}$  Au). The losses are also

Filter Section Index, $k$	6% Bandwidth Filter	
	width ( $w_k$ )	separation ( $s_k$ )
$k = 1,6$	160	70
$k = 2,5$	180	270
$k = 3,4$	180	300
Filter Section Index, $k$	13% Bandwidth Filter	
	width ( $w_k$ )	separation ( $s_k$ )
$k = 1,6$	140	30
$k = 2,5$	180	140
$k = 3,4$	180	180
Filter Section Index, $k$	18% Bandwidth Filter	
	width ( $w_k$ )	separation ( $s_k$ )
$k = 1,4$	155	25
$k = 2,3$	180	105

Table 3.4: Dimensions (in  $\mu\text{m}$ ) of the coupled line sections in the micromachined band-pass filters.



used to extract values for the  $Q$ 's of the resonators in each of the filters. This is done assuming the filters consist of uniform resonators according to the method presented in [47]. Table 3.5 summarizes the values found for the  $Q$ 's of the resonators in each filter. It is noted that the quality factors for the resonators in these band-pass filters are 1.5 to 2 times larger than the  $Q$  of the first resonance of the gap-coupled resonator presented in Section 3.3. This is mainly due to the different geometry used in the development of the band-pass filters (namely,  $w = 190 \mu\text{m}$  instead of  $98 \mu\text{m}$ , and  $h = 100 \mu\text{m}$  instead of  $50 \mu\text{m}$ ). If the resonator geometry were scaled in length only, one would expect a  $\sqrt{f}$  decrease in  $Q$  as frequency increases.

Filter Bandwidth	Measured $S_{21}$	Estimated Mismatch Loss	Resonator $Q$
6.1%	3.6 dB	0.6 dB	199
12.5%	2.2 dB	0.6 dB	155
17.7%	1.4 dB	0.6 dB	155

Table 3.5: Quality factors ( $Q$ 's) of the SMM resonators used in the band-pass filters.

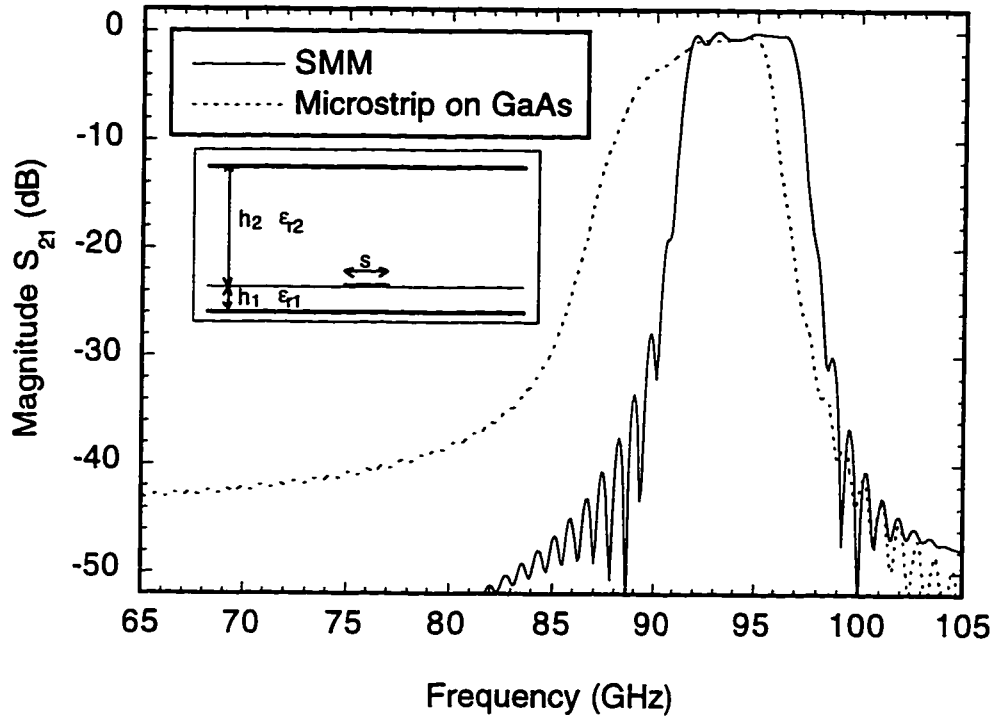
### 3.4.3 A Band-pass Filter on GaAs

As with the microshield low-pass filter, the FDTD analysis was used to compare the performance of an SMM band-pass filter to an equivalent coupled line band-pass filter realized on GaAs. Once again, a very simple design methodology was performed to realize the filter on GaAs; the filter dimensions were synthesized using PARFIL, and the resonator lengths were scaled to  $230 \mu\text{m}$  based on FDTD simulations. The ground plane separation was  $100 \mu\text{m}$  and the cover height was  $500 \mu\text{m}$ , but the substrate dielectric constant was 13 instead of 1. For the purposes of comparison, no effort was made to compensate for the

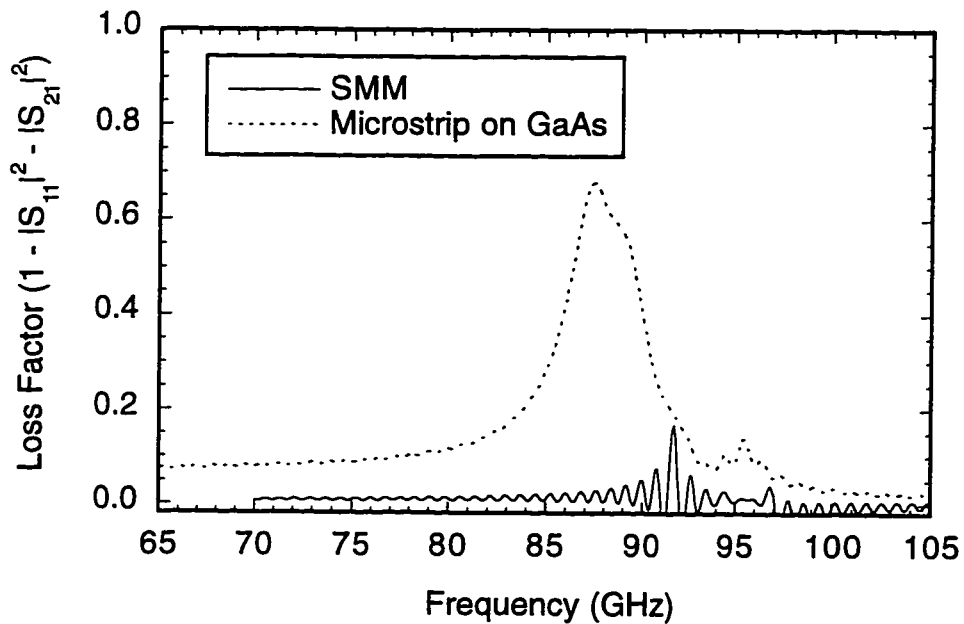
effects of the dielectric substrate (e.g. via holes or waveguide enclosures). The dimensions of the filter on GaAs are provided in Table 3.6 for comparison to the SMM filter dimensions. The theoretical performance of the filter on GaAs is plotted in Figure 3.14(a), and a severe degradation in performance is observed in comparison with the membrane supported circuit. The filter pass band is non-symmetric and the out-of-band signal rejection suffers due to radiation losses. Figure 3.14(b) shows the high levels of substrate radiation which plague the filter - note that nearly half of the input power is lost to radiation around the low frequency corner of the filter response. Specialized fabrication techniques can be used to alleviate these problems, but they usually result in increased circuit complexity and cost.

<b>Filter Section Index, <math>k</math></b>	<b>width (<math>w_k</math>)</b>	<b>separation (<math>s_k</math>)</b>
$k = 1,6$	70	70
$k = 2,5$	80	190
$k = 3,4$	80	220

Table 3.6: Dimensions (in  $\mu\text{m}$ ) of the coupled-line sections in the band-pass filter on GaAs.



(a)



(b)

Figure 3.14: (a) Theoretical performance of a coupled line band-pass filter using both conventional microstrip (on GaAs) and shielded membrane microstrip. (b) Modeled radiation losses in the band-pass filters of (a).

### 3.5 Conclusions

To demonstrate the efficacy of membrane-supported transmission lines in *W*-band applications, several filter structures were fabricated and tested. A 90 GHz low-pass filter with 0.7 dB insertion loss verifies the ability of microshield to maintain high levels of performance in the millimeter-wave frequency range. In addition, the shielded membrane microstrip line, introduced as a microstrip based equivalent to the microshield line, also proves to be an excellent medium for *W*-band circuit development. This is evinced by the uniform, broad band performance of the 25 GHz end-coupled resonator and the sharp cutoff characteristics of several coupled-line band-pass filters, ranging from 6.1% to 17.7% in measured bandwidth. FDTD simulations are used to verify measured results as well as to provide a basis for comparison between the membrane-supported circuit elements and equivalent substrate-supported components. These comparisons show that membrane-supported lines effectively eliminate the problems associated with dielectric substrates at *W*-band, and they do so without the need for complicated design procedures or intensive experimental iteration.

## **CHAPTER IV**

# **A MICROMACHINED WIDEBAND DIRECTIONAL COUPLER**

### **4.1 Introduction**

Micromachined millimeter-wave transmission lines have shown very good performance and have been used to create low-loss high-Q circuits such as filters [53],[16] and power dividers [15]. In addition, micromachined shielding cavities have been used to develop individually packaged circuits which provide additional benefits of compact size, light weight, and electromagnetic isolation [17]. This chapter describes the development of a micromachined wideband directional coupler that takes advantage of the superior performance and integrated packaging aspects afforded by the SMM line architecture.

Directional couplers are of great importance for many types of microwave systems. In particular, measurement applications (e.g. network analysis) require precise knowledge of signal characteristics without great disruption of the signal being measured. This is typically accomplished through the use of a 10-20 dB directional coupler which provides low insertion loss to the measurement signal. This type of measurement requires high directivity within the coupler so that measurement errors are minimized.

In order to realize the goal of creating a very wide band coupler, an asymmetric tapered coupled-line structure was chosen for study. This type of coupler can be designed for any desired coupling level, and is derived from the Klopfenstein impedance taper [42]. It has a high pass response, and therefore a theoretically infinite bandwidth. In practice, of course, it is impossible to achieve infinite bandwidth due to the limitations of the transmission media used in the circuit realization. It is believed that by using SMM line, however, the high frequency limitations usually encountered by conventional planar structures are far less prohibitive. For example, the dielectric loss and dispersion mechanisms which contribute to degraded high frequency performance in couple line structures fabricated on dielectric substrates will be absent in a SMM coupled line structure. Where dispersion between even and odd mode phase velocities would normally disrupt the high frequency performance of a typical coupled line coupler, the SMM architecture will permit the coupler to maintain designed performance specification through a much higher frequency range.

## 4.2 Directional Coupler Circuit Design

A schematic of the coupler circuit is illustrated in Figure 4.1. The circuit consists of two sections: a tapered coupled-line section of length  $L$ , and a uniform uncoupled section also of length  $L$ . The actual coupling function occurs in the tapered section of the circuit, and this is where the frequency response of the circuit is determined. In general, a transmission line which realizes a tapering function in characteristic impedance will have high-pass response, and this in turn gives the asymmetric tapered coupled-line coupler a high-pass response. The section of uncoupled lines provides phase compensation and gives the circuit a  $180^\circ$  phase shift between the two output ports [46].

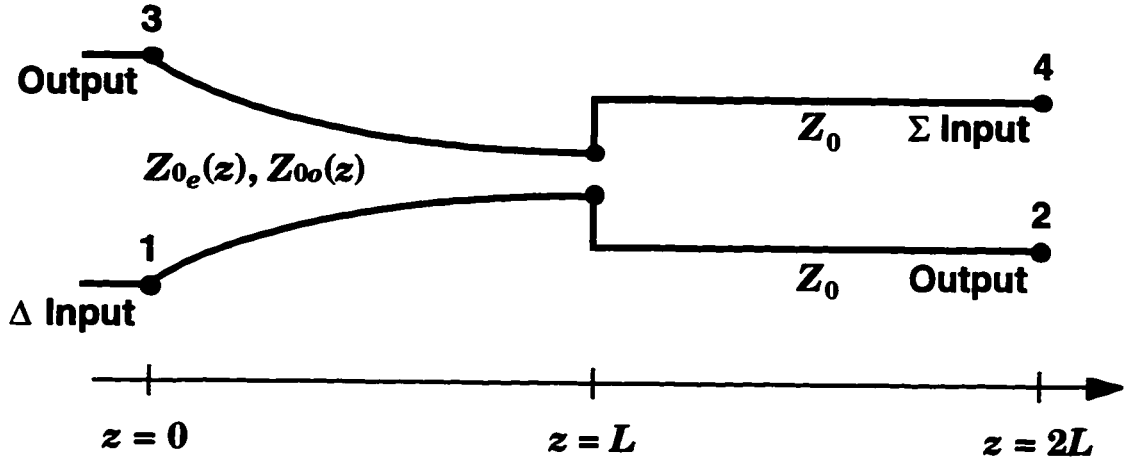


Figure 4.1: Circuit schematic of the asymmetric tapered coupled line coupler. The impedance distributions  $Z_{0e}(z)$  and  $Z_{0o}(z)$  are calculated from the Klopfenstein taper algorithm.

Design of the directional coupler is based on two parameters, the length of the coupling section,  $L$ , and a coupling factor,  $k$ , which is defined in terms of the voltage transmission coefficient,  $\alpha = |S_{31}|$ , as shown in Eqn. 4.1.

$$k = \frac{1 - \alpha}{1 + \alpha}, \quad 0 \leq k \leq 1 \quad (4.1)$$

For example, to design a 10 dB coupler (i.e.  $|S_{31}| = -10$  dB) the voltage coupling coefficient,  $\alpha$ , is chosen to be 0.316, giving a coupling factor,  $k$ , of 0.519. Once the coupling factor has been determined, it is used to calculate the even- and odd-mode impedance functions,  $Z_{0e}(z)$  and  $Z_{0o}(z)$ , of the tapered section of the coupler. At the position  $z = 0$ , the lines are uncoupled, such that  $Z_{0e}(z)$  and  $Z_{0o}(z)$  are equal to the characteristic impedance,  $Z_0$ . At  $z = L$ , the lines reach their maximum coupling, with  $Z_{0e}(L) = Z_0/k$  and  $Z_{0o}(L) = kZ_0$ . Thus, the coupling factor determines the values of the impedance functions at either end of the taper.

To complete the circuit design, the impedance distribution for  $0 < z < L$  must be calculated. In general, the even and odd functions can be calculated separately, and each can be thought of as simply a tapering function that matches the impedances at either end of the coupling section. There are many possible choices for impedance matching taper functions, but the Klopfenstein taper is commonly chosen since it provides the desired distribution in the smallest amount of space (see Section 2.3.4). Also, the Klopfenstein function requires a step change in impedance to occur at each end of the taper, and this actually simplifies the coupler circuit design. At the  $z = 0$  position, notice that an abrupt change from the coupled lines of the taper to the uncoupled input and output feed lines is necessary. This step change is much easier to implement when it is included into the impedance matching function as is the case with the Klopfenstein taper.

The preceding discussion deals with ideal transmission line theory only, and gives consideration to the transmission line geometry which will eventually be used to realize the coupler. In order to translate this design theory into practice, an SMM line with a ground plane height,  $h$ , of  $50\text{ }\mu\text{m}$ , and a cover height,  $h_c$ , of  $500\text{ }\mu\text{m}$  was selected. The width of the SMM line was set to  $100\text{ }\mu\text{m}$  to give an impedance of  $90\text{ }\Omega$ . A desired coupling level of  $-20\text{ dB}$  dictated a coupling factor  $k = 0.818$  and required even- and odd-mode impedances of  $74$  and  $110\text{ }\Omega$ , respectively, at the point of maximum coupling. Impedances at discrete intervals along the Klopfenstein taper were calculated using the algorithm described in Section 2.3.4, with a maximum reflection coefficient of  $-30\text{ dB}$ . The length of the taper was set to  $108^\circ$ , which corresponds to a minimum length of  $4.5\text{ mm}$  for an SMM line at the operating frequency of  $20\text{ GHz}$ . Finally, the physical dimensions of the coupled lines in the



taper were synthesized with the MCLIN model in *LineCalc*, using a substrate with a relative dielectric constant of 1.1 and a 500  $\mu\text{m}$  high shielding cover.

For two-port measurements, two of the four ports in the directional coupler must be matched. To provide complete four-port data of the coupler, three identical circuits were designed, each with a different combination of matched and measured ports. To realize the matching function at unmeasured ports, the Klopfenstein taper was once again utilized. In this instance, the taper was designed to match the 90  $\Omega$  SMM line in the coupler to a 70  $\Omega$  microshield line. The microshield line was then terminated by a parallel combination of two 140  $\Omega$  thin film resistors as described in Appendix C.

A photograph of the micromachined coupler without the micromachined ground plane cavity appears in Figure 4.2. The four ports of the coupler are

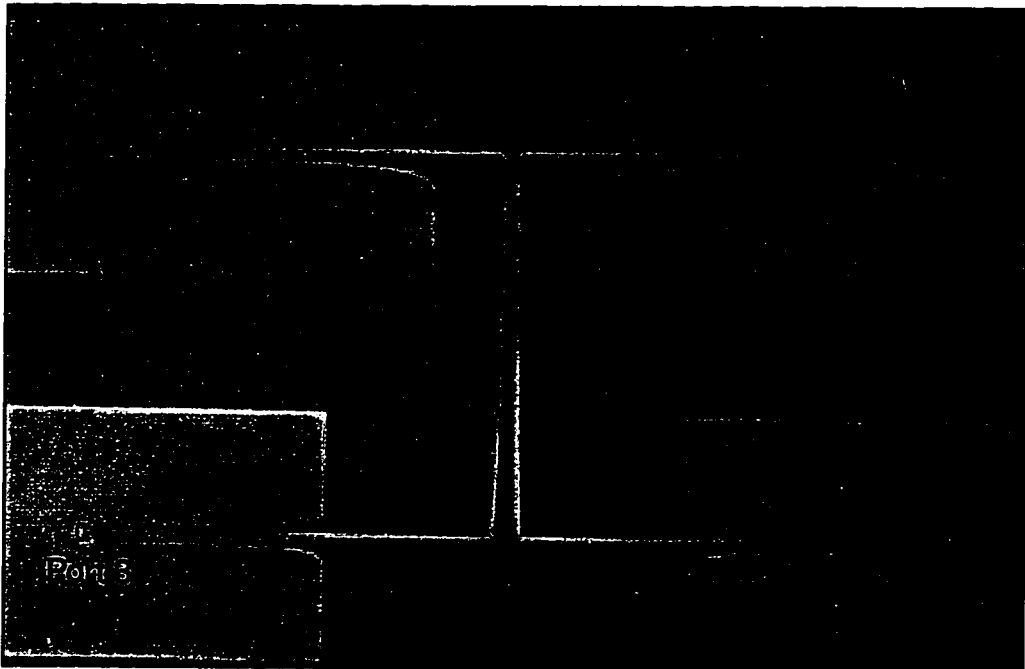


Figure 4.2: Photograph of the micromachined directional coupler with the ground plane cavity removed. The membrane supported region appears darker than the surrounding silicon support rim. Ports 2 and 4 are terminated with matching loads to permit coupled response measurements.

indicated; ports 2 and 4 are terminated in this circuit to allow measurements of the  $S_{31}$  (coupled) response. Also, note the membrane supported region, which appears darker than the silicon support rim. Subsequent attachment of the ground plane wafer was accomplished using the microsphere self-alignment technique discussed in Appendix B.

A more detailed view of the resistive termination used at the unmeasured ports appears in Figure 4.3. The thin strips of Nichrome which form the resistors are approximately  $15\text{ }\mu\text{m}$  wide by  $70\text{ }\mu\text{m}$  long.

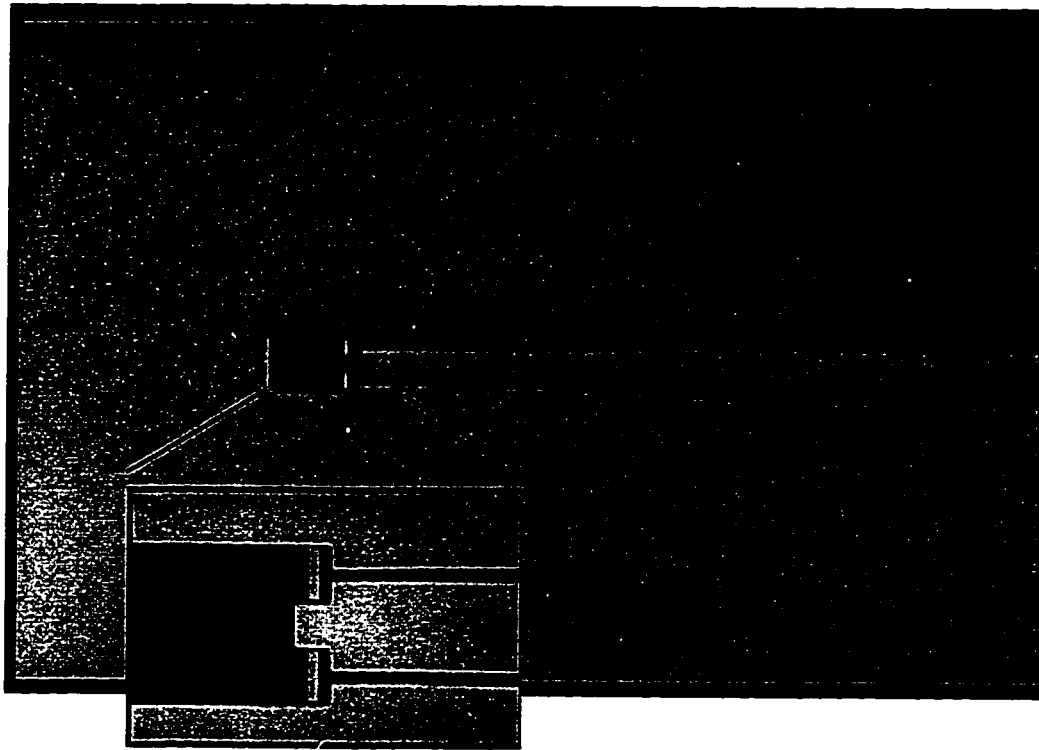


Figure 4.3: Photograph of the resistive termination, with inset showing the thin film resistors in parallel across the slots of the microshield line.

### 4.3 Measurement and Simulation

De-embedded on-wafer measurements of the micromachined coupler were accomplished using the TRL method and MultiCal. Measurements were carried out from 2 to 118 GHz using the three different test set configurations of the HP 8510C Network Analyzer and the Klopfenstein taper transition from GCPW to shielded membrane microstrip.

Simulations of the coupler were carried out using the *Touchstone/Libra* microwave circuit analysis software from HP/EEsof. The coupler circuit was approximated using a stairstep approximation of the tapered line section and the same microstrip coupled line elements that were used in *LineCalc* to synthesize the transmission line dimensions. Simulation results are provided in comparison to the measured results.

#### 4.3.1 Terminations

An isolated termination was fabricated and measured independently. DC measurements of the terminations indicated resistance values of 75-76  $\Omega$  instead of the desired 70  $\Omega$ , and microwave measurements of the termination show that the return loss peaks at approximately 13 dB at around 102 GHz, but remains in the 15–20 dB range from 2 to 118 GHz (see Figure 4.4).

#### 4.3.2 Directional Coupler

The measured coupling and isolation of the micromachined coupler are plotted in comparison to simulated *Libra* results in Figure 4.5. The coupling ( $S_{31}$ ) is  $21.2 \pm 3.3$  dB from 8 to 118 GHz and shows very nice agreement with the quasi-static results calculated with *Libra*. The consistency of the coupling function over the band is excellent. The coupler shows basically the same cou-

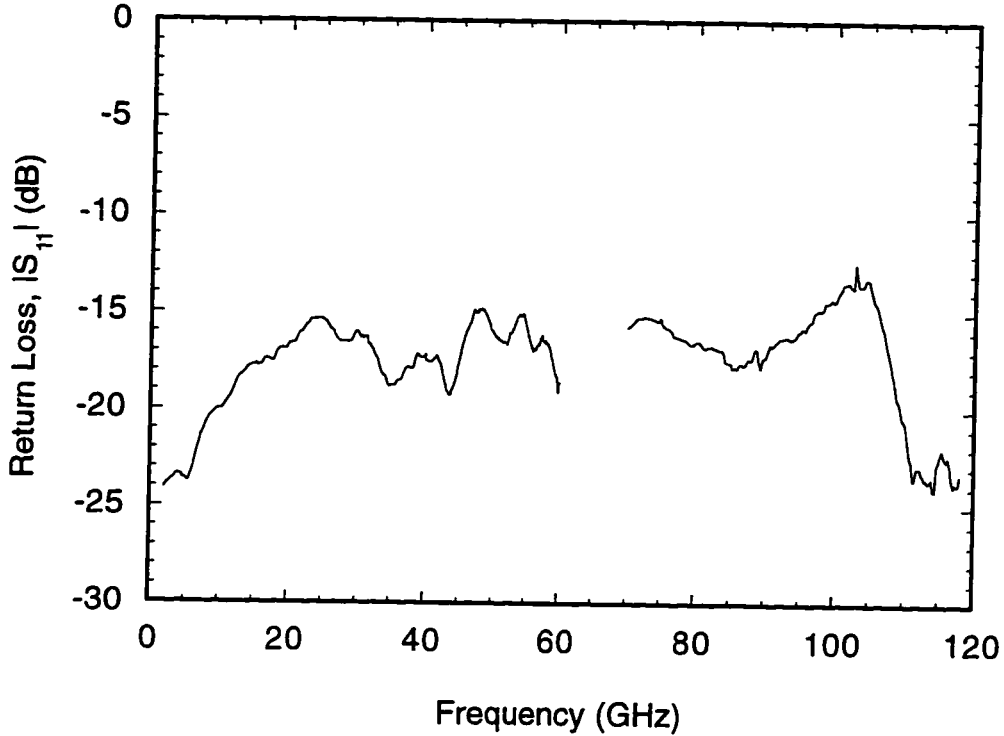


Figure 4.4: Measured return loss of the independent termination used to match unmeasured ports of the micromachined directional coupler.

pling performance at 118 GHz that it does at 8 GHz, indicating a measured bandwidth of 200%. It can be theorized that the actual bandwidth is much greater, but there is not currently a means of measuring network  $S$ -parameters on-wafer above 118 GHz. Also notable is the fact that the coupler was designed using only simple ideal transmission line theory and 2-D transmission line models, and yet it performs accurately and consistently over the measurement band. This testifies to the nearly ideal propagation characteristics of the membrane supported SMM line.

The isolation response of the coupler determines the directivity, which is an important performance parameter. The isolation of the micromachined coupler rises steadily as frequency increases, following the trend predicted by the

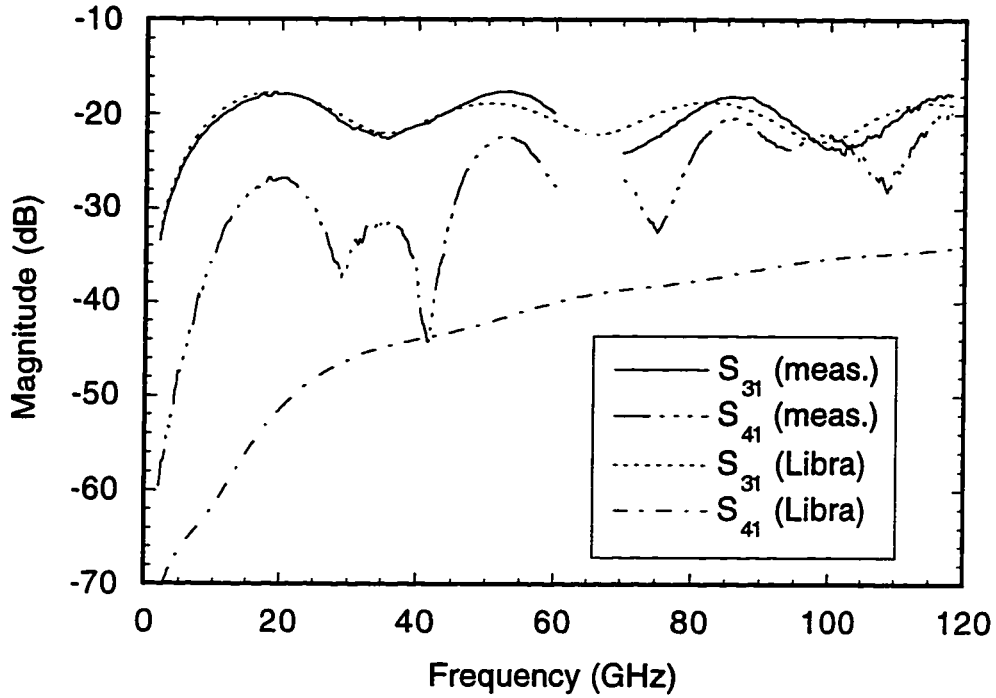


Figure 4.5: Measured and simulated coupling and isolation responses of the micromachined directional coupler from 2-118 GHz.

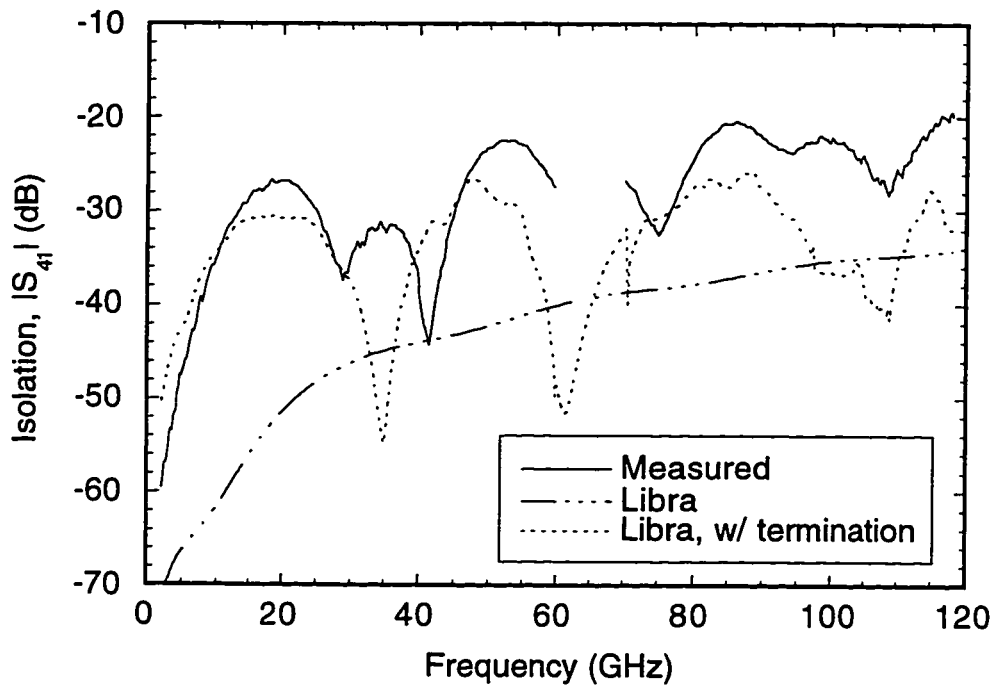


Figure 4.6: Effects of the imperfect termination on the isolation measurement of the directional coupler.

quasi-static analysis. The measured response is 15–20 dB higher than the theoretical response, and shows a periodic response indicative of a standing wave in the measurement. These factors result primarily from the imperfect nature of the resistive terminations applied to the unmeasured ports of the coupler (ports 2 and 3 in the isolation measurement). The effect of the imperfect terminations can be observed by including the measured termination response from Figure 4.4 in the quasi-static analysis (using the REFNET item in the *Libra* test bench). When this is done, the simulated response reflects the elevated isolation levels seen in the measurement, as well as the peak/null pattern (see Figure 4.6).

It should be noted that direct measurement of the isolation response of a directional coupler is an error prone technique. Any amount of power reflected on the through arm of the coupler may contribute to the measured signal at the isolated port, leading to measurement error. A far more accurate technique is described in [46] on pp. 389-391. This method, however, requires the use of a sliding matched load, and, for the case of the micromachined directional coupler, would have required three on-wafer probes. This would not have been feasible with all three of the network analyzer test sets, so the sliding load method was not utilized.

The insertion loss ( $S_{21}$ ), plotted separately in Figure 4.7 (a), is less than 1.1 dB up to 118 GHz. Once again, the smooth trend indicated by this plot demonstrates the excellent propagation characteristics of the SMM line. Two curves for the return loss of the coupler are plotted in Figure 4.7 (b). One curve represents the condition of direct termination of the coupler by the network analyzer, as in the case of the direct port measurement, and the other curve shows the response when the coupler is terminated by the on-wafer resistive termination, as in the case of the coupled port measurement. The sec-

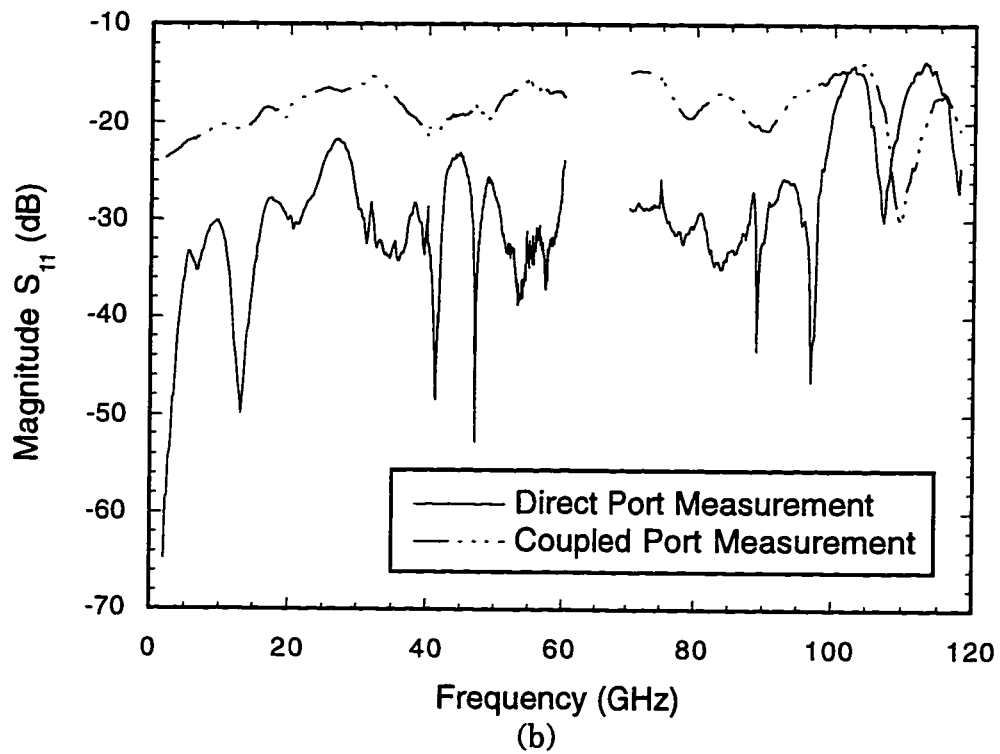
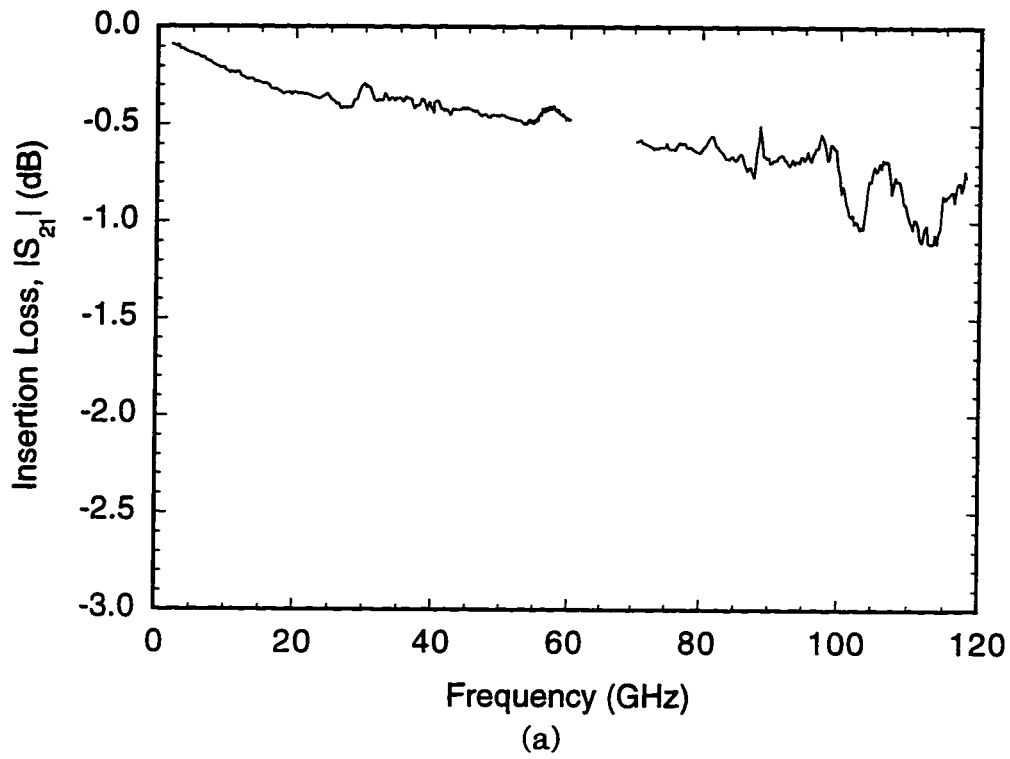


Figure 4.7: Measured (a) insertion loss and (b) return loss of the micromachined directional coupler.

ond trace is very similar to that given for the termination by itself in Figure 4.4, and the differences between the two highlight the limitations of the on-wafer termination once again.

In terms of insertion loss, this coupler represents a significant performance improvement over conventional planar technology, and even rivals the performance of *Ka*-Band waveguide couplers (see Table 4.1). A limitation of this coupler, however, is that it is not suited for reflectometer applications where directivities as high as 40 dB are preferred for accurate results. Even under ideal measurement conditions, the isolation response would only approach the quasi-static limit, which maintains 40 dB directivity only in the lowest operating frequencies.

	<b>This Work</b>	<b>Planar Coupler<sup>a</sup> [54]</b>	<b>Waveguide Coupler<sup>b</sup> [55]</b>
Frequency Range (GHz)	8 - 118	18 - 40	26.5 - 40
Coupling (dB)	$21.2 \pm 3.3$	$20 \pm 1.25$	$20 \pm 0.7$
Max. Insertion Loss (dB)	1.1	1.45	0.8
Directivity (dB)	9 to 2 <sup>c</sup>	12	37

Table 4.1: Comparison of the micromachined coupler to commercially available *Ka*-band couplers.

a. Includes coaxial connections.

b. Referenced to waveguide flanges (WR-22).

c. Directivity decreases from 9 dB at 20 GHz to 2 dB at 118 GHz.

## 4.4 A Coupler on GaAs

For purposes of comparison with the micromachined coupler, a 20 dB asymmetric tapered coupled line coupler was designed for 20 GHz operation on a 100  $\mu\text{m}$  thick GaAs substrate ( $\epsilon_r = 13$ ) with a 500  $\mu\text{m}$  shielding cover. The design procedure outlined in Section 4.2 for the SMM coupler was fol-



lowed for the GaAs coupler, and it was then simulated using Libra. The results of this simulation are shown in comparison to the simulated performance of the SMM coupler in Figure 4.8. The isolated port response of the GaAs coupler shows a significant degradation in performance, with levels 20-22 dB above those of the SMM coupler. The directivity of this coupler reaches a maximum value of only 6 dB at 20 GHz, making this circuit unsuitable for virtually any application. It should also be noted that these results are obtained from quasi-static models, which means radiative losses into substrate modes and other parasitic effects are not considered. This, combined with the fact that any

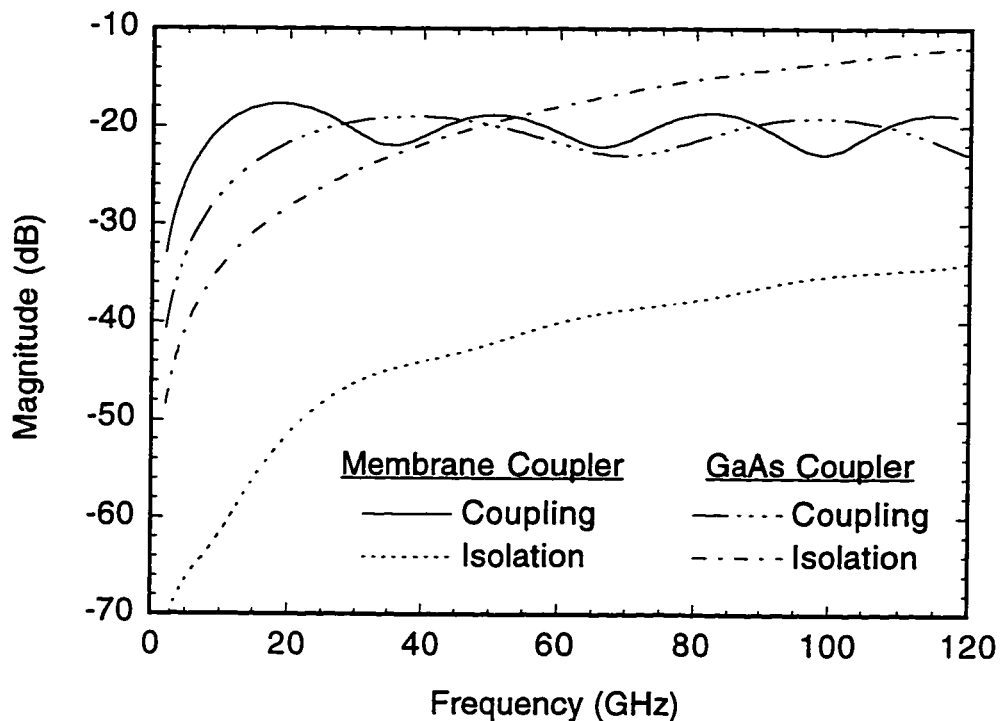


Figure 4.8: Comparison of the simulated performance of two directional couplers. The Membrane Coupler is the SMM coupler previously discussed, while the GaAs Coupler is an equivalent structure implemented on a 100  $\mu\text{m}$  GaAs substrate with a 500  $\mu\text{m}$  shielding cover.

imperfect terminations at unmeasured ports of the coupler will lead to huge performance fluctuations in the coupled port response, demonstrates the limitations created by the GaAs substrate. The performance advantages achieved by the membrane supported SMM coupler are significant.

## 4.5 Conclusions

A membrane supported 20 dB directional coupler has been designed and fabricated using the shielded membrane microstrip transmission line technology. Measured results of the coupler exhibit good performance over an extremely broad bandwidth from 2 - 118 GHz. The isolation of the coupler could not be accurately measured, but *Libra* simulations indicate that the isolation approaches levels indicated by quasi-static analysis methods. Even the isolation levels predicted by the *Libra* simulation, however, do not provide enough directivity for the coupler to be used for reflectometry applications over a broad bandwidth. In the future, a 10 dB tapered-line coupler may provide the higher directivity values needed for these applications.

Simulation of a similar coupler circuit realized in microstrip technology on a GaAs substrate indicates that the membrane-supported coupler achieves performance levels that could not be easily matched by conventional substrate technologies. In addition, design of the coupler circuit was carried out using very simple ideal transmission line theory. The measured results were quite close to the design values, indicating the near-ideal performance of the SMM line over the entire frequency range.

## CHAPTER V

# A *K*-BAND HEMT AMPLIFIER WITH MICROMACHINED CONFORMAL PACKAGING

### 5.1 Introduction

Cost savings in MMIC design and development can be achieved by reducing the number of design iterations, or prototypes, and by limiting the use of expensive materials such as GaAs and InP. Recently, integrated packaging concepts and flip-chip techniques have been studied as options for reducing MMIC cost.

Often, MMIC design efforts are complicated by the inability to predict the final packaged environment of a particular circuit. Parasitic effects such as coupling between neighboring MMICs may require an additional design iteration to regain lost performance levels. When the package is integrated with the MMIC, parasitic effects can be sharply reduced since the shielding structure can be considered during the design cycle. This type of integrated conformal packaging has been realized with silicon micromachining techniques, and has demonstrated the ability to improve the overall performance of MMIC components in *Ka*-band and *W*-band applications [17],[53],[56].

Another technique for reducing MMIC fabrication and development costs is the use of discrete flip-chip devices [57]. These devices can be designed and

optimized for individual performance specifications independent of the entire MMIC, and this can reduce costs in several ways. First, overall production yield can be improved since devices can be screened before being attached to the circuit (and they can be replaced if they later fail). Second, the MMIC itself can be designed and fabricated on a low-cost substrate such as silicon, which means expensive material costs are limited to the discrete devices. Finally, flip-chip devices can be attached to MMICs with reliable solder bump techniques, which provide repeatable, low-inductance connections that make circuit designs faster due to rapid prototype implementation.

This chapter describes the application of flip-chip device mounting techniques and integrated conformal packaging in the realization of a 20 GHz amplifier on Si. The development of micromachined conformal packages for MMIC design is discussed, followed by the design of the amplifier circuit itself. A description of the techniques employed in the fabrication of the amplifier is given, and results of  $S$ -parameter measurements are presented.

## 5.2 Packaging Concept

The concept of integrated conformal packaging was first introduced by Drayton and Katehi in 1993 [58]. It is based on the architecture of the shielded coplanar waveguide (CPW) which is illustrated in Figure 5.1. This transmission line maintains all of the advantages of open CPW, such as uniplanar processing and ease of integration with two- and three-terminal active devices. The shielded CPW line also exhibits low radiation losses and reduced parasitic coupling to neighboring components. Both fully shielded and half shielded lines have been realized, with demonstrated performance advantages in each case. Analysis of the structure is accomplished with the point matching method algorithm [35].

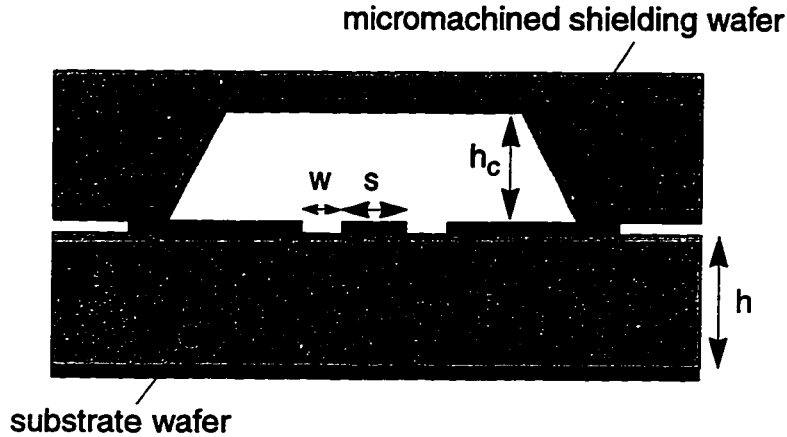


Figure 5.1: Two-dimensional representation of the shielded CPW transmission line.

The extension of the shielded CPW transmission line to a fully conformal integrated package involves the ability to shape the shielding cavity to follow the trace of the underlying CPW line on the surface of the MMIC. This is easily accomplished, since fabrication of the cavity is performed using lithographic and micromachining techniques common to Si processing. The transmission line elements in a conformally packaged circuit are individually shielded, and circuit elements can be brought much closer together than is possible with open structures. Thus, conformally packaged circuits can be used to realize space reductions in MMIC layouts. Also, design iterations can be conserved by including the shielding cavity in circuit simulations and avoiding unpredictable parasitic coupling effects.

### 5.3 Amplifier Design

The amplifier is designed around a flip-chip high electron mobility transistor developed by Hughes Research Laboratories for low noise performance [59]. The InP HEMT structure comprises a 250 nm undoped

AlInAs buffer with a 40 nm GaInAs channel, a 1.5 nm undoped spacer, an 8 nm AlInAs donor layer, a 20 nm undoped AlInAs Schottky layer, and a 7 nm GaInAs doped cap. The material is grown by molecular beam epitaxy (MBE) and is lattice-matched to an InP semi-insulating substrate. The device is passivated with a 100 nm silicon nitride layer.

The flip-chip transistor is roughly  $600 \times 600 \times 600 \text{ } \mu\text{m}^3$  in size and is mounted on the amplifier circuit via tin/lead solder bumps which have been electroplated on the transistor contact pads. The solder bumps are 25  $\mu\text{m}$  high and 50  $\mu\text{m}$  in diameter, and are reflowed to provide electrical contact to the amplifier. Figure 5.2 shows the HEMT flip-chip device, with solder bumps on the gate, drain, and both of the source contact pads. The device has a gate length of 0.15  $\mu\text{m}$ , and a total gate width of 300  $\mu\text{m}$ .

Design of the amplifier circuit was originally optimized for low noise performance in a microstrip configuration on a 250  $\mu\text{m}$  Alumina substrate. A schematic of this circuit appears in Figure 5.3, which shows the source feedback stubs used to optimize the low noise matching condition and the input and output matching networks. The input match is accomplished simply by a short section of 75  $\Omega$  transmission line, while the output matching network includes an open-circuit stub. Biasing of the HEMT is possible through the gate and drain bias networks provided at the input and output of the circuit. Radial stubs designed to resonate at 18.5 GHz produce RF isolation for the DC bias pads in conjunction with 20 pF lumped element capacitors.

Design parameters for this circuit were converted to the shielded CPW environment by maintaining equivalent impedances and electrical lengths for all transmission line sections. Results of the PMM algorithm generated the line dimensions for both 50  $\Omega$  ( $s = 94 \text{ } \mu\text{m}$ ,  $w = 53 \text{ } \mu\text{m}$ ) and 75  $\Omega$  ( $s = 34 \text{ } \mu\text{m}$ ,  $w = 83 \text{ } \mu\text{m}$ ) shielded CPW lines on a 550  $\mu\text{m}$  Si substrate with a 275  $\mu\text{m}$

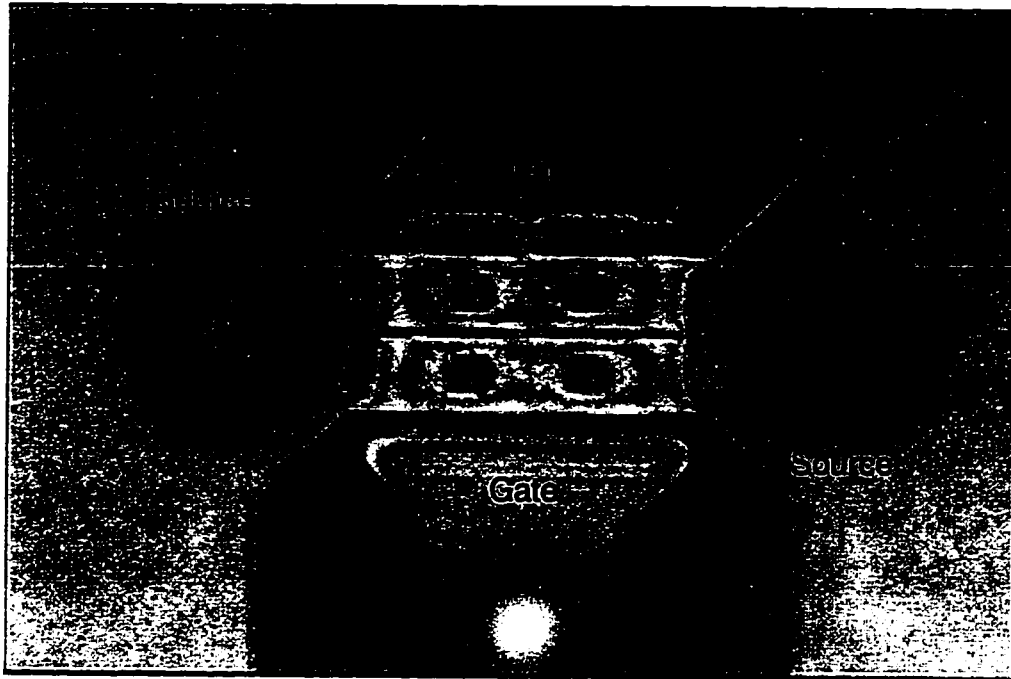


Figure 5.2: Photograph of the flip-chip HEMT showing the tin/lead solder bumps.

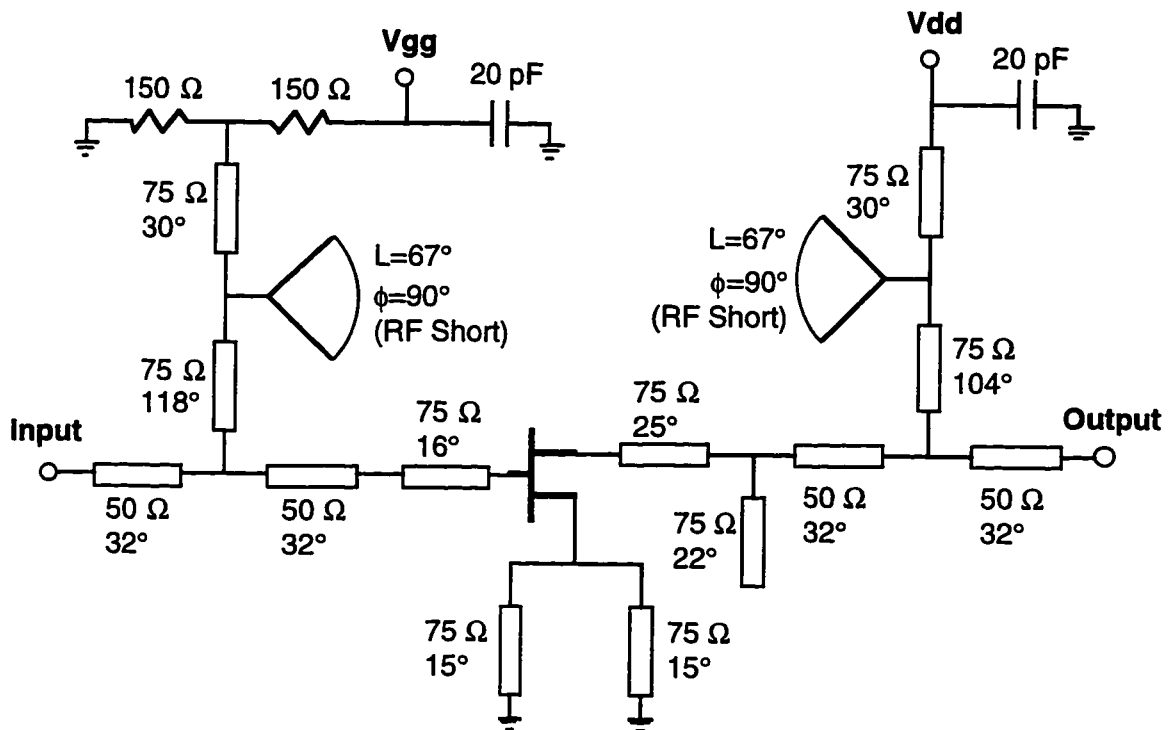


Figure 5.3: Schematic of the low noise amplifier designed for microstrip on Alumina.

shielding cavity. The width ( $s + 2w$ ) of the lines is selected to be  $200\text{ }\mu\text{m}$  to provide a convenient interface to the gate and drain pad dimensions of the HEMT. The overall width of the cavity is chosen as  $1\text{ mm}$  to allow incorporation of the flip-chip HEMT package into the conformal package.

The layout of the shielded CPW implementation of the amplifier is illustrated by the photograph in Figure 5.5. This circuit includes a few modifications as a result of the transition to the packaged CPW configuration. The output matching stub is converted to two balanced open circuit stubs, as is the radial stub in the gate bias network. The radial stub in the drain bias network is removed in favor of a  $20\text{ pF}$  capacitor and the lumped element components are integrated into the shielded amplifier circuit as thin-film resistors and MIM capacitors. The lengths of the source feedback stubs and the output matching stubs were varied slightly to optimize the noise performance of the amplifier in the new configuration. Simulation and optimization of this circuit was accomplished through microstrip line models in *Libra* [28].

## 5.4 Fabrication

The packaged amplifier is fabricated on a high-resistivity Si substrate with an  $8000\text{ }\text{\AA}$  thick layer of thermal  $\text{SiO}_2$ . The amplifier circuit patterns are created with  $3\text{ }\mu\text{m}$  thick electroplated gold. Thin film resistors are realized with a  $400\text{ }\text{\AA}$  Nichrome thin film as described in Appendix C. MIM capacitors are constructed with an evaporated  $1500\text{ }\text{\AA}$  thick  $\text{Al}_2\text{O}_3$  film with dielectric constant of approximately 8-10. Air bridges are formed with  $2\text{ }\mu\text{m}$  thick electroplated gold.

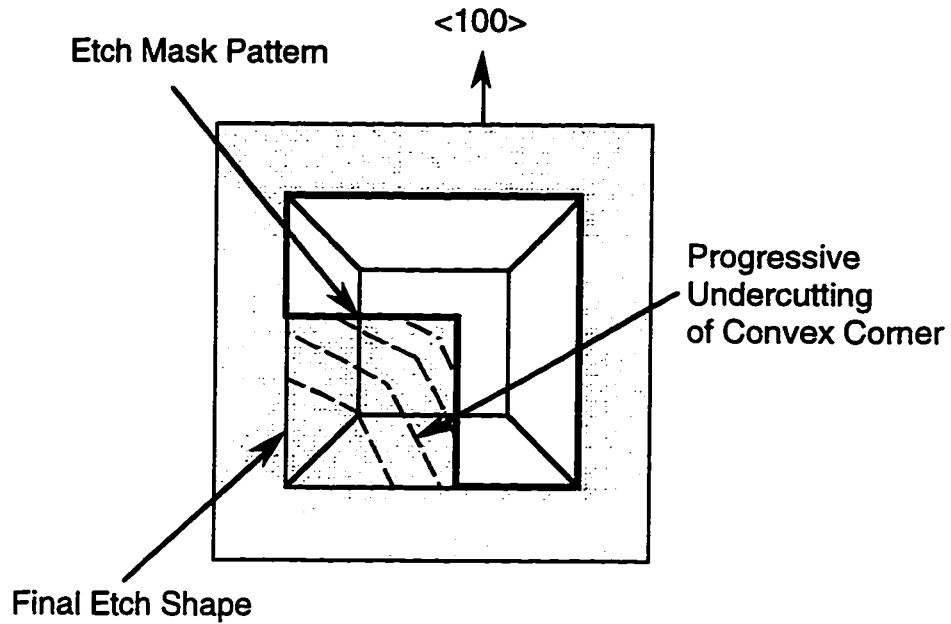
The micromachined conformal package is constructed from a separate low-resistivity silicon wafer with a thermal  $\text{SiO}_2$  masking layer on both sides. The cavities are micromachined using the anisotropic EDP etching system. Access



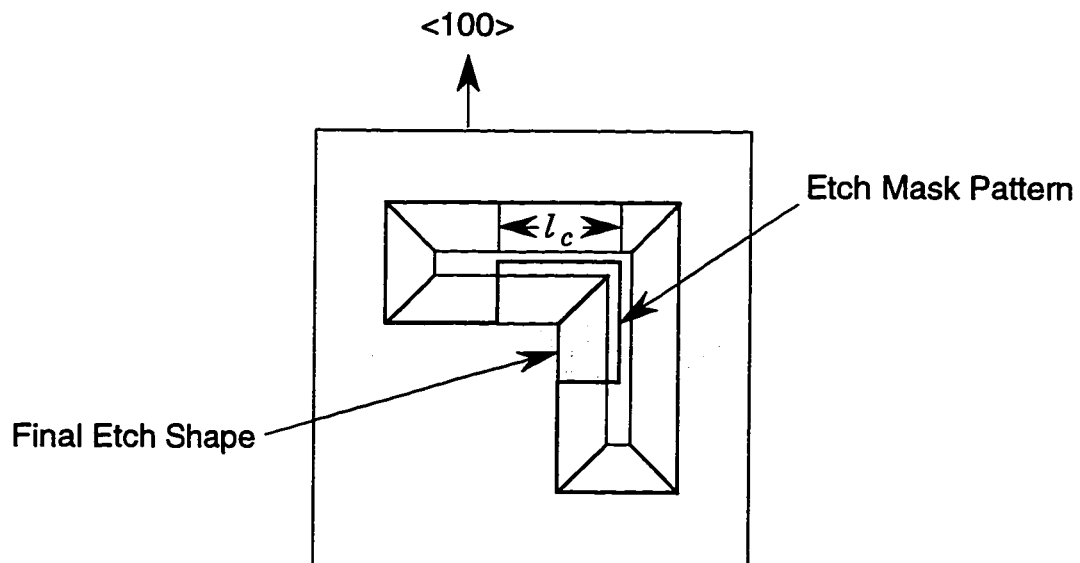
to the RF probe pads, DC bias contacts, and flip-chip mounting locations is provided with etched through-windows that are formed by etching from the back side of the cavity wafer during the conformal package creation. The depth of the shielding cavity is selected to be  $275\text{ }\mu\text{m}$ , so that when etching from both sides of the  $550\text{ }\mu\text{m}$  thick wafer, the access windows will open up as soon as the cavities reach the proper depth, and only one etching step is required. The cavity is metallized with a  $1.4\text{ }\mu\text{m}$  thick Ti/Al/Ti/Au evaporated film after all masking layers have been removed.

As described in Section 2.1.1, bulk micromachining of silicon with anisotropic etchants is most easily accomplished with rectangular shapes which are aligned to the  $\langle 110 \rangle$  direction on the Si sample. For the development of conformal cavities which require more complex shapes, special precautions must be taken in order to compensate for the rapid undercutting that will occur in areas where the shape of the cavity must deviate from the  $\langle 110 \rangle$  directions. This is illustrated in Figure 5.4(a) for the case of a right angle bend in the shielding cavity. The anisotropic etchant progressively undercuts the convex corner in the masking pattern until the final etch shape is rectangular. Figure 5.4(b) illustrates a method for compensating the etch undercut by adding a square shaped feature to the etch mask pattern. The square is centered on the corner of the desired etch pattern, and the sidelength  $l_c$ , which depends on the etch depth, is determined empirically. For a depth of  $275\text{ }\mu\text{m}$ , a sidelength of  $500\text{ }\mu\text{m}$  was found to provide adequate undercut compensation [60]. Newly reported compensation schemes for anisotropic Si etchants have also used triangular shapes based on the  $\{210\}$  crystalline planes [61].

Assembly of the low noise amplifiers was accomplished using silver epoxy [86]. Small droplets of the epoxy were placed at critical locations on the shielding wafer, which was then inverted and positioned over the circuit wafer



(a)



(b)

Figure 5.4: Compensation of convex corner shapes. (a) Undercut of a convex corner in an anisotropic etching solution. (b) Undercut compensation achieved by a square of sidelength  $l_c$  in the masking pattern.

by means of a vacuum chuck and an x-y-z positioner. A small piece of glass was attached to the shielding wafer to allow it to be held by the vacuum suction. After the two wafer pieces were properly aligned, they were brought into contact and then the epoxy was cured for 5 minutes at a temperature of 150°C. Then, the flip-chip HEMT devices were placed on the circuit wafer through the access windows in the shielding wafer, and soldered to the amplifier circuit. DC testing of the amplifier was performed to ensure good electrical contact to the amplifier circuit.

Figure 5.5 shows the fabricated LNA with the package removed, while Figure 5.6 contains a photograph of the conformal package. Finally, Figure 5.7 shows the amplifier in packaged form, with only the DC/RF probe pads and the flip-chip HEMT visible.

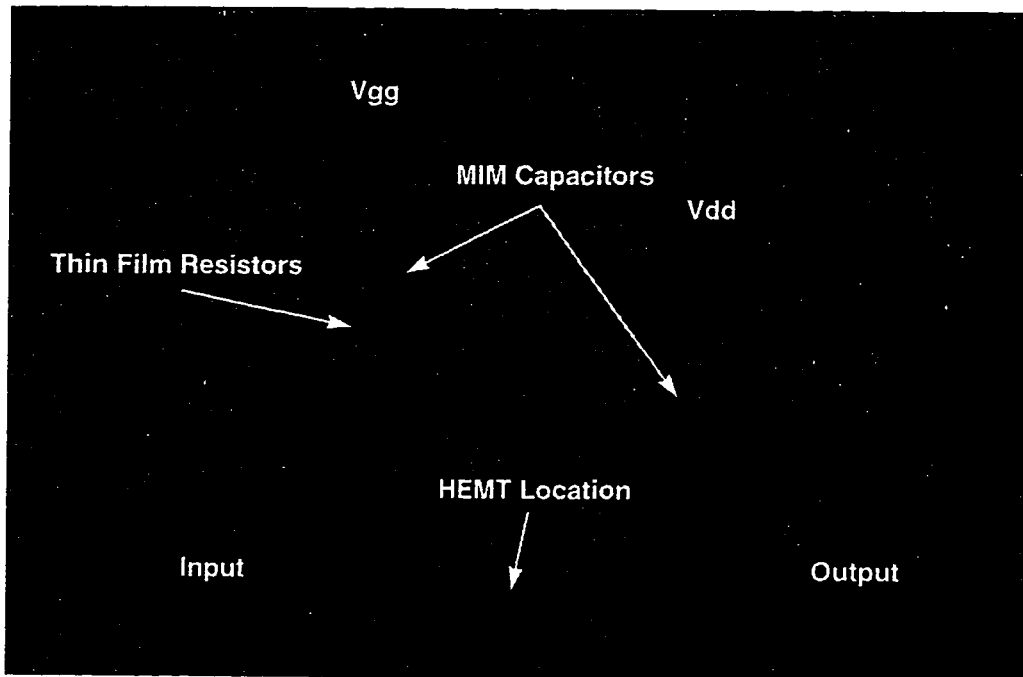


Figure 5.5: Layout of the 20 GHz low noise amplifier circuit with the micromachined shielding cavity removed (without InP flip-chip HEMT).



Figure 5.6: View from the bottom of the micromachined conformal package after final metallization has been completed.

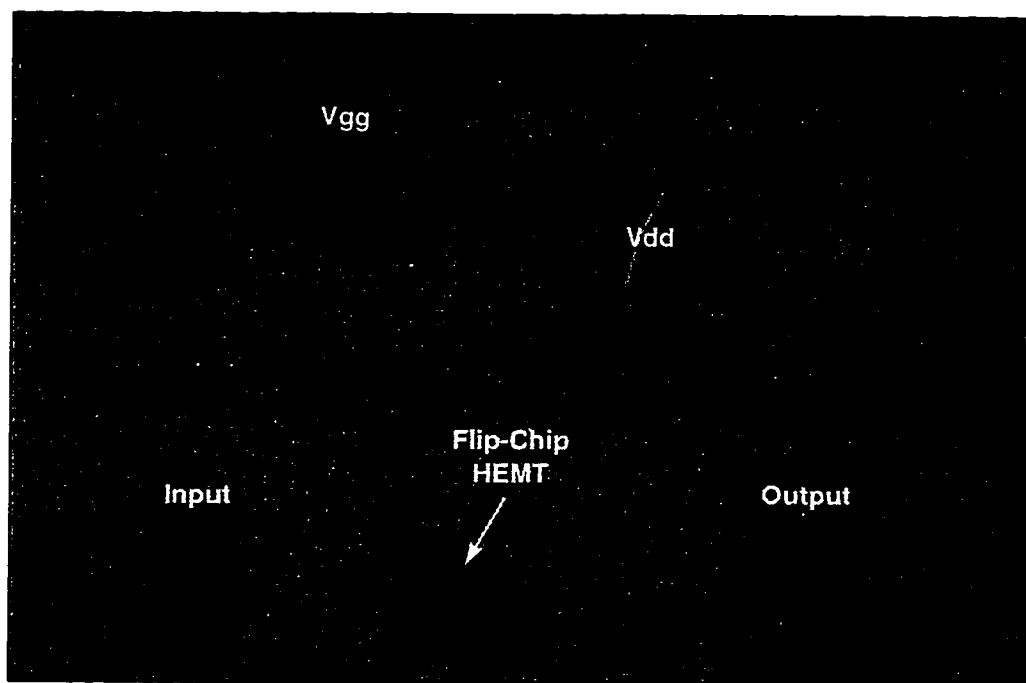


Figure 5.7: View of the low noise amplifier after enclosure with the micromachined shielding cavity. RF and DC bias probe pads are visible, as well as the inverted flip-chip HEMT.

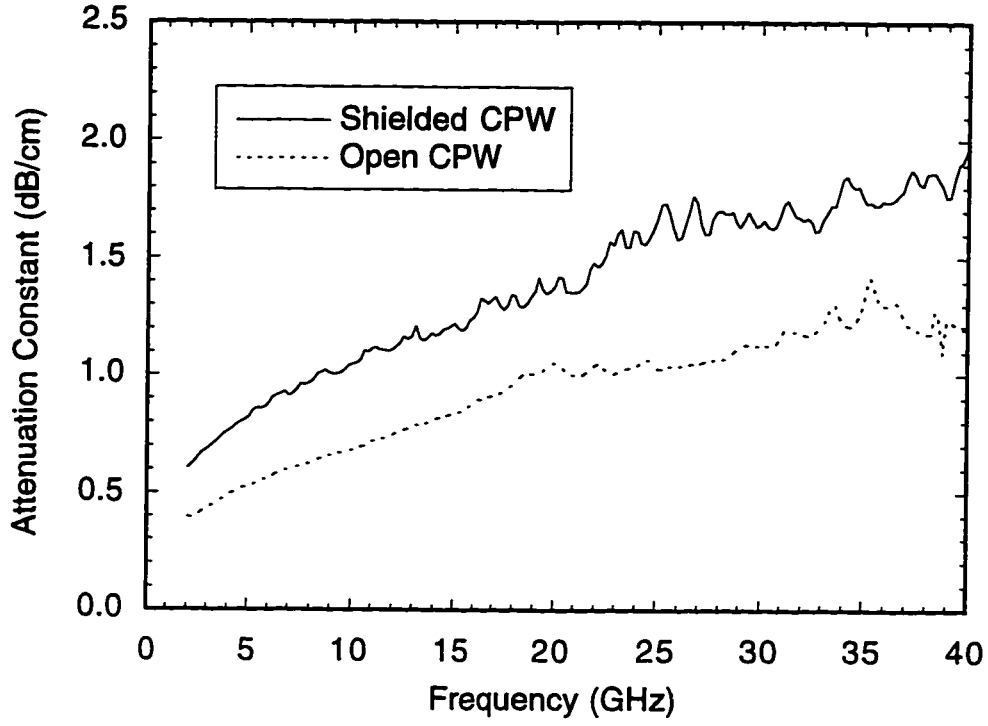
## 5.5 Measurements

S-parameter measurements of the packaged amplifier and several passive components were performed on the HP8510C Network Analyzer using the 2 to 40 GHz coaxial test set. On-wafer standards were fabricated so that a TRL calibration could be performed with MultiCal. Results of the calibration and various measurement are discussed below.

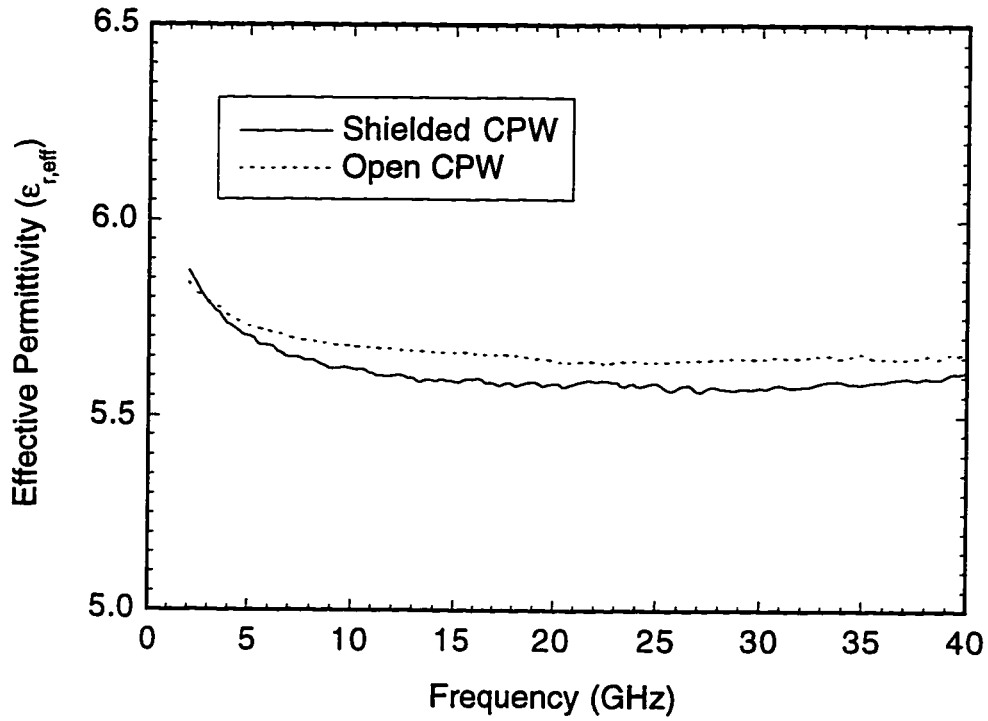
### 5.5.1 Shielded CPW Characteristics

In order to demonstrate the characteristics of the shielded CPW transmission line employed in the packaged amplifier circuit, MultiCal was used to extract data on the attenuation and effective permittivity of both shielded and open CPW transmission lines from 2 to 40 GHz. The CPW line in both cases was the  $50\ \Omega$  used in the amplifier layout ( $s = 94\ \mu\text{m}$ ,  $w = 53\ \mu\text{m}$ ). In the shielded case, the micromachined  $275\ \mu\text{m}$  cavity was placed over the transmission line, as depicted in Figure 5.1.

Figure 5.8(a) shows the attenuation constant of the two CPW lines, with the shielded line displaying approximately 0.3 dB/cm more attenuation than the open line at 20 GHz. This increased attenuation level agrees with previously measured results on shielded CPW lines [17], and is a result of two factors. First, as can be seen by examining the effective permittivity data presented in Figure 5.8(b), the characteristic impedance of the shielded line is slightly lower than that of the open line. This reduced characteristic impedance corresponds to an increase in current density on the line, and therefore an increase in ohmic losses. Second, the increased current density occurs over a larger area when the shielding structure is added to the line, and this also serves to increase the ohmic losses in the structure.



(a)



(b)

Figure 5.8: Attenuation (a) and effective permittivity (b) data for the shielded CPW line used in the low noise amplifier circuit (from MultiCal).  $s = 94 \mu\text{m}$ ,  $w = 53 \mu\text{m}$ ,  $h_c = 275 \mu\text{m}$ .

### 5.5.2 Passive Components

The balanced open stubs and the integrated MIM capacitors are the two very important circuit elements in the packaged LNA. They both perform the critical function of DC/RF isolation, in addition to maintaining the stability of the amplifier.

#### Balanced Open Stubs

Performance of the shielded CPW balanced stubs used for RF isolation in the gate bias network is shown in Figure 5.9. The stub resonates at approximately 20 GHz, instead of the desired 18.5 GHz, but has a broad response with a resonance of -30 dB in  $|S_{21}|$ .

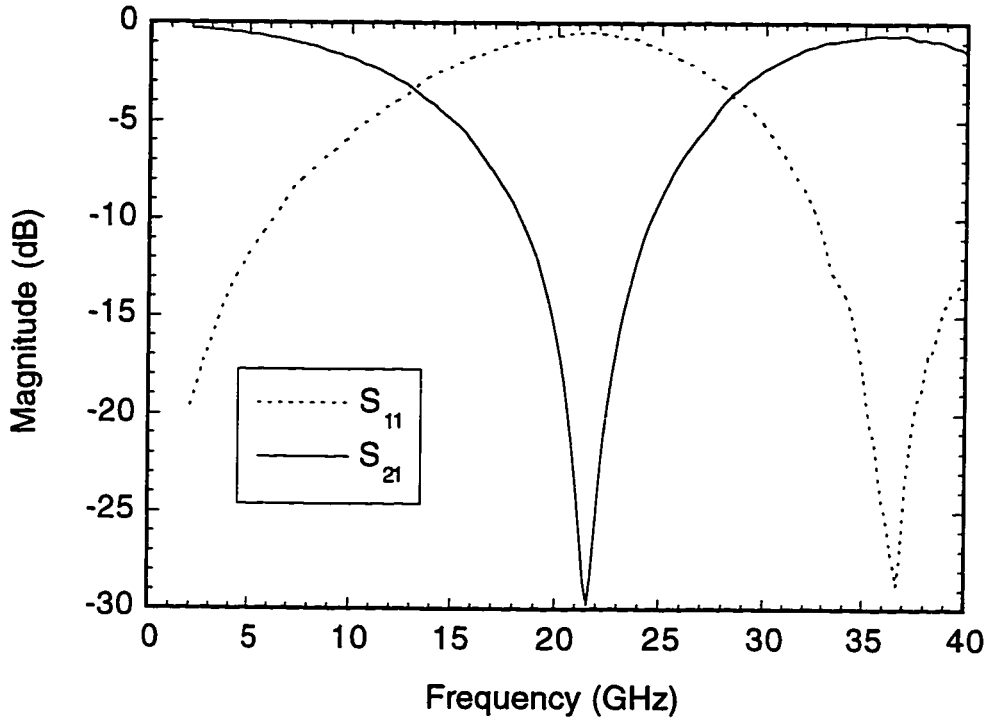


Figure 5.9: Measured S-parameters of the shielded CPW balanced stubs used in the gate bias network.

### MIM Capacitors

Measured  $S$ -parameters of an MIM capacitor appear in Figure 5.10. Comparison with an ideal capacitor model in *Libra* reveals that the capacitor has a value of approximately 23 pF, which is quite close to the desired value of 20 pF.

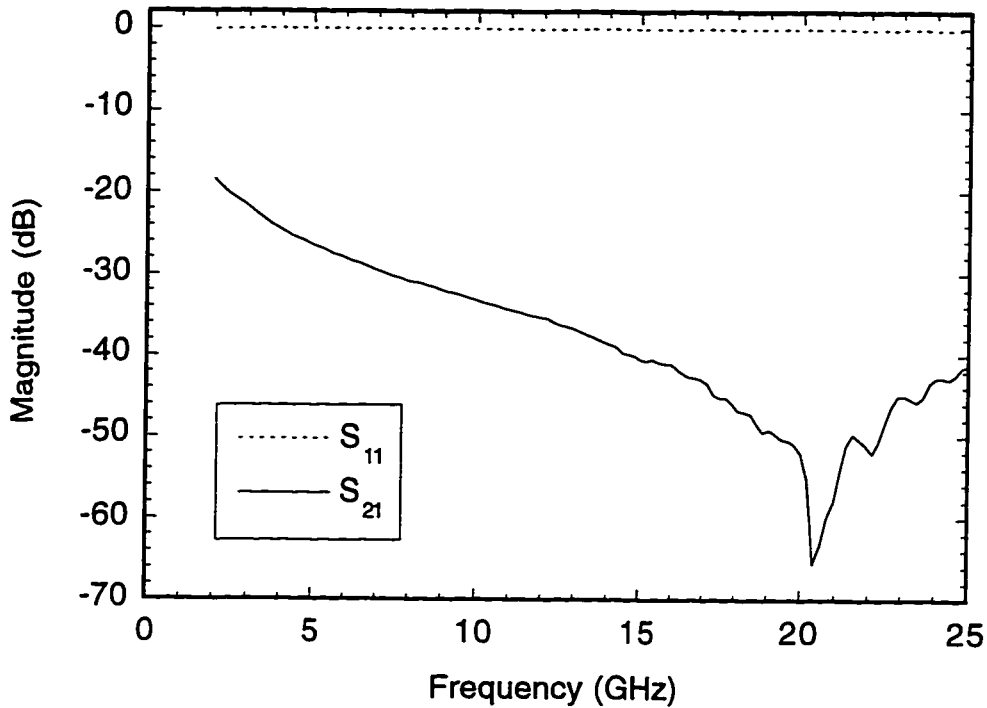


Figure 5.10: Measured  $S$ -parameters of the MIM capacitor used for RF isolation in the low noise amplifier circuit.

### 5.5.3 Amplifier Measurements

DC biasing of the HEMT during amplifier measurements was performed through the on-wafer bias networks incorporated into the amplifier circuit design. The bias point was  $V_{DS} = 1.0$  V,  $I_{DS} = 43$  mA, and  $V_G = -0.7$  V.

Measured  $S$ -parameter data appears in Figure 5.11 with the simulated results of the original microstrip amplifier design performed with *Libra* [28].



The good agreement between these data shows that accurate analysis of the conformal package was accomplished by simply including the presence of the upper shielding cavity in the design of the CPW components.

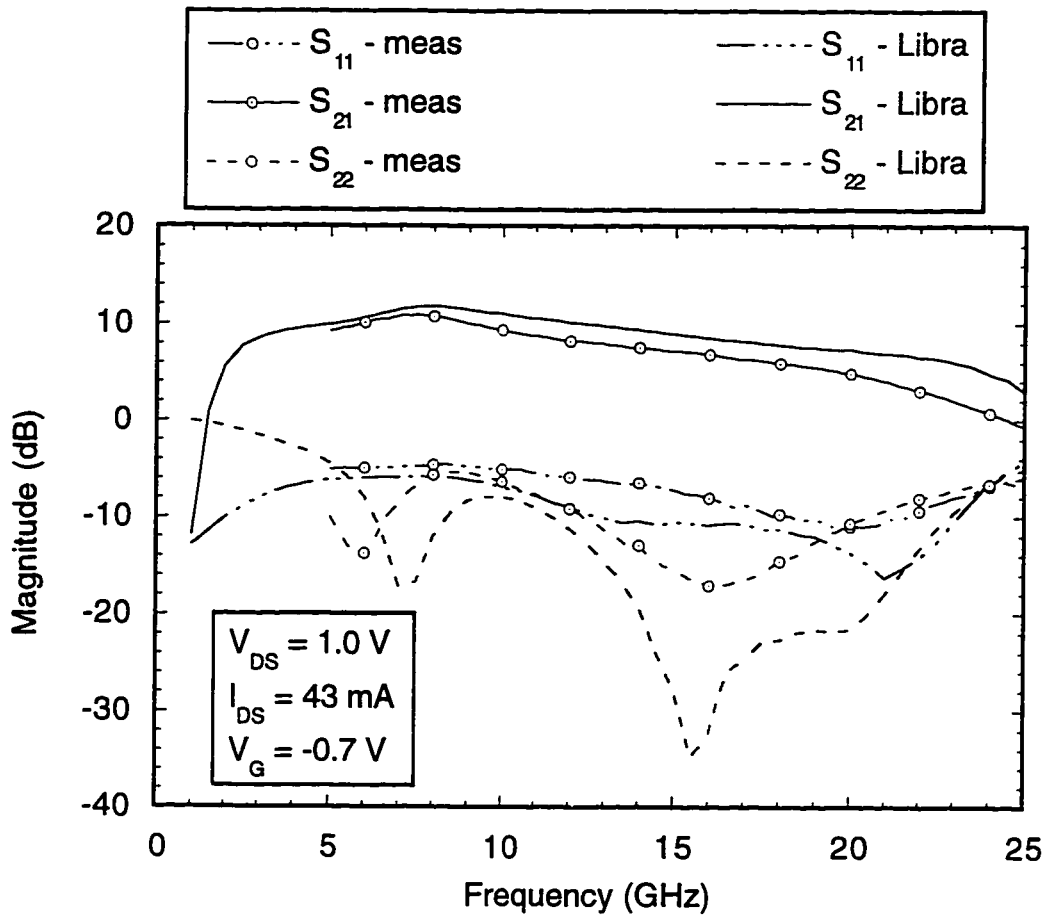


Figure 5.11: Measured S-parameters of the low noise amplifier compared to simulated results for an unshielded microstrip amplifier on an alumina substrate.

## 5.6 Conclusions

On-wafer  $S$ -parameter measurements of a 20 GHz low noise amplifier with an integrated conformal package have been demonstrated. These measurements confirm that integration of a conformal package can be achieved in MMIC applications through the use of silicon micromachining techniques. The conformal package offers the benefit of RF shielding and isolation without detriment to the performance of the amplifier, as proven by comparisons to simulated results of a microstrip low noise amplifier. In addition, the conformal packaging approach is shown to be compatible with flip-chip techniques which serve to further reduce fabrication costs and improve yield.

## CHAPTER VI

# CONCLUSIONS AND FUTURE WORK

### 6.1 Conclusions

This thesis has presented a collection of work on micromachined transmission line structures and circuits for use in *W*-band applications. Emphasis has been given to the membrane based microshield line and shielded membrane microstrip line, which have been used to develop circuit elements such as filters and directional couplers.

A microshield implementation of a stepped-impedance low-pass filter was designed and fabricated using the bulk Si micromachining techniques. On-wafer measurements showed that the filter performed with 0.7 dB insertion loss and possessed a 90 GHz cutoff frequency. This result represents some of the first planar filter measurements reported in *W*-band.

Studies of a new transmission line, the shielded membrane microstrip (SMM) line, indicated that the line is well suited to broad band applications, including high-frequency applications in *W*-band. A 25 GHz half-wavelength resonator demonstrated a very uniform response, even at the fourth resonant frequency of 100 GHz. Quality factor values extracted from the resonator measurements lead to the conclusion that attenuation in SMM lines is governed only by conductor losses, with no dielectric or radiative losses degrading the performance.

The excellent propagation characteristics of SMM line were further validated by two SMM circuits. First, bandpass filters based on conventional coupled-line technology demonstrated superior performance, with insertion losses dominated only by ohmic loss in the conducting strips. The insertion loss roll-off in the 6.1% bandwidth filter matched theoretical predictions very well, and represents the best known performance of a narrow band planar bandpass filter in *W*-band. Second, a directional coupler designed with a high-pass response validated the ability to use ideal transmission line theory in the development of SMM circuits. The coupler performance agreed with theoretical predictions at the design frequency of 20 GHz, and exhibited the desired high-pass response. This is the first report of a directional coupler with an operating frequency range extending from *X*-band all the way through *W*-band.

In each of the circuits that were measured in *W*-band, performance levels are compared to those of conventional substrate-supported circuitry through the use of computer simulations and models. From these comparisons, it is evident that the parasitic mechanisms of dispersion and radiation loss which degrade the performance of substrate-supported circuits are effectively eliminated from the responses of membrane-supported circuits. The high levels of performance achieved by the membrane-supported circuits validate the expectation that the application of micromachining technology to *W*-band circuits results in significant benefits.

## 6.2 Future Work

There are myriad possible directions for the future of micromachining in the field of *W*-band circuit development. The technology base being generated by the MEMS community continues to grow and provide new possibilities for

micromachining in RF applications [62]. In addition, the new emphasis on packaging and mixed-signal MMIC's presents opportunities for new ways to incorporate micromachining into W-band circuit applications.

### *Au-Sn Eutectic Bonding*

To date, micromachined millimeter-wave structures have been assembled by hand, using simplified bonding methods such as silver epoxy. An automated bonding process which could be integrated into the standard fabrication of the micromachined structures would greatly reduce fabrication costs and improve reliability. Thin-film bonding techniques, such as gold-tin (Au-Sn) eutectics could be used to great advantage to help integrate the assembly into the fabrication of micromachined structures. The optimization of a repeatable Au-Sn bonding process utilizing photolithographic techniques should be pursued in order to allow easier integration of micromachined and micropackaged components.

### *Micromachined Vertical Interconnects*

Interconnection to membrane supported lines remains one of the factors limiting the ability of SMM and microshield line to be easily integrated with active devices and substrate-supported circuits. One way to address this problem might be the development of a vertical transition through one or more wafers that will allow membrane supported circuits to exist on entirely separate wafers from any other active circuits. This method would have the advantage of creating a sub-wafer-level package for the membrane-supported elements of a system that could be isolated from the wafer-level devices such as transistors or diodes.

### Improved Wideband Transition to SMM using FGC Lines

Perhaps a better and more compact way to transition from the coplanar probe pads to the SMM line would be to use the newly developed finite ground coplanar (FGC) lines being studied at the University of Michigan [63],[64]. An advantage of these lines is their ability to confine the propagating fields near the surface of the substrate, thereby reducing their dependence on the height of the substrate and the presence of a lower ground plane. This would make it possible to construct a line over the sloping side wall of the membrane cavity that would be relatively unaffected by the change in substrate thickness leading to the edge of the membrane. The same type of Klopfenstein taper that has been used in the work presented previously could be employed here, with the advantage that it would require only approximately 30% of the length needed for the microshield taper. It might be necessary to extend the SMM shielding cavity over the FGC taper, so that the SMM and FGC lines would share a common ground plane, but this would need to be investigated. It might also be possible to place the end of the SMM ground cavity just at the end of the taper where the FGC line meets the membrane. In this case, the width of the SMM cavity should be made as narrow as possible in order to bring the ground contact points as close as possible to the edges of the FGC line.

### Membranes on Si-Ge Substrates

Recent developments in Si-Ge technology [65],[66] have sparked much interest in the use of silicon substrates for RF and microwave active circuit applications. As Si-Ge technology advances to higher frequency ranges, the development of high-performance microwave amplifiers and nonlinear circuits will benefit from the ability to integrate membrane supported structures such as microshield lines and membrane lumped elements [16] onto the same sub-

strate as the active devices. This would require the development of a technology for integrating the growth of the necessary dielectric layers ( $\text{SiO}_2$  and  $\text{Si}_3\text{N}_4$ ) into the process for creating the Si-Ge layer that will be used for transistors and diodes. Since the major benefit of Si-Ge is that it is compatible with standard Si processing techniques (including dielectric film growth and deposition as well as bulk Si micromachining) it should be imminently possible to incorporate membrane technology with Si-Ge devices. An alternate technique for integrating active devices with membrane components is the incorporating of membrane steps into GaAs processing. This technology is being developed with PECVD films [67] but it is not apparent at this point that PECVD films can produce membranes with the high levels of strength and rigidity in the membranes produced by Si processing techniques.

## **APPENDICES**



## APPENDIX A

# A FOLDED-SLOT ANTENNA AND QUASI-OPTICAL MIXER

### A.1 Introduction

Planar circuit designs are advantageous for producing millimeter-wave integrated circuits because they can be easily fabricated using monolithic techniques. Uniplanar circuit structures such as coplanar-waveguide (CPW) and slotline are especially useful since they eliminate the need for via holes or backside metallization and can be integrated with solid-state devices on a single surface [4]. In the past, planar microwave and millimeter-wave receivers have employed quasi-optical techniques to achieve compact size and reduced transmission line loss [68]-[70]. Also, planar quasi-optical receivers have exploited symmetry to realize balanced mixers [71].

The work described here explores the realization of a quasi-optical mixer with uniplanar structures. First, the folded-slot antenna is investigated as a planar quasi-optical mixing element. Then, slotline and CPW structures are used to implement the local oscillator (LO) feed network and the low-pass intermediate frequency (IF) filter. In the circuit configuration of Figure A.1, diodes are mounted in the slots of the antenna to provide mixing between the received radio frequency (RF) and injected LO signals. The mixer achieves balanced mixing with good conversion loss and high port-to-port isolation.

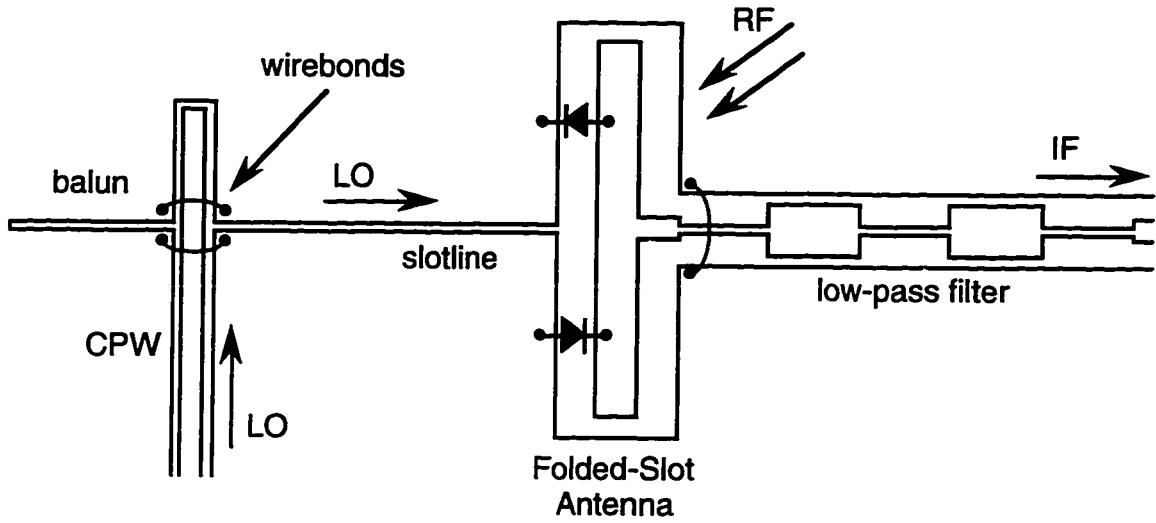


Figure A.1: Schematic layout of the folded-slot balanced mixer circuit.

## A.2 Folded-Slot Antenna

The development of the folded-slot antenna was based on previously published work on coplanar-waveguide antennas [70]-[73] and was first proposed as a microshield line antenna by Rexberg *et al.* [74]. Two main characteristics of the folded-slot antenna make it especially useful for a quasi-optical mixing application: (1) it has a planar geometry, and (2) it has the ability to support two orthogonal resonant modes.

Theoretical analysis of the antenna based on a space-domain integral equation (SDIE) method [75] shows that the folded-slot antenna is at first resonance when the length of the slots is approximately equal to half of the guided wavelength. This resonance can exist for both a CPW feed, which excites an even mode, and a slotline feed, which excites an odd mode. Figure A.2 depicts the field distributions of both of these modes for a folded-slot antenna in the first resonance. In the even mode (CPW feed) the field distribution in the slots is similar to the current distribution on a folded dipole, and the slots radiate in phase. In the odd mode (slotline feed) the slots are

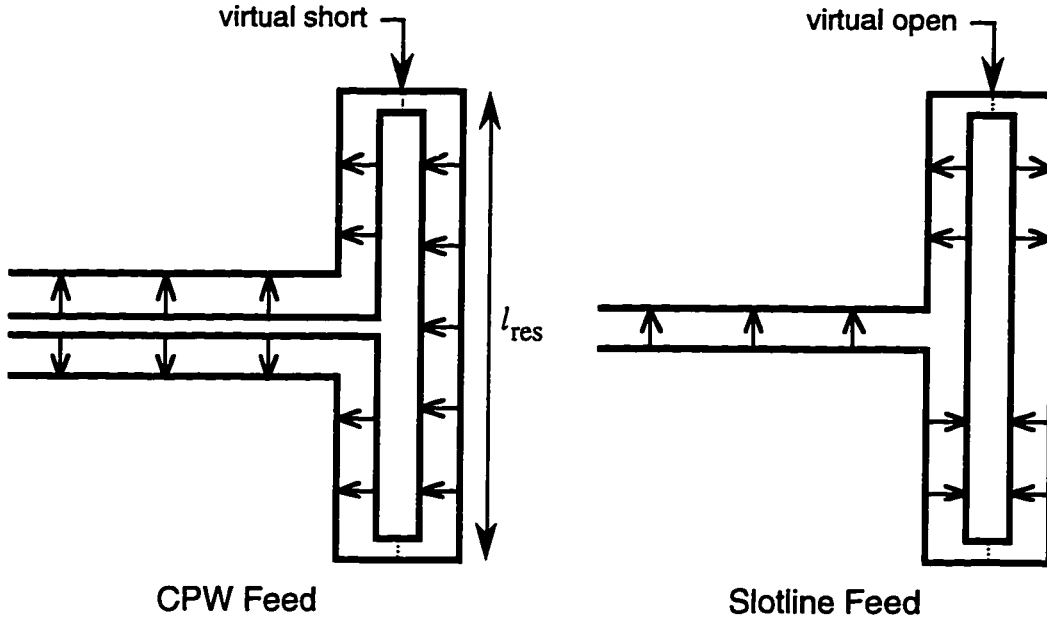


Figure A.2: Field distributions in a half wavelength folded-slot. The CPW feed excites the even (radiating) mode, and the slotline feed excites the odd (non-radiating) mode.

excited with a  $180^\circ$  phase difference, and therefore do not radiate. It is possible to excite both odd and even modes simultaneously by feeding the antenna from opposite sides with a CPW and a slotline. In this case, the two modes will not couple to each other since they are orthogonal. Feeding the antenna on adjacent sides with similar feed lines (either both CPW or both slotline) achieves the same result. Alternatively, similar feeds on opposite sides of the antenna will couple to the same mode with a  $180^\circ$  phase difference at the two feed points. In this work, the folded-slot mixer receives the RF quasi-optically in the even mode, and a slotline excites the LO in the odd mode. Thus intrinsic isolation between the two orthogonal modes serves the purpose of RF/LO isolation.

The radiating properties of the folded-slot antenna are similar to those of the single slot. Theory predicts broad E-plane patterns, and this implies that

the size of the ground plane will affect the far field radiation. The measurements shown in Figure A.3 demonstrate that, in fact, the patterns are significantly affected by ground plane truncation. E- and H-plane patterns measured at 11.44 GHz for a CPW-fed folded-slot antenna fabricated on a very thin teflon substrate with  $\epsilon_r \approx 2.0$  are markedly different for two different size ground planes. Measurements of a folded-slot antenna with a 7.5 cm diameter circular ground plane (Figure A.3(a)) show that ground plane truncation causes 7-8 dB dips in the pattern due to diffraction effects. As shown in Figure A.3(b), increasing the size of the ground plane eliminates the dips in the pattern, but causes a ripple. This effect has been predicted by studies on disk patch antennas [76]-[77], and is in agreement with previous measurements on similar types of planar antennas [69]-[70].

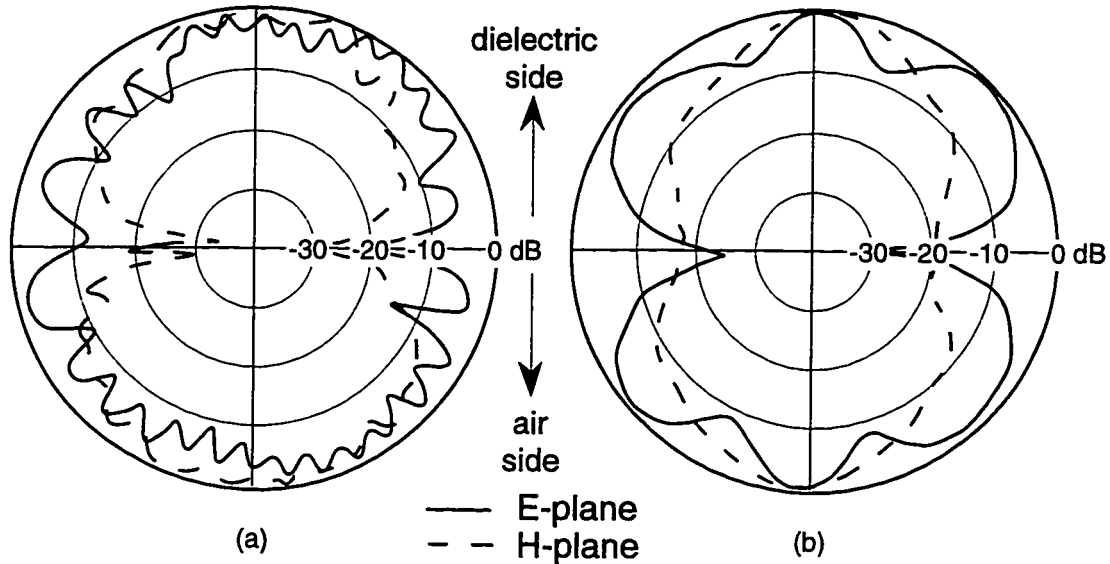


Figure A.3: Measured patterns of a) a CPW-fed folded-slot antenna at 11.44 GHz with a 7.5 cm diameter circular ground plane, and b) a CPW fed folded-slot antenna at 11.44 GHz with a 35x35 cm square ground plane.

In order to solve the problems associated with finite ground plane dimensions, the antenna may be integrated on a substrate lens [68],[78]. The lens simulates an infinite dielectric substrate and eliminates the parasitic radiation caused by surface waves. Also, with the addition of a substrate lens, the antenna radiates most of its power into the dielectric (a ratio of  $\epsilon_r^{3/2} : 1$  power radiated into the dielectric vs. power radiated into air), resulting in unidirectional radiation patterns.

### A.3 Quasi-Optical Mixer Circuit Design

#### A.3.1 CPW-to-Slotline Balun

Implementation of the folded-slot mixer requires planar circuits for the LO pumping network and the IF output filter. Connections to the circuit are made with SMA type coaxial connectors. Because of the transforming properties of the transition from SMA to CPW [79], a characteristic impedance ( $Z_0$ ) of 70  $\Omega$  is used for all transmission lines. In order to feed the LO into the mixer with a slotline, a transition from CPW to slotline is necessary. A 4-port balun transition [80] was selected for this purpose due to its simplicity. The balun (see Figure A.1) consists of an open-circuit quarter-wavelength CPW stub ( $l_{\text{cpw}} = 2.95$  mm,  $Z_{\text{cpw}} = Z_0$ ), and a short-circuit quarter-wavelength slotline stub ( $l_{\text{slot}} = 3.63$  mm,  $w_{\text{slot}} = 100$   $\mu\text{m}$ ,  $Z_{\text{slot}} = Z_0$ ). The insertion loss of back-to-back baluns fabricated on a RT/Duriod substrate ( $h = 1.27$  mm,  $\epsilon_r = 10.5$ ), including SMA-to-CPW transitions, was measured to be less than 3 dB up to 12 GHz, as shown in Figure A.4.

The IF output of the mixer couples into the even mode of the antenna [81] and is extracted by a CPW line. To prevent the RF from coupling to the CPW line, a stepped impedance low pass IF filter is used. Since this is a quasi-opti-

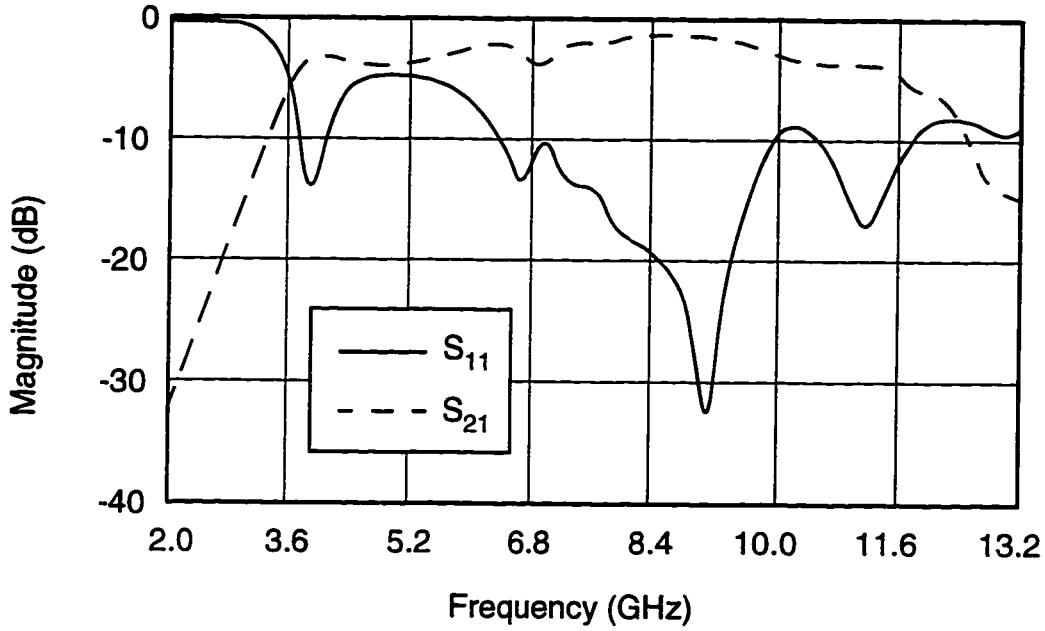


Figure A.4: Measured response of back-to-back CPW-to-slotline baluns.

cal circuit and the mixing occurs within the antenna itself, the IF filter should be designed so as not to disturb the RF fields. This is accomplished by using quarter-wavelength sections in the filter and presenting an open circuit to the RF fields at the IF/antenna connection. The IF filter has a 3 dB response at 6.4 GHz, and -18 dB rejection at 11 GHz.

In order to maximize the LO power available to the diodes, the folded-slot antenna used in the mixer is designed to be resonant for the 100  $\mu\text{m}$  slotline feed. Results of the SDIE analysis give an antenna with a slot length  $l_{\text{res}}$  of 6 mm, a slot width of 500  $\mu\text{m}$ , and a slot separation of 500  $\mu\text{m}$ . The end slots are 200  $\mu\text{m}$  wide.

### A.3.2 Diode Embedding Impedances

Further attention is given to the placement of the diodes in an effort to determine suitable embedding impedances. The magnetic current distribution obtained from SDIE analysis of a CPW-fed slot is seen to have a peak at the center of the antenna slot, with decreasing values towards each end. In an effort to understand how this magnetic current distribution relates to the RF impedance distribution in the slot, impedance measurements were performed on a low frequency model of the folded-slot antenna. The model was fabricated on StyCast ( $\epsilon_r = 12$ , thickness = 6.35 mm) and was designed to operate at 1/5 of the original 10 GHz design frequency. Copper tape was applied to the Sty-Cast substrate and cut to define the slots of the antenna. A coaxial balun probe was used to measure the input impedance of the antenna at various positions along the coupled slot of the antenna. The magnitude of this measured impedance is plotted against position along with the magnetic current distribution from the SDIE analysis in Figure A.5. The two curves show similar shapes, and this agreement verifies the assumed distribution of the electric fields in the folded-slot antenna.

The impedance information presented above could be used to select the location of the two mixing diodes based on the RF embedding impedance presented to the diodes. But this is only helpful if similar information is available for the LO embedding impedance of the diodes. It was much more difficult to measure this impedance, however, due to the sensitive nature of the slotline feed of the folded-slot antenna. Ultimately, it was decided that the diodes should be placed centrally on either side of the LO feed to try to maximize the amount of RF and LO signal incident on the diodes.

The mixer circuit is fabricated using wet etching on a circular copper clad RT/Duroid substrate with a dielectric constant of 10.5, a diameter of 7.5 cm,

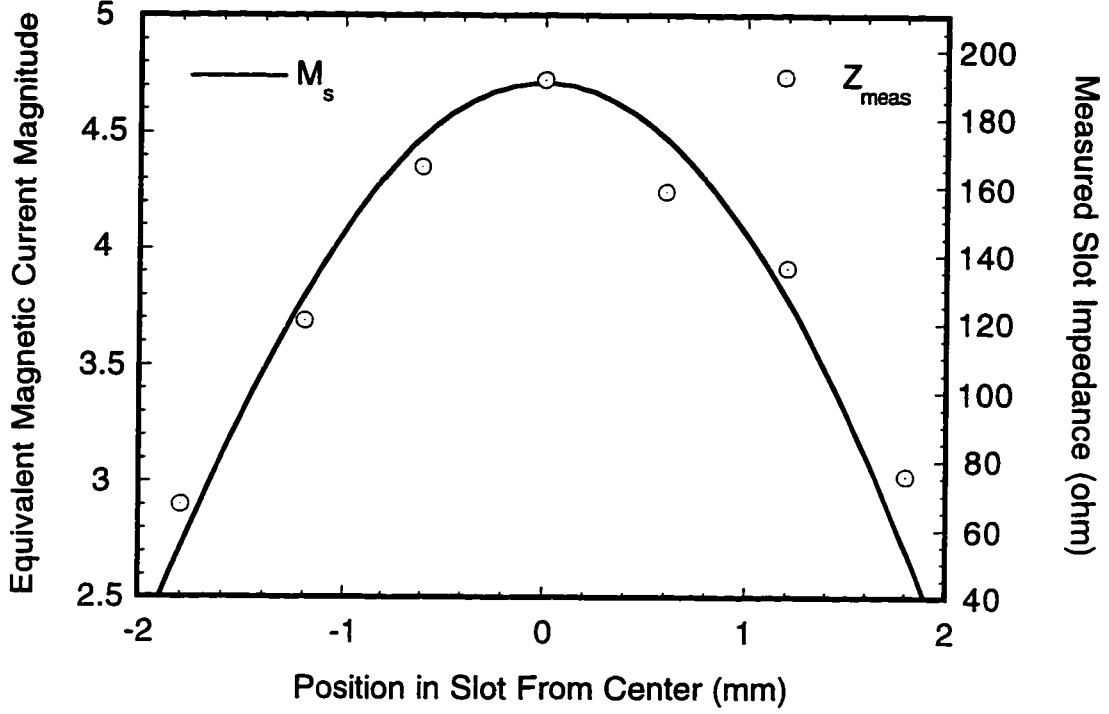


Figure A.5: Comparison of the magnetic current distribution predicted by the SDIE analysis and the slot impedance distribution measured at 2 GHz with the coaxial balun probe on the 1:5 scale model.

and a thickness of 250  $\mu\text{m}$ . The mixer diodes (Hewlett-Packard HSCH-5320,  $C_T = 0.10$  pF,  $R_s = 15$   $\Omega$ ) are mounted symmetrically about the slotline feed in an anti-parallel configuration (see Figure A.1). Balanced mixing occurs since the diodes receive the RF signal  $180^\circ$  out of phase and are pumped in phase by the LO [81].



## A.4 Measurements

### A.4.1 Radiation Patterns

Radiation patterns of the mixer itself (see Figure A.6) were obtained at 11.8 GHz by using the diodes as detectors. The RF patterns of the mixer are very similar to the measured patterns of the CPW fed folded-slot. Both patterns show the 8-10 dB dips caused by ground plane truncation. The directivity of the antenna on the dielectric side is estimated to be  $D_{fs} \approx 7$  dB by numerical integration of a full two-dimensional pattern.

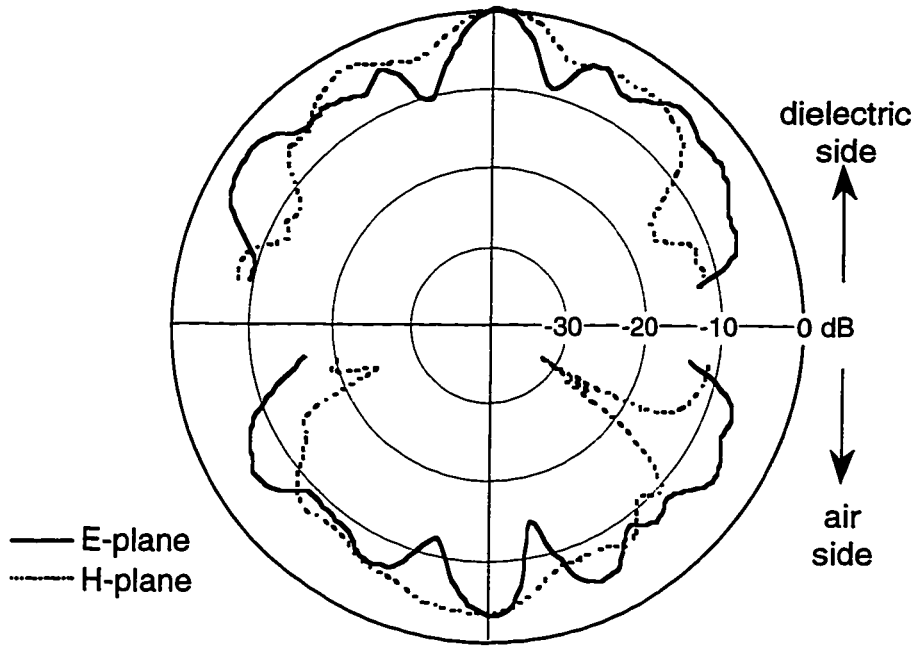


Figure A.6: Measured RF patterns of the folded-slot quasi-optical mixer using the mixer diodes as detectors at 11.8 GHz.

### A.4.2 Mixer Performance

The Friis transmission experiment shown in Figure A.7 is used to characterize the mixer. A standard gain horn illuminates the mixer with an RF plane wave, while a separate source provides the LO through the slotline feed via the CPW-to-slotline balun. The IF is extracted through the low-pass filter, and is amplified and then measured on a spectrum analyzer or power meter.

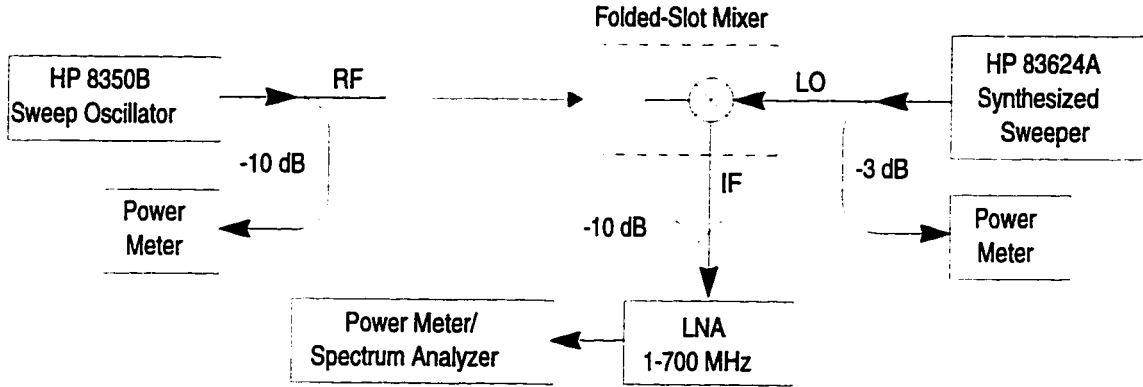


Figure A.7: Friis transmission experiment for characterization of the folded-slot quasi-optical mixer.

The mixer conversion loss is defined as the available RF power at the antenna “terminals” divided by the measured IF power. Since the antenna itself is integrated into the mixer circuit, the RF “terminals” are not accessible. Therefore, the available RF power must be defined by in terms of the effective aperture,  $A_{eff}$ , of the antenna as shown in Eqn. A.1:

$$P_{RF} = S_r \cdot A_{eff} = \left( \frac{P_t G_t}{4\pi R^2} \right) \left( \frac{\lambda^2}{4\pi} D_{fs} \right) \quad (\text{A.1})$$

$S_r$  is the incident RF power density and  $P_t$  is the RF power transmitted by the standard gain horn with gain  $G_t$ . The conversion loss of this mixer can then be found using Eqn. A.2

$$L_c = \frac{P_{RF}}{P_{IF}} = \frac{P_t G_t \left( \frac{\lambda}{4\pi R} \right)^2 D_{fs}}{P_{meas, IF} / G_{IF}} \quad (\text{A.2})$$

where  $G_{IF}$  is the measured gain of the IF path.

A minimum SSB conversion loss of 8.2 dB is measured for  $f_{RF} = 11.6$  GHz,  $f_{LO} = 11.0$  GHz, and  $P_{LO} = 8$  dBm, as shown in Figure A.8. The mixer has good port-to-port isolation, with -18 dB RF/IF isolation and at least -30 dB LO/IF isolation at the point of minimum conversion loss.

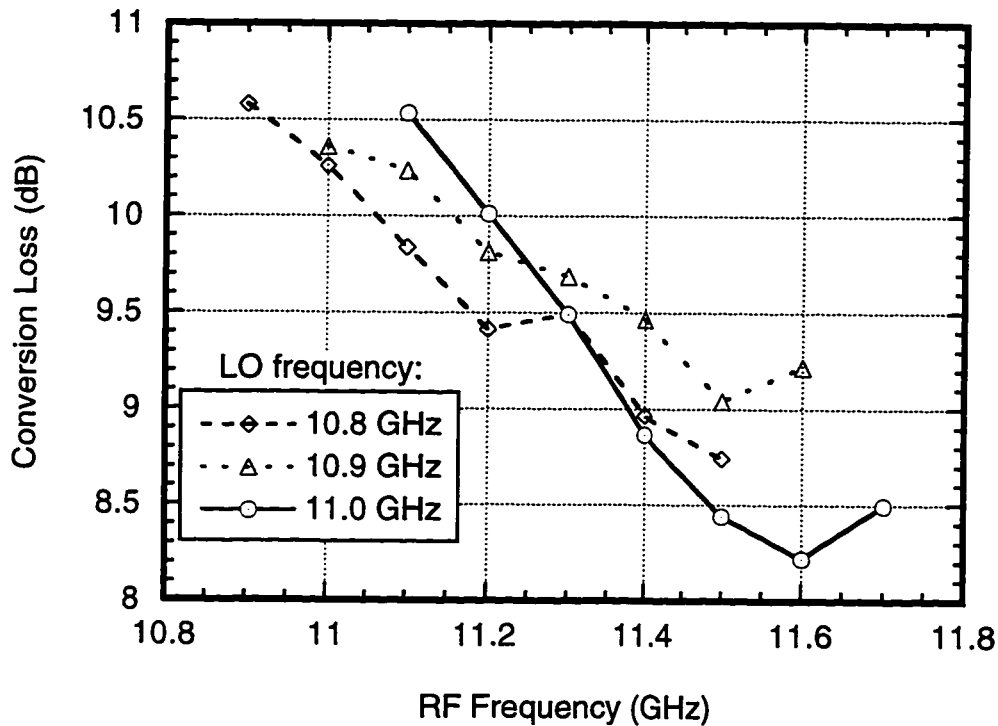


Figure A.8: Measured conversion loss of the folded-slot mixer vs. LO frequency (see text for definition of conversion loss).

The mixer can also be characterized by the *isotropic conversion loss*, which is defined as the conversion loss that would be obtained if the mixer were assumed to have an ideal isotropic radiating element [69]. The isotropic conversion loss can be calculated from Eqn.A.2 by setting the antenna directivity,  $D_{fs}$ , equal to one. For the folded-slot mixer the conversion loss of 8.2 dB includes the measured antenna directivity of 7 dB and corresponds to an isotropic conversion loss of 1.2 dB. This compares well to the measured isotropic conversion loss of approximately 3 dB at 10.1 GHz for a coupled-slot quasi-optical receiver with a non-planar feed structure [70].

## A.5 Conclusions

A planar quasi-optical mixer has been presented. The mixer achieves RF/LO isolation through the use of orthogonal modes in a folded-slot antenna, without RF filters or a subharmonic LO. Balanced mixing is achieved with good conversion loss and high port-to-port isolation. The uniplanar design of the mixer is suitable for monolithic fabrication, which extends the circuit's usefulness into the millimeter-wave frequency range. The mixer may be integrated on a substrate lens at millimeter-wave frequencies to eliminate the problem of surface modes.

## A.6 Acknowledgments

Work on the folded-slot antenna and mixer was supported by Texas Instruments, Inc. Pattern measurements of the CPW-fed folded-slot were performed by Dr. Guysik Yang of Korea Maritime University.

## **APPENDIX B**

# **SELF ALIGNMENT OF MICROMACHINED STRUCTURES USING GLASS MICROSPHERES**

### **B.1 Introduction**

Many of the micromachined microwave transmission lines and circuit elements developed to date rely on multiple wafers and micromachined pieces to complete their assembly [17],[52],[41]. In many cases, the multiple pieces must be aligned before being bonded together. For example, in the case of a shielded microwave transmission line, To date, most of the bonding procedures reported for micromachined circuits have employed silver epoxy or photoresist to adhere circuit pieces together, but there are many other technologies in wide use in the MEMS community which could be applied in various ways to micromachined RF circuits. These include, but are not limited to, soldering, eutectic bonding, and electrostatic bonding [82],[83]. Regardless of how the micromachined circuits are to be assembled, if alignment of one or more pieces is required, then special measures must be taken to ensure that the structure remains aligned during and after the bonding step. This can be accomplished by integrating the alignment apparatus with the bonding apparatus, but this may be difficult or cumbersome in some instances. In such cases, it would be very helpful to employ a method of self alignment between the two pieces, such that their final alignment is independent of the process used to bond them together.

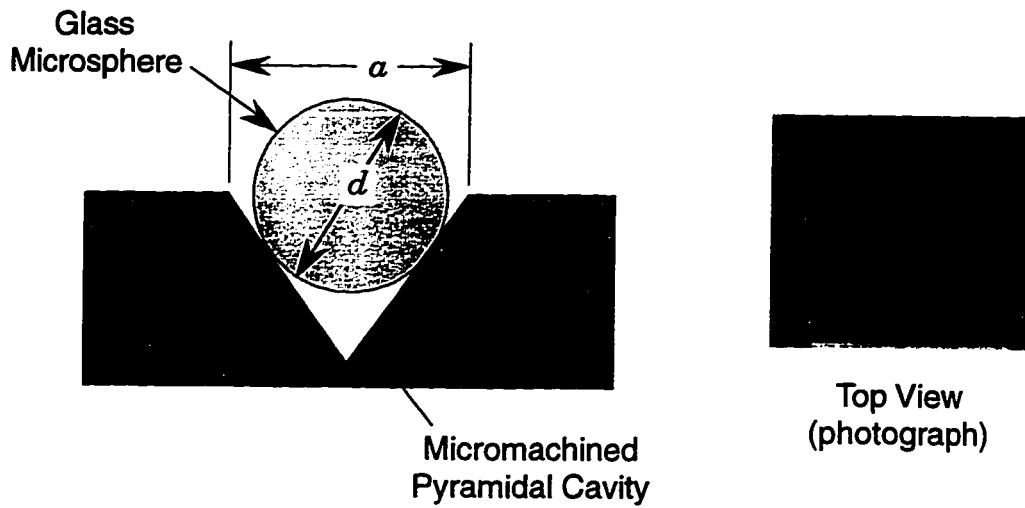
This appendix will present a method that has been used to align micromachined wafer pieces together before bonding occurs. The technique relies on the use of glass microspheres and anisotropically etched pyramidal cavities in the surfaces to be aligned [84]. The pieces can be aligned as they are brought into contact without the need for x-y-theta manipulation, and once aligned they may be bonded using whatever method is desired.

## B.2 Alignment Technique

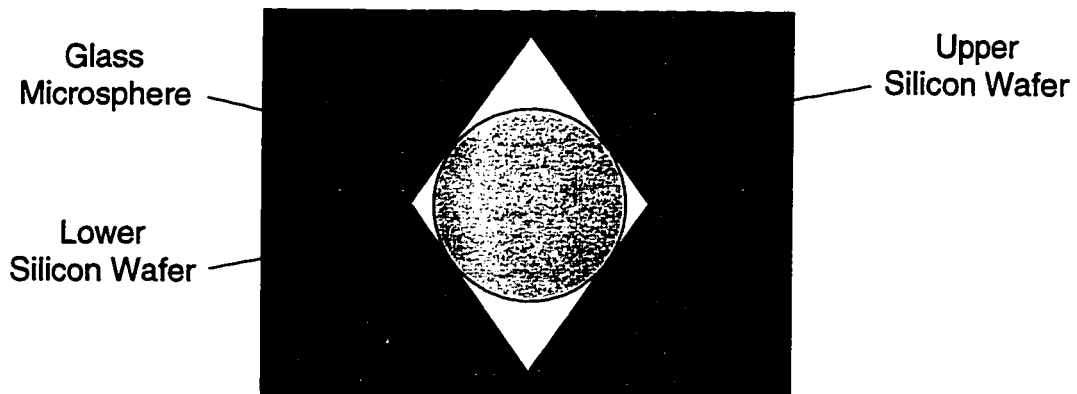
The self-alignment of micromachined structures can be accomplished by capturing glass microspheres in small pyramidal cavities that have been etched into the structures to be aligned. The cavities are created during the bulk micromachining step by square openings in the masking layer (usually SiO<sub>2</sub>, patterned with BHF), which are placed in the desired alignment positions on each micromachined piece of the structure. The cavity dimensions are chosen so that when the etch is completed, a glass microsphere can rest inside each cavity as shown in Figure B.1(a), such that half of the sphere remains above the surface of the wafer. Since the profile of the cavity is determined by the 54.74° angle of the <111> plane etch stop, the length,  $a$ , of one side of the square opening in the masking layer can be expressed in terms of the diameter,  $d$ , of the sphere as follows:

$$a = d \cdot \sec(54.74^\circ) = 1.225d \quad (\text{B.1})$$

The spheres resting in the alignment cavities of the lower micromachined wafer piece act as alignment bumps which can be captured by alignment cavities in the upper micromachined piece. The spheres allow the two wafers to come into contact only when they are completely enclosed by both of the alignment cavities, as illustrated in Figure B.1(b). To achieve bonding, any of the



(a)



(b)

Figure B.1: Schematic representation of the microsphere self-alignment technique. (a) A glass microsphere rests in the alignment cavity of the lower wafer piece. The photograph is taken looking directly down on sphere and cavity. (b) The microsphere is completely enclosed by the alignment cavities as the upper wafer piece is brought into contact with the lower wafer piece.

methods mentioned previously may be employed. The spheres are ground from a soda lime glass [85] and are able to withstand a wide range of temperatures and most of the environmental conditions that may be required for a given bonding technique.

The microsphere self-alignment technique was utilized in the attachment of the ground plane cavity wafer to the circuit wafer of an SMM transmission line structure. Spheres with nominal diameter of  $596\text{ }\mu\text{m}$  were placed in square alignment cavities that were defined with  $740 \times 740\text{ }\mu\text{m}$  square openings and micromachined in EDP. The wafers were bonded together using silver epoxy [86], which was manually applied to the ground plane wafer and then cured for 30 minutes at  $110^{\circ}\text{C}$  after the wafers were brought into contact. The cavity wafer was observed to be in good alignment with the lower circuit wafer, and the circuit assembly technician was observed to have a much better attitude about aligning micromachined shielding cavities.

### **B.3 Conclusion**

Small glass microspheres have been used in conjunction with micromachined pyramidal cavities to form a self-alignment mechanism for micromachined silicon wafers. The technique can be applied whenever two micromachined wafers need to be aligned and then bonded together. The glass microspheres are rigorous enough to withstand virtually any method used to bond the two wafers together after they have been aligned.



## APPENDIX C

# MILLIMETER-WAVE THIN-FILM RESISTORS

### C.1 Introduction

Various microwave and millimeter-wave applications require the integration of resistors into planar circuit structures. These include Wilkinson power dividers, fixed phase shifters, attenuators, matching networks, and sum and difference networks [87] that utilize 4-port couplers with matched terminations at one or more ports. In addition, measurements of 4-port circuits such as couplers are often performed using a 2-port network analyzer, and matched terminations must be utilized at the two unmeasured ports. If possible, additional wafer probes, which are immediately terminated in matched loads, should be connected to the unmeasured ports. In cases where 4 microwave probes and probe positioners are not available, it may be necessary to create a matched termination directly on the wafer surface. For this reason, an on-wafer method for terminating the unmeasured ports of a 4-port network was investigated.

The on-wafer termination involved the use of planar thin-films to create lumped element resistors. These resistors were studied in various Coplanar Waveguide (CPW) configurations to determine an effective way to terminate a  $50\ \Omega$  planar transmission line. Fabrication and testing of a termination using Nichrome thin films in a parallel configuration is discussed in detail.

## C.2 Resistor Design and Fabrication

The planar resistors are formed by patterning a thin film of Nichrome (Nickel-Chromium alloy) which, in this case, is 40% Cr by weight [88]. Nichrome films have found wide use as resistors (both thin-film and bulk) in industrial microelectronics applications [89]. The material is vacuum evaporated directly on to the circuit surface from a single source, or crucible. For the purposes of this study, the films have been patterned using a lift-off process. The process relies on a relatively thick film of photoresist (PR), since the evaporated Nichrome film is under a fairly high tensile stress and can peel up the photoresist pattern in some instances. The following recipe using AZ 5214 PR and an image reversal technique has been found to produce satisfactory results:

1. Clean the sample in a 1.2:1 ratio of concentrated Sulfuric Acid ( $\text{H}_2\text{SO}_4$ ) : DI water for a minimum of 10 min. Optionally, the sample may be cleaned by soaking in hot Acetone (ACE) and Isopropyl Alcohol (IPA) for one min. each. Dry with nitrogen ( $\text{N}_2$ ).
2. Dehydrate bake the sample on a 130° C hot plate for 2 min.
3. Spin coat Hexamethyldisilazane (HMDS) adhesion promoter and AZ 5214 PR for 30 sec. each at a speed of 2.5 krpm.
4. Soft bake the sample on a 105° C hot plate for 1 min.
5. (Optional) Align and expose any square edges or corners of the sample with an edge bead removal mask for 20 sec. at an ultraviolet (UV) light intensity of 20 mW/cm<sup>2</sup>.
6. (Optional) Develop the sample in AZ 312 MIF developer for 1 min.

7. (Optional) Remove any PR remnants from the edges and corners of the sample with an ACE swab.
8. (Optional) Soft bake the sample on an 80° C hot plate for 1 min.
9. Align and expose the sample with the metallization pattern mask for 4 sec. at a UV light intensity of 20 mW/cm<sup>2</sup>.
10. Reversal bake: hard bake the sample on a 130° C hot plate for 1 min.
11. Flood expose: expose the sample with no mask for 90 sec. at a UV light intensity of 20 mW/cm<sup>2</sup>.
12. Develop the pattern in AZ 327 MIF developer for 40-60 sec.  
Inspect the patterns and continue developing in increments of 10 sec. if the undercut does not appear to be well established.

The steps listed as “Optional” in the above recipe are referred to as “Edge Bead Removal” [90] and may be omitted. They should be included whenever the sample possesses “square” or cleaved edges which accumulate photoresist beads during spinning, and feature dimensions become less than about 20  $\mu\text{m}$ . Also, when using quarter wafer pieces that have two cleaved edges and one round edge, the presence of photoresist beads on the square edges of the sample may lead to non-uniform mask contact, since the rounded edge will not accumulate beads. This can be especially problematic in cases such as resistor formation where uniformity across the circuit can be compromised by uneven mask contact.

Additionally, it has been observed that lift-off of Nichrome films often leaves a fine particulate residue on the sample. This is caused by fragmentation of the film, which occurs when the photoresist underneath the highly tensile Nichrome dissolves in ACE during the lift-off step. The resulting Nichrome particles may be as small as a few micrometers in diameter, and as

they float randomly in the ACE they may redeposit on the surface of the sample. One solution to this problem may be to use chromium etchant (e.g. CR-14) to pattern the Nichrome film (evaporated Nichrome films have a much higher chromium content than the alloy source, due to differences in vapor pressure between the nickel and chromium constituents of the source). Chromium etchant has proven quite effective for patterning of Nichrome films, and can be masked with a thin layer of photoresist. A 400 Å film of Nichrome will etch in CR-14 in about 1-1.5 minutes, with good pattern transfer characteristics from a photoresist mask such as PR 1813.

A possible concern with Nichrome films is their potential volatility under varying atmospheric conditions. Problems have been avoided during these experiments by keeping the films at temperatures below approximately 200°C. Other methods which may be required are annealing and/or passivation.

The Nichrome films evaporated in the Solid State Electronics Laboratory (SSEL) at the University of Michigan have been found to have a bulk resistivity of approximately  $135 \mu\Omega\text{-cm}$ . This was determined from measured sheet resistances of several Nichrome films of varying thickness, as plotted in Figure C.1. This plot also demonstrates the surface effects which influence the sheet resistivity of films thinner than approximately 400 Å. For such thin films, sheet resistance cannot be determined from the bulk resistance value mentioned earlier and must be determined experimentally.

Once the sheet resistance for a particular Nichrome film thickness has been determined, the design of planar resistors is quite straightforward; a desired resistance value can be synthesized simply by forming a Nichrome rectangle with the correct surface area. The first step is to select the width of the resistor; usually this is the narrowest width that can be easily and repeat-

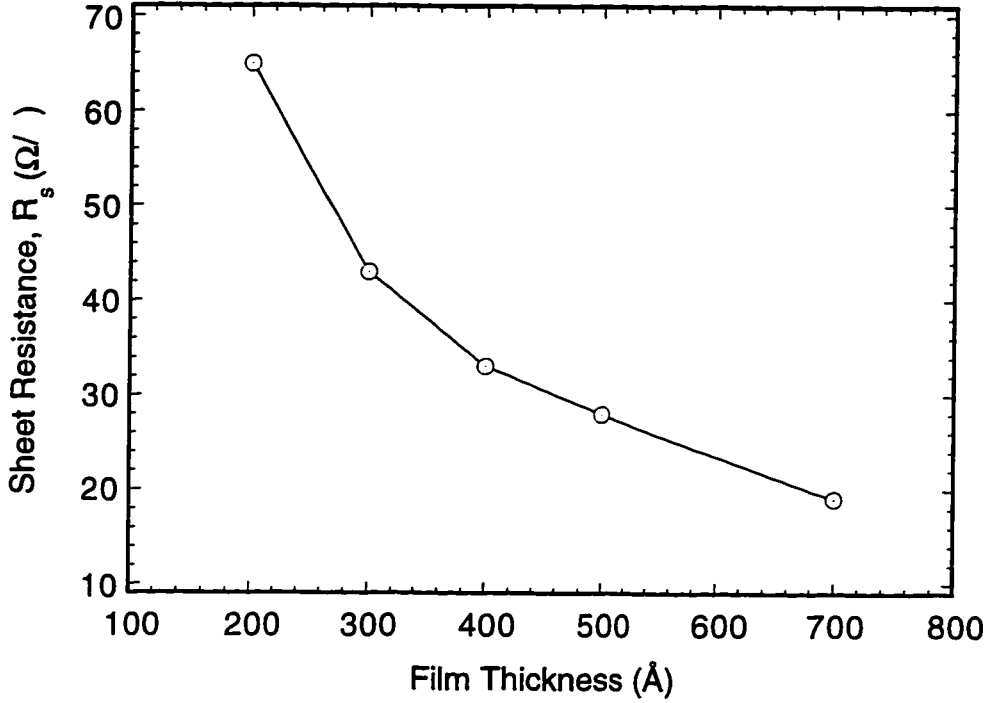


Figure C.1: Measured sheet resistances for evaporated Nichrome films.

edly fabricated. Next, the desired resistance value (in  $\Omega$ ) is divided by the sheet resistance of the film (in  $\Omega/\text{square}$ ) to find the surface area in squares. Finally, the number of squares is multiplied by the selected width to find the length of the resistor. To make sure the resistor behaves as a lumped element, the length must be limited to no more than 1/10 of the guided wavelength at the highest frequency of operation.

### C.3 Coplanar Waveguide Terminations

The planar resistors discussed until now are best suited for applications employing CPW-type structures, since they can be connected from signal to ground without the need for vias. For this reason, it was decided to study the performance of matched terminations for Finite Ground Coplanar (FGC) lines.

The FGC lines are similar to conventional CPW but their truncated upper ground planes give them advantages at millimeter-wave frequencies [63],[64]. Since they are so well-behaved at high frequencies, they are an excellent platform with which to study the performance of the thin-film resistors.

The layout of the FGC test structure and the thin film resistors is illustrated in Figure C.2. The FGC line is designed to have a characteristic impedance of approximately  $50\ \Omega$ , with center conductor width, gap spacing, and ground plane width of  $60\ \mu\text{m}$ ,  $35\ \mu\text{m}$ , and  $200\ \mu\text{m}$ , respectively. The resistor dimensions are chosen to realize two  $100\ \Omega$  resistors in parallel using a  $400\ \text{\AA}$  Nichrome thin film with a sheet resistance of  $33\ \Omega/\text{square}$ . The final dimensions of the fabricated resistors are  $35\ \mu\text{m} \times 12\ \mu\text{m}$ , or 2.9 squares, and the measured DC resistance of the termination is approximately  $51\ \Omega$ . Note that two resistors are placed in parallel instead of a single resistor in series to the CPW ground plane [91]. Two resistors combined in parallel as shown have proven to be a much more effective termination than a single resistor at fre-

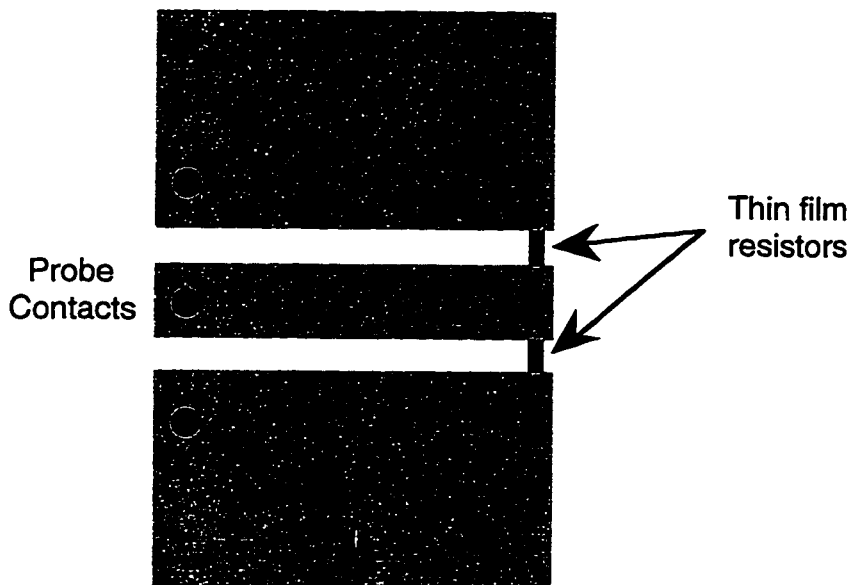


Figure C.2: Layout of thin-film resistors used as the matching termination of a finite ground coplanar transmission line.

quencies above 40 GHz. This is demonstrated by the measured results, seen in Figure C.3, which show that the termination provides an input return loss of better than 20 dB as high as 118 GHz.

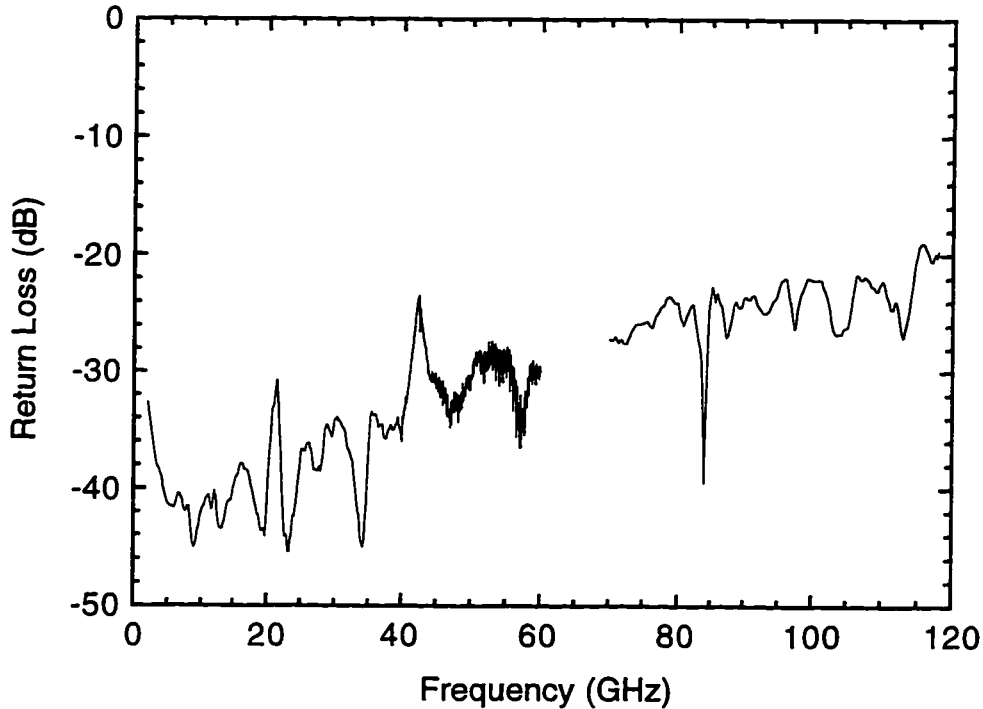


Figure C.3: Measured performance of a thin-film lumped element termination up to 118 GHz.

## C.4 Conclusions

Nichrome thin films have demonstrated their efficacy as millimeter-wave resistors that can be easily integrated into planar microwave integrated circuit processes. The resistors have been used to build on-wafer matching terminations that provide better than 20 dB input return loss at frequencies as high as 118 GHz.

## APPENDIX D

# DESIGN AND FABRICATION OF MIM CAPACITORS

### D.1 Introduction

This Appendix will present a design and fabrication methodology for creating metal-insulator-metal (MIM) capacitors for use with monolithic microwave integrated circuits. Fabrication of the capacitors is based on standard processing techniques, including contact photolithography and evaporated metal and dielectric thin films. The capacitors are designed primarily for use as RF short-circuits in CPW-type transmission line geometries [92].

### D.2 Capacitor Design and Fabrication

MIM capacitors can be designed using a simple methodology based on the relation in Eqn. D.1:

$$C = \epsilon_r \epsilon_0 \frac{A}{d} \quad (\text{D.1})$$

where the capacitance,  $C$ , is given in Farads, and  $\epsilon_r$  is the relative permittivity of the dielectric layer. The factors  $A$  and  $d$  are the area of and distance between the two capacitor plates, respectively. The choice of capacitor dielectric has a significant impact on the overall design of the capacitor. For the MIM capacitors, an evaporated film of  $\text{Al}_2\text{O}_3$  with a dielectric constant of approximately 8-10 was utilized.



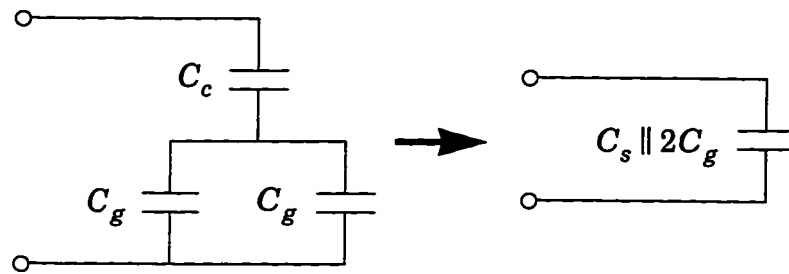
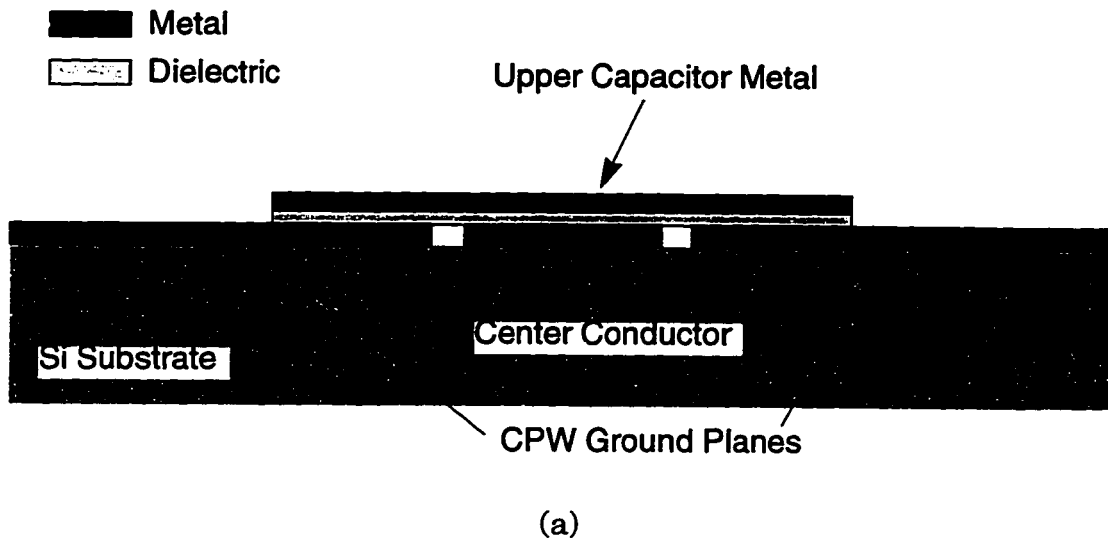


Figure D.1: (a) Cross section of the MIM capacitor structure for use as an RF short-circuit in CPW-type transmission lines. (b) Equivalent circuit representation of the capacitor structure.

In order to provide a shunt capacitance across a CPW-type transmission line, an air bridge type of fabrication technique is used to avoid problems with step coverage over the edges of the transmission line metallization patterns. To simplify the process, capacitors are deposited on top of the existing circuit metallization, with the second capacitor metal provided by an evaporated film which is deposited immediately after the capacitor dielectric. With this method, it is simpler to forego direct contact of the upper capacitor metal to

the ground plane of the CPW line and create three capacitors instead of one. This is illustrated in Figure D.1(a), which shows how the dielectric prevents the two metal layers from coming into contact. The equivalent circuit for this structure is depicted in Figure D.1(b); as long as the capacitance to the ground planes,  $C_g$ , is much larger than the capacitance to the center conductor,  $C_c$ , the equivalent capacitance is dominated by  $C_c$ , as seen in Eqn. D.2.

$$C_e = \frac{2C_c C_g}{C_c + 2C_g} \quad (\text{D.2})$$

This condition can be easily met by making the area of the ground capacitors at least twice as large as the area of the center conductor capacitor. It should be noted, however, that creating large shunt capacitors over the ground planes will limit the higher frequency operation of the capacitor. The frequency response of a typical capacitor is discussed in Section 5.5.2, and a resonance response is observed at approximately 20 GHz. Reduction of the total size of the capacitors will extend the upper frequency limit of the structure.

### D.3 Fabrication Steps

1. Clean the sample in hot Acetone (ACE) and Isopropyl Alcohol (IPA) for one min. each. Dry with nitrogen ( $\text{N}_2$ ).
2. Dehydrate bake the sample on a 130° C hot plate for 2 min.
3. Spin coat Hexamethyldisilazane (HMDS) adhesion promoter and 1827 PR for 30 sec. each at a speed of 4 krpm.
4. Soft bake the sample on a 105° C hot plate for 1 min.
5. Align and expose the sample with the “capacitor post” pattern mask for 8 sec. at a UV light intensity of 20 mW/cm<sup>2</sup>.

6. Remove the photoresist scum in a 250 mT O<sub>2</sub> plasma at 80 W for 0.6 min.
7. Contour Bake: bake the sample for 2 min on an iron chuck which has been heated to 130°C in an oven.
8. Deposit the 700 Å Ti interface layer in an evaporator.
9. Spin coat AZ 5214 PR for 30 sec. at a speed of 4.5 krpm (no HMDS required).
10. Soft bake the sample on a 105° C hot plate for 1 min.
11. Align and expose the sample with the “capacitor span” pattern mask for 4.5 sec. at a UV light intensity of 20 mW/cm<sup>2</sup>.
12. Reversal bake: hard bake the sample on a 130° C hot plate for 1 min.
13. Flood expose: expose the sample with no mask for 90 sec. at a UV light intensity of 20 mW/cm<sup>2</sup>.
14. Develop the pattern in AZ 327 MIF developer for 40-60 sec.  
Inspect the patterns and continue developing in increments of 10 sec. if the undercut does not appear to be well established.
15. Remove the photoresist scum in a 250 mT O<sub>2</sub> plasma at 80 W for 0.6 min.
16. Etch the interface Ti layer in a HF:DI H<sub>2</sub>O 1:10 solution for approximately 10 sec.
17. Deposit the capacitor dielectric and the upper capacitor metal layers in an electron beam evaporator: Al<sub>2</sub>O<sub>3</sub>/Ti/Au 1500/500/4000 Å.
18. Lift-off in heated PRS 1000 for approximately 30-60 min.

## D.4 Conclusions

A basic design procedure and fabrication process for integrated MIM capacitors have been outlined. The capacitors are formed with an evaporated  $\text{Al}_2\text{O}_3$  film, and are designed specifically for use as RF short circuits in CPW-type transmission line geometries. A fabricated capacitor has exhibited usefulness into the *Ku*-band frequency range.

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# **ABSTRACT**

## **MICROMACHINED W-BAND CIRCUITS**

by

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This dissertation presents a comprehensive demonstration of the ability of membrane-supported transmission lines to provide excellent performance in *W*-band applications. The design, fabrication, and measurements of micromachined circuits are discussed, with a strong focus on two types of membrane-supported transmission lines: the microshield line and the shielded membrane microstrip (SMM) line. The procedures for the fabrication of these structures are outlined, with treatments of thin dielectric membrane technology and bulk silicon micromachining techniques. Additionally, methods for simulation, analysis, and testing of micromachined circuits are reviewed.

A series of experimental investigations demonstrates the excellent performance levels achieved by micromachined *W*-band circuits. A 90 GHz low-pass filter is developed using the microshield line architecture and achieves one of the first known results of planar filter performance in *W*-band. Subsequently, a variety of structures are developed using the SMM technology. First, a 25 GHz end-coupled half-wavelength resonator shows conductor loss limited, dispersion-less performance over a 2-octave bandwidth. Second, coupled-line bandpass filters demonstrate excellent signal rejection performance at

94 GHz, with a 6.1% bandwidth filter displaying nearly ideal rolloff characteristics. Finally, the broad-band characteristics of SMM are exploited to create a high-pass 20 dB coupler with uniform response from 8 GHz to 118 GHz. Theoretical comparisons to conventional planar circuit elements show that membrane-supported elements achieve superior *W*-band performance.

Finally, a new direction in micromachining is explored with the development of a micromachined integrated conformal package for a *Ka*-band HEMT amplifier. The amplifier circuit is realized on silicon, with low-cost processing techniques, and utilizes a flip-chip InP High Electron Mobility Transistor for low noise gain. The measured performance of the amplifier is in good agreement with theoretical predictions, demonstrating the feasibility of creating low-cost Si-based MMICs with flip-chip devices and integrated packaging.

This thesis closes with the conclusion that micromachining techniques offer powerful advantages in the development of *W*-band circuits, including low losses and nearly ideal behavior. Several ideas are proposed for continued work in this area. The appendices provide background on uniplanar circuit development and detail additional fabrication techniques that can be applied to micromachined *W*-band circuits.