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PLANAR MICROWAVE AND MILLIMETER-WAVE COMPONENTS USING MICROMACHINING TECHNOLOGIES

Chen-Yu Chi

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by

Chen-Yu Chi

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Associate Professor Gabriel M. Rebeiz, Chairman
Professor Linda P. B. Katehi
Professor Fawwaz T. Ulaby
Associate Professor Kim A. Winick
Research Scientist Jack R. East

ABSTRACT

PLANAR MICROWAVE AND MILLIMETER-WAVE COMPONENTS USING MICROMACHINING TECHNOLOGIES

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Chairman: Gabriel M. Rebeiz

All microwave and millimeter-wave systems are made of monolithic microwave integrated circuits (MMICs) which are placed together using bond wires and discrete transmission line components (such as filters and couplers) to form microwave integrated circuits and subsystems. Most of the problems encountered in microwave circuits, being at the MMIC level or at the hybrid circuit implementation level, are due to the presence of the underlying dielectric substrate. In this thesis, we propose the use of micromachining techniques to eliminate the dielectric substrate and to create a localized low-loss and low-ϵ_r environment. The idea attacks the most basic point: How to build microwave planar circuits on very low dielectric constant substrates to eliminate dispersion and dielectric loss and to result in a TEM-wave, while still being compatible with standard silicon and GaAs processing techniques. The low-ϵ_r environment is accomplished by depositing a 1-2μm-thick dielectric mem-

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I am indebted to my master degree advisor Dr. Chen Y. Ho, who invited me into the world of microwave and continuously encouraged me through my study. I would like to extend my sincere gratitude to Prof. Linda Katehi, with whom I have regularly interacted during the course of my research, for her technical expertise, support and friendship. I would also like to thank all the members of my committee for their useful suggestions.

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Therefore, they are mostly used in millimeter-wave low-noise amplifiers (LNAs) and for RF power applications. Recent GaAs LNAs have demonstrated a noise figure of 2.6 dB with 7 dB gain at 96 GHz [2, 3], and similar work has achieved a 33.5 dB gain at 102 GHz with a chip size of around 5 mm^2 [4]. Since the development of MMICs is expensive, computer modeling techniques are therefore used in MMIC design to reduce the number of iterations in prototype development. Based on the new powerful modeling techniques and advances in low-cost processing technologies, silicon and GaAs MMICs have achieved excellent performance at the circuit level.

The implementation of MMICs at the system level together with filters, diplexers, couplers and other hybrid circuits is still causing many problems. For example, filters and diplexers used in communication systems are usually designed in a single waveguide or stripline structure to achieve the high-quality factor and low-loss needed at the front-end of the receiver. However, a good transition from the non-planar waveguide/stripline structures to the planar MMICs is difficult to achieve, and an E-plane probe is often used [4, 5]. To avoid the waveguide/stripline transition problem, some filters, which are incorporated with MMICs, are fabricated on Alumina (Al_2O_3, $\epsilon_r \simeq 9.8$) or Duroid™ (ϵ_r ranges from 2.2 to 10.8) substrates using a planar microstrip line design and implemented as a hybrid component. Sometimes filters are directly designed with RF circuitry on a single MMIC chip to reduce the number of hybrid components used in the system. However the losses and dispersion from the dielectric substrates causes many problems. First, the frequency dependence of the dielectric material and the nature of planar structure design result in a non-TEM wave and in different even- and odd-mode propagation velocities in a coupled-line structure. This creates a non-constant group delay in a planar filter. Also the dielectric loss from the substrate generally increases with frequency and results in high dielectric loss resonant frequencies, and therefore planar inductors are seldom used above X-band (8-12 GHz) in a hybrid package, and monolithic inductors are limited to around 30 GHz. In order to solve the parasitic-effect problems in planar inductors, different methods such as active inductors using transistors have been proposed [12-15]. This method has been successfully implemented up to 15 GHz. However, two to four transistors and many bias resistors are required to synthesize the inductive effect. Therefore, the active inductor is not a convenient method in millimeter-wave circuit design and a 'true' lumped planar inductor is needed for microwave and millimeter-wave MMICs design.

As outlined above, most of the problems encountered in microwave circuit level designs are related to the dielectric material used in the MMICs and the associated hybrid circuits. Therefore, in this thesis, we propose the use of micromachining techniques to eliminate the dielectric substrate and to create a localized low-loss and low-ϵ_r environment. The idea is simple and attacks the most basic point: How to build microwave planar circuits on very low dielectric constant substrates to eliminate dispersion and dielectric loss and to result in a TEM-wave, while still being compatible with standard silicon and GaAs processing techniques. The low-ϵ_r environment is accomplished by depositing a 1-2μm-thick dielectric membrane layer on top of the dielectric substrate, then using micromachining techniques to locally remove the supporting silicon or GaAs substrate. After the supporting substrate is removed, the thin dielectric membrane is suspended in air and results in an effective dielectric constant close to one ($\epsilon_r \simeq 1.0$). The fabrication process is fully compatible with the via-hole process, and therefore can be accomplished with via-hole formation in MMICs. The air-filled membrane structure provides a dispersion-free TEM mode for distributed transmission lines which greatly simplifies the analysis and modeling chined Lange-coupler is first developed at 15 GHz and achieves a 3.6±0.8 dB port-to-port coupling from 6.5 to 20 GHz while preserving a phase balance of 90±3 degree. The Lange-coupler is used in conjunction with an interdigitated filter developed in Chapter IV for single-sideband mixer applications, and an image rejection of 30 dB with an IF frequency of 1 GHz and above is achieved. Chapter VI concludes with suggestion for future work. For the completeness of the work, the fabrication procedures of the membrane supported circuits and the codes developed for the interdigitated filters and Lange-couplers are presented in the attached appendices.

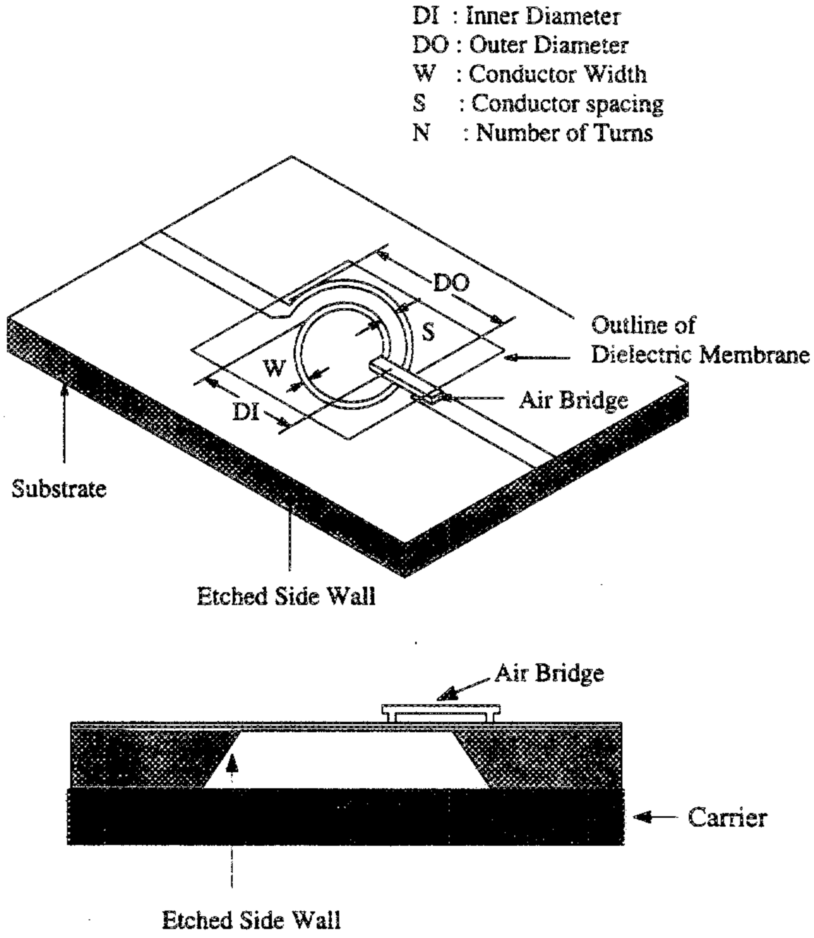


Figure 2.1: Layout of the planar inductor and the membrane outline. The membrane is defined only underneath the lumped element inductor (or capacitor)

posited using the LPCVD furnace at 920° C. The gas flow rate are N_2: 290 sccm, N_2O: 120 sccm and DCS: 60 sccm [27, 28]. It is important to note that this can also be done using GaAs or InP substrates for high speed microwave circuit applications. In this case, the membrane layer is deposited using plasma enhanced chemical vapor deposition (PECVD) [29]. The PECVD layer (or equivalent) is a standard processing step in active GaAs devices such as amplifiers and mixers. After the layer is deposited on the silicon or GaAs substrate, the planar inductor is defined on the top side of the substrate using standard lithography, gold evaporation and electro-plating to increase the thickness of the deposited gold. An opening is then defined in the membrane on the back side of the wafer just underneath the inductor (or capacitor). Next, electro-plated air-bridges are built to connect the inductors. At the last step, silicon or GaAs substrate is etched until the transparent dielectric membrane appears (see Fig. 2.2). The etchant used with silicon wafers is KOH or EDP [30]. The etchant used with GaAs wafers is an $H_2SO_4/H_2O_2/H_2O$ based solution or dry etching in an RIE machine [29]. In GaAs substrates, this procedure is totally compatible with via-hole formation which is used to contact the source-terminals in 3-terminal devices to the RF ground-plane at the back-side of the substrate.

2.3 Microwave Measurements: Microstrip Inductors

Two planar microstrip inductors were fabricated on a 355 μm-thick high-resistivity silicon substrate. Identical inductors using the same masks were also fabricated on a 1.2 μm-thick dielectric membrane using the micromachining technique outlined previously. The membrane edge is aligned with the physical edge of the inductor as shown in Fig. 2.1. The microstrip line is 1 μm-thick electro-plated gold and the air-bridge dimensions are 250 μm × 40 μm with 2 height of 2 μm using a gold electro-

Components	DI	DO	W	S	N	L_s(nH)
L_{1S}, L_{1M}	254	406.4	25.4	50.8	1.5	1.09
L_{2S}, L_{2M}	101.6	406.4	25.4	50.8	2.5	1.69

Table 2.1: Physical dimensions and the corresponding calculated inductance values for the spiral inductors. The definition of DI, DO, W, S and N are shown in Fig. 2.1. All units are in μm.

plating technique. A photograph of two completed inductors and their equivalent model are presented in Fig. 2.3 and Fig. 2.4. The microstrip inductors' dimensions are outlined in Table 1 and are designed to yield inductance values of 1.09 nH and 1.69 nH by using the following equation [24]:

$$L_s(\mathrm{nH}) = 0.01AN^2\pi[\ln(8A/C) + (1/24)(C/A)^2\ln(8A/C + 3.583) - 1/2] \qquad (2.1)$$

where A=(DO + DI)/4, C=(DO − DI)/2 (see Fig. 2.1), A and C are given in "mils" (1 mil=25.4 μm) and N is the number of turns.

The TRL (Thru-Reflect-Line) calibration routine [25] is used to measure the loss of the 50 Ω microstrip line on a high resistivity silicon substrate (2000 $\Omega-$cm) which is attached to the lumped inductor. The microstrip line is 1 mm long on each side of the inductor and exhibits a loss of 0.2 dB/mm from 3 GHz to 20 GHz. This implies that the loss of the microstrip line is dominated by dielectric loss in the substrate. The microstrip line loss is modeled as a matched attenuator (R_1, R_2, R_3). The reference plane for the inductor measurements is defined at the outer limit of the inductor geometries or simultaneously at the edge of the membrane (Fig. 2.1).

Inductors L_{1S} and L_{2S} built on a high resistivity silicon substrate are first measured from 3 GHz to 20 GHz. Then the EESof − Touchstone™ optimization routine is used to fit an equivalent circuit model to the measured S-parameters of these two

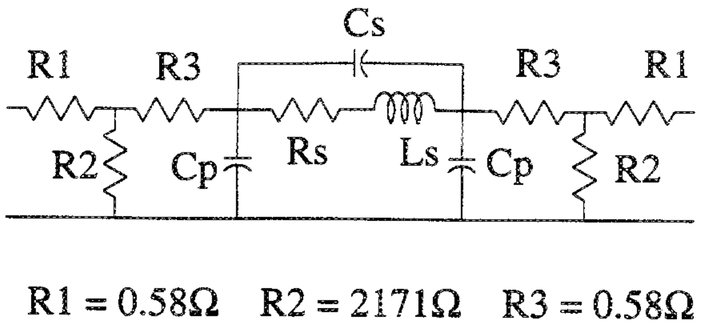


Figure 2.4: The equivalent circuit model of the spiral inductors. A 0.2 dB attenuator is placed at each end to model the loss in the 50 Ω microstrip line on the high resistivity silicon dielectric substrate.

Components	$R_s(\Omega)$	L_s(nH)	C_s(fF)	C_p(fF)
L_{1S}	3	1.2	10	33
L_{2S}	5	1.7	6	45

Table 2.2: Modeled values of the R_s, L_s,C_s and C_p for spiral inductors L_{1S} and L_{2S} from the 3-20 GHz measured data.

silicon inductors. The measured and modeled S-parameters are plotted on a Smith chart (Fig. 2.3), and the equivalent values of L_s, R_s, C_p, C_s for inductors L_{1S} and L_{2S} are summarized in Table 2. It is seen that the equivalent inductance agrees quite well with equation 2.1 and the resonant frequency is 22 GHz and 17 GHz for the 1.2 nH and the 1.7 nH planar microstrip inductor, respectively.

In order to predict the behavior of the membrane inductors, the same equivalent circuit model is used but with a simple modification involving C_p and C_s. C_p represents the parasitic capacitance between the spiral inductor top metal and the bottom ground plane. From the quasi-static point of view, the capacitance value of C_p depends on the dielectric constant of the substrate. After the silicon substrate is etched away, the dielectric material between the spiral inductor and the ground plane is simply with air $\epsilon_r = 1$, and the value of C_p is therefore reduced by a factor of ϵ_r (ϵ_r=11.7). On the other hand, C_s represents the mutual coupling between the

Components	$R_s(\Omega)$	L_s(nH)	C_s(fF)	C_p(fF)
L_{1M}	3	1.2	2	2.5
L_{2M}	5	1.7	1.2	4

Table 2.3: Modeled values of the R_s, L_s,C_s and C_p for spiral inductors L_{1M} and L_{2M} derived from the silicon inductor models (see text).

inner turns of the spiral inductor. Using a quasi-static model, half of electric field between the spiral turns is in air ($\epsilon_r = 1$) and the other half is confined to the substrate (ϵ_r=11.7). This implies that the effective dielectric constant in C_s is $(1+\epsilon_r)/2$ and should be reduced to $\epsilon_r = 1$ in the case of the membrane inductors. The inductance, L_s, and the resistance, R_s, are not changed in the membrane inductor model since the membrane and silicon inductors have identical geometries and both silicon and air have a relative permeability (μ_r) of 1. The new equivalent circuits for membrane inductors L_{1M}, and L_{2M} are shown in Table 2.3. It is seen that good agreement is achieved between the measured S-parameters from 3 to 20 GHz for the membrane inductors L_{1M} and L_{2M} and the new equivalent circuits derived from L_{1S} and L_{2S} (Fig. 2.6).

The measured and modeled 3 GHz to 20 GHz reactance (X) of the inductors on a thick silicon substrate (L_{1S}, L_{2S}) and the inductors on a thin dielectric membrane (L_{1M}, L_{2M}) is shown in Fig. 2.7. It is seen that the measured reactance (X) of the membrane inductors (L_{1M}, L_{2M}) agree well with the simple equivalent model (3 GHz to 20 GHz). The resonant frequency of the membrane inductors is pushed to around 70 GHz and 50 GHz for a 1.2 nH and a 1.7 nH inductor, respectively. The parasitic capacitances are very low for the micromachined inductors (C_p, $C_s = 2-4$ fF) and the membrane inductors can be used as "true" inductors up to 40-60 GHz. The model takes into account only the quasi-static capacitance of the lumped inductor and neglects the transmission-line effects of the pyramidal cavity underneath the lumped inductor and the radiation loss to the air. At mm-wave frequencies, the membrane inductors may result in lower resonant frequencies as predicted above due to non quasi-static (high-order modes) effects.

The micromachined inductors behave exactly the same way as the standard planar microstrip inductors at microwave frequencies. It is important to note that the micromachined planar inductors result in the same inductance values as the standard planar inductor but have much higher resonant frequencies. Therefore, it is expected that the micromachined inductor will exhibit a similar Q at microwave frequencies. A small LC series filter composed of a membrane inductor of value 0.9 nH (with a series resistance, $R_s \simeq 1.2-1.3\ \Omega$) and a chip capacitor of value 1.2 pF was fabricated. The chip capacitor is a surface mount MIS type capacitor (Metelics MBIC-1002) and has a very high Q up to 12 GHz, and its effect on the measured Q is neglected at 4.3 GHz. The measured S_{11} of the series LC combination demonstrates a quality factor of $Q = 20$ at 4.3 GHz for the membrane inductor and is close to the expected value of $Q=23.3$ from the equation $Q = \omega_0 L/R_s$ (Fig. 2.8). The measurements include the effect of two bond wires used to connect the silicon substrate to the coaxial connectors ($L_{bw} \simeq 0.1$ nH). The associated Q of membrane inductors is expected to increase as $\sqrt{f}$ with frequency (because the series resistance increases as $\sqrt{f}$ [24, 31]) to result in a Q of 50-60 at 30-40 GHz for a 0.9 nH inductor.

2.4 Microwave Measurements: Microstrip Capacitors

A similar fabrication technique was applied to planar interdigitated capacitors. In this case, the planar capacitors do not suffer from a low resonant frequency but from a relatively large shunt parasitic capacitance to ground (C_p). During modeling, the parasitic capacitance to ground is generally included with the interdigitated series

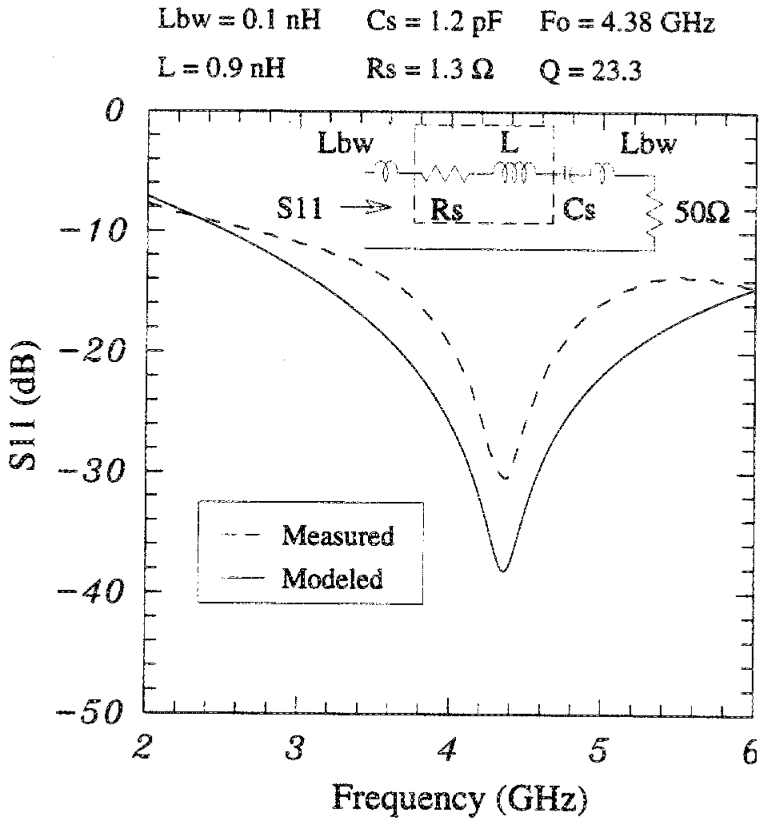
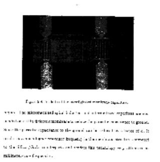
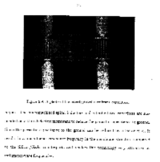
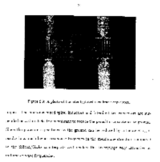
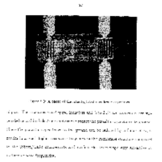


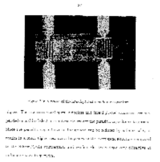
Figure 2.8: Measured and modeled S_{11} of a small LC filter. This filter shows that the 0.9 nH membrane inductor has a quality factor of 23.3 at 4.38 GHz.

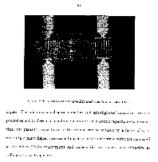


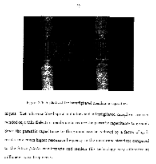


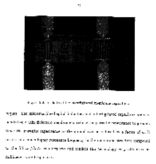












CHAPTER III

STRIPLINE RESONATORS AND ASSOCIATED DISTRIBUTED CIRCUITS

3.1 Introduction

Resonators play a very significant role in communication systems. They can be used for impedance matching and signal filtering. For filter applications, the quality factor Q of a resonator is one of the most important parameters that needs to be known, since it predicts the passband insertion loss of the filter, and can also be used to determine the roll-off response of the filter in the rejection band. In this chapter, a detailed procedure for measuring the quality factor of a transmission line is discussed. Two examples detailing the measurement of the quality factor of a micromachined membrane suspended stripline and microstrip line are given. The stripline results show a conductor-loss limited performance but the microstrip results show a small free-space radiation loss component at 13 GHz and this radiation loss becomes dominant at 40 GHz for the geometry considered herein. The measured results from the stripline are also compared to the analytical results obtained from a method-of-moment technique and a new conformal mapping analysis technique. Good agreement has been achieved between the measured results and the conformal mapping technique. Two grounded coplanar-waveguide (GCPW) transmission lines which are built on a high resistivity silicon substrate and on a thin dielectric

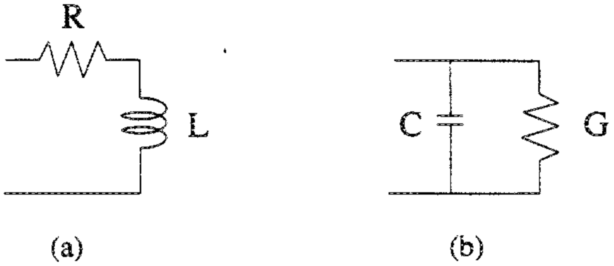


Figure 3.1: (a) A series R, L circuit, (b) a shunt G, C circuit.

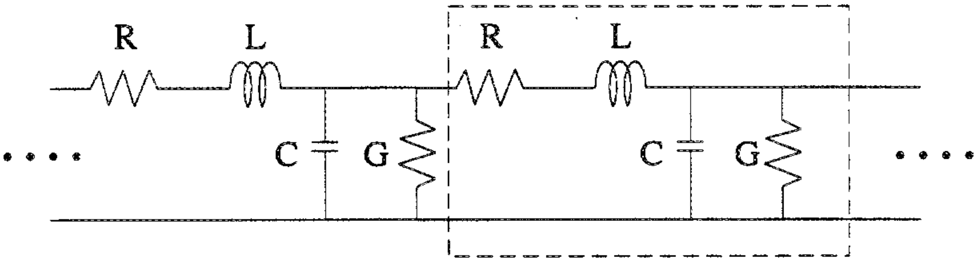


Figure 3.2: The equivalent circuit of a transmission line.

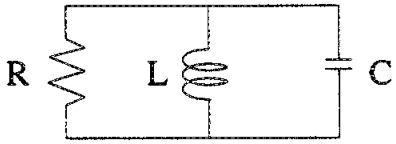


Figure 3.3: A RLC resonator.

Also, when a resonator is in the vicinity of a single mode resonance, it can be well represented by using an R, L, C equivalent circuit (Fig. 3.3). The quality factor of this resonator can be written as:

$$Q = \frac{f_0}{\Delta f_{3-dB}} = \frac{\omega_0 L}{R} = \frac{\omega_0 C}{G} \tag{3.7}$$

where G is equal to 1/R. There are many different methods for measuring the quality factor of a resonator [32, 33], and the half-wavelength end-fed capacitive gap coupling is the most commonly used method. Basically, it has an input feeding transmission line with a capacitive coupling gap to a half-wavelength resonator, then another capacitive coupling gap from the resonator to the output feeding transmission line (Fig. 3.4). At a single frequency, the behavior of the capacitive coupling gap is the same as an ideal transformer [34]. Therefore, in the vicinity of the resonant frequency, the end-coupled structure can be considered as an input source with a transformer, a GLC tank followed by another transformer to the output load. The equivalent circuit of such a resonator is shown in Fig. 3.5(a) where G_s is the characteristic conductance of the input/output transmission lines. The input/output stages in Fig. 3.5(a) can be reflected into the GLC tank through the transformers, and at the resonant frequency, the shunt LC in Fig. 3.5(a) behaves as an open circuit. By combining these two factors, the equivalent circuit in Fig. 3.5(a) is simplified and the new equivalent circuit at the resonant frequency is shown in Fig. 3.5(b).

If there is no input/output loading effect on the resonator, the quality factor Q of the resonator is given by equation 3.7 and is equal to $\omega C/g$, which is also called the *unloaded Q* (Q_u). The *external Q* (Q_e) of the resonator is defined as the Q with the input/output loading effect on the resonator (2 G_s' in parallel with the LC tank), but the loss component from the resonator itself is set to zero (*i.e.* with g=0 and $Q_u = \infty$). Thus, the external Q is:

$$Q_e = \frac{\omega_0 C}{2G_s'} \tag{3.8}$$

Combining the input/output loading effect ($2G_s'$) with the loss component (g) of the resonator itself, the *loaded Q* (Q_l) in the coupled resonator system is:

$$Q_l = \frac{\omega_0 C}{2G_s' + g} = \frac{f_0}{\Delta f_{3-dB}} \tag{3.9}$$

The loaded-Q can be expressed as:

$$\frac{1}{Q_l} = \frac{1}{Q_u} + \frac{1}{Q_e} \tag{3.10}$$

In Fig. 3.5(b), the power available from the load at the resonant frequency, assuming no loss in the resonator, is defined as:

$$P_{av}|_{g=0} = (\frac{I_s'}{2})^2 \frac{1}{G_s'} = \frac{I_s'^2}{4G_s'} \tag{3.11}$$

However, the real power delivered to the load at the resonant frequency, with a lossy component g in the resonator, is given by:

$$P_{load}|_{g\neq 0} = (\frac{I_s'}{2G_s' + g})^2 G_s' \tag{3.12}$$

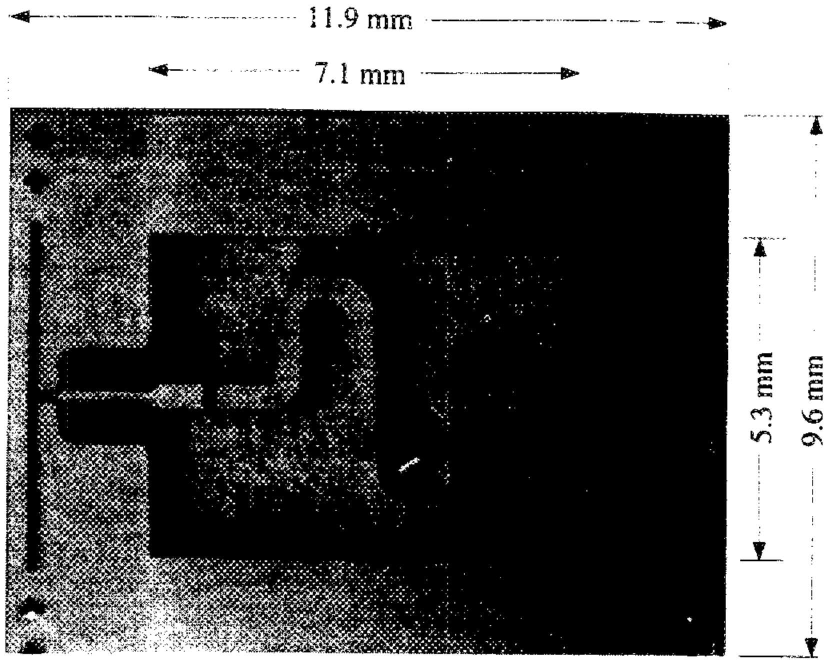
The loss of this system is defined as P_{load}/P_{av} and is equal to:

$$\text{Loss} = \frac{P_{load}}{P_{av}} = \frac{4G_s'^2}{(2G_s' + g)^2} \tag{3.13}$$

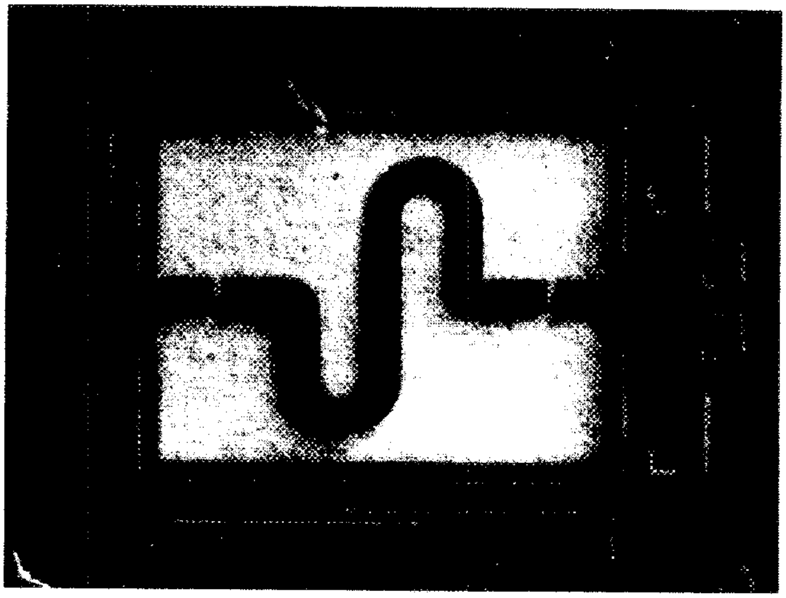
Now, if the measured total system loss is used in equations 3.14 and 3.10, then the calculated unloaded Q_u are 438 and 333 for system A and B, respectively. However, if the 1 dB loss from the feeding structures is extracted from the total loss, then the calculated unloaded Q_u for system A and B become 465 and 338. It can be seen, the 1 dB loss from the feeding structures contributes a 5.8% and 1.5% relative error into the calculated unloaded Q_u in system A and B, respectively. Therefore, it is clear that in the Q measurement technique a weak coupling structure (below -15 dB) is preferred since it will reduce the effects of the line-loss on the calculation of Q_u.

3.3 Q Measurement on the Membrane Suspended Transmission Line Resonators

The microstrip and stripline resonators are fabricated on a 350μm-thick high-resistivity silicon wafer capped with a 1.4μm dielectric membrane layer (Fig. 3.6). A top shielding cavity is used in the case of the stripline resonators at a height of 350μm above the resonator (Fig. 3.7). Details of the fabrication process and the associated via-hole process around the dielectric membrane can be found in Appendix C. The microstrip and stripline resonators are $\lambda_0/2$ long at 13.5 GHz (1.1 cm) and are fabricated using standard lithography. The resonator is 500μm-wide and 3μm-thick electro plated gold. The characteristic impedance of the stripline and microstrip line are calculated using a quasi-static analysis and are 80.8Ω and 104Ω, respectively. The input/output feeding structure is a 50Ω microstrip line on a 350 μm-thick high resistivity silicon substrate. At the end of this feeding line, there is a transition section from the 50Ω microstrip line to a T-shaped discontinuity area, and is followed by a short section of membrane transmission line (Fig. 3.6). This transition could cause some problems in a wide-band two-port measurement set-up. However, for a single frequency or a narrow frequency range, this transition can be

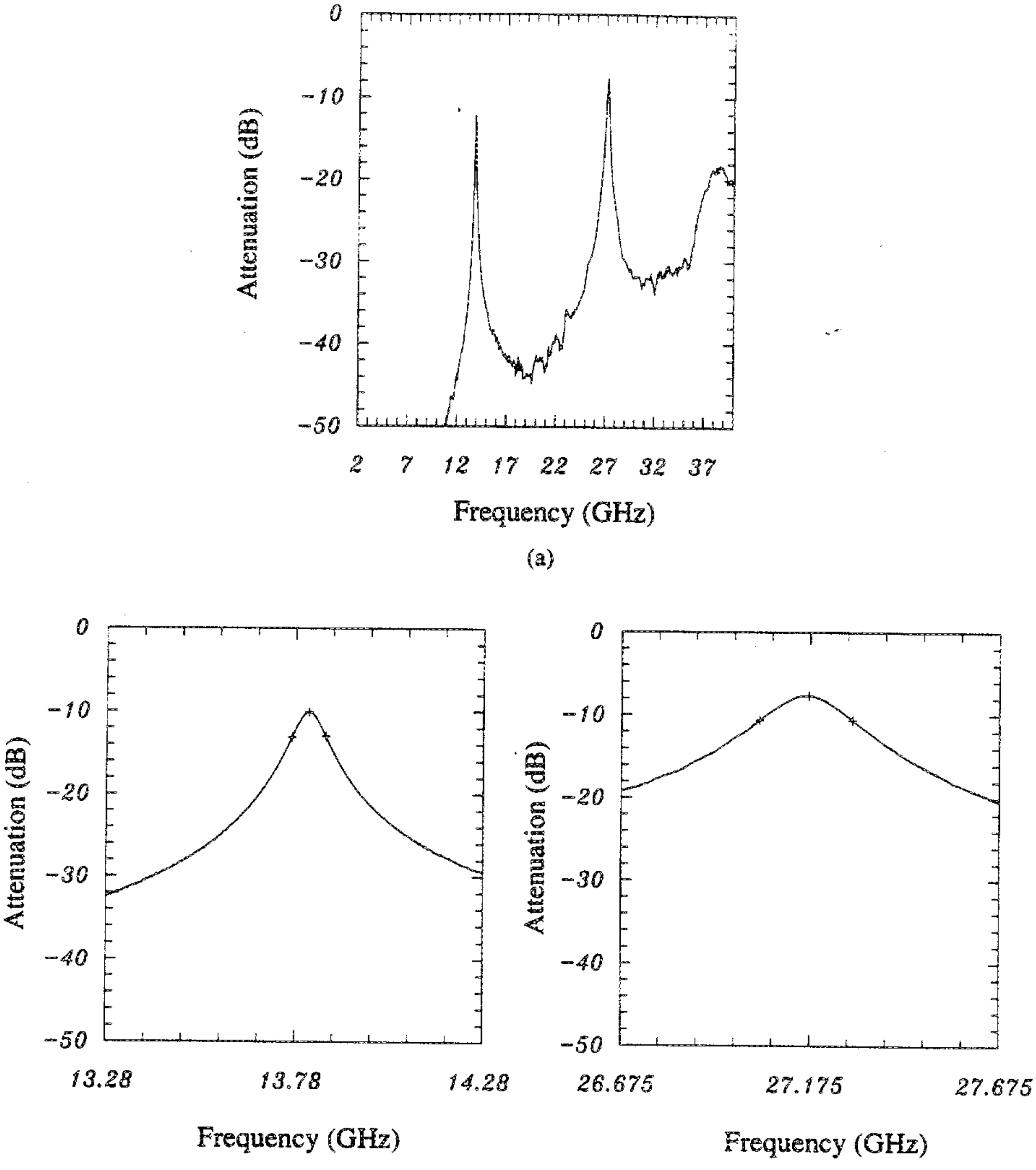


(a)



(b)

Figure 3.6: (a) Top view of the fabricated membrane suspended resonator. (b) Bottom view of the resonator. Via-holes are around the edge of membrane to provide a continuous ground plane for the stripline design. The chip size of the fabricated membrane resonator is 11.9×9.6 mm^2 and the membrane dimensions are 7.1×5.3 mm^2.



(a)

(b)

(c)

Figure 3.8: Measured response of the microstrip resonator.

the input/output line, the loaded-Q, unloaded-Q, attenuation constant, and the loss resistance of the resonator can be calculated and are listed in Table 3.2

As is evident in Table 3.2, the stripline Q_u increases as $\sqrt{f}$ with frequency. This is an indication of conductor-loss limited performance and the absence of dielectric and radiation loss mechanisms. This micromachined stripline shows a total loss of 1.35 dB/ft at 13.5 GHz which is about 0.4 dB higher than a regular 0.086-inch diameter copper jacketed semi-rigid 50Ω cable at the same frequency [35]. A lower loss can be achieved by increasing the thickness of the wafer which will result a wider strip and lower conductor loss for the same characteristic impedance.

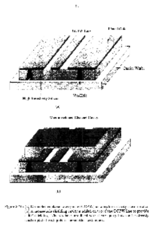
The same stripline geometries have been analyzed using three different techniques: quasi-static analysis, method-of-moment (MoM), and a new conformal mapping analysis technique developed by Tuncer, Lee and Neikirk. [36]. The quasi-static analysis is performed by the EESof Linecalc^{TM} calculation and the method-of-moment analysis is performed by the IE3D^{TM} program [37]. The conformal mapping technique uses an isolated-conductor surface impedance in conjunction with a conformal mapping for the entire transmission line cross-section to account for both skin-depth and current crowding effect, and can accurately predict the series impedance of a transmission line with finite conductivity. The MoM method can also predict the series resistance from the finite thickness and conductivity of the metal used. However, due to the current crowding effect at the edge of the stripline, the MoM results are strongly dependent on the grid size which is used to partition the cross-section of the stripline. The quasi-static analysis cannot take the current crowding effect into account, and therefore, a smaller series resistance can be expected from this analysis. The predicted series resistances from these three techniques are listed in Table 3.3. As can be seen, good agreements have been achieved between the measured results

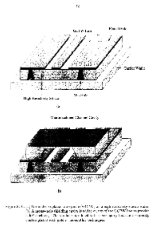
	Stripline		
	f_{01}	f_{02}	f_{03}
	13.555	27.365	39.636
$\mathrm{Q_l}$	258	331	304
$\mathrm{Q_u}$	272	386	465
$\mathrm{Q_{u_f}/Q_{u_{f_{01}}}}$	1	1.419	1.710
$\sqrt{\mathrm{f/f_{01}}}$	1	1.421	1.710
Skin Depth (μm)	0.676	0.478	0.395
α(NP/cm)	0.0052	0.0074	0.0089
$\mathrm{R_s}$(Ω/cm)	0.841	1.196	1.439

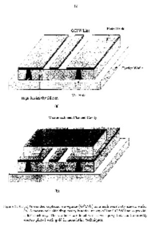
Table 3.2: The measured Q factor, attenuation constant and the loss resistance of a membrane suspended stripline resonator with an impedance of 80.8Ω.

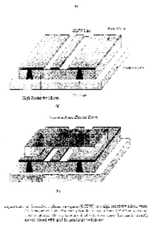
	Stripline		
	f_{01}	f_{02}	f_{03}
	13.555	27.365	39.636
$\mathrm{R_s}$(Ω/cm) *from Table3.2*	0.841	1.196	1.439
$\mathrm{R_s}$(Ω/cm) *Conformal Mapping*	0.762	1.153	1.410
$\mathrm{R_s}$(Ω/cm) *IE3D*	0.753±10.5%	1.082±13.3%	1.386±11.0%
$\mathrm{R_s}$(Ω/cm) *Linecalc*	0.634	0.949	1.166

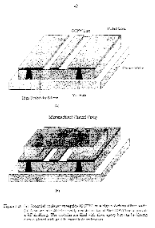
Table 3.3: Comparison of the measured loss resistance and the simulated loss resistance from three different technologies.

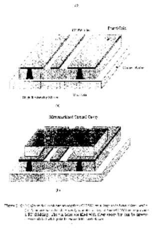


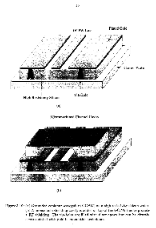


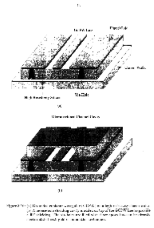










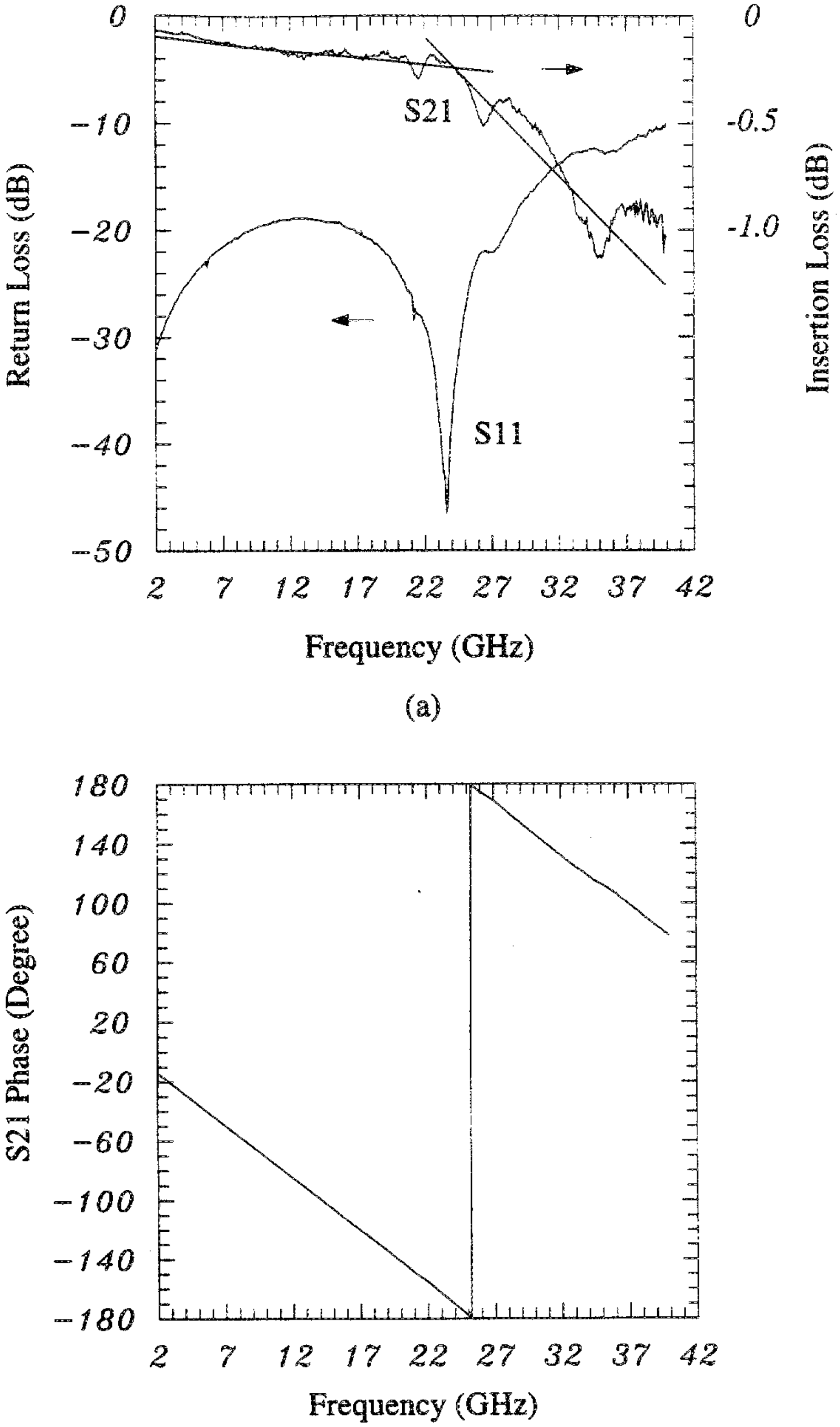


The phase of S_{21} is used to extract the effective dielectric constant of the GCPW line by knowing the physical length of the line. The calculated effective dielectric constant versus frequencies, for both shielded and unshielded cases, is plotted in Fig. 3.12. The shielded GCPW line shows a slightly higher effective dielectric constant than the unshielded one. This is expected since after putting a cavity on the GCPW line, more electric field is pushed into the dielectric substrate and this results in a higher effective dielectric constant. The silicon substrate used here has a resistivity around $2000\Omega - \text{cm}$, and is not a perfect dielectric material. Therefore, as more electric field is confined into the substrate, more loss is expected. This explains the reason why the shielded GCPW line in Fig. 3.11 shows a slightly higher loss than the unshielded case.

3.4.2 Micromachined Membrane Grounded Coplanar Waveguides

A 50Ω micromachined grounded coplanar waveguide was also built (Fig. 3.13). The GCPW line is composed of a long section of membrane suspended GCPW line and two short section of silicon substrate GCPWs at both ends to provide the required input/output feeding structures for measurement purposes. The membrane suspended GCPW has a 767 μm-wide center conductor, a 25 μm-wide gap and is 3774 μm long. The input/output sections have the same geometric dimensions as the one discussed in section 3.4.1 and each section is 380 μm long. The 175 μm-wide silicon GCPW lines directly feed the 817 μm-wide membrane GCPW line at the silicon to membrane transition area without any taper design. Two via-holes are put beside the end of the input/output feeding line to provide continuous grounding.

The membrane GCPW line is measured from 2 to 40 GHz using the same SOLT calibration technique. The measured return loss, insertion loss and the phase of S_{21}



(a)

(b)

Figure 3.14: Measured response of a 3.8 mm long 50 Ω membrane suspended grounded coplanar waveguide: (a) return loss and insertion loss, (b) phase of S_{21}.

cromachined GCPW line can be reliably used as the input/output feeding structure to planar filters, couplers integrated on thin dielectric membranes.

filter using silver epoxy. These micromachined interdigitated filters are very compact (about 1 cm^2 at Ku-band) and lightweight (about 0.4~1 grams). Micromachined filters, suspended on a thin dielectric membrane, do not suffer from dielectric loss and from dispersion and the performance of the filter is only limited by the conductor loss. Also, with the advantage of the MMIC fabrication process, batch fabricated micromachined filters can have nearly identical responses. As will be seen in section 4.3, an interdigitated filter can be easily fabricated at 60 GHz with a 100 μm thick silicon (or GaAs) wafer.

4.2 Design of Interdigitated Filters

4.2.1 Bandpass Filter Design

In a filter design, the same method is used for a high-pass, bandpass or bandstop filter. The method starts from the low-pass prototype, and different transformation functions are used to transfer the low-pass response to the desired center frequency and to achieve different frequency selective functions [49]. A typical lumped-element low-pass prototype design is shown in Fig. 4.2. The circuit of the bandpass filter can be directly obtained (Fig. 4.2(b)) by using the low-pass to bandpass transformation. After the transformation, each shunt capacitor C_j' in Fig. 4.2(a) with a value of g_j transforms to a shunt LC resonator with a capacitance $C_j = g_j\omega_1'/\omega_0\varpi$ and inductance $L_j = \varpi/g_j\omega_0\omega_1'$ (Fig. 4.2(b)). Similarly, each series inductor L_k' with a value of g_k transforms to a series LC resonator with an inductance $L_k = g_k\omega_1'/\omega_0\varpi$ and capacitance $C_k = \varpi/g_k\omega_0\omega_1'$. ω_1' is the 3-dB cut-off frequency of the low-pass prototype filter; ω_0 is the center frequency of the bandpass filter; ω_1 and ω_2 are the 3-dB cut-off frequencies of the bandpass filter; and ϖ is the fractional bandwidth of the bandpass filter and is defined as $(\omega_2 - \omega_1)/\omega_0$. The advantage of using this transformation is that it is straightforward and can easily be implemented at VHF and UHF frequencies. However, the disadvantage of this method is that the ratio of the maximum to minimum capacitance (or inductance) value required in the filter is proportion to $1/\varpi^2$ and it becomes impractically high for a narrow-band bandpass filter design with $1/\varpi^2$=20 to 50. In order to solve this problem, the concept of impedance or admittance inverters is introduced and used to absorb the shunt capacitance (or inductance). The resulting filter has only the series-type resonators or only shunt-type resonators [48]. The generalized equivalent circuit of a bandpass filter using the impedance/admittance inverters is shown in Fig. 4.3.

The $X(\omega)$ and $B(\omega)$ in Fig. 4.3, represent a series and shunt-type resonator, respectively. These resonators can be LC resonators, waveguide cavity resonators or distributed transmission resonators. At microwave frequencies, the lumped-elements are difficult to build especially with a large range of values (even with the membrane technology), and therefore, it is desired to realize the resonators in the distributed-element forms for microwave applications.

The J and K inverters in Fig. 4.3 are the coupling mechanism used to control the coupling ratio between the resonators. By changing it, different bandwidth and internal impedance can be achieved in the filter [50]. The inversion property of a J/K admittance/impedance inverter can be simply expressed by the well know relation of a quarter-wavelength transmission line:

$$Z_{\text{in}} = K^2 Y_{\text{load}} \tag{4.1}$$

where K is the characteristic impedance (or image impedance) of the quarter-wavelength transformer (or impedance inverter), Y_{load} is the loading admittance connected to the

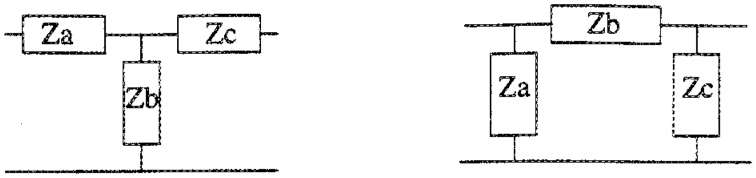


Figure 4.4: Dissipationless inverter networks.

second port of the inverter, and Z_{in} is the equivalent input impedance that looking into the impedance inverter from the first port with Y_{load} connected at the other port. The J, K inverter can also be implemented by other "dissipationless" components such as LC lumped-elements or a combination of lumped-elements and transmission lines. For the "dissipationless" inverter network, the image impedance is defined as [50, 51]:

$$K = \sqrt{Z_{sc} Z_{oc}} \tag{4.2}$$

where Z_{sc} and Z_{oc} are the short- and open-circuit input impedance of the inverter, respectively. For the T-section dissipationless network as shown in Fig. 4.4, the image impedance can be derived using equation 4.2 and is given as:

$$K = \sqrt{\frac{(Z_a + Z_b)(Z_a Z_b + Z_b Z_c + Z_c Z_a)}{Z_b + Z_c}} \tag{4.3}$$

Similarly, for the π-section, the image impedance is given as:

$$K = \sqrt{\frac{Z_a^2 Z_b (Z_b + Z_c)}{(Z_a + Z_b)(Z_a + Z_b + Z_c)}} \tag{4.4}$$

If the resonators of the filter in Fig. 4.3 are made of lumped L, C elements and the J, K inverters used are not frequency sensitive, then the response of the filter in

Similarly, the coupling factor of $k_{k+1,k}$ can be obtained by applied a voltage V2' at port 2 and finding the coupled voltage V1' at port 1.

$$k_{k+1,k} = \frac{V1'}{V2'} = \frac{\frac{1}{C_k}}{\frac{1}{C_k} + \frac{1}{C_{k,k+1}}} = \frac{C_{k,k+1}}{C_{k,k+1} + C_k} \tag{4.6}$$

If the coupled-lines system shown in Fig. 4.5(c) is symmetric, then $k_{k,k+1}$ is equal to $k_{k+1,k}$, otherwise they can be different. Notice, $k_{k,k+1}$ and $k_{k+1,k}$ are the voltage coupling factors between the coupled-lines and they are not the same as the image impedances of the impedance inverter which are usually denoted as $K_{k,k+1}$ and $K_{k+1,k}$ [54]. The image impedance of a π type capacitive impedance inverter like the one shown in Fig. 4.5(c) can be derived using equation 4.4 and is:

$$K_{k,k+1} = \frac{1}{\omega}\sqrt{\frac{(C_{k+1} + C_{k,k+1})}{(C_k + C_{k,k+1})(C_k C_{k,k+1} + C_{k,k+1} C_{k+1} + C_{k+1} C_k)}} \tag{4.7}$$

$$K_{k+1,k} = \frac{1}{\omega}\sqrt{\frac{(C_k + C_{k,k+1})}{(C_{k+1} + C_{k,k+1})(C_k C_{k,k+1} + C_{k,k+1} C_{k+1} + C_{k+1} C_k)}} \tag{4.8}$$

The expression of the coupled array in Fig. 4.5(b) assumes that there is no direct coupling between non-adjacent lines. If the coupling capacitance between the non-adjacent lines is included in Fig. 4.5(b), then the coupling factor given in equations 4.5 and 4.6 (or the image impedance of the K-inverter in equation 4.7 and 4.8) will contain some cross coupling terms from other coupled-lines and this will greatly increase the complexity of the analysis. Therefore, in the analysis of parallel coupled-lines structure, the coupling capacitance between the non-adjacent lines is set to zero to simplify the problem. However, this simplification can cause some problems in the filter design and will be discussed in section 4.5.

If one end of each coupled line in Fig. 4.5(a) is short-circuited, and if the position of the short circuits is chosen to alternate between the A and B ends of adjacent lines, then the parallel coupled-lines becomes an interdigitated structure. Due to the open and short-circuited transmission line in the interdigitated structure, the coupled-lines start to support a mode and behave like resonators when the length of the coupled-lines becomes an odd multiple number of quarter-wavelength at certain frequencies. Therefore, at these resonant frequencies, the interdigitated structure becomes as a resonator with a coupling mechanism created by the self and mutual capacitance between the adjacent resonators. The model of the interdigitated structure is exactly the same as the equivalent circuit of a bandpass filter shown in Fig. 4.3. This implies that by properly choosing the coupling coefficients $k_{k,k+1}$ in equations 4.5 and 4.6, the interdigitated structure can have a frequency selective characteristic and behaves as a bandpass filter. As mentioned earlier, the coupled-lines behave like resonators only when their length is equal to an odd-multiple number of quarter-wavelength at certain frequencies, and therefore, when the interdigitated structure is used as a filter, the passband will repeat at an odd-multiple number of the first passband (say f_0, $3f_0$, $5f_0, \ldots$).

As discussed in section 4.2.1, the bandwidth limitation of a filter depends on the bandwidth of the inverters and resonators used in the design. In the interdigitated structure, the coupling mechanism is from the self and mutual capacitance of the coupled lines (Fig. 4.5(b)). It is calculated by a quasi-static method and is not frequency sensitive. However, when the coupling structure involves transmission-line resonators, a bandwidth limitation factor occurs in the filter. For a parallel coupled-line filter, a bandwidth of less than 30% can be achieved with a response close to the LC filter [55]. An interdigitated filter can achieve a wider bandwidth

4.2.3 Design Procedure of Interdigitated Filters

The design procedure of the interdigitated suspended filter follows the low-pass to band-pass transformation discussed in section 4.2.1 and is elegantly presented by Matthaei in [47, 48, 57, 58]. Briefly, the center frequency and bandwidth of the bandpass filter is first transfered to the low-pass prototype to find the g_j values. After knowing the g_js, the admittance inverter ($J_{k,k+1}$) or the impedance inverter ($K_{k,k+1}$) required in the bandpass filter design can be directly obtained from the low-pass to bandpass transformation [50, 47]. Knowing the value of the impedance inverters and the characteristic impedance of each coupled-line (Z_{0k}), the self-capacitance (C_k) and the mutual capacitance ($C_{k,k+1}$) can be solved from Matthaei's design equations [47]. The next step and also the last step in the design is to find the corresponding physical dimensions for each coupled-line together with the value of the characteristic impedance and the self/mutual capacitance. The process of finding the physical dimensions of the filter can be accomplished with the help of the even- and odd-modes analysis of the coupling capacitance and will be discussed later. After knowing all the parameters, each resonator in the filter is then modeled by an equivalent interdigitated coupled line structure as shown in Fig. 4.6. Notice, in Fig. 4.6(a) (wide-band design), the first and last fingers are open-circuited and serve as resonators. However, in Fig. 4.6(b) (narrow-band design), the first and last fingers are short-circuited and operate as impedance transforming sections only and not as resonators.

The process of finding the physical dimensions is from the even- and odd-mode analysis of the coupling capacitance. The capacitance from the interdigitated coupled-line stage, shown in Fig. 4.7, can be represented as a capacitance matrix [53, 59, 60] which includes the self capacitance (C_k) and the mutual capacitance ($C_{k,k+1}$) between adjacent fingers. The even ($C_{fe_{k,k+1}}$) and odd-mode ($C_{fo_{k,k+1}}$) fringing capacitances

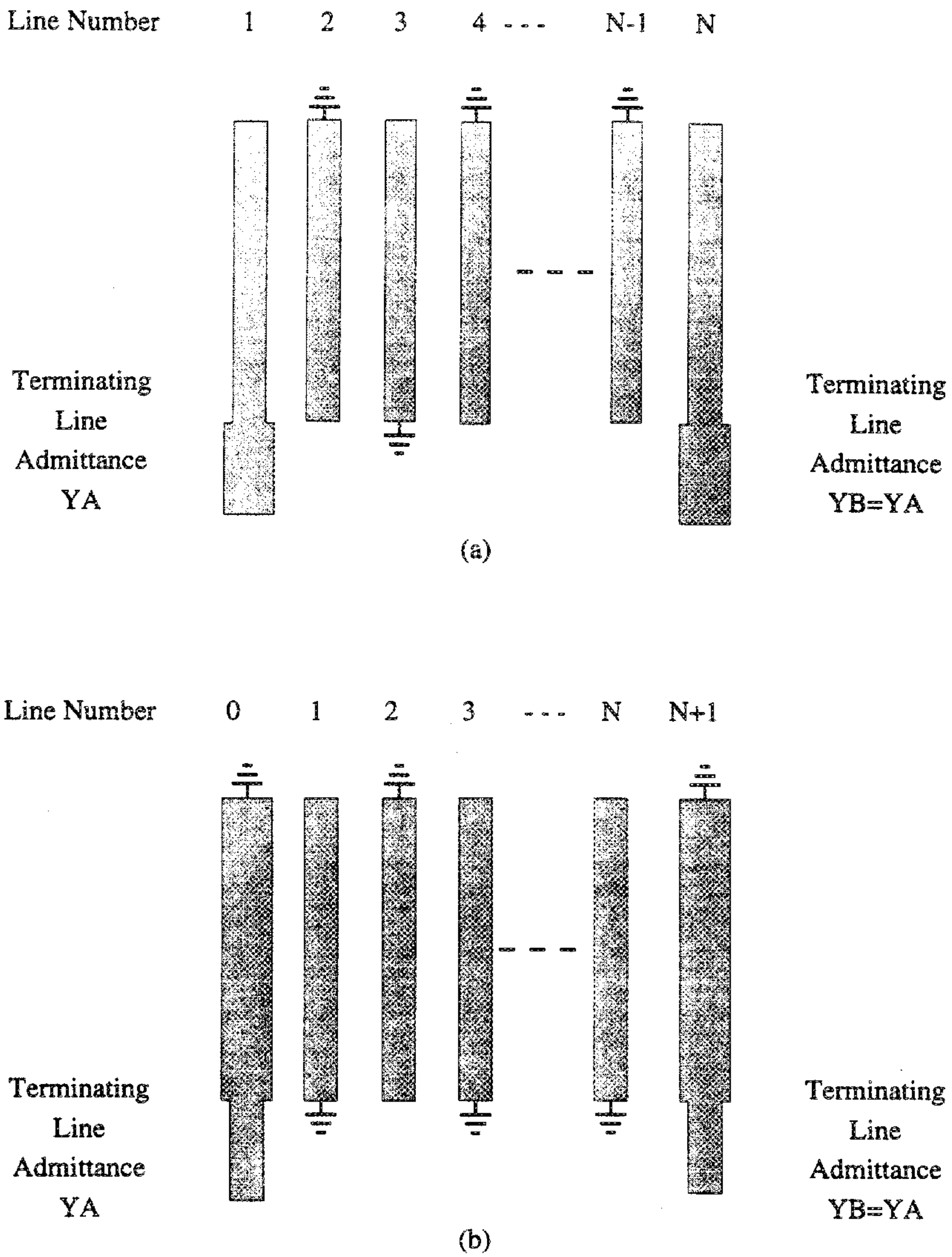


Figure 4.6: Structure of the interdigitated coupled line filter. (a) wide-band design; (b) narrow-band design [47].

which could result in undesired modes. Detail of the cavity-mode problems will be addressed in Section 4.6.

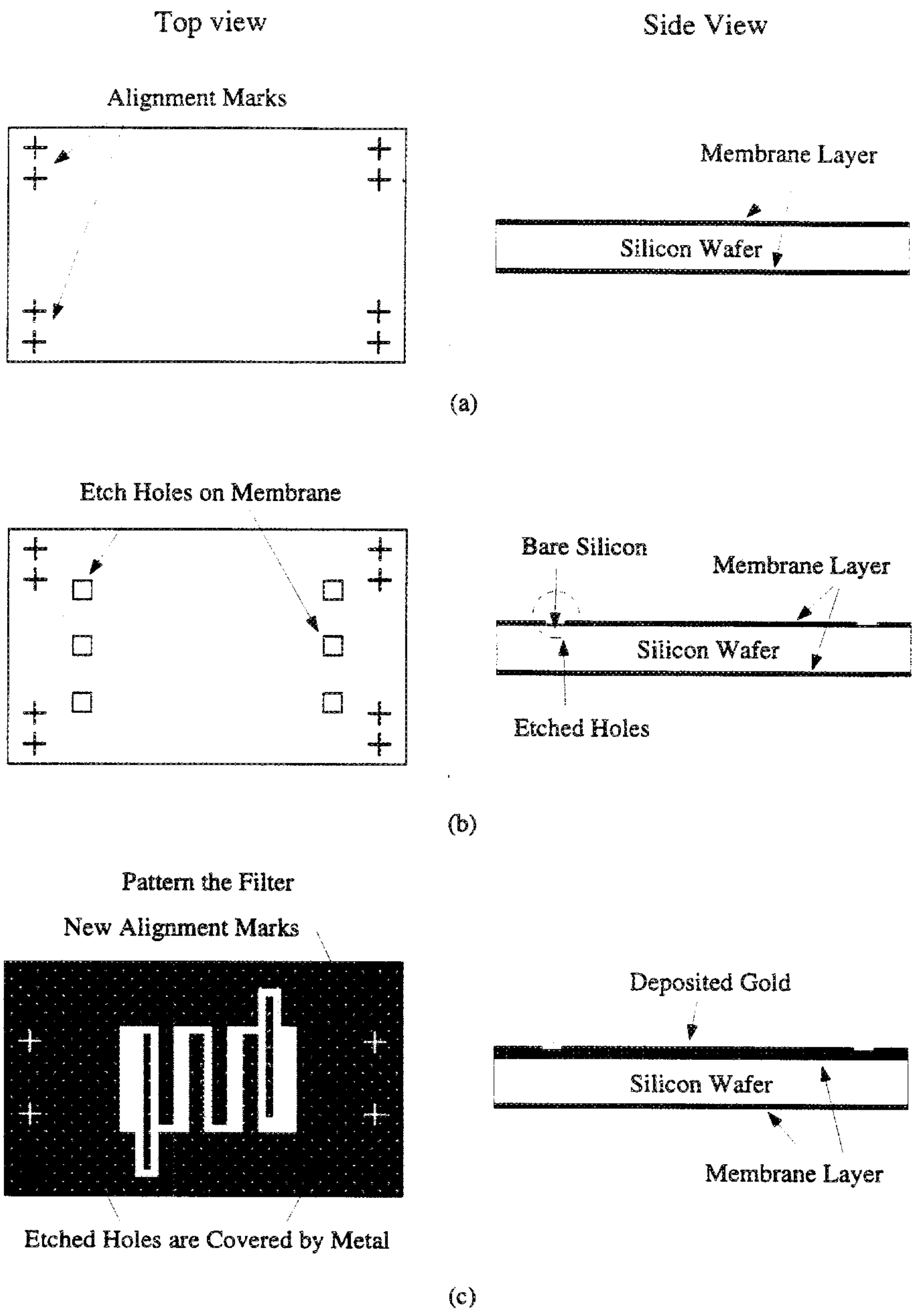
A Fortran 77 code was developed to calculate the physical parameters w_k and $s_{k,k+1}$ in an interdigitated filter design for a given bandwidth and wafer thickness b/2. This code is listed in Appendix B for the reader's convenience.

4.3 Fabrication Procedure of Interdigitated Membrane Filters

Two membrane filters were first built at 15 GHz with a 40% and 5% bandwidth respectively. The 40% filter (wide-band response) is a 6-stage design with 0.05 dB equal-ripple response. The 5% filter (narrow-band response) is a 4-stage design with 0.025 dB equal-ripple response. The coupling capacitances and dimensions for both of the two filters are calculated using the code developed in the previous section and are listed in Table 4.1 and Table 4.2. The cavity height, b, in this design is chosen to be 710 μm and is constructed using two 355 μm standard silicon wafers.

After knowing the physical dimensions of the filter, the fabrication process can start. Essentially, the interdigitated stripline filter is composed of two major parts; one is the membrane filter and the other is the top cavity used to shield the filter. The fabrication procedure for both of the two parts is outlined in this section and the detailed process can be found in Appendix C.

To start the fabrication of the membrane filter, eight alignment marks, two on each corners, are first deposited on the membrane wafer (Fig. 4.8(a)). Then, some small areas (typical 125 μm$\times$125 μm) of the membrane layer on the front side of the wafer are etched away and the bare silicon is exposed (Fig. 4.8(b)). The reason of opening these small holes will be explained in the last step of the fabrication process. In the third step of the process, the pattern of the filter is transfered onto


Top view
Side View
Alignment Marks
Membrane Layer
Silicon Wafer
(a)
Etch Holes on Membrane
Bare Silicon
Membrane Layer
Silicon Wafer
Etched Holes
(b)
Pattern the Filter
New Alignment Marks
Etched Holes are Covered by Metal
Deposited Gold
Silicon Wafer
Membrane Layer
(c)

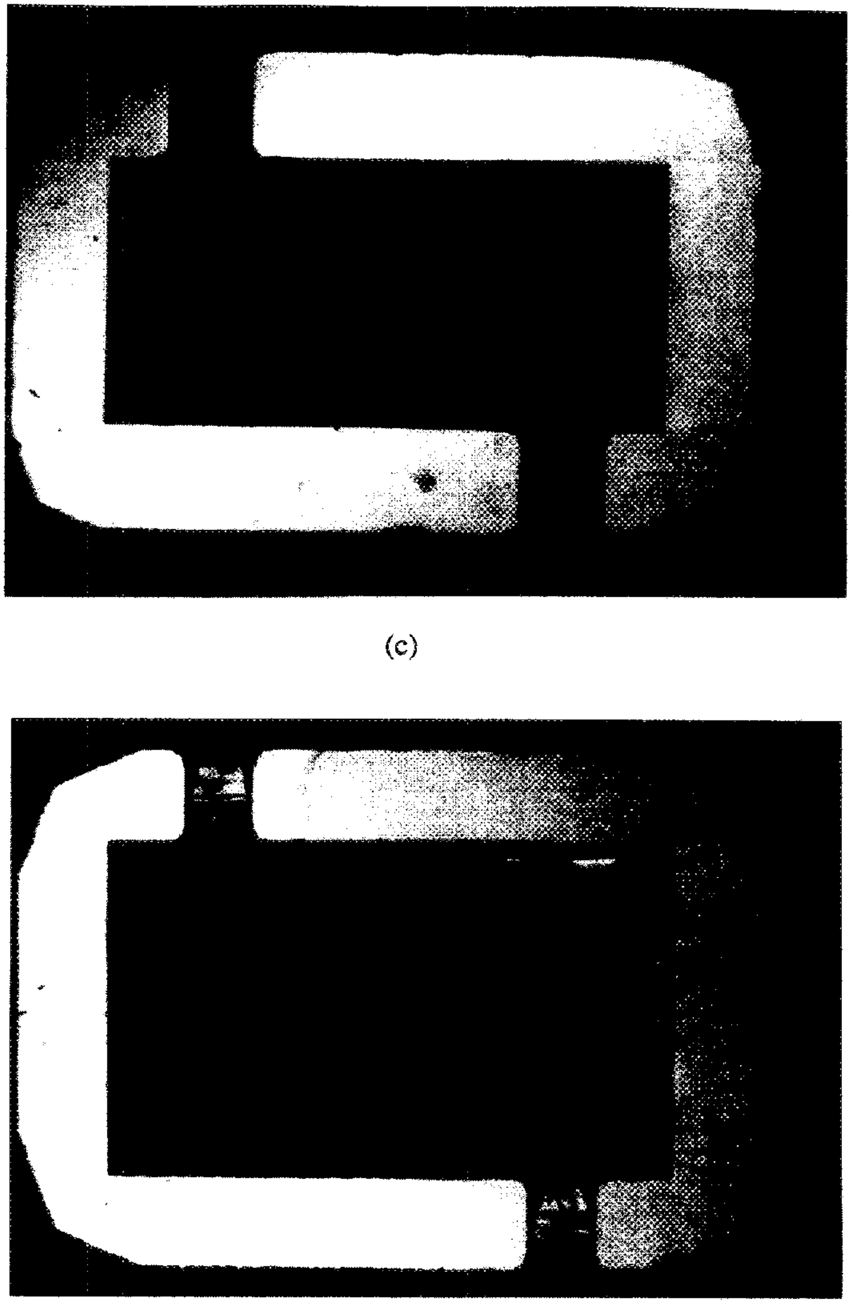
the wafer and deposited to result in a 3 μm layer of evaporated and then electroplated gold. The small holes opened in step 2 are all covered by the 3 μm-thick gold (Fig. 4.8(c)). Next a backside infrared alignment is performed to define the via-holes and the region of the suspended interdigitated fingers and a plasma etch is used to remove the backside membrane layer defined in the infrared alignment (Fig. 4.8(d)). If there is no air-bridge process, then the last step in the process is to remove the silicon substrate underneath the coupled-fingers and to create the via-holes. This is done by a wet chemical etch using EDP as the etching solution [30]. The EDP solution etches the silicon substrate at a rate around 1 μm/min at the temperature of 110° C. The etching process is stopped when the transparent membrane appears and the membrane filter is formed (Fig. 4.8(e)). As mentioned in step 2, some small areas of the membrane layer on the front side are etched. Now assuming there is no membrane layer etch in step 2, then the EDP etching of the via-holes will stop at the bottom of the front side membrane layer and there will always be a layer of dielectric membrane between the via-holes and the thin layer of gold deposited in step 3. Therefore, RF capacitors are formed between the topside metal and the via-holes resulting in an AC short. In order to achieve a DC short and provide an excellent grounding, the dielectric membrane between the topside metal and the via-holes must be removed. This explains why the membrane etching process is required in step 2. It is purely for via-hole formation.

The fabricated filters are shown in Fig. 4.11. A row of via-holes with a spacing of 2 mm ($\simeq \lambda_d/3$ at the center frequency) is etched around the membrane cavity to connect the CPW ground-plane next to the membrane to the bottom ground plane (Fig. 4.1). The via-holes are filled with silver epoxy but can be directly electro-plated with gold in monolithic fabrication techniques.

from the backside. However even with the 3 minutes BHF etch, the backside still has about 3000-4000Å SiO_2 and this is enough to protect the backside from another EDP etch. A picture of the wafer is taken at this step and is shown in Fig. 4.9(b). The next step is to put the wafer into the EDP solution again to etch the feeding channels and to continue etching the center opening. The etching process is stopped when the silicon wafer is completely etched through at the center opening. At this time the feeding channels have been etched about 150-200 μm deep and look like mouse holes (Fig. 4.9(c)). The last step is to evaporate a thin layer of gold on the entire wafer, then use electro-plating to increase the gold thickness to around 5 μm thick (Fig. 4.9(d)).

To assemble the filter, the micromachined cavity wafer with the mouse-hole channels is stacked on top of the membrane filter wafer using silver epoxy and this creates the partially shielded top cavity of the filter. A carrier wafer is stacked at the bottom of the membrane wafer to form the bottom cavity (Fig. 4.10(a)). The bottom carrier wafer has four micromachined V-shape grooves in its surface. The purpose of the four grooves is to provide a gas-escape channel for the bottom cavity. This avoids any pressure building up on the membrane layer after the bottom cavity is sealed. Another wafer is stacked on the top of the cavity wafer to shield the filter entirely (Fig. 4.10(b)). Both the top and bottom carrier wafers are electro-plated with gold to obtain a good RF ground plane. The filter is now ready to be tested.

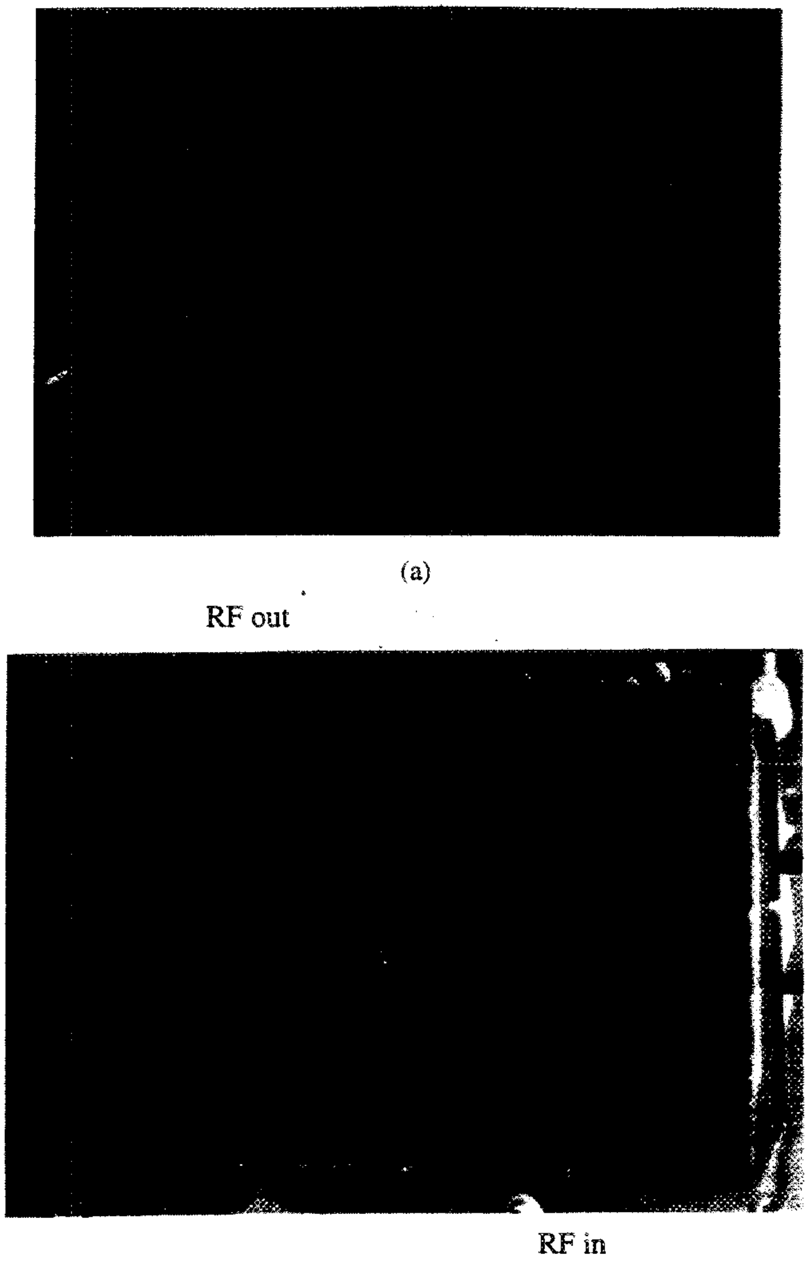
The membrane material used here is a tri-layer $SiO_2/Si_3N_4/SiO_2$ deposited on the silicon wafer. It can also be a thin layer polyimide membrane spun on the wafer but the idea is the same. Similarly, the top cavity used here does not need to be a micromachined cavity. It can be stamped using plastic material with metal coated at the surface for low cost applications, or can be milled using a numerical milling



(c)

(d)

Figure 4.9: Fabrication procedure of the micromachined cavity (see text for detail).



(a)

(b)

Figure 4.10: Assembly procedure of the micromachined filter: (a) a partially assembled membrane filter, (b) a fully assembled filter. The GCPW feeding line can be found at the up corner

In chapter 3, the quality factor of a membrane suspended stripline is measured and it gives a unloaded Q_u of 272 at 13.55 GHz which is also the center frequency of the 40% bandpass filter. Knowing the Q_u of the stripline resonators and the fractional bandwidth, the insertion loss of the filter can be predicted using equation 4.9. For the 6 sections 40% 0.05 dB equal-ripple filter, the tabular constant C_n in equation 4.9 is around 4.15 [56]. The calculated insertion loss of the filter is 0.33 dB which is almost the same as the measured result (0.3 dB). This proves that the performance of the micromachined interdigitated filter is conductor-loss limited and no another loss (radiation loss, dielectric loss) is present in this filter.

Since the filter is designed to have an equal-ripple response, the definition of pass-band is smaller than the usual 3-dB bandwidth definition. The equal-ripple bandwidth of this filter is around 43% which is very close to the designed 40% bandwidth. The center frequency shifted to 13.7 GHz from a 15 GHz design. This is quite significant and there are several factors can contribute to this frequency shift, which will be discussed in Section 4.5. The low-frequency roll-off response is very sharp with a 60 dB rejection at 5.8 GHz. The high frequency roll-off is also sharp with a 55 dB rejection at $2f_0$. The shape of the measured passband response is slightly unsymmetric. This is due to the nature of the unsymmetric coupled-line filter design and the limited quality factor Q_u of each finger. As can be seen, the filter is repetitive at $3f_0$ which is around 41 GHz and just beyond the measurement setup. The same filter is measured without the top shielding wafer (Fig. 4.13). The filter preserves the bandpass characteristics but the bandwidth increases from 6.5 GHz (43%) to 9.1 GHz (66%). The filter operates in stripline mode with the top-shielding wafer, and microstrip mode without it. As a result, the coupling capacitance between a pair of coupled-lines becomes stronger for the microstrip case, and this causes the increase in bandwidth. For both filters, with and without a top shielding wafer, the propagation media is air only, and there is no other dielectric material involved. Therefore, the filters propagate a dispersionless TEM mode. This can be seen from the measurements of group delay (Fig. 4.14) which shows a constant group delay over the entire operating bandwidth of both filters.

4.4.2 Narrow-band Interdigitated Filter (5%)

A narrow-band filter was fabricated and measured using the same approach outlined above. In this case, the finger length is 4.3 mm and the membrane dimensions are about 4.5 × 6.9 mm^2. The top cavity dimensions and the exact placement of the via-holes around the membrane are about 10% larger than the membrane dimensions. However, the finger length and the membrane length (in the resonant dimension) have been reduced by 10% to counteract this effect and to attempt to contract the frequency shift encountered in the 40% filter.

The measured port-to-port filter response is shown in Fig. 4.15. Two narrow-band planar filters are measured also yielding nearly identical results (± 0.1 dB in insertion loss). It is seen that the filter has a 14.8 GHz to 15.6 GHz equal-ripple passband with a port-to-port insertion loss of 2.0 dB at the center frequency of 15.2 GHz (including the loss of the two feed lines, 0.4 dB, and the 0.35 dB return loss from the S_{11} data). The 1.25 dB residual loss can also be traced fully to the ohmic loss [65]. The unloaded Q_u of a resonator is about 290 at 15.2 GHz using the square root relation found in Chapter 3 and the C_n is around 2.1 [56]. The calculated insertion is therefore 1.25 dB. Again, excellent agreement is achieved between the theory and measured result. The measured equal-ripple bandwidth is 5.5%. The filter shows a very sharp skirt with a 40 dB rejection at 12 GHz and 17 GHz. It is interesting to note that this filter shows a near-repetitive performance at $2f_o$. This comes from the higher cavity modes and the parasitic coupling capacitance from the tip of the fingers to the surrounding ground plane. This parasitic capacitance dominates over the weak coupling capacitance between the interdigitated fingers at $2f_o$ and renders the filter a capacitively loaded comb-line filter [48, 66]. This can be minimized by placing the tip of the fingers far away from the membrane edge.

4.5 An Interdigitated Filter Design Using Microwave Modeling Technique

In this section, a design example of an interdigitated filter based on the idea of microwave modeling technique is given. The design requirements were specified by Hughes Space & Telecommunication Group in El Segundo, CA, and are to have a 3-dB bandwidth of 3.3 GHz centered at 20.3 GHz with an input/output return loss better than 15 dB.

4.5.1 Microwave Modeling

Two design examples, based on the design equations given by [47], are presented in the previous section. Both the measured responses in Section 4.4.1 and Section 4.4.2 show a shift from the desired bandwidth and center frequency. This shift can become larger as the number of sections in the filter increases. The problem is caused by the design procedure used in [47] which neglects the mutual coupling between non-adjacent resonators. In order to eliminate this frequency shift, a bandwidth correction factor is needed to compensate for neglecting the mutual coupling between the non-adjacent resonators. Also each resonator needs to be shortened to compensate for the open-end effect. This correction, of course, preserves the correct center frequency. These problems present a challenge in the design of the 20.3 GHz micromachined interdigitated filters. Numerical techniques, although well developed for microstrip circuits, are not yet accurate for micromachined circuits. Therefore, other methods must be developed to help the design of the micromachined interdigitated filter.

Since the micromachined interdigitated filter is built on a very thin dielectric membrane (1.5 μm thick) and suspended in air as shown in Fig. 4.1, it results in a pure TEM propagation mode. Due to the nature of the TEM mode, the field distribution in the interdigitated filter can be accurately simulated by using a scaled model at a lower frequency. The microwave modeling technology has already been widely used in millimeter wave antenna design [20, 28] and provides accurate results up to several hundred GHz. Therefore, microwave model technique with TEM transmission lines can also be applied to the interdigitated filter design to solve the complicated mutual coupling problems from the non-adjacent fingers. Based on this concept, an 850 MHz microwave model is built with a scaling factor of 23.7. In this microwave model, a 152 μm thick polyethylene sheet (not scaled) is chosen to simulate the 1.5 μm thick dielectric membrane. An 8.4 mm thick Plexiglas is used to support the polyethylene membrane layer and provides the proper spacing for the top and bottom ground planes. This Plexiglas behaves similar to the 355 μm high-resistivity silicon wafer in the micromachined filters. The scaling factor, 23.7, results from the thickness ratio of the Plexiglas and the silicon wafer. The resonators and ground plane in the microwave model are made of copper tape. Metal screws are used to insure that both the top and bottom ground planes have a good DC and RF short. In order to achieve a 50 Ω input/output feeding impedance in the microwave model, two coaxial cables are used and connected right at the ends of the first and last fingers (Fig. 4.16). Matthaei's equations [47] were first used as a starting point and then the lengths, widths and gaps of the eight finger-resonators were adjusted experimentally until the design requirements were achieved. The measured results of the microwave model show a center frequency of 856 MHz and a 3-dB bandwidth of 140 MHz (Fig. 4.17). This translates into a center frequency of 20.28 GHz with a 3-dB bandwidth of 3.3 GHz for the micromachined filter.

4.5.2 Measurement of the 20.3 GHz Interdigitated Filter

Again, grounded coplanar waveguide transmission lines (GCPW) with micromachined mouse-holes are used in the 20.3 GHz micromachined filter as the feeding structures (Fig. 4.18). The physical dimensions of this filter are obtained by linear scaling the physical dimensions of the 850 MHz model with a scaling factor of 23.7 and are shown in Table 4.3. It is seen that the gap between the first finger and second finger is only 23 μm wide. Therefore, the coupling between these two fingers is very strong and disturbs the balance of the electric field on the feeding GCPW line (especially at the feeding point). This can create a non 50 Ω feeding impedance which greatly affects the response of the filter. To solve this problem, a 20 μm diameter gold wire is bonded across the first finger at the membrane-GCPW transition to equalize the two ground planes. This bonding wire is important for this filter because it forces a symmetrical field distribution at the transition and provides a 50 Ω feeding impedance at the GCPW line. The required bonding wires can be fabricated using an air-bridge technology in future designs.

There are still some dissimilarities between the microwave model and the 20.3 GHz micromachined filter. First, in the microwave model a 50 Ω coaxial cable is used to feed the filter (see Fig. 4.16), however, in the micromachined filter a grounded CPW line is used as the feeding structure (Fig. 4.11). Second, in the microwave model,

K	$s_{k,k+1}(\mu m)$	K	$w_k(\mu m)$	$L_k(\mu m)$
0, 6	23	0, 7	229	3373
1, 5	285	1, 6	503	3112
2, 4	371	2, 5	528	3101
3	376	3, 4	577	3086
K: finger number			w_k: finger width	
$s_{k,k+1}$: gap between fingers			L_k: finger length	

Table 4.3: The physical dimensions of the 20.3 GHz interdigitated filter. All the dimensions here are obtained by linear scaling the physical dimensions of the 850 MHz filter.

metal screws are used to provide a contact between top and bottom ground plane. In the micromachined filter, several V-shaped grooves are used as via holes between the top and bottom ground planes (Fig. 4.1). Third, in the microwave model, copper tape is used on the side-walls which are adjacent to the membrane. However, in the micromachined filter no metal is coated on the corresponding etched side-walls of the bottom micromachined membrane wafer (Fig. 4.1).

The 20 GHz filter is measured from 2 to 40 GHz and no tuning is attempted during the measurements. The results show a 1.7 dB port-to-port insertion loss at 20.3 GHz (including a 0.3 dB loss from each of the GCPW line) with a 3-dB bandwidth of 3.1 GHz (Fig. 4.19). The return loss is better than 15 dB in the passband. As can be seen, excellent agreement is achieved between the 850 MHz design and the 20.3 GHz results due to the TEM nature of the micromachined filter (i.e. no dispersion). Using equation 4.9, the insertion loss of the 20 GHz filter from the resonators along is calculated to be 0.79 dB (C_n=4.5 and Q=331). The input mismatch contributes 0.14 dB loss to the total insertion loss. Also, the GCPW feeding structure add another 0.6 dB (0.3 dB from each side of the feeding structure) into the total insertion loss of the filter. The calculated port-to-port insertion loss is therefore 1.53 dB which is very close to the measured value of 1.7 dB.

Fig. 4.19 shows a small discrepancy between the 850 MHz model and the 20 GHz

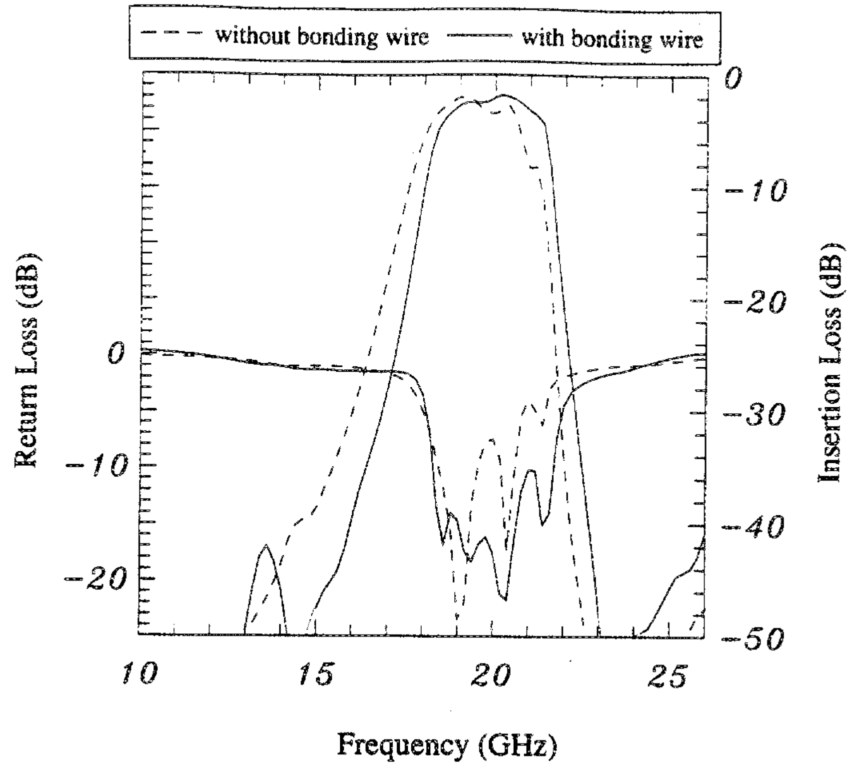


Figure 4.20: Comparison of the measured responses of the 20.3 GHz interdigitated filter with bonding wires and without bonding wires at the feeding points.

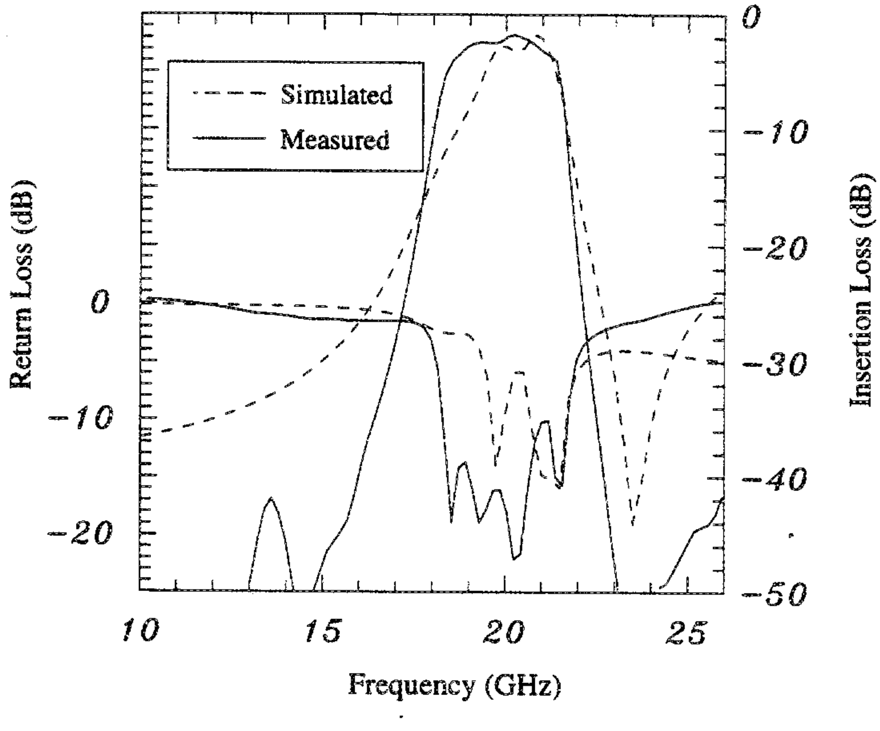


Figure 4.21: Simulated response of the 20.3 GHz interdigitated filter from *IE3D*.

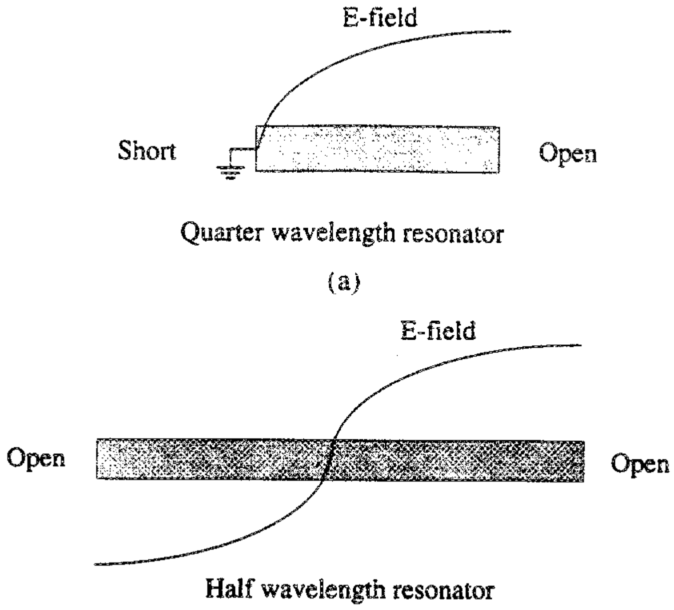
micromachined interdigitated filters.

4.6 Elimination of High-Order Cavity Modes

In the micromachined interdigitated filter designs, the quarter-wave resonators are suspended on a thin membrane and surrounded by a small micromachined cavity. The micromachined cavity prevents radiation loss and increases the quality factor of the resonator, and this results in a sharp roll-off response for filter design. However, as the operating frequency increases, the micromachined cavity can become a burden to the interdigitated stripline filters. This is especially true when the cavity size becomes a multiple of half-wavelength at the operating frequency. In that case, a cavity mode is triggered and begins to dominate the performance of the filter. This can be found in the measured results of the 15 GHz narrow band (Fig. 4.15) and the 20.3 GHz filter design (Fig. 4.20), where both of the cavities become larger than a half-wavelength at the upper rejection bands.

In order to avoid the cavity modes in a regular stripline structure, metal screws are often added along the stripline to provide a DC/RF short circuit between the top ground and bottom ground. These screws break the large mechanical housing into a lot of small cavities, and therefore, push the cavity mode to a much higher frequency. These screws can also be used to eliminate the substrate mode in the dielectric material. In the membrane design, it is impossible to use screws to break the cavity mode. However, the idea of breaking a large cavity into smaller cavities can be borrowed and used in the micromachined filter design.

In the interdigitated filter design, each finger is a quarter-wave long resonator with one end shorted to ground and the other end open-circuited. The field distribution along this resonator is very similar to the field distribution of a half-wavelength



(b)

Figure 4.22: Electrical field distribution on (a) a quarter wavelength resonator and (b) a half wavelength resonator.

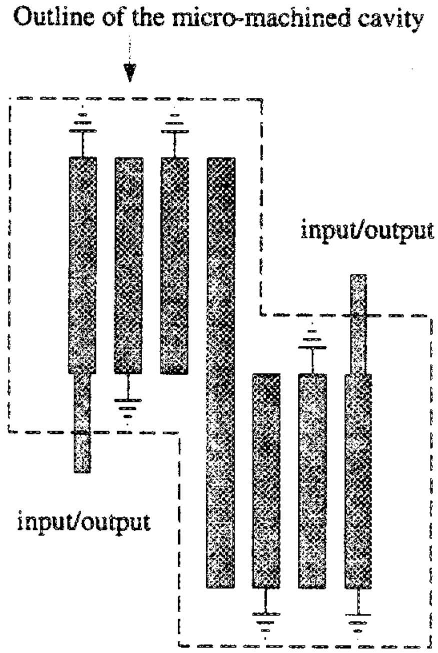


Figure 4.23: The proposed hybrid interdigitated filter. The center finger is a half wavelength resonator and it breaks the cavity into two small sub-cavities.

Bandwidth & Center Frequency	Q_U of Resonators	Calculated Loss from Resonators	Measured Loss from Feed-lines	Measured S_{11} Mismatch	Cal./Meas. Port-to-Port Insertion Loss
40% (13.5 GHz)	272	0.33 dB	0.4 dB	0.01 dB	0.74 dB/0.7 dB
5% (15.2 GHz)	290	1.25 dB	0.4 dB	0.35 dB	2.00 dB/2.0 dB
16% (20.3 GHz)	330	0.79 dB	0.6 dB	0.14 dB	1.53 dB/1.7 dB
16% (850 MHz)	1610	0.16 dB	0.3 dB	0.14 dB	0.60 dB/0.7 dB

Table 4.4: Summary of the measured and calculated loss performance of the interdigitated filters.

results on a 3-dB micromachined Lange-coupler are presented in this chapter.

Mixers are one of the basic components used in communication systems. They provide the function as a frequency multiplier (up-converter) or a frequency mixer (down-converter). However, when a mixer is used as a frequency converter, some of the undesired signals (such as the image frequency) are also involved in the conversion process. In communication systems, it is often necessary to eliminate the mixer image response and this is accomplished by using an image rejection mixer (also called a single-sideband mixer). The basic building block of an image rejection mixer is shown in Fig. 5.1. It includes two mixers (usually double-balanced mixers), a 90-degree RF hybrid, an LO power divider and a 90-degree hybrid at IF [69]. The bandwidth of the image rejection mixer is limited by the hybrid circuits used in the design. The advantage of this design is that it provides a low IF frequency with high isolation between the USB and LSB, and achieve a good isolation between the LO, RF and IF ports. If the IF signal is high (say around 1-2 GHz, similar to the direct broadcasting satellite system) and very high isolation (-40 dB to -60 dB) is not a major concern in the system level implementation, then a single-sideband mixer can be built using a bandpass filter in front of a balanced mixer (Fig. 5.2). The bandpass filter is designed to pass the RF frequency and reject the image frequency. This design employs only one balanced-mixer and does not use an RF hybrid, LO power divider and IF-hybrid, resulting in a much smaller unit. Based on this concept, a single-sideband mixer is built at Ku-band using micromachining technology. The balanced mixer used in the design is a 90-degree quadrature mixer, and the 90-degree hybrid in the balanced mixer is made using a micromachined Lange-coupler. Also, the interdigitated filter designed in Chapter 4 is used to provide the image rejection function.

5.2 Design of Lange Couplers

The Lange-coupler is a wide-band 90-degree quadrature hybrid circuit which was invented by Lange in 1969 [68]. The basic idea of this design comes from the infinite parallel coupled-line array as discussed in section 4.2.2 (Fig. 4.5) [53, 52]. The interdigitated scheme is used to achieve a tight coupling which is very difficult to achieve in a non-interdigitated edge-coupled structure. The four-port coupler is formed by alternatively connecting the ends of the coupled array together at the "A" and "B" sides (see Fig. 5.3). The analysis of the Lange-couplers is very similar to the analysis of the interdigitated filters and starts from the even- and odd-mode analysis of a pair coupled-lines, and is well explained by Ren [70] and Ou [71]. In Ren's analysis, the coupling from the non-adjacent lines are all included in the admittance matrix, but no closed design equations are available. However in Ou's analysis, the mutual coupling from non-adjacent lines are ignored, which simplifies the analysis and a set of closed design equations are given.

Briefly, the analysis starts from the static capacitance of an equally-spaced parallel-coupled line array . With the knowledge of the self and mutual coupling capacitances, an admittance matrix of the coupled array can be derived. Since the structure is perfectly symmetric, a perfect isolation can be expected at the isolated port. Also, the four ports are assumed to be terminated with 50Ω loads and a perfect match is achieved at the center frequency. By putting these two conditions into the admittance matrix, the admittance matrix can be simplified and a set of design equations are derived from it. They are given in [71] as:

$$\mathrm{Y}_0^2 = \frac{[(\mathrm{k}-1)\mathrm{Y}_{\mathrm{oo}}^2 + \mathrm{Y}_{\mathrm{oo}}\mathrm{Y}_{\mathrm{oe}}][(\mathrm{k}-1)\mathrm{Y}_{\mathrm{oe}}^2 + \mathrm{Y}_{\mathrm{oo}}\mathrm{Y}_{\mathrm{oe}}]}{(\mathrm{Y}_{\mathrm{oo}} + \mathrm{Y}_{\mathrm{oe}})^2} \qquad (5.1)$$

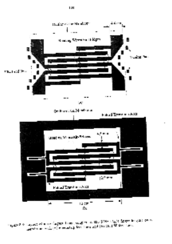
$$C_{k,k+1} = \frac{1}{2v}(Y_{oo} - Y_{oe}) = \frac{\eta_0 \epsilon_0 \sqrt{\epsilon_r}(Y_{oo} - Y_{oe})}{2} \tag{5.4}$$

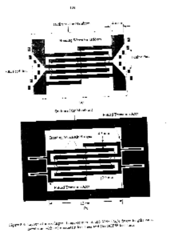
where v is the velocity of the light in the transmission medium, and in the membrane case it is equal to the light speed of 3×10^{10} cm/sec (assuming $\epsilon_{\text{eff}} \simeq 1.00$). The physical dimensions of the coupled structure can then be obtained from the even- and odd-mode capacitance analysis (Section 4.2.3). A Fortran 77 code is developed to solve the Y_{oe}, Y_{oo} and to give the corresponding physical dimensions of the Lange-coupler. This code is listed in Appendix D for the reader's convenience.

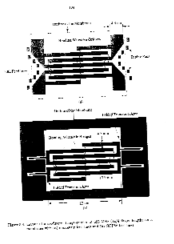
The required Y_{oe}, Y_{oo}, and the normalized $C_{k,k+1}/\epsilon_0\epsilon_r$ for three commonly used coupling ratios with different finger numbers are listed in Table 5.1. As can be seen, the required coupling capacitance $C_{k,k+1}$ for the same coupling value drops quickly as the number of fingers increase. This implies that for the same coupling, the spacing between the coupled fingers increases with the number of fingers used. Usually the wider gap spacing, the more tolerance the Lange-coupler will have in the design and fabrication. However, when the finger number increases, the required finger width decreases (less tolerance), also the complexity of the coupler increases (more bonding wires or air-bridges). Therefore, a tradeoff on choosing the number of fingers is needed to achieve a good performance (high tolerance) and low complexity for the Lange-coupler. Usually, a four-finger topology is used in a coupler built on a high dielectric constant substrate such as GaAs or Alumina. The required gap spacing and finger width for a four-finger 3-dB coupler on a 635 μm-thick alumina substrate are around 50 μm and 70 μm [72] respectively, which can be easily fabricated in a hybrid or monolithic form. For a low dielectric constant substrate, more fingers are required to achieve the same coupling ratio as the high dielectric constant substrates. For the micromachined Lange-coupler built on a membrane with an effective dielectric constant of one, a six-finger design is considered.

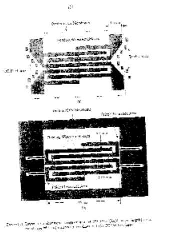
In the design equations used, the mutual coupling capacitance from the non-adjacent fingers is assumed to be small and is ignored. This is a good assumption when using a high dielectric constant substrate since most of the electric field is locally confined between the adjacent fingers, and the cross talk between non-adjacent fingers is small. However, for the membrane case, the electric field is more spread out between all the fingers due to the low dielectric constant, and therefore a strong mutual coupling is expected between the non-adjacent fingers. This implies that the design equations from Ou [71], which ignore the mutual coupling from non-adjacent fingers, are not accurate for the membrane Lange-coupler design. However, with the help of the microwave modeling technique, discussed in Chapter 4, the problem associated with the mutual coupling can be solved experimentally. A scaled microwave model is built and the finger widths and gaps are adjusted experimentally to compensate the error of neglecting the non-adjacent mutual-coupling in the design equations.

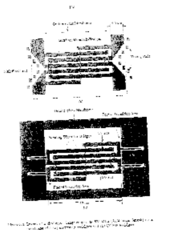
Another point that needs to be considered in the membrane Lange-coupler is whether a stripline or a microstrip design should be used. As discussed in Chapters 3 and 4, a stripline geometry results in a higher Q and lower loss than the microstrip line. However, due to the wide-band characteristic of the Lange coupler, the quality factor will not be a major concern in the design. In a stripline structure, a shielded top cavity is required, and if this cavity is larger than a half-wavelength, then cavity modes may be triggered. For the Lange coupler, each finger is quarter-wavelength long at the center frequency (f_0), and the bandwidth of a Lange-coupler can easily cover more than an octave. If the stripline design is used in the Lange-

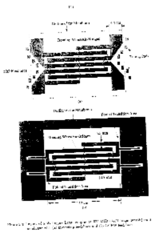


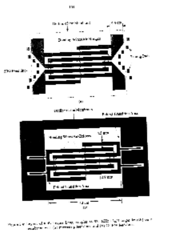


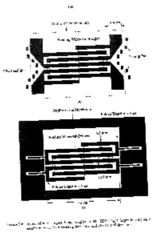












direct port and isolated port need to be terminated while measuring the coupling at the coupled port. The termination is accomplished by using 50Ω SMA terminators connected at the end of the feeding coaxial cables. In order to measure the phase difference between the coupled port and direct port, electric delays are set in the measurement system to move the reference plane to the edge of the coupler. The measured response is shown in Fig. 5.5. An input return loss better than 15 dB is achieved, which proves the idea of the transition design. The center frequency of the coupler shifts to 585 MHz. This is due to the extra length from the folded transition areas. However, a resonance occurs around 1 GHz. In order to suppress the 1 GHz resonance, two extra bonding wires (air-bridges) are placed at the centered coupled fingers (see Fig. 5.6). The measured results of the coupler with the two extra bonding wires are shown in Fig. 5.7. The measured results show amplitude balance of 3.4 ± 0.6 dB over the 300 MHz to 850 MHz frequency range and a good phase balance (90 ± 3 degree) between the coupled port and directed port from 100 MHz to 1.1 GHz. A metal sheet has also been suspended on top of the coupler to check how it affects the response of the coupler. The result shows an almost identical response as the one without the metal sheet. This indicates that the radiation loss from the tightly coupled structure is small.

Next, a 15 GHz (585 MHz × 25.6) Lange-coupler is fabricated on a 355 μm-thick high resistivity silicon wafer. The finger length, width and spacing of the 15 GHz design are translated directly from the microwave model by a scaling factor of 25.6 and are 4688 μm, 178 μm and 36 μm, respectively.

The physical dimensions of the micromachined Lange-coupler are also used in EESof Libra$^{\text{TM}}$ simulation and the simulated results are shown in Fig. 5.8. The model that Libra uses is based on Childs' formulas [75] which also ignore the mutual cou-

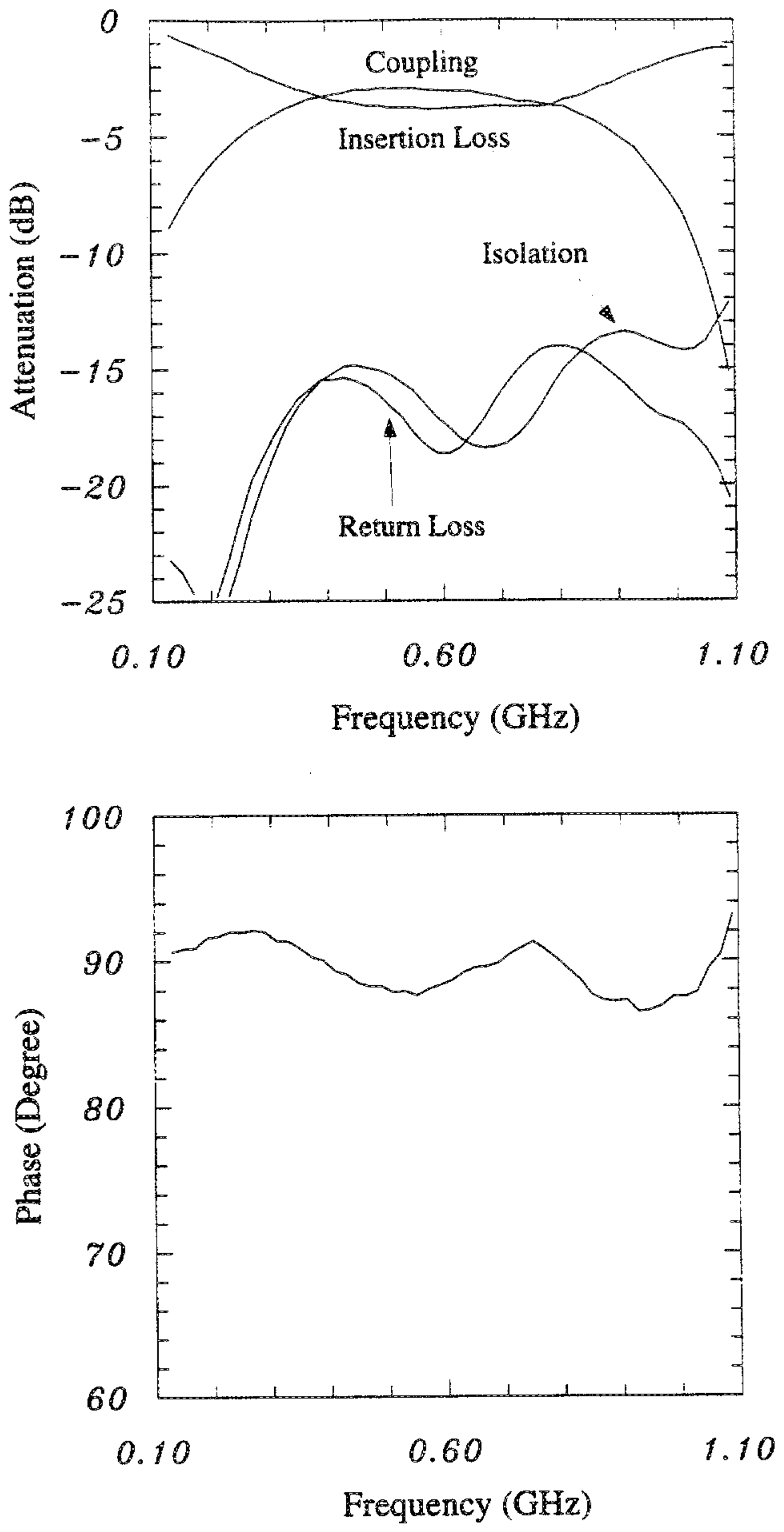


Figure 5.7: Measured response of the 625 MHz Lange-coupler after two extra bonding wires are placed.

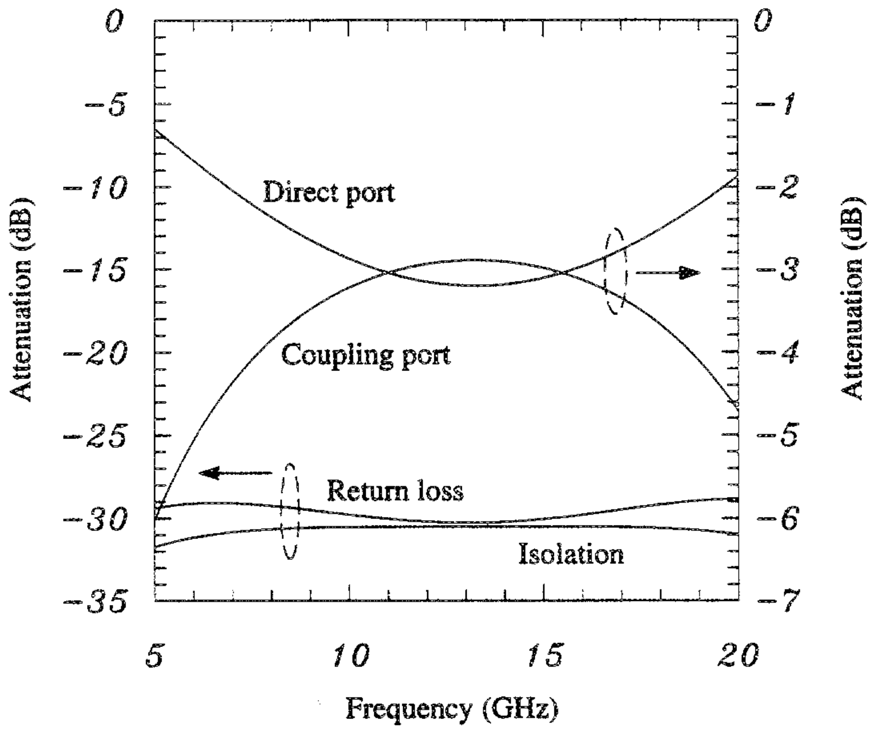


Figure 5.8: Simulated micromachined membrane Lange-coupler. The finger length is changed from 4688 μm to 5660 μm in order to compensate the extra length from the folded transition areas.

resistor. However, even with the silver epoxy, there is still some uncertainties on the exact value of each resistor, and the final resistor value is around 50±15Ω.

The measurement system is calibrated using the SOLT on wafer calibration routine as discussed in section 4.4.1. The Lange-coupler is measured from 5 to 20 GHz and the measured results are shown in Fig. 5.10. The isolation of the micromachined Lange-coupler is better than 15 dB for the entire bandwidth. However, the input return loss is 11 dB at 20 GHz, and this is believed due to the non-perfect thin film resistors. The phase difference between the coupled port and direct port is 90 ± 3 degree from 5 to 20 GHz. The coupling response is preserved but with higher insertion loss. This is due to the higher conductor loss from the fingers and the loss from the input/output feed lines. The length of the input/output feed line is 3 mm long (see Fig. 5.9) and contributes about 0.3 dB loss from each section (see Fig. 3.11). The measured 4.2±0.8 dB coupling therefore includes 0.6 dB loss from the GCPW feeding structures and also 0.15 dB from the S_{11} mismatch. The ohmic loss of the coupler can be calculated to be 0.5 dB (see Table 5.2). The coupling bandwidth covers the 6.5 GHz to 20 GHz and is centered at 13.25 GHz. Compared to the microwave model, the center frequency shifts 1.7 GHz lower. (The center frequency of the microwave model is at 585 MHz which translates to a center frequency of 14.97 GHz for the micromachined Lange-coupler.) One of the reasons that causes the frequency shift is from the folded transition areas. In the microwave model, the side-walls of the Plexiglas sheet are covered by copper tape, therefore, no electric field is coupled into the side-walls (silicon substrate). However, in the micromachined circuit, there is no metal coated at the etched side-walls (see Fig. 4.1), and the etched side-walls stopped right at the edge of the top ground plane. Therefore, when the electric field is traveling in the folded transition area, some of the electric field couples through

Measured Coupling Ratio (dB)	GCPW Feed-line Loss (dB)	Measured S_{11} Loss (dB)	Theoretical Coupling Loss (dB)	Calculated Ohmic Loss (dB)
4.2±0.8	0.6	0.15	3±0.8	0.5

Table 5.2: Summary of the measured and calculated loss performance of the micromachined Lange-coupler.

the silicon substrate and terminates at the ground plane. This results in a higher effective dielectric constant and reflects a longer electric length. Another reason is due to the higher conductor loss and mismatch which shift the shape of the coupling response. However, due to the wide-band characteristic of the Lange-coupler, this shift can be tolerated in most circuit applications and should not cause any problems. Also, future numerical modeling of the micromachined structure should solve this problem.

5.3 90-Degree Quadrature Balanced Mixers and Single-Sideband Mixers

Balanced mixers are the most popular mixers used in microwave systems. Compared to single-ended mixers, balanced mixers have better power handling capability and better immunity to the LO AM noise and to other spurious signals [69]. The balanced mixers can be separated into two categories: single-balanced mixers and double-balanced mixers. In the single-balanced mixer design, 180 degree or 90-degree quadrature hybrid circuits are used to provide the required amplitude and phase for the Schottky diodes. Usually magic tee and rat-race ring couplers are used in the 180 degree design, however, the bandwidth of these two hybrid circuits are both limited in the 20% range. For the 90-degree design, branch line and Lange-couplers can be used. The branch line coupler is a narrow-band hybrid circuit and has relatively a large physical size, hence it is seldom used. The Lange coupler is physically compact and can cover a wide bandwidth, therefore, most of the single-balanced mixers are

R_s (Ω)	C_{j0} (pF)	C_p (pF)	I_s (nA)	ϕ (eV)	F_c (GHz)
3	0.22	0.25	64	0.41	240

Table 5.3: DC parameters of the Metelics^{TM} MSS-30254-B20 low barrier silicon Schottky diode.

bandwidth using the capacitor design. In the shunt design, capacitors are needed for DC blocking, and these capacitors can be substituted by a simple coupling gap in the transmission line. Furthermore, the coupling gap design can improve the isolation between the IF and the RF/LO ports, especially for the low IF case. Therefore, from the monolithic point of view, the shunt configuration provides more attractive features than the series configuration in the circuit layout and fabrication.

A design of a single-balanced mixer is given here. In this design, the RF and LO are chosen to be 15 and 16 GHz, respectively. The 90-degree hybrid is the micromachined Lange coupled which is presented in section 5.2. The diodes are Metelics^{TM} MSS-30254-B20 low barrier Tee type silicon Schottky beam lead diodes. The diode has an anode diameter of 2.5 μm and the 1 mA current occurs at 0.25 V. Assuming a perfect Schottky diode, the barrier height and leakage current of the diode are calculated to be around 0.41 eV and 64 nA, respectively [76, 77]. Other DC parameters of the diode are listed in Table 5.3. Due to the physical layout of the diode chip (see Fig. 5.14), the series configuration in Fig. 5.11 is chosen in the design.

Both of the circuits shown in Fig. 5.11 have a symmetric structure, and therefore the analysis of the single-balanced mixers can be simplified as two identical single-ended mixers. The time harmonic nonlinear analysis technique is used to analyze the mixers [73, 74]. During the analysis, an ideal Lange-coupler is used as a diplexer to isolate the LO and RF ports. The diode is connected between the ground plane and the Lange-coupler's coupled port, and no matching circuit is added in the mixer yet (Fig. 5.13(a)). An RF choke is included in the circuit to provide a DC return path for the diode. First, the LO power is adjusted during the analysis to achieve a good conversion performance, and the diode impedance under the corresponding LO pump power is calculated. After knowing the diode impedance, a matching network is then added between the diode and the RF/LO sources to reduce the mismatch loss (Fig. 5.13(b)). The DC return path used in Fig. 5.13(a) can be substituted by a shorted stub design and absorbed into the matching network. The new circuit is analyzed again, and both the LO power level and matching network are adjusted to achieve an optimized conversion performance. The tuning process was done by the EESof Libra^{TM} optimization routine. After a good conversion-loss value is achieved, the second diode is added into the circuit, and an RF/LO short is placed between the two diodes. The matching networks in the final circuit are adjusted again to insure a good conversion performance. The RF/LO short in the circuit is accomplished by an opened quarter-wavelength radial stub design. If the IF frequency is low, then the RF/LO short can be achieved by a capacitor design. In this case, only a radial stub is used to reject the RF/LO signals. If a higher rejection level is required, an off-chip lowpass filter can be used to improve the rejection value. The simulated response of the radial stub IF filter is shown in Fig. 5.12. The equivalent circuit of the final design is shown in Fig. 5.13(c). The calculated diode impedances and conversion loss of this circuit with a 5 mW (7 dBm) LO pump power are listed in Table 5.4.

The membrane Lange-coupler designed in section 5.2 is fed by GCPW structures. Therefore, it is more convenient to use the GCPW structure for the rest of the circuit to avoid any other transition design. The physical dimensions of the GCPW transmission lines are calculated using the EESof Linecalc^{TM} and the design of the

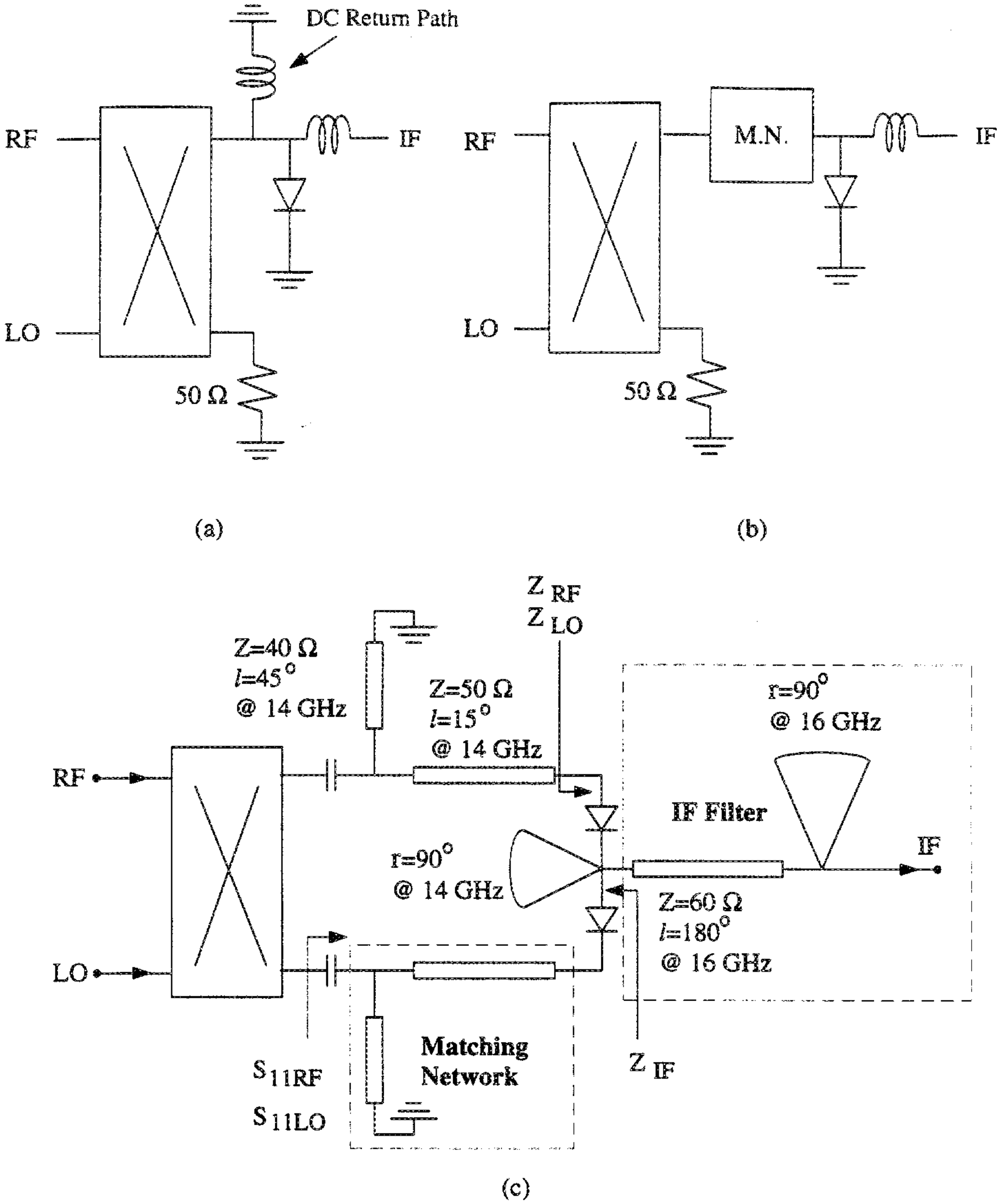


Figure 5.13: The design procedure of the 90-degree single-balanced mixer starts from a single-ended mixer (a). Then, a matching network is added between the diode and the RF/LO sources to reduce the RF mismatch (b). Finally, the second diode and an IF filter are put into the circuit to finish the design. The electric parameters of the matching network and IF filter are also included in figure (c).

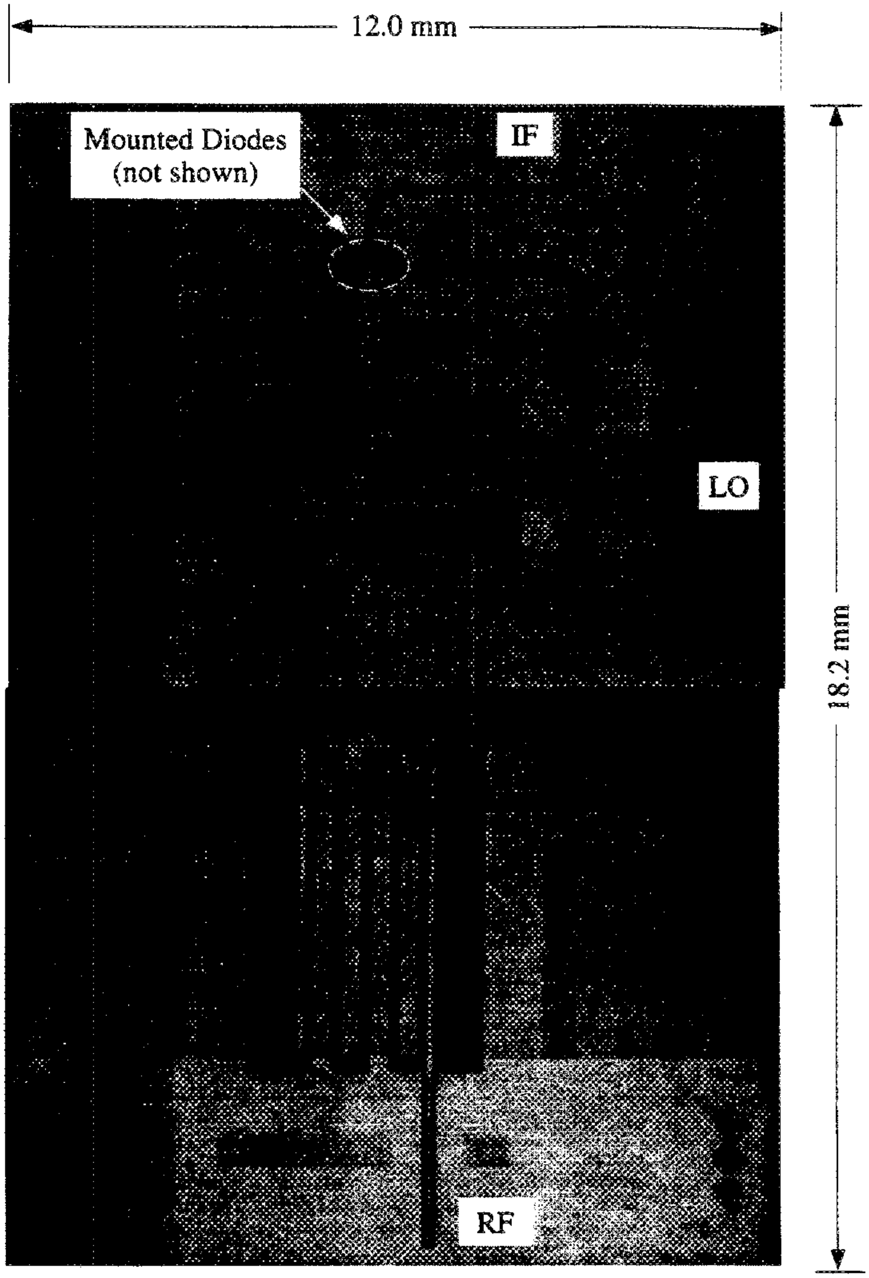


Figure 5.14: The fabricated micromachined single-sideband mixer. Dimensions of the chip are $12.0 \times 18.2\ mm^2$.

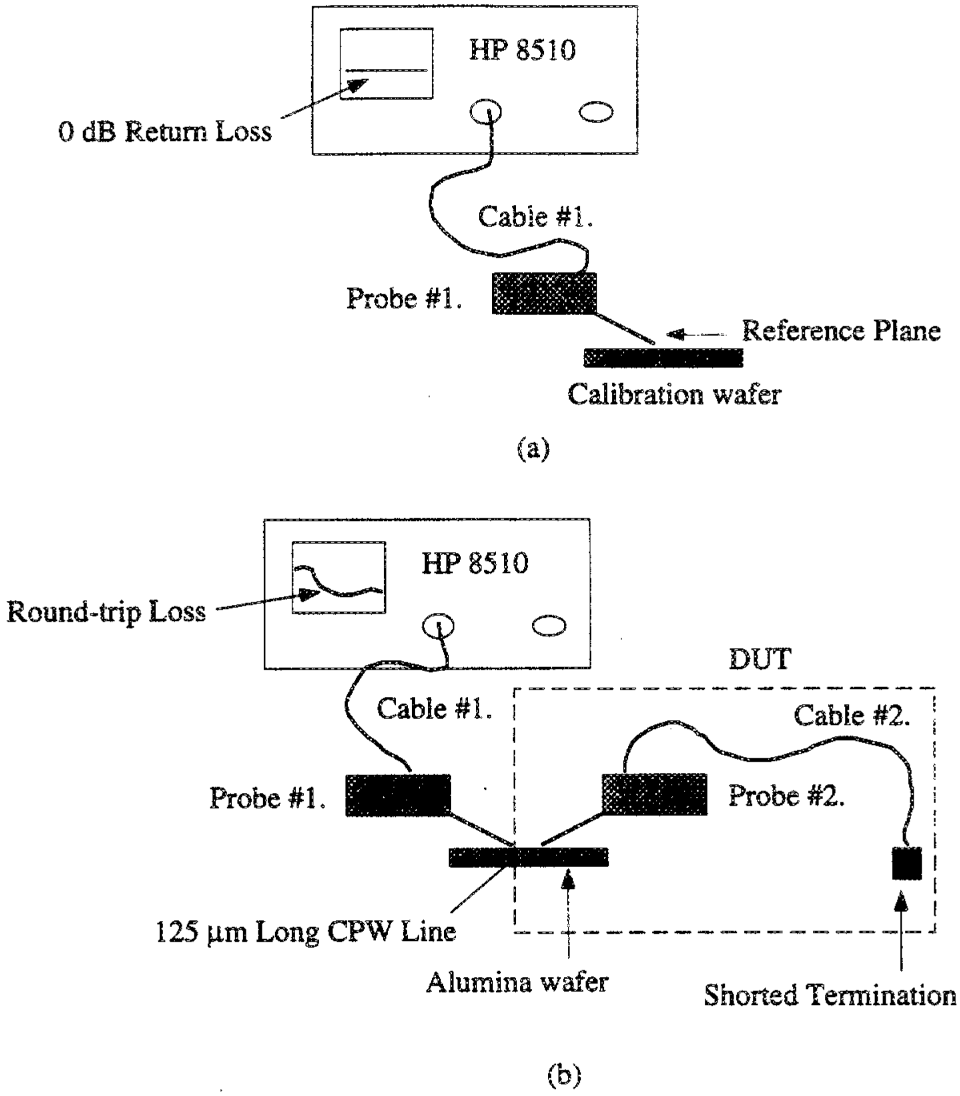
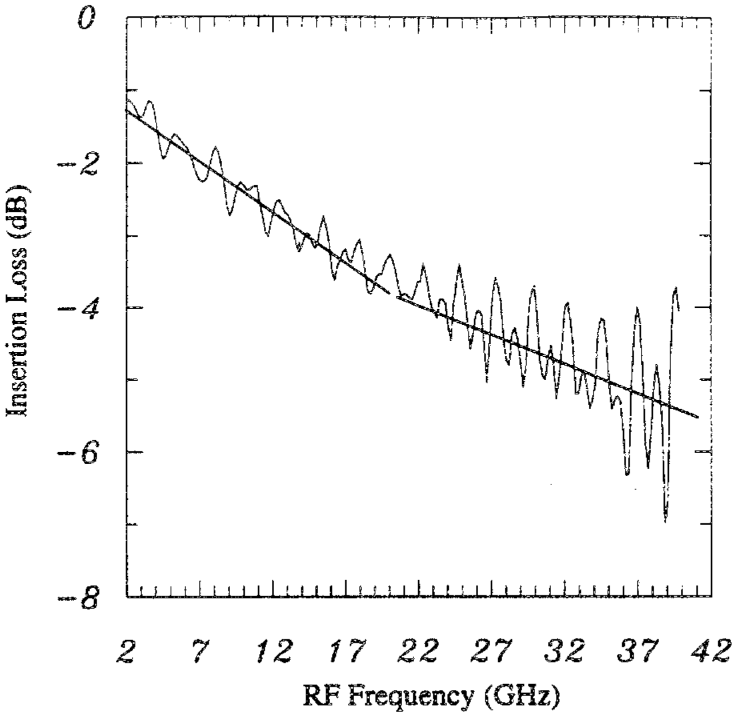
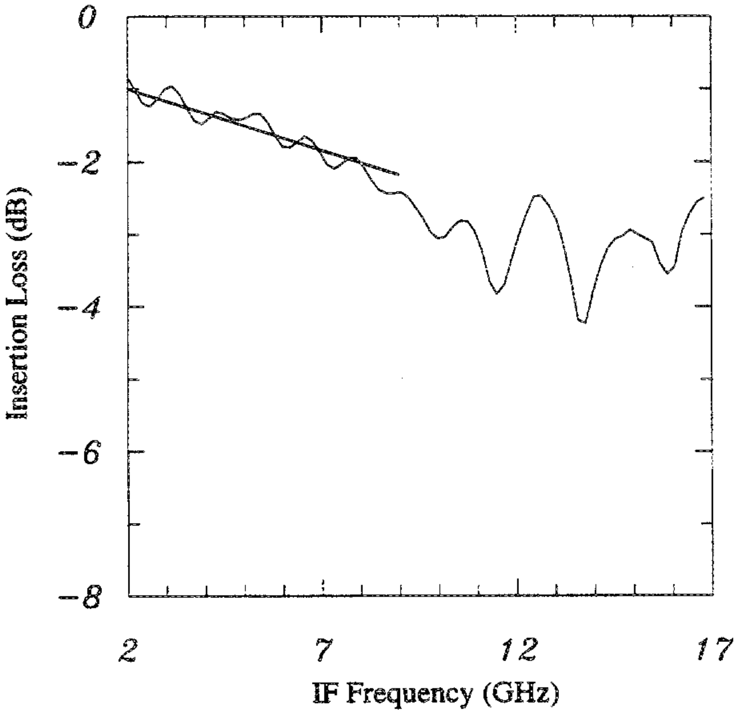


Figure 5.15: A probe system is first calibrated using the on-wafer calibration routine (a). The second probe system to be measured is shorted at one end. Then, the two probe systems are brought to a 125 μm long CPW thru line (b). The measured input return loss at the first port becomes the round-trip loss of the second probe system.



(a)



(b)

Figure 5.16: Measured insertion loss of (a) the RF probe system and (b) the IF probe system.

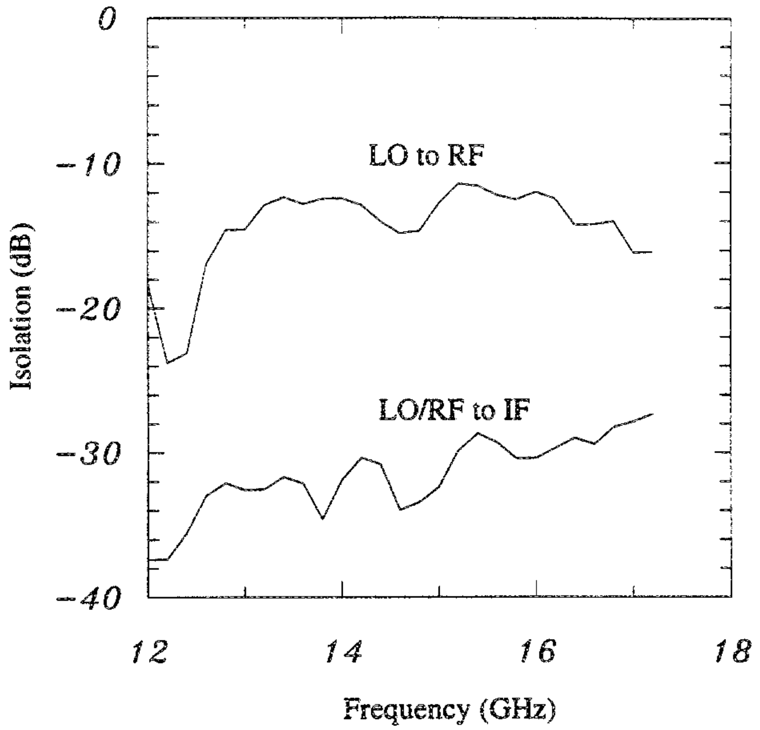


Figure 5.19: Measured port-isolation of the 90-degree single-balanced mixer.

For the single-sideband mixer, a shielding cavity is first placed on top of the filter to result in a stripline structure. The RF signal passes through the filter to the single-balanced mixer. Neither a circulator nor an amplifier is added between the filter and mixer, therefore higher conversion loss may be expected due to the internal impedance mismatch. The filter itself has an insertion loss around 0.7 dB and the knee of the upper rejection band of the filter is around 17 GHz (see Fig. 4.12). Any RF signal higher than 17 GHz will be rejected by the bandpass filter. The mixer is first measured with a fixed IF frequency, the RF signal is swept from 12 GHz to 17 GHz, and the LO frequency is set at $f_{RF} + f_{IF}$. The measured results are shown in Fig. 5.20. The conversion loss from this mixer is around 1.5 dB higher than the single-balanced mixer measured in Fig. 5.17. This 1.5 dB extra loss includes the 0.7 dB filter loss and about 0.8 dB mismatch loss between the filter and the

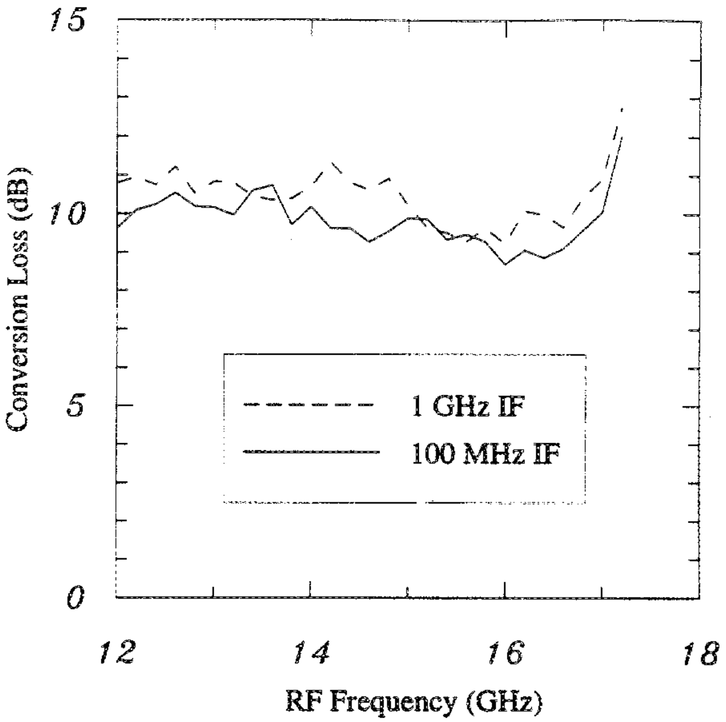


Figure 5.20: Measured conversion loss versus the RF frequency for the single-sideband single-balanced mixer.

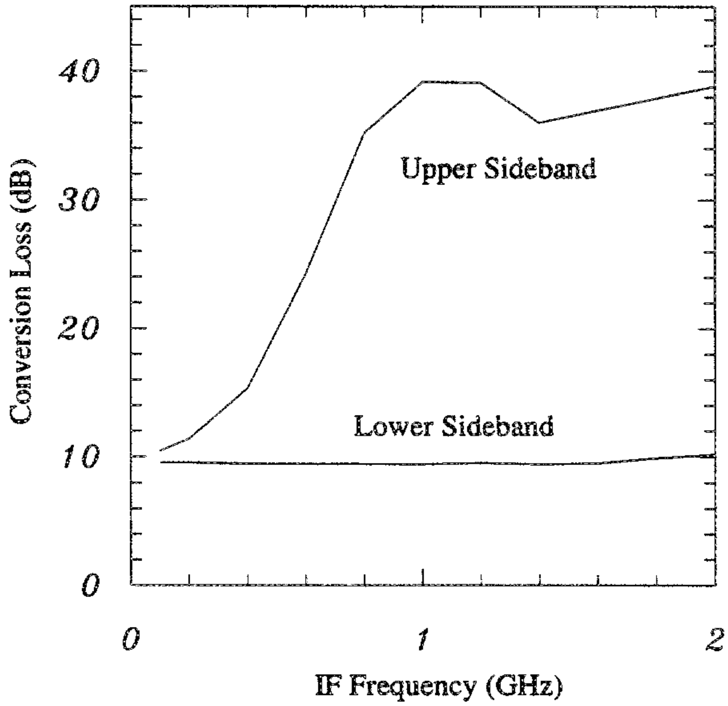


Figure 5.21: Measured conversion loss versus the IF frequency for the single-sideband single-balanced mixer. The LO frequency is kept at 17 GHz during the measurement.

CHAPTER VI

CONCLUSIONS AND FUTURE WORK

Planar lumped-elements, coupled-line filters, Lange-couplers and mixers have been developed and fabricated on high-resistivity membrane silicon wafers using micromachining technique. The micromachining technology is fully compatible with the via-hole process in GaAs and InP MMIC. The micromachined membrane technology can provide a localized area that has an effective dielectric constant close to one ($\epsilon_r \simeq 1$) in a MMIC circuit design. This localized low-ϵ_r environment has the following advantages for the MMIC design: First, due to its low dielectric constant, the parasitic capacitance from the substrate can be reduced which results in a higher resonant frequency for lumped-elements. Second, there is no dielectric loss and no dispersion in the air-only transmission medium, and this supports a pure TEM wave which is very useful for filter and passive circuit design.

Membrane suspended spiral inductors, developed employing the micromachining technology, have demonstrated a resonant frequency of 60-70 GHz which is three times higher than the same inductors built on silicon wafers. A stripline resonator built by the micromachining technology has shown a conductor-loss limited performance, and an unloaded Q_u of 460 has been measured at 39 GHz. Based on the micromachined stripline resonator, three interdigitated filters with different band-design. The possibility of employing a low-loss polyimide layer to substitute the $SiO_2/Si_3N_4/SiO_2$ membrane and the corresponding fabrication process should be developed. With these improvements and the new Silicon-Germanium (Si-Ge) heterojunction transistors, the silicon micromachined membrane technology will contribute to the high frequency MMIC design area and achieve the high-quality and low-cost in a mass-production environment.

This thesis presented a preliminary collection of high-quality circuits (filters, couplers, SSB mixers, lumped elements and resonators) that could be developed using this new technology. Examples of high frequency or more complicated circuits that can be fabricated as an extension to this work are:

1. Single-sideband mixers at 60, 77, 94 and 140 GHz: The application areas are in millimeter-wave communication systems and automotive collision avoidance radars. In these mixers, a micromachined filter is employed in front of a balanced mixer to reject the image frequency and achieve the single-sideband mixing. An amplifier can be added between the filter and mixer to isolate the two circuits and reduce the mismatch loss form the filter/mixer junction. Also, with Si-Ge transistors, these mixers can be directly integrated with antennas and front-end amplifiers as an integrated receiver module.
2. Varactor tuned stripline filters: Varactors can be used in a capacitive loaded comb-line filter or interdigitated filter as tuning components. This capacitive loaded design can significantly reduce the size of the filter and avoid cavity modes at high frequencies. Reverse bias can be applied on varactors to change their capacitance values and achieve a tunable band-

be employed in the wideband millimeter-wave circuits, such as branch-line couplers, Lange-couplers and rat-race couplers. These units can be used in monopulse radar systems to provide the required sum and difference patterns with deep nulls in the difference patterns.

This is just a collection of circuits that can be developed in the near future using this technology. However, they will only be achieved if they can be built using a low-cost process and are totally integrated with the MMIC fabrication process. Future work needs to be done to completely achieve this goal.

APPENDIX A

A QUASI-OPTICAL AMPLIFIER

This was the author's very first project at the University of Michigan, and is included for completeness purposes.

A.1 Introduction

Millimeter-wave amplifiers are currently based on waveguide designs for applications above 60 GHz. The amplifiers employ a GaAs or InP HEMT chip with an appropriate waveguide-to-microstrip or waveguide-to-cpw (coplanar waveguide) transition [82], and are hard and expensive to fabricate above 100 GHz. It is therefore important to integrate the transistor amplifier directly with a radiating structure (e.g. planar antenna or grid) which results in a monolithic amplifier that is inexpensive and can be easily scaled to millimeter-wave frequencies. This approach has been pioneered by Kim and Rutledge in a paper on a 50-element grid amplifier [83]. We have extended this approach to a single-element amplifier that is well suited for low-noise systems (Fig. A.1) or a space-fed waveguide amplifier array.

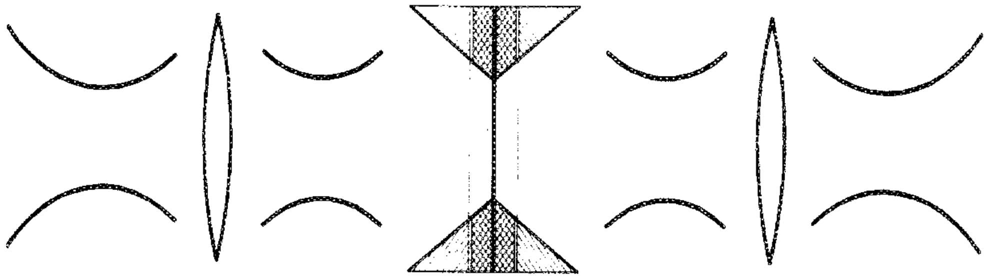


Figure A.1: Schematic view of the quasi-optical amplifier. A horn extension can be placed at the aperture of the horn to increase the directivity and the Gaussian-coupling efficiency.

A.2 Quasi-Optical Amplifier Design

The integrated horn antenna forms the building block of the quasi-optical amplifier [84]. It consists of a dipole probe suspended in an etched pyramidal horn in silicon (or GaAs). The quasi-optical amplifier employs a differential amplifier at the apex of two perpendicular dipole-probes inside the horn cavity [85]. The vertically-polarized dipole is the input port to the differential amplifier and the horizontally-polarized dipole is the output port of the amplifier. Two polarizing grids are used for isolation at the input and output ports.

A close up view of the dipole probes and differential amplifier is shown in Fig. A.2. The chip transistors used are NEC 32100 with a maximum available gain of 14 dB at 6 GHz. The gates of the two transistors are connected to the vertical dipole (input probe) using bond wires and their drains are connected to the horizontal dipole probe (output probe). The transistor source terminals are connected together using a symmetrical cross pattern at the apex of the dipoles. Two 1KΩ and 100Ω resistors are connected to the tips of the vertical and horizontal antennas, respectively, for bias considerations. A 100Ω bias resistor is connected to the source terminal and the DC source connection is achieved using a very narrow line as shown in Fig. A.2. A DC ground is printed all around the antenna structure and bypass capacitors are used on the DC bias lines to suppress low-frequency oscillations. The active substrate is a 1.25 mm thick Duroid (Rogers Corp) with $\epsilon_r = 10.5$. The polarizing reflectors are printed on very thin Duroid substrates (0.35 mm thick) with $\epsilon_r = 2.2$. All metalizations are etched in copper and the transistors, resistors and capacitors are surface mounted on the Duroid substrate.

The equivalent impedance at the gate and drain terminals is half the antenna input impedance. The impedance of the input and output dipoles can be independently adjusted by choosing the length of the dipole probes inside the horn cavity, and the positions of the grid reflectors behind the dipoles (see [84] for more detail). In this design, both antennas are chosen to be nearly $0.4\lambda_0$ long in a cavity cross-section of $0.6\lambda_0$ and the polarizing reflectors are placed $0.14\lambda_0$ behind the dipoles. The horn aperture is chosen to be $1.35\lambda_0$. This aperture dimension is compatible with quasi-integrated horn designs having 20 dB or 23 dB directivities and high Gaussian-coupling efficiencies (see [86]). The measured impedance including the effect of the bias resistors at the tip of the dipole antennas is around $(90 + j40)\Omega$ for the input dipole and $(70 + j50)\Omega$ for the output dipole (Fig. A.3). This results in a calculated differential gain of 12.5 dB at 6 GHz with a 3 dB bandwidth of 450 MHz.

It is also possible to place the differential amplifier and the polarizing grids in a square waveguide [87]. In this case, the input mode is TE_{10} and the output mode is TE_{01}. The impedance of the vertical and horizontal probes can be easily measured or electromagnetically modeled. This configuration is ideal for a space-fed waveguide amplifier at very high frequencies (75-110 GHz).

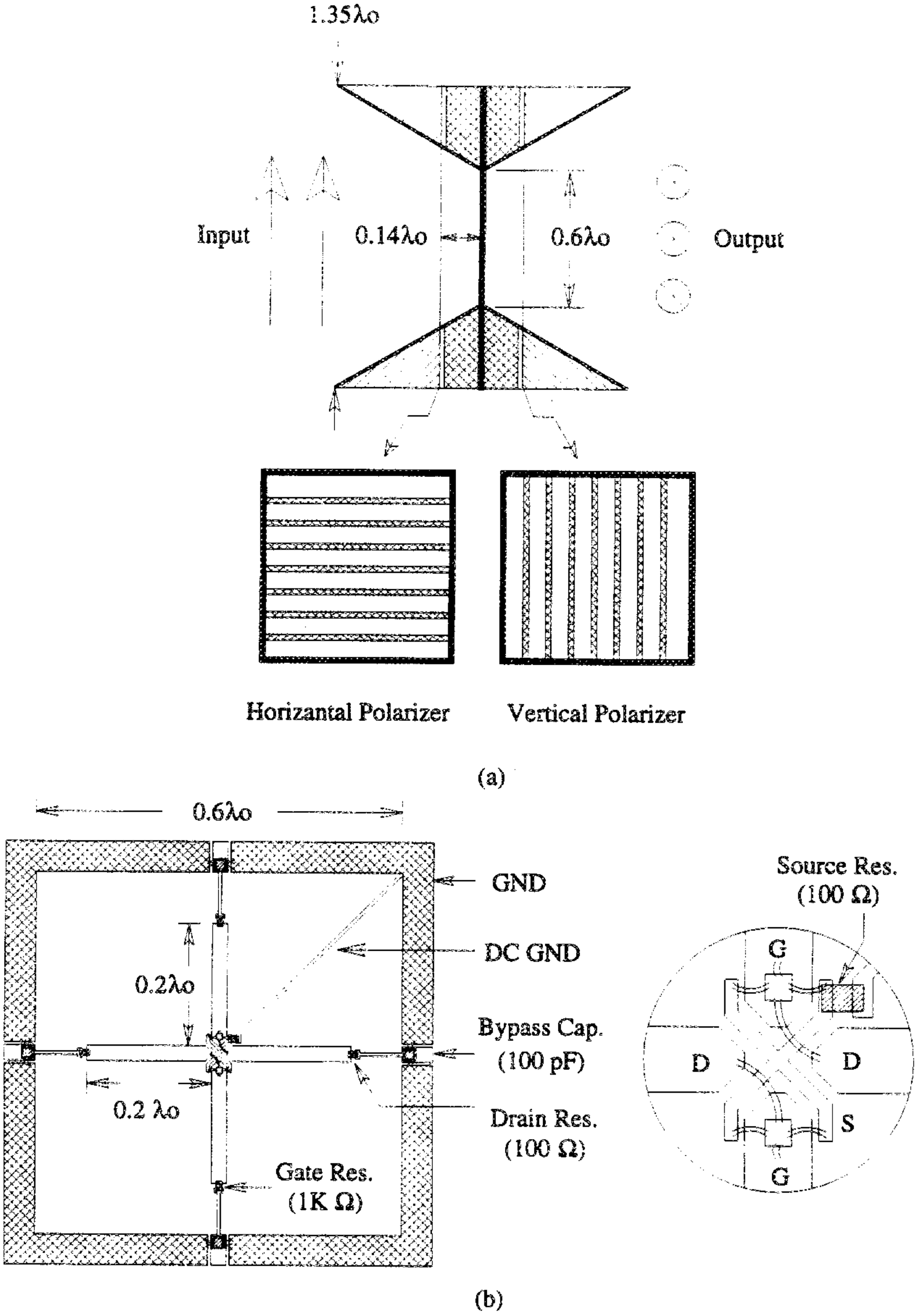
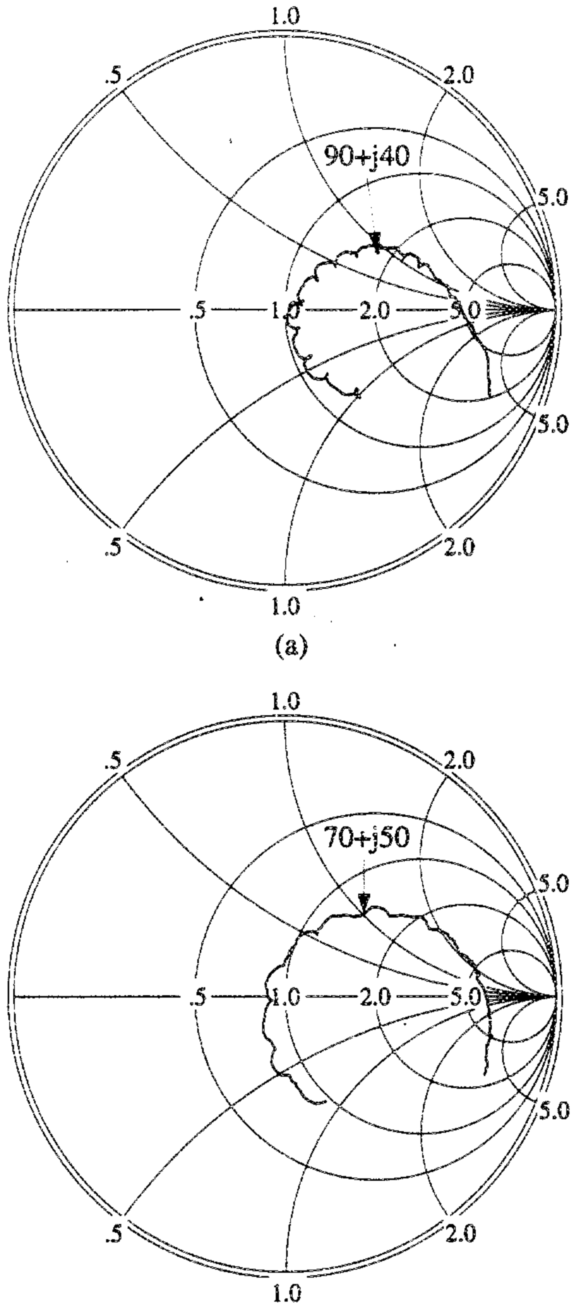


Figure A.2: Detailed side view (a) and front view (b) of the quasi-optical amplifier.



(a)

(b)

Figure A.3: Measured impedance for the (a) input dipole and (b) output dipole from 5 to 7 GHz.

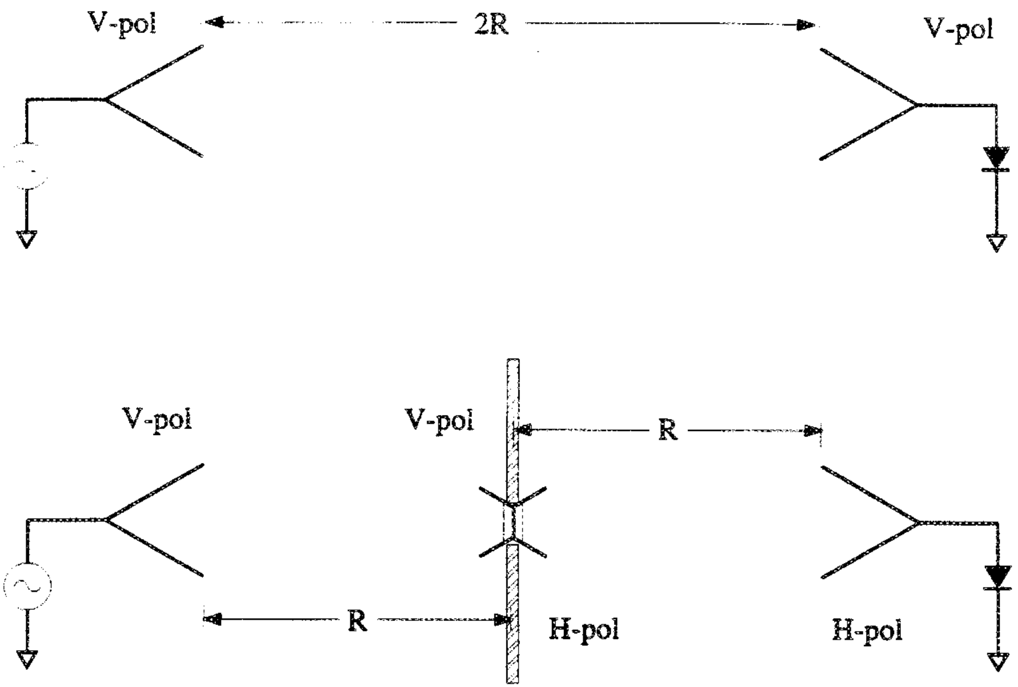


Figure A.4: The plane-wave measurement experiment.

A.3 Measurements

The quasi-optical amplifier was measured in a plane-wave test set-up shown in Fig. A.4. The amplifier gain, G, is defined by:

$$P_r = GP_t(G_tA_e/4\pi r^2)(G_rA_e/4\pi r^2) \tag{A.1}$$

where P_r and P_t are the received and transmitted powers and G_t and G_r are the corresponding gains of the transmitting and receiving standard gain horns. A_e is the effective area of the integrated horn structure [88] (estimated to be 75 ± 3% of the horn aperture) and r is the distance between the "device under test" and the transmitting (or receiving) horn. The plane-wave measurement system can be calibrated by making a measurement with the quasi-optical amplifier removed (see [83] for more detail). The first term in parentheses relates the power radiated by the transmitting horn to the power *available* at the terminals of the input dipole. The second term in parentheses relates the power *radiated* by the output dipole to the power received by the receiving horn. This expression is similar to the one used in [83] except that we use the effective area A_e and not the physical area of the quasi-optical amplifier. If the physical aperture A_{phy} is used instead of the effective aperture (A_e) of the antenna, the measured gain will drop by 2.5 dB.

As can be seen, the definition using A_e separates the amplifier gain from the input and output wave-coupling characteristics. This definition is also applicable to quasi-optical amplifiers employing wire antennas (such as dipoles, slot antennas, helical antennas,....) for coupling the input and output power. When operated as a Gaussian-beam amplifier, the physical area is of no importance and it is the Gaussian-beam coupling efficiency between the quasi-optical amplifier and the Gaussian-beam system that should be used.

Fig. A.5 shows the measured gain of the quasi-optical amplifier. In our experiment, the distance r is 250 cm insuring a good far-field condition. The amplifier oscillated at 18 MHz when the transistors were biased at the same conditions. We attribute this oscillation to having bonded two NEC 32100 chips with different DC characteristics and the large inductance on the drain due to the long bond wires used. This parasitic series inductance is estimated to be around 0.6-0.8 nH resulting in a series impedance around $j20\Omega$ to $j25\Omega$ at 6 GHz. The transistors were biased separately with I_{d1}= 8.7 mA, I_{d2}= 4.4 mA and resulted in maximum measured gain of 10.5 dB (Fig. A.5) and a 3-dB bandwidth of 80 MHz. The output power was checked on a 10 MHz to 26 GHz spectrum analyzer and showed no spurious oscillations. The amplifier is linear and is polarization dependent on the input channel.

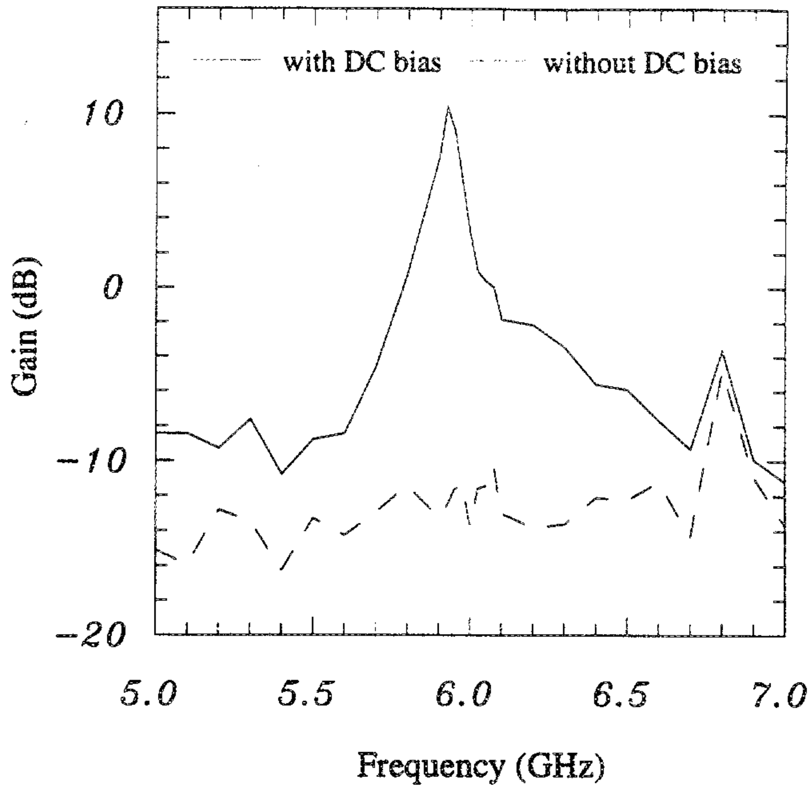


Figure A.5: Measured gain of the quasi-optical amplifier at 6 GHz.

The reverse gain is at least 20 dB lower than the forward gain at 5.9 GHz. The gain dropped to -20 dB when the input polarization was changed by 90°. Also, the polarization purity in the output port was better than 25 dB.

A.4 Conclusion

We reported a single-element quasi-optical amplifier that is based on an integrated antenna suitable for high-frequency applications. Every effort was made to render the unit compatible with standard mm-wave fabrication techniques. The dipoles and transistors can be easily integrated on a GaAs or silicon wafer (100μm thick at 94 GHz). Most important, the design is single-mode and therefore can be used in existing mm- wave systems as a low-noise amplifier stage before the RF mixer or as an amplifier stage in the transmitting circuit. Also, the unit can be suspended in a waveguide for the design of a millimeter-wave space-fed waveguide amplifier.

APPENDIX B

SYNTHESIS OF THE INTERDIGITATED FILTER

This appendix gives a complete listing of the program written to perform the synthesis of a membrane stripline interdigitated filter. This program is in a Fortran 77 code and can be run on an IBM compatible personal computer. This program is based on Matthaei's analysis [32, 47]. The required self- and coupling-capacitance for the interdigitated structure are first calculated. Then, the spacing batween the coupled strips are calculated using Cohn's equations [61] (see equation 4.10 and 4.11), and the width of each strip are calculated using Getsinger's equations [62] (see equation 4.14 and 4.15).

Input to the program is directly from the screen and the calculated results are stored under a file named " bp.out". An example of the input file is shown below:

```
Wideband or  Narrowband Design (W/N)?               ---  N
Input center frequency in GHz.                      ---  15
Input the fractional bandwidth.                     ---  0.05
Would you like to increase the fractional
bandwidth by 7 percent (y/n)?                       ---  Y
Input the pass band ripple in dB.                   ---  0.025
Input number of the resonator.                      ---  4
Input the distance between two ground plane (mil).  ---  28
Input the distance from the first finger to
the side-wall (mil).                                ---  28
Input the characteristic impedance (usually 50).    ---  50
Input the line impedance of the center resonator
(usually 70 ohm).                                   ---  70
```

```
      program inter
      real ckn(0:20),ckkn(0:20),g(0:20),f0,
     +     bw,lar,pi,z0,zint,theta,bb,s0,ckw(20),ckkw(20)
      integer nn
      character chr1
      open(unit=10,file='bp.out')

      pi=4*atan(1.0)

      call input(f0,bw,theta,lar,nn,bb,s0,z0,zint,chr1,pi)

      call cheby(lar,nn,g,pi)

      if (chr1 .eq. 'W' .or. chr1 .eq. 'w') then
      call wide(nn,g,theta,zint,z0,ckkw,ckw,pi)
      call dimensionw(bb,nn,ckkw,ckw,s0,pi)
      else
      call narrow(nn,g,theta,zint,z0,ckkn,ckn,pi)
      call dimensionn(bb,nn,ckkn,ckn,s0,pi)
      endif

      stop
      end

cccccccccccccccccccccccccccc

      function atanh(y)
      real y
      atanh=log((1+y)/(1-y))/2
      return
      end

cccccccccccccccccccccccccccccc

      subroutine input(f0,bw,theta,lar,nn,bb,s0,z0,zint,chr1,pi)
      real f0,bw,theta,lar,bb,s0,z0,zint,f1,f2,pi
      integer nn
      character chr1, chr2

 198  write(6,102)
 102  format(1x,'Wideband or Narrowband Design (W/N)?')
      read(5,114) chr1
      if (chr1 .eq. 'w' .or. chr1 .eq. 'W' .or. chr1 .eq. 'n' .or.
     +chr1 .eq. 'N') then
      go to 199
      else
      go to 198
      endif
```

```
199  write(6,100)
100  format(1x,'Input the center frequency in GHz.')
     read(5,*) f0
     write(10,101) f0
101  format(1x,'Center Frequency =',1x,f6.3,1x,'GHz')

     write(6,110)
110  format(1x,'Input the fractional bandwidth.')
     read(5,*) bw
     write(10,111) bw
111  format(1x,'Fractional Bandwidth =',1x,f5.3)
     f1=f0-f0*bw/2
     f2=f0+f0*bw/2
     write(10,112) f1,f2
112  format(1x,'Lower Frequency =',1x,f6.3,1x,'GHz',/,
    +       1x,'Upper Frequency =',1x,f6.3,1x,'GHz')

     write(6,113)
113  format(1x,'Would you like to increase the fractional',
    +          ' bandwidth by 7 percent (y/n)?')
     read(5,114) chr2
114  format(a1)
     if (chr2 .eq. 'y' .or. chr2 .eq. 'Y') then
     bw=bw*1.07
     endif

     theta=pi*(1-bw/2)/2

     write(6,120)
120  format(1x,'Input the pass band ripple in dB.')
     read(5,*) lar
     write(10,121) lar
121  format(1x,'Pass Band Ripple =',1x,f5.3,1x,'dB')

     write(6,130)
130  format(1x,'Input number of the resonator.')
     read(5,131) nn
131  format(i2)
     write(10,132) nn
132  format(1x,'Number of Resonator =',1x,i2)

     write(6,135)
135  format(1x,'Input the distance between two ground plane (mil).')
     read(5,*) bb
     write(10,136) bb
136  format(1x,'Distance B =',1x,f6.3,1x,'(mil)')

     write(6,137)
137  format(1x,'Input the distance from the first finger to',1x,
```

```
     +'the side-wall (mil).')
      read(5,*) s0
      write(10,138) s0
 138  format(1x,'Distance S0 =',1x,f6.3,1x,'(mil)')

      write(6,150)
 150  format(1x,'Input the characteristic impedance (usually 50).')
      read(5,*) z0
      write(10,151) z0
 151  format(1x,'Characteristic Impedance =',1x,f5.2,1x,'ohm')

      write(6,152)
 152  format(1x,'Input the line impedance of the center resonator',
     +           ' (usually 70 ohm).')
      read(5,*) zint
      write(10,153) zint
 153  format(1x,'Center line impedance =',1x,f6.2,1x,'ohm')
      return
      end

cccccccccccccccccccccccccccc

      subroutine cheby(lar,nn,g,pi)
      real beta,gama,lar,g(0:20),a(20),b(20),pi
      integer nn,k

      beta=log(1.0/tanh(lar/17.37))
      gama=sinh(beta/(2*nn))
      do 10 i=1,nn
      a(i)=sin((2*i-1)*pi/(2*nn))
      b(i)=gama**2+(sin(i*pi/nn))**2
 10   continue
      g(0)=1
      g(1)=2*a(1)/gama
      do 20 k=2,nn
      g(k)=4*a(k-1)*a(k)/(b(k-1)*g(k-1))
 20   continue
      k=nn/2
      if(nn-2*k .ne. 0) then
      g(nn+1)=1
      else
      g(nn+1)=1/(tanh(beta/4))**2
      endif
      do 30 i=0,nn+1
      write(10,140) i,g(i)
 140  format(1x,'G(',i2,') =',1x,f7.5)
 30   continue
      return
      end
```

```
cccccccccccccccccccccccccc

      subroutine narrow(nn,g,theta,zint,z0,ckkn,ckn,pi)
      real h,ya,zint,z0,theta,g(0:20),ckkn(0:20),ckn(0:20),j(0:20),
     +     n(0:20),m1,mn,pi
      integer k,nn

      do 30 k=0,20
      ckkn(k)=0
      ckn(k)=0
      j(k)=0
      n(k)=0
 30   continue


      k=nn/2
      if(nn-2*k .ne. 0) then
      k=(nn+1)/2
      endif

      h=z0/((1/sqrt(g(k)*g(k+1))+1/sqrt(g(k-1)*g(k))+
     +      sqrt(1/(g(k)*g(k+1))+(tan(theta))**2/4)+
     +      sqrt(1/(g(k-1)*g(k))+(tan(theta))**2/4))*zint)

      ya=1.0/z0
      j(0)=ya/sqrt(g(0)*g(1))
      do 40 k=1,nn-1
      j(k)=ya/sqrt(g(k)*g(k+1))
 40   continue
      j(nn)=ya/sqrt(g(nn)*g(nn+1))
      do 50 k=1,nn-1
      n(k)=sqrt((j(k)/ya)**2+(tan(theta))**2/4)
 50   continue
      m1=j(0)*sqrt(h)+ya
      mn=j(nn)*sqrt(h)+ya
      ckn(0)=376.7*(2*ya-m1)
      ckn(1)=376.7*(ya-m1+h*ya*(tan(theta)/2+(j(0)/ya)**2+n(1)
     +             -j(1)/ya))
      ckn(nn)=376.7*(ya-mn+h*ya*(tan(theta)/2+(j(nn)/ya)**2+n(nn-1)
     +             -j(nn-1)/ya))
      ckn(nn+1)=376.7*(2*ya-mn)
      do 60 k=2,nn-1
      ckn(k)=376.7*h*ya*(n(k-1)+n(k)-(j(k-1)/ya)-(j(k)/ya))
 60   continue
      ckkn(0)=376.7*(m1-ya)
      ckkn(nn)=376.7*(mn-ya)
      do 70 k=1,nn-1
      ckkn(k)=376.7*h*j(k)
```

```
 70   continue
      write(10,160) theta,h,m1,mn
 160  format(1x,'theta =',1x,f7.4,4x,'h =',1x,f8.5,/,
     +        1x,'m1 =',1x,f8.5,6x,'mn =',1x,f8.5)
      do 80 k=0,nn+1
      write(10,161) k,j(k)/ya,n(k),ckkn(k),ckn(k)
 161  format(1x,i2,2x,'j(k)=',2x,f8.5,3x,'n(k)=',2x,f8.5,3x,
     +                  'ckk(k)=',2x,f8.5,4x,'ck(k)=',2x,f8.5)
 80   continue
      write(10,162)
 162  format(1x,/,80('-'),/)
      return
      end

cccccccccccccccccccccccccccccccc

      subroutine wide(nn,g,theta,zint,z0,ckkw,ckw,pi)
      real h,ya,zint,z0,theta,g(0:20),ckkw(20),ckw(20),jya(20),
     +     n(20),z1za,yya(20),znza,temp,pi
      integer nn,k

      do 30 k=1,20
      ckkw(k)=0
      ckw(k)=0
      jya(k)=0
      n(k)=0
 30   continue

      ya=1.0/z0
      do 40 k=2,nn-3
      jya(k)=g(2)/(g(0)*sqrt(g(k)*g(k+1)))
 40   continue
      jya(nn-2)=sqrt(g(0)*g(2)/(g(nn-2)*g(nn+1)))/g(0)
      do 50 k=2,nn-2
      n(k)=sqrt(jya(k)**2+(tan(theta)*g(2)/(2*g(0)))**2)
 50   continue
      z1za=g(0)*g(1)*tan(theta)
      yya(2)=g(2)*tan(theta)/(2*g(0))+n(2)-jya(2)
      do 55 k=3,nn-2
      yya(k)=n(k-1)+n(k)-jya(k-1)-jya(k)
 55   continue
      yya(nn-1)=(2*g(0)*g(nn-1)-g(2)*g(nn+1))*tan(theta)/(2*g(0)*
     +          g(nn+1))+n(nn-2)-jya(nn-2)
      znza=g(nn)*g(nn+1)*tan(theta)
      k=nn/2
      if(nn-2*k .ne. 0) then
      k=(nn+1)/2
      endif
```

```
      temp=g(2)*tan(theta)/(2*g(0))

      h=z0/((sqrt(jya(k)**2+temp**2)+sqrt(jya(k-1)**2+temp**2)+
     +  jya(k-1)+jya(k))*zint)

      ckw(1)=376.7*ya*(1-sqrt(h))/z1za
      ckw(2)=376.7*ya*h*yya(2)-sqrt(h)*ckw(1)

      do 60 k=3,nn-2
      ckw(k)=376.7*ya*h*yya(k)
 60   continue

      ckw(nn)=376.7*ya*(1-sqrt(h))/znza
      ckw(nn-1)=376.7*ya*h*yya(nn-1)-sqrt(h)*ckw(nn)

      ckkw(1)=376.7*ya*sqrt(h)/z1za
      ckkw(nn-1)=376.7*ya*sqrt(h)/znza

      do 70 k=2,nn-2
      ckkw(k)=376.7*ya*h*jya(k)
 70   continue

      write(10,160) theta,h
 160  format(1x,'theta =',1x,f7.4,4x,'h =',1x,f8.5)

      do 80 k=1,nn
      write(10,161) k,jya(k),n(k),ckkw(k),ckw(k)
 161  format(1x,i2,2x,'j(k)=',2x,f8.5,3x,'n(k)=',2x,f8.5,3x,
     +                    'ckk(k)=',2x,f8.5,4x,'ck(k)=',2x,f8.5)
 80   continue
      write(10,162)
 162  format(1x,/,80('-'),/)
      return
      end

CCCCCCCCCCCCCCCCCCCCCCCCCCCCc

      subroutine dimensionw(bb,nn,ckkw,ckw,s0,pi)
      real bb,ckkw(20),ckw(20),s0,cf0,cfe(20),cfo(20),wd(20),sk(20),pi
      integer nn,k

      do 30 k=1,20
      wd(k)=0
      sk(k)=0
      cfe(k)=0
      cfo(k)=0
 30   continue

      cf0=2*log(1+tanh(s0*pi/(2*bb)))/pi
```

```
      do 90 k=1,nn-1
      sk(k)=2*bb*atanh(exp(-ckkw(k)*pi/2))/pi
      cfe(k)=2*log(1+tanh(sk(k)*pi/(2*bb)))/pi
      cfo(k)=2*log(1+1/tanh(sk(k)*pi/(2*bb)))/pi

 90   continue

      wd(1)=(ckw(1)/2-cf0-cfe(1))/2
      wd(nn)=(ckw(nn)/2-cf0-cfe(nn-1))/2

      do 95 k=2,nn-1
      wd(k)=(ckw(k)/2-cfe(k-1)-cfe(k))/2
 95   continue

      do 96 k=1,nn
      if(wd(k) .lt. 0.35) then
      wd(k)=(0.07+wd(k))/1.2
      endif
      wd(k)=wd(k)*bb
 96   continue
      do 98 k=1,nn
      write(10,162) k,wd(k),sk(k),cfe(k),cfo(k)
 162  format(1x,i2,1x,'wd(k)=',1x,f9.5,3x,'s(k)=',1x,f9.5,3x,
     +                'cfe(k)=',1x,f9.5,3x,'cfo(k)=',1x,f9.5)
 98   continue

      return
      end

ccccccccccccccccccccccccccccc

      subroutine dimensionn(bb,nn,ckkn,ckn,s0,pi)
      real bb,ckkn(0:20),ckn(0:20),s0,cf0,cfe(0:20),cfo(0:20),
     +     wd(0:20),sk(0:20),pi
      integer nn,k


      do 30 k=0,20
      wd(k)=0
      sk(k)=0
      cfe(k)=0
      cfo(k)=0
 30   continue

      cf0=2*log(1+tanh(s0*pi/(2*bb)))/pi
      do 90 k=0,nn
      sk(k)=2*bb*atanh(exp(-ckkn(k)*pi/2))/pi
      cfe(k)=2*log(1+tanh(sk(k)*pi/(2*bb)))/pi
      cfo(k)=2*log(1+1/tanh(sk(k)*pi/(2*bb)))/pi
```

```
90    continue
      wd(0)=(ckn(0)/2-cf0-cfe(0))/2
      wd(nn+1)=(ckn(nn+1)/2-cf0-cfe(nn))/2
      do 95 k=1,nn
      wd(k)=(ckn(k)/2-cfe(k-1)-cfe(k))/2
95    continue
      do 96 k=0,nn+1
      if(wd(k) .lt. 0.35) then
      wd(k)=(0.07+wd(k))/1.2
      endif
      wd(k)=wd(k)*bb
96    continue
      do 98 k=0,nn+1
      write(10,162) k,wd(k),sk(k),cfe(k),cfo(k)
162   format(1x,i2,1x,'wd(k)=',1x,f9.5,3x,'s(k)=',1x,f9.5,3x,
     +                'cfe(k)=',1x,f9.5,3x,'cfo(k)=',1x,f9.5)
98    continue
      return
      end
```

APPENDIX C

FABRICATION PROCEDURE OF MEMBRANE FILTERS

The fabrication procedure of the membrane suspended circuits mentioned in previous chapters is discussed here. The entire process can be divided into eight steps: (1) wafer cleaning; (2) alignment marks deposition; (3) front-side membrane etch; (4) front side patterning and metalization; (5) backside infrared alignment and membrane etch; (6) air-bridge formation; (7) wafer dicing; (8) EDP wafer etch. The detailed fabrication procedure in each step will be addressed in the text.

1. Wafer Cleaning:
    (a) 1 minute soak in trichloroethane (TCE). 1 minute soak in acetone (ACE). 1 minute soak in isopropyl alcohol (IPA).
    (b) Blow dry with N_2. Dehydrate bake for 2 minutes on a hot-plate at 130°C.
2. Alignment Marks Deposition:
    (a) Spin HMDS adhesion promoter and AZ 5214-E photoresist at 4.5 KRPM on the front (desired) membrane surface. This provides a photoresist thickness of approximately 1.2 μm.
    (b) Soft-bake 1 minute at 105°C on a hot-plate.

   (c) Align and expose the alignment marks pattern into the wafer using an MJB-3 mask aligner, at an ultraviolet light power density of 20 mW/cm^2 for 4.5 seconds. Total of eight alignment marks, two on each corner, will be transfered on the wafer and they will be used for future mask alignments (step 3(b) and step 4(b)). The mask used here is a clear-field photo mask, the eight alignment marks are the only dark areas in the mask.
   (d) Hard-bake 1 minute at 130°C on a hot-plate.
   (e) Flood expose the wafer on MJB-3 aligner at an ultraviolet light power density of 20 mW/cm^2 for 90 seconds.
   (f) Develop in AZ 327 developer for 40 seconds.
   (g) Rinse in de-ionized H_2O (DI water) then blow dry with N_2.
   (h) 80 W O_2 plasma de-scum for 36 seconds at 250 m Torr.
   (i) Deposit 500 Å thin film chrome (Cr) on the wafer as the alignment marks by using an e-beam evaporator. The reason of choosing Cr instead of Ti is that Cr cannot be attacked by buffered hydrofluoric acid (BHF), which will be used in step 3(f) and 3(n) later.
   (j) Lift off thin film Cr in ACE

3. Front-side Membrane Etch:
   (a) Spin HMDS adhesion promoter and S1400-37 photoresist at 3.5 KRPM on the front membrane surface. Soft-bake 30 minutes at 90°C in an oven.
   (b) Align a dark-field membrane etching mask on the front side of the wafer. The first alignment mark which has been deposited in step 2

will be used to help the alignment process here and the other alignment mark on each corner which is also deposited in step 2 will be protected by the photoresist and used for future pattern deposition alignment purposes (step 4(b)).

The reason for doing the front-side membrane layer etch is to etch a lot of small holes in the dielectric membrane layer where the opening of the via-holes are going to be located. Therefore, a real DC ground can be provided from the bottom of the wafer thru the via-hole to the front-side membrane in the via-hole process.

(c) Expose with UV light at 20 mW/cm^2 for 15 seconds.

(d) Develop the wafer in MF319 developer for 50 seconds. Rinse in DI water.

(e) Hard-bake 1 minute at 130°C on a hot-plate.

(f) BHF etch to remove the top silicon dioxide layer from the tri-layer membrane structure. At this step, the silicon dioxide at the backside of the wafer will also be etched away and the middle silicon nitride layer will be exposed after the etching process. After the BHF etch, rinse in DI water, then follow by ACE to remove the photo resist. 1 minute soak in IPA. Dry with N_2. Dehydrate bake for 2 minutes on a hot-plate at 130°C.

(g) Spin HMDS adhesion promoter and S1400-37 photoresist at 3.5 KRPM on the back side of the wafer. Soft-bake 30 minutes at 90°C in an oven. This step is to protect the backside silicon nitride layer from the CF_4 plasma nitride etch in step 3(j).

(h) Spin HMDS adhesion promoter and S1400-37 photoresist at 3.5 KRPM on the front side of the wafer. Soft-bake 30 minutes at 90°C in an oven.

(i) Use the same mask which used in step 3(b), and re-align. Expose with UV light at 20 mW/cm^2 for 15 seconds. Develop the wafer in MF319 developer for 50 seconds. Rinse in DI water. Hard-bake 1 minute at 130°C on a hot-plate.

(j) CF_4 plasma etch to remove the front-side silicon nitride for via-hole opening. In this step, the etching chamber is pumped down to 75 mTorr and CF_4 and O_2 are then flowed in at about 20 sccm and 0.5 sccm, respectively; the CF_4 flow rate is adjusted until the chamber pressure reaches 250 mTorr. After allowing the system pressure to stabilize, a 100 W RF plasma is ignited which will etch the nitride at a rate of approximately 700Å/minute.

(k) 1 minute soak in ACE to remove the photoresist from both side of the wafer. 1 minute soak in IPA. Dry with N_2. Dehydrate bake for 2 minutes on a hot-plate at 130°C.

(l) Spin HMDS adhesion promoter and S1400-37 photoresist at 3.5 KRPM on the front side of the wafer. Soft-bake 30 minutes at 90°C in an oven.

(m) Use the same mask which used in step 3(b), and re-align. Expose, then develop in MF319. Rinse in DI water. Hard-bake 1 minute at 130°C on a hot-plate.

(n) BHF etch to remove the last silicon dioxide layer for the front-side via-hole opening. At this step, the silicon nitride layer at the backside of the wafer can protect the silicon dioxide layer from the BHF etch. Rinse in DI water. Clean with ACE to remove the photoresist.

In this front-side membrane layer removal process for the via-holes, we use three separate processes to spin photoresist and perform the etch for the front side via-hole opening. The reason of doing this is to increase the yield rate of the fabrication. Because, if only one photoresist is spun and if there is a pin hole on the photoresist; after going through these three etching procedures, this membrane will be one hundred percent damaged. However, with three separate processes, the probability to have a pin hole which located at the same place is almost zero. Therefore, a higher yield rate can be achieved.

4. Front side Patterning and Metalization:
    (a) Spin HMDS adhesion promoter and AZ 5214-E photoresist at 4.5 KRPM on the front surface. Soft-bake 1 minute at 105°C on a hot-plate.
    (b) Align a clear-field pattern mask on the front side of the wafer. This mask contains all the front-side patterns that need to be transfered to the wafer. The second alignment mark which is deposited in step 2 will be used in this alignment process. Also two extra alignment marks which are in this pattern mask are transfered on the wafer during this step so they can be used for future backside infrared alignment and air-bridge formation. After the alignment, the wafer is exposed for 4.5 seconds at 20 mW/cm^2 UV light. Then bake for 1 minute on a 130°C hot-plate followed by 90 seconds flood expose at 20 mW/cm^2 UV light and the AZ 327 developing process.
    (c) A 500Å chrome (Cr) and 2000Å gold (Au) is evaporated on the surface. Then ACE lift off. At this time, those small holes opened for via-hole

formation in step 3 should be covered by a thin layer of metal. Later when the via-holes are etched from the backside of the wafer (step 8), the etching process will stop at the deposited Cr/Au metal layer.

(d) Electro-plate 3 ~ 5 μm of gold on the pattern. All the pattern that are going to be plated must have a DC path to conduct current. The gold plating solution used is a 6.87% Potassium Aurocyanide ($KAu(CN)_2$) solution and is made by Technic Inc. [89]. First, the solution is heated to around 55°C and a magnetic spinner is used to agitate the solution in order to achieve better uniformity during the plating. Then, the wafer is placed at the cathod in the plating solution and Platinum (Pt) is used at the anode. The plated DC current density need to be kept at low, otherwise a rough surface will be resulted.

5. Backside Infrared Alignment and Membrane Etch:

   (a) Spin HMDS adhesion promoter and S1400-37 photoresist at 3.5 KRPM on the front side of the wafer. Soft-bake 30 minutes at 90°C in an oven. This photoresist will be used to protect the front side of membrane from the CF_4 nitride and BHF dioxide etch in step 5(d) and 5(e), respectively.

   (b) Spin HMDS adhesion promoter and S1400-37 photoresist at 3.5 KRPM on the back side of the wafer. Soft-bake 30 minutes at 90°C in an oven.

   (c) Align a dark-field via-hole and membrane etching mask on the backside of wafer by the MJB-3 infrared aligner. This mask defines the area of the wafer and via-holes that are going to be etched away in step 8. At this time the third alignment mark which deposited in step 4 will be used for the infrared alignment. Expose UV light at 20 mW/cm^2

for 15 seconds. Develop the wafer in MF319 developer for 50 seconds. Rinse in DI water. Hard-bake 1 minute at 130°C on a hot-plate.

(d) CF_4 plasma etch to remove the backside silicon nitride for via-holes and membrane circuit opening.

(e) BHF etch to remove the backside silicon dioxide for via-holes and membrane circuit opening. Rinse with DI water. Dry with N_2. Use ACE to remove photoresist from both sides. Soak in IPA for 1 minute. Dry with N_2. Dehydrate bake for 2 minutes on a hot-plate at 130°C.

6. Air-bridge Formation:

   (a) Spin HMDS adhesion promoter and S1400-37 photoresist at 3.5 KRPM on the back side of the wafer for protection. Soft-bake 1 minute at 105°C on a hot-plate.

   (b) Spin HMDS adhesion promoter and S1400-37 photoresist at 3.5 KRPM on the front side of the wafer. Soft-bake 1 minute at 105°C on a hot-plate.

   (c) Align a dark-field air-bridge pedestal mask on the front side of the wafer. This mask defines the pedestals of air-bridges. The forth alignment mark which deposited in step 4 will be used in this alignment process. Expose with UV light at 20 mW/cm^2 for 15 seconds. Develop the wafer in MF319 developer for 50 seconds. Rinse in DI water. Hot-plate conformal bake 1 minute at 130°C.

   (d) Evaporate a Ti/Au/Ti (300/1200/200 Å) seed layer for the electroplating process (step 6(h)).

   (e) Spin S1400-37 photoresist at 3.5 KRPM on the front side of the wafer. Soft-bake 20 minutes at 80°C in an oven. *Notice, no HMDS is used* *in this step and also this photoresist must be baked in an oven.* The reason of using oven instead of using hot-plate is to avoid the thermal stress which can cause cracking on the evaporated seed layer.

(f) Align a dark-field air-bridge mask on the front side of the wafer. This mask defines the bridges. Again, the forth alignment mark which deposited in step 4 is used in this alignment process. Expose with UV light at 20 mW/cm^2 for 15 seconds. Develop the wafer in MF319 developer for 50 seconds. Rinse in DI water.

(g) Etch the top Ti layer (200Å) underneath the bridges opening using BHF or a 1:15 $HF{:}H_2O$ solution. This etching process lasts only a couple of seconds. Bubbles can be found during the etch. Rinse in DI water. Blow dry with N_2.

(h) Electro-plate the air-bridges.

(i) Flood expose the wafer for 30 seconds. Put the wafer into MF319 developer to develop out the top layer photoresist. Rinse with DI water. Dry with N_2.

(j) Use the same solution in step 6(g) to etch away the entire top layer Ti. Rinse in DI water. Dry with N_2.

(k) Put the wafer into a gold etching solution to remove the 1200Å evaporated gold. Rinse in DI water. Blow dry with N_2.

(l) Use the same solution in step 6(g) to remove the bottom Ti (300Å) layer. Rinse in DI water. Blow dry with N_2.

(m) Clean with ACE to remove the bottom layer photoresist spun in step 6(b).

7. Wafer Dicing:

   (a) Spin HMDS adhesion promoter and S1400-37 photoresist at 3.5 KRPM on front side of the wafer. Soft-bake 30 minutes at 90°C in an oven. The purpose of this process is to protect the air-bridges during the dicing.

   (b) Dice wafers.

8. EDP Wafer Etch:

   (a) Put the wafer into the EDP solution. The EDP solution is made by 48 mL of de-ionized H_2O, 48 gm of catechol, 0.9 gm of pyrazine, and 150 mL of ethylenediamine. (Different quantities of the solution can be mixed by proportionally adjusting the amount of each substance.) This solution is heated to 110°C then wafers are put into the EDP solution. The etch rate is around $1\mu m$/minute. For a $350\mu m$ thick wafer, it usually takes about six hours to etch through it.

   (b) After the EDP etch, the wafers are put into DI water to dilute the EDP residue. The wafers are then put into a methanol solution overnight to completely remove any EDP residues.

APPENDIX D

SYNTHESIS OF LANGE-COUPLERS

This appendix gives a complete listing of the program written to perform the synthesis of a membrane stripline Lange coupler. This program is in a Fortran 77 code and can be run on an IBM compatible personal computer. This program is based on Ou's design equations [71] (see equation 5.1 and 5.2).

Input to the program is directly from the screen and the calculated results are stored under a file named "coupler.out". An example of the input file is shown below:

```
Input the effective dielectric constant.              ---  2.0
Input the distance between the two ground
plane (in mil).                                       ---  28
Input the number of fingers.                          ---  4
Input coupling coefficient C in dB.                   ---  3.0
```

```
      program coupler
      real ca,cab,er,yoo,yoe,y0,j11,j12,j21,j22,v,effer,
     +b,wk,sk,cabfe,cabfo,pi,y1,y2,det,tol,f1,f2,nca,ncab
      integer k,n,m
      character chr*1

      open(unit=10, file='coupler.out')

      pi=4*atan(1.0)
      v=3.0e10
      er=8.85418e-14
      y0=1.0/50
      tol=1e-5

5     write(6,104)
104   format('Input the effective dielectric constant')
      read(5,*) effer
      write(6,105)
105   format(1x,'Input the distance between the two ground plane (in mil)')
      read(5,*) b
      write(10,106) b
106   format(1x,'ground plane distance b =',1x,f4.1,1x,'mils')

10    write(6,100)
100   format(1x,'Input the number of fingers')
      read(5,110) k
110   format(i1)

      n=k/2
      if (k-2*n .ne. 0) then
      write(6,120)
120   format(1x,'It need to be an even number. Try again!')
      go to 10
      endif
      write(10,125) k
125   format(1x,'number of lines k =',1x,i1)

      write(6,130)
130   format(1x,'Input coupling coefficient C in dB')
      read(5,*) c

      if (c .lt. 0) then
      c=-1*c
      endif
      write(10,135) c
135   format(1x,'coupling ratio C =',1x,f6.3,1x,'dB',/)

      c=10**(-1*c/10.0)
```

```
      yoo=0.5
      yoe=0.5
      n=20
      m=0


 20   call function1 (y0,yoo,yoe,k,f1)
      call function2 (yoo,yoe,k,c,f2)

      call jocobian11 (y0,yoo,yoe,k,j11)
      call jocobian12 (y0,yoo,yoe,k,j12)
      call jocobian21 (yoo,yoe,k,c,j21)
      call jocobian22 (yoo,yoe,k,c,j22)

      det=j22*j11-j12*j21
      y1=(f2*j12-f1*j22)/det
      y2=(f1*j21-f2*j11)/det

      yoo=yoo+y1
      yoe=yoe+y2
      m=m+1

      if(sqrt(y1**2+y2**2) .lt. tol) then
      go to 30
      endif

      if(m .gt. n) then
      go to 200
      endif
      go to 20

 30   write(6,140) yoo,yoe
      write(10,140) yoo,yoe
 140  format(1x,'yoo =',1x,f7.5,2x,'yoe =',1x,f7.5,/)

      call findc (yoo,yoe,v,ca,cab,er,effer,nca,ncab)
      write(6,150) nca,ncab
      write(10,150) nca,ncab

 150  format(1x,'normalized self capacitance ca =',1x,f7.5,/,
     +1x,'normalized matual coupling capacitance cab =',1x,f7.5,/)

      call findws(nca,ncab,wk,sk,b,cabfe,cabfo,pi)

      write(6,160) wk,sk,cabfe,cabfo
      write(10,160)  wk,sk,cabfe,cabfo
 160  format(1x,'line width wk =',1x,f7.3,1x,'mil',/,
     +1x,'gap between lines Sk =',1x,f7.3,1x,'mil',/,
```

```
     +1x,'cabfe =',1x,f7.5,/,1x,'cabfo =',1x,f7.5,/)
      go to 210
200   write(6,170)
      write(10,170)
170   format(1x,'no solution')
      go to 210
210   write(6,180)
180   format(ix,'Do you need another run? (y/n)')
      read(5,190) chr
190   format(a1)
      if (chr .eq. 'y' .or. chr .eq. 'Y') then
      write(6,300)
      write(10,300)
300   format(/,80('-'),/)
      go to 5
      endif
      stop
      end



      subroutine function1(y0,yoo,yoe,k,f1)
      real y0,yoo,yoe,f1
      integer k
      f1=((k-1)*yoo**2+yoo*yoe)*((k-1)*yoe**2+yoo*yoe)
     +-y0**2*(yoo+yoe)**2
      return
      end

      subroutine function2(yoo,yoe,k,c,f2)
      real yoo,yoe,c,f2
      integer k
      f2=(k-1)*yoo**2-(k-1)*yoe**2-sqrt(c)*((k-1)*yoo**2
     ++2*yoo*yoe+(k-1)*yoe**2)
      return
      end

      subroutine jocobian11 (y0,yoo,yoe,k,j11)
      real y0,yoo,yoe,j11
      integer k
      j11=(2*(k-1)*yoo+yoe)*((k-1)*yoe**2+yoo*yoe)
     ++yoe*((k-1)*yoo**2+yoo*yoe)-2*y0**2*(yoo+yoe)
      return
      end

      subroutine jocobian12 (y0,yoo,yoe,k,j12)
      real y0,yoo,yoe,j12
      integer k
```

```
      j12=(2*(k-1)*yoe+yoo)*((k-1)*yoo**2+yoo*yoe)
     ++yoo*((k-1)*yoe**2+yoo*yoe)-2*y0**2*(yoo+yoe)
      return
      end

      subroutine jocobian21 (yoo,yoe,k,c,j21)
      real yoo,yoe,c,j21
      integer k
      j21=2*(k-1)*yoo-sqrt(c)*(2*(k-1)*yoo+2*yoe)
      return
      end

      subroutine jocobian22 (yoo,yoe,k,c,j22)
      real yoo,yoe,c,j22
      integer k
      j22=-2*(k-1)*yoe-sqrt(c)*(2*(k-1)*yoe+2*yoo)
      return
      end

      subroutine findc(yoo,yoe,v,ca,cab,er,effer,nca,ncab)
      real yoo,yoe,v,ca,cab,er,effer,nca,ncab
      ca=377*yoe*er*sqrt(effer)
      cab=377*er*sqrt(effer)*(yoo-yoe)/2
      nca=ca/(er*effer)
      ncab=cab/(er*effer)
      return
      end

      subroutine findws(nca,ncab,wk,sk,b,cabfe,cabfo,pi)
      real nca,ncab,wk,sk,b,cabfe,cabfo,pi
      sk=2*b/pi*atanh(exp(-pi*ncab/2))
      cabfe=2*log(1+tanh(sk*pi/(2*b)))/pi
      cabfo=2*log(1+1/tanh(sk*pi/(2*b)))/pi
      wk=(nca/2-2*cabfe)*b/2
      if(wk/b .lt. 0.35) then
      wk=(0.07*b+wk)/1.2
      endif
      return
      end

      function atanh(y)
      real y
      atanh=log((1+y)/(1-y))/2
      return
      end
```

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