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ELECTROMAGNETIC MODELING OF HIGH-SPEED HIGH-FREQUENCY INTERCONNECTS

by

Jong-Gwan Yook

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
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Doctoral Committee:

Professor Linda P. B. Katehi, Chair
Adjunct Associate Professor Hal G Marshall
Professor Karem Sakallah
Assistant Professor Kamal Sarabandi
Rainee Simons, Senior Engineer, NASA

This thesis is dedicated to my parents
in memory of their devotion and selfless love

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ABSTRACT

ELECTROMAGNETIC MODELING OF HIGH-SPEED HIGH-FREQUENCY INTERCONNECTS

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Chair: Linda P. B. Katehi

This dissertation develops in detail an approach to a three-dimensional full-wave electromagnetic field simulator, namely the finite element method (FEM), and applies it to various high-speed high-frequency interconnects, ranging from a simple via hole to an entire K/Ka-band MMIC phase shifter package. This approach has several essential features: the utilization of tetrahedron-based edge basis functions rendering spurious-free solutions, a non-uniform structured mesh generator giving flexible modeling capabilities, and implementation of artificial absorbing layers helping to simulate open boundary problems. In addition, the FEM is fully parallelized on a distributed memory machine (the IBM SP2). Two different parallelization strategies are implemented, among which the task parallelization strategy provides linearly scalable performance improvement due to the minimal communication overhead among the processors.

With all the above features, the parallelized FEM has been successfully applied to the characterization of planar/non-planar high frequency interconnects, hermetic transitions, and K/Ka-band MMIC packages. In particular, the undesirable internal package resonances and energy leakages in the MMIC package are identified, and furthermore, a few mechanisms for the suppression of the above phenomena are suggested, and these are supported by rigorous numerical data. The lumped equivalent circuits for the vertical via holes are utilized in the system level EM modeling to provide appropriate inductances and capacitances. In this dissertation, characterization of various high-frequency interconnects has been stressed as well as parametric study.

Special attention is devoted to development of the system level electromagnetic modeling for high-speed digital circuits and packages. This system level modeling is achieved by combining the FEM and the well known circuit simulator, HSPICE. It is based on the so-called tiling processor, which generates equivalent circuits for PCBs and ICs, and then the circuit simulator is employed for time or frequency domain characterizations. The hybrid approach implemented in this study renders effective simulations in frequency as well as time domain for a given geometry. The detailed derivation and applications of the system level electromagnetic modeling tool are described. Its validity and accuracy are proved by modeling the INTEL P6 board and package containing eight layers of signal, power, and ground planes and hundreds of signal traces.

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CHAPTER I

INTRODUCTION

1.1 Motivation and Background

In the recent advancement of satellite, mobile and personal communication systems, military and commercial radar systems, remote sensing technologies, and numerous other areas, high-speed high-frequency MMICs (monolithic microwave integrated circuits) play an essential role in terms of small volume, low weight, low power consumption, and low cost. In spite of these advantages of using MMICs, their design and optimization are not an easy task due to their complexity and sophisticated functionalities, especially as the operating frequency increases up to the X-band. In many cases, both the microwave and millimeter-wave subsystem with MMICs chips and the overall system are very complex and interrelated, and the functions of the circuits and interconnects are very sensitive to their mechanical and electrical environment. Depending on the system, there exist many different interconnection structures, ranging from simple through lines to whole packages, which need to be characterized and fully understood. Furthermore, the advent of high-speed computers and their subsidiary systems require high-speed operations reaching Gigabits per second switching times and data transfer, and the resulting electromagnetic interference and spurious radiation arising from the circuit discontinuities, in many cases,

cause serious malfunction of the system if not carefully designed.

For these reasons, the successful development of efficient design and analysis tools has been an essential step toward advances in these technologies. For low frequency lumped electric circuits and solid state devices, there are numerous circuit simulators providing accurate time domain characterization of digital and analog circuits. Similarly, design and optimization software is also available for canonical planar circuits in the microwave frequency region. Existing electric circuit simulators and microwave circuit design tools, however, have their own limitations, including lack of modeling capability for electromagnetic interactions between closely or sometimes remotely placed circuit components. In the case of microwave and millimeter-wave circuit design and characterization tools, in particular, when there are material inhomogeneities and three-dimensional structural discontinuities, the limitations of those tools become apparent.

Recently, to overcome the shortcomings of the available simulation tools a number of full-wave analysis methods have been developed based on the integral representation of Maxwell's equations [1] or on partial differential operators [2, 3, 4]. The method of moment (MoM) and mode matching techniques are examples of the former approach, while the finite element method (FEM) and the finite difference time domain (FDTD) method are most frequently encountered as examples of the latter approach.

The aforementioned full-wave techniques are considered to provide complete solutions to complicated structures by solving Maxwell's equations rigorously under proper boundary conditions. The MoM, in general, provides accurate and efficient solutions, and, thus, is recommended for use whenever applicable. In practical applications, however, the MoM is mainly employed for planar two-dimensional and fairly

simple three-dimensional circuit characterizations due to the difficulties in obtaining relevant Green's functions for non-canonical geometries.

In contrast to the MoM, the partial differential equation (PDE) techniques, such as the FEM and FDTD methods, do not require the knowledge of Green's functions for a given problem, thus providing flexible modeling capability regardless of two and three-dimensional discontinuities. In principle, the FEM and FDTD methods are similar to the MoM in terms of using basis functions on discretization space and performing weighting operations. In the FDTD method [5, 6], however, the pulse functions are used in both the basis and weighting function spaces, and as a result the FDTD method requires discretization of the whole three-dimensional space with a dense sampling rate (at least 15 samples/λ_g) due to its simple basis and weighting functions. On the other hand, FEM employs similar discretization and weighting operations to find weak solutions of Maxwell's equations, except for the fact that any arbitrary functions of higher order can be used as basis and weighting functions [2, 3, 7]. With higher order basis and weighting functions, the same accuracy can be achieved with less discretization, because of their modeling efficiency for highly varying electromagnetic fields.

Another important feature of the FEM is the usage of non-uniform discretizations for adaptive modeling of rapidly changing local electromagnetic field distributions, thus allowing optimum mesh or sub-domain sizes. The meshing flexibility of the FEM also contributes to reduced overall problem size and faster solution time, and poses clear advantages over the regular FDTD method. In addition, recent developments in high-speed parallel computing facilities including shared and distributed memory machines have an impact on practical application and real time computation of numerical techniques.

In view of the above discussion, the frequency domain finite element method is developed and parallelized in this study for the characterization of arbitrary-shaped three-dimensional high-speed, high-frequency interconnects. In the following, the objectives of the study and the overview of this thesis will be described in detail.

1.2 Objectives

The goal of the present dissertation has been to develop and apply an accurate and fast modeling method for the characterization of high-speed, high-frequency circuits and interconnects, and to explore the three-dimensional finite element method using two fundamental features, tetrahedral sub-domain elements and their corresponding edge-based vector basis functions. While the conventional node-based finite element method has been plagued by spurious modes and requires special treatment to obtain physically correct solutions [8]-[12], the edge-based finite element method provides spurious-free solutions by enforcing correct boundary conditions at the material interface and sharp metal discontinuities [13]-[19], making the approach attractive. As a result, the edge-based finite element solution scheme has been developed to provide reliable solutions for very complicated structures without using any further post-processing or sorting of the solution.

Furthermore, to overcome the difficulties in applying time-consuming full-wave techniques to the real-time characterization of a given circuit or interconnect, the development of efficient parallelization strategies is desirable. Therefore, the frequency domain FEM has been parallelized on distributed memory parallel computers, such as the IBM SP2, using the message passing paradigm [20]. The linear scalability of the FEM code is rooted in the frequency independent nature of the method, which requires minimal inter-processor communication overhead. The parallelized FEM

can provide near-real-time characterization of a given circuit and in turn opens the door to the use of the full-wave techniques for circuit design, as well as tools for optimization.

This developed tool has been applied for the characterization of various high-speed high-frequency interconnects and the theoretical results have been compared with measurements or other theoretical techniques whenever possible for validation. Accurate characterizations of the aforementioned individual interconnects are of critical importance for successful design of more complicated circuits. Furthermore, to tackle open boundary problems often encountered in real situations, design equations for isotropic absorbing layers have also been sought, and their validity and effects have been fully tested under several different circumstances.

The characterization of high-speed digital circuits and packages in the frequency as well as the time domain is an important but difficult task, especially with full-wave techniques, due to their heavy computational burdens. To overcome this limitation, a hybrid approach has been explored in this study which combines the frequency domain full-wave FEM and time domain circuit simulator, HSPICE [21]-[25]. In this approach, various digital ICs and packages are discretized into a number of smaller pieces, called tiles, and for each tile an equivalent circuit is derived using FEM and a simpler microwave network theory. After all the equivalent circuit extraction procedures have been completed, time domain circuit simulations are performed to model the whole structure, and develop noise maps and time domain potential fluctuations plots. The information obtained from the system level modeling is essential for diagnosis of simultaneous switching noise (SSN) and for effective suppression of the noise arising from the high-speed digital circuits.

1.3 Overview

This thesis is focused on the development of a rigorous theoretical technique, namely the FEM, for the characterization of three-dimensional high-speed high-frequency interconnects and its applications to various geometries. Each geometry has its own unique characteristics and complexities which have prevented them from being fully characterized with conventional approach.

In Chapter 2, the theoretical framework of the three-dimensional finite element method is briefly summarized. Unlike the conventional approach to FEM theory, the Hilbert space representation of the method is adopted starting from the weak form of the wave equations. Since appropriate boundary conditions should be specified to obtain a unique solution of the wave equations, the most fundamental boundary and interface conditions often encountered in the practical problems are described. Furthermore, in view of the importance of using the edge basis functions, as described in the previous section, for obtaining spurious-free solutions, the rationale of using the Whitney edge basis functions is fully discussed. In addition, excitation mechanisms in the FEM system and customized tetrahedral mesh generation schemes are presented. For the simulation of unbounded problems which are in many cases unavoidable, isotropic lossy materials are utilized to simulate the open boundary conditions. The last part of this chapter contains the theoretical background of the idea of incorporating passive lumped elements into the FEM framework. Even though an extensive study of this method is not presented in this dissertation, a preliminary study shows its effectiveness and accuracy.

In Chapter 3, several different eigenvalue problems are tackled to validate the developed FEM and to assess its accuracy. For a rectangular cavity having lossy

dielectric material, the linear system of equations incorporating an excitation mechanism is solved, and the resonant frequency and the quality factor are computed. From the above information, the real and imaginary parts of the dielectric material can be extracted easily. After the FEM is validated, it is also parallelized on a distributed memory parallel computer (the IBM SP2) and two different parallelization strategies are examined. With the "task parallelization" strategy, in particular, almost linearly scalable performance improvement has been obtained, which is quite remarkable. Furthermore, the design concept of the artificial absorbers proposed in Chapter 2 is examined through several different circuit configurations supporting quasi-TEM as well as non-TEM waves.

Starting from Chapter 4, applications of the developed FEM to various practical high-speed, high-frequency interconnects are presented. In Chapter 4, eight different types of basic building blocks of the MMICs are characterized [26, 27, 28] and in some cases the equivalent circuits are obtained [29, 30]. In particular, the equivalent circuits for via hole geometries are used in Chapter 7 to provide appropriate equivalent circuits for the power and ground pin tiles.

In Chapter 5, the performance of intra- and inter-chip hermetic transition structures are fully characterized to provide design guidelines to MMIC designers [31, 32]. Specifically, the microstrip-through-CPW configuration is employed for an intra-chip transition, while hermetic bead structure is utilized for inter-chip transition. The effect of various grounding via holes, cavity size, and the shape of the hermetic beads are carefully examined.

In Chapter 6, the K/Ka-band (18 to 40 GHz) MMIC package fabricated for a phase shifter is characterized and the effects of the structural symmetry/asymmetry, bonding wires, gaps, side walls formed by 12 via holes, and the DC bias lines are

also studied [33, 34]. Furthermore, the spurious package resonances are identified and several techniques for suppressing them are suggested with rigorous numerical data. To the best of the author's knowledge this is the first comprehensive study of RF energy leakage and internal resonances in a practical millimeter-wave package.

In Chapter 7, the detailed procedure for the system level electromagnetic modeling of high-speed digital ICs and packages is presented. In the tiling procedure, three types of primitive tiles are identified and their equivalent circuits are devised, including power/ground plane tile, power/signal/ground plane tile, and power/ground pin tile. Upon building the equivalent circuit library, several different printed circuit boards and source configurations are studied along with an Intel test circuit for validation of the proposed approach. The simulation and measurement results show very good agreement. Considering that there are 8 layers in the PCB and hundreds of vertical pins and traces, the remarkably good comparison between the measurement and the simulation proves the accuracy and effectiveness of the proposed hybrid approach.

Finally, in Chapter 8, a brief summary of the achievements and original contributions of the present research are presented. Also, concluding remarks and directions for future studies are provided for later study.

CHAPTER II

THEORETICAL METHODOLOGY: 3D VECTOR FINITE ELEMENT METHOD

2.1 Introduction

The finite element method (FEM) has been extensively applied to scattering, radiation and propagation problems [35]-[40]. Recently, it has found application to circuit problems as well and has led to successful treatment of microwave and millimeter wave circuits with complex geometrical shapes and inhomogeneous material combinations [33]-[30]. In this chapter, the basic principles and general procedures of the three-dimensional (3D) vector finite element method are presented starting from Maxwell's equations and subsequent vector wave equations. The 3D vector FEM is based on the discretization of the weak form of the wave equation in frequency domain, and provides accurate full wave solutions to the most general electromagnetic problems.

In this study, even though both electric and magnetic field formulations are given for the sake of completeness, only the electric field formulation is implemented for several practical reasons, such as ease of application of boundary conditions and reduction of overall problem size. The current formulation presented is valid for geometries having isotropic dielectric materials whether lossy, lossless or a combination and perfect conductors. However, it can be easily extended to incorporate anisotropic

materials and lossy conducting surfaces. The FEM developed in the study is capable of handling closed as well as open boundary problems. In the following sections, the essential formulation of the finite element method and its discretization procedure will be discussed in detail.

2.2 Vector Wave Equation

Consider an arbitrary shaped three dimensional geometry which contains material inhomogeneities and geometrical discontinuities, as shown in Figure 2.1. The electromagnetic fields in the domain Ω are characterized by Maxwell's equations

$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t} - \mathbf{M}_i \tag{2.1}$$

$$\nabla \times \mathbf{H} = \frac{\partial \mathbf{D}}{\partial t} + \mathbf{J}_i \tag{2.2}$$

$$\nabla \cdot \mathbf{D} = \rho_e \tag{2.3}$$

$$\nabla \cdot \mathbf{B} = \rho_m \tag{2.4}$$

and the appropriate constitutive relations

$$\mathbf{D} = \epsilon \mathbf{E} \tag{2.5}$$

$$\mathbf{B} = \mu \mathbf{H} \tag{2.6}$$

where $\mathbf{E}$ and $\mathbf{H}$ are electric and magnetic field intensity in [Volt/m] and [Amp/m], respectively and similarly, $\mathbf{D}$ and $\mathbf{B}$ represent electric and magnetic flux density in [Coul/m^2] and [Weber/m^2], and the sources and material parameters are defined as:

$\mathbf{J}_i$: impressed electric current in [Amp/m^2]

$\mathbf{M}_i$: impressed magnetic current in [Volt/m^2]

ρ_e : electric charge density in [Coul/m^3]

ρ_m : magnetic charge density in [Weber/m^3]

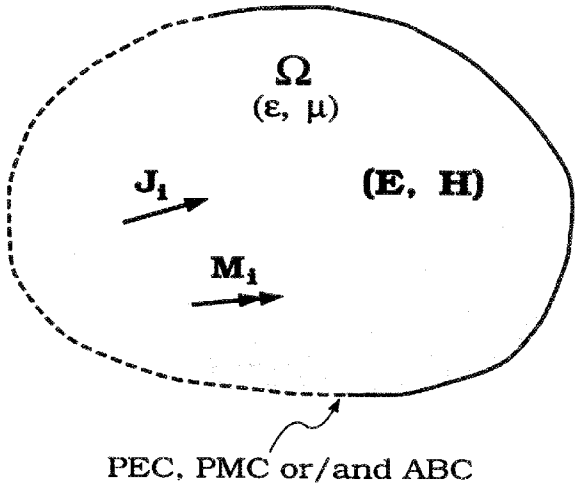


Figure 2.1: Geometry of three dimensional volume which has current sources $\mathbf{J}_i$ and/or $\mathbf{M}_i$ with possible material inhomogeneities and geometrical discontinuities. The boundary of the volume V is closed by some combination of PEC, PMC, and ABC.

$$\epsilon = \epsilon_o \epsilon_r \quad : \quad \text{permittivity in [F/m]}$$

$$\mu = \mu_o \mu_r \quad : \quad \text{permeability in [H/m]}$$

Without loss of generality, it is assumed that fields have time harmonic variations (e^{jwt}) and the impressed sources are not present in the computational domain. Then the source-free vector wave equations can be derived from Maxwell's equations :

$$\nabla \times \begin{bmatrix} \mu_r^{-1}(\nabla \times \mathbf{E}) \\ \epsilon_r^{-1}(\nabla \times \mathbf{H}) \end{bmatrix} - k_0^2 \begin{bmatrix} \epsilon_r \mathbf{E} \\ \mu_r \mathbf{H} \end{bmatrix} = 0 \tag{2.7}$$

where k_o ($= \omega\sqrt{\mu_o \epsilon_o}$) is the wave number in the medium. Later sections will address the fact that the circuits can be excited by using the surface integral term which is equivalent to the impressed sources.

For a numerical solution of the electromagnetic fields in a given domain, the wave equations, which are second order partial differential equations, need to be solved with appropriate boundary conditions for a unique solution. However, since finding

a strong solution of the wave equations is not always possible, weak solutions will be sought in this study with appropriate weighting and testing operations.

Among the two equivalent formulations, **E**- and **H**-field formulation, the **E**-field formulation will be presented and tackled. As mentioned before, the **E**-field formulation has clear advantages over the **H**-field formulation when there are many perfect electrically conducting (PEC) surfaces or bodies. Moreover, with the **E**-field formulation, the implementation of the boundary condition for a perfect magnetically conducting surface, which is the natural boundary condition, is also straightforward and will be discussed in the next section.

2.3 Weak Form of Wave Equation and Its Discretization

As a first step towards finding the finite element solution, a given solution space Ω is subdivided into number of smaller sub-domains Ω_e, and in each Ω_e the electric field is expressed as a linear combination of basis functions $\mathbf{P} = \{\mathbf{P}_1, \mathbf{P}_2, \ldots, \mathbf{P}_m\}^T \subset \mathcal{H}_1$, a Hilbert space, [1] as follows;

$$\mathbf{E} = \sum_{i=1}^{m} x_i \mathbf{P}_i \tag{2.8}$$

where $\mathbf{x} = \{x_1, x_2, \ldots, x_m\} \subset C^m$, m-vectors of complex coefficients, is the unknown coefficient vector to be determined. Note that due to the nature of approximation of the discretization procedure, the original problem is modified to become a new problem which has a different solution space [43]. After substituting Eq. (2.8) into

[1] Let $(\mathcal{H}, (\cdot,\cdot))$ be an inner-product space. If the associated normed linear space $(\mathcal{H}, \|\cdot\|)$ is complete, then $(\mathcal{H}, (\cdot,\cdot))$ is called a **Hilbert space**. The inner product $(\cdot,\cdot)$ on a linear space $\mathcal{H}$ satisfies

(a) $(v, v) \geq 0 \ \ \forall v \in \mathcal{H}$

(b) $(v, v) = 0 \Leftrightarrow v = 0.$

Eq. (2.7), we obtain discretized wave equation:

$$\sum_{i=1}^{m} x_i(\nabla \times \mu_r^{-1}\nabla \times \mathbf{P}_i - k_o^2\epsilon_r\mathbf{P}_i) = 0. \tag{2.9}$$

The next step is the discretization of the range of the differential operator, $\mathcal{L} = \nabla\times(\mu_r^{-1}\nabla\times) - k_o^2\epsilon_r$, and defining the weighting functions $\mathbf{Q} = \{\mathbf{Q}_1, \mathbf{Q}_2, \ldots, \mathbf{Q}_n\}^T \subset \mathcal{H}_2$, a Hilbert space. Now, the weighting operation on the discretized wave equation is performed as

$$\sum_{i=1}^{m} x_i\langle \mathbf{Q}_j, (\nabla \times \mu_r^{-1}\nabla \times \mathbf{P}_i - k_o^2\epsilon_r\mathbf{P}_i)\rangle = 0 \quad \text{for j=1,...,n} \tag{2.10}$$

where the inner product $\langle \mathbf{A}, \mathbf{B}\rangle$ is defined as follows:

$$\langle \mathbf{A}, \mathbf{B}\rangle \;=\; \iiint_{\Omega_e} \mathbf{A}\cdot\mathbf{B}\; dv.$$

Now, with aid of some of vector identities[2] and the divergence theorem[3], Eq. (2.10) can be written as

$$\sum_{i=1}^{m} x_i\{\langle \mu_r^{-1}\nabla \times \mathbf{P}_i, \nabla \times \mathbf{Q}_j\rangle - \; k_0^2\langle \epsilon_r\mathbf{P}_i, \mathbf{Q}_j\rangle\}$$
$$+\sum_{i=1}^{m} x_i \oint_{\partial\Omega_e} \hat{\mathbf{n}}\cdot[\mu_r^{-1}(\nabla \times \mathbf{P}_i)\times\mathbf{Q}_j]ds = 0 \quad \text{for j=1,...,n.} \tag{2.11}$$

where the last term can be modified to accommodate an equivalent surface current as

$$-\,j\omega\mu_0 \oint_{\partial\Omega_e} (\hat{\mathbf{n}}\times\mathbf{H})\cdot\mathbf{Q}_j ds. \tag{2.12}$$

In view of the continuity of the magnetic field across any material interface bearing no surface current, it is recognized that the contribution from the last term of Eq. (2.11) for interior Ω_e is zero except the cases when there are surface current sources.

[2] $\mathbf{B}\cdot\nabla\times\mathbf{A} = \nabla\cdot(\mathbf{A}\times\mathbf{B}) + \mathbf{A}\cdot\nabla\times\mathbf{B}$

[3] $\int_\Omega \nabla\cdot\mathbf{A}d\Omega = \oint_{\partial\Omega}\mathbf{A}\cdot d\mathbf{S}$

The linear system of equation (2.11) can be represented in a matrix form for each subregion Ω_e as follows;

$$[\mathbf{A}^e]^T [\mathbf{x}^e] = [\mathbf{b}^e] \tag{2.13}$$

where

$$\begin{aligned}
[\mathbf{A}^e] &= [\mathbf{U}^e] - k_o^2 [\mathbf{V}^e] \\
U_{ij}^e &= \langle \mu_r^{-1} \nabla \times \mathbf{P}_i, \nabla \times \mathbf{Q}_j \rangle \\
V_{ij}^e &= \langle \epsilon_r \mathbf{P}_i, \mathbf{Q}_j \rangle \\
x_i^e &\in [x_1^e, \ldots, x_m^e] \\
b_j^e &\in [b_1^e, \ldots, b_n^e] = -j\omega\mu_0 \oint_{\partial\Omega_e} (\hat{\mathbf{n}} \times \mathbf{H}) \cdot \mathbf{Q}_j ds
\end{aligned}$$

and $1 \leq i \leq m$, $1 \leq j \leq n$. The column vector $[\mathbf{b}^e]$ in the right hand side of Eq. (2.13) can be used as a forcing function to impress an arbitrary surface current.

2.4 Basis and Weighting Functions

Given the limitation of the node-based FEM, such as incorrect modeling of boundary conditions, and solutions contaminated by unwanted spurious modes, we applied in this study the edge-based vector basis functions $\mathbf{W}_j^e$ with tetrahedral sub-domain elements [13]–[19], which are known as Whitney 1-form,[4] as both basis and weighting functions ($\mathbf{P}_i = \mathbf{W}_i^e$ and $\mathbf{Q}_j = \mathbf{W}_j^e$) leading to Galerkin's method.[5]

In terms of global coordinate systems the edge basis function $\mathbf{W}_j^e$ is defined as follows (refer to Fig. 2.2) for $j = 1, \ldots, 6$,

$$\mathbf{W}_j^e = \begin{cases} \mathbf{f}_j + \mathbf{g}_j \times \mathbf{r}, & \mathbf{r} \in \Omega_e \\ 0, & \mathbf{r} \notin \Omega_e \end{cases} \tag{2.14}$$

[4] See section 2.7.2.

[5] Galerkin's method is known to provide second-order accuracy [44].

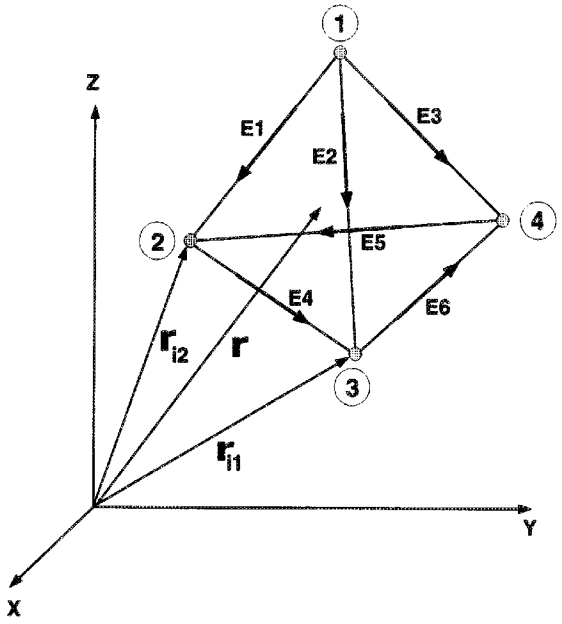


Figure 2.2: Tetrahedral element and associated nodes and edges definitions. The circled numbers 1 to 4 represent four node labels and **E1** to **E6** six edges associated with those nodes. $\mathbf{r}_{i1}$ and $\mathbf{r}_{i2}$ are node vectors associated with the i^{th} edge and $\mathbf{r}$ is an arbitrary vector which lies in the tetrahedron.

where

$$\begin{aligned} \mathbf{f}_j &= \frac{b_j}{6\Omega_e}\mathbf{r}_{(7-j)1} \times \mathbf{r}_{(7-j)2} \\ \mathbf{g}_j &= \frac{b_j b_{7-j}}{6\Omega_e}\mathbf{e}_{7-j} \\ \mathbf{e}_{7-j} &= (\mathbf{r}_{(7-j)2} - \mathbf{r}_{(7-j)1})/b_j \\ b_{7-j} &= \mid \mathbf{r}_{(7-j)2} - \mathbf{r}_{(7-j)1} \mid \end{aligned}$$

and $\mathbf{e}_j$ is the unit vector for the j^{th} edge and b_j is the length of the edge. The $\mathbf{r}_{(7-j)1}$ and $\mathbf{r}_{(7-j)2}$ are the vectors from the origin to the two nodes consisting of the $(7-j)^{th}$ edge. Alternatively, the definition of the edge basis function with respect to local coordinates has a quite different form. For an edge $p = \{i, j\}$,

$$\mathbf{W}_p^e = \lambda_i \nabla\lambda_j - \lambda_j \nabla\lambda_i \tag{2.15}$$

where $\lambda_n(\mathbf{r})$ ($n = i$ or j node) is the barycentric weight of $\mathbf{r}$ in its tetrahedron with respect to vertex n and forms a continuous piecewise-linear function.[6] The behavior of the basis function $\mathbf{W}_p^e$ can be visualized as shown in Fig. 2.3, that is, the fields turn around the axis $k-l$ ("central axis") remaining normal to planes containing the central axis. Also, the field has a magnitude proportional to the distance to the axis. Note that $\nabla\lambda_j$ and $\nabla\lambda_i$ are orthogonal to facets $\{i, k, l\}$ and $\{j, k, l\}$, respectively.

[6] For example, λ_i is defined in a tetrahedron $\{i, j, k, l\}$ in Fig. 2.3 as $\lambda_i = \frac{volume\{r,j,k,l\}}{volume\{i,j,k,l\}}$ and can be evaluated as

$$\lambda_i = \begin{cases} 1 & \text{if } x \text{ coincides with the } i^{th} \text{ node} \\ 0 & \text{if } x \text{ coincides with the } j^{th} (j \neq i) \text{ nodes.} \end{cases}$$

For an arbitrary point $r = (x, y, z) \in \Omega_e$, the relationship between the global and local coordinate systems can be found as

$$\begin{bmatrix} x \\ y \\ z \\ 1 \end{bmatrix} = \begin{bmatrix} x_1 & x_2 & x_3 & x_4 \\ y_1 & y_2 & y_3 & y_4 \\ z_1 & z_2 & z_3 & z_4 \\ 1 & 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} \lambda_1 \\ \lambda_2 \\ \lambda_3 \\ \lambda_4 \end{bmatrix}$$

where (x_i, y_i, z_i) denotes the global coordinates of the 4 vertices of a tetrahedron.

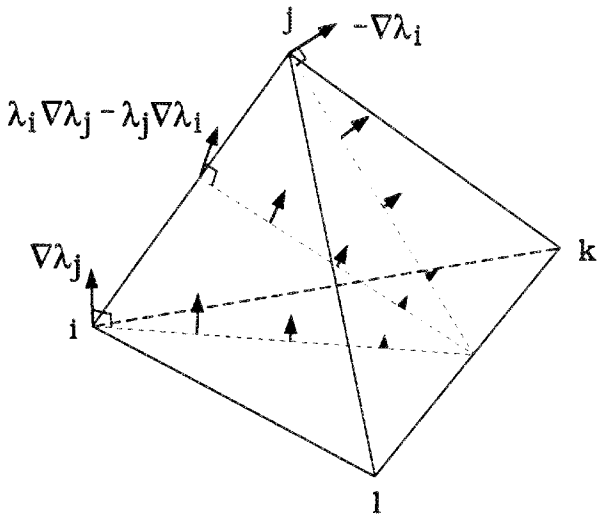


Figure 2.3: Behavior of edge element $\mathbf{W}_p^e$ for edge $p = \{i, j\}$.

This basis function has several other important properties as follows:

$$\nabla \cdot \mathbf{W}_p^e = 0 \tag{2.16}$$

$$\nabla \times \mathbf{W}_p^e = 2\mathbf{g}_p = 2\nabla\lambda_i \times \nabla\lambda_j \tag{2.17}$$

$$\mathbf{W}_p^e \cdot \mathbf{e}_q \mid_{\text{r on the } p^{th} \text{ edge}} = \delta_{pq} \tag{2.18}$$

where δ_{pq} is the Kronecker delta function. The basis functions satisfy "the divergence-free condition" since the $\mathbf{E}$ field obtained from a linear combination of the basis functions exactly satisfy $\nabla \cdot \mathbf{E} = 0$. More importantly, the edge basis function enforces the tangential continuity of the $\mathbf{E}$ fields across the material interfaces and allows discontinuity in the normal component across the interface, which render correct modeling of the physical boundary conditions. In addition, the modeling capability of the edge basis functions for the null-space of the curl operator contribute to the fact that the solutions are not contaminated with spurious modes [43]–[47], a serious drawback of the node based FEM. Equation (2.17) is interpreted as meaning that the curl of the basis function is a constant vector and provides a convenient tool for

calculation of the **H** field from a given **E** field as

$$\mathbf{H} = \frac{2j}{\omega\mu} \sum_{i=1}^{6} x_i \mathbf{g}_i. \tag{2.19}$$

However, the **H** field computed above has a constant value in each tetrahedral element and thus provides limited accuracy in modeling the magnetic fields. The third property, Eq. (2.18), implies that $\mathbf{W}_p^e$ has no tangential components along any of the edges except p^{th} one. Therefore, coefficient x_i can be considered as a projection of the electric field onto the i^{th} edge. This property can be easily verified by considering the facts that $\lambda_i = 0$ on the edges $\{j,k\}$, $\{j,l\}$, and $\{l,k\}$ and $\lambda_j = 0$ on the edges $\{i,k\}$, $\{i,l\}$, and $\{l,k\}$, and the fact that $\mathbf{W}_p^e$ has no tangential component on the facets $\{j,k,l\}$ and $\{i,k,l\}$.

2.5 Assembly of Matrix Equation and Its Solution Methods

From the sub-domain matrix equation, $[\mathbf{A}^e]^T[\mathbf{x}^e] = [\mathbf{b}^e]$, the global matrix equation is constructed by assembling the contributions from all the tetrahedrons. In practice, a unique global edge numbering system, global-to-local indexing, is introduced to every edge and the augmenting procedure is performed based upon this edge numbering system. In other words, for every tetrahedron a 6×6 element matrix is created according to the local numbering system and a lookup table, $I(e,i)$, for global edge numbering system. The lookup table relates the local edge number, i, on a particular element, e, to its position in the global data structure. To assemble the global matrix equation, each row and column in $[\mathbf{A}^e]$ is added to the global matrix $[\mathbf{A}]$ by referring to the lookup table, and a similar procedure is applied to $[\mathbf{x}^e]$ and $[\mathbf{b}^e]$ to form $[\mathbf{x}]$ and $[\mathbf{b}]$, respectively. As a result, the final matrix equation is assembled as:

$$[\mathbf{A}]^T [\mathbf{x}] = [\mathbf{b}] \tag{2.20}$$

where

$$
\begin{aligned}
[\mathbf{A}] &= \bigcup_{e=1}^{M} \{[\mathbf{U}^e] - k_o^2[\mathbf{V}^e]\} \\
[\mathbf{x}] &= \bigcup_{e=1}^{M} [\mathbf{x}^e] \\
[\mathbf{b}] &= \bigcup_{e=1}^{M} [\mathbf{b}^e].
\end{aligned}
$$

The M denotes the total number of tetrahedrons in the domain Ω, which is, in general, different from the total number of edges, say L. The set operation $\bigcup_{e=1}^{M}$ represents assembly operations based upon the global edge numbering system for all M tetrahedrons. Therefore, the matrices $[\mathbf{A}]$, $[\mathbf{x}]$, and $[\mathbf{b}]$ become $L \times L$, $L \times 1$, and $L \times 1$ matrices, respectively. With the tetrahedral edge basis functions, Eq. (2.14) or (2.15), the matrix elements for $[\mathbf{U}^e]$ and $[\mathbf{V}^e]$ are evaluated as (see Appendix A for details):

$$U_{ij}^e = \langle \mu_r^{-1} \nabla \times \mathbf{W}_i, \nabla \times \mathbf{W}_j \rangle \tag{2.21}$$

$$V_{ij}^e = \langle \epsilon_r \mathbf{W}_i, \mathbf{W}_j \rangle. \tag{2.22}$$

It is crucial to be aware of the properties of the final FEM matrix $[\mathbf{A}]$. For lossy or lossless materials and even for uniaxial anisotropic materials, the i^{th} and j^{th} edges in a tetrahedron have identical contributions to $[\mathbf{A}^e]$ and eventually to $[\mathbf{A}]$ rendering the matrix $[\mathbf{A}]$ complex symmetric, but not Hermitian. Also, it is observed that the set of eigenvalues of the source-free equation[7] contains multiple zero eigenvalues corresponding to the solution of the DC gradient electromagnetic fields. As a result, the matrix $[\mathbf{A}]$ becomes positive semi-definite system. Another very important and fundamental property of the matrix $[\mathbf{A}]$ is its sparsity, which is a natural consequence of the compact supported expansion and weighting functions.

[7]The eigenvalues are the solution to the generalized eigenvalue problem: $[\mathbf{U}][\mathbf{x}] = \lambda[\mathbf{V}][\mathbf{x}]$

The degree of the sparsity varies case by case, but for structured mesh it can be predicted, as will be presented in later section.

In this work, the conjugate (CG) and bi-conjugate gradient (BiCG) method [48]–[57] for real symmetric or Hermitian matrices and the conjugate orthogonal conjugate gradient (COCG) method [58] for complex symmetric matrix have been implemented with diagonal preconditioning to speed up the convergence rate and to improve the solution accuracy (refer to Appendix B for detail). In general, the CG type linear equation solver requires $\mathcal{O}(N^2)$ floating point operations in each iteration for the full $N \times N$ matrix $[\mathbf{A}]$. As a result, if it takes n iterations to solve a full matrix equation, $[\mathbf{A}][\mathbf{x}] = [\mathbf{b}]$, the required operation count is $\mathcal{O}(nN^2)$, which could be $\mathcal{O}(N^3)$ for large n comparable to N. In this case, the CG type solver loses its attractiveness and feasibility for solving huge matrix equations. Fortunately, the matrix equation generated by the FEM is very sparse and its sparsity [8] reaches higher than 99% in the usual practical problems. This sparsity gives a real attraction to the CG type solver, since the required operation counts become $\mathcal{O}(nmN) \ll \mathcal{O}(nN^2)$, where m is the average number of non-zero entries in a sparse matrix [9]. As described in detail in section 2.9, m becomes at most 20 for structured mesh and N is several orders of magnitude greater than m.

In particular, the BiCG and COCG methods are computationally efficient for positive semi-definite matrices since these methods require only 1 matrix-vector multiplication in each iteration, compared to 2 in the CG case. Even though the CG method guarantees its monotonic convergence for non-singular matrix regardless of whether

[8] The definition of the sparsity is given:

$$\text{sparsity} := \frac{N^2 - M_o}{N^2} \times 100 \ [\%], \quad \text{for } N \times N \text{ matrix}$$

where M_o is the total number of non-zero matrix entries.

[9] The definition of the average number of non-zero entries in a matrix is given as $m := M_o/N$

the matrix is positive definite or not, in this study, the BiCG and COCG methods with diagonal pre-conditioning are applied in view of their performance which is superior to the CG method. These methods reveal faster convergence (fewer iterations) and require a reduced computational burden in almost all cases.

2.6 Treatment of Boundary and Symmetry Conditions

2.6.1 Boundary Conditions

To obtain a unique solution of the wave equation in a given space (Ω), appropriate boundary conditions are required on the surface ($\partial\Omega$) enclosing the volume Ω. There are two important boundary conditions encountered in the electromagnetics applications, namely perfect electric conducting (PEC) and perfect magnetic conducting (PMC) boundaries. On the PEC (PMC) surface, the tangential electric (magnetic) field should be zero. The mathematical form of these conditions can be written as:

$$\hat{\mathbf{n}} \times \mathbf{E} = 0 \qquad \text{(PEC)} \tag{2.23}$$

$$\hat{\mathbf{n}} \times \mathbf{H} = 0 \qquad \text{(PMC)} \tag{2.24}$$

where $\hat{\mathbf{n}}$ is the unit normal vector pointing outward from the surface (refer to Fig. 2.4). The implementation of the PEC or PMC boundary conditions with the edge basis functions in the context of the FEM can be done in a straightforward manner. For example, in the **E** field formulation, the PMC surface becomes the natural boundary having zero normal electric field component on the surface, and is implemented naturally due to the divergence-free property of the basis function, as explained in section 2.3. However, the PEC condition can be enforced by setting to zero the coefficients of the edges x_i comprising the PEC surface, because the tangential field on a triangular surface of a tetrahedron is generated only by the three edge vectors which make up the triangle. It should be noted that when there are PEC

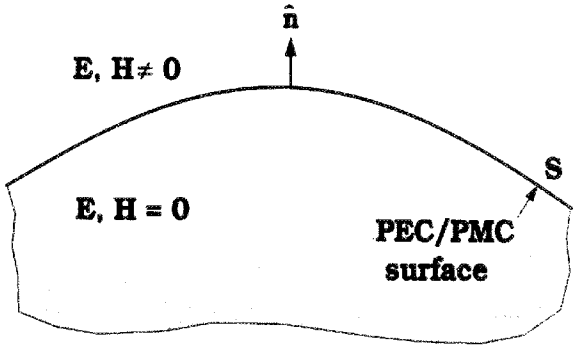


Figure 2.4: PEC or PMC surface S with outward unit normal vector $\hat{\mathbf{n}}$.

surfaces, the total number of unknowns is reduced accordingly since the unknown coefficients for the edges on the surfaces are removed, producing a reduced system of equations.

Another important outer boundary condition is the radiation boundary condition (RBC) describing the field behavior at infinity, as written below:

$$\lim_{R\to\infty} R[\nabla \times \mathbf{F} + jk_o\hat{\mathbf{r}} \times \mathbf{F}] = 0, \quad \mathbf{F} = \{\mathbf{E} \text{ or } \mathbf{H}\} \qquad \text{(RBC)} \tag{2.25}$$

where $\hat{\mathbf{r}}$ is the radial unit vector and $R = \sqrt{x^2 + y^2 + z^2}$ is the distance from the origin to the observation point. The RBC demands that the electric and magnetic fields decrease as $1/R$ in 3-dimensional space when $R \to \infty$.

At the interface between two different materials, more general boundary conditions are required since the fields on both sides have non-zero values. When there are surface currents ($\mathbf{J}_s$) and charges (ρ_s) at the interface, the tangential electric field should be continuous and the normal electric flux density is allowed to be discontinuous due to ρ_s. Similarly, at an interface bearing a surface current source the normal magnetic flux density is continuous and the tangential magnetic field should be discontinuous with the amount of $\mathbf{J}_s$. The boundary conditions are summarized

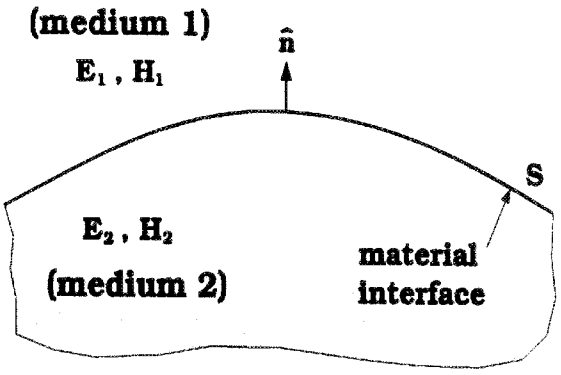


Figure 2.5: Material interface S with unit normal vector $\hat{\mathbf{n}}$.

as follows:

$$\hat{\mathbf{n}} \times (\mathbf{E}_1 - \mathbf{E}_2) = 0 \tag{2.26}$$

$$\hat{\mathbf{n}} \cdot (\mathbf{B}_1 - \mathbf{B}_2) = 0 \tag{2.27}$$

$$\hat{\mathbf{n}} \times (\mathbf{H}_1 - \mathbf{H}_2) = \mathbf{J}_s \tag{2.28}$$

$$\hat{\mathbf{n}} \cdot (\mathbf{D}_1 - \mathbf{D}_2) = \rho_s \tag{2.29}$$

where the $\hat{\mathbf{n}}$ is a unit normal vector pointing from medium 2 to 1 as defined in Fig. 2.5.

The surface charge density, ρ_s, and the surface current density, $\mathbf{J}_s$, are related to each other through the continuity equation:

$$\nabla_s \cdot \mathbf{J}_s = \frac{\partial \rho_s}{\partial t} \tag{2.30}$$

where the $\nabla_s \cdot$ denotes the surface divergence operator. It is worth mentioning that the equations (2.26) and (2.27) are equivalent and similarly the equation (2.28) and (2.29) are equivalent to each other. If one of the media is a perfect electric or perfect magnetic conductor, the electric and magnetic fields are zero inside and thus equations (2.23) and (2.24) are derived from equations (2.26)-(2.29). Note that no

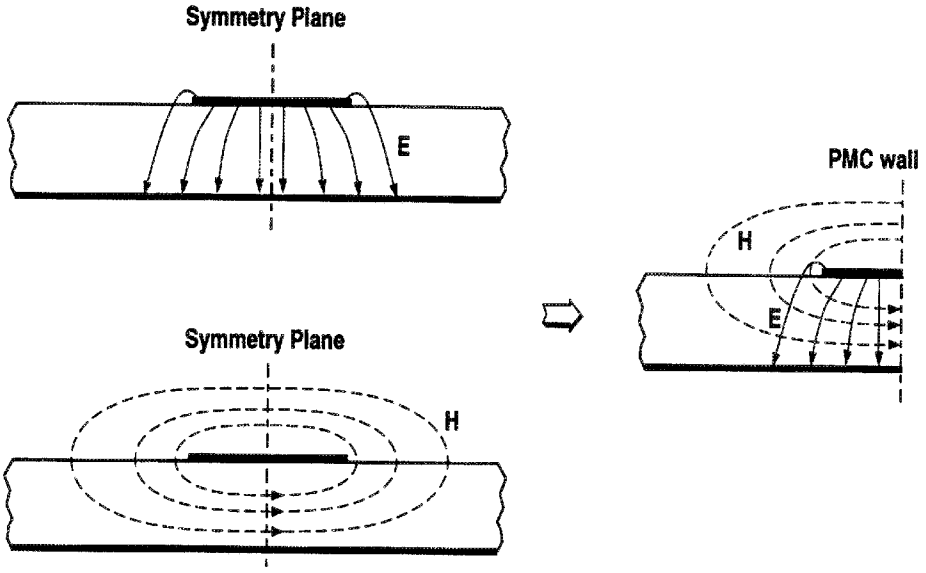


Figure 2.6: An example of a circuit configuration (microstrip line) bearing a symmetrical plane at the center and its electric and magnetic field distributions. As presented on the right, the original problem can be replaced with half of the structure, with PMC symmetry condition on one side.

surface current or charges can exist on the surface of perfect conducting bodies.

2.6.2 Symmetry Conditions

In general, many microwave and millimeter-wave circuits and interconnects contain geometrical and electrical symmetries, which, if handled properly, can confer computational advantages and simplicity. In this study, two types of symmetry boundary conditions (refer to Fig. 2.6 and Fig. 2.7) are exploited based on the electric and magnetic fields distributions.

As illustrated in Fig. 2.6, when there are only tangential electric and normal magnetic fields components on an arbitrary plane or surface, the plane can be modeled as a PMC surface. By applying the PMC boundary condition, the original problem is

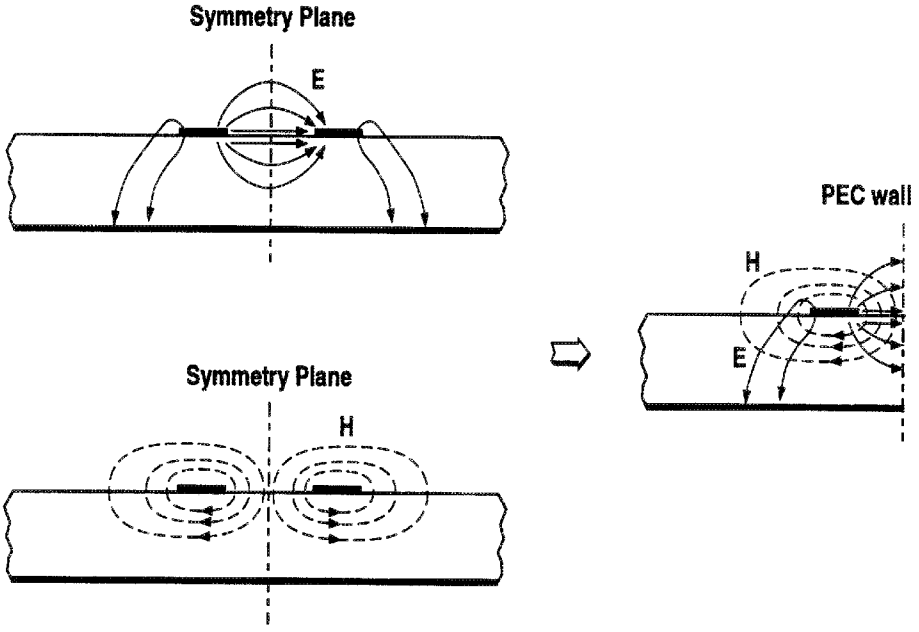


Figure 2.7: An example of a circuit configuration (double strip line) containing symmetry at the center and its electric and magnetic field distributions. The original problem can be replaced with the half of the structure with PEC symmetry condition at the center as shown on the right.

replaced with the reduced one as shown on the right hand side of the figure without changing the original field distributions and thus the solution of the original electromagnetic problem can be obtained by solving the half structure. Needless to say, it is much easier and more efficient to handle the reduced equivalent problem than the original one. Analogously, as shown in Fig. 2.7, a fictitious surface bearing only a tangential magnetic and normal electric field components can be interchanged with the PEC boundary, resulting in a reduced equivalent problem. Even though Fig. 2.6 and 2.7 illustrate the symmetries in the microstrip and double strip lines, similar symmetries can be found in the coplanar waveguide (CPW) and in the slot-line with their dominant mode distributions.

In many case, the symmetry planes are generated due to specific source con-

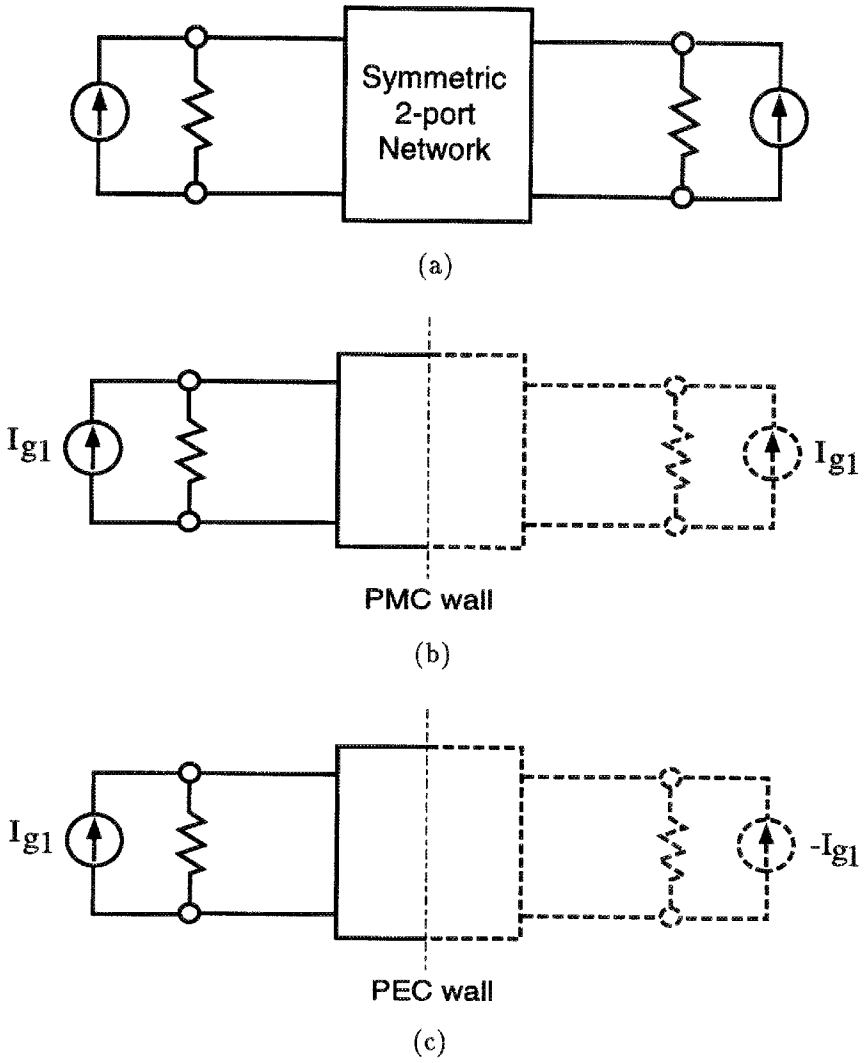


Figure 2.8: Reduced equivalent circuits for symmetric 2-port network depending on excitation configurations: (a) original network, (b) reduced equivalent network for even mode excitation, and (c) reduced equivalent network for odd mode excitation.

figurations. For example, a symmetric 2-port network with even and odd mode excitations [10] can be transformed into either of two simplified equivalent networks, depending on source arrangements, as shown in Fig. 2.8. In this case, to characterize the original network, only half of the problem can be solved with PEC or PMC condition according to a given source configuration.

Obviously, with the CG type linear equation solver the reduced equivalent problem requires much less computational costs, since the BiCG and COCG routines used in this study demand $\mathcal{O}(nmN)$ floating point operations for an $N \times N$ matrix [11] and $\mathcal{O}(\tilde{n}m\tilde{N})$ for $\tilde{N} \times \tilde{N}$ matrix, where $\tilde{n} < n$ for $\tilde{N} < N$. For example, if an $N \times N$ matrix takes $n = N$ iterations for convergence and an $\tilde{N} \times \tilde{N}$ ($\tilde{N} = N/2$) matrix needs $\tilde{n} = N/2$ iterations, then $\mathcal{O}(\tilde{n}m\tilde{N}) = \mathcal{O}(nmN)/4$. Hence, the half-reduced equivalent problem takes only 1/4 of the computational cost of the initial problem. For structures having two symmetry planes, when the symmetry is fully accounted, the required operation counts for the equivalent problem are reduced to 1/16 of the operation counts for the original problem. As mentioned in the previous section, the PEC and PMC boundary conditions are implemented without any further theoretical and practical complications. On the contrary, those will provide great advantages on reducing the problem size to a half, a quarter, or even to a 1/8 of the original problem. When the number of FLoating point OPerations (FLOPs) is considered, as summarized in Table 2.1, it becomes clear what is the real advantage gained due to the reduction in problem size. This is one of the most important aspects of the symmetry boundary conditions and the reason why the symmetry of a given problem should be fully exploited whenever possible.

[10] See appendix C.
[11] See section 2.5.

Symmetry Planes	Problem Size	FLOP Count
0	mN	$\mathcal{O}(mN^2)$
1	$mN/2$	$\mathcal{O}(mN^2)/4$
2	$mN/4$	$\mathcal{O}(mN^2)/16$
3	$mN/8$	$\mathcal{O}(mN^2)/64$
k	$mN/(2^k)$	$\mathcal{O}(mN^2)/(2^{2k})$

Table 2.1: Summary of FLoating point OPeration (FLOP) counts for reduced equivalent problems. In the table, the number of iterations for convergence are assumed to be the maximum which is the matrix size.

2.7 The Question of Spurious Solutions: A Rationale for Using the Edge Basis Function

2.7.1 The Origin of Spurious Solutions

The occurrence of physically incorrect spurious solutions in the various numerical techniques, such as the FEM, the method of moment (MoM), etc, has been noted, and many attempts have been made to explain and cure spurious modes [40], [43]-[17], [45], [46], [59]-[71][12]. It has been found that these spurious solutions satisfy the finite element equations, but not the physical boundary conditions, and occur regardless what combination of vector components are involved. Thus, the spurious modes and the physically correct solutions may be discriminated by applying the exact boundary conditions on the inter-element and inter-material interfaces. On the interface of two different materials or on the boundaries of interior sub-domain elements, the tangential electric ($\hat{\mathbf{n}} \times \mathbf{E}$) and magnetic ($\hat{\mathbf{n}} \times \mathbf{H}$) fields should be continuous if there are no current sources, while the normal components $\hat{\mathbf{n}} \cdot \mathbf{E}$ and $\hat{\mathbf{n}} \cdot \mathbf{H}$ are allowed to be discontinuous across the material interfaces. It has also been observed that the spurious solutions exhibit non-zero divergence fields even without containing any sources. Hence, the spurious solutions can be distinguished *a posteriori* by monitoring the divergence of the computed solutions or the behavior of eigenvectors.

[12] From the abundance of literature dealing with the spurious modes phenomenon, one can imagine how difficult and how important this task is.

This observation has led to the speculation that the enforcement of the divergence-free condition through the penalty function method would cure the occurrence of the non-physical solutions [8]-[12]. However, it has been proved [43, 46, 72] that the enforcement of the divergence-free condition cannot insure spurious-free solutions. Furthermore, even though this penalty function approach has gained partial success by removing or relocating the spurious solutions from the spectral region of interests, it is considered to be "sweeping dust under the rug" [16].

Recently, a rigorous theoretical analysis has been presented [43] on the cause of the spurious modes in numerical electromagnetic field eigenvalue problems. In view of the vastness of the spurious modes phenomenon across many different numerical methods, a source of the phenomenon has been identified as a misconception of the discretization of a parameter dependent indefinite or semi-definite linear operator. When such an operator family is applied to an n-dimensional subspace of its domain, the family image in general may contain a subspace of dimension higher than n. As a result the discretization of the parameter independent set of expansion and weighting functions of equal cardinality has the potential to fail. This reasoning is not incompatible with the conjecture in [73] which describes the root cause of the spurious solutions as the improper approximation of the null-space of the curl operator.

2.7.2 Why the Whitney Edge Element?

Based upon the above observations, the Whitney edge element [13]-[18], [74] is employed in this study for the implementation of a robust finite element method known *a priori* to produce spurious-free solutions. As is already discussed in section 2.4, the edge basis function has many desirable properties, including its divergence-

free condition

$$\nabla \cdot \mathbf{W}_p^e = 0 \quad \Rightarrow \quad \nabla \cdot \mathbf{E} = \nabla \cdot (\sum_{j=1}^{6} x_i \mathbf{W}_p^e) = 0$$

and accurate modeling of boundary conditions for tangential as well as normal electric field components. Furthermore, the discrete algebraic-geometric-differential [75]-[77] structure of the Whitney element closely matches the continuous one, providing a good approximation method. The Whitney complex can be represented as

$$W^0 \xrightarrow{grad} W^1 \xrightarrow{curl} W^2 \xrightarrow{div} W^3 \qquad \text{(ascending sequence)} \qquad (2.31)$$

$$W^0 \xleftarrow{grad_*} W^1 \xleftarrow{curl_*} W^2 \xleftarrow{div_*} W^3 \qquad \text{(descending sequence)} \qquad (2.32)$$

where W^p is the finite dimensional subspace generated by taking linear combinations, with complex coefficients, of p-Whitneys. The adjoint operators $grad_*$, $curl_*$, and div_* coincide with $-div$, $curl$, and $-grad$, respectively, on its complement domain and the Whitney elements of order $p = 0, 1, 2, 3$ correspond to node, edge, facet, and volume elements, respectively. Considering the inherent mathematical symmetry of structure in electromagnetics

$$\Phi \xrightarrow{-grad} \mathbf{E} \xrightarrow{-\frac{curl}{j\omega}} \mathbf{B} \xrightarrow{div} 0 \qquad (2.33)$$

$$\Omega \xrightarrow{-grad} \mathbf{H} \xrightarrow{\frac{curl}{j\omega}} \mathbf{D} \xrightarrow{div} \rho_e, \qquad (2.34)$$

where Φ and Ω denote electric and magnetic scalar potentials, respectively, the remarkable similarity of the Whitney complex to Maxwell's equations leads to its excellent modeling capability for electromagnetic fields. Further, the conformity of the Whitney complex

$$W^0 \subset \text{domain}(grad) \qquad (2.35)$$

$$W^1 \subset \text{domain}(curl) \qquad (2.36)$$

$$W^2 \subset \text{domain}(div) \qquad (2.37)$$

reinforces the similarity between them and gives some of the basic properties of the Whitney elements:

- Function W^0 (node element) is continuous across facets
- The tangential component of W^1 (edge element) is continuous across facets
- The normal component of W^2 (facet element) is continuous across facets.

In this study, the Whitney 1-form, W^1, the so-called edge element, is employed to model the electric field distributions in each sub-domain. As mentioned above, W^1 shares many basic properties with the electric field, $\mathbf{E}$, and thus renders spurious-free solutions.

2.7.3 Eigenvalue Analysis with Edge Element

From the source-free vector wave equation (2.7), the system of linear equations (2.20) obtained after applying Galerkin's procedure is reduced to the generalized eigenvalue problem. The generalized eigenvalue problem can be stated as:

$$([\mathbf{U}] - \lambda[\mathbf{V}])[\mathbf{x}] = 0 \tag{2.38}$$

where

$$[\mathbf{U}] = \bigcup_{e=1}^{M}[\mathbf{U}^e], \quad [\mathbf{V}] = \bigcup_{e=1}^{M}[\mathbf{V}^e]$$

and the matrix entries of $[\mathbf{U}^e]$ and $[\mathbf{V}^e]$ are defined as in equations (2.21) and (2.22). The eigenvalue λ is the square of a propagation constant, $k_o = \sqrt{\lambda}$, and has real non-negative values for a lossless isotropic medium. A set of eigenvalue and eigenvector, $\{\lambda, \mathbf{x}\}$, represents the electromagnetic field distribution at a specific frequency, $f_0 = (c/2\pi)k_0$. The spurious eigenvalues are identified by examining the corresponding eigenvectors. In general, the eigenvectors of the spurious modes exhibit non-physical field distributions, such as node-to-node variations, or have significantly

higher divergence values:

$$\iiint_{\Omega} | \nabla \cdot \mathbf{E} |^2 \, dv \gg 0.$$

With the edge element, it has been found that no spurious modes are interspersed among the physical solutions. However, the computed set of eigenvalues of the generalized eigenvalue equation (2.38) contains multiple zero eigenvalues ($\lambda = 0$) which correspond to the DC gradient electric fields, Φ. Note that any gradient fields satisfy the vector wave equation with $\nabla \times (\nabla \Phi) = 0$. These zero eigenvalues can be interpreted as a separate class of spurious modes since their existence does not interfere with finding physical solutions, except when the discrete numerical scheme does not approximate them properly. This inaccurate approximation has been considered as a possible source of the non-physical spurious modes [66, 73]. The number of zero eigenvalues, N_{zero}, can be accurately predicted for structured tetrahedral mesh, in which the domain is divided into bricks and then each brick is subdivided into 5 tetrahedrons, as follows:

$$N_{zero} = \begin{cases} (N_x - 2)(N_y - 2)(N_z - 2), & \text{for } \mathbf{E}\text{-field formulation} \\ N_x N_y N_z - 1, & \text{for } \mathbf{H}\text{-field formulation} \end{cases} \tag{2.39}$$

where N_x, N_y and N_z are the number of nodes in x, y, and z directions, respectively. For the **E**-field formulation, the N_{zero} is coincident with the number of interior nodes in a simply connected domain surrounded with the PEC boundary conditions. For the **H**-field formulation, the number of zero eigenvalues is identical to the number of edge-tree branches in the domain with PEC outer surface, which will be the natural boundary condition. The number of edge-tree branches can be computed from the difference between the total number of edges and the number of independent algebraic equations [78]. Tables 2.2 and 2.3 show examples of the number of zero eigenvalues

(N_x, N_y, N_z)	Total # of edges	# of surface edges	Matrix Size M	# of interior nodes	N_{zero}
(3,3,3)	90	72	18	1	1
(4,4,4)	252	162	90	8	8
(5,5,5)	540	288	252	27	27
(6,6,6)	990	450	540	64	64
(7,7,7)	1638	648	990	125	125

Table 2.2: Number of zero eigenvalues for simply connected cavity with **E**-field formulation.

(N_x, N_y, N_z)	Total # of edges	# of surface edges	Matrix Size M	Total # of nodes	N_{zero}
(2,2,2)	18	0	18	8	7
(3,3,3)	90	0	90	27	26
(4,4,4)	252	0	252	64	63
(5,5,5)	540	0	540	125	124
(6,6,6)	990	0	990	216	215
(7,7,7)	1638	0	1638	343	342

Table 2.3: Number of zero eigenvalues for simply connected cavity with **H**-field formulation.

and other relevant quantities for the **E**- and **H**-field formulations in various mesh configurations. As shown in the tables, the **E**-field formulation requires a lower computational cost, i.e., a smaller matrix size M, than that of the **H**-field, due to the PEC boundary condition, as described in section 2.6.1.

2.8 Excitation Mechanism

In the application of the FEM for the characterization of high frequency and high-speed interconnects, many different types of excitation mechanisms could be employed. Since the extracted circuit parameters should be independent of the excitations, one can choose a convenient excitation method suited to specific applications. For faster convergence, two dimensional (2D) field distributions on each face of the port can be used: however, this approach requires another 2D electromagnetic field simulator. In this study, ideal impulse current sources are employed and imposed on

the corresponding edges of the tetrahedrons. Even though the ideal current sources generate impulses at the sources, the electromagnetic fields quickly conform to the appropriate field distribution according to the boundary conditions, even in the close vicinity of the sources.

In the finite element formulation, the ideal current source could be implemented either in conjunction with the inhomogeneous wave equation, or using the appropriate boundary conditions with the homogeneous wave equation (see Eq. (2.7)). Consider the right-hand side of the weak form of the homogeneous wave equation (2.13):

$$b_i^e = -jk_0 Z_0 \oint_{\partial\Omega_e} \mathbf{W}_i^e \cdot (\hat{\mathbf{n}} \times \mathbf{H})\, dS. \tag{2.40}$$

In the kernel of the integral, the $\hat{\mathbf{n}} \times \mathbf{H}$ can be interpreted as a current source $\mathbf{J}$ and the dot product between $\mathbf{J}$ and $\mathbf{W}_i^e$ can be considered as a line current $\mathbf{J}_l$ on the edge of the surface triangle $\partial\Omega_e$. As a result, the excitation vector $[\mathbf{b}^e]$ with an appropriate scaling factor is given as

$$\oint_{\partial\Omega_e} \mathbf{W}_i^e \cdot \mathbf{J}\, dS = \delta_{ij} \quad \text{for a source at } j^{th} \text{ edge.} \tag{2.41}$$

When there are several sources, as in the case of a multi-port network, the excitation vector $[\mathbf{b}^e]$ has non-zero elements and the positions of those non-zeros correspond to the global indices of the excitation edges, as shown below:

$$[\mathbf{b}^e]^T = [0 \quad 0 \cdots 0 \quad b_i \quad 0 \cdots 0 \quad b_j \quad 0 \cdots 0] \tag{2.42}$$

where the b_p $(1 \leq p \leq N, p = \{i, j\})$ are an appropriate non-zero pair of numbers for various sets of excitation mechanisms such as the even, odd, or sum excitation discussed in Appendix C. In Figure 2.9, two different configurations of the current source excitations used in this study are illustrated. As shown in the figure, horizontal or vertical excitations produce identical results.

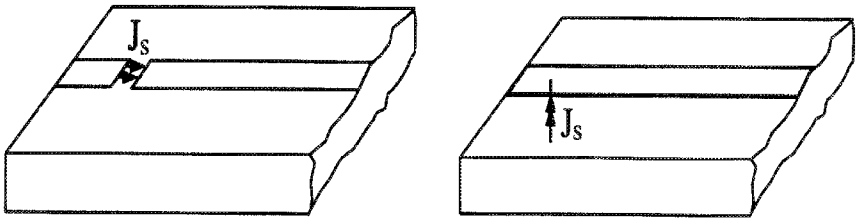


Figure 2.9: Two types of ideal excitation configurations: (a) horizontal current source on the transmission line plane. (b) vertical current source.

2.9 Customized Generation of Tetrahedral Mesh

The first step of the finite element analysis is a discretization of the domain of interest into appropriate sub-domain elements. In this study, for the discretization of a given three-dimensional space Ω into a number of tetrahedral sub-domain elements Ω_e, a simple and efficient structural mesh generation algorithm is developed. In particular, to accommodate and model effectively the large contrast in geometrical details commonly found in high-speed high-frequency interconnects, both uniform and non-uniform meshing schemes are implemented. In non-uniform mesh, variable size rectangular bricks are created first and then each brick is subdivided into five tetrahedrons in two different ways as shown in Figure 2.10 (see Table 2.4 for labeling system). Note that those two different ways of subdividing a brick are mirror images of each other. For continuity of the edges across the brick faces, all of the neighboring bricks sharing a face with each other are assigned to have different types of dispositions.

One advantage of using the structural mesh is its regularity, which allows accurate prediction of the total number of edges (i.e., the total number of unknowns) and tetrahedrons, the edge connectivities, and the resulting memory requirement for a given problem. For an edge which is parallel to the Cartesian axis, there are 4

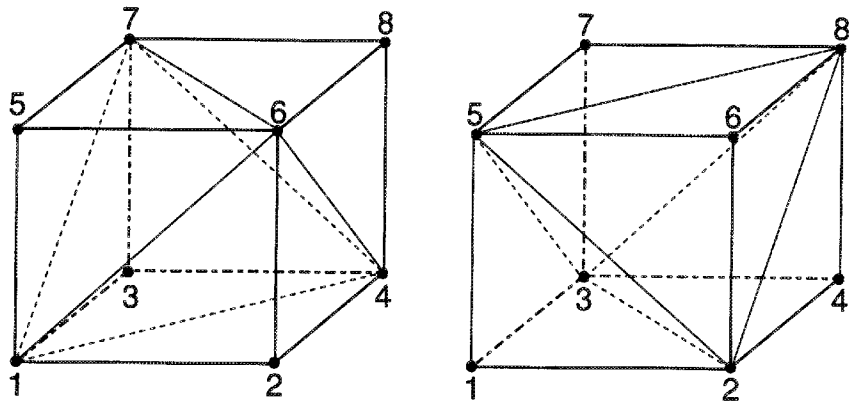


Figure 2.10: Two types of rectangular bricks which containing five tetrahedral elements: (a) Type I, (b) Type II

Tetrahedron	Type I	Type II
$\{i, j, k, l\}$	{1, 2, 4, 6}	{1, 2, 3, 5}
	{1, 5, 6, 7}	{2, 3, 4, 8}
	{1, 3, 4, 7}	{3, 5, 7, 8}
	{4, 6, 7, 8}	{2, 5, 6, 8}
	{1, 4, 6, 7}	{2, 3, 5, 8}

Table 2.4: Two types of tetrahedral labeling systems.

tetrahedrons surrounding the edge and 13 edges are associated with that. However, for a typical diagonal edge, 6 tetrahedrons are connected to that edge and therefore 19 edges are associated with that. As a result, the total number of non-zero entries in a row or column of an arbitrary FEM matrix is pre-determined to be 13 or 19 with the structural meshing scheme. Further, the average edge connectivity would be determined to be 15 from the fact that there are 12 edges parallel to the Cartesian axis and 6 edges diagonal in a rectangular brick [13]. The pre-determined edge connectivity allows efficient memory management and planning and building effective data structures for the best possible use of computing facilities, since the total number of edges in Ω determines the overall problem size to be solved.

The relationship between the number of tetrahedrons, nodes, and edges for a simply connected region, whether the structural meshing scheme is used or not, can be estimated as follows [79]

$$N_{edge} = N_{tet} + N_{node} + N_{surf} - 3 \tag{2.43}$$

where N_{tet}, N_{edge}, N_{node} and N_{surf} are the total number of tetrahedrons, edges, nodes, and surface nodes, respectively. This formula is very useful for the prediction of a problem size in either case, whether structured or unstructured mesh is used. However, for an unstructured mesh, it is not always possible to predict accurately the number of tetrahedrons, nodes and surface nodes, and even further, the edge connectivity varies over a large range.

Roughly, the total number of edges can be estimated as six times the total number of nodes and as a result the estimated number of total non-zero entries in a FEM matrix is 90 times of the total number of nodes. The average matrix density also can be estimated from the average number of non-zero entries in a row (or column)

[13] Average edge connectivity = (12 edges $\times$ 13 + 6 edges $\times$ 19)/18 edges = 15

Total # of nodes : N_{node}	$N_x N_y N_z$
Total # of tetrahedrons : N_{tet}	$5(N_x-1)(N_y-1)(N_z-1)$
Total # of surface nodes : N_{surf}	$2(N_xN_y+N_yN_z+N_zN_x)$ $-4(N_x+N_y+N_z)+8$
Total # of edges : N_{edge} (# of unknowns)	$6N_xN_yN_z-3(N_xN_y+N_yN_z+N_zN_x)$ $+5(N_x+N_y+N_z)+2$
# of non-zero entries in a row or column	13 or 19
Average # of non-zero entries in a row or column	15
Total # of non-zero entries in FEM matrix : M_o	$90N_xN_yN_z-75(N_xN_y+N_yN_z+N_zN_x)$ $-75(N_x+N_y+N_z)+30$
Average matrix density	$2.5/(N_xN_yN_z)$

Table 2.5: Estimations of some of the important quantities in the structural tetrahedral mesh. It is assumed that the domain is simply connected and there are no interior PEC surfaces which will reduce the total edge counts. N_x, N_y and N_z are the number of nodes in x, y and z direction, respectively.

and the size of the square matrix. Since the average edge connectivity has been determined to be 15 for any arbitrary problem, the overall problem size is directly proportional to the total edge count. Therefore, the sparsity of the FEM matrix can be estimated as given below

$$\text{sparsity} = (1-\frac{15}{N_{edge}})\times 100 \quad [\%] \tag{2.44}$$

$$\simeq \frac{2.5}{N_xN_yN_z}\times 100 \quad [\%]. \tag{2.45}$$

Note that the sparsity of the FEM matrix is approaching 100 % as the size of the problem, N_{edge}, is becoming larger. These relations are summarized in Table 2.5.

It has been found numerically that the iterative linear equation solvers mentioned in section 2.5 converge much faster with the uniform mesh than the non-uniform scheme, implying that the uniform mesh leads to a better matrix condition number. However, even though uniform mesh has the definite advantage of fast solution time for a fixed number of unknowns, it is not always advantageous to use the uniform mesh when there are large variations in detailed geometries as found in usual high-

speed high-frequency interconnects. In general, the uniform mesh generates a much larger matrix system than the non-uniform case when there are very small details in a structure and eventually causes a longer solution time. With these observations, the non-uniform structural meshing scheme is developed in this study to provide effective mesh data for circuits with large variations in detailed dimensions. Even in the non-uniform meshing scheme, the quality of each sub-domain element is also very important, since one badly distorted tetrahedral element could leads to a poor matrix condition number.

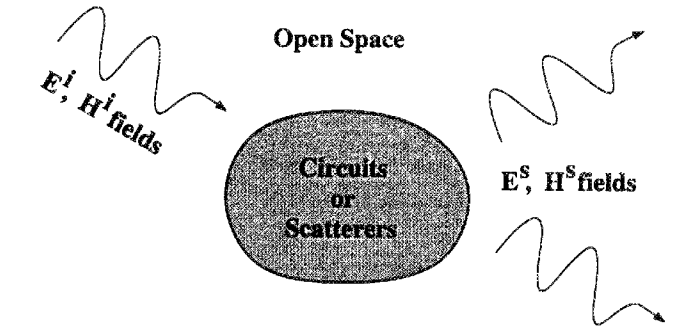
2.10 Treatment of Open Boundary Problems

Accurate modeling of high-speed high-frequency interconnects often requires treatment of closed as well as open boundary problems. However, due to the fact that one of the fundamental ideas based on partial differential equation (PDE) techniques is the restriction of the computational domain to a finite region, the open domain problem requires special techniques for appropriate approximation of the outer boundaries, as shown in Figure 2.11. In general, the difficulties in the treatment of open domain problems with appropriate outer termination boundaries have become a hindrance in the efficient PDE solution of practical problems. In the context of the finite element method, the open domain problems can be simulated in several different ways, such as the FEM-boundary integral (FEM-BI) type method [80]-[87], the application of higher-order absorbing boundary conditions (ABCs) [38, 39], [88]-[117] or the use of the perfectly matched layer (PML) [118]-[131]. The FEM-BI type method is considered more rigorous than the other methods since it applies exact boundary conditions through Green's function. However, the FEM-BI type method produces a fully populated matrix subsystem, which causes difficulties in storing and

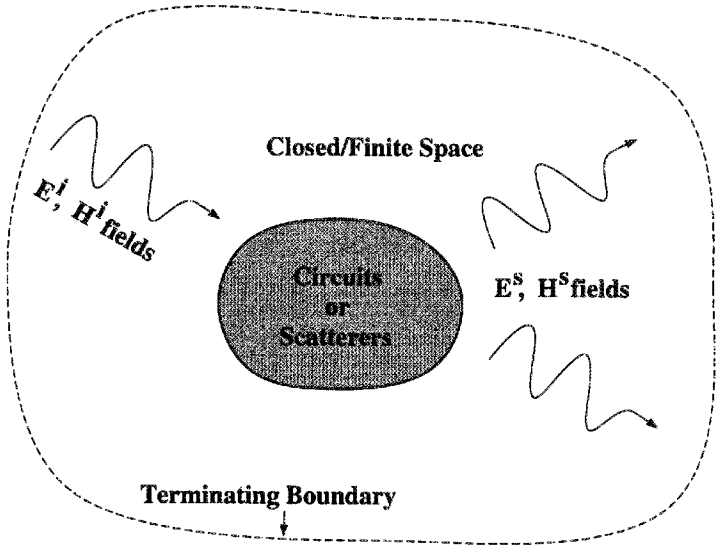
solving large systems of equations.

Compared to the global boundary condition of the FEM-BI method, the ABC and PML type approaches produce local boundary conditions. The locality of the boundary conditions contributes to the generation of a sparse matrix system and offers great advantages in storing and solving the matrix system. In higher order ABCs, accurate prediction of the local curvature of the wave front is crucial to the overall accuracy as well as convergence of numerical methods. Unfortunately, however, the curvature of the wave front is, in general, unknown and therefore the accuracy of ABCs is limited by its poor approximation of the tangential electromagnetic fields at the outer surface. Also, ABCs reveal difficulties in the termination of the inhomogeneous boundary value problems since they were developed for homogeneous open spaces with plane wave incidence. Moreover, these ABCs do not provide optimum design procedures for a given error tolerance except by increasing the separation distance between the object and the boundary surface, which will eventually intensify the computational burden and require the use of higher order boundary conditions. As a results, the ABC type approaches lead to inferior numerical performance such as slow convergence and spurious reflections at the outer boundary.

With these observations, the design of absorbing material with the perfectly matched layer (PML) concept becomes an alternate way of terminating outer boundaries and thus simulating infinite space. The PML technique is based on two essential ideas, namely impedance matching at the interface and damping of the waves in the material for least amount of reflections coming from the finite thickness of the material. These types of absorbing layers, in general, produce a symmetric FEM matrix and provide flexible design parameters in order to satisfy a given error bound. Moreover, the PML type absorber can be placed within fractions of a wavelength



(a)



(b)

Figure 2.11: Treatment of open boundary problem: (a) Original open boundary problem, (b) Equivalent closed/finite boundary problem.

without sacrificing accuracy. Among the known artificial absorbers, Berenger's PML has demonstrated excellent performance for 2D and 3D problems in the context of a finite difference time domain technique. However, Berenger's PML equations are non-Maxwellian and suffer from instabilities when applied to layered inhomogeneous problems. Furthermore, the implementation of the absorber in the context of FEM is not straightforward [131].

Another similar type of PML has been presented recently, introducing uniaxial anisotropic materials to implement a non-reflecting interface for an arbitrary angle of incidence. Such an interface condition with a material having broadband characteristics, satisfies Maxwell's equations and has been implemented using anisotropic material. For example, the characteristics of the anisotropic absorbing material facing $z = constant$ plane are diagonal tensors:

$$[\epsilon]^{PML} = \begin{bmatrix} p & 0 & 0 \\ 0 & p & 0 \\ 0 & 0 & 1/p \end{bmatrix} \epsilon, \tag{2.46}$$

$$[\mu]^{PML} = \begin{bmatrix} p & 0 & 0 \\ 0 & p & 0 \\ 0 & 0 & 1/p \end{bmatrix} \mu \tag{2.47}$$

where $p = \alpha - \jmath\beta$ and the values of α and β have to be carefully chosen for best numerical performance. In theory, the above PML material yields a reflectionless interface for an arbitrary angle of incidence, polarization, and frequency. However, the performance of the PML concept in the FEM context reveals several practical difficulties, including the difficulty of choosing appropriate α and β for various structures, slow convergence in the iterative matrix solver, and direction dependency of the material.

In contrast to the above anisotropic absorber, an isotropic artificial absorber has also been devised to simulate a free space buffer layer. This type of material is not independent of the angle of incidence. However, its loss mechanism is clearly understood and thus provides a well defined design procedure for optimum performance. Also, it can be designed to be a PML absorber for well defined field distributions as inside a waveguide. Furthermore, the absorber can be easily incorporated into an existing FEM code and renders much faster convergence compared to the anisotropic one. In view of the advantages of using the isotropic absorber, in the following subsections, design procedures are presented the absorber, for MMIC and waveguide applications.

2.10.1 Isotropic Absorbers for MMIC Applications

Transmission line structures, as commonly encountered in usual MIC/MMIC applications such as microstrip, CPW and slot line, support quasi-TEM or hybrid type modes, as opposed to the TEM nature of plane waves excited in free space. Moreover, when there are circuit discontinuities, evanescent or higher order modes are excited which leak power into the substrate. As a result, design of an appropriate layer capable of absorbing all of these waves, including the dominant mode, is a rather challenging task.

In our application of the absorber to MMICs, we find three different situations. The first is encountered when the absorber is used as a termination boundary in transmission lines to simulate a matched load, the second occurs when we need to simulate free space, and the third corresponds to the termination of a substrate. For the design of effective absorbing layers for the above three cases, matching the wave

impedances at the absorber interface will result in a non-reflecting surface:

$$Z_r = Z_{AA}$$

where Z_r and Z_{AA} are the wave impedances in the dielectric and the artificial absorber, respectively.

Since the wave impedance for a TEM wave is identical to the intrinsic impedance of the medium in which it propagates, matching the intrinsic impedances across the material-absorber interface is equivalent to matching the wave impedances. Similarly, in a homogeneous waveguide terminated with an artificial absorber, TE and TM mode wave impedances in both media are identical, if the intrinsic impedances are the same. Therefore for effective absorption and minimal reflection of the surface waves and higher order evanescent modes created by a circuit discontinuity, the intrinsic impedances at the absorber interface need to be matched. In addition, to avoid any secondary reflections at the end of the absorbing layer, the material parameters need to be optimized to maximize the attenuation of the waves transmitted into the absorber. This leads to complex values for the electric permittivity ($\epsilon_{AA} = \epsilon'_{AA} - j\epsilon''_{AA}$) and magnetic permeability ($\mu_{AA} = \mu'_{AA} - j\mu''_{AA}$) of the absorber with large imaginary parts.

Based on the above observations, the design procedure of the artificial absorbing layer interfacing a dielectric layer with ϵ_r and μ_r can be summarized as follows:

1. Choose the operating frequency ($f_o = c/\lambda_o$) and an arbitrary thickness of the absorber (δt).

2. Compute relative intrinsic impedance of the dielectric layer ($\tilde{\eta}_r = \sqrt{\mu_r/\epsilon_r}$).

3. Choose $Re(\epsilon_{AA}) = \epsilon_r$ and $Im(\epsilon_{AA})$ such that $Im(\epsilon_{AA}) \geq -\frac{1}{4\pi}(\frac{\lambda_o}{\delta t})\frac{1}{\tilde{\eta}_r}\ln(\alpha)$, where

α is the maximum magnitude of the reflected wave which can be tolerated at the interface.

4. Choose $\mu_{AA} = \tilde{\eta}_r^2 \epsilon_{AA}$ (impedance matching condition).

It is noted that even though the absorbing layer is designed under the assumption of normal incidence, the design procedure can be modified for the elimination of a wave incident from a certain angle.

2.10.2 Isotropic Absorbers for Waveguide Applications

In homogeneous waveguides where mode patterns are well defined, an isotropic absorber can be optimized to simulate an infinite waveguide. Since for each propagating mode at a certain frequency one can define an equivalent incident angle using ray optics, optimization of the absorber parameters to that particular angle of incidence can minimize the reflections at the interface. The thickness of the absorbing layer is chosen to provide enough attenuation of the waves in the absorbing material and to minimize the computational domain. The following steps summarize the design procedure for the isotropic absorber for a given mode (TE_{mn} or TM_{mn}) and a specific guided frequency (f_g). The a and b ($a \geq b$) are the waveguide dimensions and ϵ_r and μ_r are the relative permittivity and permeability, respectively, in the waveguide.

1. Choose an arbitrary thickness of the absorber (δt).

2. Compute relative intrinsic impedance of the waveguide material ($\tilde{\eta}_r = \sqrt{\mu_r/\epsilon_r}$). Usually, $\lambda_g/10$ is enough for δt.

3. Let $Re(\epsilon_{AA}) = Re(\epsilon_r)$ and $Im(\epsilon_{AA})$ such that $Im(\epsilon_{AA}) \geq -\frac{1}{4\pi}(\frac{\lambda_g}{\delta t})\frac{1}{\tilde{\eta}_r}\ln(\alpha)$, where α is the maximum magnitude of the reflected wave which can be tolerated at

the interface. [14]

4. Calculate μ_{AA} using the following equations, derived from the interface matching conditions for TE and TM wave incidence with angle θ_i

   - for TE_{mn} ($\{m,n \mid 0 \leq m,n < \infty \text{ and } m = n \neq 0\}$) modes,

   $$\mu_{AA} = \frac{\epsilon_{AA}\mu_r}{2\epsilon_r \cos^2\theta_i} + \sqrt{(\frac{\epsilon_{AA}\mu_r}{2\epsilon_r})^2 - (\mu_r \tan\theta_i)^2} \tag{2.48}$$

   - for TM_{mn} ($\{m,n \mid 1 \leq m,n < \infty\}$) modes,

   $$\mu_{AA} = \frac{\mu_r}{\epsilon_r \epsilon_{AA}}[\epsilon_r^2 \sin^2\theta_i + \epsilon_{AA}^2 \cos^2\theta_i] \tag{2.49}$$

   where $\theta_i = \cos^{-1}(\sqrt{1-(f_c/f)^2})$, $f_c = \frac{c_o}{2\sqrt{\epsilon_r\mu_r}}\sqrt{(\frac{m}{a})^2 + (\frac{n}{b})^2}$ and c_o is the speed of light in vacuum.

It is noted that even though the absorbing layer is designed for a specific mode at a given frequency, and that as a result it has narrow bandwidth characteristics, its performance under single mode operation can be maximized by adaptively changing the absorber parameters at each frequency. As a result, the application of the absorber to the frequency domain FEM can be easily optimized. For the evanescent modes below the cutoff frequency, the performance of the absorber in the context of the FEM cannot be easily evaluated. However, in practice, any instability effect has been observed in the evanescent mode region with the absorber. It should also be pointed out that the performance of the isotropic absorber near the cutoff frequency is degraded, as happens with other types of PML.

2.11 Passive Lumped Elements

In high-frequency high-speed circuits, the passive and active lumped elements constitute indispensable ingredients along with distributed circuits, while the sizes

[14] Even though one can choose a much larger value of $Im(\epsilon_{AA})$ than the criterion, it is not always advisable since it will require much higher discretization to model the highly varying fields inside the absorber.

of the lumped elements are negligible compared to that of the distributed network. In spite of their small size, in many cases, the lumped elements strongly interact with the surrounding environment, including the distributed circuits. As a result, it is very important to have a three-dimensional full-wave electromagnetic field characterization of the circuits having both distributed and lumped elements, and several investigations have recently been reported with time domain PDE techniques [132]-[143]. The incorporation of the lumped elements into the finite element method, however, has not been well understood, nor its effectiveness and possibilities assessed despite its importance. In this study, the passive lumped elements, such as resistors, inductors, and capacitors, are modeled in three-dimensional finite element techniques in two different manners.

The effect of the lumped elements can be implemented starting from the inhomogeneous wave equation:

$$\nabla \times \mu_r^{-1}(\nabla \times \mathbf{E}) - k_0^2 \epsilon_r \mathbf{E} = -j\omega \mathbf{J}_i. \tag{2.50}$$

Similar to the method given in section 2.3, Galerkin's procedure is applied to Eq. (2.50) on Hilbert space and the weak form is found as: for $j = 1, ..., n$,

$$\langle \mu_r^{-1} \nabla \times \mathbf{E}, \nabla \times \mathbf{Q}_j \rangle = -jk_0 Z_0 \langle \mathbf{Q}_j, \mathbf{J}_i \rangle + jk_0 Z_0 \oint_S (\mathbf{H} \times \mathbf{Q}_j) \cdot \hat{\mathbf{n}} dS \tag{2.51}$$

where the weighting functions, $\mathbf{Q} = \{\mathbf{Q}_1, \mathbf{Q}_2, \ldots, \mathbf{Q}_n\}^T \subset \mathcal{H}_2$, are defined on a Hilbert space and eventually the electric field, $\mathbf{E}$, will be also expanded on a Hilbert space, $\mathcal{H}_2$, with the same weighting function. Now, the lumped elements could be implemented through the two different methods discussed below, using the right hand side terms of Eq. (2.51). In the following two subsections, the detailed mathematical formulations will be discussed for the so-called volume current approach and surface impedance approach.

2.11.1 Volume Current Method

In this method, the first term in the right hand side of the Eq. (2.51) is utilized to incorporate lumped impedance elements:

$$\mathcal{I}_1 = -\jmath k_0 Z_0 \langle \mathbf{Q}_j, \mathbf{J}_i \rangle \quad \text{for j=1,...,n.} \tag{2.52}$$

where Z_0 is the free space intrinsic impedance.

In the above equation, the volume current density can be represented in terms of electric field and conductivity as:

$$\mathbf{J}_i = \sigma \mathbf{E} \tag{2.53}$$

where $\sigma = l/(Z_L s)$ and Z_L, s, and l represent, as shown in Figure 2.12, load impedance in ohms (Ω), cross-sectional area, and length of the load, respectively. After Eq. (2.53) is combined into Eq. (2.52), we obtain

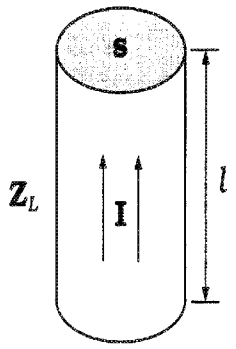


Figure 2.12: Impedance load.

$$\mathcal{I}_1 = -\jmath k_0 Z_0 \frac{l}{Z_L s} \langle \mathbf{Q}_j, \mathbf{E} \rangle \quad \text{for j=1,...,n.} \tag{2.54}$$

Now, the electric field is expanded in Hilbert space based on tetrahedral elements as

$$\mathbf{E} = \sum_{i=1}^{6} x_i \mathbf{Q}_i \tag{2.55}$$

and as a result we have

$$\mathcal{I}_1 = -\jmath k_0 Z_0 \frac{l}{Z_L s} \sum_{i=1}^{6} x_i \langle \mathbf{Q}_j, \mathbf{Q}_i \rangle \quad \text{for j=1,...,n.} \tag{2.56}$$

If the impedance load is located on the i^{th} edge in a tetrahedron, the inner product between the basis and weighting functions becomes constant: $\langle \mathbf{Q}_j, \mathbf{Q}_i \rangle = \Delta V \delta_{ij}$, where ΔV is the volume of the load given as $\Delta V = sl$. Therefore, in most practical situations, Eq. (2.56) is simplified to

$$\mathcal{I}_1 = -\jmath k_0 Z_0 \frac{l^2}{Z_L} x_i. \tag{2.57}$$

This term only contributes to the diagonal terms, A_{ii}, in the FEM matrix [**A**] in Eq. (2.20).

2.11.2 Surface Impedance Method

The incorporation of the passive lumped elements into the finite element method can be also implemented using the surface integral term, the second term of the Eq. (2.51),

$$\mathcal{I}_2 = -\jmath k_0 Z_0 \oint_S (\mathbf{H} \times \mathbf{Q}_j) \cdot \hat{\mathbf{n}} dS \quad \text{for j=1,...,n.} \tag{2.58}$$

and the resistive sheet condition [144]:

$$\hat{\mathbf{n}} \times (\hat{\mathbf{n}} \times \mathbf{E}) = -R \ \hat{\mathbf{n}} \times (\mathbf{H}^+ - \mathbf{H}^-) \tag{2.59}$$

where $\mathbf{H}^+$ and $\mathbf{H}^-$ are magnetic fields defined on the surface s^+ and s^-, respectively, as shown in Fig. 2.13. For a thin dielectric layer of thickness t, the equivalent resistive sheet having surface resistivity R ($\Omega/\square$) can be derived from the equivalent polarization current [145, 146]:

$$R = \frac{Z_0}{\jmath k_0 (\epsilon_r - 1) t}. \tag{2.60}$$

For a thin dielectric layer, $\mathcal{I}_2$ can be split into two terms for the upper and lower surfaces:

$$\mathcal{I}_2 = -\jmath k_0 Z_0 \int_{S^+} \mathbf{Q}_j \cdot (\hat{\mathbf{n}} \times \mathbf{H}^+) \ dS + \int_{S^-} \mathbf{Q}_j \cdot (\hat{\mathbf{n}} \times \mathbf{H}^-) \ dS \tag{2.61}$$

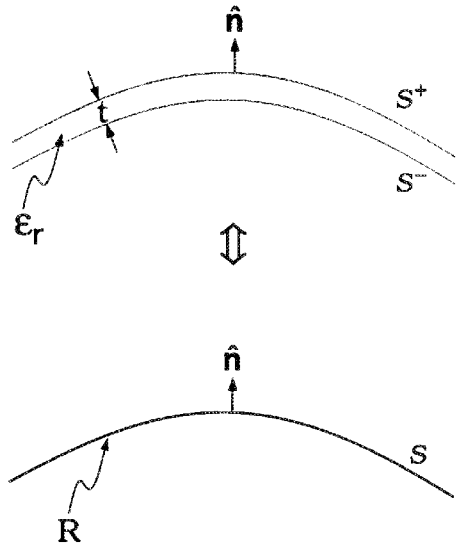


Figure 2.13: Resistive sheet and equivalent thin dielectric layer.

and on the assumption that $k_0 t \ll 1$, it is further reduced to

$$\mathcal{I}_2 = -\jmath k_0 Z_0 \int_{S+} \mathbf{Q}_j \cdot [\hat{\mathbf{n}} \times (\mathbf{H}^+ - \mathbf{H}^-)] \; dS. \tag{2.62}$$

Now, Eq. (2.59) is substituted into the above, yielding

$$\mathcal{I}_2 = -\jmath k_0 Z_0 \int_S \frac{1}{R} (\hat{\mathbf{n}} \times \mathbf{Q}_j) \cdot (\hat{\mathbf{n}} \times \mathbf{E}) \; dS \tag{2.63}$$

and its discretized form on Hilbert space with the edge basis function is found as:

$$\mathcal{I}_2 = -\jmath k_0 Z_0 \sum_i x_i \int_S \frac{1}{R} (\hat{\mathbf{n}} \times \mathbf{Q}_j) \cdot (\hat{\mathbf{n}} \times \mathbf{Q}_i) \; dS \quad \text{for j=1,...,n.} \tag{2.64}$$

This term is evaluated numerically for a given surface and its resistivity.

To a first order, this equation can be used to simulate the presence of a thin dielectric layer by choosing an equivalent resistive sheet having resistivity R. Alternatively, a resistive sheet may be equivalently replaced by a thin dielectric layer

having thickness t and a relative permittivity of

$$\epsilon_r = 1 - j\frac{Z_0}{k_0 t R}. \tag{2.65}$$

Note that with the latter approach, for resistive lumped elements, a small volume of dielectric material is allocated to have the equivalent dielectric constant. This approach can be also expanded to capacitive and reactive elements by substituting the Z_L for load impedance for the resistivity R in Eq. (2.65). In this study, both approaches are implemented, and the performance and accuracy are compared.

CHAPTER III

VALIDATION AND PARALLELIZATION

3.1 Introduction

Presented in this chapter is validation of the edge-based finite element method by means of the generalized eigenvalue problems for lossless cavities. The motivation behind of using the eigenvalue problem to validate the FEM is the fact that the excitation and the eigenvalue problems share the identical matrices, and the exact solutions can be found for certain eigenvalue problems. As a result, by examining the accuracy of the eigenvalues for various problems, the developed edge-based FEM code can be validated. Furthermore, the validated FEM code is parallelized on the distributed memory parallel computer (the IBM SP2) using the message passing paradigm (MPL). Two types of parallelization schemes are examined in this study and the performance of each scheme is investigated in depth. Having done the validation and parallelization of the FEM, a design guideline for artificial absorbing materials is introduced for waveguide and MMIC applications, and its effectiveness is verified with several examples. The use of absorbing materials is crucial for simulation of open boundary problems as proved whole throughout the thesis.

3.2 Eigenvalue Problems

Seeking the solutions of eigenvalue problem using source-free Maxwell's equations allows basic understanding of the electromagnetic characteristics of a given geometry. In particular, the eigenvalues and the corresponding eigenvectors provide complete signature of the fundamental electromagnetic properties of the structure. Any field distributions in a cavity or guiding structure can be represented as a linear combination of eigenvectors. Strictly speaking, any closed non-radiating geometries support discrete eigenvalues and eigenvectors, in contrast to continuous counterparts of the open or radiating problems. For example, the eigenvalues and the eigenvectors of a lossless cavity, whether it is homogeneous or not, represent resonant frequencies and their mode distributions. On the other hand, the eigenvalues of lossy cavity become complex numbers and thus correspond to complex modes having attenuating as well as non-attenuating components.

When there are no excitation mechanisms in domain Ω, the generalized eigenvalue equation can be derived from Eq. (2.20) as:

$$[\mathbf{U}][\mathbf{x}] = \lambda[\mathbf{V}][\mathbf{x}] \tag{3.1}$$

where

$$[\mathbf{U}] = \bigcup_{e=1}^{M}[\mathbf{U}^e] \quad \text{and} \quad [\mathbf{V}] = \bigcup_{e=1}^{M}[\mathbf{V}^e]$$

and the matrix entries of the submatrices $[\mathbf{U}^e]$ and $[\mathbf{V}^e]$ are determined as given in Eq. (2.21) and Eq. (2.22):

$$\begin{aligned} U_{ij}^e &= \langle \mu_r^{-1} \nabla \times \mathbf{W}_i, \nabla \times \mathbf{W}_j \rangle \\ V_{ij}^e &= \langle \epsilon_r \mathbf{W}_i, \mathbf{W}_j \rangle. \end{aligned}$$

Here, the eigenvalue λ is given as k_0^2 which is a square of the propagation constant. Note that for lossless isotropic material the matrix [**U**] is symmetric, and [**V**] is symmetric and positive definite since the basis functions $\mathbf{W}_i$ are independent. Using the fact that any positive definite matrix can be decomposed into two triangular matrices, [**V**] can be written as

$$[\mathbf{V}] = [\mathbf{C}][\mathbf{C}]^T \tag{3.2}$$

where [**C**] is the triangular matrix. Now, the original eigenvalue equation is transformed into

$$[\tilde{\mathbf{U}}][\tilde{\mathbf{x}}] = \lambda[\tilde{\mathbf{x}}] \tag{3.3}$$

where $[\tilde{\mathbf{U}}] = [\mathbf{C}]^{-1}[\mathbf{U}][\mathbf{C}]^{-T}$ and $[\tilde{\mathbf{x}}] = [\mathbf{C}]^T[\mathbf{x}]$. Therefore, for lossless isotropic medium, all the eigenvalues λ become real numbers, since the matrix $[\tilde{\mathbf{U}}]$ is symmetric. The solution of the generalized eigenvalue equation could be found using the iterative method, such as Lanczos method, to take advantage of the sparsity of the FEM matrix. In this study, however, all of the eigenvalues including zeros are found using the standard factorization method. [1]

Herein, the eigenvalues are calculated for several different types of homogeneous as well as inhomogeneous cavities, and the numerical results are compared with the analytic solution, if available, to validate the developed edge-based finite element method. When analytic solution is not obtainable for inhomogeneous problem, the excitation problem, having exactly the same configuration except the source, is solved to compare the resonant frequency. In many practical applications, the solution of the excitation problem can be found more accurately and efficiently than that of the eigenvalue problem with aid of efficient linear equation solver. Furthermore,

[1] There are standard EISPACK routines, such as RSG and QZHES, for generalized eigenvalue problems.

to characterize unknown dielectric material having complex dielectric constant, the excitation problems are solved and compared with the eigenvalues to extract real and imaginary parts of the permittivity.

3.2.1 Lossless Cavities

(a) Empty Rectangular Cavity

As a first step toward validating the developed edge-based FEM code, the generalized eigenvalue problem is solved for rectangular cavity shown in Fig. 3.1. The resonant frequency, f_o^{mnp}, of each mode in the cavity can be also obtained as

$$f_o^{mnp} = \frac{1}{2\pi\sqrt{\epsilon\mu}}\sqrt{(\frac{m\pi}{a})^2 + (\frac{n\pi}{b})^2 + (\frac{p\pi}{c})^2}$$

where $\{m, n, p \mid m \geq 0, n \geq 0, p > 0, m = n \neq 0\}$ for TE^z and $\{m, n, p \mid m \geq 1, n \geq 1, p \geq 0\}$ for TM^z mode. As is summarized in Table 3.1 and Table 3.2, the FEM-computed eigenvalues are accurate within ± 1.0 % error bound for all the cases listed in the tables. Note that the degenerated modes having the same resonant frequency are also predicted very accurately in both cases. Furthermore, it is also observed that the total number of zero eigenvalues is equal to the number of internal FEM nodes as discussed in Section 2.7.3, and more importantly, no spurious modes are detected in the eigenvalue spectrum.

With the remarkable accuracy obtained by the edge-based FEM for the empty cavities, eigenvalues for inhomogeneous cavities having dielectric material are computed in the below.

(b) Partially-Filled Cavity

Having been proved the accuracy of the edge-based FEM for the simplest cavity structures, the accuracy of the FEM is tested for more complicated geometries. In this study, the eigenvalues of the partially-filled cavity, as shown in Fig. 3.2, with

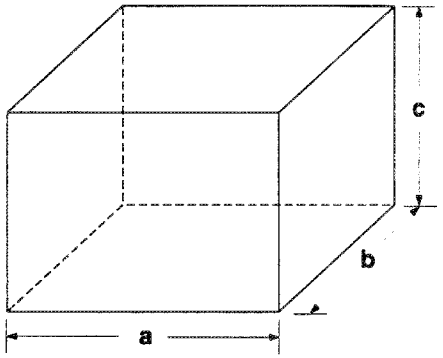


Figure 3.1: Rectangular cavity having PEC walls and dimensions a, b, and c in x-, y-, and z-direction, respectively.

mode (m,n,p)	f_0 [GHz]		error [%]
	Analytic	FEM	
(1,1,0)	21.2133	21.2090	0.02
(1,0,1)	21.2133	21.2090	0.02
(0,1,1)	21.2133	21.2090	0.02
(1,1,1)	25.9808	26.1173	−0.53
(2,1,0)	33.5409	33.3714	0.51
(0,2,1)	33.5409	33.3714	0.51
(1,0,2)	33.5409	33.3714	0.51
(1,1,2)	36.7424	36.7696	−0.07
(2,1,1)	36.7424	36.7696	−0.07
(1,2,1)	36.7424	36.7696	−0.07
(2,2,0)	42.4266	42.2972	0.30
(2,0,2)	42.4266	42.2972	0.30
(0,2,2)	42.4266	42.2972	0.30

Table 3.1: First few eigenvalues of an empty rectangular cavity having $a = b = c = 10$ mm.

mode (m,n,p)	f_0 [GHz]		error [%]
	Analytic	FEM	
(1,1,0)	6.2500	6.2543	−0.07
(1,0,1)	8.3852	8.3766	0.10
(2,1,0)	9.0141	9.0040	0.11
(0,1,1)	9.0141	9.0336	−0.21
(1,1,1)	9.7627	9.7799	−0.18
(2,0,1)	10.6064	10.5696	0.35
(1,2,0)	10.6799	10.7353	−0.52
(2,1,1)	11.7261	11.7313	−0.04

Table 3.2: First few eigenvalues of an empty rectangular cavity having $a = 40$, $b = 30$, and $c = 20$ mm.

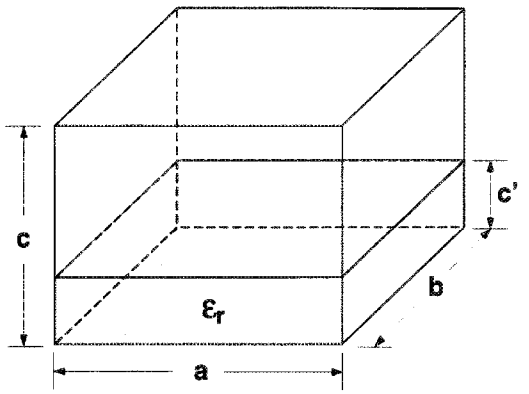


Figure 3.2: Partially-filled rectangular cavity having dielectric material with ϵ_r and thickness c'.

two different dielectric material are computed and the results are compared with the analytic data.

As tabulated in Table 3.3 and Table 3.4, the first few of the FEM-computed eigenvalues for $\epsilon_r = 2.5$ and 12.9 are listed and revealed excellent agreement with the analytic data. It is observed that the error for the higher dielectric constant material shows slightly higher than that of the smaller one mainly due to the numerical discretization error. Similar to the previous empty cavity examples, there are no spurious modes in the whole frequency spectrum.

(c) Loaded Rectangular Cavity

As a last example of the lossless eigenvalue problem, dielectric cube having dimension a', b', and c' with dielectric constant ϵ_r is placed at the center of the cavity bottom plane as shown in Fig. 3.3. In this section, to quantify the effect of the size of the dielectric cube and its dielectric constant on the resonant frequency of the dominant mode, the dielectric constant ϵ_r is varied from 1 to 50, and the filling

mode (m,n,p)	f_0 [GHz]		error [%]
	Analytic	FEM	
LSM_{111}	5.6736	5.6469	0.47
LSE_{101}	7.8617	7.8578	0.05
LSM_{211}	7.9493	7.8826	0.84
LSE_{011}	8.4350	8.4087	0.31
LSM_{121}	8.8660	8.8654	0.01
LSE_{111}	9.1125	9.1031	0.10
LSM_{121}	9.2044	9.1104	1.02
LSE_{201}	9.8677	9.8513	0.17
LSM_{311}	10.3579	10.2504	1.04
LSM_{311}	10.4876	10.3985	0.85

Table 3.3: First few eigenvalues of a partially-filled rectangular cavity having $a = 40$, $b = 30$, $c = 20$, $c' = 5$ mm, and $\epsilon_r = 2.5$.

mode (m,n,p)	f_0 [GHz]		error [%]
	Analytic	FEM	
LSM_{111}	3.9809	3.9302	1.27
LSM_{211}	4.5625	4.5074	1.20
LSE_{101}	4.6704	4.6360	0.74
LSM_{121}	4.8837	4.8416	0.86
LSE_{011}	4.8977	4.8418	1.14
LSE_{111}	5.1405	5.1169	0.46
LSM_{311}	5.2048	5.1684	0.70
LSM_{221}	5.2462	5.1988	0.90
LSE_{201}	5.4039	5.3750	0.53

Table 3.4: First few eigenvalues of a partially-filled rectangular cavity having $a = 40$, $b = 30$, $c = 20$, $c' = 5$ mm, and $\epsilon_r = 12.9$.

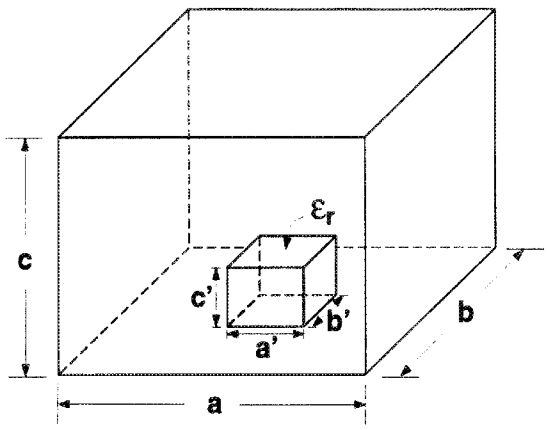


Figure 3.3: Rectangular cavity having dielectric cube at the center of the cavity bottom having dielectric constant ϵ_r and a', b', and c' in x-, y-, and z-dimension, respectively.

factor r has been varied from 0.1 to 0.25, where r is defined as:

$$r = (a'/a) = (b'/b) = (c'/c). \tag{3.4}$$

In addition, the frequency shift due to the dielectric material is defined as:

$$\delta f = \mid 1 - \frac{\tilde{f}_0}{f_0} \mid \times 100 \ \ [\%] \tag{3.5}$$

where f_0 is the resonant frequency of the dominant mode for the empty cavity, while $\tilde{f}_0$ is the shifted resonant frequency of the dielectric loaded cavity. For instance, $\epsilon_r = 1$ or $r = 0$ corresponds to empty cavity, while $r = 1.0$ to fully filled cavity.

With the above definitions, the resonant frequencies of the dielectric loaded cavities are computed and summarized in Fig. 3.4. As shown in the figure, the variation of δf as a function of ϵ_r is clearly revealed for several different size of the material. As can be observed, as the permittivity ϵ_r or filling factor r increases, the resonant frequency of the loaded cavity $\tilde{f}_0$ becomes lower and in turn δf increases.

Therefore, for a given dielectric configuration, it is straightforward to predict the resonant frequency of the loaded cavity. In fact, for any unknown dielectric

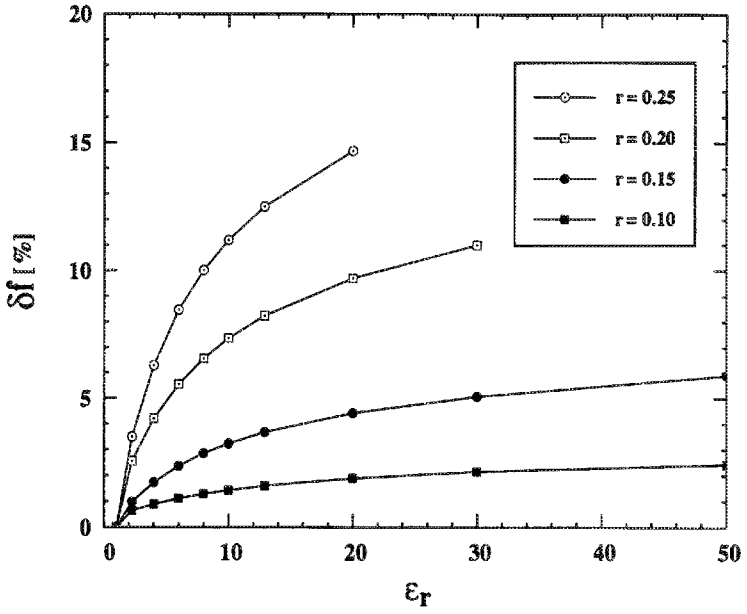


Figure 3.4: Variation of the resonant frequency of the dominant mode for various size and ϵ_r of the dielectric material.

material, it is possible to accurately determine the dielectric constant of the material by comparing the resonant frequencies of the empty and loaded cavities, and looking up the curves in Fig. 3.4. When the material has complex permittivity, the real part can be extracted by measuring the shift of the resonant frequency, while the imaginary part can be deduced from the quality factor of the loaded cavity as will be discussed in the next section. It should be pointed out that the accuracy of the resonant frequencies of the dielectric loaded cavity has been found within 2 % by comparing the data obtained from the excitation problem.

3.2.2 Lossy Cavities

When a lossy dielectric material having complex permittivity ϵ_r is placed inside of a cavity, the eigenvalues become complex numbers and the quality factor of the cavity becomes finite as illustrate in Fig. 3.5, in contrast to infinity for lossless case.

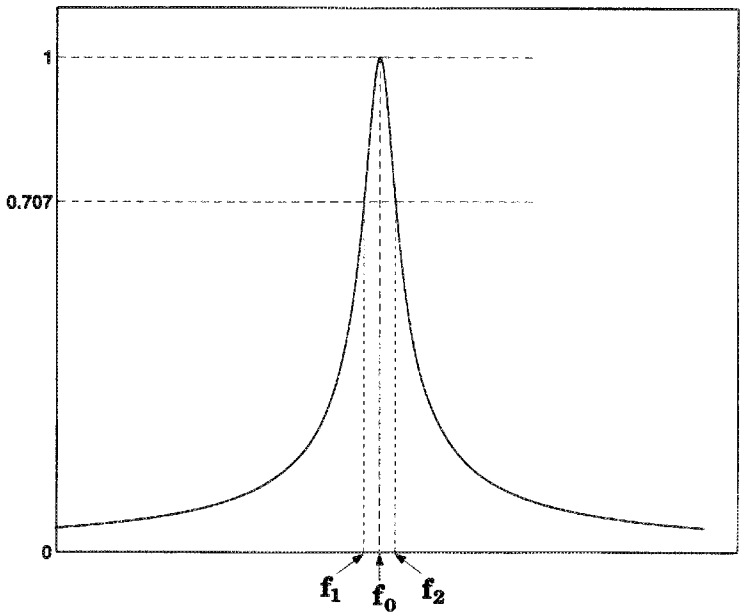


Figure 3.5: Typical resonance curve of a lossy cavity. The quality factor Q is defined based on the center frequency, f_0, and two adjacent frequency points, f_1 and f_2.

In general, the quality factor (Q-factor) of a lossy cavity is defined as:

$$Q = \frac{f_0}{BW} \tag{3.6}$$

where the frequency f_0 is the center frequency. As illustrated in Fig. 3.5, the bandwidth BW is defined as $BW = f_2 - f_1$, where f_1 and f_2 are the frequency points correspond to $1/\sqrt{2}$ of the maximum.

In this study, various lossy dielectric materials having different level of loss are modeled using the excitation problem and the intensity of the electric fields are measured to determine the resonant frequency and Q-factor. As can be observed in Table 3.5, the resonant frequencies of the lossy dielectric loaded cavities are mainly determined by the real part of the permittivity, while the imaginary part contributes to finite Q-factors. Note that the Q-factor is linearly proportional to the loss tangent, $\tan\delta$, of the material.

r	ϵ_r	$\tan\delta$	f_0 [GHz]	BW [MHz]	Q
0.1	$6.0 + j0.1$	0.0167	6.2140	1.09	5700
0.25	$2.25 + j0.0$	0.0	6.0717	0.0	∞
0.25	$2.25 + j0.001$	0.00044	6.0717	0.222	27350
0.25	$2.25 + j0.01$	0.0044	6.0717	2.24	2710
0.25	$2.25 + j0.1$	0.044	6.0717	22.3	272
0.25	$6.0 + j0.0$	0.0	5.8044	0.0	∞
0.25	$6.0 + j0.01$	0.00167	5.8044	0.93	6241
0.25	$6.0 + j0.1$	0.0167	5.8044	9.29	624.8
0.25	$12.9 + j0.0$	0.0	5.6032	0.0	∞
0.25	$12.9 + j0.001$	0.000078	5.6032	0.038	147454
0.25	$12.9 + j0.01$	0.00078	5.6032	0.38	14745
0.25	$12.9 + j0.1$	0.0078	5.6032	3.9	1455

Table 3.5: Resonant frequencies and Q-factors for lossy dielectric loaded cavities having various amount of losses.

3.2.3 Summary

In this section, the validity and accuracy of the edge-based finite element method is proved using the generalized eigenvalue problems. In particular, the eigenvalues of the empty as well as dielectric loaded cavities are accurately predicted, and more importantly, no spurious modes are observed. In addition, it is found that the number of zero eigenvalues are equal to the number of internal tetrahedral nodes. For inverse problem of predicting the dielectric properties of a material, variety of dielectric configurations are examined. Finally, it is demonstrated that when there are lossy dielectric material in a cavity, the real and imaginary parts of the permittivity can be extracted from the resonance curves.

3.3 Parallelization

3.3.1 Motivations

The three dimensional edge-based vector FEM is well established and applied for the characterization of many 2D and 3D circuits and interconnects which contain complicated dielectric and metallic configurations [33, 34, 28]. It is proved to be very

accurate, computationally inexpensive and highly parallelizable [20]. In this section, two different types of parallelization schemes, parallelization of the linear equation solver and task parallelization, based on distributed memory machine (IBM SP2) are presented for the 3D-FEM code and the performance of each scheme is closely examined. For the implementation of efficient parallel FEM code, message passing paradigm using MPL (Message Passing Library) has been utilized.

In the following section, the parallelization schemes for BiCG routine and the task parallelization are presented and the performances of two approaches are examined. The first strategy, the parallelization of the BiCG routine, is based upon the observation that more than 90% of the execution time of the FEM code is taken by the routine. As a result, development of an efficient linear equation solver can reduce overall computation time. On the other hand, the second approach, the task parallelization scheme, is evolved from the fact that the FEM is a frequency domain technique. When the frequency domain technique is used to characterize any high frequency interconnects, many repetitive calculations at each different frequency point are required, which is time consuming. However, the FEM system of equations for different frequency points are independent each other and can be solved simultaneously as presented in the next section. It has been found that the task parallelization strategy can provide an almost linearly scalable FEM code on a distributed memory parallel computer and it renders fast and efficient computation of the circuit parameters.

3.3.2 Parallelization Strategies

(a) Parallelization of the Linear Equation Solver : [A][x] = [b]

In most of the practical problems, the generation of the matrix **[A]** requires much less computational effort compare to solving the linear or eigenvalue equation. As

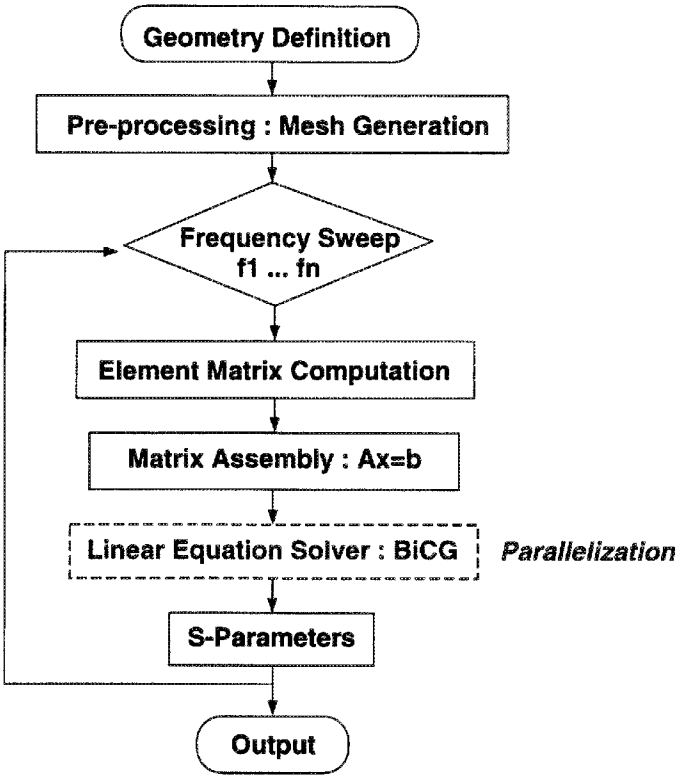


Figure 3.6: Parallelization of the linear equation solver, BiCG method, in the FEM scheme.

a result, efficient and fast method of solving the equation can speedup the whole solution process. In this study, many efforts are devoted to implement parallelized BiCG method as illustrated in Fig. 3.6. As is well known, the BiCG method with diagonal preconditioning requires one matrix-vector multiplication in every iteration. The matrix [**A**] is computed once in the beginning of the solution process and used repeatedly during the iterations, while the unknown coefficient vector [**x**] has to be renewed in every iteration. Furthermore, to maximize the usage of the storage space and to minimize the number of floating point operations in the iterative solver, such as the BICG, only non-zero matrix entries and its integer coordinates are stored.

For parallelization of the matrix-vector multiplication, the matrix [**A**] computed

by the master node is partitioned into smaller matrices $[\mathbf{A}_i]$ such that

$$[\mathbf{A}] = \cup_{i=1}^{N} [\mathbf{A}_i] \tag{3.7}$$

where N is the number of nodes (CPUs), and each partitioned matrix $[\mathbf{A}_i]$ is distributed to all the other slave nodes in the beginning of the BiCG procedure. Since for a given frequency the matrix $[\mathbf{A}]$ is fixed during the BiCG iteration process, it can be broadcasted once and for all. This is the step 1 in Fig. 3.7 . On the other hand, the vector $[\mathbf{x}]$ which will be multiplied to the matrix $[\mathbf{A}]$ has to be distributed in the every iteration (step 2). As indicated in Fig. 3.7 each node performs partial matrix-vector multiplication simultaneously (step 3) and the results are collected to produce the final result (step 4).

The following shows an example of broadcasting the matrix $[\mathbf{A}]$ using the message passing paradigm (MPL):

```
CALL MP_BCAST(A,MsgLngth,Source,AllGroup)
```

In a typical distributed memory machine, every node is connected each other using fast internal network, called switch in IBM SP2, and the internal network has its capacity (bandwidth) and resulting communication overhead. In our SP2 system, the bandwidth of the switch is 35 Mbyte/sec and the communication overhead due to the latency is 40 μsec. Communication buffer size is also limited. As a result, when the size of the matrix or message exceeds a certain limit, the performance of the switch degraded remarkably. To overcome the communication overhead and acquire maximum speed, the size of the matrix should be sufficiently big. In the following example, multiple `Send` and `Block Receive` method is used to overcome the bandwidth limitation:

```
IF (TaskID.EQ.0) THEN ← master node
```

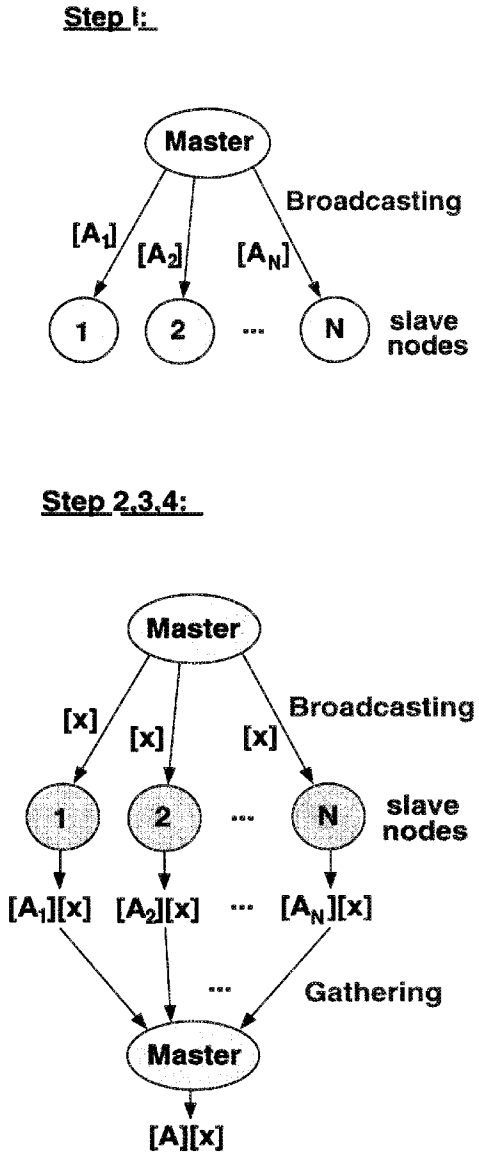


Figure 3.7: Parallelization of the matrix-vector multiplication. Step 1: broadcast the partitioned FEM matrix $[A_i]$. Step 2: broadcast the vector $[x]$ in every iteration. Step 3: perform partial matrix-vector multiplication $[A_i][x]$ on each machine, where $[A] = \cup [A_i]$ for $i = 1, \ldots, N$. N is the number of slave nodes. Step 4: gather the results to form $[b]$.

```
      DO I = 1,NumOfTask-1
         Destination = I
         Ntype = I
         CALL MP_SEND(A,MsgLngth,Destination,Ntype,MessageID)
      ENDDO
   ELSEIF(TaskID.NE.0) THEN ← slave nodes
      Source= 0
      CALL MP_BRECV(A,MsgLngth,Source,TaskID,MessageID)
   ENDIF
```

Note that to ensure the synchronism between the source (master node) and destination (slave nodes), the block receive subroutine (MP_BRECV) has been used. After the [**A**] has been broadcasted, the vector [x] is also broadcasted in a similar way in every iteration. Now, each small portion of the matrix-vector multiplication is carried out in each node simultaneously and the final results are gathered to form the resulting vector [**b**]. In the following an example of the parallel pseudo-Fortran code for matrix-vector multiplication is shown:

```
   N = INT(MatrixSize/NumberOfTask)
   Nstart = TaskID*N + 1
   Nstop = Nstart + N - 1
   DO I = Nstart,Nstop ← matrix-vector multiplication at each node
      VI = [A_i][x]
   ENDDO
   CALL MP_GATHER(VI,b,BlockLength,Destination,AllGroup)
```

In the above example, the sparsity of the matrix [**A**] can be fully utilized by using the

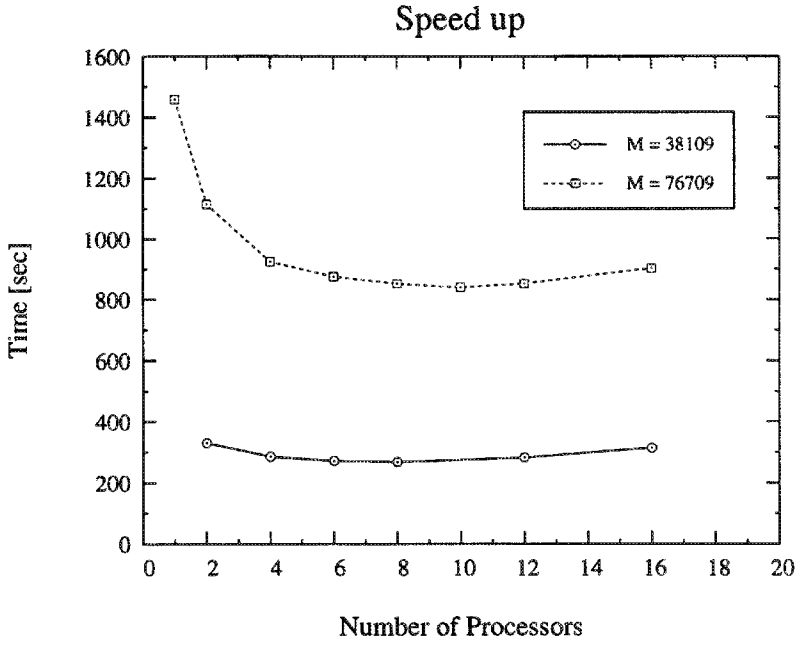


Figure 3.8: Speedup curves of the parallel matrix-vector multiplication for two different problem sizes. M indicates the number of unknowns.

indirect index scheme with possible adverse effect such as inefficient memory/cache access.

Fig. 3.8 illustrates the performance of the FEM code with the parallelized linear equation solver for two different problem sizes M. As can be observed in the figure, the larger problem size has better performance improvement compare to the smaller one. This is mainly due to the communication overhead and task size, that is, the advantage of the "divide-and-conquer" strategy is offset by the communication latency for M=38190 case.

(b) Parallelization of the Tasks

The previous approach has gained marginal performance improvement due to the limited bandwidth and communication latency. To overcome these difficulties,

task/frequency parallelization strategy is explored in this section. This strategy is based upon the property of the frequency domain method such that the system of linear equations of each frequency point is independent each other. As a result, for a given problem the set of linear equations for different frequency points can be constructed and solved independently and simultaneously to obtain the complete spectrum of the scattering parameters over the broad range of frequency.

In this scheme the computational tasks which correspond to different frequency points are distributed among the different nodes, and the solutions are found simultaneously. Indeed, as shown in Fig. 3.9, each slave node is assigned to have different set of problem corresponding to different frequency and the element matrix generation, matrix assembly and the solution process of the matrix equation using the BiCG are performed concurrently on each node. This type of parallelization scheme is often called "embarrassingly parallelized" version of the FEM code, since it only requires minimum parallelization skill, but can provide perfect and almost linearly scalable parallelization performance as illustrated in Fig. 3.10.

It is worth mentioning that this approach is equivalent to using many separate computers in a fast network without requiring any communication between them. This would not be considered as a real parallelization in a strict sense, but it can be beneficial to the users of the parallel computers and provides a truly scalable parallelization strategy.

Following shows an example of the pseudo-Fortran code for the task parallelization scheme:

```
DO I = 1, NFRQ, NUMTSK
   IFREQ = TASKID + I
   IF(IFREQ.GT.NFRQ) STOP
```

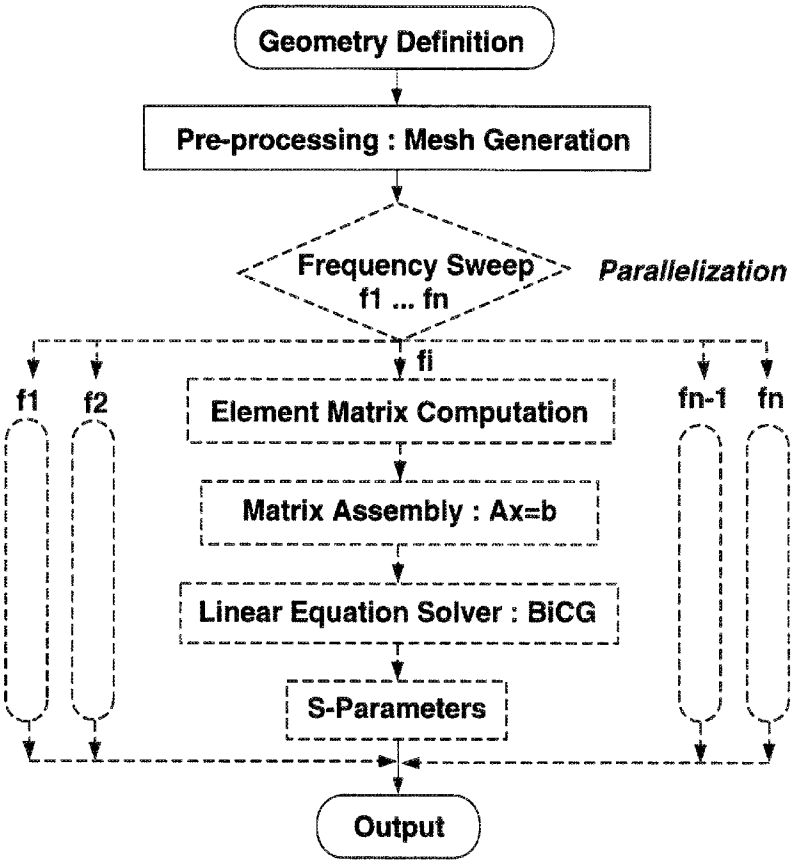


Figure 3.9: The concept of the task parallelization.

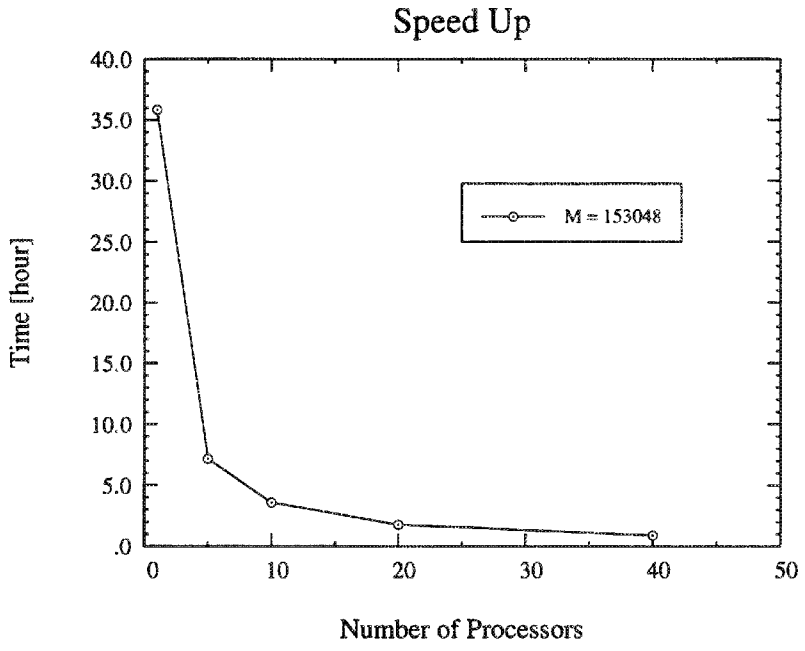


Figure 3.10: Speedup curve for the task parallelization.

```
    ⋮
    (Serial FEM code for each frequency point)
    ⋮
ENDDO
```

3.3.3 Discussion

To find more effective parallelization strategy for the frequency domain finite element method, two different approaches are studied and the performance of those approaches are measured in terms of total amount of time required to solve a given problem. With the first approach, the parallelization of the matrix-vector multiplication, two different problems having size M equals 38109 and 76709 are solved. As shown in Fig. 3.8, simply increasing the number of CPUs does not guarantee

reduced execution time, especially for the smaller problem size. On the other hand, increasing the number of nodes for the larger problem size renders slight performance improvement with diminishing return after a certain point. The number of nodes for maximum speedup depends on the problem size as clearly shown in this study. Note that using more slave nodes over the optimum number causes degraded performance due to the heavy communication overhead and limited buffer size, and thus offsets the advantage of using multiple nodes. Hence, the optimum number of CPUs for a given problem size depends on the capacity of the communication network, CPU speed, the performance of the switch (bandwidth), and the buffer size.

Having the marginal perofomance improvement with the first approach, the frequency parallelization strategy is devised and its performance is fully examined. As discussed in the previous section, this approach is proved to give truly linearly scalable parallel FEM code due to the negligible amount of communication between the processors. Its simplicity and minimum required parallelization effort are the main advantages of this approach, and even more importantly, this strategy allows scalable parallel code and can be applied to many other applications.

3.4 Performance of the Artificial Absorbers

In this section, the performance of an artificial absorber presented in section 2.10 is examined in the context of the finite element method for characterization of microwave and millimeter-wave circuits having inhomogeneous dielectric configurations. As an artificial absorber, a medium with designed complex permittivity and permeability is used to introduce a controllable amount of loss. Such an absorber can be effectively placed near circuit discontinuities to absorb the excited dominant and higher order modes as well as surface waves propagating in the substrate. In order to

minimize the unwanted reflections at the dielectric-absorber interface, the absorber is designed to provide impedance matching at the interface allowing the waves to be effectively transmitted through the interface and subsequently attenuated while they propagate into the absorber. To validate the concept of impedance matching between an inhomogeneous dielectric half space and an artificial absorbing layer in various situations, six different circuit configurations are examined including microstrip, CPW and waveguide structures. It has been found that a judicious choice of the artificial absorber makes it possible to reduce reflections less than -40 dB.

3.4.1 Microstrip Thru Line

A 50 Ω microstrip line is designed on 635 μm thick substrate and the computational domain is terminated with PEC surfaces as shown in Fig. 3.11. The microstrip line is terminated with two absorber layers to simulate infinite transmission line. The position of the mesh termination surfaces is chosen to prevent the excitation of a waveguide mode in the frequency range of interest (low frequency region) and the side walls are placed $4H_1$ apart from the microstrip edge. As a result, the microstrip line has only dominant quasi-TEM mode below 22 GHz. Above 22 GHz, however, the overall structure starts to support the dominant as well as higher order waveguide modes depend on operating frequency in addition to the microstrip mode. The absorbers are designed to have two parts. The upper portion of the absorber is chosen to have $\epsilon_1 = \mu_1 = 1.0 + j3.0$ so that it is matched to the air side. The imaginary part of the absorber is chosen to introduce enough losses for the wave propagating in the absorber. For the lower layer of the absorber, the material constants are chosen as $\epsilon_2 = 3.4 + j10.0$ and $\mu_2 = 1.0 + j2.9412$ so that its intrinsic impedance is matched to the substrate impedance ($\eta_2 = \eta_o/\sqrt{\epsilon_r} = \eta_r$).

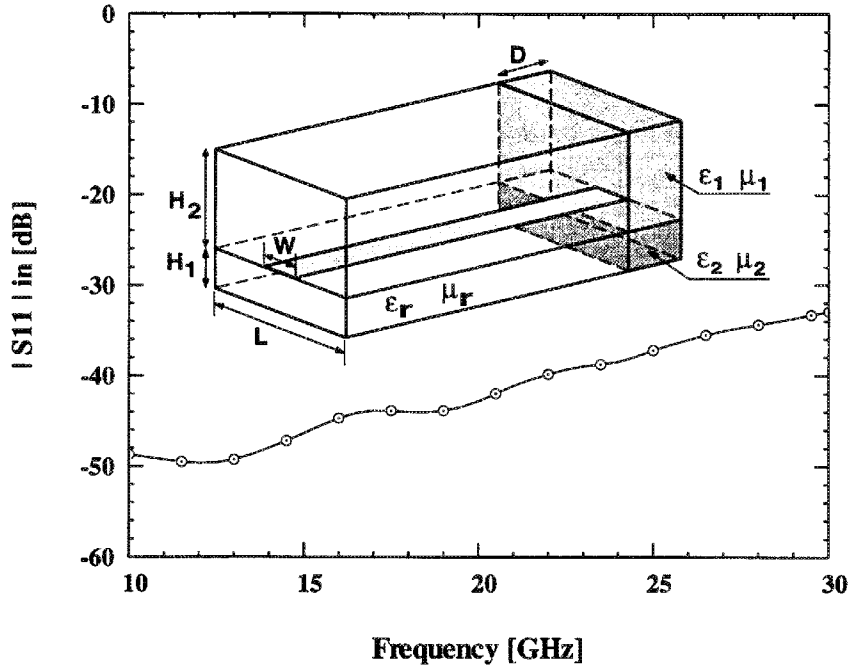


Figure 3.11: Computed return loss for the microstrip line terminated with artificial absorbers. Geometrical and material factors : $L = 6.38$ mm, $W = 1.3$ mm, $D = 5.0$ mm, $H_1 = 0.635$ mm, $H_2 = 3.365$ mm, $\epsilon_r = 3.4$, $\mu_r = 1.0$, $\epsilon_1 = 1.0 + j3.0$, $\mu_1 = 1.0 + j3.0$, $\epsilon_2 = 3.4 + j10.0$, and $\mu_2 = 1.0 + j2.9412$

As observed in Fig. 3.11, the reflection from the absorbing layer is smaller than -40 dB up to 22 GHz. Considering the electrical thickness of the absorbing layer ($D = 0.27\lambda_g$ at 10 GHz) and the hybrid nature of the excited fields, the performance of the absorber is excellent in very broad frequency range. The gradual increase in the $|S_{11}|$ is mainly due to insufficient discretization of the FEM mesh at high frequency end of the spectrum. The dependency of the reflections on the discretization is examined further in later sections.

3.4.2 Microstrip Junction Terminated with Absorber

To measure the performance of the absorbing layer in the close vicinity of circuit discontinuities, the absorber is placed at three different positions from the microstrip

impedance junction as shown in Fig. 3.12. The thickness of the absorber T is fixed to be $0.16\lambda_g$ (λ_g at 10 GHz) and the return loss is computed while varying the distance D from $0.08\lambda_g$ to $0.32\lambda_g$. As presented in Fig. 3.12, the computed $|S_{11}|$ data for three different absorber positions agree very well with the data derived by the finite difference time domain method within 1.0 dB in the whole frequency region. It is quite remarkable to obtain the above accuracy with isotropic absorbing layer having only $0.16\lambda_g$ thickness and placed at a distance less than $0.1\lambda_g$ from the discontinuity. It is worth mentioning that for a given circuit if only $|S_{11}|$ data is needed to be computed, all the other ports can be terminated by placing appropriate absorbers and measure the reflection coefficient at the designated port, resulting in significant reduction of required computational cost.

3.4.3 CPW Series Stub

In this section, the performance of the isotropic absorber is examined under non-TEM type field distribution. In particular, a CPW series stub as shown in Fig. 3.13 is designed and absorbers are placed at four different places to evaluate the performance of the absorber. Since CPW supports non-TEM mode and its discontinuity generates evanescent and surface waves, placing the absorber in the close vicinity of the discontinuity can indicate the performance of the absorber under non-ideal condition.

To simulate an infinitely long CPW thru line, absorbing layers are designed and placed at the end of the line as a matched load. The thickness of the absorber is fixed to $0.24\lambda_g$ (λ_g at 20 GHz). The return loss is calculated for the CPW series stub as a function of the position of the absorber ($D = 0.093\lambda_g$, $0.213\lambda_g$, $0.334\lambda_g$, and $0.574\lambda_g$. As shown in Fig. 3.13, the calculated reflection coefficients converge

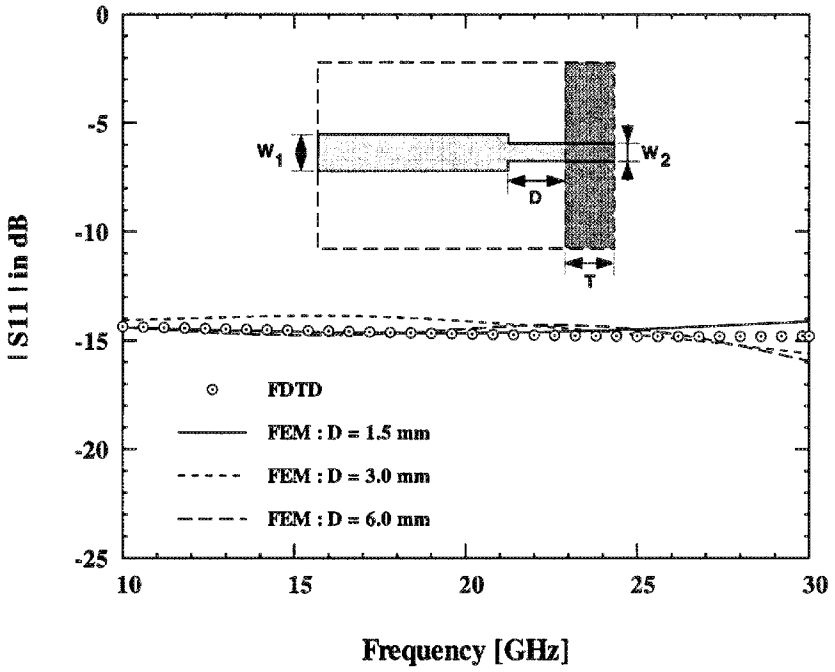


Figure 3.12: Computed return loss for the microstrip junction terminated with artificial absorbers. Absorbers are placed at the side and top walls also in addition to the termination end. Geometrical factors : $W_1 = 1.3$mm, $W_2 = 0.6$mm, and $T = 3.0$mm. The thickness and the dielectric constant of the substrate are $H = 0.635$mm and $\epsilon_r = 3.4$. The absorbers at the end are chosen as : $\epsilon_1 = 1.0 + j15.0$ and $\mu_1 = 1.0 + j15.0$ for the air side and $\epsilon_2 = 3.4 + j15.0$ and $\mu_2 = 1.0 + j4.412$ for the dielectric side.

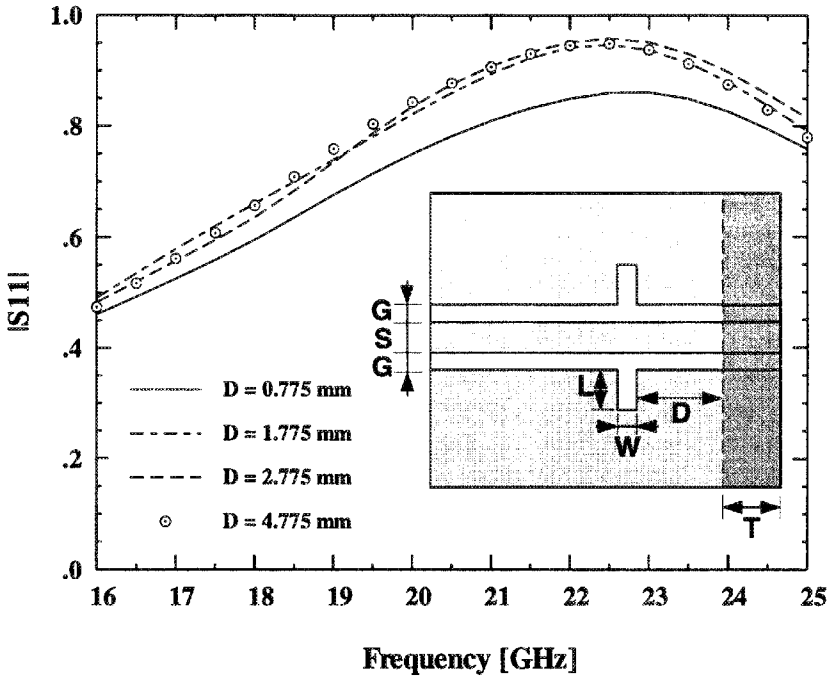


Figure 3.13: Computed return loss for the CPW series stub terminated with artificial absorbers (closed structure) at 4 different positions. Geometrical factors: $G = 0.225$mm, $S = 0.45$mm, $L = 1.35$mm, $W = 0.225$mm, and $T = 2.0$mm. The thickness and the dielectric constant of the substrate are $H = 0.635$mm and $\epsilon_r = 9.9$. The absorbers at the end are chosen as : $\epsilon_1 = 1.0 + j15.0$ and $\mu_1 = 1.0 + j15.0$ for the air side and $\epsilon_2 = 9.9 + j20.0$ and $\mu_2 = 1.0 + j2.02$ for the dielectric side.

rapidly as the distance between the CPW series stub and the absorber increases. Compare to $0.1\lambda_g$ of the previous microstrip case, the absorbers have to be placed slightly further ($0.2\lambda_g$) in CPW case due to the non-TEM type field distribution. It should be noted that a proper position of an absorber to simulate an infinite line or non-reflecting surface is dependent on the field distribution as can be seen in the case of the microstrip junction and CPW series stub.

3.4.4 CPW Series Stub: Open Structure

For the simulation of an open structure, the absorbing layers are placed on top and side walls of the circuit in addition to the termination end as shown in Fig. 3.14.

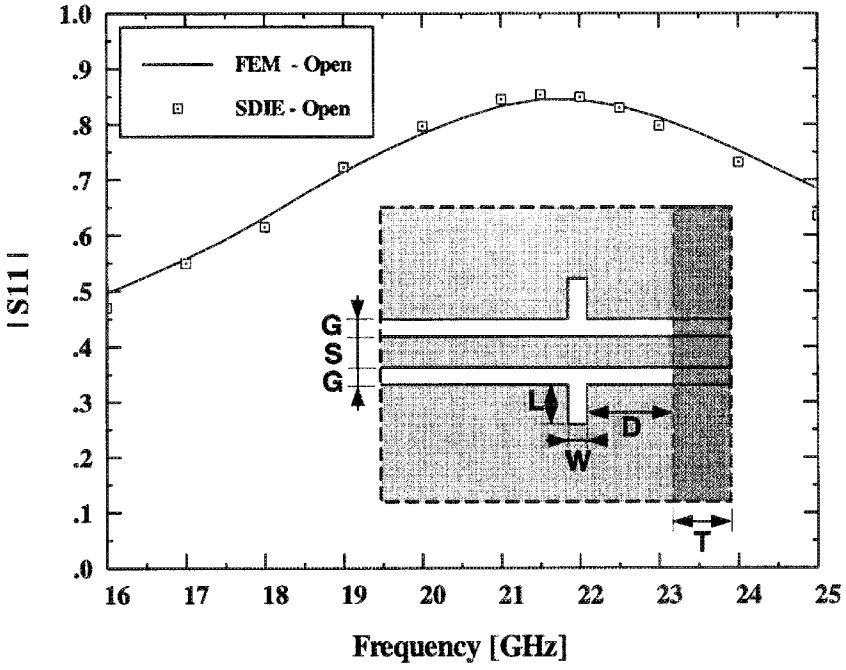


Figure 3.14: Computed return loss for the CPW series stub terminated with artificial absorbers (open structure). Geometrical factors: $G = 0.225$mm, $S = 0.45$mm, $L = 1.35$mm, $W = 0.225$mm, $D = 1.775$mm and $T = 2.0$mm. The thickness and the dielectric constant of the substrate are $H = 0.635$mm and $\epsilon_r = 9.9$. The absorbers at the end are chosen as : $\epsilon_1 = 1.0 + j15.0$ and $\mu_1 = 1.0 + j15.0$ for the air side and $\epsilon_2 = 9.9 + j20.0$ and $\mu_2 = 1.0 + j2.02$ for the dielectric side.

In this example, the absorbing layer having thickness T (= 2.0 mm = $0.32\lambda_g$ at f_0 = 20 GHz) is placed in the distance D (= 1.775 mm = $0.28\lambda_g$) from the discontinuity. The distance D is chosen to minimize the computational domain while maintaining the required accuracy (refer to Fig. 3.13). The computed results reveal excellent agreement with the data obtained from the space domain integral equation technique [147]. Even though the thickness of the absorber is 2.0 mm in this case, it can be reduced further by increasing the amount of loss in the material. Increasing the mesh density also contributes to the improvement of the accuracy due to the smaller numerical errors.

3.4.5 Waveguide Absorber

To verify the concept and the performance of the isotropic waveguide absorber, the design equations of the absorber presented in section 2.10 is implemented. The designed isotropic material is placed in a waveguide as shown in Fig. 3.15 and the dominant TE_{10} mode is excited. In contrast to the absorber used in the previous sections, the permittivity and permeability of the waveguide absorber are a function of frequency and excited mode in the waveguide.

The amount of reflections from the absorbing layer is measured using the standing wave patterns in the waveguide similar to the microstrip and CPW cases. As shown in the figure, the reflection coefficient in the whole frequency range is below -30 to -40 dB except in the immediate vicinity of the 3.15 GHz which is the cutoff frequency of the dominant TE_{10} mode. The gradual increase of $|S_{11}|$ in the higher frequency region is mainly owing to the insufficient discretization. Since the amount of reflections at the absorber interface is zero, one can further reduce the numerical reflections at the interface by increasing the mesh density and by adopting smooth

transition of mesh in the computational domain especially at the material interface. In our simulations the mesh sizes in x-, y-, and z-direction (δx, δy, and δz) are varied in the absorber region as indicated in the figure. As can be observed, the amount of reflected waves at the absorber interface is decreasing as the mesh size in each direction decreases, in particular, in x-direction (δx).

As another example, to investigate the performance of designed waveguide absorber in close vicinity of discontinuities in a waveguide, a 3-dimensional obstacle is placed inside of a waveguide as illustrated in Fig 3.16. As shown in the figure, the width (d_1), length (d_2), and height (d_3) of the conducting cube are 9.0 mm, 9.0 mm, and 6.0 mm, respectively, and it is placed at the center of the waveguide. The waveguide has been operated in the dominant mode region ($f_c^{TE_{10}} = 6.56$ GHz and $f_c^{TE_{20}} = 13.12$ GHz) and the absorber is placed at the end of the waveguide at 11.0 mm (= 0.168 λ_g at 8 GHz) away from the cube. The computed result using the FEM is compared with the measurement in [148] and reveals very good agreement. Note that the thickness of the absorber is chosen to be 5.0 mm (= $0.076\lambda_g$ at 8 GHz) and δx, δy, and δz in the absorber layer are 0.5 mm, 1.386 mm, and 1.04 mm, respectively.

3.4.6 Summary

In this section, the application of the artificial absorber to microwave and millimeter-wave structures have been investigated. The design concept of the artificial absorber through the matching of the intrinsic impedances has been found simple and effective. Due to the loss mechanism of the absorber, the artificial absorbing layer can suppress higher order modes as well as the dominant mode in the guided wave structures. Furthermore, incorporation of the concept of the absorber

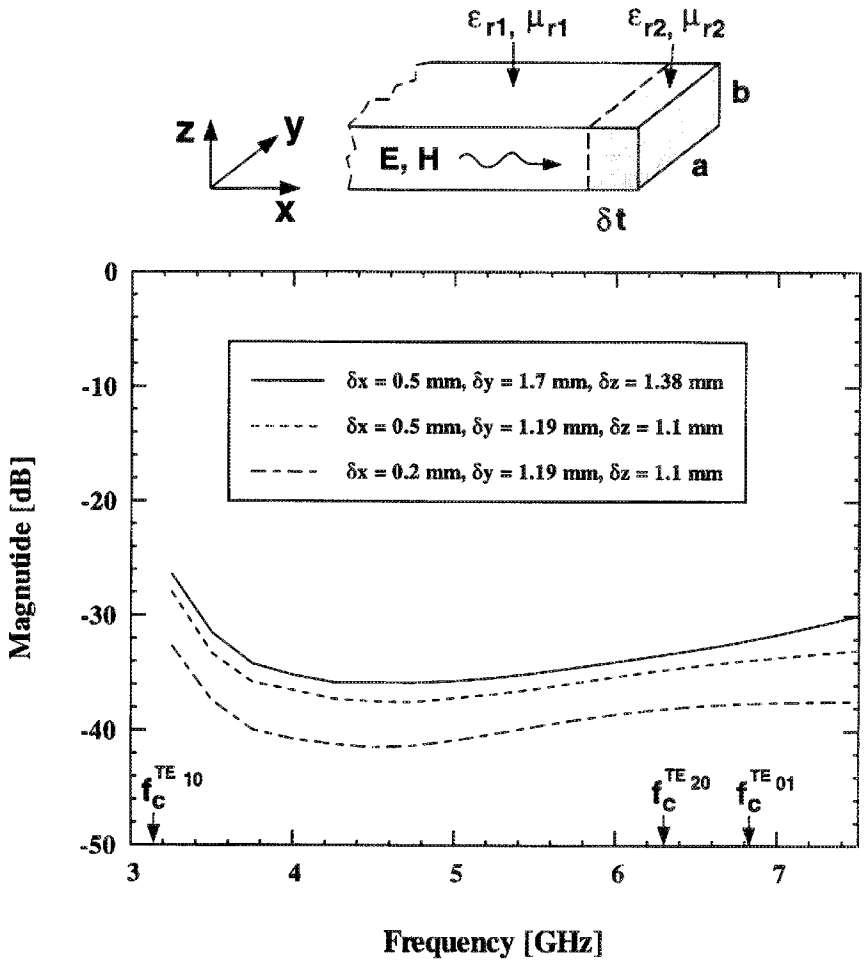


Figure 3.15: Computed reflection coefficient of the artificial absorber in a waveguide designed for absorption of the dominant TE_{10} mode as a function of mesh size (δx, δy, and δz) in the absorber region. Geometrical and material parameters of the waveguide: $a = 47.6$ mm, $b = 22.0$ mm, $\epsilon_{r1} = 1.0$, and $\mu_{r1} = 1.0$. The thickness of the absorber, δt, is $0.041\lambda_g$ (5.0 mm) at 4.0 GHz. $f_c^{TE_{10}}$, $f_c^{TE_{20}}$, and $f_c^{TE_{01}}$ are the cutoff frequency of each mode.

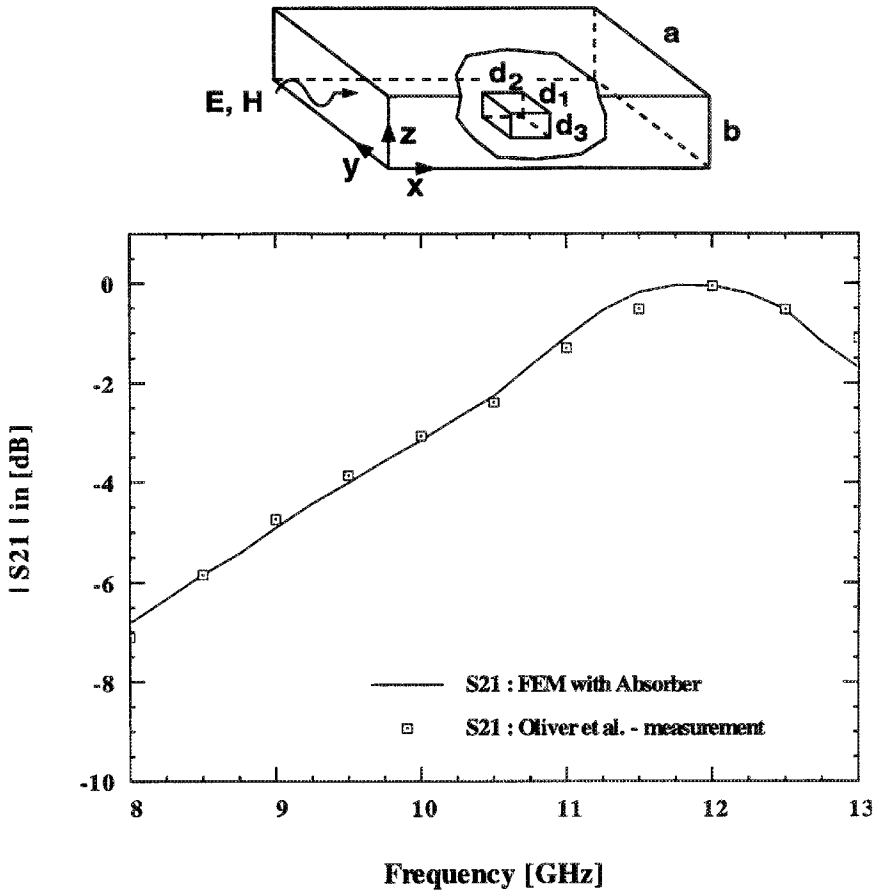


Figure 3.16: Computed transmission coefficient for a conducting cube of dimensions $d_1 = d_2 = 9.0$ mm and $d_3 = 6.0$ mm. The width and height of the waveguide: $a = 22.86$ mm and $b = 10.16$ mm. The thickness of the absorber at the end of the waveguide is fixed to 5.0 mm which is $0.06\lambda_g$ at 8.0 GHz.

into the existing FEM code is straightforward and does not require additional effort. The use of the isotropic absorber does not impose any degradation of the matrix condition number in contrast to the usual ABC's. Application of the absorbing layer also renders the possibility of alleviating the computational burden by reducing the computational domain.

3.5 Conclusions

This chapter has presented the validation of edge-based finite element method using the generalized eigenvalue problems for lossless cavity. The eigenvalues for homogeneous and inhomogeneous cavities are found accurately within 1% error, and more importantly no spurious solutions are observed. After the validation, the FEM code is parallelized on the distributed memory machine, the IBM SP2, and two different types of parallelization strategies are examined. In particular, the task parallelization scheme is found to give linearly scalable performance improvement. Finally, a design procedure of the isotropic artificial absorbing layer is presented and its performance in various MMIC and waveguide applications are thoroughly investigated. The absorbing material is crucial for open boundary problems frequently encountered in many MIC/MMICs and waveguide applications.

CHAPTER IV

PLANAR/NON-PLANAR HIGH FREQUENCY INTERCONNECTS

4.1 Introduction

As has been pointed out by Montgomery [149] in 1989, Microwave Integrated Circuit (MIC) and Monolithic Microwave Integrated Circuit (MMIC) packages remain a performance and cost challenge in many applications. In the past, the microwave industry has treated the packaging of circuits as a necessary and rather obvious step to be taken after the completion of the circuit design cycle. Such an approach was heavily concerned with the thermal and mechanical properties of the package, but ignored important electrical effects which could dominate circuit performance. As a result, package interference made design cycles very costly and many times unsuccessful.

It has been only recently that current R&D in industry and government laboratories has initiated an effort to address the critical problems of packaging in a way which links electrical performance with thermal and mechanical properties [150]. MIC and MMIC packages that are capable of good performance at frequencies as high as 60 GHz need to have small volume, low weight, microstrip or coplanar line compatibility, and most important, they should exhibit negligible electrical interference including low insertion and return losses.

For these packages to acquire some of the characteristics described above, special provisions need to be made during circuit design and layout stages. Specifically, in order to achieve lower weight/volume and reduce cost, designs lead to block and layered configurations where each layer performs a separate function. This design approach results in high density circuits where a large number of interconnects are printed on electrically small surface areas and communicate through the substrate in a direct through-via fashion or electromagnetically through appropriately etched apertures. In a circuit environment of this complexity, parasitic effects such as radiation and cross talk are intensified, thus making the interconnection problem very critical [151]. In order to reduce these effects with circuit layout compensations, accurate modeling tools are needed which can provide the exact correlation between circuit parasitics and geometrical characteristics. The establishment of a multi-layered multi-task monolithic circuit technology presumes a computer-aided design capability far more powerful and versatile than any presently commercially available. Furthermore, it requires a combination of tools varying from static to dynamic and from time to frequency domains, and the needs for a dynamically reconfigurable computational environment becomes more and more important as advancing technologies lead to increasingly complex geometries.

As a response, this study presents frequency domain characterizations of a few of the most commonly found planar/non-planar interconnect elements in a multi-layered circuit environment. Vertical transitions through apertures have been characterized in the past [151]-[156] and have been found to provide an efficient broadband bandpass RF connection. However, these transitions, due to their bandpass character, cut any low frequency or DC component which may need to propagate vertically to other layers, along with the RF signal as happens in detectors and mixers. In

such cases, direct interconnections through via holes are introduced along with their parasitic effects which, if not well understood, can degrade electrical performance to unacceptable levels.

One example of such a simple but yet vital interconnection is a via used for ground potential equalization in monolithic circuits where more than one ground planes is utilized. In many configurations, grounded CPW lines are unintentionally created and thus lead to the excitation of parallel plate waveguide modes which, strong as they are, couple various parts of the circuit and introduce high levels of parasitic radiation [157]. One technique to suppress these modes is the use of vias which connect the ground planes printed on opposite sides of the substrate layer. In practical implementations, more than one via is needed, perhaps as many as five to ten per guided wavelength, leading to long structures of inductive elements periodically placed around the circuitry. While this configuration nearly equalizes the ground potentials, it can also excite Floquet waveguide modes that tend to propagate along the via structure and couple to the rest of the circuitry strongly and destructively. Such waves can turn a well designed band pass filter into an element with unrecognizable characteristics.

Many recent efforts have emphasized the analytical and numerical evaluation of via inductance and capacitance using a variety of quasi-static and full wave techniques [131], [158]-[169]. In many cases, an equivalent circuit for the via is constructed through a scattering parameter evaluation, while in other cases, the inductance is computed from the total magnetic energy stored around the via or from the use of an excess inductance. While all of these techniques provide reasonable solutions, they disagree in the predicted values by as much as 10 to 30%. Unavoidably, this brings up the issue of which definition is more valid and, for that manner, more effective in

providing representative values.

Herein, vertical transitions of via-type are analyzed in the frequency domain and the performance under sinusoidal excitation is studied to provide a complete understanding of their electrical characteristics at low as well as high frequencies. In this study, the problems of printed circuit board via holes are analyzed through both the scattering parameters and the flux/current methods, and the results are compared in an effort to establish the relationship between the two techniques and evaluate their contributions [21]. In addition, several different types of planar/non-planar transition geometries including microstrip-to-CPW, CPW-to-slot, and CPW-to-waveguide are fully characterized. The modeling of these structures is performed with the edge-based 3-D finite element method and compared with the time domain FDTD data.

4.2 Microstrip Short Circuit

Fig. 4.1 shows a microstrip line printed on a 250 μm GaAs substrate. This line is short-circuited through a via hole which is etched in the substrate and then metallized to provide a DC connection to the ground. For the sake of simplicity the geometry of the via is considered cylindrical and not pyramidal as it is in high frequency monolithic applications. Fig. 4.2 shows the electrical characteristics of the microstrip short circuit vs. frequency evaluated by the FEM and demonstrate very good agreement with the FDTD data. The slight discrepancy between the values can be attributed to numerical errors associated with both techniques. As shown in Fig. 4.2, the via provides good ground to the line up to 5 GHz and fails gradually at frequencies above that.

Using the derived fields in the frequency domain, an equivalent inductance for

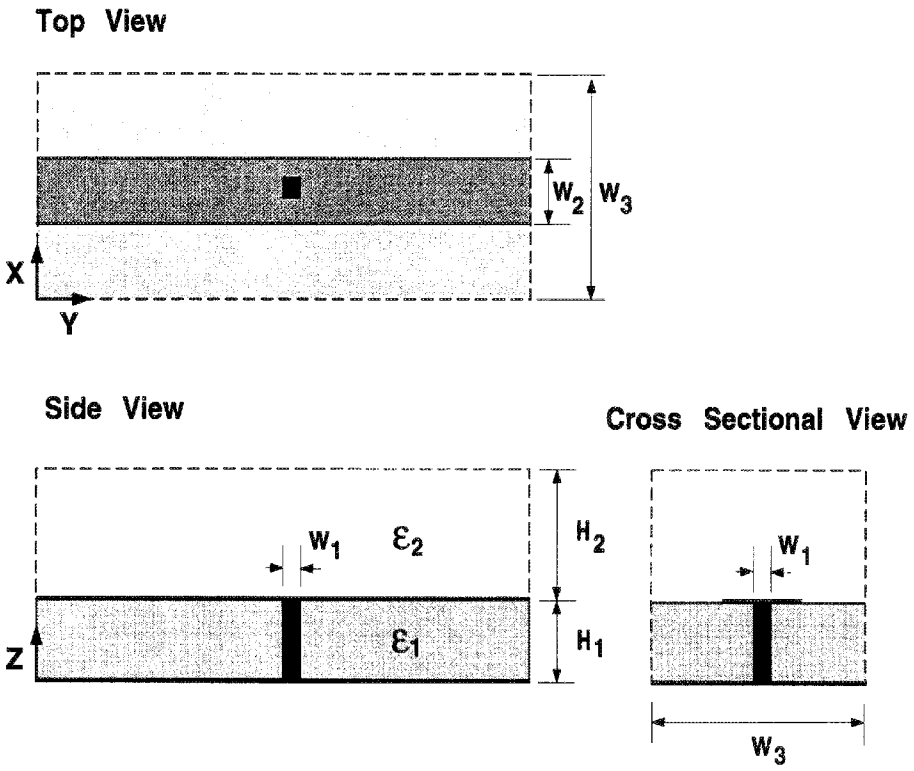


Figure 4.1: Geometry of a microstrip short circuit via hole at the center of the line. The dashed lines represent PEC walls to terminate FEM meshes. $W_1 = 85\mu$m, $W_2 = 600\mu$m, $W_3 = 1785\mu$m, $H_1 = 250\mu$m, $H_2 = 600\mu$m, $\epsilon_1 = 12.9$, and $\epsilon_2 = 1$. The dotted lines around the geometry represent the outer boundaries for FEM mesh termination.

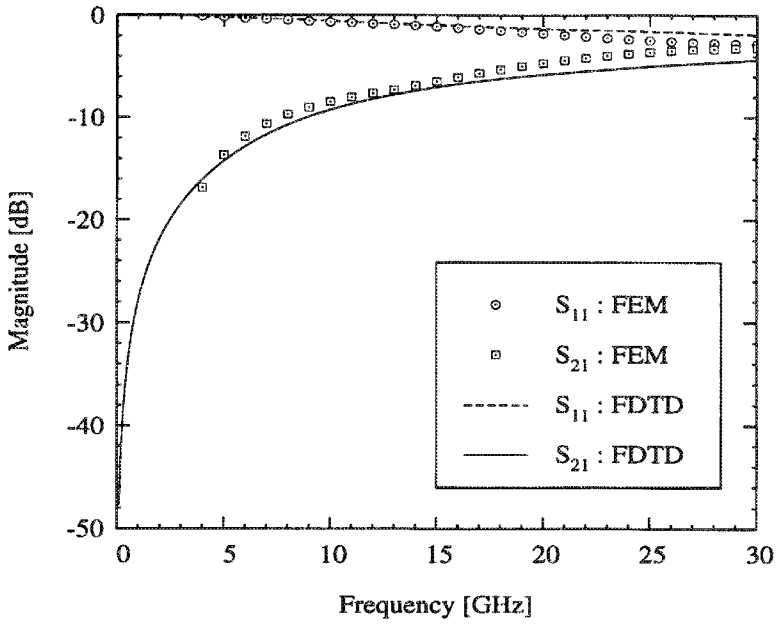


Figure 4.2: Scattering parameters for the via.

the via can be derived using two different approaches. One approach is based on the flux/current definition of inductance and is applied, herein, to the fields derived by the FEM. The other approach is based on the derivation of an appropriate equivalent circuit by fitting the derived scattering parameters in the frequency range of interest [168, 170]. For the geometries under study, a cascade of T-equivalent circuits, having two series capacitors and a shunt inductor, is used to model the discontinuity. It is found that the values of the capacitors are negligible ($\sim 10^{-14}$ F), thus reducing the equivalent circuit to a shunt inductor. This equivalent circuit approach is applied to scattering parameters derived by the FDTD method. The inductances derived by these two approaches are shown in Fig. 4.3 and exhibit very good agreement.

Let us now view the structure of Fig. 4.1 as two microstrip lines connected to the same ground via. It can be observed from Fig. 4.2 that $|S_{21}|$ of the microstrip short circuit increases with frequency, thus leading to unwanted coupling between the two

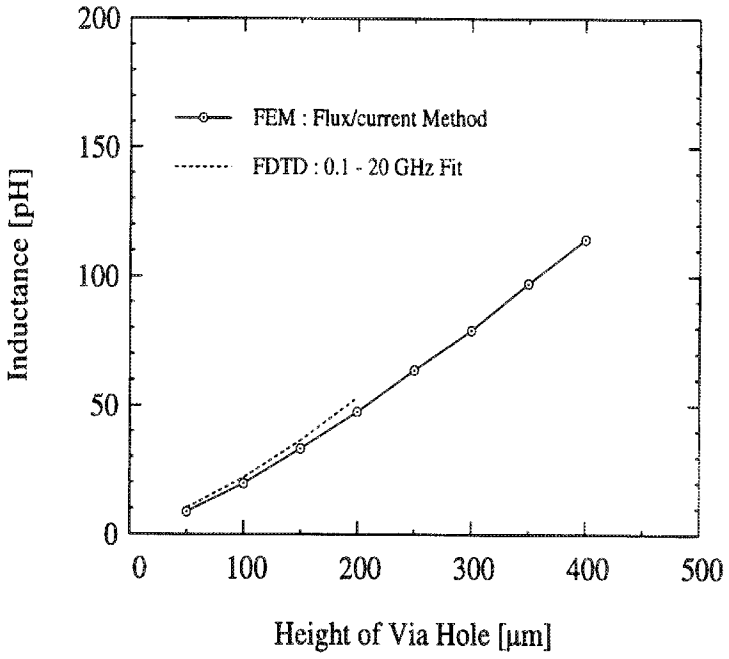


Figure 4.3: Inductance of the microstrip short circuit with via hole. The inductance is calculated using two different methods. In FEM, the flux density around the via is used (f = 10 GHz). In FDTD, however, the via inductance is extracted by fitting the derived S-parameters to a T-equivalent circuit.

microstrip line sections. In particular, the magnitude of the coupling coefficient S_{21} increases from -30 dB at 1.0 GHz to -4 dB at 30 GHz. The failure of the via to provide a good DC connection at higher frequencies is intensified by increasing the via height, as shown by the variation of the equivalent inductance and of the scattering parameters vs. via height (see Figs. 4.3 and 4.4).

The frequency dependence of the via characteristics shows up also in the distribution of the electric fields and the associated current flow, as illustrated in Fig. 4.5. At lower operating frequencies, where the via presents an almost perfect ground, the current flows from the microstrip line to ground through the wall of the via facing the feeding line. Under these frequency conditions, an almost zero current flow is observed toward the other connecting line, providing very high isolation between the

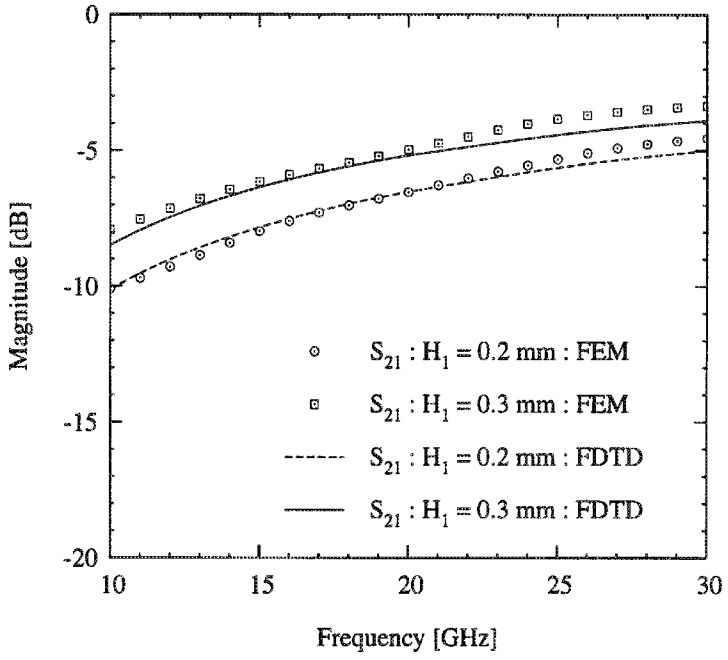
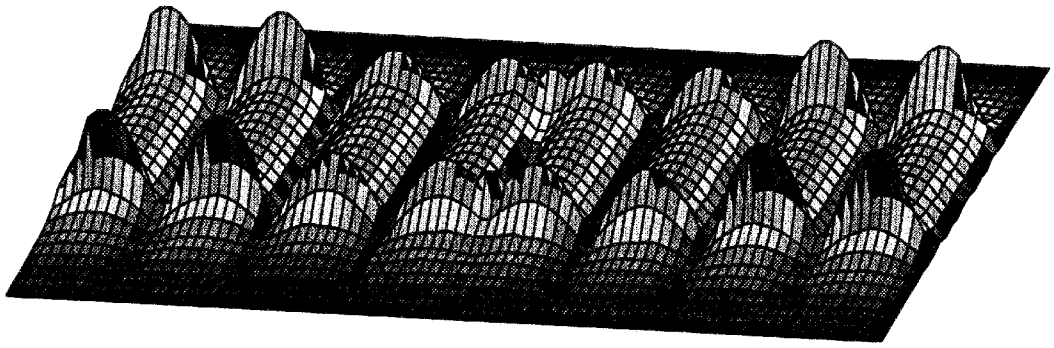
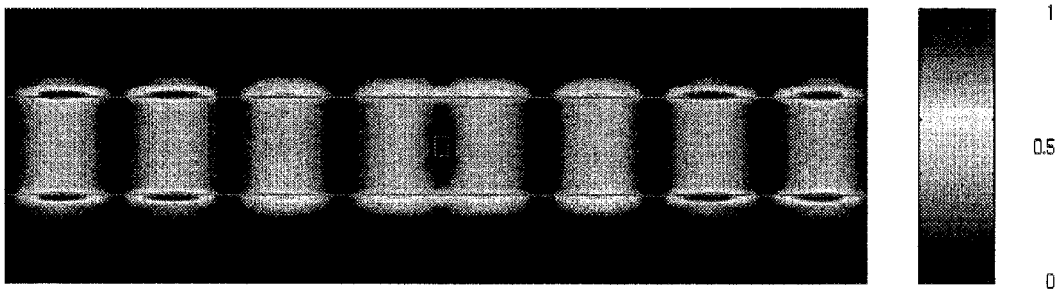


Figure 4.4: Scattering parameters of the microstrip short circuit for two different substrate heights (H_1 = 0.2, 0.3 mm) with via hole grounding at the center of the line.



(a)



(b)

Figure 4.5: Magnitude of the electric field distribution at $f = 20$ GHz under the microstrip short circuit ($z = 0.19$ mm plane). The edge singularity and the standing wave patterns of the electric field distribution are clearly revealed.

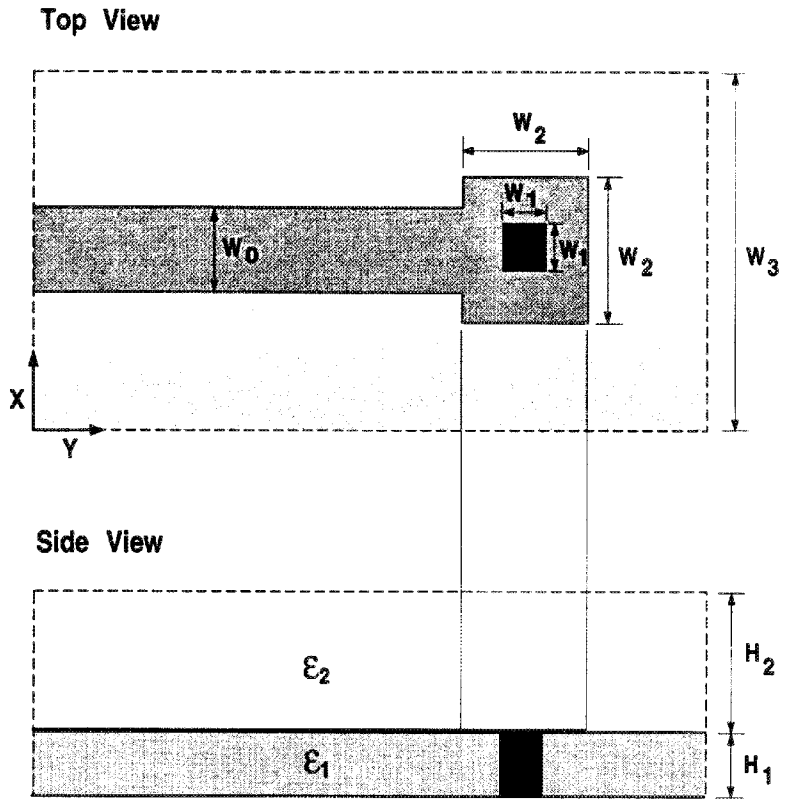


Figure 4.6: Geometry of a 1-port microstrip ground pad. This is a board level via. W_0 = 2.30 mm, W_1 = 1.15 mm, W_2 = 2.88 mm, W_3 = 10.0 mm, H_1 = 1.0 mm, H_2 = 2.0 mm, $\epsilon_1 = 3.4$, $\epsilon_2 = 1$. The dotted lines around the geometry represent the outer boundaries for FEM mesh termination.

two lines. As the operating frequency increases, current flows to ground from the two side walls of the via, with considerable current flowing towards the other microstrip line, resulting in substantial coupling between the two lines.

4.3 Microstrip Ground Pad

In many high frequency applications, ground connections on substrate surfaces opposite to the ground plane are commonly called for and need to be carefully characterized. These DC/RF ground connections can be realized with the use of ground pads, as shown in Fig. 4.6. In general, the characteristics of the vertical via hole

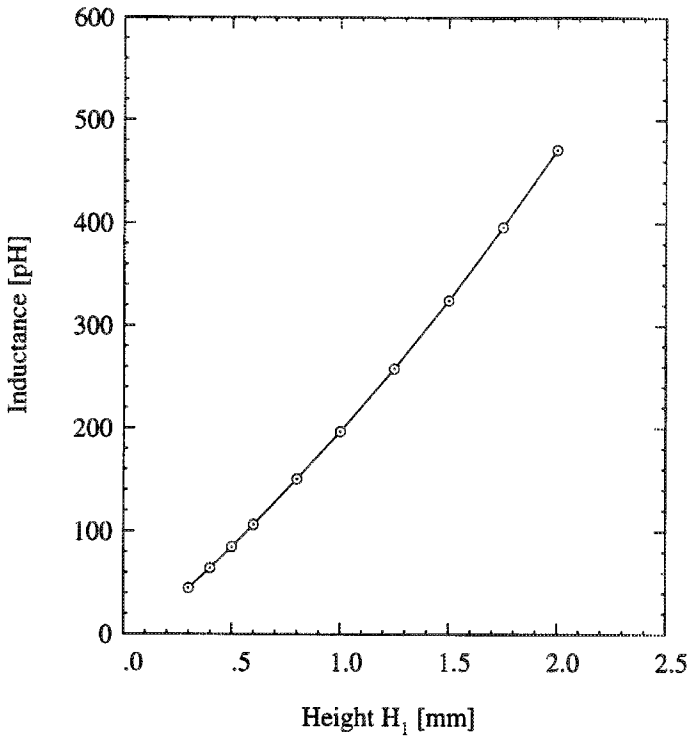


Figure 4.7: The via inductance calculated from the flux/current definition at 10 GHz as a function of via height.

and the ground pad can be represented by an appropriate lumped element. In this study, the vertical via hole is modeled by an inductive element in view of its role as a vertical current path from the microstrip line to the lower ground plane. The inductance of the via hole has been computed in a wide frequency range and, without loss of generality, the inductance is computed at 10 GHz as a function of via hole height (see Fig. 4.7) using the well known flux/current relation applied to magnetic field distributions.

One important issue associated with the high frequency characterization of distributed components, such as the ground pad, is the use of an appropriate reference plane in the evaluation of the scattering parameters. The choice of this reference plane greatly affects the derivation of a meaningful equivalent circuit. As shown in

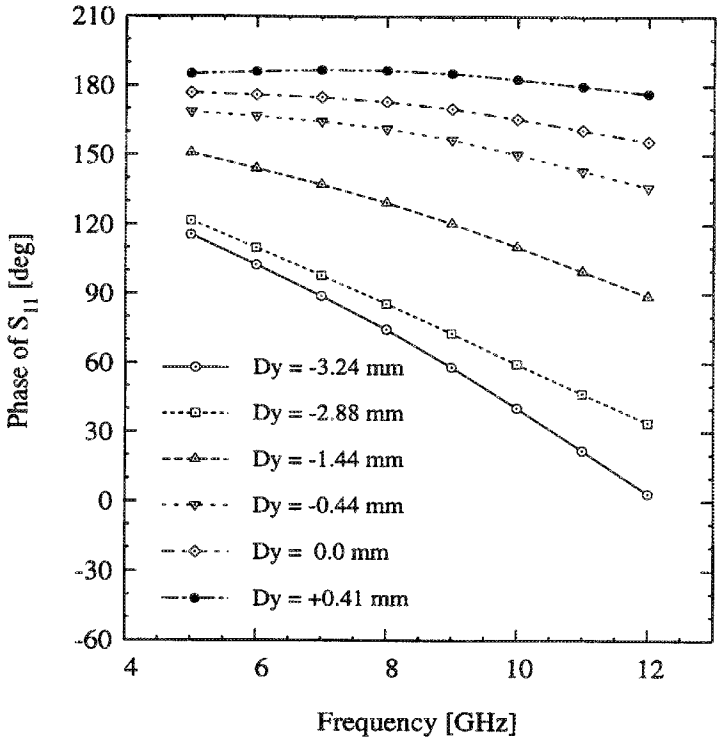


Figure 4.8: Phase of the S_{11} of the microstrip ground pad computed using the FEM at several different reference planes (D_y = +0.41, 0.0, −0.44, −1.44, −2.88, and -3.24 mm from the top to the bottom of the graphs). D_y is 0.0 mm at the geometrical center of the via. H_1 = 1.0 mm.

Fig. 4.8, the phase of the scattering parameter S_{11} always varies with frequency, irrespective of the position of the reference plane, in a way that makes it very hard to find an equivalent inductance which is both frequency and reference plane independent. One might need to consider a more complex circuit arrangement to successfully fit the derived parameters over a wide frequency range. As a result, the use of the scattering parameters for the derivation of a simple equivalent circuit becomes much less successful, as compared to the previous approach which is based on the flux/current definition.

The variation of the inductance, which is computed based on the flux/current

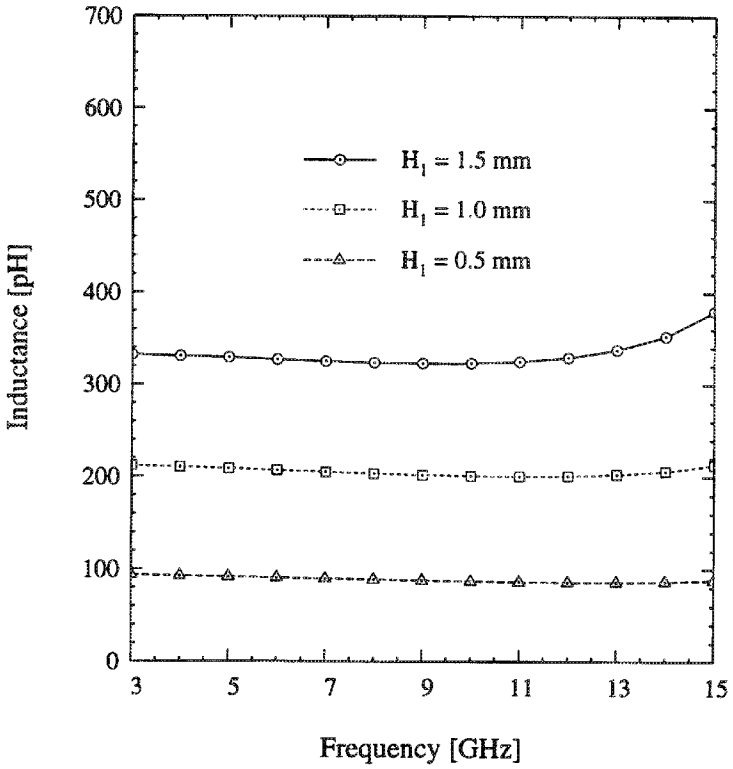
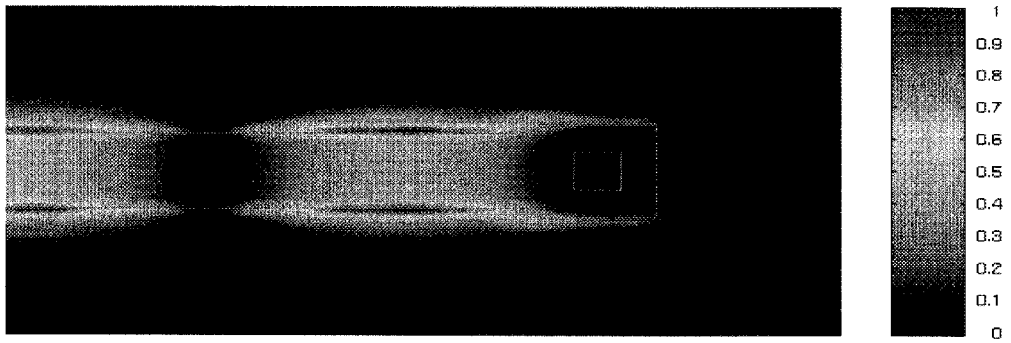
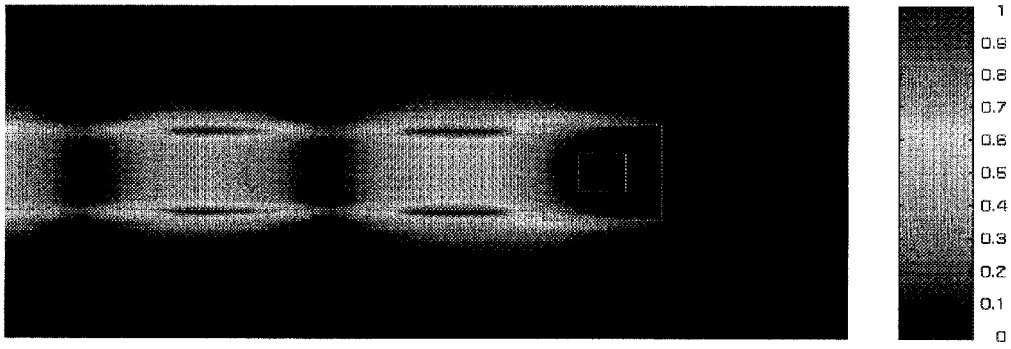


Figure 4.9: The via inductance of the microstrip ground pad calculated from the flux/current definition for three different via heights (H_1 = 0.5, 1.0, 1.5 mm) as a function of frequency.

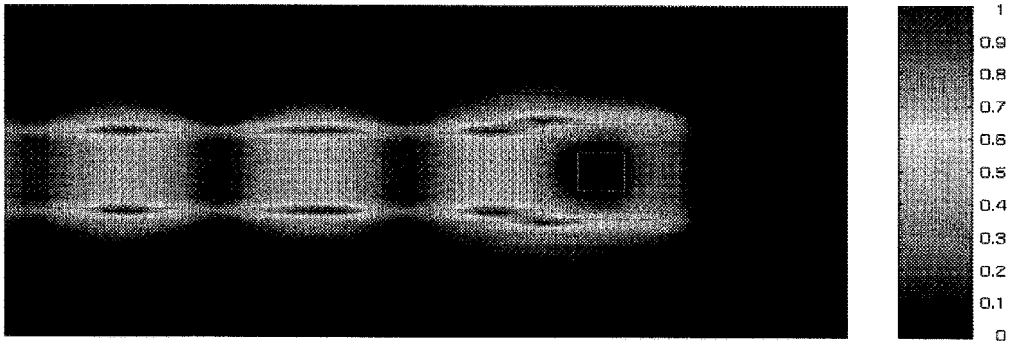
definition, vs. frequency for various via heights is shown in Fig. 4.9. As seen from these results, for substrate thicknesses which are approximately less than one fifteenth of the guided wavelength, the inductance is independent of frequency, indicating that the quasi-static predictions could be very accurate. The advantage of using partial differential equation techniques, such as the finite element method, is found in their ability to compute fields and power/energy distributions around the circuit and its discontinuities. The visualization provided by the FEM technique can enhance the qualitative understanding of the electrical performance of the components under study. For example, Fig. 4.10 reveals the electromagnetic energy distribution under the microstrip line at a plane 0.9 mm above the ground. As seen from the these



(a)



(b)



(c)

Figure 4.10: Magnitude of the total electric field distribution at (a) f = 10 GHz, (b) f = 15 GHz, and (c) f = 20 GHz under the microstrip line at z = 0.9 mm plane. The edge singularity and the standing wave patterns of the electric field distribution are clearly revealed.

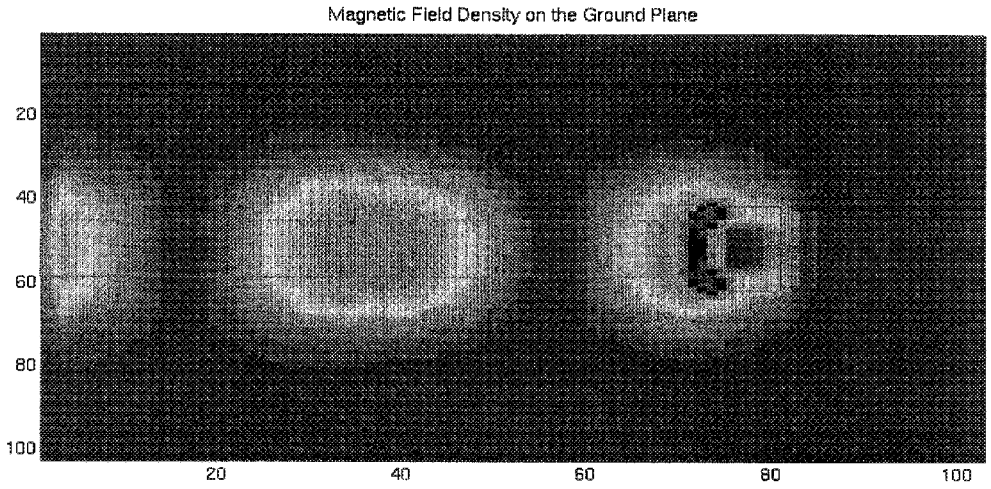


Figure 4.11: Magnitude of the magnetic energy distribution on the ground plane at $f =$ 10 GHz. The via inductance is mainly determined by the magnetic energy surrounding the via.

figures, at 10 to 15 GHz region, most of the energy is concentrated on the front wall of the via with little fields distributing in the area around it. However, as the operating frequency increases up to 20 GHz, the electromagnetic energy starts to spread into the sides and back of the vertical via holes. In the same figure, the standing wave patterns and edge singularity of the electric fields on the microstrip line connected to the pad are clearly revealed. From the magnetic field distribution around the vertical via hole, the frequency dependent via inductance has been calculated. As shown in Fig. 4.11, the magnetic energy is concentrated at the front side of the via hole, along the shortest current path from the line to the ground plane.

4.4 CPW-to-Microstrip Through-Via Transition

4.4.1 Without Via Hole

In high frequency applications, for better use of real estate, both surfaces of the substrate incorporate printed circuit components which may contribute to similar

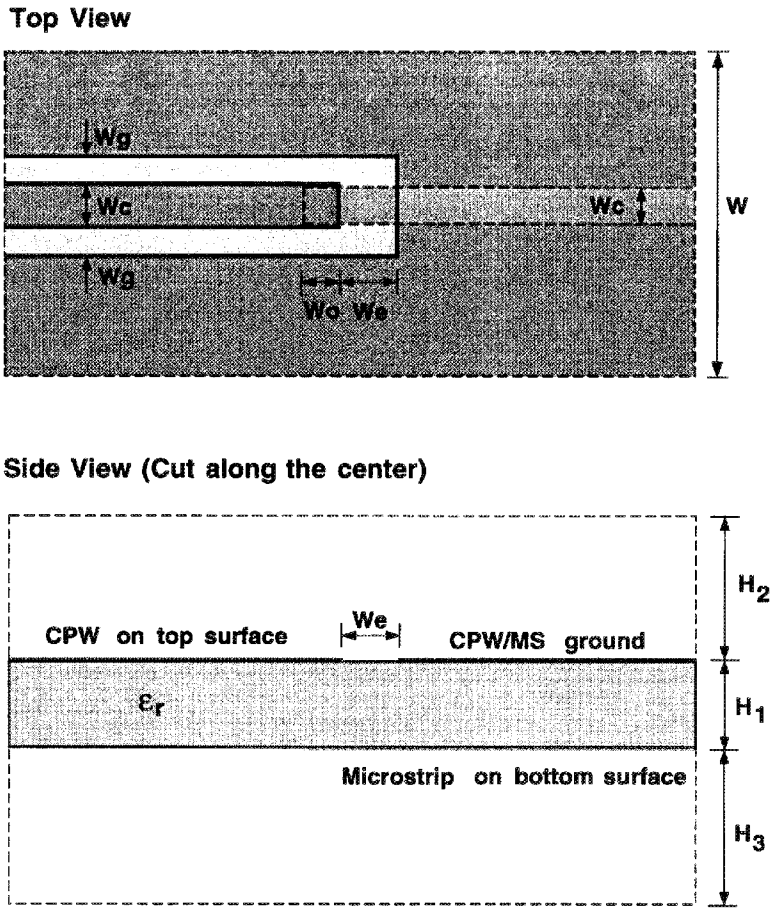


Figure 4.12: Geometry of the transition from CPW to microstrip on different layers without via hole. $W_g = 50\mu$m , $W_c = 75\mu$m , $W_o = 75\mu$m , $W_e = 200\mu$m , $W = 1000\mu$m , $H_1 = 100\mu$m , $H_2 = H_3 = 400\mu$m , and $\epsilon_r = 12.9$.

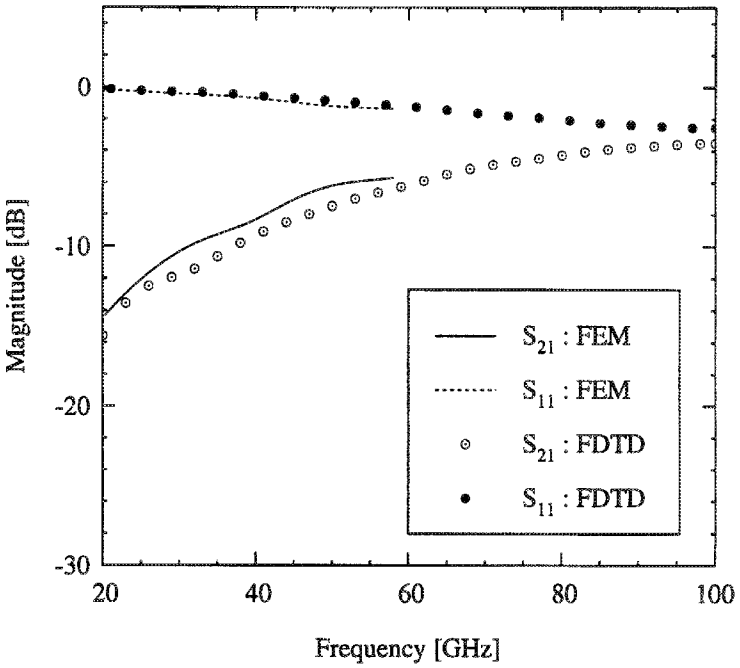


Figure 4.13: Scattering parameters for the transition from CPW-to-microstrip on different layers without via hole connection.

electric functions or tasks. When this approach is incorporated into circuit design, the two substrate surfaces host complementary geometries to reduce cross-talk and to increase the degree of circuit integration.

In this section, as an effort to use both sides of a substrate, a coplanar waveguide-to-microstrip configuration is investigated. As shown in Fig. 4.12, the CPW line is printed on top of a substrate and the microstrip line is fabricated on the other side of the substrate surface. With this arrangement, the ground of the CPW can serve as the ground of the microstrip, while the CPW apertures and microstrip run in parallel and are separated by some distance to reduce parasitic cross-talk.

Given the geometrical details, the CPW transmission line has characteristic impedance 43 Ω , while the microstrip line reveals 50 Ω. These lines are fabricated on different sides of a 100 μm thick GaAs substrate. As shown in Fig. 4.13,

the computed cross-talk ($|S_{21}|$) between the lines is near -15 dB at 20 GHz and decreases further as frequency decreases. In other words, more than 95% of the input power is reflected back to the input port in the low frequency region, revealing relatively good isolation between the ports. However, as the operating frequency increases up to 100 GHz, this cross-talk increases monotonically up to approximately -4 dB. The increased cross-talk could be ascribed to several facts: high frequency radiation effects from the open end of the CPW and microstrip, or the higher order and substrate modes generated between the two transmission lines.

4.4.2 With Via Hole

The CPW-to-microstrip transition structure studied in the previous section can be modified to have much less insertion loss by placing a via hole between the two transmission lines, as shown in Fig. 4.14. When those two lines are interconnected through the metallized via hole between the end of the microstrip line and the center conductor of the CPW, a wide band direct DC/RF connection is obtained. As a result, the transition structure can operate in an ideal fashion, at least in the low frequency region.

The computed S-parameters of the transition are shown in Fig. 4.15. The return loss remains under -20 dB for frequencies as high as 40 GHz. The FEM calculated values agree very well with that of the ideal transmission line. Note that the theoretical value of the reflection coefficient of an ideal transmission line is given as -22.5 dB for 43 Ω-to-50 Ω impedance step. As the operating frequency increases up to 100 GHz, the performance of the transition starts to degraded, giving a return loss of about -9 dB. Even though the transition shows degraded performance in the high frequency region, the overall characteristics closely follow that of the ideal transmis-

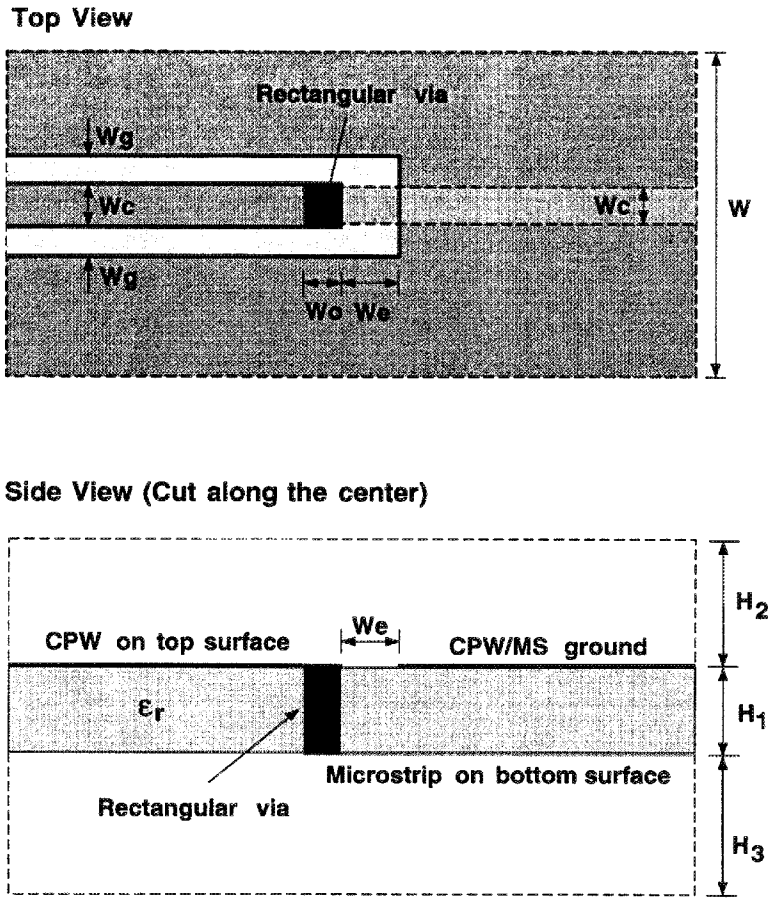


Figure 4.14: Transition from CPW to microstrip on different layers through via hole. $W_g = 50\mu$m, $W_c = 75\mu$m, $W_o = 75\mu$m, $W_e = 200\mu$m, $W = 1000\mu$m $H_1 = 100\mu$m, $H_2 = H_3 = 400\mu$m , and $\epsilon_r = 12.9$. The vertical via is an empty rectangular cavity with PEC walls.

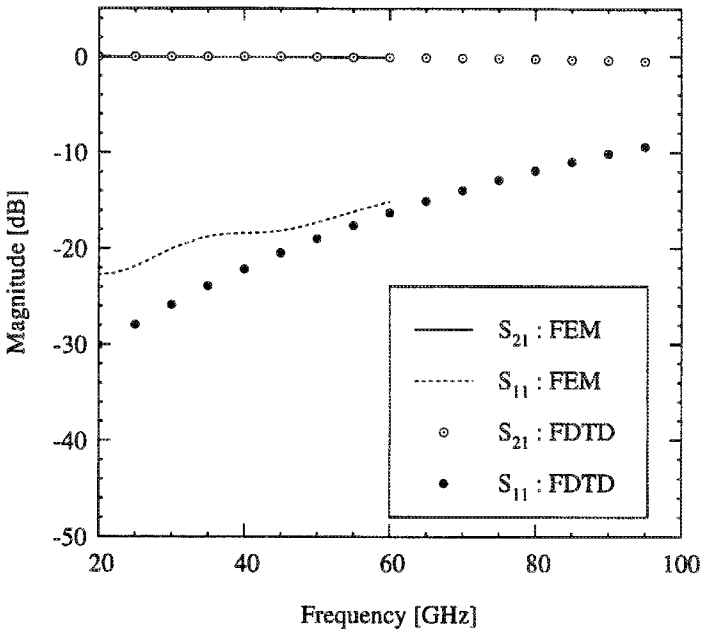


Figure 4.15: Scattering parameters of the CPW-to-microstrip transition with vertical via hole connection.

sion lines in the low frequency region. This type of transition structure can be used in multi-layer MIC or MMIC interconnects, the hermetic sealing of a package, and antenna feeding networks.

4.5 Channelized CPW-to-Microstrip Transition

In this section, another type of CPW-to-microstrip transition geometry, which is planar instead of the non-planar configuration in the previous section, is carefully designed and characterized for broadband applications. The planar CPW-to-microstrip transition has found many important applications in the area of hermetic packaging, high frequency probing, etc. Fig. 4.16 shows the transition from a channelized CPW [171] to a microstrip line and in the transition, both CPW and microstrip lines are printed on the same substrate surface, as opposed to the previous CPW-to-microstrip transition.

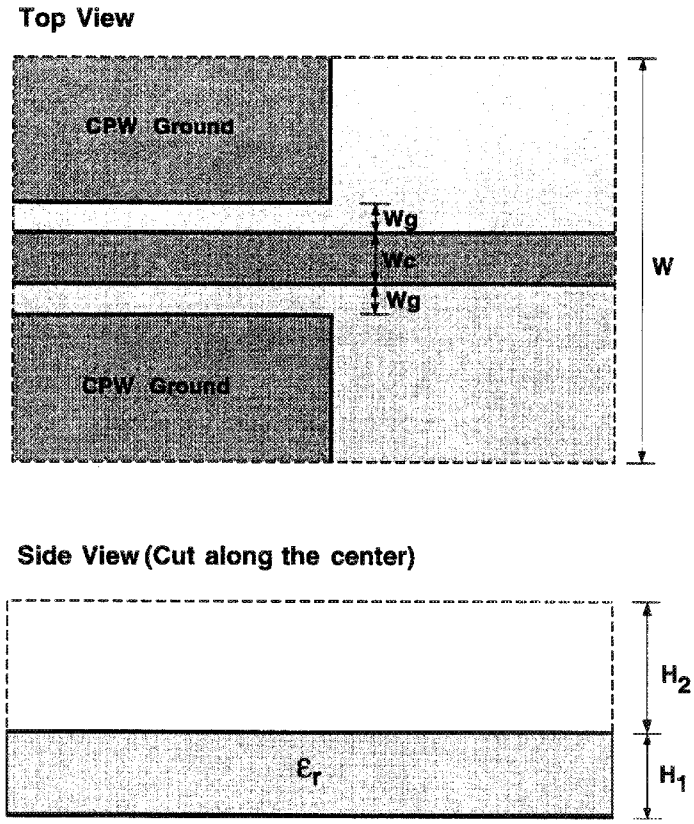


Figure 4.16: Geometry of a channelized CPW to microstrip transition. $W_g = 50\mu$m, $W_c = 75\mu$m, $W = 1000\mu$m, $H_1 = 400\mu$m, $H_2 = 500\mu$m and $\epsilon_r = 12.9$.

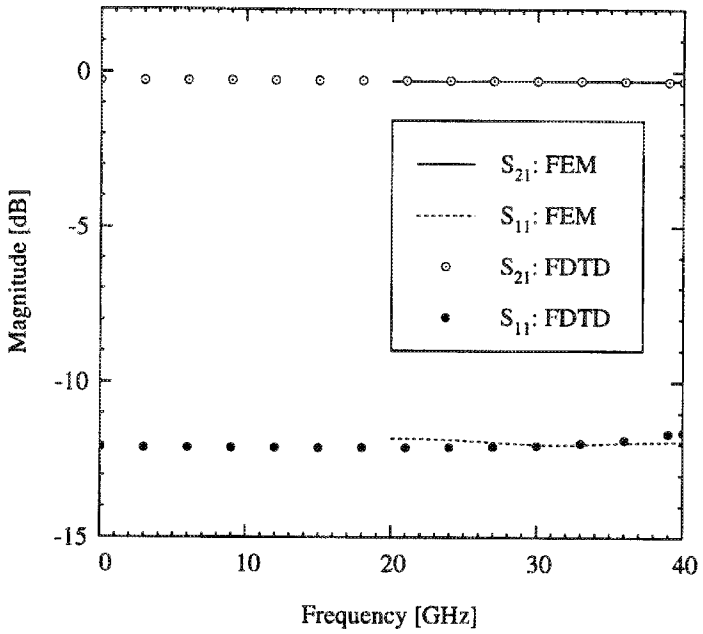


Figure 4.17: Scattering parameters for the channelized CPW-to-microstrip transition.

The scattering parameters of such a transition geometry printed on GaAs substrate of thickness 400 μm are shown in Fig. 4.17. The insertion and return losses remain almost constant in the frequency range up to the 40 GHz region. The agreement between the FEM and FDTD results is very good, and further the results of both techniques agree very well with those obtained using the space domain integral equation method (SDIE) [172]. Also, compared to the value -12.7 dB computed from the ideal transmission line step discontinuity, 50-to-80 Ω, the computed data give very close results regardless of its non-TEM propagating modes.

Similar behavior has been found for the case of 100 μm GaAs substrate, except that in this case the return loss decreases to about -20 dB. Note that the return loss of the ideal transmission line having a 43-to-49.5 Ω discontinuity is -22.5 dB. The reason for this good performance irrespective of the substrate thickness is that the field distribution around the center conductor of the chanellized CPW becomes

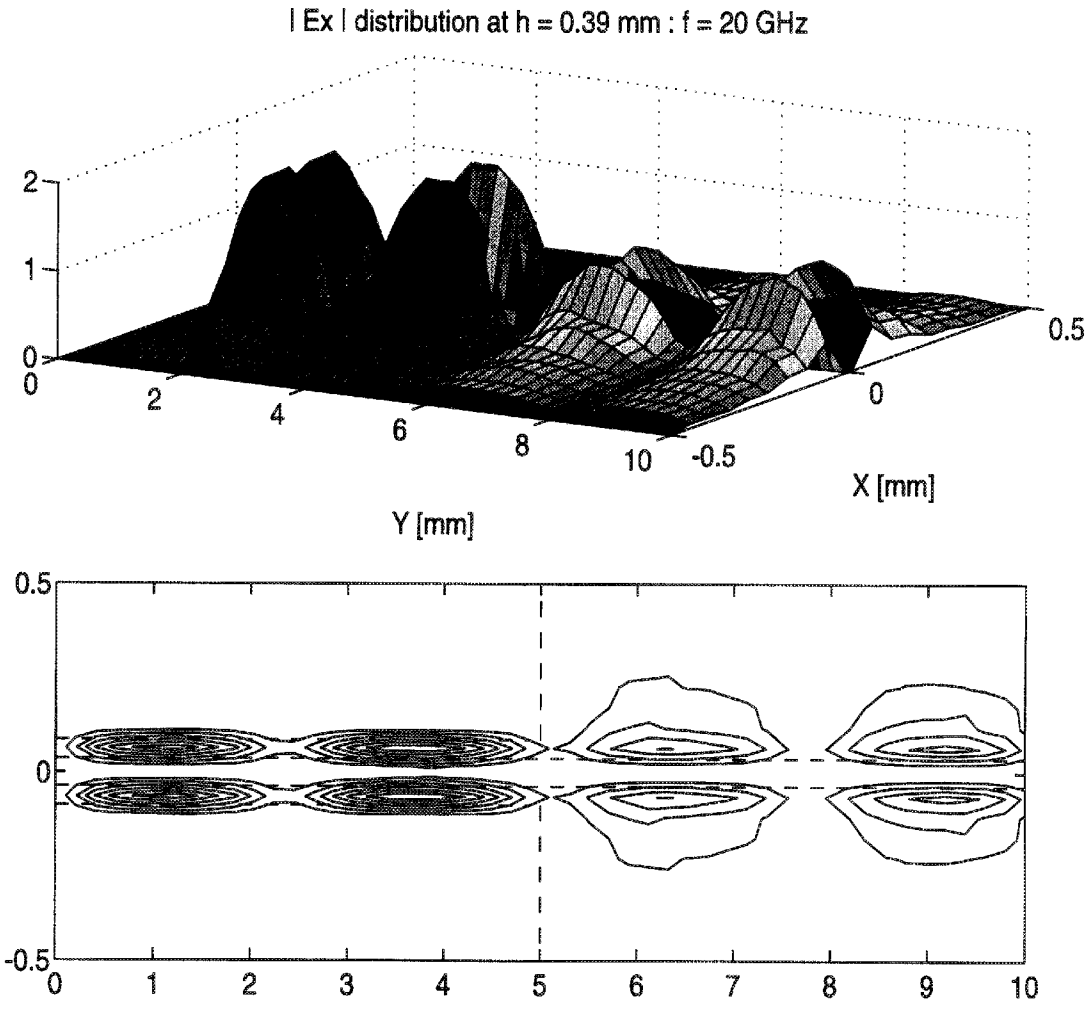


Figure 4.18: Magnitude of transverse component of the electric field at $z = 390\mu$m plane.

very similar to that of the microstrip (i.e., most of the fields are confined under the center strip). Fig. 4.18 shows the magnitude of the tangential (to the surface) component of the electric field at a plane just underneath the dielectric-air interface at 20 GHz. The standing wave patterns along the CPW and microstrip lines can be clearly observed.

4.6 Asymmetric 2-port Via with Plated-Through-Hole

In a multi-layer circuit environment, the vertical interconnections between various signal lines in different layers are frequently encountered and need to be modeled for a thorough understanding of low as well as high frequency effects. As a matter of fact, the modeling procedure is focused on the stage of finding an appropriate lumped equivalent circuit, due to its usefulness and simplicity, despite its limited accuracy. In general, the vertical interconnections are fabricated using a plated-through-hole (PTH) in the ground planes located between the signal layers. Even though it is possible to have more than one ground plane and signal layer, in this section, we considered a simplified geometry which has two signal layers and one ground plane between them, and the two signal lines are connected through a vertical via hole.

Fig. 4.19 has the schematic view of an asymmetric 2-port via hole with a PTH in the middle of the substrate. The PTH is filled with air, while the two substrates have the same relative dielectric constant ($\epsilon_r = 4.5$) and thickness ($H_1 = H_2 =$ 0.2 mm). To examine the effect of PTH size on the transition performance, three different PTH opening sizes have been examined while the other geometrical factors remained unchanged.

At first glance, it is expected that as the size of the opening D increases, the capacitance between the vertical via and the ground plane becomes smaller and the

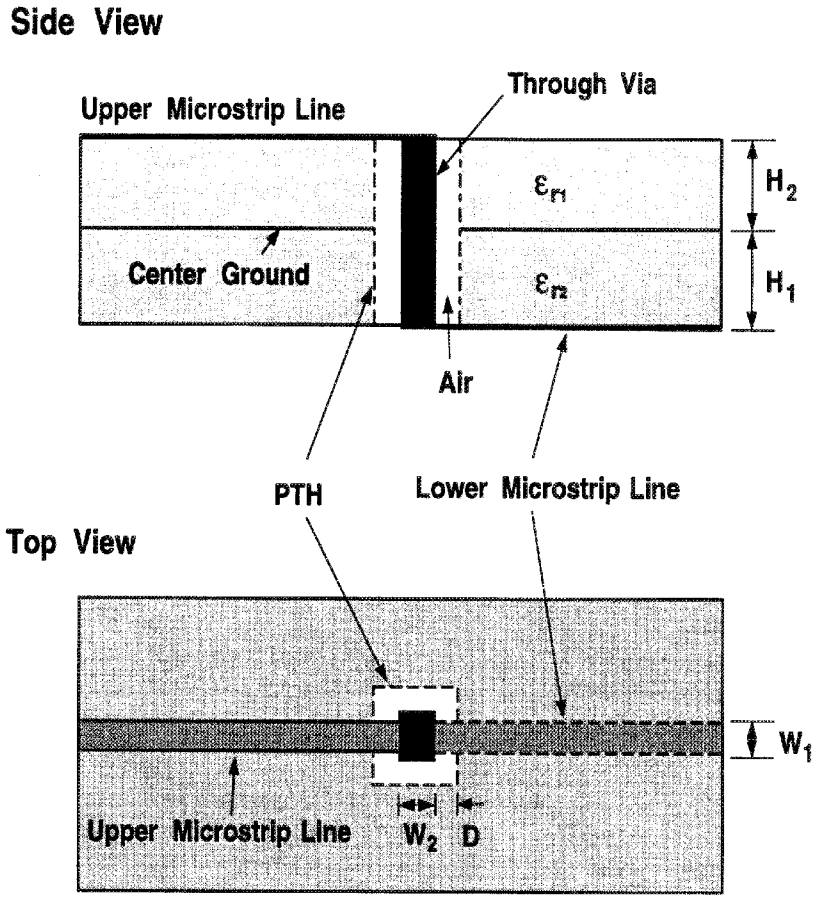


Figure 4.19: Geometry of asymmetric two port via hole passing through a plated-through-hole (PTH) in the middle of the substrate. $H_1 = H_2 = 0.2$ mm, $W_1 = 0.4$ mm, $W_2 = 0.8$ mm, $\epsilon_{r1} = \epsilon_{r2} = 4.5$, $D = 0.2, 0.4, 0.7$ mm (3 cases).

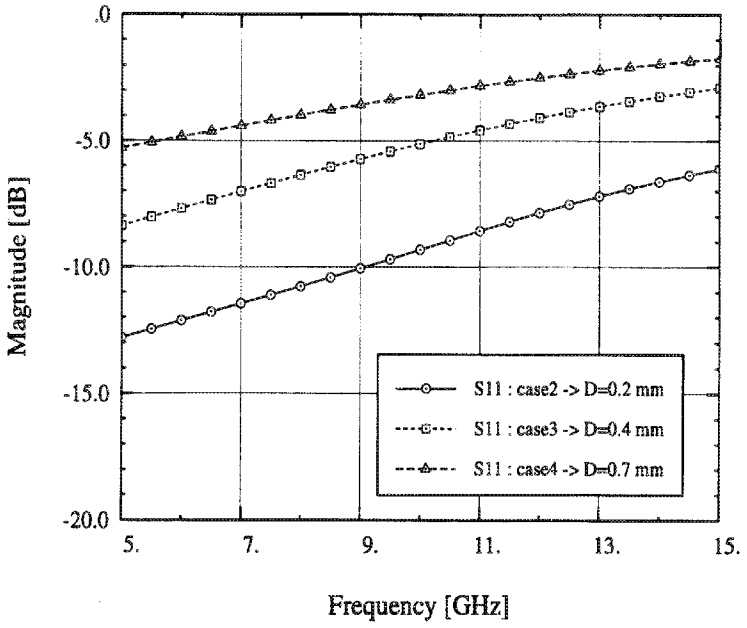


Figure 4.20: Comparison of the S-parameters for 3 different PTH sizes.

resulting reflection coefficient would be reduced. However, as shown in Fig. 4.20, the reflection coefficient increases as the distance between the via hole and the opening in the ground plane increases, which means there is more reflection with larger opening size. Considering the fact that increasing D implies less and less interaction between the via hole and the ground plane, the above results seem to be contradictory. However, as seen in Fig. 4.19 the microstrip lines are connected to the vertical via through its pads, and there are impedance mismatches between the microstrip lines on the substrate and lines crossing the air gap between the via pads and the microstrip lines. While the characteristic impedance of the microstrip lines is 48 Ω, that of the line across the gap has a much higher value. As a result, as the length of the high impedance line section becomes longer, the effect of the discontinuities becomes intensified. Therefore, it is inappropriate to use the above configuration to examine the effect of the PTH opening size. It is recommended, instead, that for the

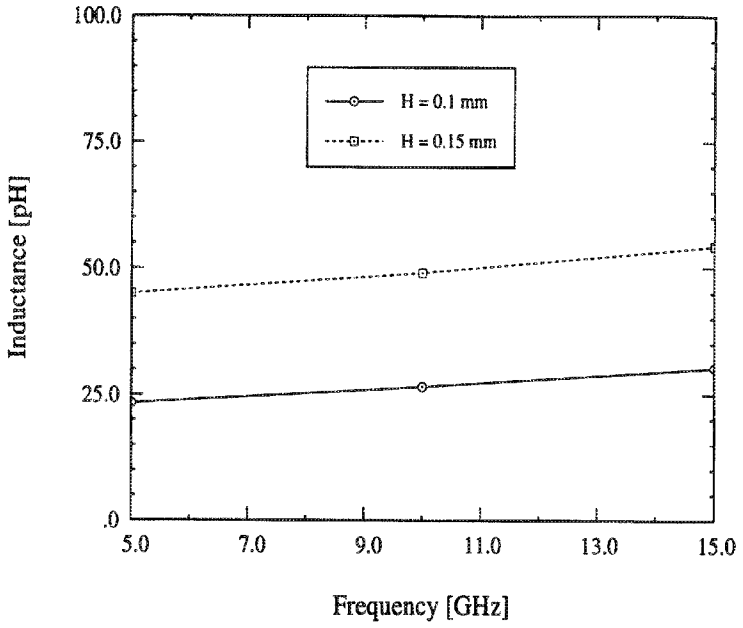


Figure 4.21: Via inductances of two different via height: $H_1 = H_2 = 0.1$ and 0.15mm and D = 0.4 mm. Inductances are evaluated from the magnetic flux density surrounding the via.

characterization of the effect of the PTH sizes, the air region between the via and PTH has to be filled with the same dielectric material to minimize the transmission line discontinuities.

The equivalent via hole inductances having two different heights ($H_1 = H_2 = 1.0$ and 1.5 mm) are computed from the magnetic flux density, as shown in Fig. 4.21. It is observed that the equivalent inductance of the via hole inside of the PTH has a slight variation as operating frequency increases and shows deviation from linear dependence on the via hole height. Fig. 4.22 shows a simple equivalent circuit (so called, type I) of the asymmetric 2-port via hole geometry. While the inductance values (L_{via}) of the via hole are extracted from the flux model, the shunt capacitance is found by matching the scattering parameters, both magnitude and phase, as computed from the FEM with the equivalent circuit.

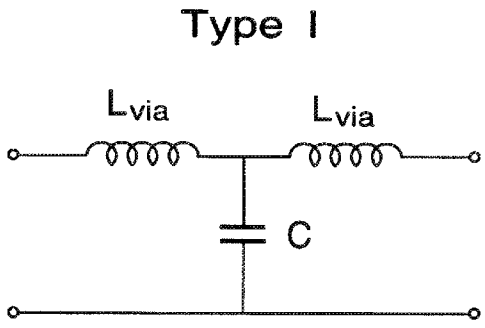


Figure 4.22: Type I equivalent circuit used for the asymmetric 2-port via hole geometry. Note that if the PTH opening becomes smaller, C increases and finally becomes a short circuit.

Fig. 4.23 shows an example of the matching procedure. As shown in the figure, the magnitude and phase data reveal some degree of discrepancies due to the over-simplified equivalent circuit. For the transition with D = 0.2 mm and $H_1 = H_2 =$ 0.1 mm, the inductance and capacitance values of the type I equivalent circuit are determined as $L_{via} = 25$ pH and $C = 0.28$ pF for the best agreement between the FEM and the equivalent circuit data.

It is interesting to observe that increasing the distance D causes a smaller capacitance value and finally renders zero capacitance, leading to an open circuit as D becomes infinity. This observation is consistent with the physical structure, since infinite D implies no ground plane. Similarly, decreasing D causes a larger capacitance and eventually makes the shunt capacitance a short circuit, which is what is happening in reality.

4.7 Double Via Hole

In many microwave and millimeter-wave circuits, more than one via hole is used in close proximity to provide certain functionality, such as ground path, shielding, or vertical transition. However, these via holes can cause undesirable effects due to their

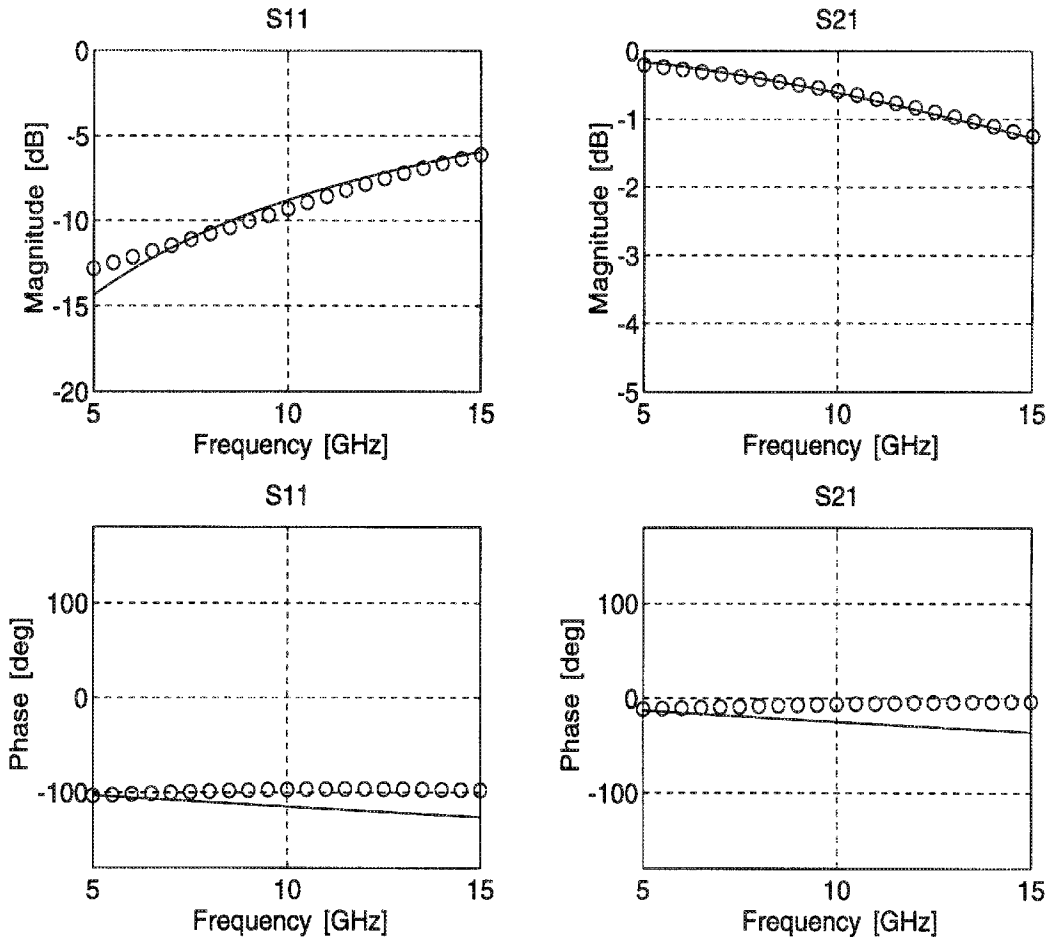


Figure 4.23: Matching the S parameters using the type I equivalent circuit (Circle : FEM data, Line : Equivalent circuit). $H_1 = H_2 = 0.1$ mm and D = 0.2 mm. L_{via} = 25 pH, $C = 0.28$ pF with type I equivalent circuit.

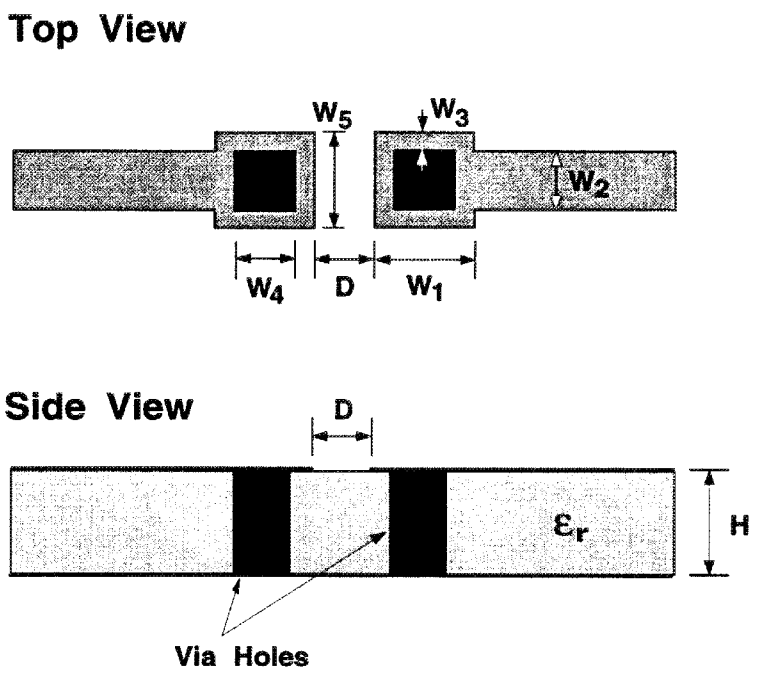


Figure 4.24: Geometry of double via hole. H = 1.6 mm, W_1 = 1.4 mm, W_2 = 1.0 mm (85 Ω), W_3 = 0.2 mm, W_4 = 1.0 mm, W_5 = 1.4 mm, ϵ_{r1} = 4.5, D = 0.2, 0.4, 0.6, 0.8 mm (4 cases)

mutual interactions, that is, electromagnetic coupling, depending on the operating frequency and geometrical factors. As a result, these closely spaced via holes have to be modeled and used carefully to provide the desired properties and prevent spurious phenomena. For successful design of high performance high frequency circuits, it is imperative to accurately predict the mutual coupling of multiple via holes. In view of this, in this section, the effect of the electromagnetic coupling between two identical ground via holes are studied and an appropriate equivalent circuit is developed to depict the coupling effects.

As shown in the schematic view of the structure in Fig. 4.24, two via holes are placed face to face each other with separation distance D. To model the coupling from one via hole to the other, the separation distance is changed from 0.2 to 0.8 mm

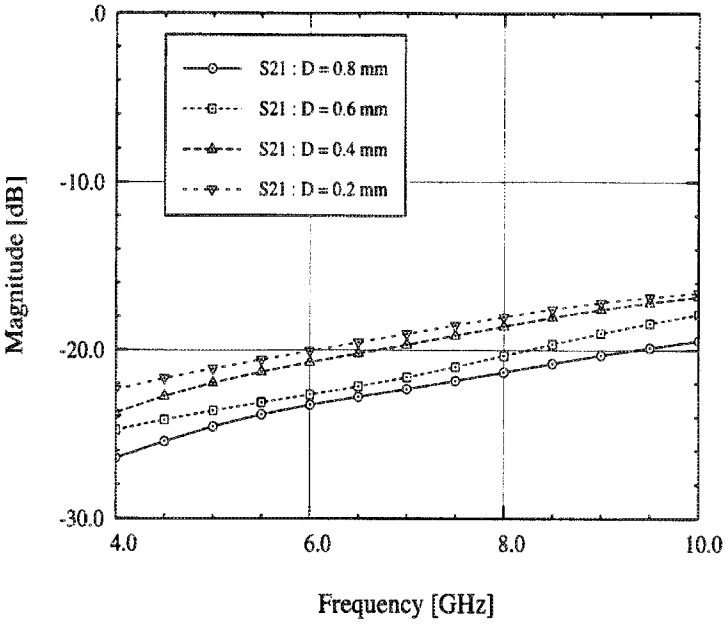


Figure 4.25: Comparison of the S-parameters for 4 different separation distances.

and the corresponding scattering parameters are computed as presented in Fig. 4.25. As can be observed in the figure, the cross talk, $|S_{21}|$, between two via holes gradually increases as the operating frequency increases and becomes stronger as the distance becomes smaller. The electromagnetic field distributions around the transition are shown in Fig. 4.26 revealing the standing wave patterns on the microstrip lines and its edge singularity. Also, as shown in the figure, more electromagnetic energy is coupled from one line to other as operating frequency increases.

Derivation of an appropriate equivalent circuit representing the coupling effects between the via holes could provide a useful tool for design and optimization of high performance MIC and MMIC circuits, in addition to intuitive understanding of the electromagnetic phenomena. As a response, in this study, the type II equivalent circuit shown in Fig. 4.27 is derived for the geometry. Note that as the separation distance D becomes very large, the mutual inductance L_{12} and capacitance C_{12}

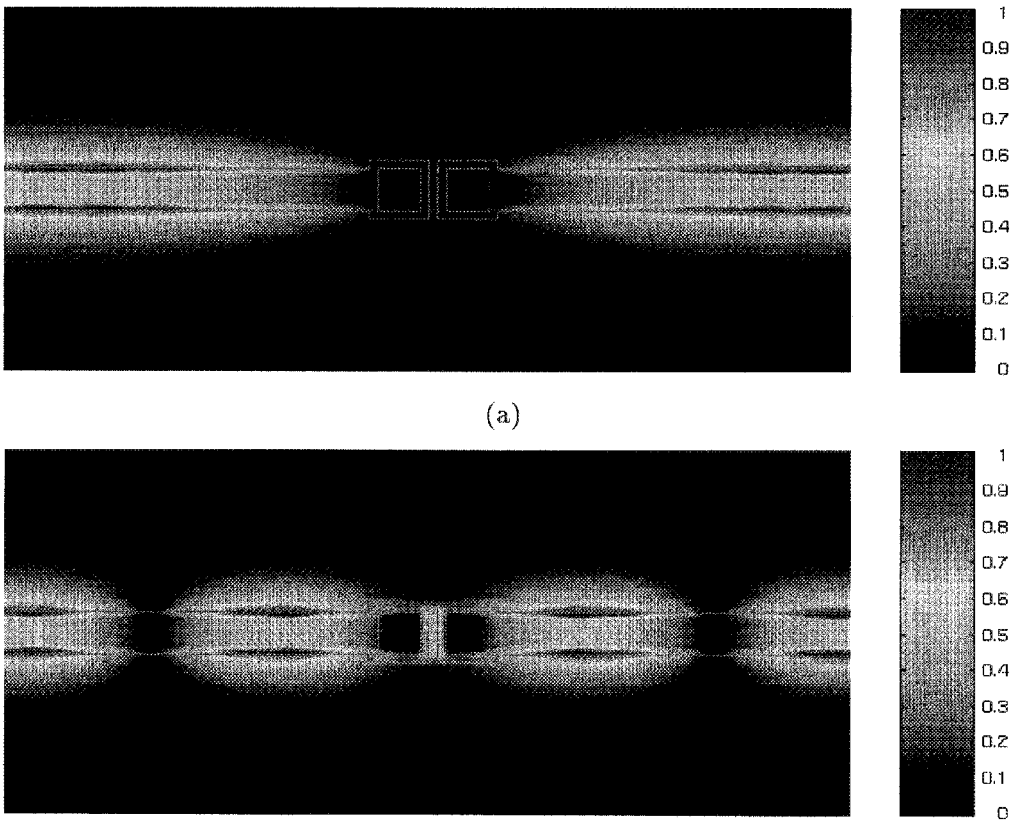


Figure 4.26: Magnitude of the total electric field distribution at (a) f = 4 GHz and (b) f = 10 GHz under the microstrip line at $z = 1.5$ mm plane. The edge singularity and the standing wave patterns of the electric field distribution are clearly revealed.

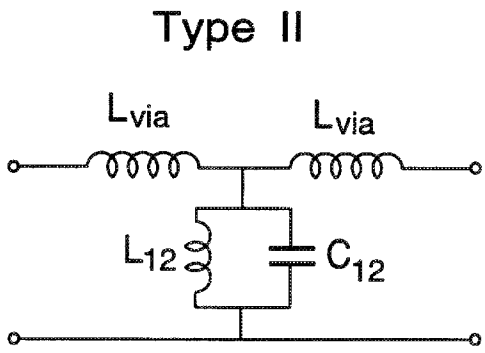


Figure 4.27: Type II equivalent circuit used for the double via hole geometry. The L_{12} and C_{12} represent the mutual coupling between the via holes. Note that if the separation distance D increases, the L becomes smaller and finally becomes ideal short circuit.

become negligible, and finally become two separate circuits having L_{via} connected to the ground plane directly. It is also interesting to observe that there are resonances in the high frequency region due to the shunt impedance elements and these frequencies are tabulated in Table 4.1.

Fig. 4.28 shows an example of the S-parameter matching procedure, and in Table 4.1 the equivalent circuit parameters are listed for the four different separation distances. For all the cases, the via inductance L_{via} is forced to have the same value, while the mutual inductance L_{12} and capacitance C_{12} are searched to find the best fit of the FEM data. As shown in the table, the capacitance values remain constant in all the cases, but the mutual inductance L_{12} changes as a function of separation distances. As the distance D increases, L_{12} decreases from 120 to 80 pH for $D = 0.2$ and 0.8 mm, respectively. The constant coupling capacitances and changing inductance reflect the fact that the coupling is mainly coming from the vertical current flow on the via holes and their resulting magnetic fields. The derived equivalent circuit can be used to model and predict the electromagnetic coupling among the multiple via

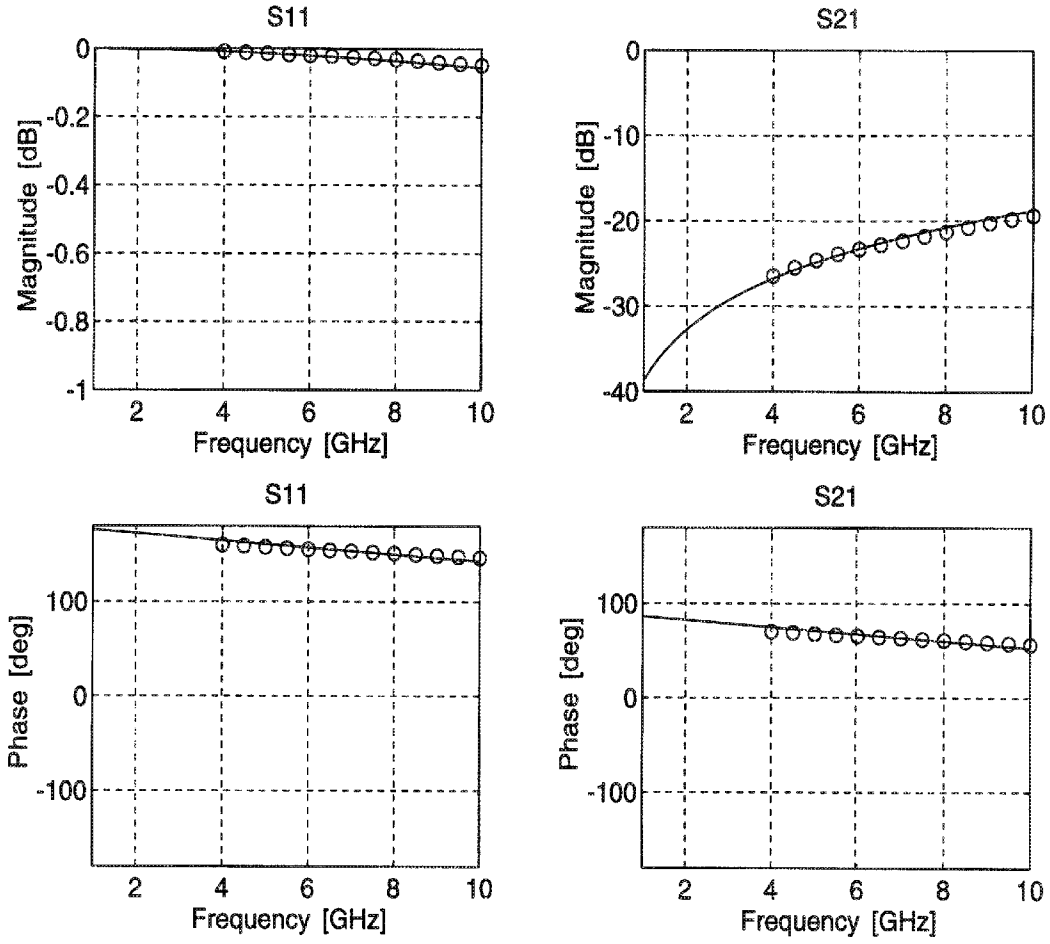


Figure 4.28: Matching the S parameters with the type II equivalent circuit. L_{via} = 380 pH, L_{12} = 80 pH, and C_{12} = 0.1 pF. H = 1.6 mm, W_1 = 1.4 mm, W_2 = 1.0 mm, W_3 = 0.2 mm, W_4 = 1.0 mm, W_5 = 1.4 mm, ϵ_{r1} = 4.5, D = 0.8 mm. Circle : FEM data, Line : Equivalent circuit.

D [mm]	L_{via} [pH]	L_{12} [pH]	C_{12} [pF]	f_{res} [GHz]
0.2	380	120	0.1	45.94
0.4	380	105	0.1	49.12
0.6	380	90	0.1	53.05
0.8	380	80	0.1	56.27

Table 4.1: The equivalent circuit parameters of the double via hole structure and corresponding resonance frequency. The via inductance L_{via} is extracted from the flux model, while the shunt terms, L_{12} and C_{12}, are determined to match the FEM data with the equivalent circuit.

holes often encountered in the MIC and MMICs.

4.8 CPW-to-Slotline Transitions

With the advance of the slot antenna and its array technology, leading to a high efficiency and narrow beam antenna system [173], the effective feeding network of the antenna plays a critical role for its performance [174]–[179]. In this study, two different types of slot antenna feeding networks, planar and non-planar, are modeled using the finite element method. The first transition is designed for direct coupling of RF power from the CPW to the slotline, and printed on the same side of the substrate, which is easy to fabricate. In contrast, the second structure is devised for electromagnetic coupling from the grounded CPW to the slotline on the opposite side of the wafer without using bonding wires, and is thus more reliable for harsh environments.

4.8.1 Planar Transition

The schematic diagram of a planar CPW-to-slotline transition with an air bridge is illustrated in Fig. 4.29. The characteristic impedances of the CPW and slotline are 60 and 70 Ω, respectively. The input CPW line is terminated in an open circuit and an air bridge is used to connect the open end of the CPW center conductor

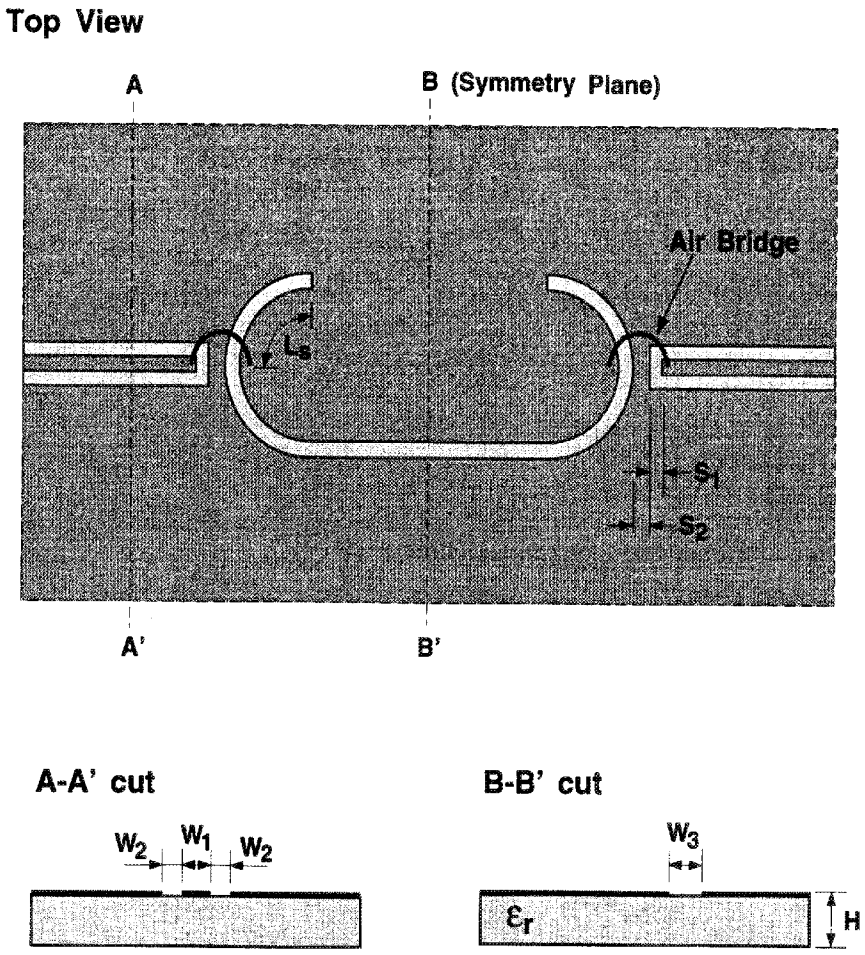


Figure 4.29: Geometry of the CPW-to-slotline planar transition with air bridge: $L_s = 4.751$ mm, $S_1 = 0.114$ mm, $S_2 = 0.129$ mm, $W_1 = 0.305$ mm, $W_2 = 0.254$ mm, $W_3 = 0.178$ mm, $H = 0.635$ mm, and $\epsilon_r = 10.5$.

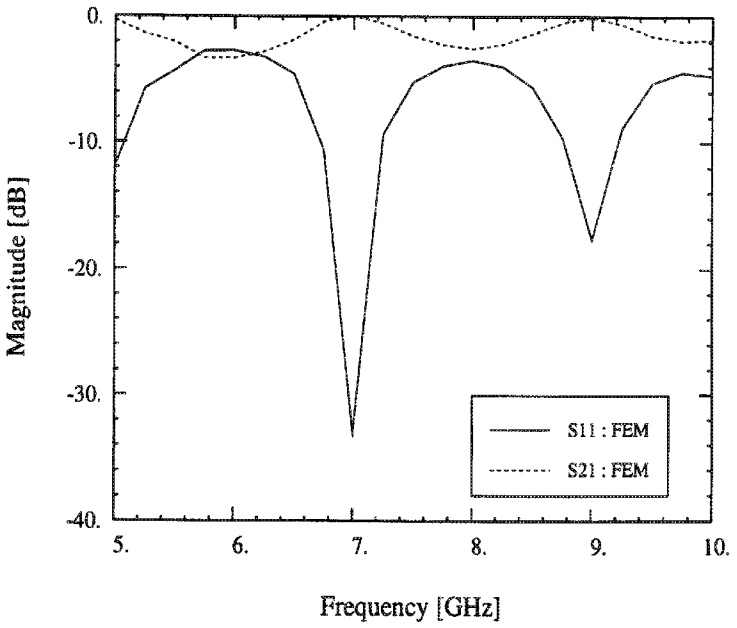


Figure 4.30: Scattering parameters for the coplanar waveguide-to-slotline transition with air bridge.

to the opposite edge of the slotline. The air bridge plays a role of equalizing the potential between the two conducting surfaces and suppressing any spurious modes. The thickness H of the substrate is 0.635 mm with $\epsilon_r = 10.5$, and the other side of the substrate is not metallized. The circular bend at the end of the slotline is intended to provide a smooth transition and the length L_s is designed to be $\sim \lambda_{g(slotline)}/4$ at the center frequency, 7 GHz. As a result, the electric field has a minimum at the end of the slotline (short circuit) and a maximum at the transition region.

In the modeling procedure, the circular bend of the slotline section is approximated to a rectangular geometry having the same length, and the curved air bridges are also replaced with infinitely thin piecewise linear PEC wires. Note that the FEM modeling is performed under a shielding environment. The performance of the transition is shown in Fig. 4.30. It exhibits very narrow band characteristics due to the

rectangular approximation and also shows periodicity of frequency response.

4.8.2 Non-Planar Transition

A non-planar CPW-to-slotline transition, illustrated in Fig. 4.31, is studied in this section. The characteristic impedance of each transmission line section is 70, 80, and 70 Ω for the CPW, microstrip (elongated CPW center conductor) and slotline, respectively. To provide a good short circuit effect, the open end of the CPW ground planes has been extended by length W_4 which is $\lambda_{g(microstrip)}/4$. In addition, to suppress the parallel plate waveguide mode between the two conducting surfaces, the CPW ground planes are trimmed to finite. The overlapping lengths of the elongated CPW center conductor and the underlying slotline are designed to be $\lambda_{g(microstrip)}/4$ and $\lambda_{g(slot)}/4$, respectively, at the center frequency, 6 GHz. Since the normal electric field has a maximum value at the open end of the microstrip line, the magnetic field has its maximum at $\lambda_{g(microstrip)}/4$ from the open end, thus providing maximum coupling from the microstrip to the slotline.

For numerical modeling, the curved section of the slotline is approximated to a rectangular geometry for simplicity and the whole structure is placed inside of closed PEC surfaces (i.e., a shielding environment). On the other hand, the measurement was performed under an open environment. As shown in Fig. 4.32, the modeled and measured data reveal a reasonable correspondence, including the prediction of the two resonances in the frequency region of interest, even though the modeled geometry has narrow bandwidth and inferior performance due to the rectangular approximation. From the above observation, it becomes clear that to accurately predict the performance of the transition structures having circular geometries, the curved structures need to be modeled exactly. Compare to rectangular shaped geometries,

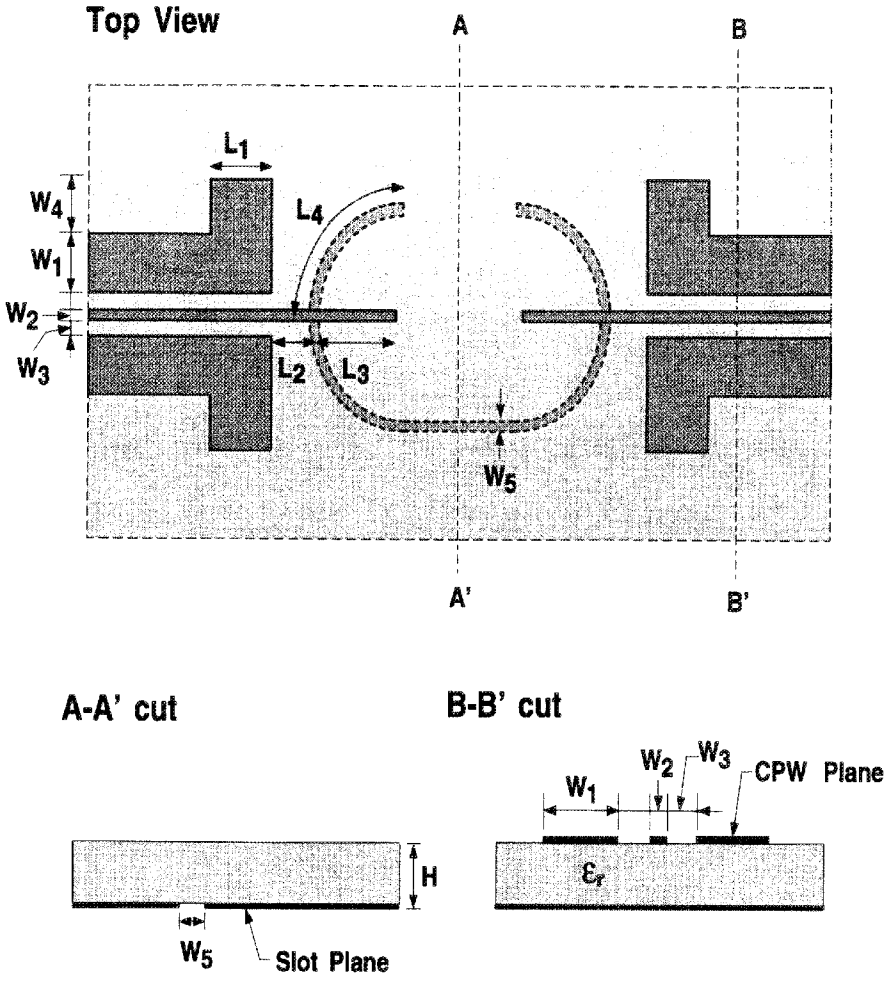


Figure 4.31: Geometry of the CPW-to-slotline non-planar transition: $L_1 = 2.54$ mm, $L_2 = 2.54$ mm, $L_3 = 5.0$ mm, $L_4 = 6.229$ mm, $W_1 = 2.54$ mm, $W_2 = 0.152$ mm, $W_3 = 0.318$ mm, $W_4 = 2.54$ mm, $W_5 = 0.178$ mm, $H = 0.635$ mm, and $\epsilon_r = 10.5$.

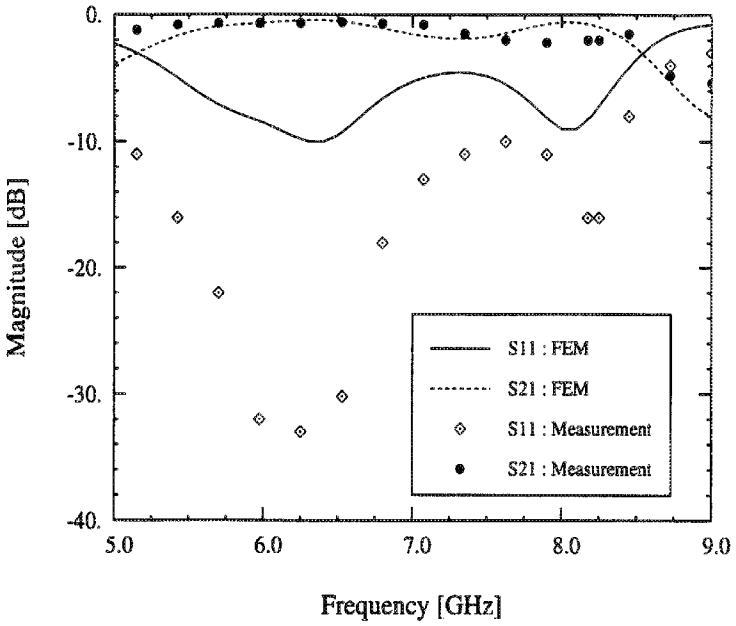


Figure 4.32: Scattering parameters for the coplanar waveguide-to-slotline transition under shielding environment. The design frequency is 6 GHz.

the smooth curved transitions exhibit wide band characteristics as revealed in this study.

4.9 CPW-to-Waveguide Transition

In many millimeter and submillimeter-wave waveguide mounting structures and waveguide probe stations (refer to Fig.4.33), passive and active circuits are embedded into the waveguide [180]–[185]. In these structures, accurate prediction of the driving point impedance and input reflection coefficient is of critical importance to designers. However, the interactions between the lumped or distributed printed circuits and the waveguide are not well understood, and furthermore, the design of such structures heavily depends on experimental data and experience. Thus, the design of a waveguide probe station with maximum coupling from the probe into the waveguide is a tedious and difficult task. In this study, a CPW-to-waveguide transition typically

found in the waveguide mounting or probe structures is characterized using the open boundary FEM and its results are verified using the FDTD technique.

As shown in Fig. 4.34, the waveguide probe is fed by a shielded coplanar waveguide and has the shape of a rectangular patch antenna. The probe is inserted into the waveguide through a slot. Note that the front end of the probe inserted into the waveguide is not connected to any waveguide walls. For the simulation of the infinite waveguide structure having more than one mode as frequency increases, an isotropic absorbing layer optimized for a dominant waveguide mode is applied[1].

The dimensions of the probe as well as the thickness and the dielectric constant of the substrate are very important to achieve maximum energy transfer from input port to the rectangular waveguide. In this study, the thickness of the dielectric substrate carrying the probe is chosen to be 2.0 mm with ϵ_r=12, and the width and length of the probe are 3.8 and 10.8 mm, respectively. This probe is designed to feed a WR-187 rectangular waveguide and the scattering parameters are computed in the 3.1 to 7.4 GHz range. Even though the probe is printed on top of dielectric substrate, the dielectric material under the probe can be removed, resulting in a membrane-supported structure, to maximize the coupling and to minimize the dielectric loss, especially in the high frequency region.

In the simulated frequency range, three different modes, TE^z_{10}, TE^z_{20} and TE^z_{01}, are excited inside the waveguide with cutoff frequencies at 3.15 GHz, 6.30 GHz and 6.82 GHz, respectively. To characterize the probe performance, the magnitude of the reflection coefficient $|S_{11}|$, as well as of the coupling coefficient $\sqrt{1-|S_{11}|^2}$ for the dominant TE^z_{10} mode have been calculated, as presented in Fig. 4.35 (a) and (b). For validation purposes, the results for the reflection and coupling coefficients

[1]see Section 2.10

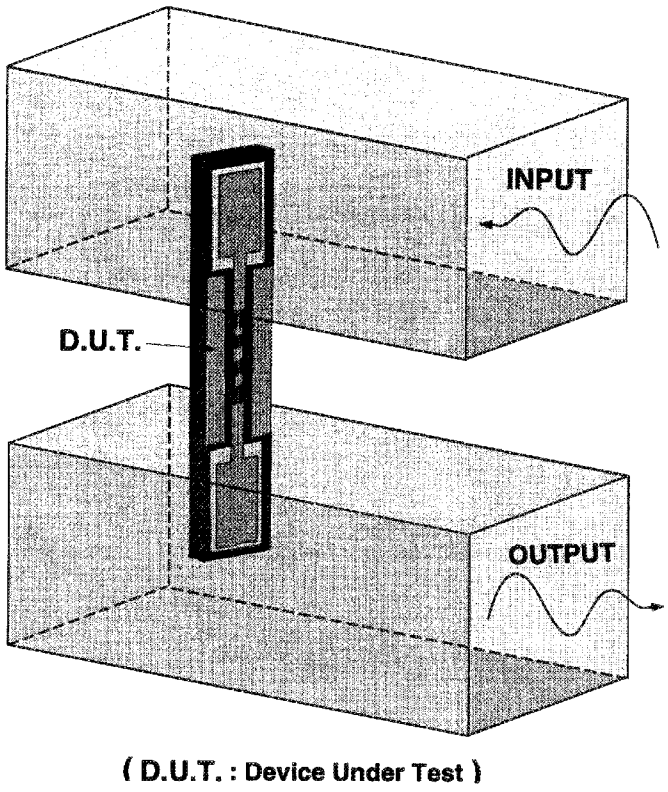


Figure 4.33: An example of a CPW-to-waveguide probe station.

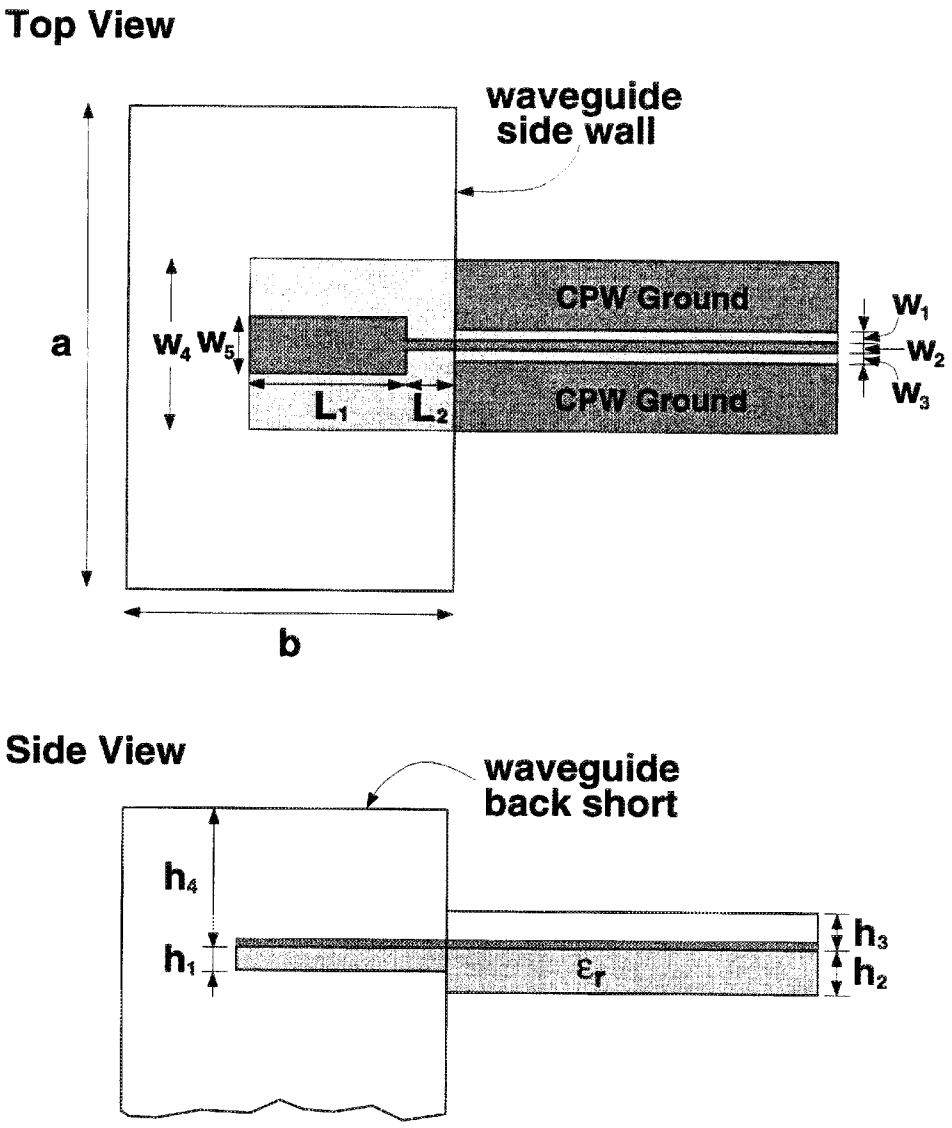
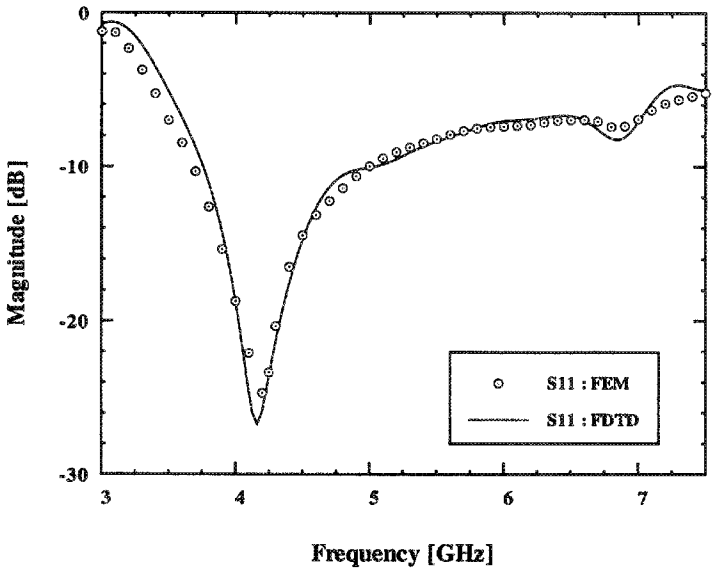
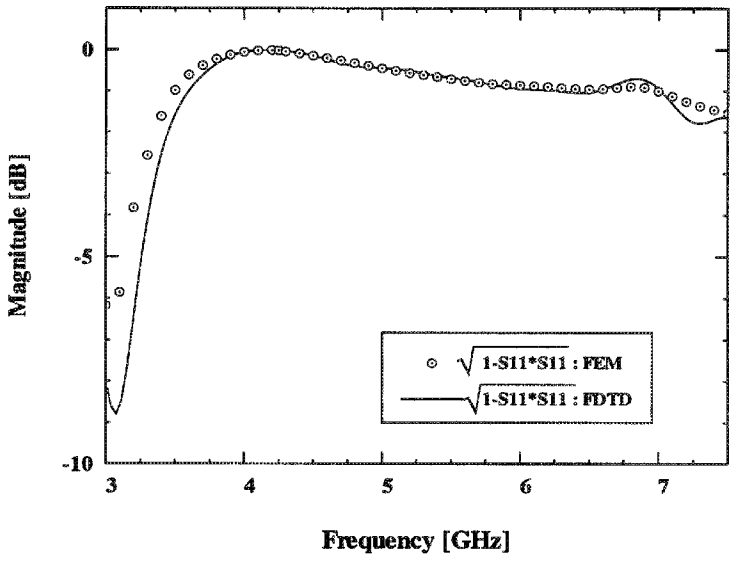


Figure 4.34: CPW-to-waveguide transition: a = 47.6 mm, b = 22.0 mm, L_1 = 10.8 mm, L_2 = 0.8 mm, W_1 = 0.5 mm, W_2 = 0.8 mm, W_3 = 0.5 mm, W_4 = 11.8 mm, W_5 = 3.8 mm, $h_1 = h_2$ = 2.0 mm, h_3 = 1.2 mm, h_4 = 13.2 mm, and ϵ_r = 12.0.



(a)



(b)

Figure 4.35: Scattering parameters of the CPW-to-waveguide transition.

have been compared with the FDTD result, revealing excellent agreement between them. For the geometry analyzed in this study, the 10 dB bandwidth is very small ($\leq$ 1 GHz) which is unacceptable as a wide band probe station. However, further study [28] reveals that a probe having material with lower dielectric constant, such as a membrane-supported structure, can provide much better performances. Also, for a given dielectric material, a wider patch (near square) exhibits improved performances.

4.10 Numerical Convergence

The convergence characteristics of the finite element method largely depend on the electrical parameters under study. Specifically, it has been found that more than 30 cells per guided wavelength are required for the accurate evaluation of a via inductance as indicated in Fig. 4.36, while fewer cells are needed to compute electric fields and resulting scattering parameters. This is due to the form of the utilized basis function, which is linear and has compact support, and the approach followed herein for the computation of the inductance based on the flux/current definition. The electric field edge basis functions used in the study impose a linear variation for the electric field within each tetrahedron, but at the same time, provide a lower order variation for the magnetic field, which remains constant within the same volume Ω_e. The use of higher order basis functions, while it could complicate computations, may provide faster convergence for both the electric and magnetic fields.

In parallel with checking the convergence of a solution with respect to mesh density, we need to make sure that the iterative solver converges. Even though there are many ways to define the convergence criterion for the linear equation solver, in

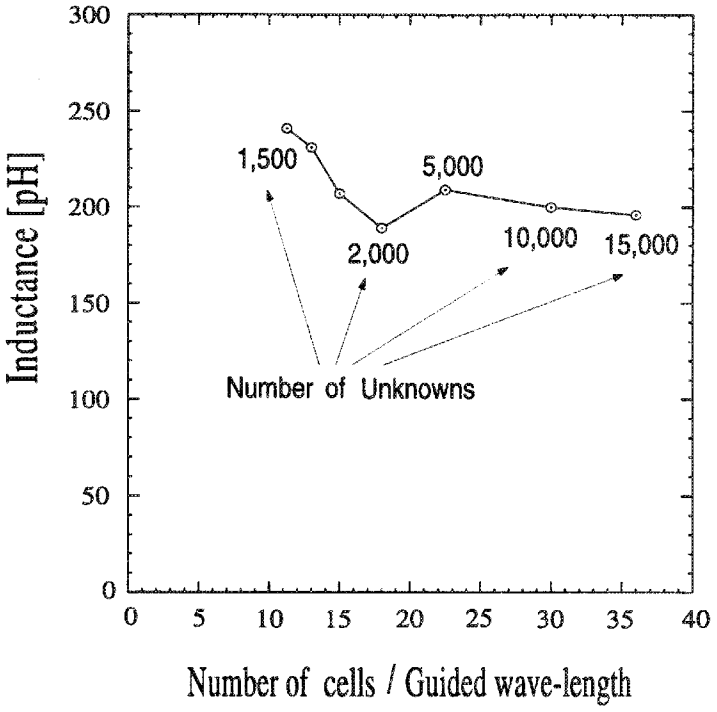


Figure 4.36: An example of the convergence test of the FEM. The inductance of the microstrip ground pad shown in Fig .4.6 as a function of the number of cells per guided wavelength.

this study, it is specified as the relative residual norm, L_2 norm,[2] to be less than 10^{-4} to 10^{-6}. The reason for choosing this error criterion is the sensitivity of the S-parameters with respect to the maxima and minima positions of the voltage standing wave pattern. The scattering parameters are found from the standing wave pattern of the voltage or current waves, and as a result, accurate values for the positions of the extrema are important for stable results.

[2]Let V be a finite-dimensional vector space. For every real number p $\geq$ 1, the function $\| \cdot \|_p$ defined by

$$\| v \|_p = (\sum_i | v_i |)^{1/p}$$

is norm. In particular, it is called L_2 norm, when $p = 2$.

4.11 Conclusions

The finite element method in the frequency domain has been applied to characterize several commonly found discontinuity structures in microwave and millimeter-wave circuits. Specifically, microstrip short-circuit, microstrip ground pad, CPW-to-microstrip through-via transition, channelized CPW-to-microstrip transition, asymmetric 2-port via with plated-through-hole, double via hole, planar/non-planar CPW-to-slotline, and finally CPW-to-waveguide transition have been analyzed and their electrical performance has been studied. The derived results from the FEM agree very well with that of the FDTD. Even further, the field visualizations in the discontinuity regions provide deep insight into the electromagnetic phenomena and their coupling mechanism.

It has been found that a via hole at the center of a microstrip line fails to provide a good DC connection at higher frequencies, resulting in substantial coupling between the two sections of the line. It has also been found that the equivalent inductance for the microstrip via hole and its ground pad is sensitive to the scattering parameters due to ambiguity in the choice of the reference plane. Furthermore, the electromagnetic field distributions around via holes confirm the fact that the current tends to flow through shortest path from the line to ground plane.

Three different types of the CPW-to-microstrip transitions have been found to operate efficiently in the low frequency region for the vertical transition and over a wide frequency range for the channelized transition. In particular, the latter case reveals its frequency independence (up to 40 GHz). In the asymmetric 2-port via hole and double via hole structures, lumped equivalent circuits have been developed for various geometrical parameters to provide guidelines for design of high density

MIC and MMICs. As a feeding network of slot antennas, two types of CPW-to-slotline transitions have also been characterized in a back-to-back fashion. Finally, a preliminary study of the scaled W-band waveguide probe structure with open boundary FEM has been presented.

CHAPTER V

HERMETIC TRANSITIONS

The finite element method in frequency domain technique is applied to characterize the microstrip hermetic transition geometries in an effort to investigate high-frequency effects, and the derived results are compared with that of the the finite difference in time domain technique. Measurements are also performed on these transitions and compared favorably with theories. In this chapter, two different types of transitions structures have been analyzed from 10 to 25 GHz and have been found to be limited in performance by higher return loss as frequency increases. It is shown that microstrip-through-CPW hermetic transitions in the shielded environment may suffer from parasitic waveguide modes which, however, can be eliminated with the use of vias at appropriate locations. The hermetic wall on top of the CPW section shows a relatively small ($\leq$ 2 dB) effect on the original circuit performance. Similarly, the hermetic bead transition shows good performance at a lower frequency region while it degrades as frequency increases. This indicates the need for very careful characterization of transitions intended for use in microwave and millimeter-wave applications.

5.1 Introduction

Hermetic packages are frequently utilized in microwave integrated circuits to provide protection from a hostile environment in addition to reduced electromagnetic interference and radiation leakage. Although hermetic packages are designed to isolate one or more parts of the circuitry and protect them from parasitic electromagnetic noise generated by other analog or digital components, they should not affect the functionality of the packaged circuit. Despite these widely acknowledged and desired attributes of packages, the state of the art in packaging is hindered by design inefficiencies and shortcomings. As mentioned in many studies [149],[150],[186]-[198], the electrical performance of hermetic packages is not considered during the first circuit design stage and, in many cases, it turns out that the presence of the package drastically disturbs circuit characteristics. Recently, more rigorous analysis of the effect of hermetic walls and packages has been reported [170],[199]-[209] and reveals a complex and vague design problem which is largely intensified by uncontrollable package interference effects on circuit performance [193].

Inevitably, the circuit in a package needs to be connected to the outer world by means of effective transitions, and the performance of those transition structures needs to be carefully studied to obtain desirable overall circuit response. In most applications, a hermetic wall, which allows access to the interior of a package, is made of a perfect electric conductor placed on top of a low dielectric constant material (ceramic). The package is placed on top of the circuit in such a way that the input and output lines are sandwiched between the ceramic and the substrate in a stripline type of configuration. The transition of the feeding line, from an outside microstrip to an inside stripline through a hermetic wall, locally alters the characteristics of the

line, thus leading to reflections and many times localized resonance effects. There have been several studies on the effect of hermetic packages on circuit performance based on the use of an appropriate equivalent circuit which replaces the package walls. The element values of this equivalent circuit are computed through a combination of measured data and ideal transmission line theory.

A hermetic package with a coplanar waveguide type transition was used in [188] to achieve input and output port insertion loss of less than 0.25 dB. In [189], a microwave surface mount package was modeled as a combination of coplanar waveguide and microstrip line sections with via holes to simulate the walls and equalize ground potential. In this situation, the circuit components and transmission lines were replaced by electric equivalent circuits whose element values were extracted from measurements. For relatively high-frequency applications (up to 20 GHz) with low transmission line loss and high port-to-port isolation, a surface-mounted MIC package with plated through holes to a microstrip transition structure has been reported [190]. Finally, in [191], a 70 mil microstrip package for a high-frequency high-power circuit application was modeled by equivalent RLC circuit and the values of those equivalent circuit elements were determined by measurements augmented with computer calculations.

In this study, the effects of hermetic walls on the characteristics of two different types of transitions are studied. The first type is an intra-chip transition whereas the second type is an inter-chip transition in which the packaged circuits and connecting lines are printed on different substrates. As a result the transition geometries of the second type include finite gaps between the chips that may cause increased interference or even resonances and may substantially affect performance. The main characteristic of the first type transition is the use of a CPW configuration at the

transition region. This choice is based on the observation that the characteristic impedance of the microstrip line is determined mostly by the substrate thickness and conductor width, whereas that of the CPW is mainly affected by the ratio of the center conductor width to gap width. This implies that a microstrip transition could be more sensitive to the surrounding environment than a transition of CPW type.

In the following sections, a 50 Ω to 50 Ω microstrip-to-CPW transition is studied and the effect of the hermetic wall which is laid on top of the CPW section is investigated. As another type of hermetic transition, a hermetic bead transition structure is also analyzed. Even though the equivalent circuit approaches based on measurement data can provide an understanding of the effect of the hermetic packages on the original circuit, rigorous theoretical investigation is required for the thorough understanding of the electrical performance of these transitions. In this work, the finite element method with edge-based vector basis function is used to characterize various types of hermetic transitions and the finite difference time domain method as a validation tool. The use of both techniques indicates that there is very good comparison with the exception of moderate differences at frequencies close to resonances.

5.2 Intra-chip Transition: Microstrip-through-CPW Hermetic Transition

For an effective transition through a cavity wall, the microstrip line can be gradually changed into a coplanar waveguide which extends beyond each face of the hermetic wall as shown in Figure 5.1. The employed section of the coplanar waveguide is back metallized by the ground of the microstrip line and gives rise to parallel plate waveguide modes, parasitic radiation, and unwanted resonances that occur within

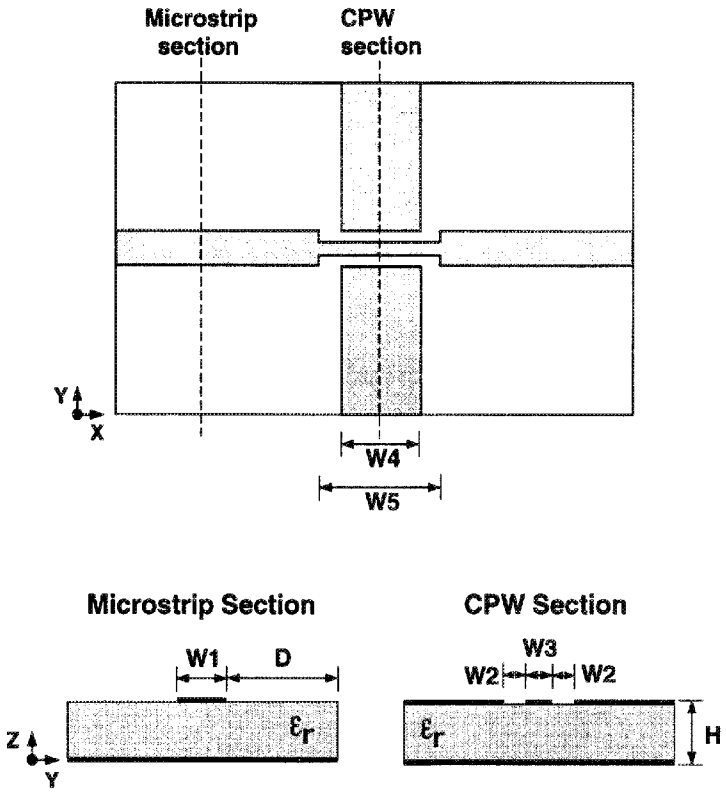


Figure 5.1: Geometry of the Microstrip-to-CPW transition without hermetic wall. W_1 = 0.48 mm, W_2 = 0.14 mm, W_3 = 0.2 mm, W_4 = 2.0 mm, W_5 = 3.0 mm, H = 0.635 mm, ϵ_r = 12.5. Case 1 : D = 2.26 mm. Case 2 : D = 1.76 mm.

the range of the operating frequencies. These resonances are pronounced when the structures are shielded, but are considerably damped when these transitions operate in an open environment.

To understand these effects, the hermetic transition is studied in several steps. At first, a simple microstrip-through-CPW transition, operating in open environment, is analyzed using FDTD and compared with experiments to understand the parasitic effects such as radiation and resonances introduced by the CPW section. The transition structure is then placed inside a closed cavity and characterized by using the FEM and the FDTD. Because the side walls can affect the performance of

the circuit, one needs to be very careful in the choice of cavity width. In this study, to examine the effect of the cavity width, two different cavity sizes are considered without changing the other geometrical factors. In addition, vertical wires, rectangular via holes, extended via holes, and PEC walls are employed to connect the CPW ground planes with the CPW backside metalization to eliminate the excited waveguide mode type resonances, and the effects of these connections on the original circuit are investigated. By doing this, the effects of the resonances due to the cavity and the waveguide-like section under the CPW section are closely examined. Finally, a hermetic wall is introduced to complete the transition geometry.

5.2.1 Open Transition Through a CPW Section

To quantify the performance of the CPW section utilized in the transition, the microstrip-through-CPW planar transition in an open environment without via holes (refer to Fig. 5.1) is studied first. For the computation of scattering parameters using the finite element method, artificial absorbing layers are designed to simulate the open boundary problem as described in Section 2.10. The study in this section has revealed that the transition itself introduces a resonance around 17 GHz with a very low Q due to high parasitic radiation. Furthermore, the same structure is measured [1] experimentally using the 8510 ANA and the Wiltron test fixture. The measurements are performed using a TRL de-embedding procedure and time domain gating is employed to suppress multiple reflections due to the finite substrate. As shown in Fig. 5.2, the overall agreement between the FEM, FDTD and experimental results is satisfactory. The discrepancy observed in the higher frequency end of the spectrum is due to the structural difference between the modeled and measured geometries and the performance of the absorbing boundary conditions utilized in

[1] The measurement was performed by Mr Eray Yasan in the University of Michigan

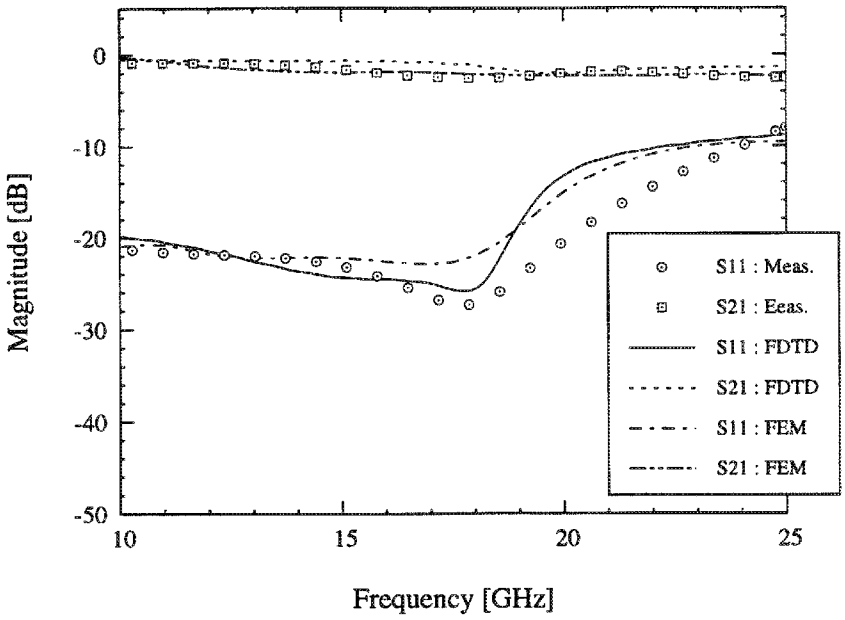
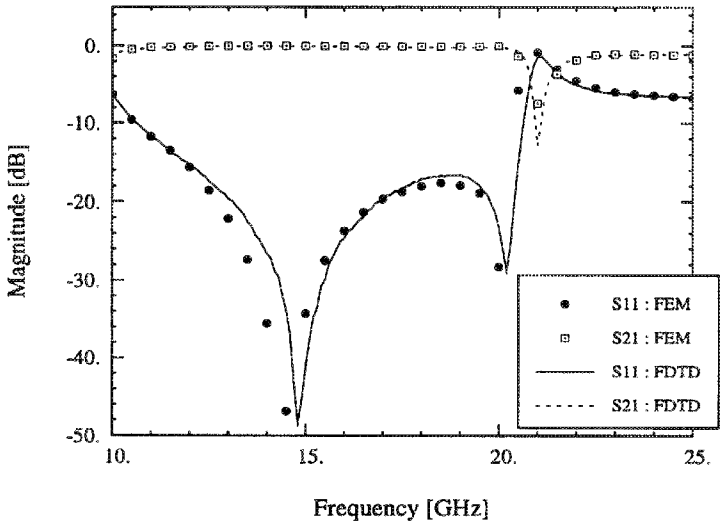


Figure 5.2: S-parameters for the open transition shown in Fig. 5.1. In this case, duroid substrate, which has a relative dielectric constant ϵ_r of 10.8, is used. The CPW ground planes and the PEC underneath the substrate are connected in the measurements.

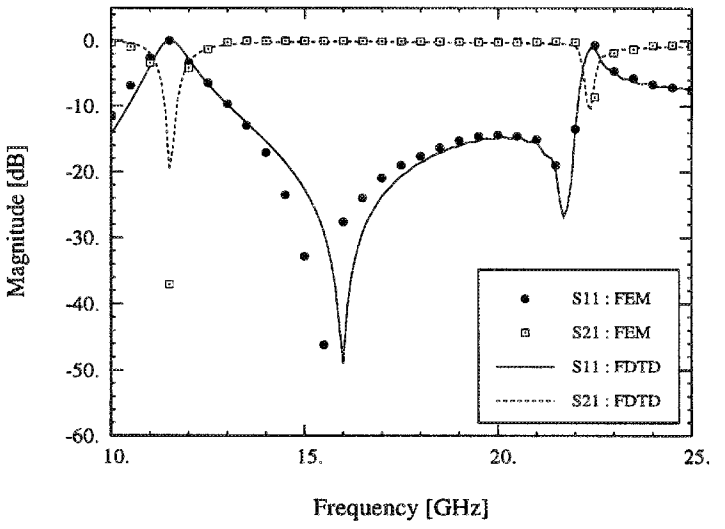
both FEM and FDTD techniques. In particular, the FDTD approximated the exact geometrical factors of the transition to accommodate a uniform mesh and assumed an infinite substrate with the upper CPW ground and the lower conductor at exactly the same potential. However, in the experiment we had to use finite-sized substrate and, even further, the CPW ground planes and lower conductor were connected using conducting strips to provide the same potential.

5.2.2 Closed Transition Through a CPW Section

Following the treatment of the open transition, the same geometry is placed inside a metallic cavity and is characterized for two different cavity sizes. Fig. 5.3 shows the computed S-parameters for $D = 2.26$ mm and 1.76 mm. As seen from the figures, the presence of the cavity, even though it is designed to be below cutoff at the frequencies of interest, drastically affects the performance by introducing high Q resonances. As



(a)



(b)

Figure 5.3: Comparison between FEM and FDTD data for (a) case 1 ($D = 2.26$ mm) and (b) case 2 ($D = 1.76$ mm).

expected [199]-[201], these resonances are shifted to higher frequencies as the cavity size decreases. For the case $D = 2.26$ mm, there are two resonances in $|S_{21}|$ which are clearly observed at 21 GHz and around 9 GHz (not shown in the figure). These strong resonances are due to TE-like modes [210]-[211] excited in the region between the ground planes of the CPW section, its back metalization, and the side walls. In particular, the resonance around 10 GHz corresponds to the TE_{10} mode of that waveguide-like section as clearly shown in Fig. 5.7(a). The dips in $|S_{11}|$ around 15 GHz in Fig. 5.3 are due to the length of the narrow microstrip line (refer to W_5 in Fig. 5.1) as confirmed through another numerical experiment in Fig. 5.4. That is, when the effective length of that section is $\lambda_g/2$, total transmission can occur with the same input and output transmission lines as in our cases. Also, similar argument can be applied to the drops at 20 and 21 GHz in Fig. 5.3 with the length of the CPW section. The return loss of case 1 is less than -10 dB in the frequency range of 11 to 20 GHz showing a good transition performance.

Theoretical data derived by the FEM show very good agreement with that of the FDTD method and reveal resonance phenomena indicating the need for a mechanism to suppress them. The next subsections will be devoted to the investigation of variety of mechanisms needed to suppress the excitation of the parasitic waveguide modes responsible for the previously observed resonances.

5.2.3 Vertical Wire Grounding

As a first attempt to eliminate the effect of the excited waveguide modes under the CPW section, vertical wires are inserted between the CPW ground planes and the PEC back-metalization under the substrate as shown in Fig. 5.5. On either side of the longitudinal symmetry plane, four wires (400 μm apart) are inserted at a

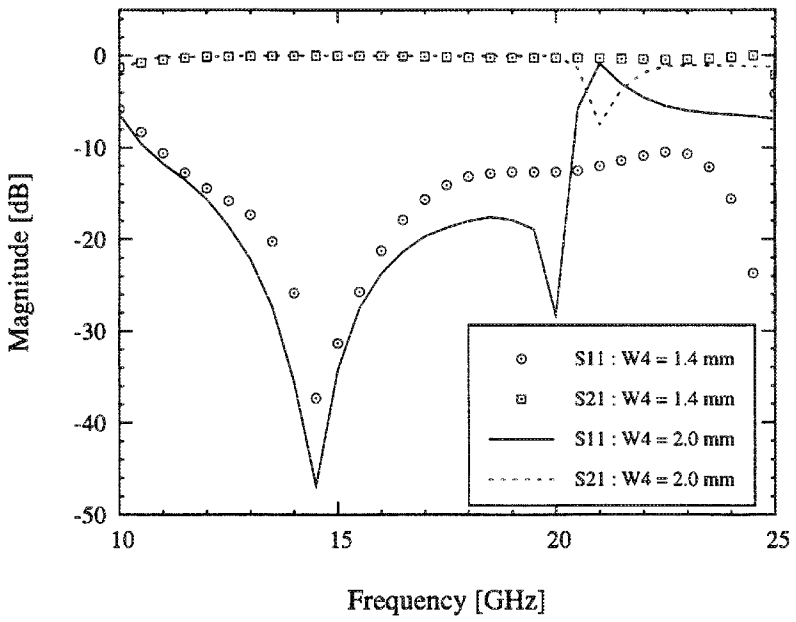


Figure 5.4: S-parameters for two different size of CPW ground plane (W_4 in Fig. 5.1). Other geometrical factors are remain the same.

distance of 466 μm from the symmetry plane. These vertical wires are implemented as infinitely thin PEC wires for convenient numerical simulations.

The scattering parameters of the modified structure are computed using the finite element method and show very good agreement with the FDTD results as shown in Fig. 5.6. The results shown in the figure indicate that, in the low frequency region (up to 13 GHz), the transition circuit performs fairly well, while its performance degrades as the operating frequency increases beyond 13 GHz. This degradation indicates that the wires play a role in increasing the resonance frequency, but do not suppress it completely. This is due to a waveguide-type resonance (TE_{10}-like mode) which develops between the wires and the side walls under the CPW section. They will always exist in some form as long as there is an enclosure. Fig. 5.7(b) shows the vertical electrical field distribution around the transition region at 10 GHz.

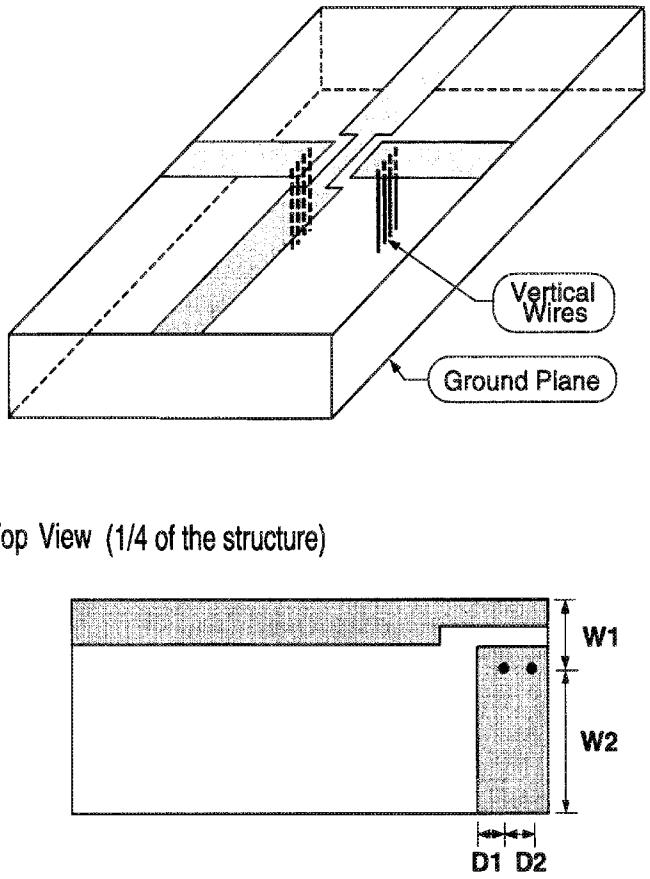


Figure 5.5: Geometry of the microstrip-through-CPW transition without hermetic wall : vertical wire grounding. $W_1 = 0.466$ mm, $W_2 = 2.034$ mm, $D_1 = 0.40$ mm, and $D_2 = 0.40$ mm. Other geometrical factors are the same as those in the previous example.

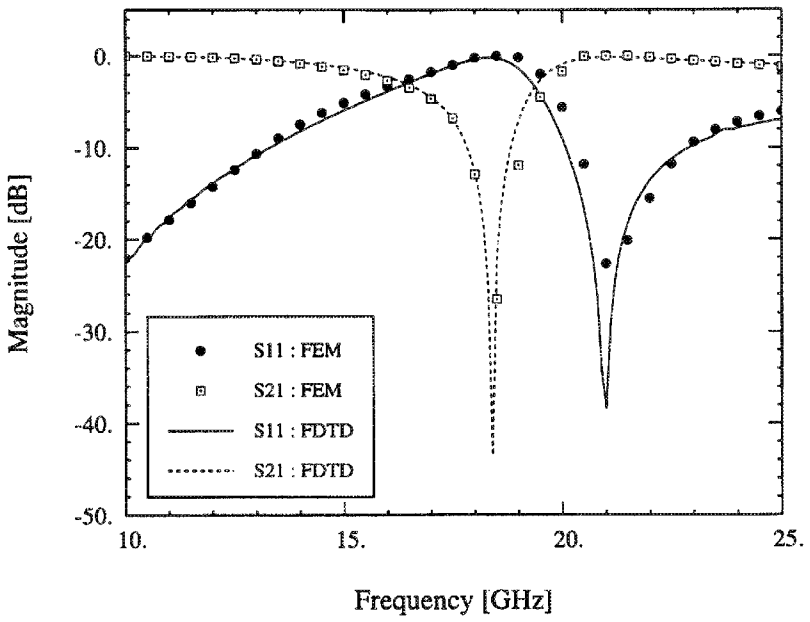


Figure 5.6: S-parameters of the vertical wire grounding case.

5.2.4 Rectangular Via Hole Grounding

In this subsection, rectangular PEC via holes are used to connect the CPW ground planes to the bottom PEC surface as shown in Fig. 5.8. There are four vertical via holes, and the size of each via hole is 600×452 μm and the height is 635 μm, which is the same as the substrate thickness. Also, the ground plane of the CPW is reduced to half of the original size to alleviate the strong resonance under the CPW grounds.

The calculated S-parameters are shown in Fig. 5.9. The overall frequency response of the structure is similar to the wire grounding case, but the resonant frequency is shifted to a further higher frequency region. This is due to the reduced distance ($W_3 + W_4 = 1.582$ mm in Fig. 5.8) between the PEC via walls and the cavity side walls. Note that the aforementioned waveguide-like structure has incomplete side and top walls as shown in the figure, and this explains the reduced Q at the resonance of approximately 23 GHz.

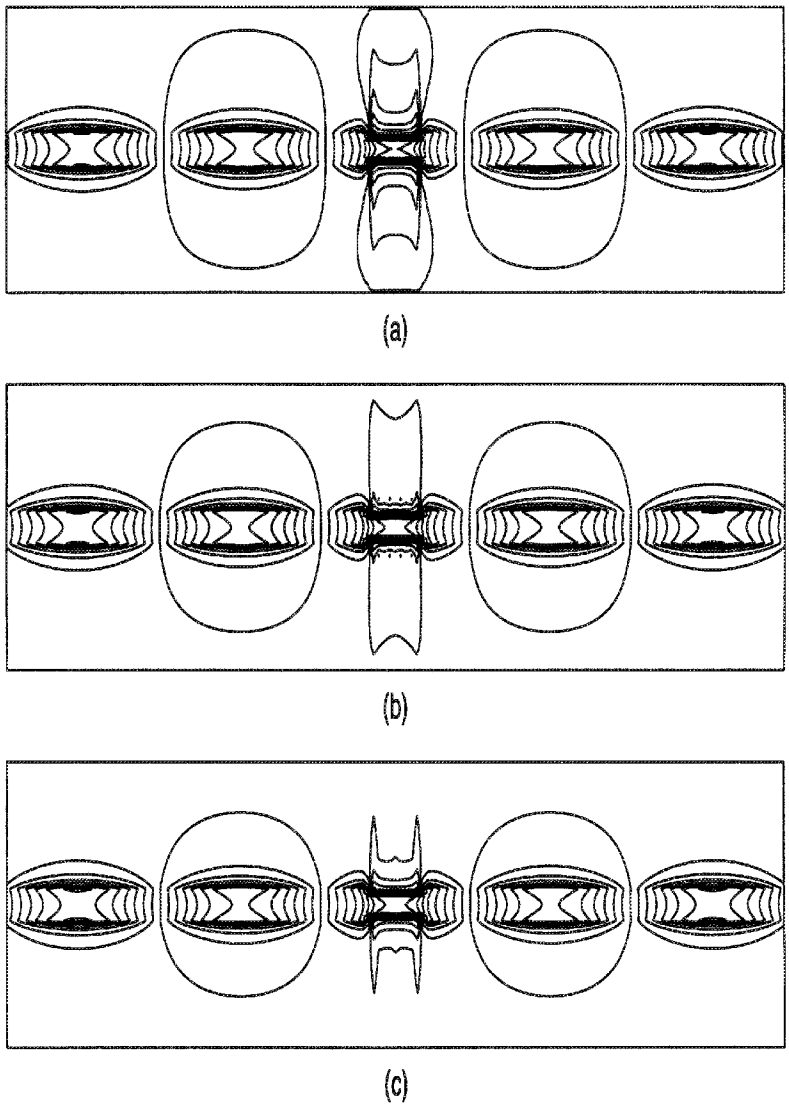


Figure 5.7: Electric field ($\mathbf{E}_z$) distribution around the transition region at f=10 GHz. (a) Microstrip-through-CPW transition, (b) Microstrip-through-CPW transition with vertical grounding wires, and (c) Microstrip-through-CPW transition with extended rectangular vias.

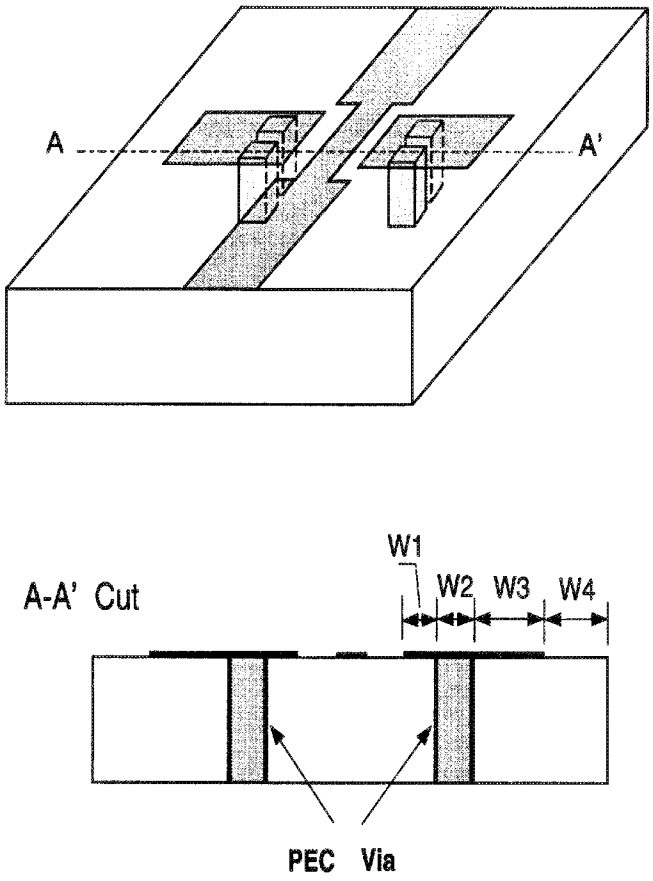


Figure 5.8: Geometry of the microstrip-through-CPW transition without hermetic wall : Rectangular via hole grounding with finite size CPW ground plane. The size of the via hole is 0.452×0.6 mm. $W_1 = 0.226$ mm, $W_2 = 0.452$ mm, $W_3 = 0.452$ mm, $W_4 = 1.13$ mm. Other geometrical factors are identical to the first example.

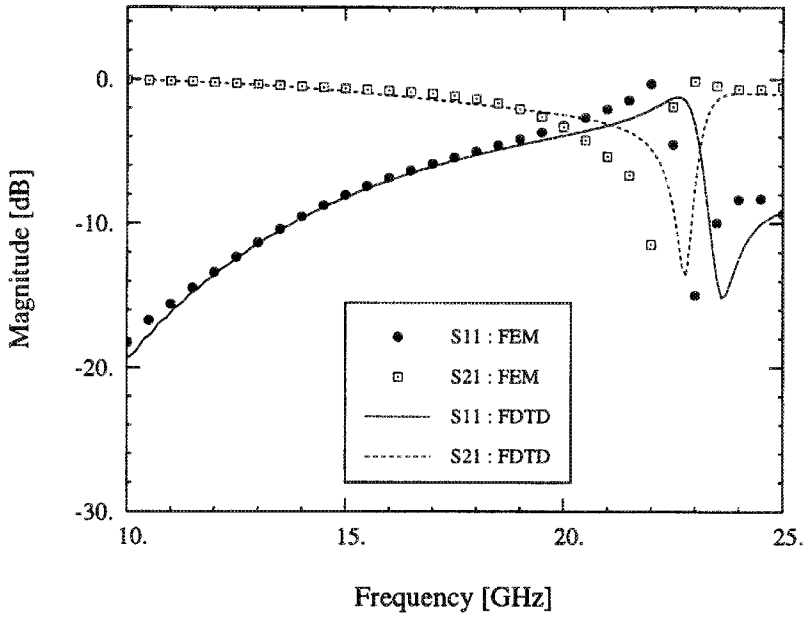


Figure 5.9: S-parameters for the rectangular via hole grounding case.

5.2.5 Extended Rectangular Via Hole Grounding

To avoid excitation of resonant waveguide-like modes under the conductor-backed CPW section, extended via holes are placed under the CPW ground planes as shown in Fig. 5.10 and their effect is investigated. Analysis of this structure confirms that the extended rectangular via holes suppress unwanted resonances (refer to Fig. 5.11). The field distribution around the transition region also verifies the suppression of the resonant field under the CPW ground pads. As shown in Fig. 5.11, the overall return loss is improved by about 2 dB by extending the via holes while the performance of the transition structure degrades as frequency increases. Specifically, over 15 GHz, it has greater than -10 dB return loss. The effect of the extended vias may be simulated by an array of vias.

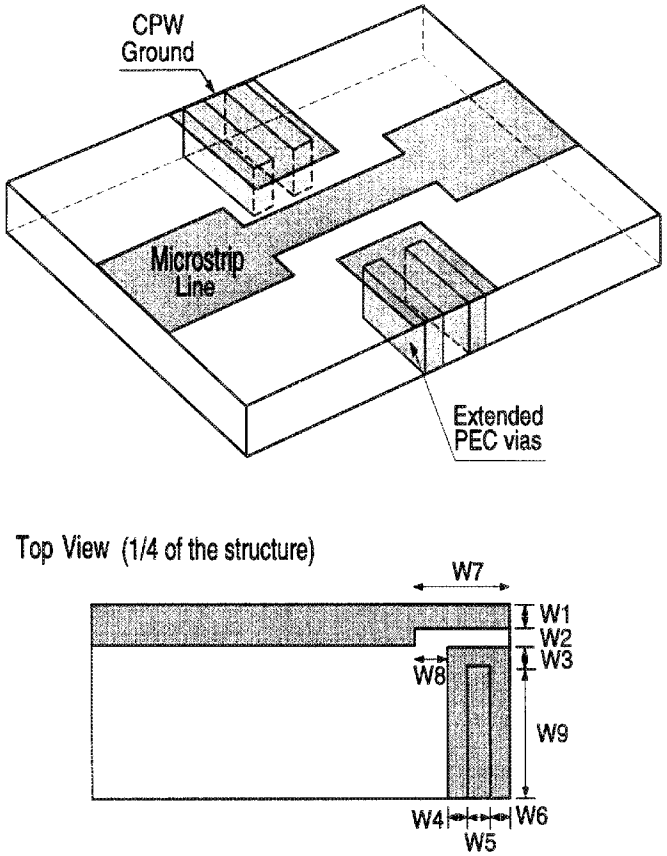


Figure 5.10: Geometry of the microstrip-through-CPW transition without hermetic wall : extended rectangular via hole grounding. The top view shows one quarter of the whole geometry. $W_1 = 0.1$ mm, $W_2 = 0.14$ mm, $W_3 = 0.226$ mm, $W_4 = 0.2$ mm, $W_5 = 0.6$ mm, $W_6 = 0.2$ mm, $W_7 = 1.5$ mm, $W_8 = 0.5$ mm, $W_9 = 2.034$ mm.

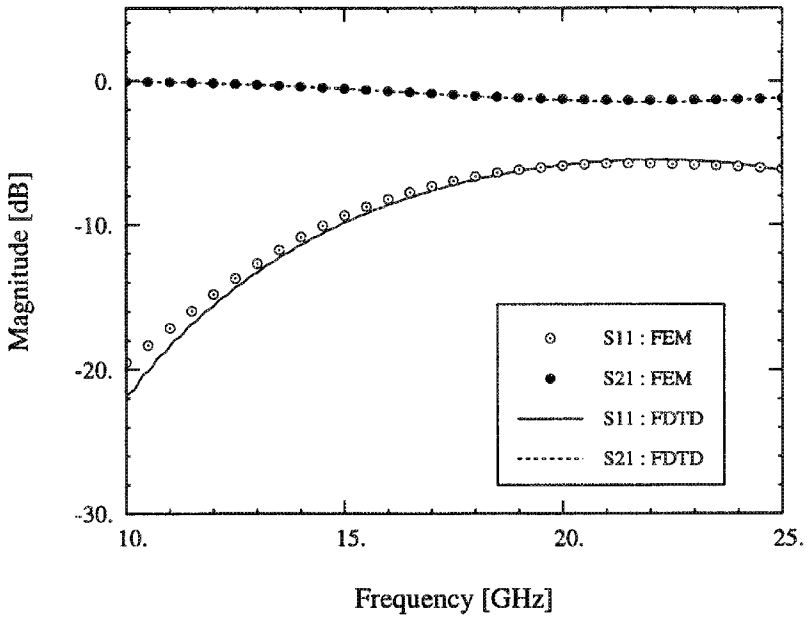


Figure 5.11: S-parameters of the extended rectangular via hole grounding case.

5.2.6 PEC Wall Grounding

In this subsection, the effect of further extension of the via holes to form solid walls under the CPW ground pads is studied. The schematic view is shown in Fig. 5.12 and Fig. 5.13 shows the computed frequency response of the transition with solid walls under the CPW ground pads. As expected, the transition characteristics are improved over the previous structure having extended via holes. After the PEC walls are inserted, the resonance phenomenon is completely vanished, and as a result the $|S_{11}|$ is decreased. In particular, in the high frequency region, the circuit performance with the solid PEC wall is improved by 2 to 3 dB in return loss.

Up to this point, the effects of the cavity size, vertical wires, and various shapes of via holes which connect the CPW ground to the PEC surface under the substrate have been examined. It is worth mentioning that the vertical via holes having various shapes can be implemented in practical circuits by removing the substrate material

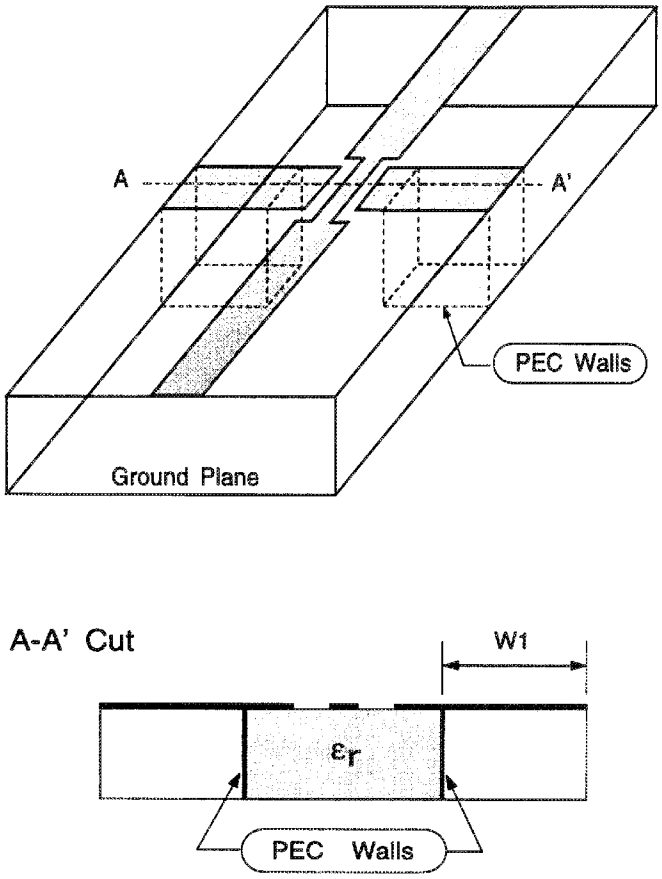


Figure 5.12: Geometry of the microstrip-through-CPW transition without hermetic wall : PEC wall grounding. W_1 = 2.034 mm and other geometrical factors are identical to the first example.

followed by back metallization, so called micro-machining technique. In the next subsection, the effect of the hermetic wall on top of the circuit is studied.

5.2.7 Microstrip-through-CPW Transition With Hermetic Wall

In this subsection, the effect of the hermetic wall on top of the microstrip-through-CPW transition having extended vias is investigated. The hermetic wall is formed by a metallic wall bonded on top of a ceramic or dielectric material which forms the upper part of the wall. Fig. 5.14 shows the geometrical details of the hermetic transition structure with extended via holes. The height of the ceramic is equal to the

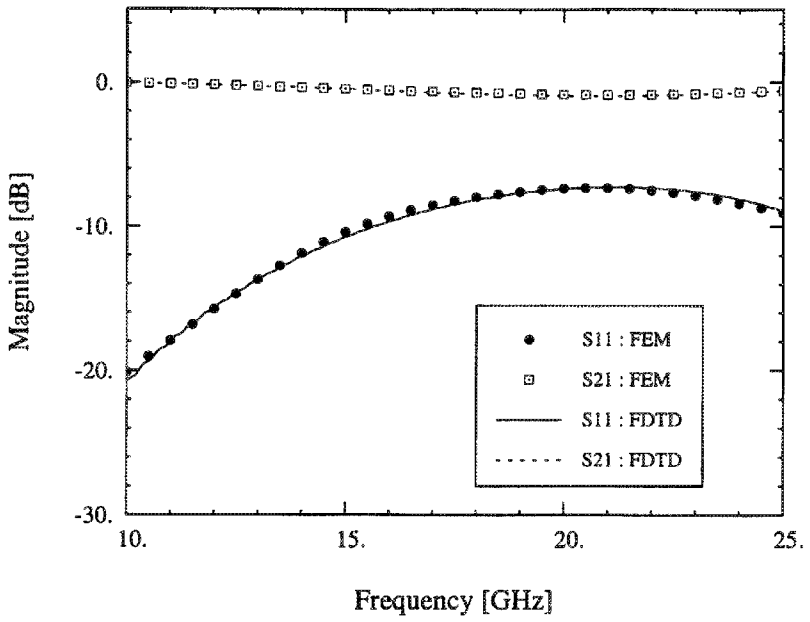


Figure 5.13: S-parameters of the PEC wall grounding case.

substrate thickness while its relative dielectric constant is chosen to be $\epsilon_{r2} = 2.3$, in contrast to the 12.5 of the substrate. From a circuits point of view, the ceramic on top of the transmission line may alter the characteristic impedance of the line, and hence it may affect the resulting S-parameters. Since there is a conducting plane on top of the ceramic, the CPW with hermetic wall can be considered as an inhomogeneously sandwiched CPW section and its characteristic may be slightly affected.

In Fig. 5.15, the magnitude of the scattering parameters obtained using the FEM and FDTD are compared. After placing the hermetic wall on top of the CPW section, the overall return loss has increased by 2 to 3 dB while its frequency dependency has remained unchanged. In the whole frequency region considered, from 10 to 25 GHz, the return loss is less than -5 dB. However, in the low end of this frequency region, up to 13 GHz, the return loss is less than -10 dB. The effect of the hermetic wall is small as expected from the field distribution in the CPW structure.

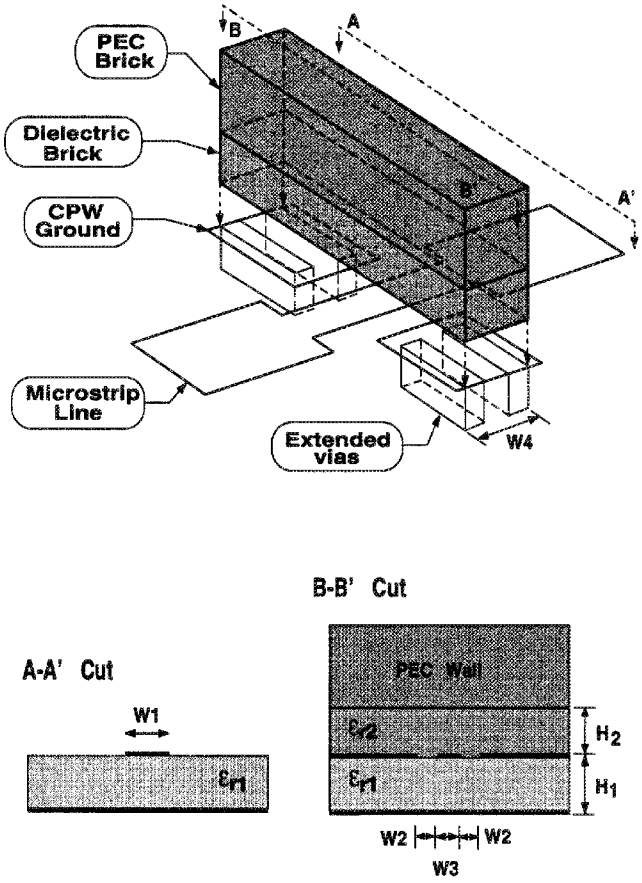


Figure 5.14: Geometry of the microstrip-through-CPW transition with hermetic wall on top of the extended PEC via grounding case. The width of the hermetic wall is 1.6 mm. $W_1 = 0.48$ mm, $W_2 = 0.14$ mm, $W_3 = 0.2$ mm, $W_4 = 1.6$ mm, $H_1 = H_2 = 0.635$ mm, $\epsilon_{r1} = 12.5$, and $\epsilon_{r2} = 2.3$.

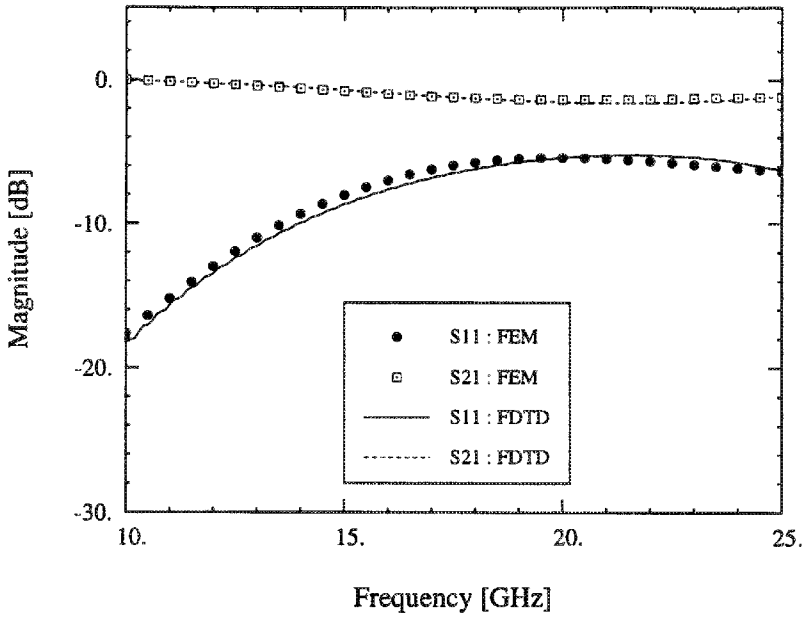


Figure 5.15: Comparison of the S-parameters for the transition with hermetic wall on top and extended PEC via under the circuit plane.

5.2.8 W-Band Application of the Hermetic Transition

Based on the previous results, a transition from the microstrip-through-CPW section has been designed to investigate the possibility of using the hermetic wall transition in the W-band application. The hermetic wall is built on top of the CPW section of the microstrip-through-CPW transition, and the width and thickness are chosen to be 250 μm and 100 μm, respectively, with a dielectric constant of 2.5. The S-parameters computed in the shielded environment using the FEM are shown in Fig. 5.16. It is observed that the transitions with and without the hermetic wall show very similar characteristics. In particular, in the high frequency region, over 70 GHz, the transition reveals very good performance, having less than -20 dB of return loss.

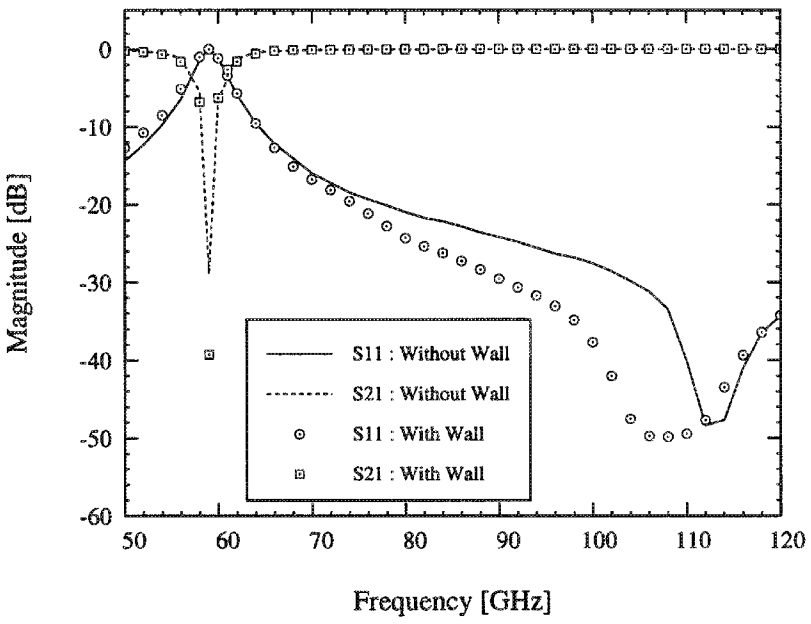


Figure 5.16: S-parameters for the transition with and without hermetic wall on top of the CPW section. The geometrical factors : $W_1 = 70$ μm, $W_2 = 30$ μm, $W_3 = 40$ μm, $W_4 = 300$ μm, and $W_5 = 350$ μm (refer to Figure 2). The width and height of the dielectric brick under the PEC wall are 250 μm and 100 μm, respectively.

5.3 Inter-Chip Transition: Hermetic Bead Transition

Another type of commonly encountered feed-through, the hermetic bead transition structure, is analyzed in this section. Unlike the previous intra-chip transitions, the hermetic bead transition, so called, inter-chip transition, can be used as an effective interconnection method between chips and other circuit components through PEC wall. For optimum design of the transition structures, several different configurations, including square and circular dielectric rings, are carefully investigated in this study to provide design guidelines.

5.3.1 Squire Dielectric Ring

As shown in Fig. 5.17, a circular coaxial line is approximated with rectangular-shaped stripline and the dimensions are chosen to have 50 Ω characteristic impedance. The dielectric constant of the ring is also chosen as 10.8, which is the same as the substrate. The thickness of the hermetic wall and the air gap spacings are chosen as 1.5 mm and 0.4 mm, respectively.

S-parameters computed using the FEM are presented in Fig. 5.18 showing very good agreement with the FDTD results. The hermetic bead transition performs quite well in the low end of the frequency spectrum as expected, while the return loss degrades as frequency increases. To improve the performance of the transition and to provide useful design information, the air gap spacing (L_2) is varied from 0.4 mm to 0.1 mm. The computed S-parameters are shown in Fig. 5.19 for three different cases. As can be observed, the overall transition performances are improved as the air gap spacing is decreased. Although the geometrical factors are not optimized for better transition characteristics, the overall performance of the circuit gives an essential understanding of the performance of this type of transition.

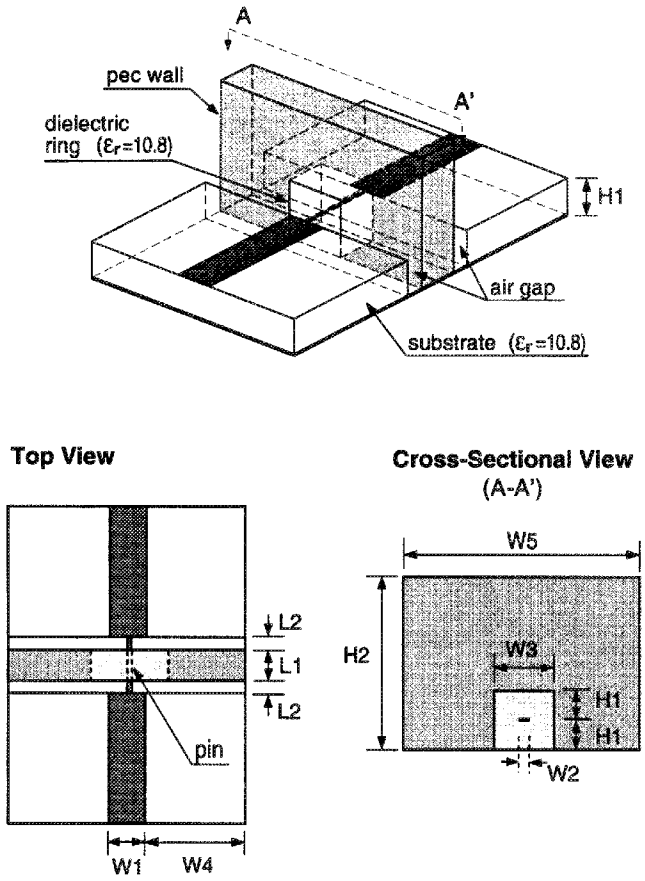


Figure 5.17: Geometry of the hermetic bead transition. $W_1 = 0.55$ mm, $W_2 = 0.21$ mm, $W_3 = 1.27$ mm, $W_4 = 2.225$ mm, $W_5 = 5.0$ mm, $H_1 = 0.635$ mm, $H_2 = 4.0$ mm, $L_1 = 1.50$ mm, $L_2 = 0.40$ mm, and $\epsilon_r = 10.8$.

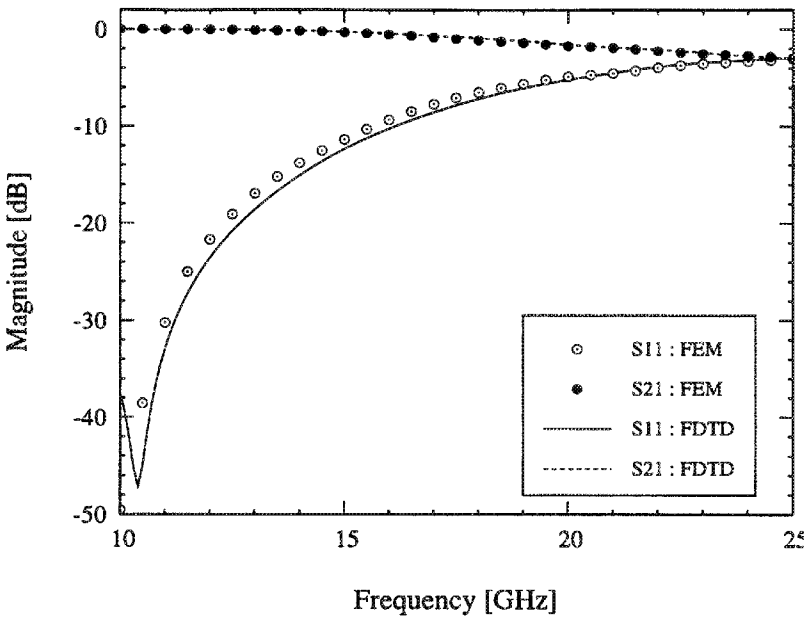


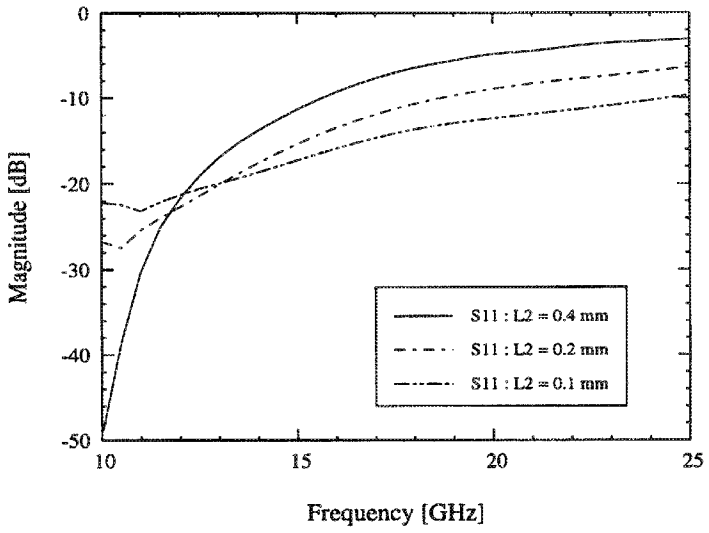
Figure 5.18: S-parameters of the hermetic bead transition with square dielectric ring.

5.3.2 Circular Dielectric Ring

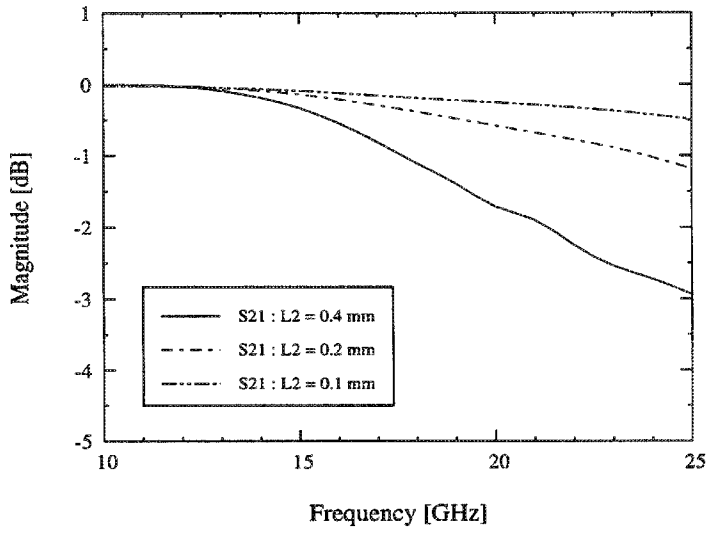
For an investigation of the effect of the rectangular approximation of a circular ring, the hermetic bead transition with circular dielectric ring is studied in this subsection. The radius of the circular ring is chosen as H_1 so that the circular ring is fit into the square hole. As shown in Fig. 5.20, the performance of the circular ring is very similar to that of the square one except at the lower frequency region. The slightly degraded performance of the circular ring is mainly due to the effect of the conductor placed closer than the square one.

5.4 Conclusions

The finite element method has been successfully applied to characterize the effect of the hermetic wall/bead transitions commonly found in MIC and MMIC packaging. The derived FEM results agree very well with the FDTD data in low as well as high frequency regions. It has been shown that the grounding structures (wires, vias, and



(a)



(b)

Figure 5.19: Comparison of the S-parameters for the hermetic bead transition of three different air gap width L_2. (a) $|S_{11}|$ and (b) $|S_{21}|$.

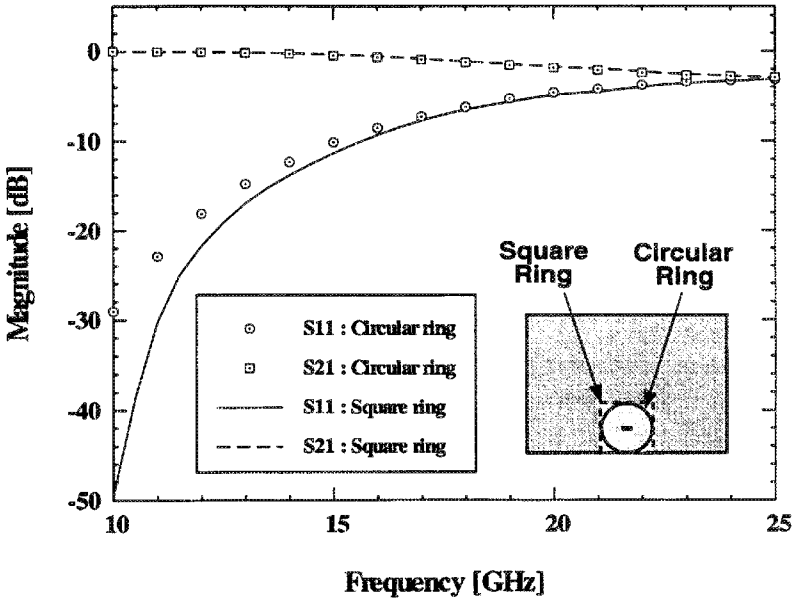


Figure 5.20: Comparison of the S-parameters of the hermetic bead transition with square and circular dielectric ring of radius equals H_1.

PEC walls), which are placed under the CPW ground pads to equalize the potential between the ground planes on the upper and lower surfaces, play a key role in the performance of this type of transition. The hermetic wall placed on top of the CPW transmission line section degrades the return loss of the original circuit only by a couple of decibels. In addition, a hermetic bead transition structure was designed and analyzed for the circular- and rectangular-shaped rings, and the effect of air gap spacing is also studied. The performance of this transition is found to gradually degrade as frequency increased.

CHAPTER VI

K/Ka-BAND MMIC PACKAGE

In this chapter, electromagnetic leakage and spurious resonances in a K/Ka-band (18 - 40 GHz) MMIC hermetic package designed for a phase shifter chip are studied using the finite element method and the numerical simulation results are compared with the measurement data. Both the measured and calculated data indicate several spurious resonances in the 18 to 24 GHz region, and the origin of this phenomenon is identified by virtue of the modeling capability of the FEM. Moreover, the effect of DC bias lines, bond wires, shielding and the asymmetry of the package on electrical performance are closely examined. In addition, the effect of adding a resistive coating to the inside surface of the package lid and also the use of dielectric packaging materials with very high loss tangent are studied in view of the suppression of the spurious resonances. Finally, design guidelines for the improved package are presented.

6.1 Introduction

In general, packages for low frequency integrated circuits (ICs) have been designed without consideration of the high frequency effects and have revealed satisfactory performance. However, high performance packages, especially for microwave and millimeter-wave integrated circuit applications, should satisfy stringent mechan-

ical, electrical and environmental requirements. From a mechanical and environmental point of view, a package should provide protection to the internal circuits from the surroundings. Furthermore, packages are required to exhibit minimum insertion loss, good isolation between the ports as well as electromagnetic shielding for minimum interference [193, 195]. Another important electrical requirement of a package is non-invasiveness with respect to circuit performance [212]: a package fails electrically if parasitic cavity resonances substantially deteriorate circuit performance. As a result of all of these requirements, successful development of a high frequency package requires careful design strategies. Recently, low cost high performance MMIC packages have been developed by using approximate equivalent circuit models or experimental data [186, 188]. However, due to the limited accuracy of the modeling tools, the designed packages exhibit a serious performance degradation at higher frequencies. To overcome the above difficulties in designing high-frequency high-performance package, frequency domain full-wave electromagnetic tool, FEM, is applied [31, 208, 209, 213] for various applications.

The goal of this study is to characterize the electrical performance of a K/Ka-band hermetic package designed for a MMIC phase shifter (refer to Fig. 6.1) and comprehend the parasitic effects introduced by the package geometry. For thorough understanding of the package performances, the effects of the various features of the package, such as metal filled vias, DC bias lines, bond-wires, structural symmetry/asymmetries, and even the effect of the test fixture on the circuit performance are extensively investigated. Furthermore, the use of dielectric packaging materials with high loss tangent and the influence of a resistive coating on the inside surface of the package lid are also examined. For the EM characterization of the K/Ka-band MMIC package, a parallelized three dimensional finite element method, which

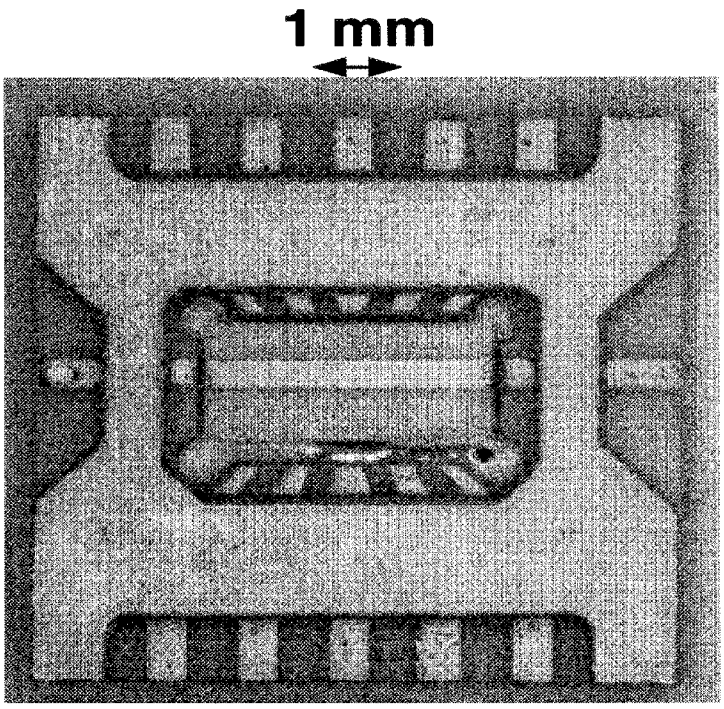


Figure 6.1: Top view of the K/Ka-band MMIC package.

is optimized on the distributed memory machine with task parallelization strategy, is applied [20, 29]. The parallelized 3D FEM code exhibits near linearly scalable performance improvement due to the frequency independent nature of the frequency domain FEM. To the best of the author's knowledge, this is the first comprehensive high frequency full-wave treatment for an existing millimeter-wave package.

The modeling effort described herein is divided into three parts. In the first part, the input and the output microstrip lines are symmetrically located with respect to the two planes of symmetry of the package. In addition, the package is considered to be free standing, i.e., totally isolated. Under these assumptions only one quarter of the package needs to be considered, and as a result the modeling effort is computationally simpler. In the second case, the input and the output microstrip lines are asymmetrically located with respect to one of the plane of symmetry. This is of

more general interest since in real applications the transmission lines on the MMIC chip need not be symmetrically located. In the last part, the microstrip lines are asymmetrically located and the package is placed inside a test fixture. By placing the package inside the text fixture, the interactions between the fields leaking through the package dielectric walls and the surroundings can be modeled. This model is of great practical interest since it points towards ways and means to improve future package performance. The modeled characteristics are compared with experimental results and show very good agreement. In addition, the effects of the three different types of packaging features, such as additional metal-filled vias, resistive coating, and lossy packaging materials, are carefully examined to improve the package performance. This modeling procedure has the potential to predict the performance of other types of packages such as those used in wireless communications which include multi-chip modules.

6.2 Modeling of the Package

A schematic is shown in Fig. 6.2 for the K/Ka-band MMIC package fabricated by Hughes Aircraft Company for the NASA Lewis Research Center. The package has 50 Ω microstrip input/output feed lines for the RF signal and two sets of five metal lines on either sides for DC bias and control. In addition, a set of twelve metal filled vias tie the top and bottom PEC ground planes to provide mechanical strength and also serve as an EM shield. The package is fabricated from alumina (92 % pure, $\epsilon_r = 9.5$) using the high temperature co-fired ceramic (HTCC) process. To characterize the package, a 50 Ω through line is placed in the recess as shown in Fig. 6.2 and is wire-bonded to the input/output microstrip feed lines. The peripheral dimensions of the package are $7.112 \times 7.112 \times 0.762$ mm. It can be observed from

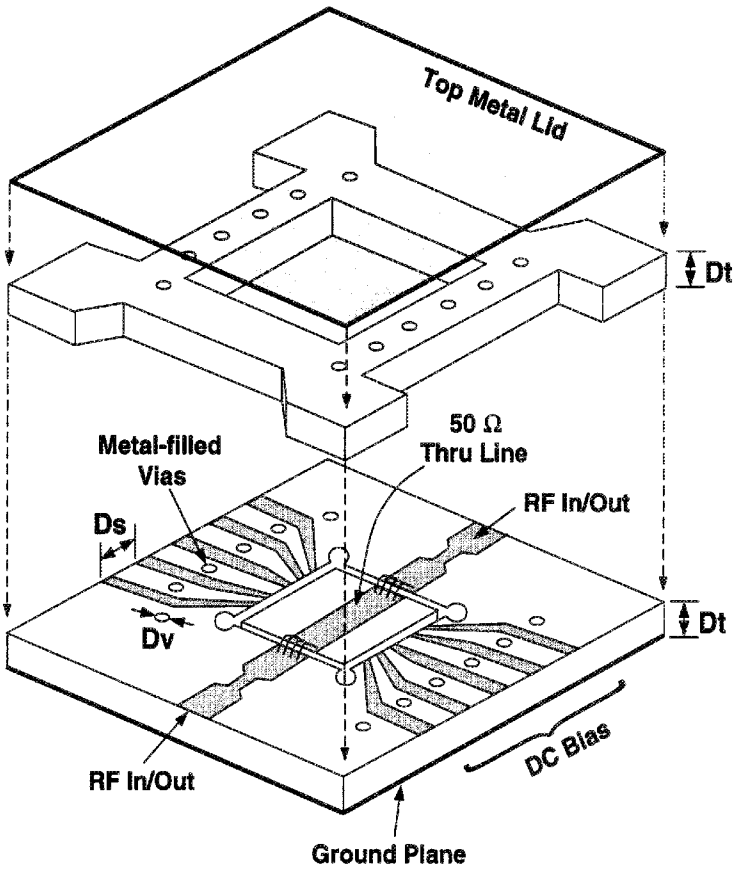


Figure 6.2: Schematic diagram of the K/Ka-band hermetic package designed and manufactured for a MMIC phase shifter chip. The diameter of the vertical metal filled vias are $D_v = 0.203$ mm and the distance between these vias are $D_s = 1.016$ mm. The upper and lower alumina layers are each 0.381 mm thick (D_t).

the figure that the metal filled vias and the input/output microstrip feed lines are displaced towards one side of the package introducing a package asymmetry. This asymmetry is attributed to the specific geometry of the MMIC phase shifter which the package intends to house.

While this package provides hermeticity, it does not provide perfect electromagnetic shielding, and as a result the packaged circuits are exposed to a semi-open environment. For the simulation of this environment, artificial absorbing layers have been designed using lossy isotropic dielectrics as shown in Fig. 6.3. The performance of the absorber is controlled by assigning a certain amount of losses in the absorbing material and by specifying its thickness [1]. In this study, we designed two different types of isotropic absorbing materials for air and dielectric side terminations. The material parameters are chosen to be $\epsilon_{AA}^{air} = \mu_{AA}^{air} = 1.0 + j10.0$ for the air side, and $\epsilon_{AA}^{diel} = 9.5 + j15.0$ and $\mu_{AA}^{diel} = 1.0 + j1.5789$ for the dielectric side. The thickness t of the artificial absorbers is assigned to be 0.70 mm to allow enough damping of the fields inside of the absorbers and to minimize the computational domain. It is well known that this type of absorber performs well for near-normal incident fields.

6.3 Numerical and Experimental Results and Discussions

6.3.1 Modeling of Isolated Symmetric Package

First of all, an isolated symmetric package is designed and modeled, in which the structural details are very close to that of Fig. 6.2 except a few minor modifications for symmetric arrangement. The input/output microstrip lines and the through line are adjusted to the center of the package, and the two asymmetric metal filled vias are aligned in line. The computed scattering parameters are shown in Fig. 6.4. The return loss is less than -20 dB over the entire frequency range and the insertion

[1] refer to Section 2.10

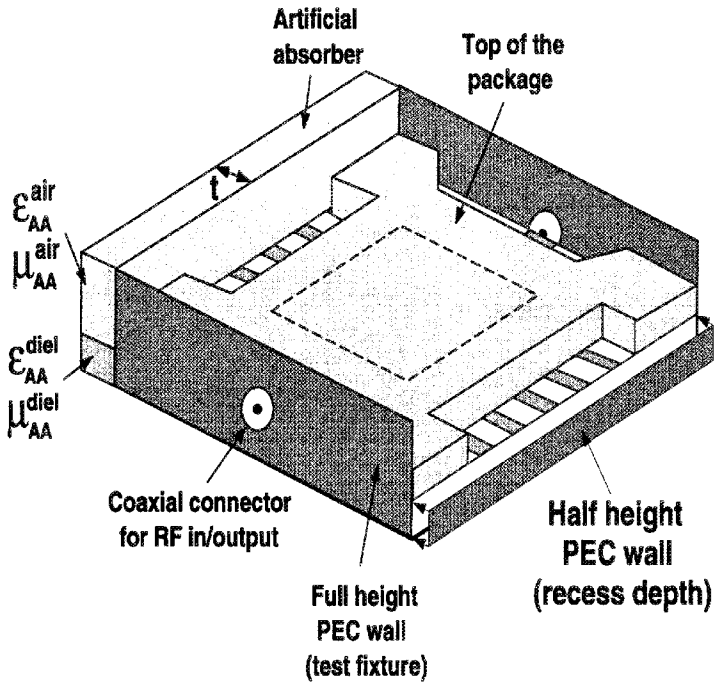


Figure 6.3: Schematic showing the location and extent of PECs in addition to the artificial absorbers which simulate the test fixture and open environment. Two different types of absorbers ($\epsilon_{AA}^{air} = \mu_{AA}^{air} = 1.0 + j10.0$, $\epsilon_{AA}^{diel} = 9.5 + j15.0$, and $\mu_{AA}^{diel} = 1.0 + j1.5789$) are designed and placed in either side of the package facing the DC bias lines (not fully shown in the figure for simplicity).

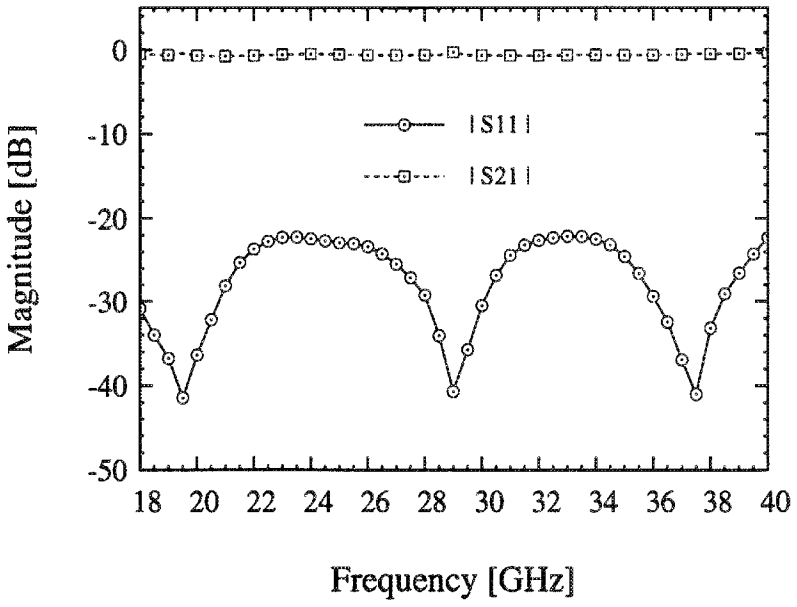


Figure 6.4: Computed S-parameters for the isolated symmetric package.

loss remains within -1.0 dB. As will be shown in the later sections, the symmetric arrangement of the package impacts on the performance of the package greatly.

6.3.2 Modeling of Isolated Asymmetric Package

In this section, the performance of the isolated asymmetric package is modeled and the computed S-parameters are presented in Fig. 6.5. As can be observed in the figure, the package reveals relatively good performance with better than -10.0 dB return loss over the entire frequency range. It is also noted that no cavity or spurious resonances are observed, even though the size of the overall package becomes larger than half guided wavelength at frequencies above 15 GHz. The absence of any resonance is also evident from Fig. 6.6, which shows the computed vertical electric field distribution in the package, and is attributed to the imperfect EM shielding. Even though the package provides excellent mechanical/environmental protection and hermeticity, the virtual side walls formed by the 12 vertical metal filled vias

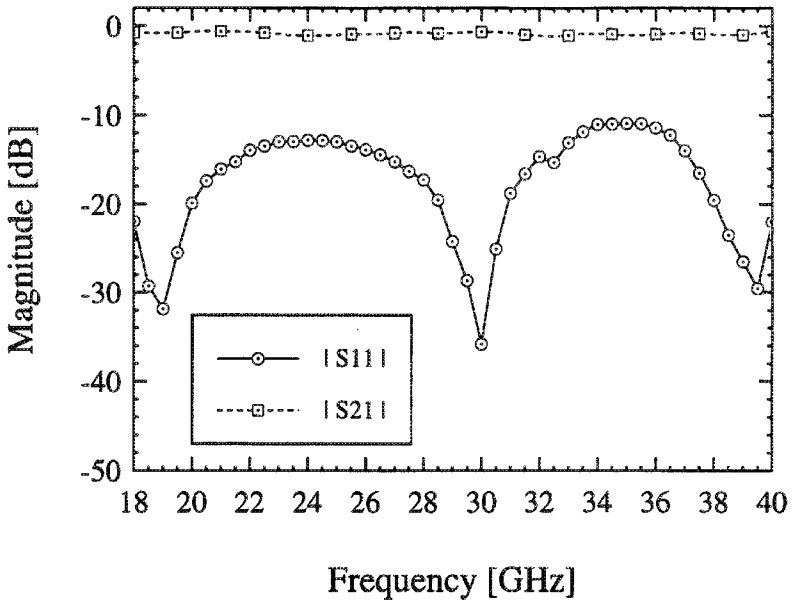
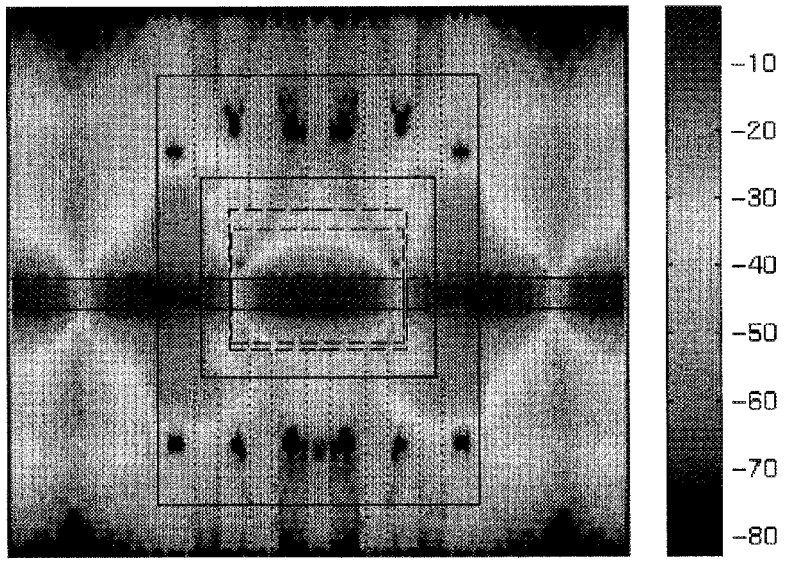


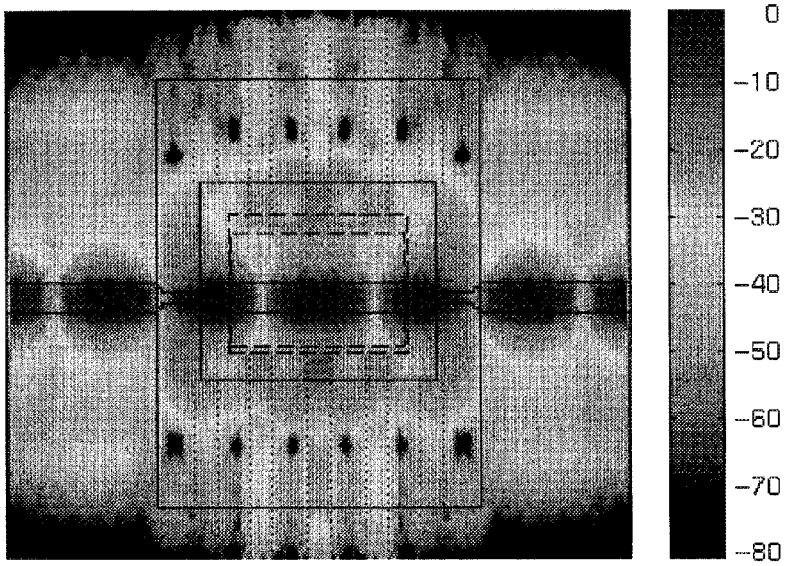
Figure 6.5: Computed S-parameters for the isolated asymmetric package.

between the DC bias lines do not provide a solid EM shield. Leakage from the cavity semi-open walls drains the energy from the cavity and in turn contributes for the suppression of the occurrence of cavity resonances.

The effects of the bond wires and DC bias lines on the characteristics of the package are also studied. This is accomplished by computing the scattering parameters of the modified package: the four bond wires are eliminated between input/output RF microstrip lines and the 50 Ω through line remaining 40 μm gap between them, and 5 DC bias lines are also removed from both sides of the package. The computed scattering parameters for the simplified structure shown in Fig. 6.7 reveal no discernible differences from the original package. This result implies that the presence of the bond wires and the DC bias lines is not critical to the performance of the package. Furthermore, it can be argued that the shape of those structures, namely bonding wires and DC bias lines, should not disturb the overall characteristics of the



(a)



(b)

Figure 6.6: Computed vertical electric field distribution (dB scale) at (a) f = 20.5 GHz and (b) f = 29.5 GHz in the isolated asymmetric hermetic package.

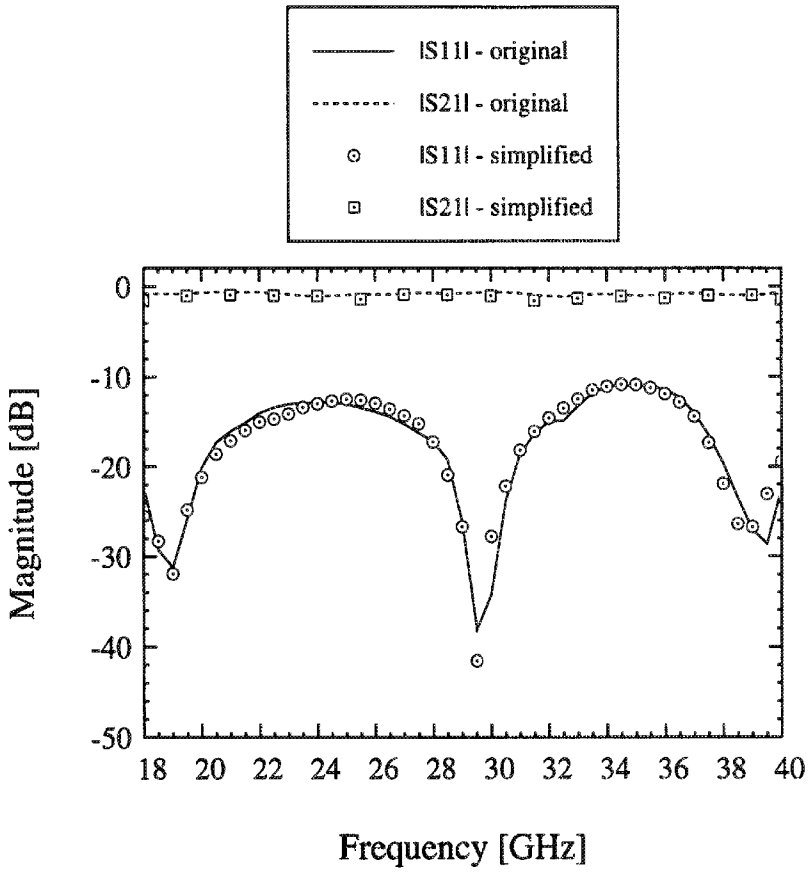


Figure 6.7: Comparison between the computed S-parameters for the isolated asymmetric package with (original) and without (simplified) DC bias lines and bond wires.

package. Compared to the performance of the symmetric package shown in Fig. 6.4, the return loss of the asymmetric package surprisingly increases about 10 dB.

6.3.3 Modeling of Asymmetric Package Placed in a Test Fixture

The asymmetric package is now placed inside of a test fixture and the whole structure is modeled to quantify the susceptivity of the package to the environment and to identify the electromagnetic field leakages and spurious resonances. The test fixture is modeled by using PEC walls along the ends of the package with an opening at the center for the input/output coaxial connectors as illustrated in Fig. 6.3. The

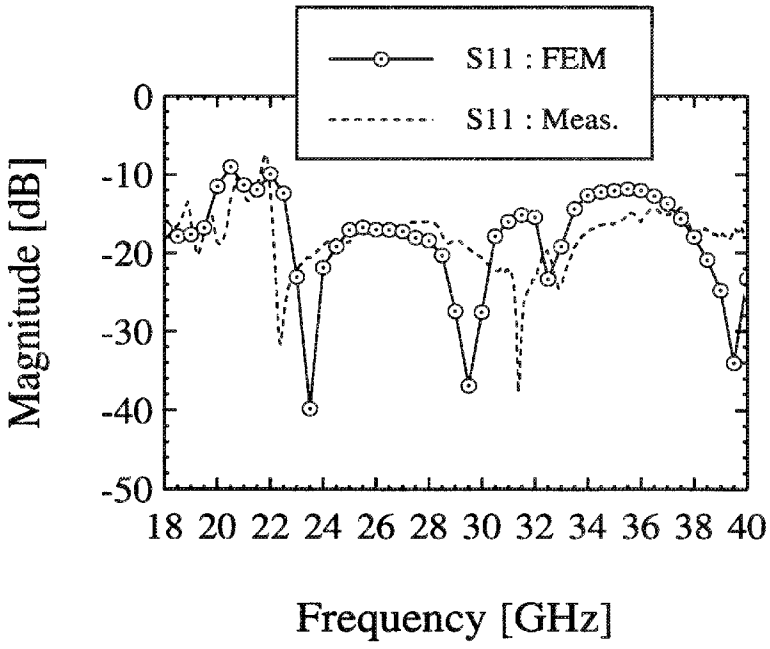
half height PEC walls are designed for the simulation of the recess depth of the test fixture, and the absorbers are placed around the package on top of the half PEC walls. The measured and computed scattering parameters for the package placed in the test fixture are presented in Fig. 6.8 revealing very good agreement. As can be observed, the overall structure including the package and test fixture suffers from spurious resonances in the low frequency region (18 to 24 GHz), even though it exhibits very good performance in the rest of the frequency range.

The resonance phenomenon can be also understood by investigating the EM field distributions at various frequencies as shown in Fig. 6.9. For example, at f = 20.5 and 22.0 GHz, $|S_{11}|$ has peaks (high insertion loss) indicating strong mismatch and energy leakages through the input/output RF microstrip lines as well as between the metal filled vias as clearly shown in Fig. 6.9 (a). It is also observed that at these frequencies the excited EM fields are strongly concentrated in the package frame, having the shape of a dielectric ring, placed on top of the input/output microstrip lines and the DC bias lines. Even though the strong resonances in the package should be suppressed by allowing energy leakage, it should be noted , however, that the poor EM hermeticity could cause a serious EM compatibility (EMC) problem. Fig. 6.9 (b) shows the field distribution at 29.5 GHz, where $|S_{11}|$ has a dip indicating small insertion loss. The calculated results also show the voltage standing wave pattern of the EM field on the microstrip line.

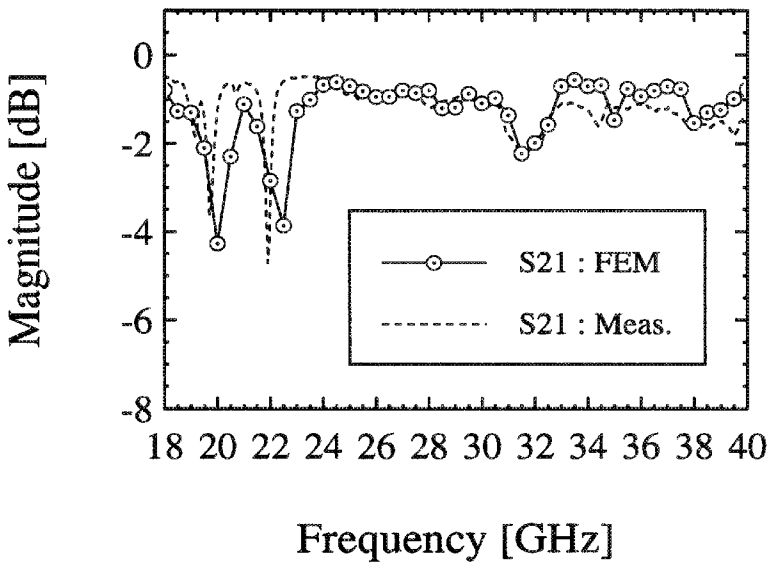
6.4 Features Which Can Enhance Package Performance

6.4.1 Asymmetric Package with Additional Metal Filled Vias

To investigate the role of the vertical metal filled vias on the EM hermeticity of the package, and to study the energy leakage from the input/output ends of the

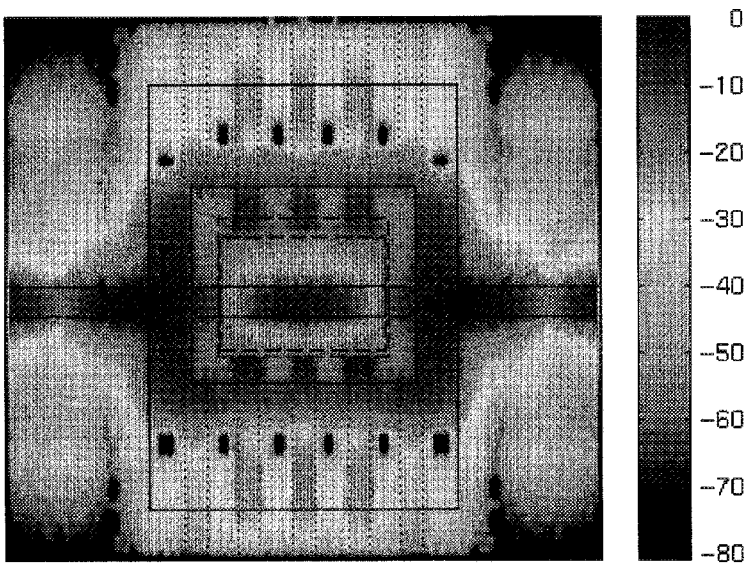


(a)

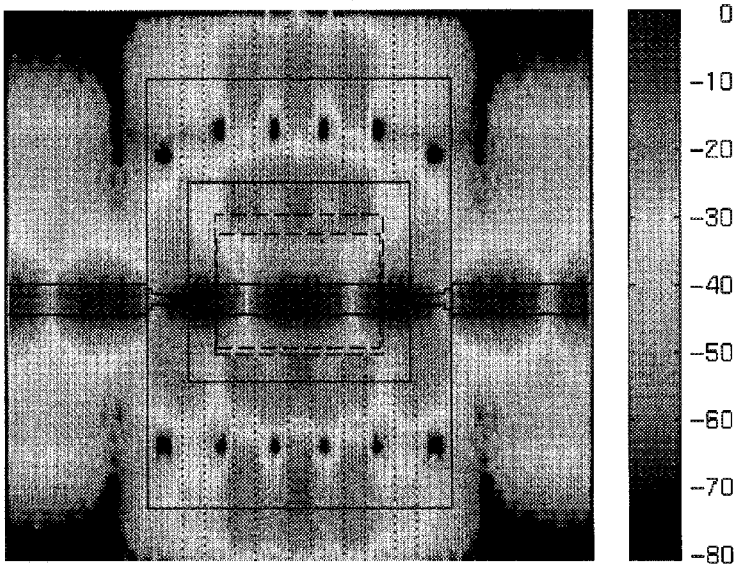


(b)

Figure 6.8: Measured and computed S-parameters ((a) $|S_{11}|$ and (b) $|S_{21}|$) for the asymmetric package residing in the test fixture.



(a)



(b)

Figure 6.9: Computed vertical electric field distribution (dB scale) in the asymmetric hermetic package placed in the test fixture at (a) f = 20.5 GHz and (b) f = 29.5 GHz in the isolated asymmetric hermetic package.

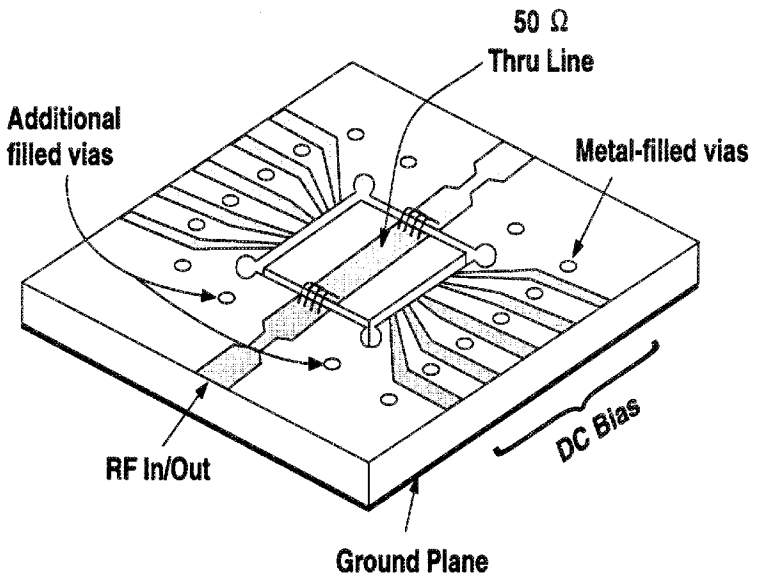


Figure 6.10: Schematic diagram of the asymmetric hermetic package showing four additional vias at the input and output ends of the package.

package, four additional vias are placed as shown in Fig. 6.10. The dimensions of the additional vias are the same with those of the previous set of vias. As shown in Fig. 6.11, the frequency response of the package is quite degraded in the most of the frequency region, indicating the fact that providing additional vias could aggravate the package internal resonances by suppressing the leakage of the EM fields. Interestingly enough, the enforcement of strong EM hermeticity by placing additional vias causes strong unwanted internal resonances, while poor EM hermeticity makes the package more susceptible to the surrounding environment. To overcome the above contradictory difficulties, the effect of using lossy packaging materials are examined in the following sections for the suppression of the unwanted cavity resonances as well as energy leakages.

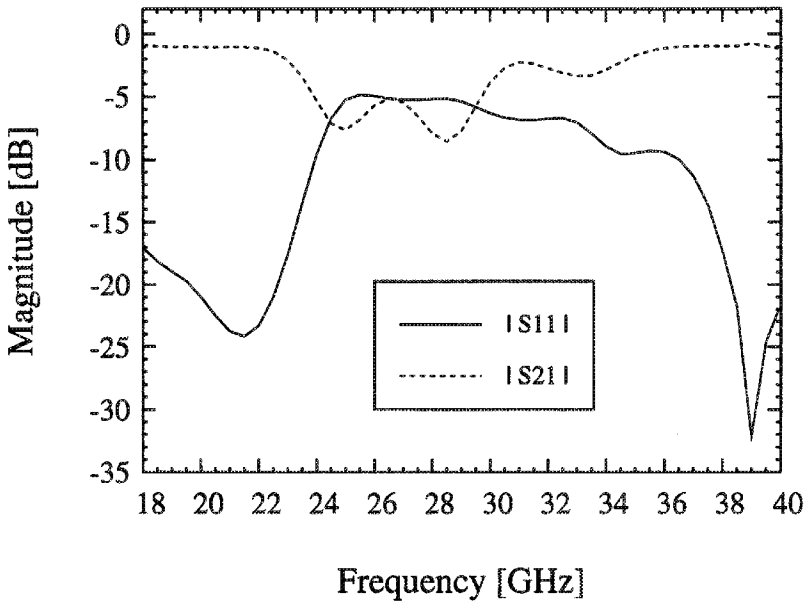


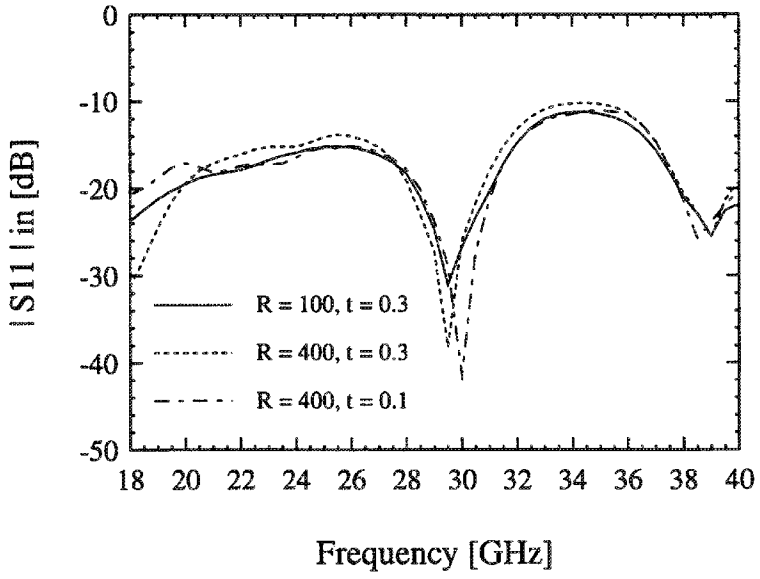
Figure 6.11: Computed S-parameters for the asymmetric package with four additional vias at the input and output ends of the package.

6.4.2 Asymmetric Package with Resistive Coated Lid

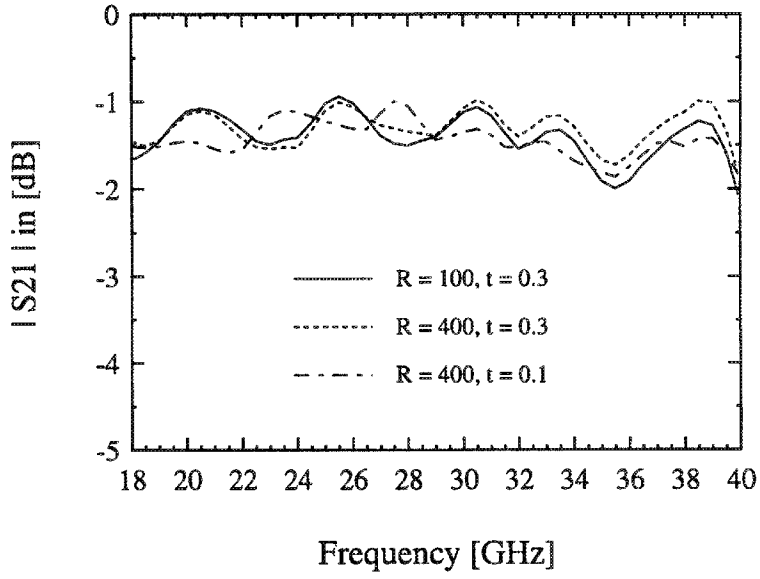
As an effort to suppress the unwanted cavity resonances in the 18 to 24 GHz region (refer to Fig. 6.8(b)), a resistive sheet backed by PEC plane is placed on top of the package. The value of the resistivity R of the sheet is chosen to be 100 $\Omega/\square$ and 400 $\Omega/\square$, and the thickness t to be 0.1 or 0.3 mm. As shown in Fig. 6.12, the spurious resonances in the low frequency region (18 to 24 GHz) are completely suppressed for all 3 cases, and there are no distinguishable differences between them. This observation indicates that placing resistive material on the inside surface of the package lid can suppress the unwanted resonances by imposing lossy boundary condition on the fields resonating inside the package.

6.4.3 Asymmetric Package with Lossy Dielectric Frame

It is very important to take measures for the suppression of the internal resonances during the first design stage in order to avoid performance degradation. Suppression of the internal resonances may be accomplished through a variety of approaches. One approach may suggest the design of a leaky package so that strong resonances are not supported. This approach has been examined in the previous sections and reveals that the package interferes strongly with its surroundings. As an alternate approach, one can fabricate the package frame from a dielectric material having non-zero loss tangent. Fig. 6.13 shows S-parameters of the package with two different dielectric materials: case 1 : $\epsilon_r = 9.5(1.0 + j0.1)$, $\mu_r = 1.0 + j0.0$, and Case 2 : $\epsilon_r = 9.5(1.0 + j0.5)$, $\mu_r = 1.0 + j0.0$. As can be realized from the figure, the unwanted cavity resonances in the low frequency region are completely suppressed by the assigned small amount of loss in the packaging material. It is also important to notice that the insertion loss increases to -2 dB due to the loss in the packaging



(a)



(b)

Figure 6.12: Computed S-parameters ((a) $|S_{11}|$ and (b) $|S_{21}|$) for the asymmetric package residing in the test fixture with resistive coating on the inside surface of the lid. The resistivity and the thickness of the coating is indicated as R in [$\Omega/\square$] and t in [mm], respectively.

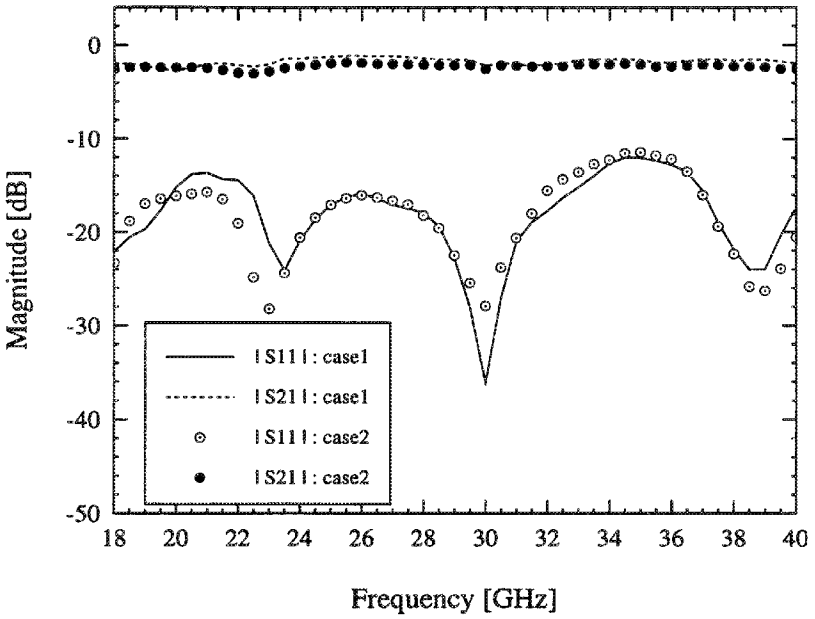


Figure 6.13: Computed S-parameters for the asymmetric package with frame constructed from dielectric material with high loss tangent. Case 1 : $\epsilon_r = 9.5(1.0 + j0.1)$ and $\mu_r = 1.0 + j0.0$. Case 2 : $\epsilon_r = 9.5(1.0 + j0.5)$ and $\mu_r = 1.0 + j0.0$.

material. The differences in the scattering parameters for two cases corresponding to different loss tangents remain negligible in the whole frequency spectrum.

6.5 Conclusions

In this study, a 18 to 40 GHz hermetic package is experimentally characterized and also modeled using the finite element method. The FEM accurately predicts the S-parameters, energy leakage and spurious resonances which degrade the package performance. To the best of author's knowledge this is the first comprehensive study of RF leakage and resonances in a millimeter-wave package. The modeled results show that the unwanted spurious resonances in the package can be suppressed by incorporating a resistive coating on the lid and by the use of dielectric materials with high loss tangent. The modeled S- parameters for a symmetric package predict low insertion loss on the order of -1.0 dB over the 18 to 40 GHz band. From this

study, it becomes clear that symmetry in the package construction is crucial for good performance.

CHAPTER VII

SYSTEM LEVEL EM MODELING OF DIGITAL ICs AND PACKAGES

In this chapter, as an application of the finite element method to system level electromagnetic modeling for digital ICs and packages, a new hybrid technique is developed combining a full-wave EM field analysis tool (FEM) and a circuit simulator (HSPICE). The three-dimensional FEM has been used as a tool to extract equivalent circuits from the detailed structures and the circuit simulator is the used for efficient time domain analysis of the lumped element network. This hybrid methodology provides accurate *noise maps*[1] at any place in the circuit topology and guides effective placement of decoupling capacitors.

7.1 Introduction

Inductively induced voltage fluctuations in the power and ground lines of digital systems are a source of performance degradation and may pose serious reliability problems. Variously termed simultaneous switching noise (SSN), inductive noise, delta-I noise, and ground bounce, this phenomenon is most severe when a large number of high frequency chip drivers switch simultaneously, and cause a large amount

[1]The noise maps are generated by measuring maximum, minimum, or peak-to-peak voltage fluctuations on any given plane, such as the power and ground planes. In other words, at each electrical node, the desired values are recorded in the whole simulation period. As a result, the values in the noise maps, in general, correspond to different time instants.

of current to be injected into the power distribution network. The adverse effects of SSN are manifested in a variety of transient and permanent system malfunctions, including the appearance of undesirable glitches on what should otherwise be quiet signal lines and the flipping of state bits in registers and memories. Because of their unpredictability, SSN-related bugs have been reported to be among the most difficult to track down and correct [214].

While the fundamental mechanism underlying SSN, namely current switching, has been widely recognized for many years [215]-[219], the computer-aided design tool kits available to a digital system designer today still lack adequate SSN modeling, analysis, and design capabilities. This lack of modeling tools can be partially attributed to the complexity of the EM modeling required to obtain accurate estimates of the inductive parasitics responsible for SSN, coupled with the need for system-wide global analysis of this effect. Current approaches for dealing with SSN are largely ad hoc, relying primarily on the ability of expert designers to postulate worst-case scenarios for the occurrence of SSN-related errors and to analyze these scenarios using pessimistic estimates of packaging parasitics.

The goal of this study is to take a first step towards evolving a systematic methodology for modeling and analysis of SSN in printed circuit boards (PCBs). In this methodology, the seemingly contradictory goals of modeling accuracy and global analysis efficiency are reconciled through a divide-and-conquer process, namely micro- and macro-modeling. Accuracy is insured by performing detailed EM field analysis on appropriately chosen small sections of the PCB, referred to as "tiles", to create lumped electrical equivalent circuit models. PCB tile models are subsequently combined with models for chip current drivers and package leads to produce an electrical simulation model for the PCB power distribution subsystem. A circuit

simulator such as SPICE [220] is then used to exercise this model under a variety of current excitation conditions to yield noise maps that indicate the variation in power and ground potential as a function of location on the PCB.

It is instructive to note that this approach is similar, at least in spirit, to the approach routinely employed in modeling and simulation of very large scale integrated (VLSI) chips. Accurate circuit simulation of VLSI chips containing tens of thousands of transistors is made possible by separating the detailed physical models of 3-D transistor structures from the global chip-wide electrical analysis. Device modeling involves creating lumped electrical equivalent circuits that are obtained by solving the partial differential semiconductor equations governing the movement of charge carriers within the semiconducting material. These equivalent circuits, appropriately parameterized by material, geometrical and environmental factors, are then combined to produce a complete electrical model for a chip that is amenable to analysis by fast circuit simulators.

The rest of this chapter is organized in four sections. Section 7.2 reviews current approaches to the modeling and analysis of SSN and motivates our approach to the problem. The tiling procedure central to our method is described in Section 7.3 along with the equivalent circuits for three different tile types. In Section 7.4, several simulation results are presented for a number of different PCB configurations that are aimed at enhancing the understanding of the SSN phenomena. In particular, the hybrid approach developed in this study is validated by comparing the measurement data provided by Intel for their P6 "gadget". The contributions of this work and directions for future work are summarized in Section 7.5.

7.2 Problem Statement and Previous Work

A simplified model of the current path through a PCB-mounted IC chip is shown in Fig. 7.1 [215]-[217],[221]. Current enters the PCB through a metal connector from an external power supply (denoted as V_{DD}) and flows through the conducting material of the board's power plane, the chip's package leads, and bonding wires to a V_{DD} pad (point A) connected to the chip's internal power distribution network. Current then flows through one or more output pad drivers C and returns through a V_{SS} pad (point B), bonding wires and package leads, to the board's ground plane and ground connector to the external power supply. In this simplified model, lumped inductances are used to represente the PCB power and ground planes (labeled L_{PCB}) and the package leads (L_{PIN}). It is also assumed that the internal chip power distribution network is mostly resistive and does not significantly contribute to the overall inductance responsible for SSN. Techniques for efficient design of chip power distribution are discussed in [222].

When a pad driver C changes state to charge or discharge its load capacitance, the resulting current surge through the power distribution network produces inductive voltage drops and in turn lowers the potential at point A below V_{DD} and raises the potential at point B above V_{SS}. Such glitching, or noise, in what should otherwise be quiescent power and ground rails leads to harmful effects on the chip circuitry, such as increased driver delay and loss of signal integrity [215, 216]. The increase in driver delay is directly attributable to the temporary lowering (raising) of potential at point A (point B) causing a reduction in the current drive available for charging (discharging) the load capacitance to V_{DD} (V_{SS}). The second effect is more insidious, as it may lead to logic errors. Since the power and ground lines establish the reference

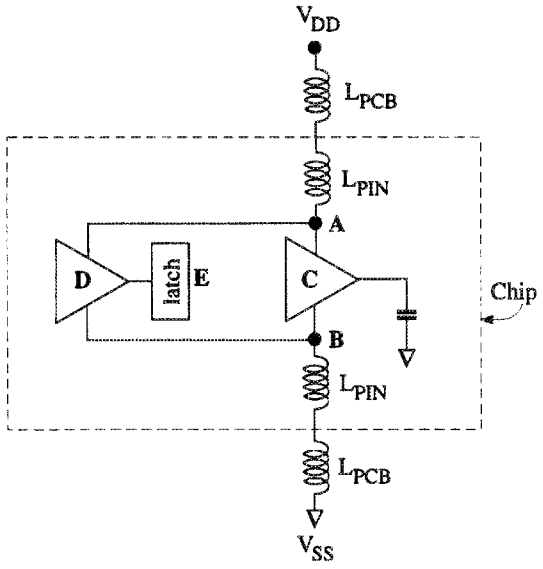


Figure 7.1: Traditional way of modeling the inductances of the PCBs and package bonding wires.

levels for all other signals, fluctuations in these levels may be misinterpreted as logic transitions in data and clock lines. If these transitions are inadvertently latched, the circuit may end up in an incorrect logic state. For example, a dip in potential at point A may be seen as a spurious glitch at the output of the quiet driver D that flips the state of latch E. These problems are compounded when a large number of output drivers switch simultaneously on a PCB with many chips.

Much of the previous work on SSN can be characterized as seeking (1) the determination of an aggregate effective inductance L_{eff} that accounts for the power and ground leads, the board itself, and the mutual inductances between the chip packaging and the PCB, and (2) the development of design guidelines to reduce SSN effects. Some of the early work in this area was done in [216], where a detailed electrical model of the package is simulated using ASTAP [223] and a gross value of

L_{eff} is determined using:

$$L_{eff} = V_n/(N\frac{di}{dt}) \tag{7.1}$$

where V_n is the noise magnitude, N is the number of simultaneously switching drivers and $\frac{di}{dt}$ is the rate of change of driver current. In this approach, only a single chip is considered and the computed L_{eff} is used to represent the noise effects. In a similar manner, Rainal [218] gives detailed formulas for calculating the self and mutual inductances, assuming that the pin inductances are the principal sources of switching noise on a chip. Using detailed electrical models of the package and the noise tolerance level of a logic family, Katopis [217] applies statistical design rules to determine the maximum number of drivers that may switch simultaneously. Furthermore, EDN's Advanced CMOS Logic ground bounce tests [224] conclude that centrally placed ground pins or surface mounted packages reduce the ground bounce effects. In all these treatments, the parasitic inductance of the PCB is ignored and the lead inductances of the package pins are considered to be the primary contributors to SSN.

Recently, however, several attempts have been made to account for the effect of the PCB power and ground plane inductances. Specifically, the current distribution on the power and ground planes is computed by solving the field equations using source and sink points. In [225], the switching noise due to inductances in the board as well as the vias is computed using an appropriate SPICE model. The board is assumed to have four layers: signal, power, ground, and reference layer for the measurements. The model is created by appropriately discretizing the power and ground planes and finding the equivalent circuit for each mesh.

More recent work [219] has shown that the induced noise voltage is, in fact, sub-linear in the number of switching drivers. This phenomenon is due to the fact

that the ground bounce acts as a form of negative feedback, reducing the drive of the CMOS transistors. In this work L_{eff} is calculated by placing centralized point sources and distributed sinks on the power planes. The static field equations are then solved for the power planes, and the L_{eff} is computed in a modified form of Eq. (7.1) to take into account the negative feedback effect. The level 1 SPICE model of the CMOS transistors used in deriving the noise equations limits the accuracy of the model when it is applied to sub-micron technologies. Moreover, the computed value of L_{eff} varies with location when many chips are placed on a PCB. A detailed EM analysis of the interconnect structure in a computer package is performed in [170, 226] using the FDTD and transmission line matrix (TLM) methods. While accurate, these approaches become computationally infeasible for realistic systems where a PCB may contain several hundred ICs with multiple layers of power, signal, and ground planes.

An accurate SSN simulator must consider the inductances due to both the PCB and the pins themselves. The technique developed during the study presented in this chapter uses a combination of both macroscopic and microscopic modeling approaches, as illustrated in Fig. 7.2. The micromodeling provides an accurate electrical representation of the board as an interconnection of N-port networks. These networks are three-dimensional ladders of RLC elements and represent the electrical equivalents of subsections of the board, referred to as tiles. The tile equivalent circuits are defined according to the expected electric field signatures inside the board, and high accuracy is achieved by taking into account the dynamic nature of the electromagnetic fields. Depending on the substructure, these models may be based on quasi-static or full-wave solutions. The resulting board equivalent circuit is augmented with models for chip current drivers and simulated using HSPICE [227] .

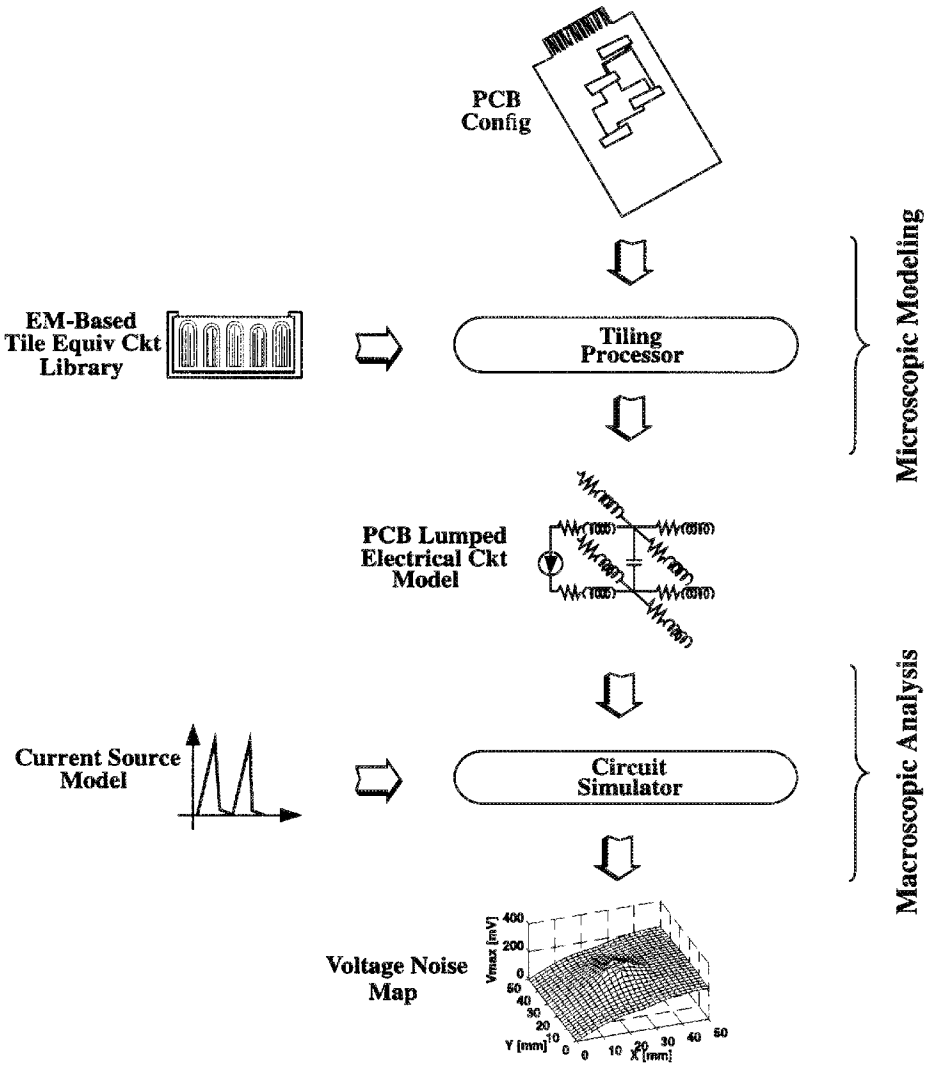


Figure 7.2: Modeling of simultaneous switching noise (SSN) and simulation methodology.

The macroscopic model considers the SSN at the system level and accounts for its variations across the PCB due to the flow of current along the conducting paths on all planes. A noise map of the power and ground planes is obtained as a result of the macromodeling and the regions where the effect of noise is maximum are identified for the possible insertion of bypass capacitors.

While the hybrid approach developed in this study is similar to [225], it has the advantage of combining the accuracy of a full-wave field simulator with the large-scale capacity of SPICE electrical simulation, and can be easily generalized to handle any number of power, ground and signal layers. Moreover, since the equivalent circuits resulting from the full-wave analysis consist of lumped R, L and C elements, we can potentially use the AWE-based simulators, which are 3 to 4 times faster than SPICE [228], provided that the drivers are linearized appropriately.

In the following sections, detailed descriptions of the micromodeling approach will be presented, while relatively short discussion is devoted to the macromodeling in view of its well-founded feature.

7.3 PCB Tiles and their Lumped Equivalent Circuits

In this section, the hybrid modeling methodology is presented starting with the tiling procedure and concluding with a summary of the primitive equivalent circuits structures which are the main building blocks of the printed circuit board geometry.

7.3.1 Tiling Procedure

The board is partitioned into a set of tiles, primitive structures, using a systematic discretization, or so-called *tiling*, procedure. In this procedure, grid points (nodes) are introduced for all the physical details of the structure. These physical nodes correspond to crossings and bends of traces, via connections to planes, corners of

the printed circuit boards, connections to connectors and drivers, apertures on the planes, connections to loads, decoupling capacitors, etc. These nodes exist on all planes of the PCB and may vary in number from plane to plane. The intent of the tiling approach is to construct a three-dimensional grid that preserves all the geometrical details of the printed circuit board. The resulting tiles are rectangular and non-uniform, and their grid points provide the electrical nodes for the three-dimensional SPICE model which is generated at the end of the tiling process.

It is important to notice that the interactions between the neighboring tiles are fully accounted for by electrically connecting them together. Any spurious coupling between them, which is a second order effect, however, is not considered here, unless the tile equivalent circuit reflects it. As a result, to minimize the error due to the tiling approach, all the closely coupled geometries have to be modeled together to yield an appropriate tile and this can be accomplished by applying the finite element method whenever necessary.

A simple example of the tiling procedure is shown in Fig. 7.3. During the tiling procedure three different types of tiles can be defined according to their shape: interior, edge, and corner tiles. The interior tile has a cross-shaped lumped equivalent circuit having four branches (or ports), and this tile can be also used to represent the edge and corner tiles by appropriately terminating one or two branches. On the other hand, tiles can be classified into three different primitive structures according to their functionality, as illustrated in Fig. 7.3: power/ground plane tiles, power/signal/ground tiles and power/ground pin tiles. The equivalent circuits for these primitives are derived by using appropriate electromagnetic simulation tools, as will be discussed below. In addition, the equivalent circuit representations for the input current and voltage sources as well as connectors are considered. Throughout

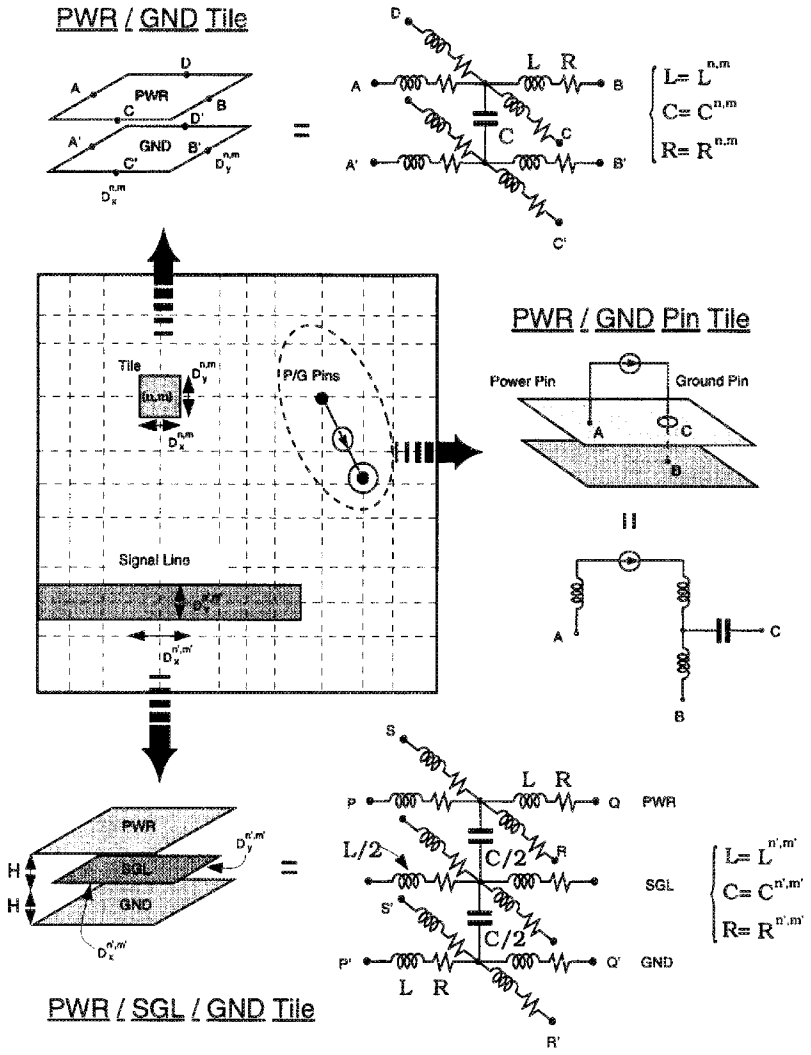


Figure 7.3: Equivalent circuits for three different tiles, such as power/ground tile, power/ground pin tile, and power/signal/ground tile.

the present study it has been assumed that the connectors are attached to one side of the PCB to maintain constant potentials on power and ground planes.

For PCBs having multiple power/ground planes, as commonly encounted in high-speed digital circuits, the equivalent circuits for each tile can also be stacked vertically to model the three-dimensional nature of the geometry. As a result, the tiling approach has no inherent limitations in terms of number of layers, except an increased computational burden.

The information from all of these equivalent circuits are recorded in an HSPICE input file, and then circuit simulation is performed in time or frequency domain. From the time domain circuit simulation, the potential distributions on the power and ground planes are obtained, and from these potential distributions the switching noises can be estimated. The input impedance at the driving port can be also easily computed from the voltage and current information at a given electrical node.

7.3.2 Equivalent Circuits

As mentioned above, a variety of modeling approaches are followed in order to identify the equivalent circuits for the primitives defined during the tiling procedure. Descriptions of these approaches are given below.

(a) Power/Ground Plane Tiles

A power/ground plane primitive is considered as a section of a parallel plate waveguide. From microwave circuit theory, the equivalent circuit for such a structure can be represented as a 4-port network, as shown in Fig. 7.3. Under the assumption that the parallel plate waveguide supports only a TEM wave, while evanescent higher order modes are weakly excited and can be practically considered non-existent, the equivalent circuits can be easily computed using the ideal transmission line theory.

The above underlying assumptions are, in general, valid for clock frequencies up to the GHz range. Furthermore, to take into account the floating potentials on the power and ground planes, a special form of an equivalent circuit is devised, as shown in Fig. 7.3. Since an arbitrary surface current can be decomposed into two orthogonal components, the parallel plate waveguide is decomposed into two orthogonal 2-port transmission lines corresponding to each direction of the current, and as a result a 4-port cross shaped equivalent network is obtained.

For the 4-port network, the appropriate equivalent inductances $L_x^{n,m}$ and $L_y^{n,m}$ for two orthogonal directions and the capacitances $C^{n,m}$ are derived from the 2-port ideal transmission line as:

$$\omega L_x^{n,m} = \frac{30\pi h}{D_y^{n,m}\sqrt{\epsilon_r}} \sin(\beta_g D_x^{n,m}) \tag{7.2}$$

$$\omega L_y^{n,m} = \frac{30\pi h}{D_x^{n,m}\sqrt{\epsilon_r}} \sin(\beta_g D_y^{n,m}) \tag{7.3}$$

$$\omega C^{n,m} = \frac{\sqrt{\epsilon_r}}{120\pi h}[D_y^{n,m} \tan(\frac{\beta_g}{2} D_x^{n,m}) + D_x^{n,m} \tan(\frac{\beta_g}{2} D_y^{n,m})] \tag{7.4}$$

where $D_x^{i,j}$ and $D_y^{i,j}$, $1 \leq i \leq N$ and $1 \leq j \leq M$ are the x and y dimensions of the $(i,j)^{th}$ tile as shown in Fig. 7.3. N and M are the number of tiles in x and y direction, respectively. Furthermore, h and ϵ_r are the thickness and relative dielectric constant of the dielectric material separating the conducting layers of the printed circuit board and β_g is the propagating constant at the frequency of equivalent circuit extraction. In addition to the inductive and capacitive elements, resistive elements are also added to take into account the effect of the ohmic losses and to prevent pure inductive loops in the equivalent circuits. The value of the resistive element can be calculated as:

$$R = \sqrt{\frac{\omega\mu_0}{2\sigma}} \tag{7.5}$$

where σ is the conductivity of the material.

Under the assumption that the electrical dimensions of the tile are much smaller than the wavelength at the operating frequency, that is, $\beta_g D_x^{n,m}$ and $\beta_g D_y^{n,m} \ll 1$, the above equations can be reduced to a more compact form using the small argument approximation of the trigonometric functions:

$$L_x^{n,m} = \frac{30\pi h}{c}\left(\frac{D_x^{n,m}}{D_y^{n,m}}\right) \tag{7.6}$$

$$L_y^{n,m} = \frac{30\pi h}{c}\left(\frac{D_y^{n,m}}{D_x^{n,m}}\right) \tag{7.7}$$

$$C^{n,m} = \frac{\epsilon_r}{240\pi hc}\left(D_x^{n,m} \times D_y^{n,m}\right) \tag{7.8}$$

where c is the speed of light in free space.

As can be recognized from the above expressions, the inductance and the capacitance become frequency independent as both the size of each tile and the distance between the power and ground planes become relatively small compared to the smallest wavelength of interest in the propagation signals. As frequency increases, however, the inductance and capacitance values may vary accordingly, giving rise to high-frequency effects. For the examples presented in this study, we assume that the inductances and capacitances in all equivalent circuits are independent of frequency.

(b) Power/Signal/Ground Tiles

The signal line located between two conducting planes is modeled as a stripline (as illustrated in Fig. 7.3). Similar to the power/ground plane tile, the equivalent circuit for a signal line is developed to take into account the effect of the signal line on the potential fluctuations at the power and ground planes by using the series inductances and shunt capacitances as shown in the figure. Derivation of the equivalent circuit is completed in two steps. First, the characteristic impedance of the stripline is evaluated from the empirical formula [229] which includes the effect of the fringing fields. Second, an equivalent T-network is constructed for a stripline

of length $D_x^{n',m'}$ and width $D_y^{n',m'}$, as shown in the bottom of the figure, and the values of the capacitance and inductance in the equivalent circuit are determined after taking a procedure similar to that in the previous subsection. The values of the inductances and capacitances for this primitive can be calculated as follows:

$$\omega L^{n',m'} = Z_o^{n',m'} \tan(\frac{\beta_g D_x^{n',m'}}{2}) \tag{7.9}$$

$$\omega C^{n',m'} = \frac{\sin(\beta_g D_x^{n',m'})}{Z_o^{n',m'}} \tag{7.10}$$

where

$$Z_o^{n',m'} = \frac{30\pi}{\sqrt{\epsilon_r}} \cdot \frac{1}{(W_e/H) + 0.441} \tag{7.11}$$

$$\frac{W_e}{H} = \frac{D_y^{n',m'}}{H} - \begin{cases} 0 & \text{if } D_y^{n',m'}/H > 0.35 \\ (0.35 - \frac{D_y^{n',m'}}{H})^2 & \text{if } D_y^{n',m'}/H < 0.35 \end{cases} \tag{7.12}$$

After the equivalent circuit components are determined, those elements are augmented into the equivalent circuit network of the power/ground planes: that is, $P - P'$ is connected to $A - A'$ and $Q - Q'$ to $B - B'$. By doing this, the interaction between the signal line and the power/ground plane can be fully accommodated.

In general, the equivalent inductance $L^{n',m'}$ and capacitance $C^{n',m'}$ are functions of frequency. However, if the length of the transmission line tile is smaller than that of the wavelength corresponding to the clock frequency, then $\beta_g D_x^{n',m'} \ll 1$, thus leading into frequency independent circuit components. As a result, the above equations are simplified to the following:

$$L^{n',m'} = \frac{Z_o^{n',m'} D_x^{n',m'} \sqrt{\epsilon_r}}{2c} \tag{7.13}$$

$$C^{n',m'} = \frac{D_x^{n',m'} \sqrt{\epsilon_r}}{Z_o^{n',m'} c}. \tag{7.14}$$

where $Z_o^{n',m'}$ is the characteristic impedance of the signal line.

(c) Power/Ground Pin Tiles

To model the power and ground pins connected to a current source or driver, as shown in Fig. 7.3, a simple equivalent circuit is employed. The power pin, directly connected to the power plane, is modeled as a vertical inductance element, while the ground pin, which is connected to the ground plane through a via hole on the power plane, is replaced by two inductances, one for the line above the power plane and one for the line below. Furthermore, to increase the accuracy of the model, one capacitor is added between the ground pin and the power plane, as shown in Fig. 7.3. This capacitor represents the parasitic capacitive effect between the pin and the opening in the plane.

The appropriate inductance and capacitance values are computed for a given geometry from an electromagnetic simulator, the finite element method (FEM) [29, 30], developed in the previous chapters. The FEM is based on tetrahedral edge basis functions and provides a highly accurate model of the fields including their dynamic effects. The values of the inductance and capacitance in the equivalent circuit are extracted by matching the S-parameters derived from the FEM to the S-parameters of the equivalent circuit representing the power/ground pin tiles. A similar type of equivalent circuit could be derived from a simplified analytic expressions, as presented in [169]. It has been found in the previous chapter that the inductance of the pin is a function of the length and diameter of each pin, and in practice, the inductance can be considered frequency independent. The amount of the capacitive effect between the pin and the via hole in the power plane is mainly determined by the diameters of the pin and surrounding hole. Note that as the diameter of the vertical via or pin increases, the inductance of the structure decreases due to the increased width of the current path.

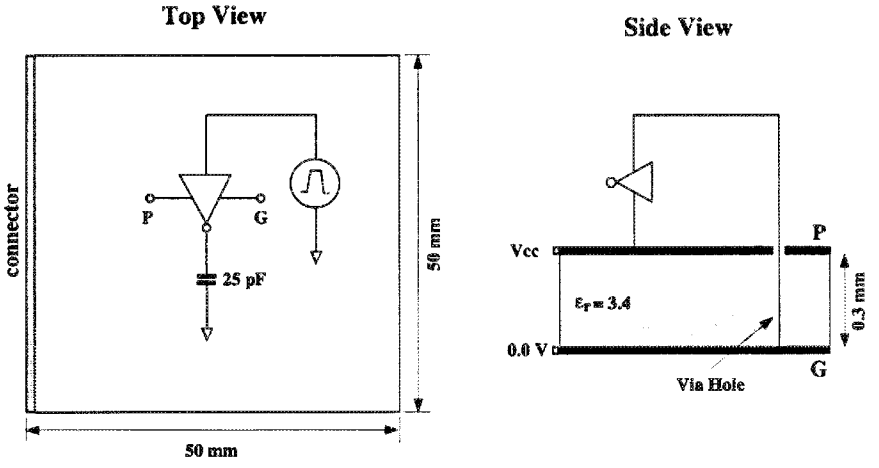


Figure 7.4: Example PCB used in the validation experiments.

7.4 Simulation Results

The modeling and simulation methodology described above was used to analyze SSN for a number of configurations of an example PCB whose physical characteristics are shown in Fig. 7.4. These configurations differed in the locations of the power/ground connectors, the number and placement of the current sources and sinks, the amount of current injected by each driver, and the size and location of decoupling capacitors. The effect of a signal trace has been also modeled as a stripline in one of the experiments.

Using the flow outlined in Fig. 7.2, a PCB configuration is tiled and simulated in the time domain using HSPICE. Transient simulation results, in the form of voltage waveforms at the power and ground grid points, have been subsequently converted to produce 3-D noise maps. In these maps, the maximum drop in voltage at each grid point on the power plane and the maximum increase in voltage at each grid point on the ground plane have been plotted, unless otherwise specified. In general, depending on physical importance, several different types of noise maps can be generated, such

as average, RMS, peak-to-peak, and maximum or minimum values on the power and ground planes.

7.4.1 Convergence Test: Tiling Optimization

The first task is to determine how changing the number of tiles used to model the power and ground planes affects the noise maps, and the experimental setup is shown in Fig. 7.5(a). The connector is placed on the left hand side and a current source is connected between the power and the ground planes as shown. The point "p" denotes the connection to the power plane and the point "g" denotes the connection to the ground plane through a via hole. The current waveform, shown in Fig.7.5(a), is a triangular pulse with rise (t_r) and fall time (t_f) of 500 ps and a peak value (I_{max}) of 10 mA. This wave shape is chosen to model the actual current flowing through the n and p-type transistors of a switching CMOS inverter. The noise maps for the various tiling cases are shown in Fig.7.5 (b) and (c) for the power and ground plane, respectively. These maps indicate a maximum voltage drop of 2.73 mV on the power plane (corresponding to point "p") and a maximum voltage increase of 3.69 mV on the ground plane (corresponding to "g") regardless of the number of tiles. As can be seen from the maps, the essential features of the noise maps remain the same, with maps corresponding to finer grids showing better resolution of the noise magnitude.

Fig. 7.6 illustrates the CPU and memory usage as a function of the number of tiles for this configuration. The CPU and memory requirement for the circuit simulation increases rapidly as the number of tiles increases. As a result, 625 tiles for the partitioning of the PCB is chosen as a reasonable compromise between the accuracy and simulation time for all other experiments described in this section, except for the Intel P6 board.

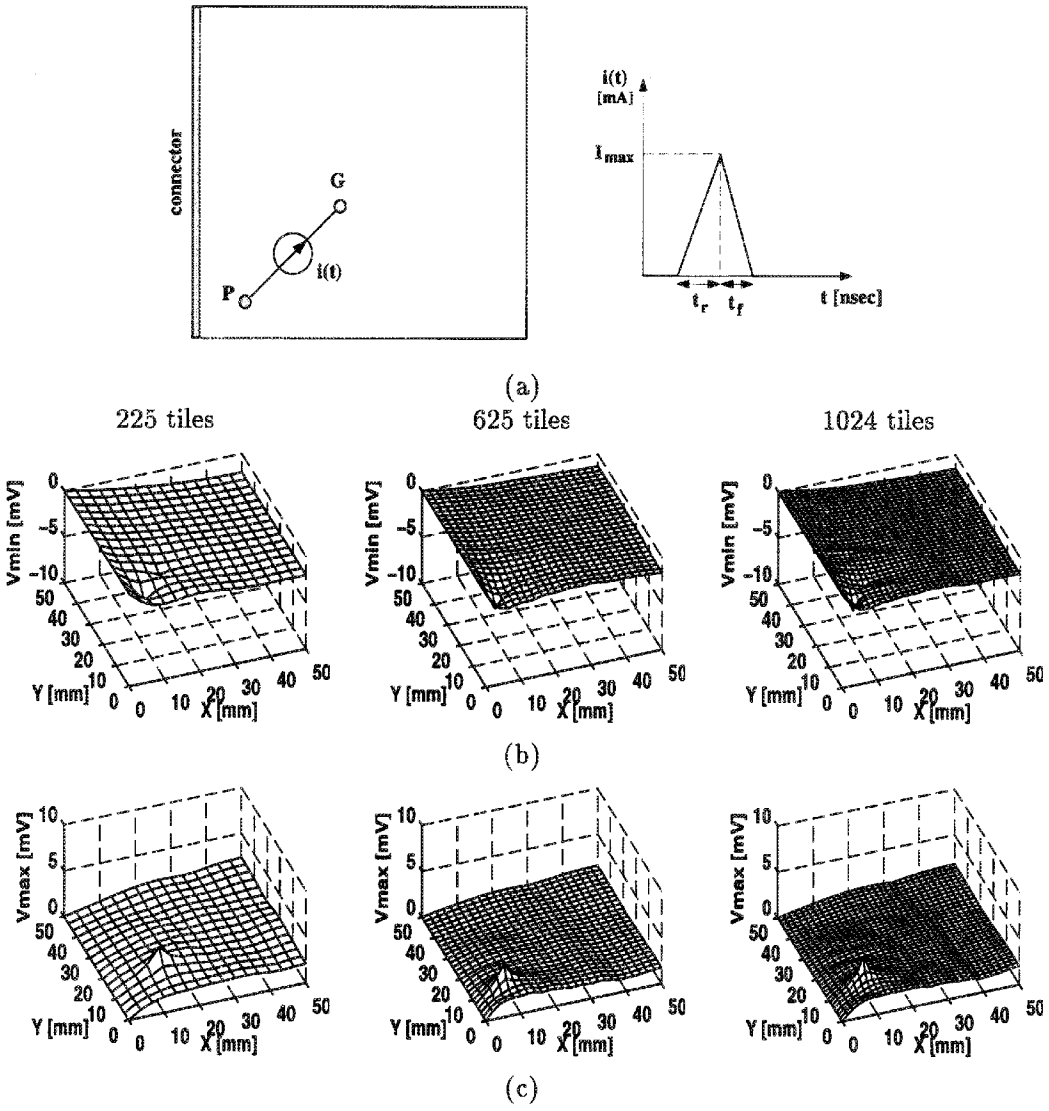


Figure 7.5: (a) Board layout and current waveform for validation experiments. Noise maps on the (b) power plane and (c) ground plane for three different number of tiles.

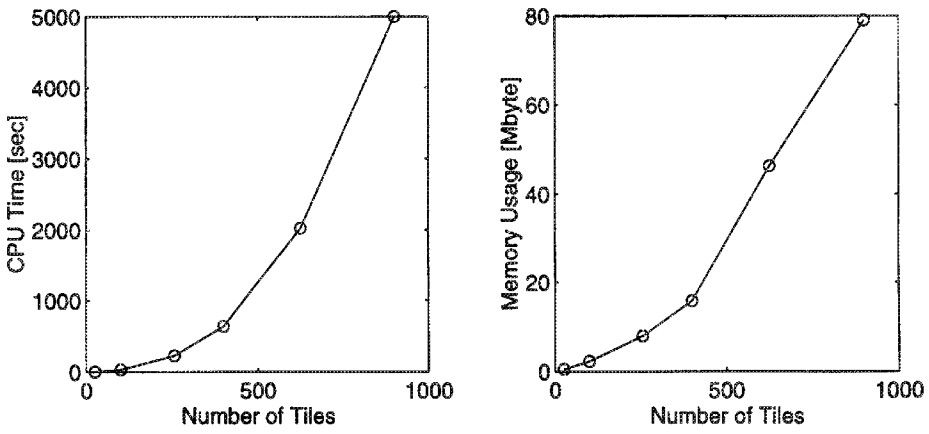


Figure 7.6: CPU and memory usage versus the number of tiles.

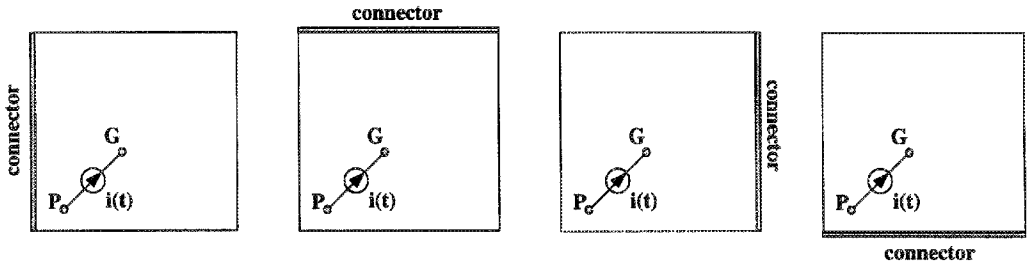


Figure 7.7: Variation in the position of the connector.

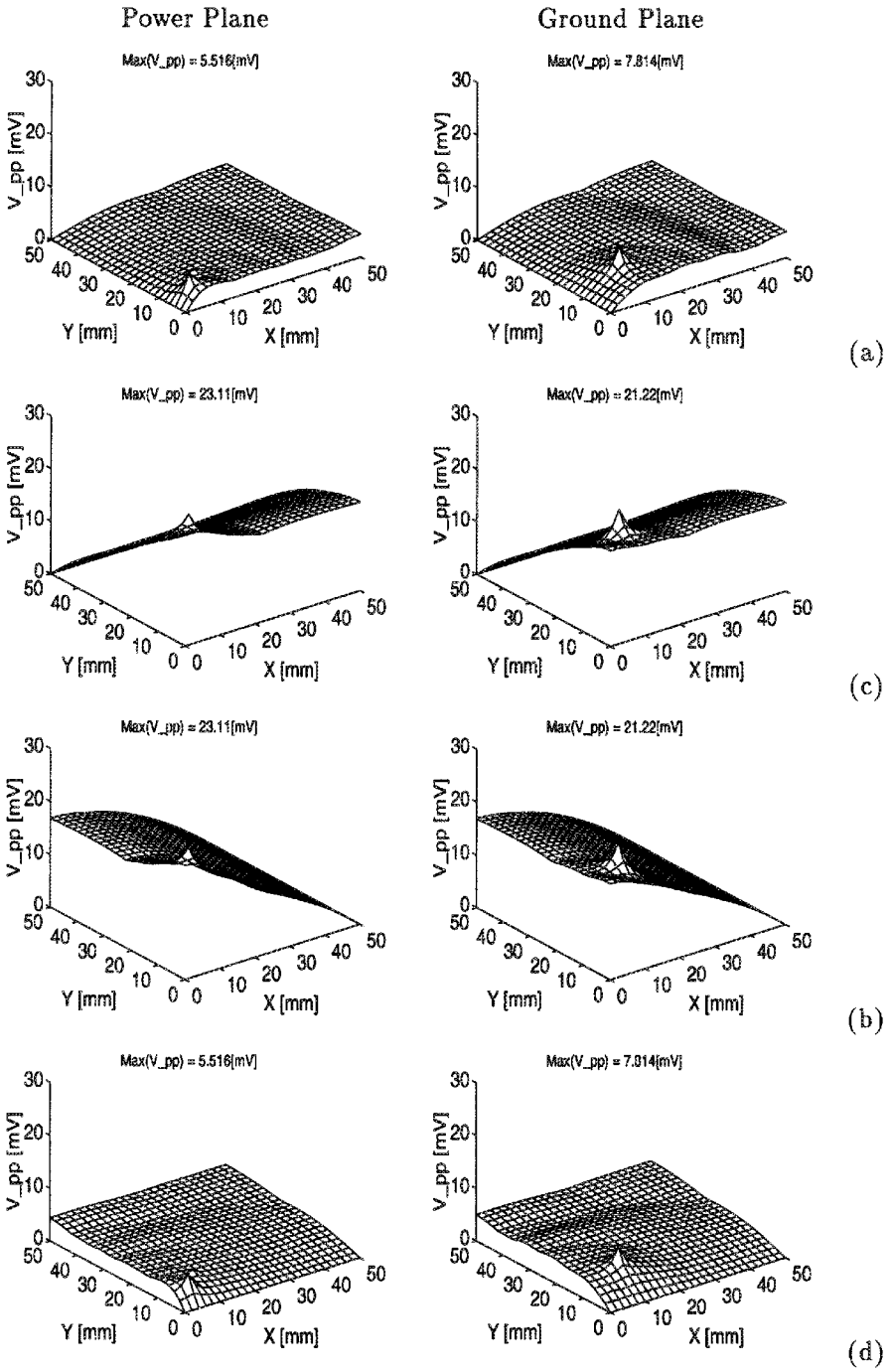


Figure 7.8: Noise map (peak-to-peak voltage variations) on the power and ground planes with connector in various places: (a) left, (b) top, (c) right, (d) bottom.

The position of the connectors is then varied keeping the coordinates of the current injection points on the PCB identical, as shown in Fig. 7.5. The connectors are alternately placed on the left, top, right and bottom edges of the PCB (see Fig. 7.7). As can be observed in Fig. 7.8, the potential fluctuations on the power and ground planes have their maximum values when the connectors are placed on the top and right edges. This is readily explained by noting that the current injection points for these two configurations are farther away from the DC power supply than in the other two configurations, making them more susceptible to noise.

7.4.2 Seven Drivers with Decoupling Capacitors

In order to obtain more realistic values of the noise voltages, the PCB with actual transistor drivers replacing the ideal piecewise linear current source has been simulated. Seven large CMOS inverters were connected to different points on the power and ground planes. Transistor sizes and capacitive loads have been chosen to represent realistic VLSI chip pad drivers: 1400 μm/1.2 μm for p-channel MOSFETs, 800 μm/1.2 μm for n-channel MOSFETs, and 25 pF load capacitance. Each driver is excited by a 1.7 ns wide voltage pulse with 0.8 ns rise/fall times. The resulting noise maps are shown in Fig. 7.9 (a) and indicate that the maximum noise levels on the power and ground planes are -439.26 mV and 560.93 mV, respectively.

In order to quantify the effect of the decoupling capacitors, 100 nF ideal capacitances (i.e. with no lead inductance) are connected across the power and ground leads of the seven drivers as illustrated in Fig. 7.10. The corresponding noise maps are shown in Fig. 7.9 (b) and indicate a reduction in the switching noise to -149.4 mV and 98.43 mV, respectively, on the power and ground planes. It is observed that the decoupling capacitance connected between the power and ground leads of the

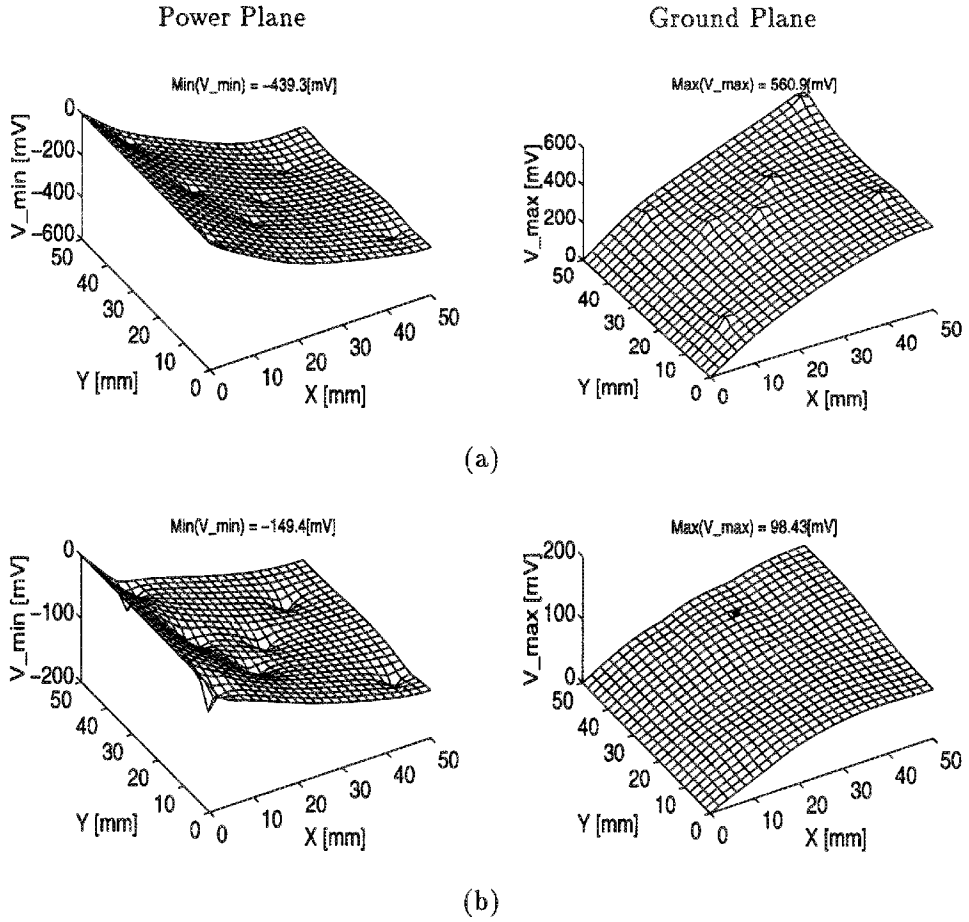


Figure 7.9: Noise maps (minimum on power and maximum on ground plane) (a) without and (b) with decoupling capacitors. Note that the scale of the vertical axis is not identical for both cases.

driver allows the most effective noise reductions on the power and ground planes.

Variation in noise levels as a function of the magnitude of decoupling capacitance is shown in Fig. 7.11. In general, larger values of decoupling capacitance contribute to reduce the noise level. However, switching noise cannot be reduced to zero regardless of the amount of decoupling capacitance used. Instead, the noise tends to saturate to a specific level beyond a certain critical value of the decoupling capacitance (the "knee" of the curves). While the critical value has been turned out roughly 1.0 nF with the given configuration, it is possible to have different values for different

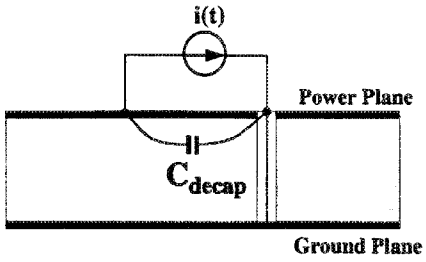


Figure 7.10: Configuration of the decoupling capacitance.

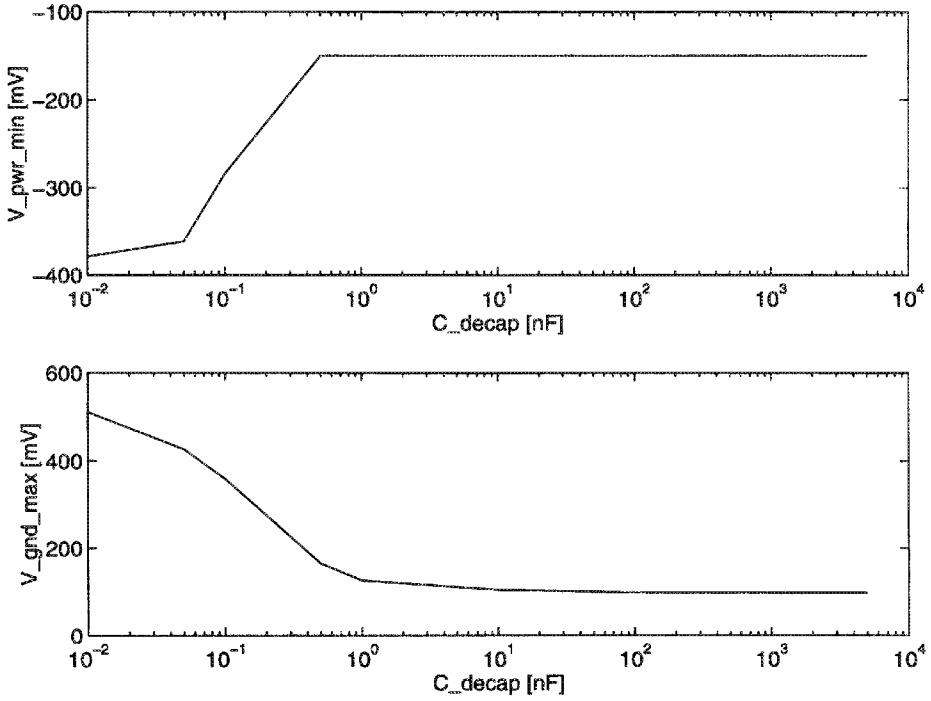


Figure 7.11: Noise variation on power and ground planes with various decoupling capacitances.

configurations.

7.4.3 Modeling of Signal Traces

In this section, the effect of a signal trace on the switching noise is studied. For the experiment, one signal line having width 0.5 mm and length 42 mm is placed in the middle of the dielectric substrate ($\epsilon_r = 3.4$) and a current source is connected at the center of the line. The current driver and its excitation pulse waveform are identical to those used in the previous experiment. In addition, one end of the signal line is terminated with 50 Ω lumped resistor, while the other end of the line is connected to a trapezoidal voltage source having 0.8 nsec rise/fall time and 1.7 nsec pulse width, and its peak value is 5 V. The PCB configuration used in this experiment and the equivalent circuit of the stripline with current source are shown in Fig. 7.12.

The resulting noise maps, minimum potential on the power and maximum on the ground planes, are shown in Fig. 7.13 for the both cases: with and without stripline. As can be observed in the figure, the presence of the stripline or signal trace causes a minor perturbations (i.e., reduced potential difference between the power and ground planes) to the potential distributions in the power and ground planes, especially in the ground plane. When the stripline is present, the maximum noise levels in the power and ground planes become -93.5 mV and 141.0 mV, respectively. However, when the stripline is removed, the noise levels in the power and ground planes are slightly changed to -87.0 mV and 168.6 mV, respectively, due to the reduced overall inductance and current injection into the planes. Note that those peaks on the power and ground planes correspond to the locations of the driver pins connected to each plane. When the width of the signal line becomes narrower, the interactions between the signal line and the power/ground planes are expected to be reduced due to the

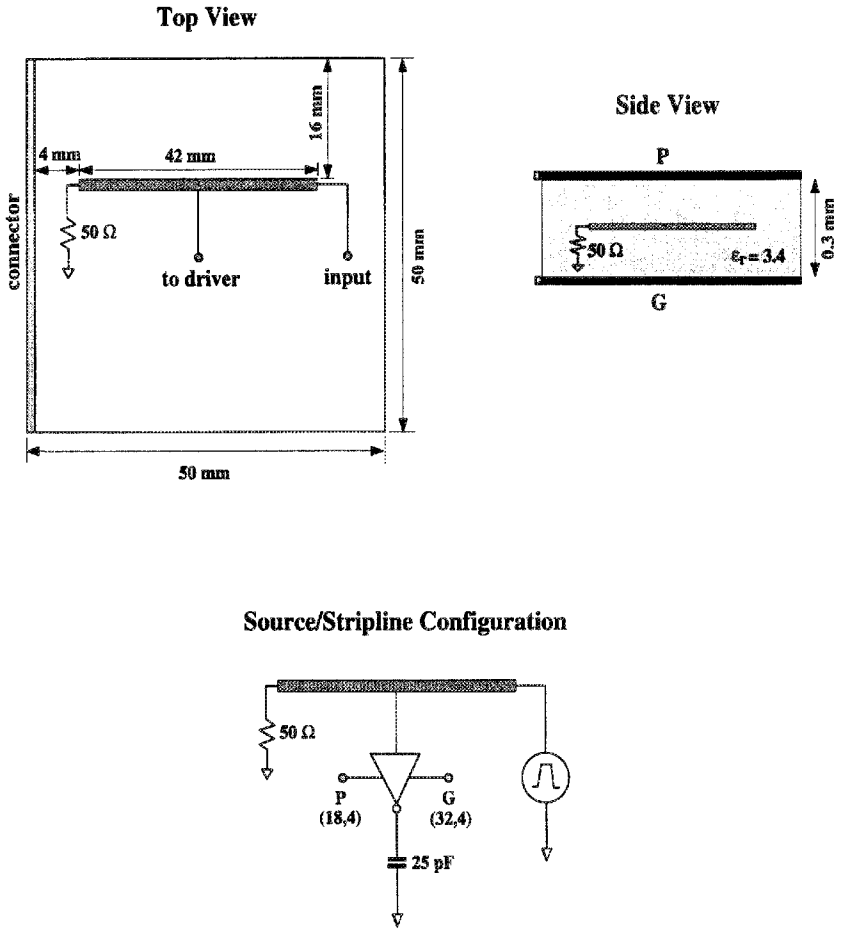


Figure 7.12: Top and cross sectional views (not to scale), and source/stripline configuration. The parenthesized numbers are coordinates in [mm] relative to lower left corner of the PCB. $\triangledown$ denotes connection to ideal ground, i.e., node 0 of HSPICE.

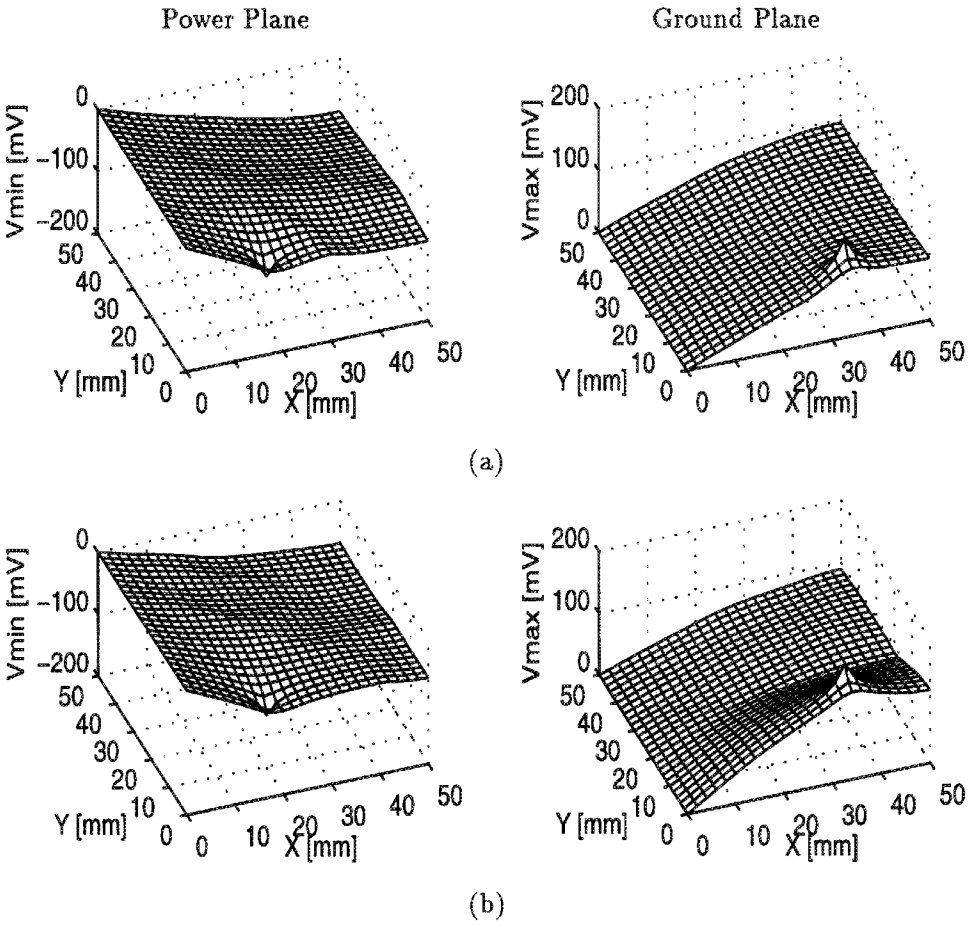


Figure 7.13: Noise maps on the power and ground planes (a) with signal trace and (b) without signal trace.

decreasing mutual capacitances. As a result, for very narrow signal traces, the effect of the traces can be considered as a secondary phenomenon.

7.4.4 Split PCBs

As shown in Fig. 7.14, a given PCB layer is split into two or more planes to provide better noise immunization and resulting reduced SSN. This type of structure can be modeled by introducing gap capacitances between two conducting planes in a close proximity, and the appropriate capacitance values, C_g and C_p, are extracted from the equivalent circuit of the microstrip gap geometry [230, 231] as illustrated in Fig. 7.15:

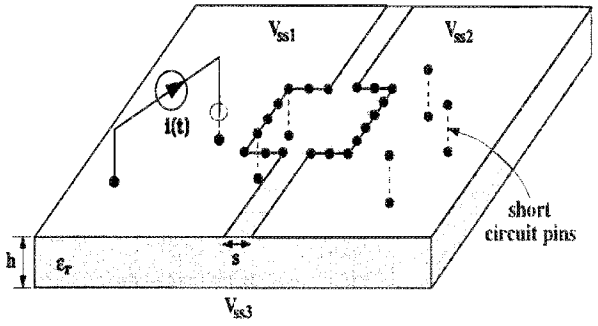


Figure 7.14: Split PCB and short circuit pins.

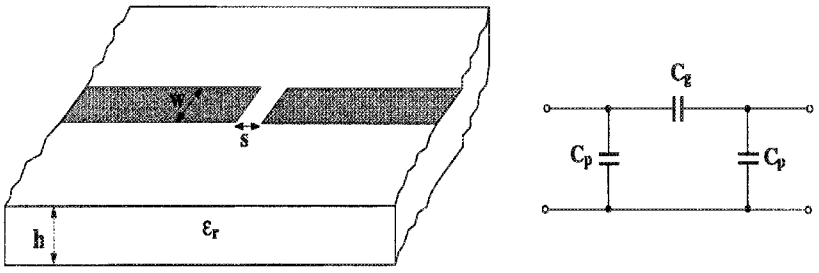


Figure 7.15: Gap in a microstrip line (a) and its lumped equivalent circuit (b).

for $\epsilon_r = 9.8$ and $0.5 \leq w/h \leq 2$,

$$C_p = C_{even} \tag{7.15}$$

$$C_g = (C_{odd} - C_{even})/2 \tag{7.16}$$

where

$$C_{odd}/w = (\frac{s}{w})^{m_o} e^{k_o} \quad [\text{pF/m}]$$

$$C_{even}/w = (\frac{s}{w})^{m_e} e^{k_e} \quad [\text{pF/m}]$$

with

$$m_o = \frac{w}{h}[0.619 \log(w/h) - 0.3853] \qquad \text{for } 0.1 \leq s/w \leq 1.0$$

$$k_o = 4.26 - 1.453 \log(w/h) \qquad \text{for } 0.1 \leq s/w \leq 1.0$$

$$m_e = 0.8675, \quad k_e = 2.043(\frac{w}{h})^{0.12} \qquad \text{for } 0.1 \leq s/w \leq 0.3$$

$$m_e = \frac{1.565}{(w/h)^{0.16}} - 1, \quad k_e = 1.97 - \frac{0.03}{(w/h)} \qquad \text{for } 0.3 \leq s/w \leq 1.0$$

For any other dielectric material in the range $2.5 \leq \epsilon_r \leq 15$, the the even and odd mode capacitances can be calculated by using the following factors:

$$C_{odd}(\epsilon_r) = C_{odd}(9.6)[\frac{\epsilon_r}{9.6}]^{0.8}$$

$$C_{even}(\epsilon_r) = C_{odd}(9.6)[\frac{\epsilon_r}{9.6}]^{0.9}$$

After the equivalent capacitances are found, those elements are augmented into the original network, and the inductance elements in the gap region are then removed. The large void area in the central region is also modeled by removing the electrical nodes corresponding to that area. On the other hand, for the modeling of the short circuit pins as shown in Fig. 7.14, an appropriate inductor is allocated to each pin.

To quantify the effect of the gaps and short circuit pins in the split PCB, the 64 mm $\times$ 64 mm PCB is split into two sections as illustrated in Fig. 7.16 and the gap

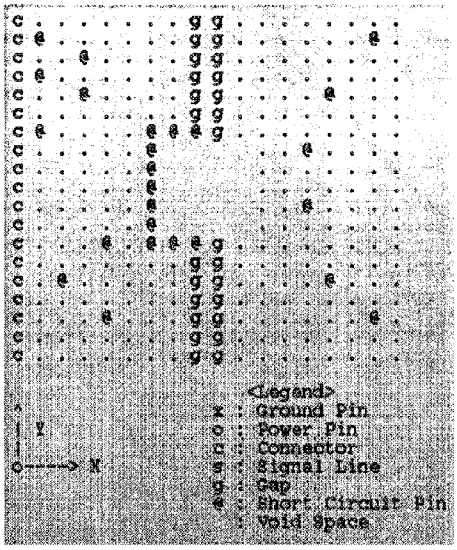
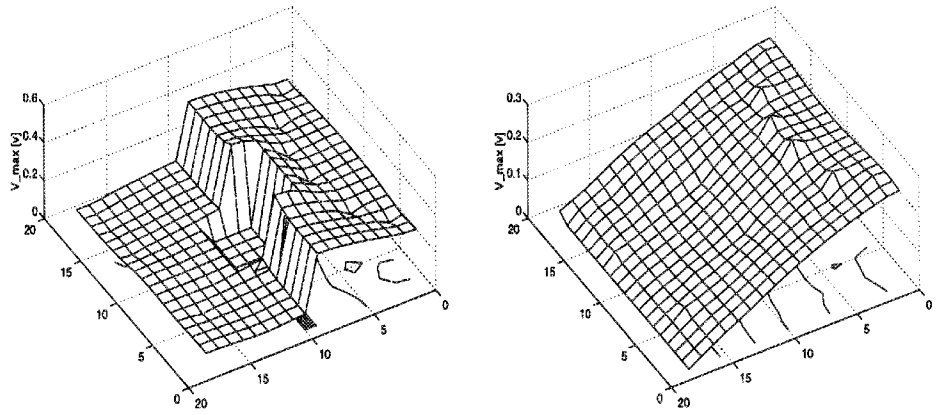


Figure 7.16: Configuration of the split PCB having 25 short circuit pins ('@') and 11 current sources (I_{max} = 100 mA and 0.5 nsec rise/fall time). The dots ('.') represent electrical nodes on the planes. Note that the connector is placed at the left hand side of the board supplying 0.0 V only for the lower plane.



(a) (b)

Figure 7.17: Noise maps on the (a) upper (V_{max} = 420 mV) and (b) lower planes (V_{max} = 260 mV).

spacing s is chosen to be 2.54 mm. In addition, 25 short circuit pins are distributed evenly in the left and right hand sides, and 11 current sources are connected in the central region of the left hand side (denoted as '@' also). The magnitude of the current sources is 100 mA and the rise and fall times are fixed to 0.5 nsec. Fig. 7.17 depicts the potential fluctuations on the upper and lower planes, and reveal the effect of the short circuit pins. The short circuit pins have a tendency to elevate the potential on the lower plane and lower on the upper plane. The potential fluctuation on the left hand side is much smaller than that of the right hand side both on the upper and lower planes because of the connector providing constant potential. Furthermore, the potential difference between the two split planes on the upper plane suggests the effectiveness of the gaps for reducing the overall noise level.

7.4.5 Intel P6 Gadget

For the validation of the proposed approach, the noise level is measured under the control environment for the Intel P6 gadget as illustrated in Fig. 7.18. To minimize the effect of the measurement errors, multiple drivers are provided to switch simultaneously, and then the voltage difference between the power and ground planes at various locations are measured and compared with the modeled result. For the modeling, the lower half of the P6 board is discretized into number of tiles (34×37 non-uniform tiles) and 64 triangular current sources are injected simultaneously between the power and ground pins. Those 64 sets of power and ground pins form two groups (32 in each group) and each aggregated source current group is located in the upper left and right conner of the chip area. The input current waveform and its frequency component are shown in Fig. 7.19. Note that the Fourier components in the signal span up to near Gigahertz range.

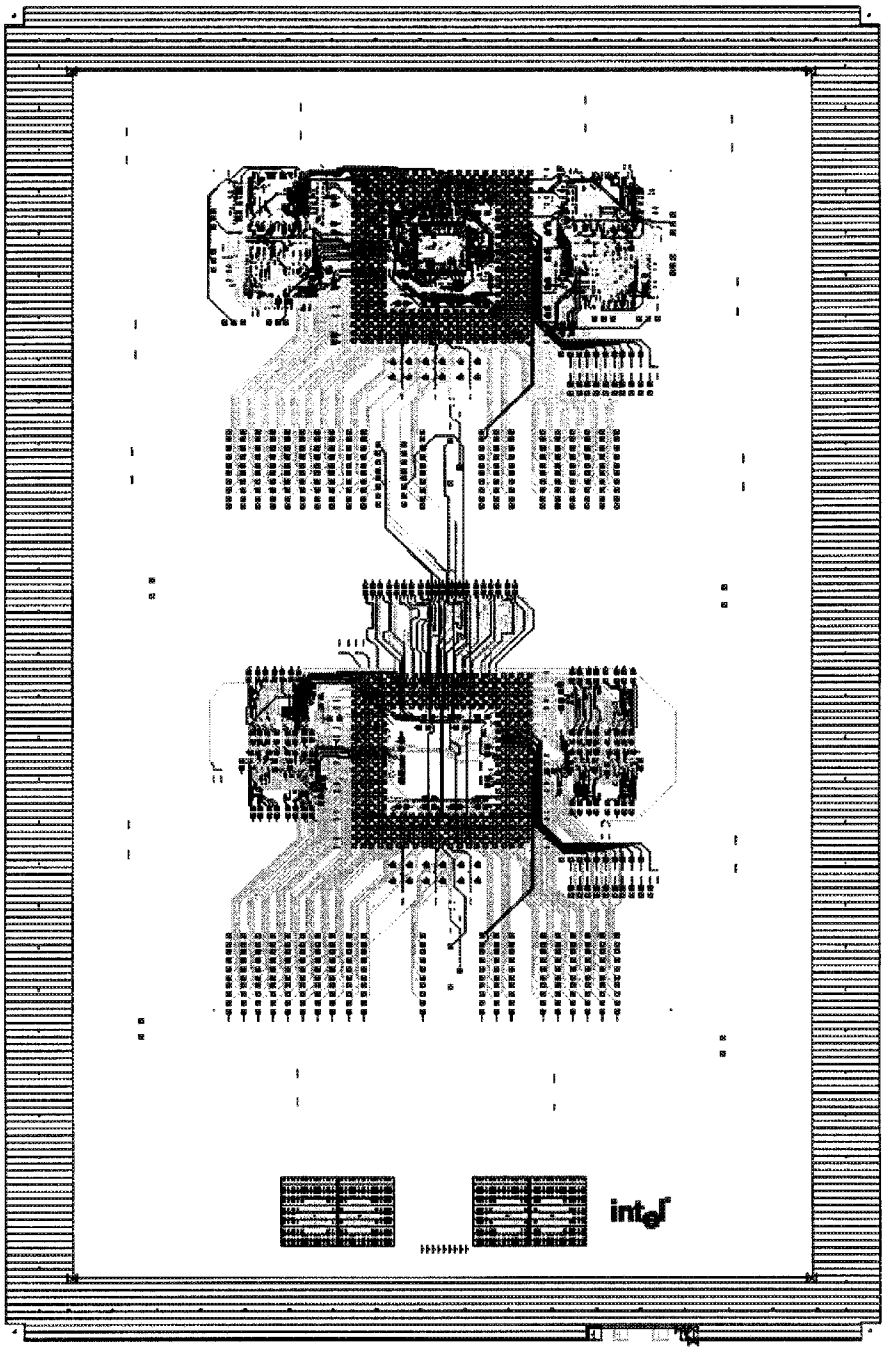


Figure 7.18: Schematics of the Intel P6 gadget.

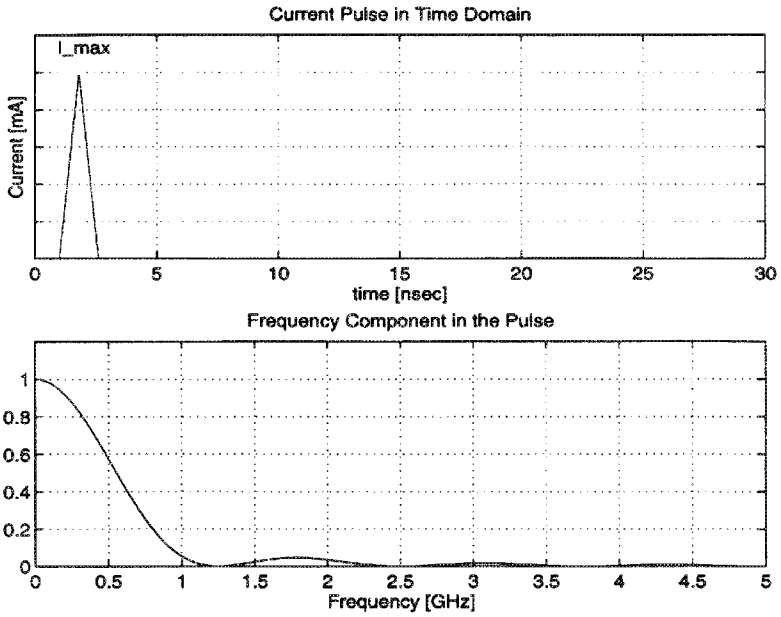


Figure 7.19: Input current waveform (0.8 nsec rise and fall time) and its frequency component.

Fig. 7.20 shows the comparision between the measured and simulated voltage waveforms at 4 different locations denoted as AS41, AP28, AC35, and AL27. These measurement points are located in the upeer right corner of the chip area. As can be observed in the voltage waveforms, the simulated results follow the measurement very closely, even for the small details. With this comparison, the validity and effect of the proposed approach have been proved. Note that in the measurement, voltage sources are used to excite the board, while in the simulation, the equivalent current sources are utilized.

7.4.6 Summary

From the experiments performed in this chapter, the following observations can be made. First, for a given amount of current injection, the SSN increases when the current drivers are placed farther away from the equipotential connectors that

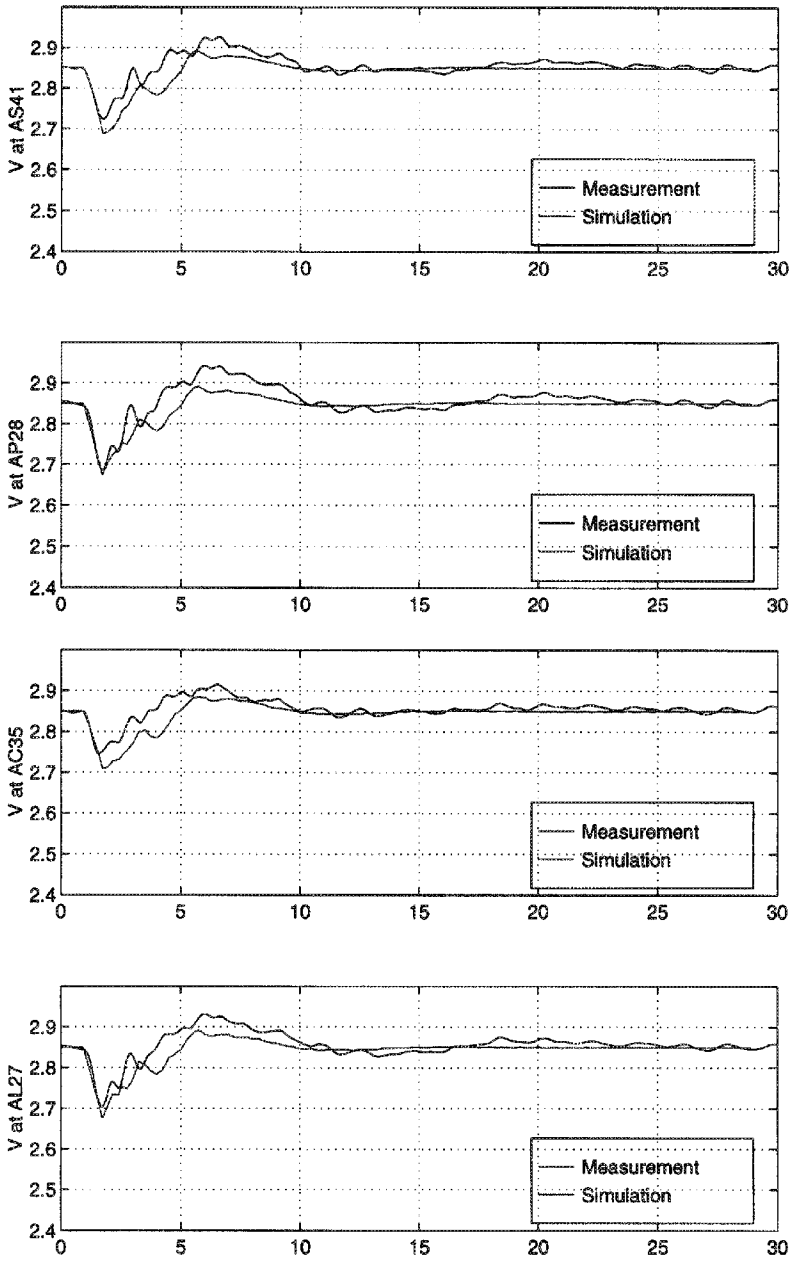


Figure 7.20: Output current waveforms at 4 different points with 64 input current sources switching simultaneously: magnitude I_{max} = 15 mA and rise/fall time t_r = t_f = 0.8 nsec

supply DC power to the board. Second, maximum reduction in the SSN occurs when decoupling capacitors are placed in the vicinity of the current injection points (i.e. between the power and ground driver pins). Third, increasing the value of the decoupling capacitance tends to reduce the magnitude of the SSN. Beyond a critical value, however, further increases in capacitance value does not reduce the overall SSN. This critical value depends on the PCB configuration and the amount of current injected by the drivers. Fourth, the presence of the signal traces marginally contribute to noise on the power and ground planes. Limited evidence, however, suggests that this contribution is dwarfed by the current injection from the drivers. Additional experiments also suggested that significant lead inductances introduced by the decoupling capacitors may in some cases nullify the noise reduction benefits of these capacitors. Fifth, the effective of splitting the power or ground planes are examined giving the evidence of suppressed noise. Finally, the actual 8 layer Intel P6 board is modeled and the excellent comparison between the measurement and simulation proves the accuracy of the hybrid approach.

7.5 Conclusions

This chapter has presented a systematic methodology, combining the finite element full-wave electromagnetic tool and circuit simulator HSPICE, for the modeling and analysis of SSN in digital ICs and packages. In this hybrid methodology, the seemingly contradictory goals of modeling accuracy and global analysis efficiency are reconciled through a divide-and-conquer process. The accuracy is insured by performing detailed EM field analysis on appropriately chosen small sections of the PCB, referred to as tiles, to create lumped electrical equivalent circuit models. The PCB tile models are subsequently combined with the models for chip current and/or

voltage drivers and package leads to produce an electrical simulation model for the PCB power distribution subsystem. A circuit simulator is then used to exercise this model under a variety of current or voltage excitation conditions to yield noise maps that indicate the variation in the power and ground potential as a function of location on the PCB. Furthermore, the effect of the decoupling capacitances and splitting the PCB are simulated, and discovered that the noise levels on the power and ground planes are saturated to a certain value as the decoupling capacitance increases. Finally, a realistic circuit, Intel P6 gadget, is modeled and found that the agreement between the measurement and simulations is very satisfactory, thus proving the effect and accuracy of the proposed hybrid approach.

CHAPTER VIII

CONCLUSIONS

8.1 Summary of Achievements

The main theme of this dissertation is the development of a rigorous but efficient and flexible three-dimensional full-wave electromagnetic modeling tool for the characterization of high-speed high-frequency interconnects ranging from a simple via hole to an entire millimeter-wave package. For this purpose, the edge-based finite element method with tetrahedral sub-domain elements has been successfully developed and parallelized on a distributed memory parallel computer, the IBM SP2. It is worth mentioning that the use of the edge-based basis functions renders the FEM solutions free from spurious modes which until now have been a bottleneck of the node-based FEM. To overcome the limitation imposed on general partial differential equation techniques regarding the truncation of the computational domain at a finite size, an isotropic absorbing material is utilized for the simulation of open boundary problems, and its performance is proved to be satisfactory in MMIC applications, which have inhomogeneous material configurations. Furthermore, the parallelization of the developed FEM technique makes the time consuming full-wave analysis more affordable and attractive as a design and optimization tool for high-speed high-frequency interconnects.

The development of a stable and rigorous FEM technique raises the possibility of real time characterization of complicated microwave and millimeter-wave devices and circuits which was not feasible before. In this research effort, the parallelized FEM technique has been applied to the characterization of various MMIC components: single and double via holes, plated-through-hole, CPW-to-microstrip transitions, CPW-to-slot transitions, CPW-to-waveguide transition, and hermetic wall and bead transitions. Furthermore, a K/Ka-band MMIC package with dozens of vertical via holes, DC bias lines, bonding wires and gaps is thoroughly investigated, and the internal package resonances are identified along with a few possible treatments of the phenomenon.

For the via hole geometries, appropriate equivalent circuits are derived to represent the structures as a lumped circuit. These equivalent circuits are then used in system level electromagnetic modeling of digital ICs and packages in Chapter 7 to provide equivalent circuits for tiles.

One of the greatest advantage of using the finite element method is its capability of field reconstructions at any computational domain. Field visualization by means of these field reconstructions in a domain offers a thorough understanding of the electromagnetic phenomena occurring in reality and helps to diagnose any potential circuit malfunctions.

Hybrid approach combining electromagnetic full-wave analysis and circuit simulation has also been proposed for the system level modeling of digital ICs and packages. As presented in Chapter 7, remarkable agreement between the simulation results and measurement data has been achieved for an 8-layer INTEL P6 gadget. Considering the fact that there are hundreds of signal traces and vertical via holes, the correlation between the predicted and measured data proves the effectiveness

of the proposed technique. Furthermore, the simultaneous switching noise and its suppression by placing decoupling capacitors are also closely studied and visualized. Since the technique does not assume the actual ground planes to be perfect, the potential fluctuations on the power as well as ground planes are easily simulated.

8.2 Suggested Future Work

Several possible directions could be taken as future research:

- refinement and improvement of the finite element method itself
- application of the FEM for the characterization of structures which are not feasible to characterize using other methods
- efficient parallelization on shared as well as distributed memory machines
- further improvement of the hybrid method presented in Chapter 7 including automatic interfacing between circuit layout files and tiling processor.

First of all, the refinement and improvement of the finite element method includes a few interesting topics, such as the development of a more sophisticated and adaptive three-dimensional mesh generator, improvement of absorbing boundary conditions, application of a more efficient linear equation solver, more effective and interactive electromagnetic field visualization, etc. Furthermore, passive and active lumped electrical elements can be also incorporated into the FEM framework.

Second, the finite element method can be applied to the characterization of other interesting high-speed high-frequency circuits and interconnects as well as packages. The recent trend of using the electromagnetic simulator for system level applications suggests a possible direction. Since most circuit and system designers heavily

depend on their experience and intuitions which might be misleading, rigorous theoretical data can contribute to a more thorough understanding of the electromagnetic phenomena occurring in and around circuits.

Third, effective parallelization of the finite element method on different types of parallel computers based on shared or distributed memory can speed up the time consuming full-wave analysis and could lead to the full-wave analysis tool becoming a design and optimization vehicle. Another important task is the effective parallelization of conjugate gradient type linear equation solvers. Since these types of solvers utilize repeated matrix-vector multiplications, efficient parallel matrix-vector multiplication could enhance the overall performance of the FEM technique.

Finally, the hybrid approach combining the FEM and circuit simulator for system level modeling of digital ICs and packages can be evolved to its next generation by developing automatic interfacing between circuit layout and tiling processors, constructing a more accurate and extensive equivalent circuit library, and automatic placement of decoupling capacitors to minimize the simultaneous switching noise. Furthermore, for the accurate simulation of the non-linear characteristics of the drivers, more sophisticated driver modeling will be necessary.

APPENDICES

APPENDIX A

Calculation of the Element Matrix Entries

The final matrix equation of the FEM could be read as follows:

$$[\mathbf{A}]^T[\mathbf{x}] = [\mathbf{b}]$$

where

$$\begin{aligned}
[\mathbf{A}] &= \bigcup_{e=1}^{M}\{[\mathbf{U}^e] - k_o^2[\mathbf{V}^e]\} \\
[\mathbf{x}] &= \bigcup_{e=1}^{M}[\mathbf{x}^e] \\
[\mathbf{b}] &= \bigcup_{e=1}^{M}[\mathbf{b}^e]
\end{aligned}$$

and M denotes total number of tetrahedrons. The number of linear equations, which is equivalent to the dimensions of matrix $[\mathbf{A}]$, is in general different from the number of tetrahedrons in the domain. The entries of the elementary FEM matrices for each tetrahedron could be evaluated by analytical and numerical integrations of the inner product with the aid of basic integration formulas for shape functions[1]. The final expressions for each matrix entry of the equation are derived as follows:

$$A_{ij}^e = U_{ij}^e - k_o^2 V_{ij}^e$$

[1] $\int\int\int_{V^e}(\lambda_1)^a(\lambda_2)^b(\lambda_3)^c(\lambda_4)^d dxdydz = \frac{a!b!c!d!}{(a+b+c+d+3)!}6V^e$

where

$$\begin{aligned} U_{ij}^e &= \langle \mu_r^{-1} \nabla \times \mathbf{W}_i, \nabla \times \mathbf{W}_j \rangle \\ V_{ij}^e &= \langle \epsilon_r \mathbf{W}_i, \mathbf{W}_j \rangle \end{aligned}$$

and $1 \leq i, j \leq 6$. Considering the fact that the $\mathbf{g}_i$ and $\mathbf{g}_j$ are constant vectors, the evaluation of the U_{ij}^e can be performed directly by using one of the properties of the edge basis function, equation (2.17), and yields:

$$U_{ij}^e = 4V^e \mu_r^{-1} (\mathbf{g}_i \cdot \mathbf{g}_j).$$

The V_{ij}^e may be broken into three terms as

$$V_{ij}^e = \epsilon_r (P_1 + P_2 + P_3)$$

where

$$\begin{aligned} P_1 &= \langle \mathbf{f}_i, \mathbf{f}_j \rangle = V^e (\mathbf{f}_i \cdot \mathbf{f}_j) \\ P_2 &= \langle \mathbf{f}_i, \mathbf{g}_j \times \mathbf{r} \rangle + \langle \mathbf{g}_i \times \mathbf{r}, \mathbf{f}_j \rangle \\ P_3 &= \langle \mathbf{g}_i \times \mathbf{r}, \mathbf{g}_j \times \mathbf{r} \rangle. \end{aligned}$$

Note that the computation of P_1 can be perfomed easily since the $\mathbf{f}_i$ and $\mathbf{f}_j$ are constant vectors by definition. Evaluation of the P_2 and P_3 can also be done analytically:

$$P_2 = \frac{V^e}{4} (T_x S_x + T_y S_y + T_z S_z)$$

and

$$\begin{aligned} P_3 = \frac{V^e}{20} \{ & \quad (g_{iy} g_{jy} + g_{iz} g_{jz}) [S_{xx} + (S_x)^2] \\ & + (g_{ix} g_{jx} + g_{iz} g_{jz}) [S_{yy} + (S_y)^2] \\ & + (g_{ix} g_{jx} + g_{iz} g_{jz}) [S_{yy} + (S_y)^2] \end{aligned}$$

$$
\begin{aligned}
&- (g_{ix}g_{jy} + g_{iy}g_{jx})[S_{xy} + S_x S_y] \\
&- (g_{iy}g_{jz} + g_{iz}g_{jy})[S_{yz} + S_y S_z] \\
&- (g_{ix}g_{jz} + g_{iz}g_{jx})[S_{xz} + S_x S_z] \quad \}
\end{aligned}
$$

where

$$
\begin{aligned}
\mathbf{T} &= T_x\hat{x} + T_y\hat{y} + T_z\hat{z} = (\mathbf{f}_i \times \mathbf{g}_j) + (\mathbf{f}_j \times \mathbf{g}_i) \\
\mathbf{g}_i &= g_{ix}\hat{x} + g_{iy}\hat{y} + g_{iz}\hat{z} \\
S_x &= \sum_{i=1}^{4} x_i, \quad S_y = \sum_{i=1}^{4} y_i, \quad S_z = \sum_{i=1}^{4} z_i \\
S_{xx} &= \sum_{i=1}^{4} x_i^2, \quad S_{yy} = \sum_{i=1}^{4} y_i^2, \quad S_{zz} = \sum_{i=1}^{4} z_i^2 \\
S_{xy} &= \sum_{i=1}^{4} x_i y_i, \quad S_{yz} = \sum_{i=1}^{4} y_i z_i, \quad S_{xz} = \sum_{i=1}^{4} x_i z_i.
\end{aligned}
$$

In the above, the constant vectors $\mathbf{T}$ and $\mathbf{g}_i$ are computed numerically for a given tetrahedron. The volume of a tetrahedron with four nodal coordinates of the vetexes, $(x_i, y_i, z_i), i = 1, \ldots, 4$, is given by determinant of 4×4 matrix as follows:

$$
V^e = \frac{1}{6}\det \begin{bmatrix} 1 & x_1 & y_1 & z_1 \\ 1 & x_2 & y_2 & z_2 \\ 1 & x_3 & y_3 & z_3 \\ 1 & x_4 & y_4 & z_4 \end{bmatrix}.
$$

APPENDIX B

Pre-conditioned Conjugate Orthogonal Conjugate Gradient Method

For the solution of linear equation $\mathbf{Ax} = \mathbf{b}$ with sparse complex symmetrix matrix $\mathbf{A}$, the conjugate orthogonal conjugate gradient (COCG) method [58] is implemented in this study. The COCG method is different from other projection type methods, such as the congugate gradient (CG) method, conjugate gradient squared method and GMRES, since these methods are based on forming an orthogonal basis for Krylov subspace[1], but not in the COCG case. For the non-Hermitian symmetric matrix, the orthogonality cannot be achived in a simple way.

The key step in the COCG method is the new definition of the orthogonality[2] for the residual vectors:

$$(\bar{\mathbf{v}}_m, \mathbf{v}_n) = \delta_{mn}$$

where

$$(\mathbf{x}, \mathbf{y}) = \sum_j \bar{x}_j y_j.$$

The subscripts m and n in the vectors, $\mathbf{x}_m$ and $\mathbf{x}_n$, denote the vectors in the m^{th} and n^{th} iterations. Now, with the new definition of the conjugate orthogonality in mind,

[1]The j-dimensional Krylov subspace $K^j(\mathbf{A} : \mathbf{r}_o)$ for a linear system $\mathbf{Ax} = \mathbf{b}$ with non-singular $\mathbf{A}$ is defined as the span of the vectors $\{\mathbf{v}_o, \mathbf{Av}_o, \ldots, \mathbf{A}^{j-1}\mathbf{v}_o\}$ for a given initial residual $\mathbf{v}_o = \mathbf{r}_o = \mathbf{b} - \mathbf{Ax}_o$.

[2]The definition of the Hermitian orthogonality in the inner product space is given as : $(\mathbf{x}_m, \mathbf{x}_n) = \delta_{mn}$

the COCG algorithm can be derived from the standard conjugate gradient procedure [48]-[57] by replacing the complex Hermitian inner product with the bilinear form $[\mathbf{x},\mathbf{y}] = \sum_j x_j y_j$ as summarized in the following:

Initialization

$$\begin{aligned}
\mathbf{x}_o &: \text{ given} \\
\mathbf{v}_o &= \mathbf{b} - \mathbf{A}\mathbf{x}_o; \quad \mathbf{p}_{-1} = 0; \quad \beta_{-1} = 0; \\
\mathbf{w}_o &= \mathbf{K}^{-1}\mathbf{v}_o; \quad \rho_o = [\mathbf{v}_o, \mathbf{w}_o];
\end{aligned}$$

For $j = 0, 1, 2, \ldots$ iterations

$$\begin{aligned}
\mathbf{p}_j &= \mathbf{w}_j + \beta_{j-1}\mathbf{p}_{j-1} \\
\mathbf{u}_j &= \mathbf{A}\mathbf{p}_j \\
\mu_j &= [\mathbf{u}_j, \mathbf{p}_j]; \qquad \text{if } \mu_j = 0, \text{ then quit. } \Rightarrow \text{ Failure !} \\
\alpha_j &= \rho_j/\mu_j \\
\mathbf{x}_{j+1} &= \mathbf{x}_j + \alpha_j\mathbf{p}_j; \quad \text{if } \mathbf{x}_{j+1} \text{ is accurate enough, then quit. } \Rightarrow \text{ Convergence !} \\
\mathbf{v}_{j+1} &= \mathbf{v}_j - \alpha_j\mathbf{u}_j \\
\mathbf{w}_{j+1} &= \mathbf{K}^{-1}\mathbf{W}_{j+1}; \\
\rho_{j+1} &= [\mathbf{v}_{j+1}, \mathbf{w}_{j+1}]; \quad \text{if } \rho_{j+1} \text{ is small, then quit. } \Rightarrow \text{ Failure !} \\
\beta_j &= \rho_{j+1}/\rho_j
\end{aligned}$$

Next j

Note that $\mathbf{K}$ is used as a pre-conditioning matrix and in this study the diagonal entries of the matrix $\mathbf{A}$ are used, i.e. $[K_{ij}] = [A_{ij}\delta_{ij}]$. As a result, the inverse of $\mathbf{K}$ can be computed without additional computations: $[K_{ij}]^{-1} = [A_{ij}^{-1}\delta_{ij}]$. Considering the fact that the most computional efforts in the CG type algorithm is devoted to the matrix-vector multiplication, the COCG method provides clear advantage over the

CG methods, since COCG method requires only one matrix-vector multiplication in each iteration instead two in the CG method. Furthermore, the matrix-vector multiplication of a sparse symmetric matrix can be highly optimized with minimum storage requirements. Parallelization of the matrix-vector multiplication routine on shared and distributed memory machines would be promising.

APPENDIX C

Network Parameters

To characterize a given circuit, several different network parameters are needed to be extracted. For example, for a vertical via hole, connecting two different signal lines on different layers or providing a ground path to a transmission line, the inductance of the via hole is a vital information for its characterization, and this inductance can be computed by two different methods. In the followings, two different methods of extracting equivalent via hole inductance are sketched, and the mathematical background of the extraction of the scattering parameters for one and two-port networks are briefly discussed. In general, the scattering parameters are used to characterize any given VLSI and MMIC interconnects.

C.1 Inductance of Vertical Via Hole

The inductance of a vertical via hole can be computed from several different methods, however, in this study, two different methods are utilized: current/flux method and scattering parameter method. In the flux/current method, the inductance of a via hole is calculated by taking the ratio of the current flowing on the via hole to the flux surrounding the current path as illustrated in Fig. C.1. The current flowing through the vertical via hole is evaluated from the closed path line integral as

$$I = \oint_C \mathbf{H} \cdot d\mathbf{C} \quad [Ampere]$$

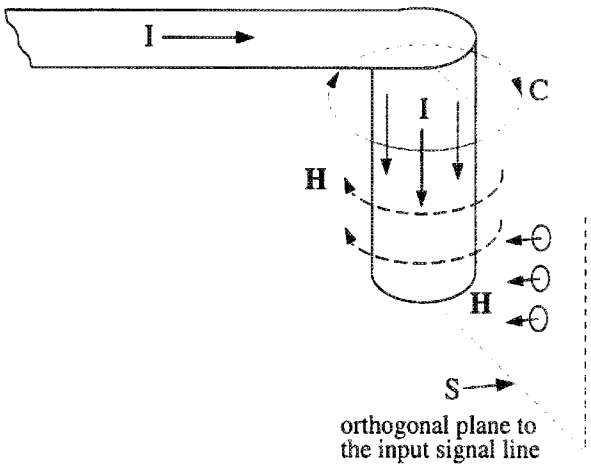


Figure C.1: Vertical via hole as a current path.

and the flux wounding the vertical current path is computed as

$$\Phi = \iint_S \mu_o \mu_r \mathbf{H} \cdot d\mathbf{S} \quad [Wb/m^2].$$

From the value of the current and flux computed above, the inductance of the vertical current path is computed as:

$$L = \frac{\Phi}{I} \quad [Henry].$$

This approach has a certain advantage to understand and characterize the effect of the vertical via hole, since the effect of the vertical current can be isolated from the other current components due to the orthogonality property of the electromagnetic fields. Thus inductance computed from the flux/current definition contains the effect of the via only.

In the second approach, the scattering parameters and lumped equivalent circuit network are used to extract the equivalent via hole inductance. The scattering parameters are computed from the voltage or current standing wave patterns on the input transmission line as will be discussed in the following sections. After the

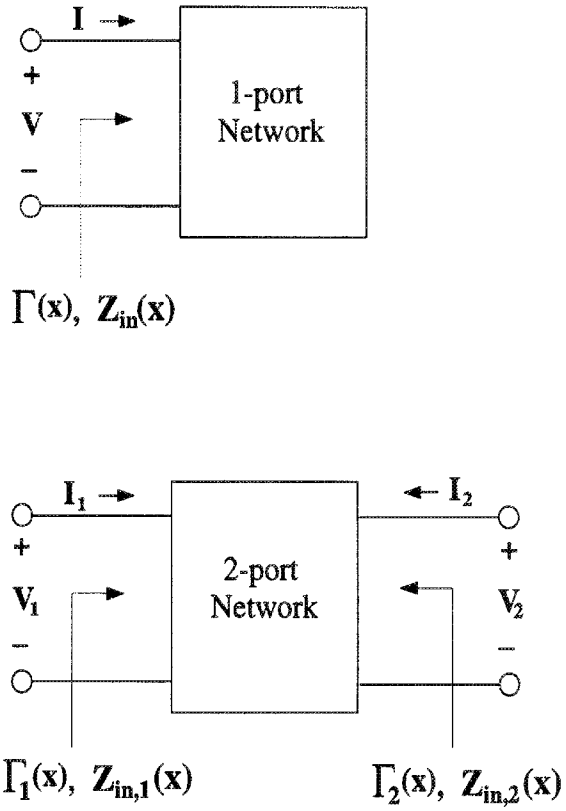


Figure C.2: Equivalent circuits for one- and two-port network.

scattering parameters are obtained, those values are matched with the frequency response of the chosen equivalent circuit. Note that the obtained inductance and capacitance values comprise the overall effect beyond the reference plane and also depend on the position of the reference plane.

C.2 One-Port Network

To characterize any one-port network (refer to Fig. C.2), the input reflection coefficient is determined from the voltage standing wave pattern, and to obtain unique values of the phase and magnitude of the reflection coefficient, the position of the reference plane has to be predefined and fixed. In this syudy, all the scattering pa-

rameters are computed with the reference plane chosen at the position where the discontiniuty starts. First, from the voltage maximum and minimum values the voltage standing wave ratio (VSWR) is determined:

$$VSWR = \frac{|V_{max}|}{|V_{min}|}.$$

Note that for a lossless circuit, the VSWR has infinite value. After the VSWR is computed, the reflection coefficient looking towards the discontinuity is determined anywhere on the transmission line as:

$$\Gamma(x) = \frac{VSWR - 1}{VSWR + 1} e^{-j2\beta_g(x_{max} - x)}$$

where x_{max} is the position of a voltage maximum. If a circuit is lossless, then the magnitude of $\Gamma(x)$ becomes unity, and as a result, the phase of the reflection coefficient $\Gamma(x)$ becomes an important factor. Moreover, the normalized input impedance $z(x)$ at any point on the transmission line can be determined from the reflection coefficient $\Gamma(x)$ as:

$$z(x) = \frac{1 + \Gamma(x)}{1 - \Gamma(x)}.$$

C.3 Symmetric Two-Port Network

The network parameters for symmetric two-port networks can be determined by analyzing the voltage or current distributions on the input and output ports with the even and odd mode excitations. In general, any symmetric two-port network can be represented as shown in Fig. C.2 and characterized by the following relationship between the voltage and current at the ports ([232], pp.216-220)

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}.$$

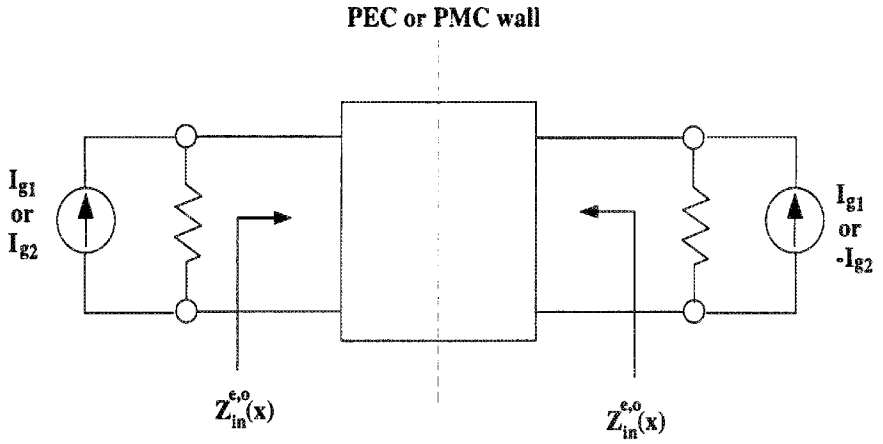


Figure C.3: Symmetric two port network with the even and odd mode excitations corresponding to placing magnetic and electric walls at the center of the circuit.

First of all, to extract the scattering parameters the even and odd mode input impedances (z_{in}^e, z_{in}^o) are computed from the two different excitations, even and odd mode. From these values, the impedance parameters are determined according to

$$z_{11} = \frac{z_{in}^e + z_{in}^o}{2}, \quad z_{12} = \frac{z_{in}^e - z_{in}^o}{2}.$$

Note that for the passive symmetric two-port reciprical networks, the z_{11} is equal to z_{22}, and z_{21} to z_{12}. When the excitation sources are current as shown in Figure C.3, the even mode excitation ($I_{g1} = I_{g2} = I_o$) corresponds to placing a perfect magnetic conducting (PMC) wall at the center of the circuit, since the voltage standing wave pattern has maximum at the center and the voltage maximum is equivalent to open circuit, thus leading to PMC wall. Similarly, the odd mode excitation ($I_{g1} = -I_{g2} = I_o$) corresponds to placing the PEC wall at the center of the circuit.

The scattering parameters are then obtained from the normalized impedance parameters by using the following equations:

$$S_{11} = S_{22} = \frac{z_{11}^2 - 1 - z_{12}^2}{z_{11}^2 + 2z_{11} - z_{12}^2 + 1}$$

$$S_{12} = S_{21} = \frac{2z_{12}}{z_{11}^2 + 2z_{11} - z_{12}^2 + 1}$$

where S_{11} is equal to S_{22}, and S_{12} to S_{21}, because the 2-port network is reciprocal and symmetric.

C.4 Asymmetric Two-Port Network

In order to characterize any asymmetric two-port network, three different excitation mechanisms are needed to obtain the impedance parameters z_{11}, z_{22} and z_{12} with the method employed in this study. As three different excitation pairs, the even ($I_{g1} = I_{g2} = I_o$), odd ($I_{g1} = -I_{g2} = I_o$) and sum ($I_{g1} = 1$, $I_{g2} = 2$) excitation mechanisms are utilized in this study. From these excitations, the normalized impedance parameters are evaluated by using the following relations [233]

$$\begin{aligned} z_{11} &= z_{1s} + (z_{1s} - z_{1o})(z_{1s} - z_{1e})\frac{(z_{2e} - z_{2o})}{\Delta} \\ z_{22} &= z_{2s} - (z_{2s} - z_{2o})(z_{2s} - z_{2e})\frac{(z_{1e} - z_{1o})}{\Delta} \\ z_{12} &= \pm(z_{1e} - z_{11})\sqrt{\frac{z_{2e} - z_{22}}{z_{1e} - z_{11}}} \end{aligned}$$

where

$$\Delta = (z_{1s} - z_{1o})(z_{2s} - z_{2e}) - (z_{1s} - z_{1e})(z_{2s} - z_{2o}).$$

In the above expressions, z_{1e}, z_{2e}, z_{1o}, z_{2o}, z_{1s} and z_{2s} are the normalized input impedances at the port 1 and 2 for even, odd and sum excitation pairs, respectively. The sign of the z_{12} should be carefully decided as discussed in [233].

The scattering parameters for asymmetric 2-port network can be determined with the following expressions:

$$S_{11} = \frac{z_{11}^2 - 1 - z_{12}^2}{(z_{11} + 1)(z_{22} + 1) - z_{12}^2}$$

$$S_{22} = \frac{z_{22}^2 - 1 - z_{12}^2}{(z_{11}+1)(z_{22}+1) - z_{12}^2}$$
$$S_{12} = \frac{2z_{12}}{(z_{11}+1)(z_{22}+1) - z_{12}^2}$$

Note that for reciprocal 2-port network the S_{12} is equal to the S_{21}, and for symmetric network, S_{11} equals S_{22}. For a lossless 2-port network, $|S_{11}|^2 + |S_{12}|^2 = 1$.

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