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MMIC Passive and Active Structures

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by

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ABSTRACT

MMIC PASSIVE AND ACTIVE STRUCTURES

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In this thesis several passive and active MMIC structures are designed, fabricated and tested in order to develop a monolithic transmit/receive system residing on a single chip with enhanced performance at millimeter-wave frequencies. The capability of applying micromachining to improve the efficiency of microstrip patch antennas on high index materials such as silicon, GaAs, or InP is validated. Patch antennas on Duroid substrates resonating at 13 GHz with 64% and 28% increase in impedance bandwidth and efficiency, respectively, as well as smooth radiation patterns are successfully demonstrated by creating a cavity underneath the antenna. The importance of the placement of the cavity relative to the radiating edges of the antenna in order to improve the efficiency is also shown. A minimum distance equal to two times the substrate thickness is required. A planar micromachined resonator on silicon with a high quality factor, Q, at 10.4 GHz is also fabricated and tested; the measured Q is 506 while the insertion loss and the bandwidth are 0.36 dB and 5% , respectively. A bandwidth of 2% with a loss of 1.1 dB is also achieved for a slightly different topology of the micromachined resonator. Insertion loss measurements under different

temperature ambients showed a negligible drift in the resonant frequency.

Regarding active structures, Finite Ground Coplanar line based monolithic multipliers and mixers operating in W-band are designed, fabricated and tested. The performance of FGC lines on GaAs and quartz substrate with a polyimide overlay for passivation is first investigated. Experimental results that show the dependence of the line characteristics on the geometry rather than the substrate material are presented. Next, a Q=2 monolithic doubler with 17.2% efficiency, 10% minimum bandwidth and 66 mW output power, as well as a Q=3 doubler with 22% efficiency, 8.5% bandwidth and 50 mW output power in W-band are demonstrated. A doubler from 37.5 to 75 GHz that implements four diodes with a 12.5% efficiency and an output power of 115 mW is also presented. Furthemore, a method that increases the efficiency of monolithic multipliers by reducing the loss of the FGC lines is shown. Finally, a monolithic mixer residing on the same material with the multipliers is fabricated and tested. A novel fabrication technique that combines channel etched diodes of small areas with air-bridges for the passive circuits is developed. A single-sideband conversion loss of 11 dB is achieved at 79 GHz for an IF frequency of 4 GHz and an LO power of 8.8 dBm.

To my beloved mother,

Areti-Eleni Spiliopoulou

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INTRODUCTION

1.1 Motivation

The use of millimeter-wave technology in military and commercial applications has drawn the attention of the microwave community for more than three decades due to its advantages over other bands of the electromagnetic spectrum, as well as the lack of frequencies for new services. Since the size of any microwave circuit or component is dictated by the frequency of operation, implementation of the millimeter-wave region (30-300 GHz) can result in very small systems. This is extremely important for airborne and space applications, where launch and deployment costs depend heavily on the volume of the system that is to be deployed. Furthemore, millimeter-waves allow for antennas with high gain and directivity that are essential for point-to-point communication systems (e.g. between a satellite and an earth base station) and radars.

For space and airborne applications attenuation through the earth's atmosphere is a major consideration. In general, the attenuation of the microwave energy increases with frequency with the exceptions of a few minima that occur at 35 GHz, 94 GHz, 140 GHz, 220 GHz etc. These "windows" of minimum atmospheric absorption make millimeter-wave

systems ideal for such applications. In addition, millimeter-waves unlike infrared and optical wavelengths have the ability to permeate fog, dust and smoke.

Commercial applications of millimeter-wave systems include short-haul line-of-sight transmission links for personal communication networks (PCN's) that operate at 38 GHz, wireless cable at 28 GHz, wireless radio local area networks (LAN's) and mobile broadband systems [4]. In recent years, research efforts have also focused on automotive radar sensors for anti-collison radars at 77 GHz, intelligent cruise control and road transport informatics. Aircraft landing systems and earth remote sensing are other areas where millimeter-waves have been employed [5]. The latter is of major significance due to the intense environmental studies currently under way and the changing conditions of our planet. Of course, military communication systems and radars as well as satellite communications were the first applications of millimeter-wave systems.

Until the early 80's most of the millimeter-wave components and systems were built with waveguide technology (rectangular or cylindrical). Waveguides offer low-loss, high quality factor circuits but are bulky and heavy thus imposing cost limitations on airborne and space systems. In addition, waveguide components are expensive to manufacture since they have to be precision machined one at a time, and at higher operating frequencies their fabrication complexity increases. The bandwidth of such systems is also limited by the operational bandwidth of the waveguides that are used. With the maturity of integrated circuit (IC) fabrication techniques and the increased need for high circuit integration and compact designs, the microwave community has started focusing its attention on Monolithic Microwave/Millimeter-wave Integrated Circuits (MMIC's). MMICs offer the advantages of small size and weight, that further decrease the cost of airborne and space applications, low fabrication cost since they can be batch fabricated using standard IC techniques and

improved reproducibility and reliability. Moreover, MMIC's can allow for broad band operation if designed properly and easy integration of active devices such as diodes and transistors. As a result, entire communication and radar systems can now be fabricated on a single planar substrate or a multi-layered chip with vertical interconnects connecting the various layers [6], [7]. The operating frequency can also be increased, thus satisfying the high demand for new spectrum bands.

As system requirements for faster data transmission in lighter compact designs drive the technology area, higher frequency design solutions with large density layouts that include radiating elements, passive circuitry, oscillator sources and have light weight, small size and optimum performance, are required. Such a design can be seen in Fig. 1.1 and represents a monolithic transmit/receive system that operates at higher frequencies (W-band) and constitutes the RF front end of any communication or radar system. The transmitter includes a frequency multiplier that translates a lower frequency signal into a much higher one, an amplifier that increases the output power of the multiplier and an antenna that radiates the incoming energy. At the receiver, the high frequency signal captured by the antenna is amplified by a low noise amplifier (LNA) and is then down converted to a much lower one by a sub-harmonic mixer. For isolating a particular frequency spectrum, narrow band filters and diplexers can be impemented either right after the antenna or at other stages of the receiver. On-wafer packaging that reduces interaction between the different components and offers electrical and mechanical protection, as well as a means for heat dissipation, to both the transmitter and receiver can also be achieved. All of the passive and active components, including the package, can be fabricated on Silicon or GaAs substrate with standard integrated circuit fabrication techniques that would significantly lower the total cost.

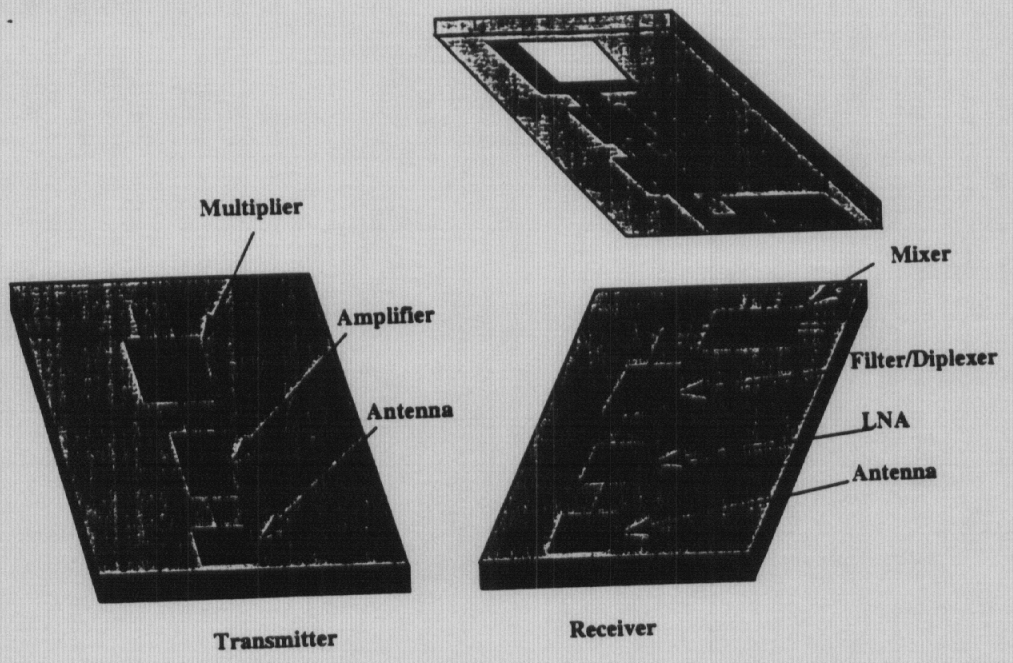


Figure 1.1: Monolithic transmit/receive module for communication and radar systems.

MMIC's are designed and fabricated using planar circuit technology that usually implements two types of transmission lines: the microstrip line (Fig. 1.2(a)) and the coplanar waveguide (CPW) (Fig. 1.2(b)). The air-dielectric interface that exists in both of these lines introduces several parasitic effects that are pronounced as the operating frequency increases. These effects include increased dielectric loss, substrate moding where the power can propagate inside the substrate in the form of unwanted modes, and dispersion. As a result, MMIC's operating at high frequencies (W band) can have some important limitations. These limitations are augmented by the non-availability of higher frequency solid-state oscillator sources that are difficult to fabricate. These sources are very important for heterodyne receiver applications where an incoming high frequency (RF) signal is down converted to a much lower frequency (IF) signal. The objective of this thesis is to find techniques that address these limitations encountered in planar, monolithically integrated passive and active circuits operating at higher frequencies (W band), with the goal of designing a monolithic

transmit/receive module that offers optimum performance and minimum cost.

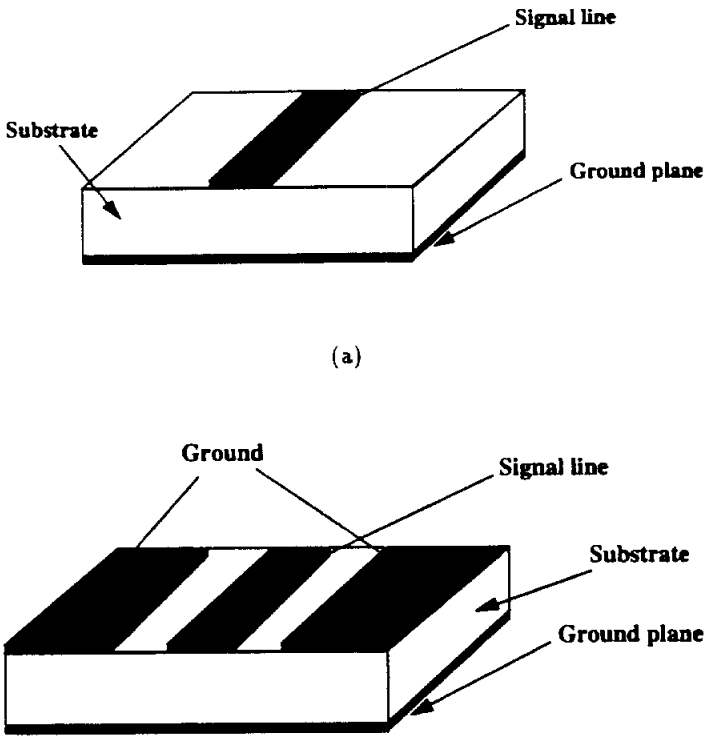


Figure 1.2: Planar transmission lines: (a) microstrip and (b) coplanar waveguide (CPW).

One of the solutions to the restrictions imposed in passive MMIC's, makes use of the micromachining techniques. Micromachining is a technology widely used in the development of micro-electro-mechanical systems (MEMS), sensors and actuators [8] and its implementation in the microwave field is relatively new. The first application in microwave circuits was that of membrane supported antennas for imaging arrays [9]. Other developments on antennas reported since then include microstrip patches suspended on a dielectric membrane [10] over air or sitting on a substrate with periodically spaced holes [11] in order to increase the radiation efficiency. Regarding planar resonators and filters, micromachining was used to suspend microstrip and CPW resonators on membrane [12]- [13] in order to increase

the quality factor and achieve filter designs with very narrow bandwidth and very small loss. All of the previous mentioned examples illustrate the potential of micromachining to circumvent the problems associated with planar circuits operating at high frequencies.

For active MMIC structures, frequency multipliers and mixers operating in W-band and D-band have been realized. Frequency doublers on GaAs using microstrip line technology with 25% efficiency at 94 GHz and 2.8% efficiency at 320 GHz have been reported [14]-[15]. A modified version of the CPW line, the Finite Ground Coplanar (FGC) line, was used to fabricate a 40/80 GHz doubler with 15-16% efficiency and wide bandwidth [16]. A hybrid x2 subharmonic mixer on silicon with the diodes flip-chip bonded achieved a conversion loss of 7 dB at 94 GHz [17]. The excellent results obtained with all of the above active MMIC structures demonstrate the capability to integrate active devices with passive circuits in planar environments at high operating frequencies with very good performance.

1.2 Silicon Micromachining

Silicon has been used as a mechanical material in order to make miniature devices and components since the early 70's, with the first applications in the areas of sensors and transducers. The major process that gives silicon "chips" the various shapes and geometries is micromachining. When a silicon wafer is immersed in an appropriate chemical, then it starts to etch with the process depending on the etchant, the orientation of the wafer and the presence of dopants. The most commonly used etching systems are: a) ethylene diamine, pyrocatechol and water (EDP), b) KOH and water, c) HF, HNO_3 and acetic acid and d) Tetramethyl Ammonium Hydroxide in water (TMAH) [18],[19]. Except for HF-Nitric, all of these chemical etchants are anisotropic. This means that the etch rate strongly depends on the crystallographic orientation of the wafer.

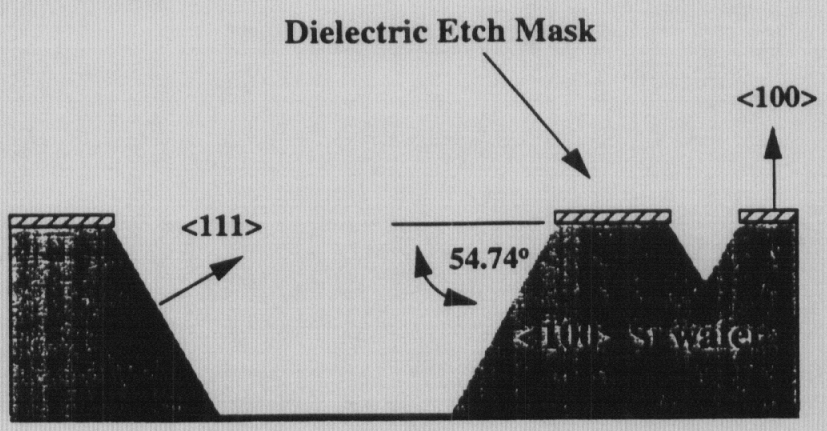


Figure 1.3: Anisotropic etching profile and geometry for the ≺100≻ oriented silicon wafer.

The crystal lattice of the silicon wafer is described by the "Miller indices", which express directions and planes within the crystal using three integer numbers [20]. For EDP, KOH and TMAH the anisotropic behavior is due to the fact that ≺111≻ surfaces are attacked at a much slower rate than all other crystallographic planes (etch-rate ratios as high as 1000 have been reported). Fig. 1.3 shows the etching profile of a standard ≺100≻ oriented wafer, used for all of the work presented in this thesis. In this case, the etchant proceeds rapidly in all directions that are perpendicular and parallel to the surface of the wafer until the ≺111≻ planes become exposed, where the etching effectively stops leaving a sloping side wall in the profile with a 54.74° angle [21]. Any rectangular hole oriented on the surface of the wafer in the ≺110≻ direction, will result in a pyramidal-shaped pit when an anisotropic etchant is used (Fig. 1.4(a)). If the silicon is etched long enough, any randomly shaped closed pattern will also result in a rectangular pit as seen in Fig. 1.4(b). The ≺100≻ silicon etch rate for EDP is approximately 1.2μm/min at 110°C, and for 22% TMAH solution it is 1.0μm/min at 90°C.

An important factor in determining the appropriate etchant is its selectivity towards different masking films. For SiO_2 and Si_3N_4 that are widely used as a mask etch the

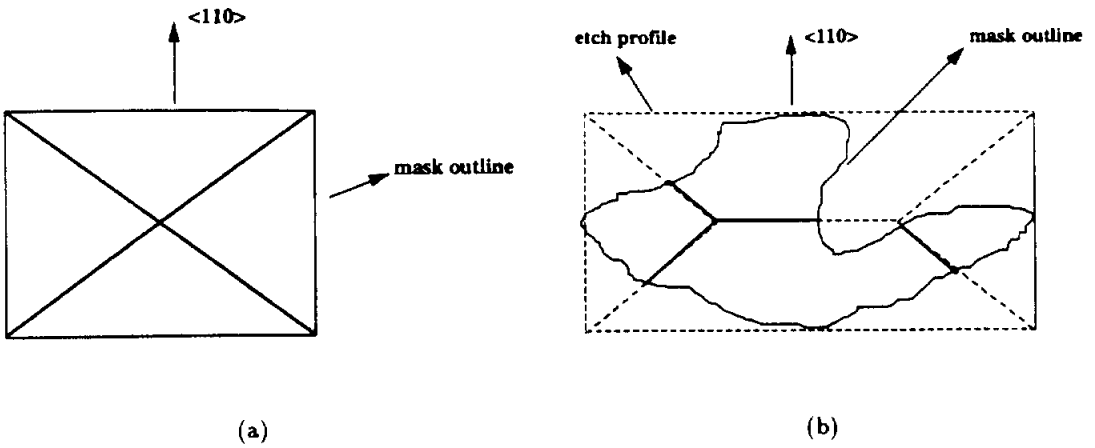


Figure 1.4: Pyramidal pits of a $\prec 100 \succ$ silicon wafer for: a) a rectangular etch mask pattern and b) a random etch mask pattern and long etching time.

corresponding rates can be seen in Table 1.1 [22], [23]. From this table we observe that for long etches Si_3N_4 is preferred for KOH and HF-HNO_3, whereas for EDP and TMAH both dielectric films can be used. In addition, the etch rate for SiO_2 in TMAH is almost four orders of magnitude lower than those of $\prec 100 \succ$ and $\prec 110 \succ$ crystallographic directions, depending on the solution temperature and concentration.

Etchant	SiO_2 (nm/min)	Si_3N_4 (nm/min)
HF-HNO_3	10-30	low
EDP	1-80	low
KOH	1-10	low
TMAH	1	1-10

Table 1.1: Etch rates of different chemicals for SiO_2 and Si_3N_4.

1.3 Schottky Barrier Diode

The Schottky barrier diode has been used in numerous millimeter-wave mixer and multiplier applications since the early 70's. The rectifying or Schottky barrier type junction is formed by placing a metal of higher work function in intimate contact with an n-type semiconductor of lower work function [2]. Platinum, Ti and gold are the most commonly used anode materials for fabricating GaAs diodes [24]; gold and aluminum have also been used, although these materials have poor reliability. The size and shape of the anode are selected to give the appropriate electrical characteristics (junction capacitance and series resistance) for the intended application. The circular anodes of microwave and millimeter-wave diodes vary in diameter from less than 1.5 μm to 20μm. For practical reasons a large number of anodes are defined on the surface of a single chip and are isolated from each other by an oxide or nitride layer or by selective etching (mesa) around each diode. An ohmic contact is also formed on the substrate, and for GaAs alloyed gold- germanium is most commonly used.

In thermal equilibrium, a depletion region forms within the semiconductor at the metal interface that is positively charged, since all of the mobile electrons are absent and only the ionized donor atoms are present. The width, W, of the depletion region assuming a uniform doping N_D can be found by solving Poisson's equation to be [25]:

$$W = \sqrt{\frac{2\epsilon(V_{bi} - V)}{qN_D}} \tag{1.1}$$

where ϵ is the dielectric constant of the semiconductor, N_D is the doping concentration in the n^- layer, q is the electric charge of the electron, V_{bi} is the built-in potential and V is the applied voltage at the anode. The charge ,Q, and capacitance ,C, per unit area can be

evaluated from:

$$Q = qN_D W = \sqrt{2q\epsilon N_D(V_{bi} - V)} \tag{1.2}$$

$$C = \frac{\partial Q}{\partial V} = \sqrt{\frac{q\epsilon N_D}{2(V_{bi} - V)}} = \frac{\epsilon}{W} \tag{1.3}$$

Equation 1.3 can also be written as:

$$C_j = C(V) = \frac{C_{jo}}{\sqrt{1 - \frac{V}{V_{bi}}}} \tag{1.4}$$

where C_{jo} is the zero bias capacitance given by:

$$C_{jo} = \sqrt{\frac{qN_D\epsilon}{2V_{bi}}} \tag{1.5}$$

The relationship linking the current , I, through the diode with the applied voltage ,V, can be found with the help of thermionic emission-diffusion theory [25]:

$$I = I_s(e^{\frac{qV}{nkT}} - 1) \tag{1.6}$$

where

$$I_s = A^*T^2Se^{\frac{-q\Phi_b}{kT}} \tag{1.7}$$

In equations 1.6,1.7 n is the ideality factor of the diode, k is Boltzmann's constant, T is the temperature in Kelvin, Φ_b is the barrier height, S is the junction area and A^* is the effective Richardson constant which is approximately 4.4 $Acm^{-2}K^{-2}$ for a metal-GaAs contact. The ideality factor , n, is an indication of how much the diode deviates from the perfect case (n=1) and is a measure of the quality of the junction. It is used to account

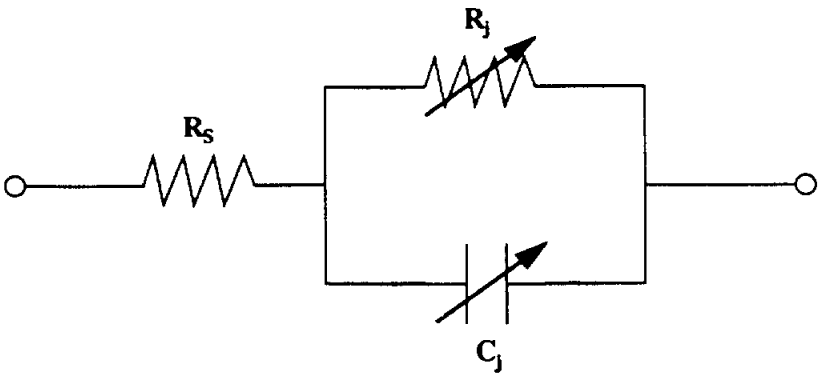


Figure 1.5: Equivalent circuit for the Schottky-barrier diode.

for any type of imperfections in the junction and for phenomena that cannot be explained with the thermionic diffusion theory. Typical values of n range from 1.05 to 1.3.

The equivalent circuit of a Schottky-barrier diode can be seen in Fig. 1.5 [24]. The diode consists of three elements, two of which, the junction capacitance and resistance, are non-linear. The junction resistance R_j accounts for the generation-recombination current, the diffusion current and the surface leakage current. The parasitic series resistance R_s, which is a result of the undepleted high resistivity epitaxial material, is also non-linear but varies slightly both in forward and reverse bias. In mixers and multipliers R_s can be a very significant loss mechanism.

One way to measure R_s is to plot the diode I-V characteristic on semi-log coordinates. If there was no loss in the junction the I-V would follow the straight line, as indicated by equation 1.6. However, because of the loss (i.e. R_s) the I-V characteristic deviates from the ideal line and the difference ΔV between the expected and actual voltage for a particular value of current I yields R_s as follows (see Fig. 1.6):

$$R_s = \frac{\Delta V}{I} \tag{1.8}$$

The capacitance C_j of the diode can be measured with the help of an LCR meter for

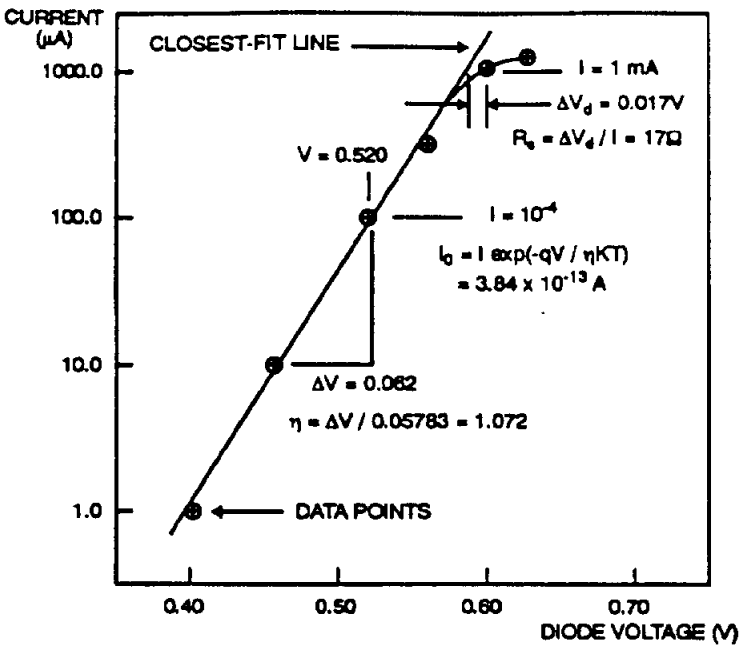


Figure 1.6: I-V characteristic of a Schottky diode on a semi-log plot.

different biasing conditions. Once R_s and C_{jo} are found, a figure of merit for the diode , the cutoff frequency f_c can be evaluated from:

$$f_c = \frac{1}{2\pi R_s C_{jo}} \tag{1.9}$$

Usually, for the calculation of the cutoff frequency the dc quantities of the diode are used, without taking into account high frequency skin-effects and parasitics.

For MMIC applications the planar disk type Schottky diode shown in Fig. 1.7(a) is commonly used (this type of diode was used in the work presented in this dissertation). In this mesa-type diode both contacts (anode and cathode) are on the top surface of the chip and the current through the device flows down from the anode and spreads laterally around the base of the mesa before flowing out of the cathode [14]. Assuming that the current is confined within a skin depth δ, the series resistance can be broken in several components

(Fig. 1.7(b)), and the analytical equations for these componenta are given by the following equations [26], [27]:

$$R_n = \frac{t - W}{\sigma_n \pi a^2} \tag{1.10}$$

$$R_1 = \frac{\delta_s}{2\sigma_s \pi a^2} \tag{1.11}$$

$$R_2 = \frac{1}{4\pi\sigma_s\delta_s} \tag{1.12}$$

$$R_3 = \frac{1}{2\pi\sigma_s\delta_s} ln(\frac{b}{a}) \tag{1.13}$$

$$R_4 = \frac{\rho_m\rho_s}{\rho_m\delta_s + \rho_s\delta_m}[\frac{1}{2\pi} ln(\frac{c}{b}) + \frac{\delta_s}{\rho_s}(AI_o(\beta c) + BK_o(\beta c)) + \frac{\delta_m}{\rho_m}(AI_o(\beta b) + BK_o(\beta b))] \tag{1.14}$$

where

$$A = \frac{1}{2\pi\beta\Delta}[\frac{\rho_m K_1(\beta b)}{\delta_m c} + \frac{\rho_s K_1(\beta c)}{\delta_s b}] \tag{1.15}$$

$$B = \frac{1}{2\pi\beta\Delta}[\frac{\rho_m I_1(\beta b)}{\delta_m c} + \frac{\rho_s I_1(\beta c)}{\delta_s b}] \tag{1.16}$$

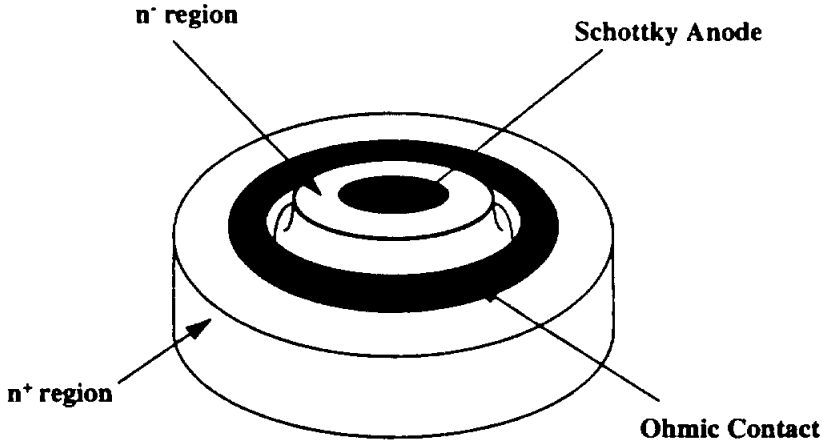
$$\Delta = I_1(\beta c)K_1(\beta b) - I_1(\beta b)K_1(\beta c) \tag{1.17}$$

$$\beta = \sqrt{\frac{1}{\rho_c}(\frac{\rho_m}{\delta_m} + \frac{\rho_s}{\delta_s})} \tag{1.18}$$

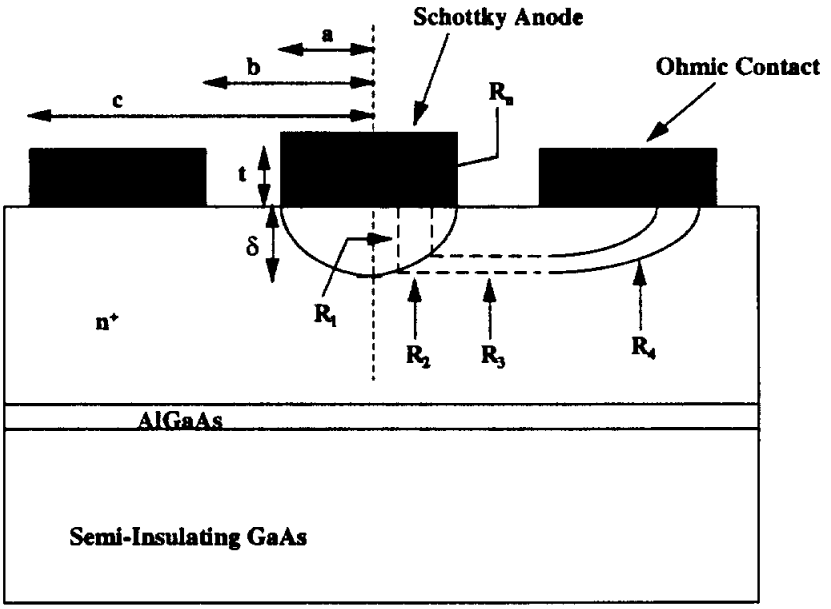
ρ_c is the ohmic contact resistance, δ_s and δ_m are skin depths, ρ_s and ρ_m are resistivities, σ_s and σ_m are conductivities, in the substrate and metal regions, respectively. $I_n()$ and $K_n()$ are modified Bessel functions of the first and second kind, respectively. The total series resistance , therefore, of the disk-type diode of Fig. 1.7(a) is :

$$R_s = R_n + R_1 + R_2 + R_3 + R_4 \tag{1.19}$$

For a W-band (40 to 80 GHz) multiplier diode with a=4.8 μm, b=8.3 μm, c=12.3 μm, an epi-layer thickness of 4000 $\AA$ and a doping of $1x10^{17} cm^{-3}$ $R_s \approx 1.5\Omega$ from equation 1.19,



(a)



(b)

Figure 1.7: a) Disk type diode for MMIC applications and b) cross section of diode showing different components of the series resistance (from [14]).

while for a mixer diode with a=1.1 μm, b=3.1 μm, c=7 μm, an epi-layer thickness of 2000 $\mathring{A}$ and a doping of $3x10^{17} cm^{-3}$ $R_s \approx 6.4\Omega$.

The efficiency of a Schottky-barrier diode that is used as a varactor is expressed as the quality factor , Q, which is the ratio of the energy stored in the junction to the energy dissipated by it [25]:

$$Q = \frac{\omega C_j R_j}{1 + \omega^2 C_j^2 R_j R_s} \approx \frac{1}{\omega C_j R_s} = \frac{X_{in}}{R_{in}} \tag{1.20}$$

1.4 Measurement Techniques

Measurements on monolithic microwave/millimeter-wave circuits are performed using an HP 8510C Vector Network Analyzer (VNA). The analyzer is capable of measuring the S-parameters of various circuits from 2 to 118 GHz,with three different test sets. From 2 to 40 GHz, the 8516A test set is used with coaxial cables having K-connectors at the end. These cables are connected to model 40A probes from GGB Industries that are designed for on-wafer measurements up to 40 GHz. From 40 to 60 GHz, the synthesizer of the VNA drives the 83556A mm-wave source module that uses frequency multipliers (triplers) in order to produce the range of interest. The module is connected to a waveguide system that includes couplers and mixers for sampling the incident/reflected energy and downconverting the measured signals to the 1.2 MHz baseband. At the end of the waveguide system there is a waveguide-to-coax transition that leads to a 1.89 mm connector where the coaxial cable is attached. The other end of the cable is connected to model 67A probes that are used to measure the planar circuit. The measurement is controlled and recorded with the 85105A millimeter wave controller. The same controller is used for W band measurements from 70 to 118 GHz. In this case, the W85104A modules are used to produce the frequencies of interest

from those of the synthesizer with the help of quadruplers. The output of the W band test set modules is a WR-10 adaptor that is connected to a long piece of WR-10 waveguide. The waveguide is followed by model 120A-BT probes that have a WR-10 adaptor and a bias-tee network for biasing active structures (such as multipliers and mixers) during measurements without affecting the RF frequencies. All the different models of probes that were mentioned are compatible with coplanar-waveguide transmission lines and consist of three tips, two for the ground and one for the signal, that launch the CPW mode into the planar passive or active structure. The distance between the center tip and each of the outer tips is called the probe "pitch" and is either 150 or 100 μm (for most of the measurements in this thesis it is 150 μm). The system available for measurements does not cover the range from 60 to 70 GHz and ,therefore, in the graphs presented herein this band will be presented either with a straight line or a gap in the data.

In order to measure the S-parameters of a circuit, the errors introduced by the various components of the network analyzer, the cables/waveguides, the connectors, the adaptors and the probes must be removed. The process of removing these errors is called calibration or de-embedding. The two methods that are widely used for calibrating the VNA are the Short-Open-Load-Thru (SOLT) and the Thru-Reflect-Line (TRL). In the SOLT method the system is calibrated up to the end of the probe tips and, thus, the errors introduced from the probe to planar circuit transition are not accounted for. For a full two port calibration, error correction is achieved by measuring four standards (open, short, 50 Ω load and thru line) with known responses. The model that represents the various mechanisms of error in the system and is used for de-embedding, consists of twelve error coefficients (for a one port calibration three standards are used and three error coefficients are calculated). By measuring four known standards a system of twelve equations with twelve unknowns is

formed and solved. The error coefficients are then loaded into the VNA and calibration is achieved on-line.

In the TRL method, the reference planes for the measurement are inside the planar circuit and the errors from the probe-to-circuit transition as well as the transmission lines before the device under test (DUT) can be de-embedded [28], [29]. The standards that are used in this method are fabricated on the same wafer with the DUT and consist of a thru line, one or several delay lines and a short or open. With appropriate selection of the standard dimensions, the designer has the flexibility to define the reference planes anywhere in the circuit before the DUT of interest. The length of the thru line is twice the distance between the point where the probe tips touch the circuit and the reference plane. Usually, the length of the thru line is equal to a wavelength at a particular frequency of interest but any arbitrary length can also be chosen. The length of the reflect standard is half the length of the thru line and depending on the type of line a short or an open is used. For a microstrip configuration an open is much easier to fabricate since a short would require a via hole, while for a CPW configuration a short is usually preferred.

For the delay lines, the lengths are $\lambda/4$ longer than that of the thru line at various frequencies. These frequencies are determined by the user to ensure a good calibration over the entire band of interest. The delay lines allow the network analyzer to compute calibration coefficients so that the proper phase response of the DUT can be found. For this reason, a delay line is "good" as long as $0.5 \leq \mid sin(\beta l) \mid \leq 1$,where l is the excess length of the delay line, over the frequency range of interest. If the previous relationship is not true for the entire band, then several delay lines that meet the previous criterion must be designed in a way that they overlap and cover all the range. Each delay line will therefore be effective in a sub-region of the entire frequency band. The best phase correction results

are possible when βl is closer to 90° or 270°. One restriction of the TRL method stems from the maximum length of the delay lines that must fit in the available wafer area. If multiple columns of calibration standards are needed on the wafer, then the length of the lines should be designed to account for the amount of space available. The resonance frequency may have to be altered in order to obtain shorter delay lines, if they are too long for multiple columns.

The National Institute of Standards and Technology (NIST) has developed a program called *Multical* [30],[31], that performs a TRL calibration of the HP8510C VNA on line and runs under HTBasic in a Windows 3.11 environment. This program makes the TRL calibration faster and more convenient. Rather than defining standards on the HP8510C VNA, the standards are quickly defined on screen by editing a calibration menu and corrections or alterations can be made rather easily. *Multical* is capable of calculating the error coefficients and loading them in the HP8510C VNA so that the user can measure the S-parameters of the SUT directly. Besides the scattering parameters, Multical can plot and analyze various data such as propagation constant, attenuation, effective permittivity, characteristic impedance and capacitance of a line.

1.5 Simulation Tools

Monolithic microwave/millimeter-wave integrated circuits are designed and analyzed with the help of commercially available or built-in house software. Presently, there is an abundance of computer programs that can solve both passive and active structure related problems. It is up to the designer to select the software that is most suitable for the geometry under investigation, in terms of accuracy in results, minimum running time and memory size. For the structures that will be presented in this thesis, the available programs

are based on two methods : a) the quasi-static analysis and b) the full wave analysis.

In the first method, the quasi-static, the electromagnetic problem is solved with the help of ideal transmission line theory without taking into account any parasitic or secondary effects. The best known program based on this method is *HP EEsof Libra* [32] developed by Hewlett-Packard. Libra implements circuit models for each different section of the DUT (transmission line, capacitor, resistor, inductor, diode, transistor) as well as measurement data provided by the user for a specific component of the structure, in order to calculate scattering parameters or any other functions. It can also incorporate ohmic and dielectric loss, based on simple models, for more accurate simulations. For active structures, such as frequency multipliers and mixers, *Libra* can perform a harmonic balance analysis yielding conversion loss, embedding impedances, return loss and output power spectrum. An optimizer can also be used to match modeled data to either measured data or results obtained from a full wave analysis.

In the second method, the full wave technique, Maxwell's equations are solved and all components of the electric and magnetic field are evaluated. With this approach all effects of the electromagnetic structure are taken into account. The solution to Maxwell's equations is achieved with the implementation of several numerical techniques. Finite Difference Time Domain (FDTD) is one of these techniques, where Maxwell's differential equations are replaced by finite difference equations that are algebraic in form [33]. The value of a dependent variable at a point in the solution region is related to the values of some neighboring points. Therefore, a grid or mesh of points that are related to each other is created and boundary conditions are applied to the points on the outer surfaces or edges of the grid. The most famous scheme in FDTD is Yee's cell [34] that relates the electric and magnetic field components in a cubic cell. For an unbounded or radiating structure an

appropriate absorber that simulates free space must be used so that the grid is truncated and finite. One of the advantages of FDTD is that it can be applied to non-planar geometries, such as micromachined micromave and millimeter-wave structures.

Another numerical technique that is used for the solution of electromagnetic problems is the method of moments. This method is more appropriate for unbounded or radiating structures and is based on converting an integral equation into a matrix equation using basis functions or weighting functions. Once the matrix elements are found, the equation is solved and the parameters of interest are calculated. Two popular programs that implement the method of moments for MMIC's are *IE3D* and *Sonnet* [35],[36]. For a planar circuit, the geometry is first entered in both of these programs with the help of a geometrical editor and then a grid is created by dividing the conducting areas into cells. In each cell, the electric currents are the unknowns that are found from the solution of the appropriate matrix equation. From the currents the electric and magnetic fields as well as the scattering parameters are derived. For more complex geometries and inhomogeneous media the Finite Element Method (FEM) is used, where the solution region is divided into a finite number of subregions or elements. In each element the equation of interest is first derived and then all of the elements are assembled together into a system that is solved. A commercial program that makes use of FEM for solving various electromagnetic structures is *HFSS* by HP-EESOF [37]. *HFSS* has the capability of solving both planar and non-planar (e.g. micromachined) MMIC structures.

1.6 Dissertation overview

Several passive and active MMIC structures are presented in this dissertation, with the objective of showing that a transmit/receive system with enhanced performance at high

operating frequencies can be monolithically integrated on a single chip. The design of the circuits was realized by using software tools and by creating microwave models, while the fabrication was done with standard IC fabrication techniques and the electrical performance was tested with various equipment. The dissertation is organized into two main sections; the presentation of passive monolithic circuits on silicon and the presentation of active monolithic circuits on GaAs. It comprises of 6 chapters and three appendices.

Chapter 2 deals with micromachined patch antennas on high-index materials. Two techniques that enhance the antenna performance are implemented. In the first technique that was developed by R.F. Drayton [38] an air-cavity is created under the patch by removing material. Efficiency measurements for antennas fabricated on Duroid substrate, according to this method, that resonate in Ku-band are performed to validate the technique. Results show an increase of 28% for a 75%-25% air-dielectric substrate region when compared to a regular high index patch. The dependence of the efficiency improvement on the cavity placement relative to the patch radiating edges is also investigated. It is shown that in order to improve the antenna performance a minimum distance equal to two times the substrate thickness is required between the cavity and radiating edges. Return loss measurements and radiation patterns for the fabricated antennas are also demonstrated. An increase of 64% in the micromachined antenna bandwidth is observed, as well as smooth E-plane patterns. In the second technique the dimensions of the rectangular antenna are adjusted so that the dominant TM_0 mode is suppressed and simulated results with FDTD are presented. The aim of this effort is to show that integration of planar radiating elements on high dielectric constant substrates with optimal performance is feasible, thus allowing for high circuit density and compact designs.

Chapter 3 presents the implementation of micromachining for high-Q resonators. A fully

monolithically integrated cavity resonator with very low loss and narrow bandwidth that surpasses the performance of traditional planar resonators is fabricated and tested. Design considerations for the resonator can be found in [1]. Measured results show a quality factor of 506, a bandwidth of 5% and an insertion loss of 0.36 dB. The measurements are compared with simulations done by Jui-Ching Cheng [1], based on a hybrid FEM/MoM technique that he developed. In addition, the performance of the resonator under different ambient temperatures is presented and analyzed. The dependence of the resonator response on the location of the coupling slots relative to the center of the cavity is also demonstrated, along with some on-wafer packaging schemes. This resonator can be used as a building block for the fabrication of narrow-band low-loss filters necessary in various communication systems.

Chapter 4 presents GaAs monolithic frequency multipliers based on FGC line technology for W band. This type of multiplier was first demonstrated by Brauchler [2] and for a Q=2 design an efficiency of 15-16% at 80 GHz and a wide bandwidth (12%) were achieved. Designs for higher efficiency and output power are pursued here. The characteristics of FGC lines with and without a polyimide overlay used for passivation are given first and then results from different line geometries and impedances are compared. The dependence of the line loss on its geometry rather than the substrate material is shown. A two-diode Q=2 doubler with different anode areas than [2] is designed with 17.2% efficiency, 10% bandwidth and 66 mW output power at 76.3 GHz. A Q=3 doubler is also designed and fabricated and results show an efficiency of 22%, a bandwidth of 8.5% and 50 mW output power. A W-band doubler with four diodes, 12.5% efficiency and 115 mW maximum output power, which is the highest in that band, is also presented. In addition, a method that increases the multiplier efficiency by changing the topology of the FGC passive circuit is described and measured results that exhibit 20-25% performance improvement are shown.

Chapter 5 presents a monolithic FGC W-band x2 subharmonic mixer on GaAs that will be part of a fully monolithic transmit/receive module, as well as a novel fabrication technique that allows the fabrication of both FGC based multipliers and mixers with air-bridges for the passive circuits and channel etched fingers for the diodes on the same substrate. A single-sideband conversion loss of 11 dB is achieved at 79 GHz for an IF frequency of 4 GHz, an LO power of 8.8 dBm and epi-layer parameters that are a compromise between the optimum doubler and mixer ones. Chapter 6 summarizes the work presented in the dissertation with conclusions and recommendations for future work. Appendix A revisits the fundamentals of the first technique used in chapter 2 for the performance enhancement of patch antennas, while appendices B and C describe the various fabrication steps that were followed for the realization of monolithic multipliers and mixers.

CHAPTER 2

MICROMACHINED PATCH ANTENNAS

2.1 Introduction

The first component of the monolithic transmit/receive module that will be studied is the radiating structure. For a planar environment the microstrip antenna has been widely used and implemented in a broad range of applications from communication systems (radars, telemetry and navigation) to biomedical systems, primarily due to its simplicity, conformability, low manufacturing cost [39], and enormous availability of design and analysis software. Integration, however, of the microstrip antenna in a compact circuit design, such as the monolithic transmit/receive module, that is typically achieved in a high index material is in direct contrast to the low index substrates needed by antenna performance requirements. The ideal solution requires the capability to integrate the planar antenna on electrically thick low index regions while the circuitry remains on the high index regions in the same substrate. In the past, this requirement was satisfied by selecting the substrate that offers optimum component performance; unfortunately this led to hybrid integration schemes and high development cost. As the frequency increases, however, this approach becomes increasingly difficult and costs are prohibitively high.

Microstrip antenna designs show significantly degraded performance in high index materials, such as silicon and GaAs, used for monolithic architectures due to the pronounced excitation of surface waves in these substrates. As a result, the antenna has lower efficiency, reduced bandwidth, degraded radiation patterns and undesired coupling between the various elements in array configurations. Optimum antenna performance depends on the choice of dielectric material as well as the choice of feeding network and is achieved when the radiated power occurs primarily as space waves with little or no components of "undesired" surface waves. Such microstrip designs are typically fabricated on electrically thick, low index materials and characterized by maximum antenna bandwidth and efficiency as reported by a vast number of theoretical and experimental researchers.

Only a few experimental approaches have been put forth to resolve the excitation of substrate modes in microstrip antennas. In 1984, a substrate-superstrate configuration [40] using a horizontal antenna element showed an increase in the radiation efficiency. Superstrate materials such as GaAs or Si, however, require a very thin substrate thickness that yields exceedingly small values of radiation resistance. In the past three years, researchers have begun to use physical substrate alterations as a means of perturbing the surface wave excitation. Circular patch designs in duroid [41] are based on the choice of an appropriate patch radius to suppress the excited surface waves. Given the patch radius for a desired operation frequency, the antenna is forced to resonate at the first higher order mode (TM_{120}) rather than the dominant (TM_{110}) one. Other approaches rely on suspending the rectangular patch over an air cavity through the use of a membrane or over closely spaced periodic holes in the substrate (either drilled or micromachined) [10], [42], [11].

This chapter presents two different techniques based on the implementation of micromachining technology, that address the previously mentioned problems of patch antennas

on high-index substrates. In the first technique developed by R.F. Drayton [38], material is removed laterally in a region under and around the patch antenna in an effort to locally reduce the dielectric constant. Experimental results for Ku-band antennas fabricated on Duroid substrate show a significant increase in antenna efficiency and smoother radiation patterns, when compared with a regular rectangular patch. A minimum distance equal to two times the substrate thickness between the radiating edges of the patch and the edges of the machined area is also required in order to enhance the antenna performance. In the second technique, the resonant length of the patch is adjusted in order to minimize the dominant TM_0 surface wave mode [43]. Because the dimensions required to suppress the surface wave are larger than the dimensions for the desired frequency of operation, dielectric material is removed in an area only under the patch. Simulation results with FDTD show a significant decrease in the excited surface waves between the micromachined antenna and the regular one.

2.2 Reduction of the Effective Dielectric Constant (Technique I)

2.2.1 Review of Technique

To integrate patch antennas into circuit designs on high index substrates without losing the advantages of low index materials, the regions in the substrate which will house the radiating elements must have low index of refraction. This is achieved by using micromachining to eliminate a portion of the substrate material as can be seen in Fig. 2.1. The micromachined antenna configuration that was developed by R.F. Drayton consists of a rectangular patch centered over the cavity, sized according to the effective index of the

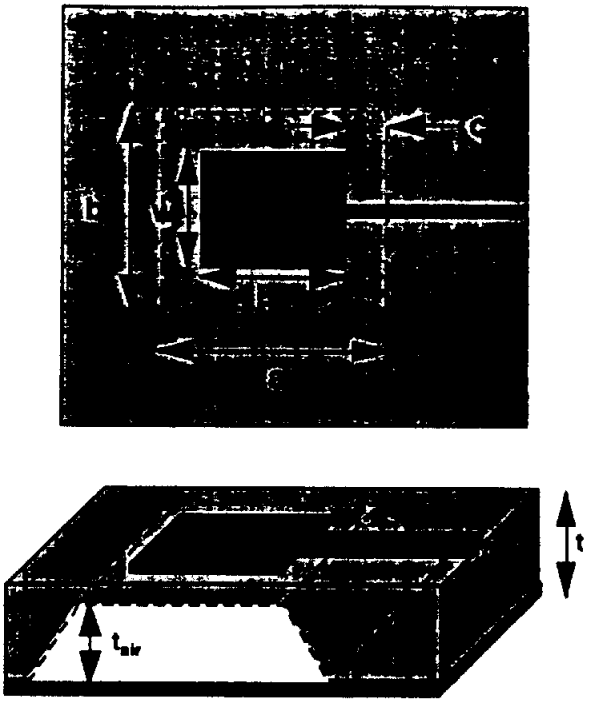


Figure 2.1: Geometry of the micromachined patch antenna.

cavity region and fed by a microstrip line. To produce the mixed substrate region, silicon micromachining is used to laterally remove the material from underneath the specified cavity region resulting in two separate dielectric regions of air and silicon [38]. In order to predict the effective dielectric constant of the mixed air-silicon region for varying thickness ratios underneath the antenna, a quasi-static model based on series capacitors is used [38]. A detailed description of this model along with results can be found in Appendix A.

From Fig. A.3 of Appendix A we observe that an effective dielectric constant of approximately 2.2 is achieved for a mixed air-silicon ratio of 1:1 (model with $\Delta L=0$) or 3:1 (model with ΔL calculated from [44]). Based on these results , two antennas (one micromachined and one regular) with resonant frequencies in the K-band were fabricated on Silicon by R.F. Drayton [38]. Preliminary measurements of the return loss indicated an increase in the bandwidth of the micromachined patch when compared with the regular patch. In addition, radiation pattern measurements showed a much smoother E-plane pattern for the

micromachined antenna (for more details see Appendix A). Both of these measurements provide the first indicator of a potential increase in total radiation from the antenna. Efficiency measurements, however, need to be made in order to observe the increase in power radiated into space waves as opposed to power radiated into surface waves. Since the existing test equipment operated at a lower frequency, a scaled model of the antenna on Silicon was fabricated on a mixed air-substrate cavity and was realized by machining a high-index (10.8) duroid substrate. For comparison purposes, conventional patch designs on both high and low index materials were also fabricated.

In the following sections, the theory of radiation efficiency is described first and then the antenna performance is characterized based on bandwidth, radiation pattern and efficicency measurements.

2.2.2 Theory of Radiation Efficiency

In order to measure the radiation efficiency of the patch antenna a radiometric method was used [45], [46]. This method is based on the fact that a lossy antenna under test (AUT) pointed at a cold load/target will generate more noise power than a less lossy antenna pointed at the same target. Antenna efficiency is obtained by characterizing the system receiver first and then the composite system (system receiver plus antenna). The output powers P_L^H and P_L^C measured at the receiver when connected to a hot and cold 50 Ω load, respectively, are given by [47]

$$P_L^H = KT_{HL}BG_r + P_r \tag{2.1}$$

$$P_L^C = KT_{CL}BG_r + P_r \tag{2.2}$$

where K is Boltzmann's constant, G_r is the receiver gain, B is the effective bandwidth of the receiver and T_{HL}=295 K, T_{CL}=77 K are the hot and cold load temperatures, respectively. The ratio of the two powers can be defined as

$$Y_r = \frac{P_L^H}{P_L^C} = \frac{KT_{HL}BG_r + P_r}{KT_{CL}BG_r + P_r} \tag{2.3}$$

If we divide both the numerator and denominator of equation 2.3 with KT_oBG_r and we recall that [47]

$$\frac{P_r}{KT_oBG_r} = F_r - 1 \tag{2.4}$$

where F_r is the noise factor of the receiver system and T_o=295 K, then by solving for F_r equations 2.3, 2.4 yield

$$F_r = \frac{T_{HL} - Y_rT_{CL} + T_o(Y_r - 1)}{T_o(Y_r - 1)} \tag{2.5}$$

Since $T_o = T_{HL}$=295 K equation 2.5 gives

$$F_r = \frac{(T_{HL} - T_{CL})}{T_{HL}(1 - 1/Y_r)} \tag{2.6}$$

Individual AUTs are measured in the composite system to obtain hot and cold measurements where the black body absorber (Ecosorb), placed in front of the antenna element in a way that covers all of its radiation pattern, has been held at room temperature (T_{HA}= 295 K) for the hot load and has been immersed in liquid nitrogen (T_{CA}= 77 K) for the cold load. Note that the 50 Ω calibration load is submersed into the liquid nitrogen. The resulting composite system noise factor is expressed as

$$F_C = \frac{(T_{HA} - T_{CA})}{T_{HA}(1 - 1/Y_C)} \tag{2.7}$$

where the measured power ratio of the antenna, Y_c, is P_A^H/P_A^C. Since the measured output noise powers of the receiver and the composite system with the hot load are known, the antenna gain can be obtained from the following expressions

$$P_L^H = KT_{HL}BG_rF_r \tag{2.8}$$

$$P_A^H = KT_{HA}BG_rG_AF_C \tag{2.9}$$

where G_r and G_A are the receiver and antenna gain, respectively. After dividing the two hot load power equations [2.9 by 2.8] and substituting in the noise factor parameters, F_r (equation 2.6) and F_C (equation 2.7), the antenna gain expression becomes

$$G_A = \frac{P_A^H - P_A^C}{P_L^H - P_L^C} \tag{2.10}$$

Equation 2.10 assumes equal temperatures for the 50 Ω load and AUT in either the hot ($T_{HL} = T_{HA}$=295 K) or cold ($T_{CL} = T_{CA}$=77 K) load measurement.

A modified gain expression is shown in 2.11 that accounts for temperature differences observed in the application of the test methodology in the measurement of the cold 50Ω load and AUT. Since the absorber is immersed into liquid nitrogen and then removed to cover the antenna, the cold temperature is slightly elevated and is assumed to be T_{CA}=88 K based on past experience with this measurement [48], while the 50 Ω load, submersed continuously into the liquid nitrogen, maintains a constant temperature, T_{CL}, of 77 K. Hence,

$$G_A = 1.038 \frac{P_A^H - P_A^C}{P_L^H - P_L^C} \tag{2.11}$$

2.2.3 Ku-Band Micromachined Patch Antenna

Since the available measurement set-up imposes an operating frequency range between 12.5 and 13.5 GHz, several rectangular patch designs were fabricated on duroid substrates of high (10.8) and low (2.2) index constants with substrate thickness, t, of 635 and 500 μm, respectively. Scaled model micromachined antennas were also fabricated in which the cavity is created by machine milling. The final geometry is similar to those shown in Fig. 2.1 without the sloping sidewalls, and the dimensions for the various antennas can be found in Table 2.1, where the parameters a and b are given by their actual values and not the average ones since the sidewalls are vertical. To describe the findings of the various patch configurations investigated, the notation used in the following sections refers to antennas on full thickness substrates as "regular" high- (10.8) or low- (2.2) index designs and those printed on a mixed air-duroid cavity as scaled models. Each patch is fed by a 50Ω microstrip feedline, is fabricated on a 75 mm^2 substrate, and is mounted in the test fixture shown in Fig. 2.2. Since the micromachined scaled model antenna resides over the mixed dielectric material, approximately 3.65 mm of the feed line has an impedance based on the mixed air-duroid region compared to the feedline of regular antennas on full thickness material. The width of the feeding line (560 μm) for the scaled model patch is maintained over the mixed region and is the same with the width of the 50 Ω line on full substrate resulting in a characteristic impedance of approximately 96 Ω.

The return loss is measured (Fig. 2.3) and the input impedance values referenced at the RF connector are shown in Table 2.2; notice the good agreement between the scaled

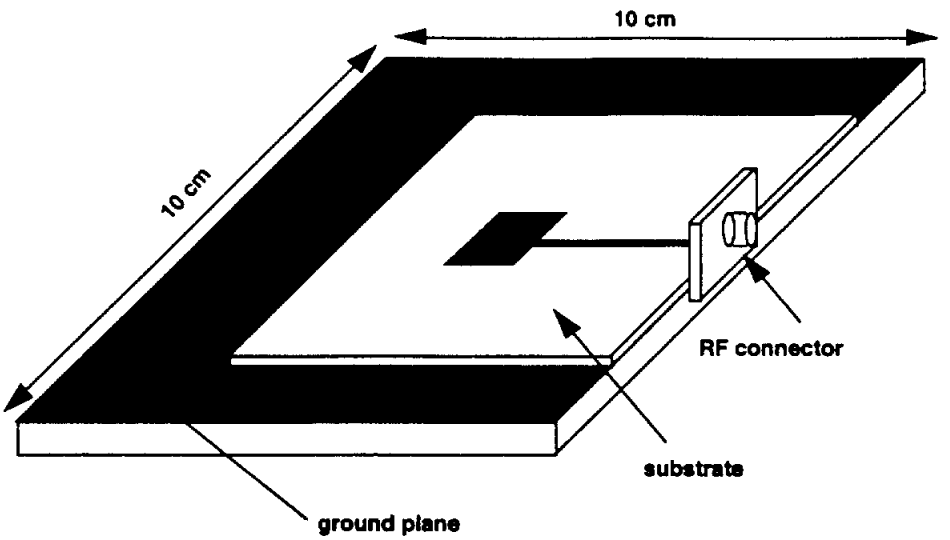


Figure 2.2: Text fixture with micromachined antenna mounted.

model and regular low index antenna. In Fig. 2.3 the bandwidth of the scaled model increases from 1.4% to 2.3%, a 100% increase over the -10 dB bandwidth of the regular patch printed on the high index material. Since bandwidth is inversely proportional to the quality factor, Q,defined as the ratio of total energy stored in the antenna to the energy dissipated or radiated from the antenna, the increase in bandwidth provides the first indicator of an increase in total radiation (space and surface waves) from the patch. This increase in bandwidth was also observed in the silicon micromachined antenna. It should be noted here that the return loss measurement of the micromachined patch exhibits a second resonance around 12.4 GHz, that is due to the presence of a low permittivity cavity inside a high dielectric constant area.

Radiation patterns (Fig. 2.4) were also taken for the three antennas and in order to minimize the interaction between the connector and the antenna during the measurements, a small piece of absorber is placed over the RF connector to reduce the effects of secondary reflections on the antenna pattern. In Fig. 2.4(a) the "regular" high index pattern has a large peak in the E-plane at approximately -50^{o} degrees, indicating large power leakage

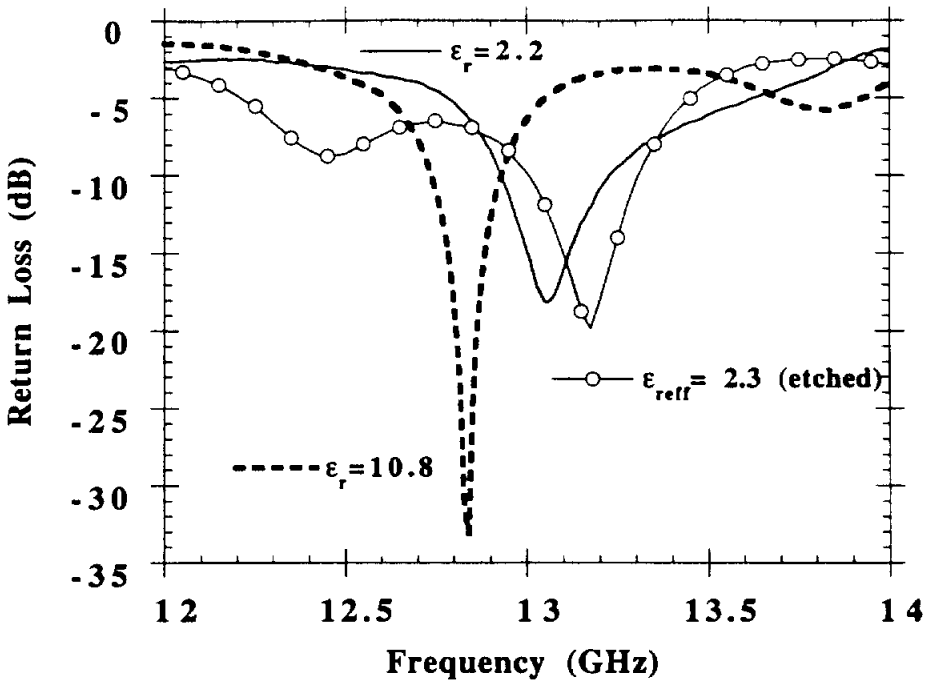


Figure 2.3: Measured return loss for the scaled model patch antenna ϵ_{reff}=2.3 (etched) and regular patch antennas ϵ_r=2.2 and ϵ_r=10.8.

Patch	t(mm)	t_{air}(mm)	L(mm)	w(mm)	a(mm)	b(mm)	c(mm)
Regular (10.8)	0.635	0	3.750	4.420	0	0	0
Scaled Model (10.8)	0.635	0.476 (75%)	7.624	6.676	15.190	14.478	3.783
Regular (2.2)	0.500	0	7.570	7.340	0	0	0

Table 2.1: Dimensions of the fabricated scaled model and regular antennas.

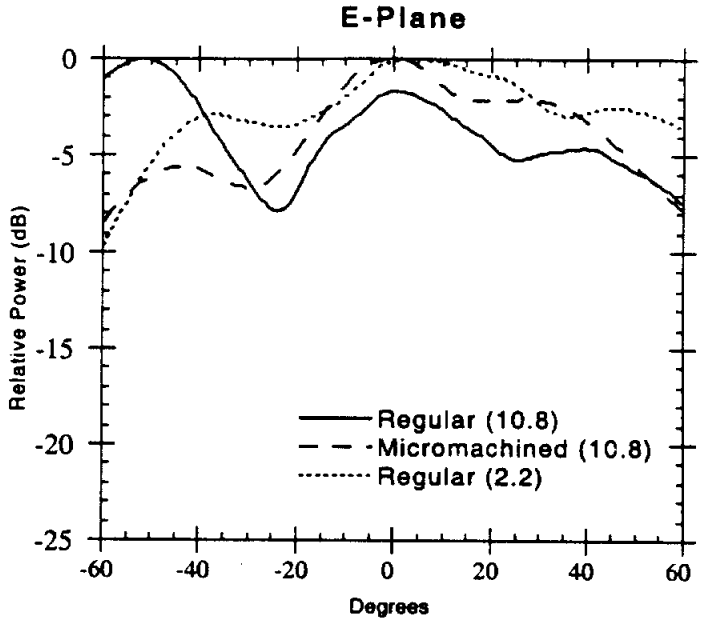
Patch	Input Impedance (Ω)	Resonant Frequency (GHz)	Feed Line Length (mm)
Regular (10.8)	49.2-j0.37	12.84	27.6
Scaled Model (10.8)	67.5-j1.04	13.165	27
Regular (2.2)	67.5-j0.14	13.044	34

Table 2.2: Input impedance characteristics of the regular and scaled model antennas

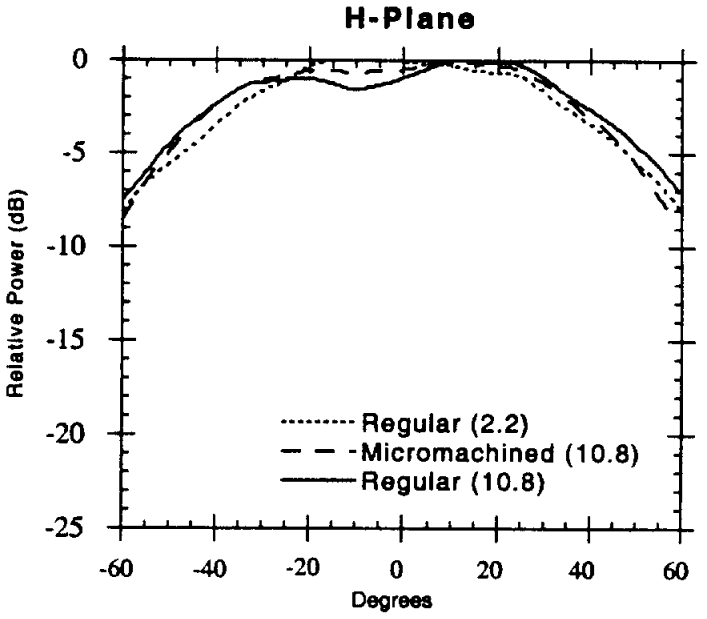
to surface waves. This behavior is also observed in [10]. In contrast, the scaled model patch has a much smoother E-plane pattern and is very similar to the E-plane pattern of the "regular" low index antenna. As expected, the H-plane patterns (Fig. 2.4(b)) are similar in all cases. The differences between the E-plane pattern of the antenna on high-index duroid (Fig. 2.4(a)) and the E-plane pattern of the antenna on Silicon (Fig. A.5(a)) (both antennas are "regular") can be attributed to the slightly different dielectric constant, the different experimental set-up used for the pattern measurements and the fact that the distance between the antenna and the edge of the finite ground plane is not the same in terms of guided wavelengths.

2.2.4 Efficiency Measurements

The system configuration [11] is illustrated in Fig. 2.5 and has component specifications consisting of an RF bandpass filter with an insertion loss of 3 dB in the 12.5 to 13.5 GHz range and a mixer intermediate frequency (IF) of 1.5 GHz. Since the calibration plane of the system is at the RF connector, the measured efficiency values include the feed line, connector and mismatch losses. In order to determine the de-embedded antenna efficiency, the losses must be determined and extracted. The losses associated with the feed line



(a)



(b)

Figure 2.4: (a) E-plane and (b) H-plane radiation patterns for the three antennas under test.

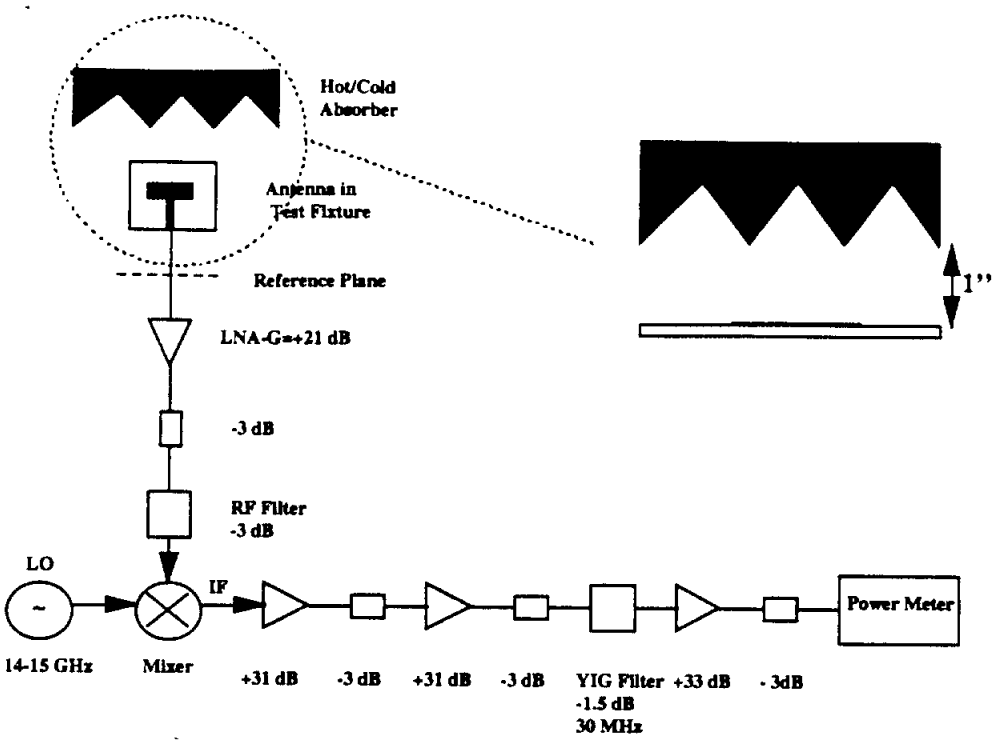


Figure 2.5: System diagram of the efficiency measurement setup.

lengths (Table 2.2) are calculated using HP Momentum [11], [32]; the RF connector loss is based on an empirical value; and the mismatch loss is determined from the measured return loss data.

In Fig. 2.6, the measured efficiency data, which are averaged values, show 73±3% for the scaled model having an air-substrate thickness ratio of 3:1 and 56±3% for the "regular" antenna printed on the high index material. The patch printed on 2.2 duroid was found to have an efficiency of 76±3%. It should be noted here, that during the efficiency measurements the absorber that covered the radiation pattern of the patch antennas was placed at least one inch (2.54 cm) above the antenna plane in order to avoid perturbing the near field. Based on the far-field approximation formula ($r_{ff} \geq 2D^2/\lambda$, where D is the maximum antenna dimension) for the patches with the dimensions of Table 2.1 $r_{ff} \geq 1cm$. In Table 2.3, a summary of the measured efficiency, specific losses, and de-embedded

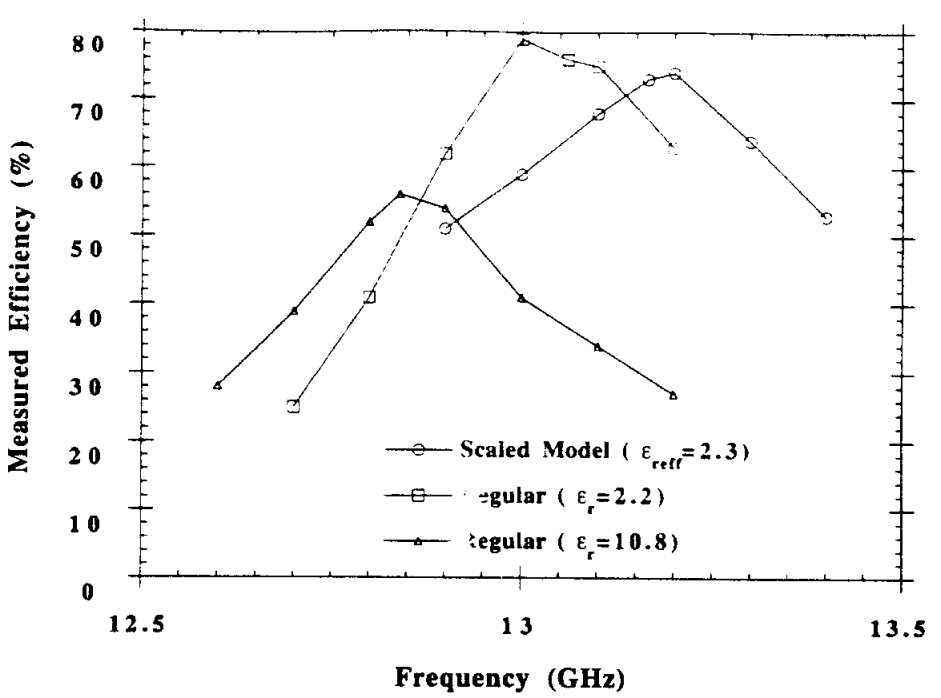


Figure 2.6: Measured efficiency for the scaled model and regular patch antenna designs.

efficiency are documented. The scaled model case shows sensitivity to the distance c between the radiating edges of the antenna and the edges of the micromachined cavity. From the results summarized in Table 2.4, it can be observed that for an air-substrate thickness ratio of 1:1 and separation c=0, the efficiency of the scaled model is similar to that of a patch on high index substrate. However, when the distance is at least twice the substrate thickness, 2t, for the same air-substrate thickness ratio, the de-embedded efficiency increases by about 10%. This is further validated in the measured data shown in Table 2.3 for a distance of c=3.783mm (6 times the substrate height, 6t). The improvements observed are attributed to the presence of fringing fields that usually extend one to two times the thickness t beyond the radiating edges of the antenna into the substrate environment. The above results emphasize the importance of the air-substrate thickness ratio on bandwidth, and also the importance of the distance between the radiating edge of the antenna and the micromachined cavity in order to enhance the antenna's efficiency. A plot of the measured efficiency versus the ratio

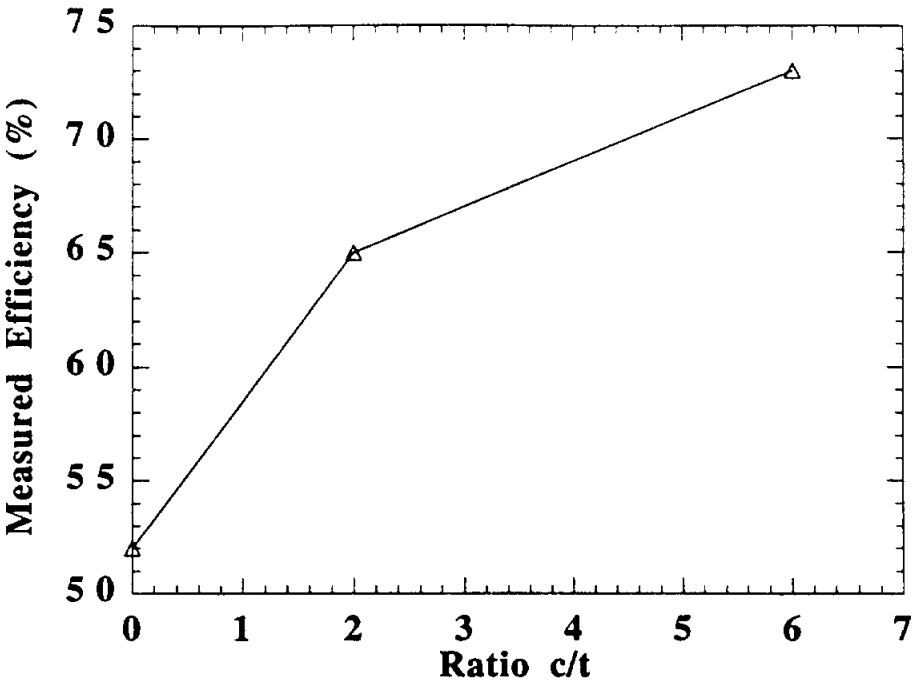


Figure 2.7: Measured efficiency versus the ratio of the distance c over the substrate thickness t.

of the distance, c, between the cavity and the radiating edges over the substrate thickness, t, can be seen in Fig. 2.7.

The de-embedded efficiencies of the individual antenna elements (see Table 2.3) are 85% for the micromachined scaled model and 66% and 82% for the antennas on 10.8 and 2.2 duroid substrate, respectively. The latter values are in good agreement with the calculated efficiencies of 86% and 67% for the regular low and high-index antennas, that can be found in [11]. As a result, the efficiency of the micromachined patch increases by 28% over the high index patch and the efficiency performance approaches the patch on low index duroid within the bounds of measurement error. When the modified efficiency expression (Eq. 2.11) is used to account for differences in the cold measurement of the 50 Ω load and AUT, the measured and de-embedded efficiencies increase by 2-3% as seen in Table 2.3. In this case, no significant difference is observed between either approach since the accuracy of the measurement system is 3%.

Antenna	Regular ϵ_r=10.8	Scaled Model ϵ_r=10.8	Regular ϵ_r=2.2
Measured Efficiency			
Based on Eq. (8)	56%	73%	76%
Based on Eq. (9)	58%	76%	79%
Mismatch loss (dB)	0 (100%)	0.05 (99%)	0.08 (98%)
Connector loss (dB)	0.15 (97%)	0.15 (97%)	0.15 (97%)
Feed line loss (dB)	0.56 (88%)	0.48 (90%)	0.1 (98%)
Total loss (dB)	0.71 (85%)	0.68 (86%)	0.33 (93%)
De-embedded Efficiency			
Based on Eq. (8)	66%	85%	82%
Based on Eq. (9)	68%	88%	85%

Table 2.3: De-embedded efficiency for the scaled model and regular patch antennas at resonance

Patch Antenna	Mixed air-substrate thickness ratio (1:1) c=0	Mixed air-substrate thickness ratio (1:1) c≈2t
t (mm)	0.635	0.635
t_{air} (mm)	0.330	0.330
L (mm)	5.415	7.624
w (mm)	6.676	6.676
a (mm)	5.415	10
b (mm)	10.590	14
Measured efficiency	52%	65%
Total loss (dB)	0.69 (85%)	0.69 (85%)
De-embedded efficiency	61%	76%

Table 2.4: Efficiency results and dimensions for two scaled model antennas on duroid substrate with ϵ_r=10.8

2.3 Elimination of TM_0 Surface Wave (Technique II)

2.3.1 Theoretical Analysis

Our purpose is to design a rectangular patch antenna with a suppressed TM_o surface wave mode. In our analysis we assume that the operating frequency of the antenna and the substrate thickness are such that the higher order surface mode is not excited. Thus, elimination or suppression of the fundamental mode should be sufficient in order to minimize the surface wave losses. According to the equivalence principle and the cavity model for a patch, in terms of radiation a rectangular microstrip antenna can be modeled as a rectangular loop of magnetic current. From the cavity model, the electric field of the dominant TM_{10} mode for the geometry shown in Fig. 2.8 is given by

$$E_z = A\cos_{(}\frac{\pi y}{b}) \tag{2.12}$$

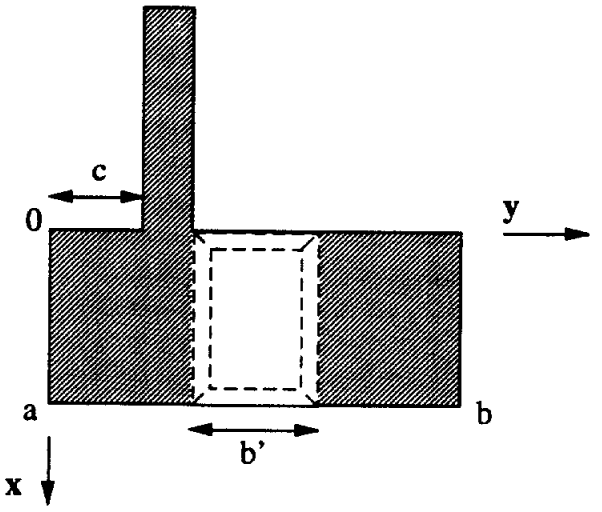


Figure 2.8: Micromachined antenna for the elimination of TM_0 mode.

where a,b are the width and the resonant length of the patch, respectively. Here the assumption is made that the patch is fed in such a way that only the TM_{10} mode is excited. Thus, the radiating edges will be at y=0,b. The equivalent magnetic current at these two

edges is

$$\vec{M} = 2\vec{E} \times \vec{n} = 2A\vec{x} \tag{2.13}$$

As it is known, a single Hertzian magnetic dipole, oriented in the x direction at a height z' above the ground, will give rise to a TM_o surface wave field given by [41]

$$\Psi = K(z, z')H_1^{(2)}(\beta_{TM_0}\rho)\sin(\phi) \tag{2.14}$$

where β_{TM_0} is the propagation constant of the TM_o mode and $K(z, z')$ is an amplitude factor that depends on the height of the source and the observation point. By integrating over the two radiating edges of the rectangular patch for the magnetic current distribution, the total surface wave field radiated by the magnetic currents takes the form

$$\Psi = -4A\frac{B(z)}{\beta_{TM_0}}H_1^{(2)}(\beta_{TM_0}\rho)\tan(\phi)\cos(\beta_{TM_0}\frac{b}{2}\sin(\phi))\sin(\beta_{TM_0}\frac{a}{2}\cos(\phi)) \tag{2.15}$$

where

$$B(z) = \int_0^h K(z, z')dz' \tag{2.16}$$

In order to derive the above expression the far field approximation for the phase of the radiated surface wave is used. The pattern of equation 2.15 is shown in Fig. 2.9 (dashed line). By setting $b = \frac{\pi}{\beta_{TM_0}}$ nulls are placed at the location of the peaks of the lobes at $\phi = \frac{\pi}{2}, \frac{3\pi}{2}$ so that four minor lobes replace the two major lobes (Fig. 2.9- solid line). As a result, the surface wave pattern is reduced.

Choosing b according to the above formula, results in greater resonant length than the one chosen for the design frequency. In order to overcome this decrease in operating

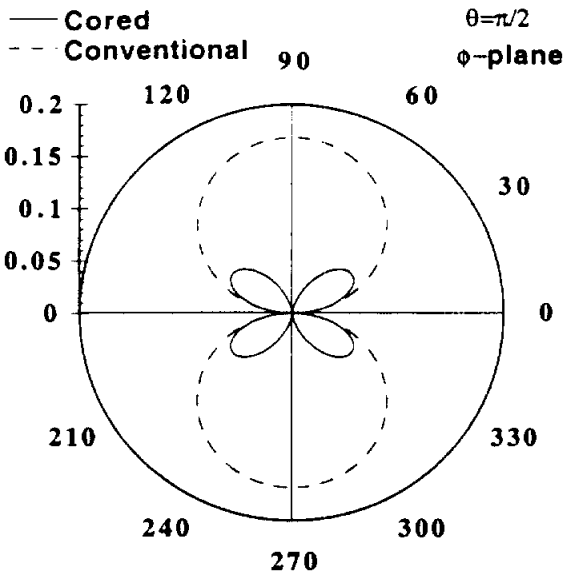


Figure 2.9: Surface wave field pattern for the regular antenna and the micromachined antenna.

frequency, the material in a rectangular region under the patch is removed, thus creating a lower effective dielectric constant which will permit the desired increase in operating frequency. The length of this "cored" region is found from the transcedental equation (2.17), which is derived from the field expressions of the dominant mode of the cavity, after applying the boundary conditions at the various interfaces:

$$2\tan(K_1\frac{(b-b')}{2}) - \tan(K_o b')(\frac{K_1}{K_o}\tan^2(K_1\frac{(b-b')}{2}) - \frac{K_o}{K_1}) = 0 \qquad (2.17)$$

where K_o and K_1 are the propagation constants in the air and dielectric regions, respectively. By creating this "cored" region under the patch according to 2.17, the antenna is forced to resonate at the first or second higher order mode depending on the choice of b' (Eq. 2.17 yields two solutions other than $b' = b$ which is a trivial one). As a result the radiation pattern of the micromachined antenna will be altered, since at the second resonance there is a null ,instead of a maximum, at boresight and at the third resonance the pattern exhibits secondary or minor lobes (i.e the major lobe of the first resonance breaks into several lobes).

Patch Type	Conventional	Cored
b (mm)	1.894	6.665
a (mm)	1.0	1.0
b'(mm)	0	2.174
c (mm)	0.615	1.058

Table 2.5: Dimensions for the cored and conventional patch that were used in the FDTD simulations.

If the application that the patch antenna will be used requires one maximum at boresight and broad beamwidth, then only the trivial solution (i.e. $b' = b$) of 2.17 can be used. In the latter case, of course, the material is removed in the entire area underneath the patch.

2.3.2 Results

In order to test the accuracy of the previous analysis a rectangular patch with a resonant frequency of 22.5 GHz was designed on Silicon with ϵ_r=11.7 and a substrate thickness of 500μm. Since for the given substrate, higher order surface modes exist above 40 GHz elimination only of the dominant TM_0 mode is sufficient. The micromachined patch was compared with a regular patch on the same substrate and with the same resonant frequency. The dimensions of the two patches are given in Table 2.5 and the results from the FDTD simulations [49] can be seen in Fig. 2.10. Measurement of the normal field inside the dielectric region showed a suppressed electric field for the cored antenna, which was more than 10 dB lower than the field of the conventional patch (Fig. 2.10). Measurement of the reflection coefficient also with the help of FDTD, showed good agreement between the resonant frequencies of the cored patch and the conventional patch.

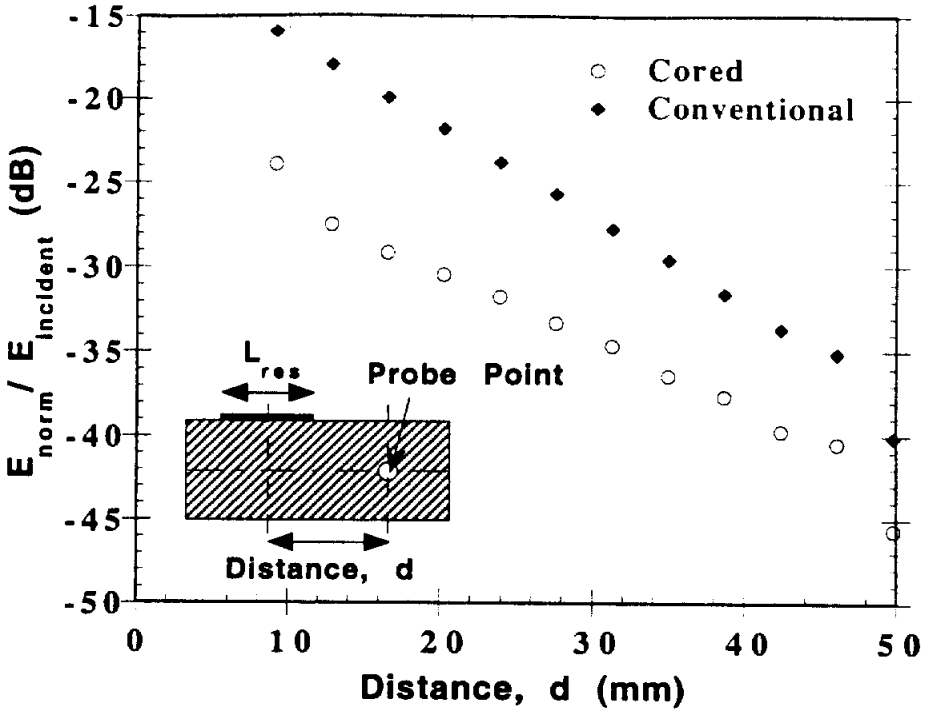


Figure 2.10: Normalized electric field inside the dielectric versus distance from the center of the antenna for the micromachined (cored) patch and regular patch.

2.4 Conclusions

Two different techniques for the reduction of surface waves in microstrip patch antennas were presented in this chapter. In the first technique, material was removed laterally underneath and around the patch in an effort to reduce locally the dielectric constant [38]. Experimental results of a micromachined patch fabricated on high-index Duroid showed superior performance when compared with a regular patch on the same substrate. The impedance bandwidth and the efficiency of the antenna increased by as much as 64% and 28%, respectively. The E-plane radiation patterns of the micromachined patch were also much smoother than those of the regular patch. In addition, for the micromachined antenna it was shown that placement of the antenna's radiating edges with respect to the edges of the cavity is critical to improving the power radiated as space waves (i.e. the efficiency) and must be at least twice the substrate thickness.

In the second technique, the resonant length of the rectangular patch was adjusted to a critical value in order to suppress the dominant TM_0 surface wave mode. Since this value is larger than the regular length of the antenna for a specific frequency of operation, a cored region that decreases the resonant frequency but forces the patch to operate at the first or second higher order mode was created underneath it. Simulation results with FDTD between a regular patch and one designed according to this technique, showed a substantial decrease in the electric field inside the dielectric. Both of the techiques presented in this chapter result in the enhancement of the antenna performance and indicate that patch elements can be integrated in compact MMIC designs on high-index environments.

CHAPTER 3

MICROMACHINED RESONATORS

3.1 Introduction

With the trend to incorporate all microwave components on a single chip, as is the case of a monolithic transmit/receive system, there is an increased need to build high-Q resonators that can be monolithically integrated with the rest of the circuitry on the same substrate. High-Q resonators are the building blocks for narrow-band, low-loss filters that are used mainly in communication and radar systems. Traditionally, for microwave frequencies these resonators are made of rectangular and cylindrical metallic waveguides that offer very low loss and flexibility in tuning by inserting backshorts and screws. Waveguides, however, are heavy, large (especially at lower frequencies) and costly to manufacture since each component must be precision machined one at a time. In addition, waveguides do not allow for an easy integration with monolithic circuits and active devices.

The implementation and maturity of micromachining techniques in the fabrication of microwave and millimeter-wave circuits [50] - [51] allows us now to make miniature silicon or GaAs micromachined waveguides or cavities that can be used for the fabrication of high-Q bandpass filters and multiplexers. The quality factor that can be achieved with this

technique is much higher than the quality factor of traditional planar microstrip or stripline resonators either printed on a dielectric material or suspended in air with the help of a dielectric membrane [12], [13]. The latter type of resonators can give filters with less than 1 dB insertion loss and bandwidths exceeding 10%.

This chapter discusses the development of a silicon micromachined high-Q X-band resonator that consists of a cavity, input and output microstrip lines and coupling slots. Experimental results of the performance of the resonator are shown and compared with simulations performed by Jui-Ching Cheng [1]. In addition, the quality factor of the resonator is evaluated based on s-parameter measurements. The effects of different ambient temperatures and the positioning of the slots relative to the center of cavity on the response of the resonator are also presented and analyzed, as well as some on-wafer packaging considerations.

3.2 X-Band Micromachined Resonator

3.2.1 Design and Fabrication

The X-Band resonator shown in Fig. 3.1 (for design see [1]) consists of input and output microstrip lines that reside on top of a Silicon wafer and couple energy via slots into a micromachined cavity that is formed inside a second wafer. The energy that is coupled to the cavity can travel through it in the form of a propagating or evanescent wave. Evanescent waves give the advantage of using smaller cavity sizes since the modes are operating below cut-off frequency. This resonator can be used as a building block for the fabrication of high-Q filters, such as the one shown in Fig. 3.2. Several wafers are stacked together and one or more cavities are formed inside them. Energy is coupled from one cavity to the other with the help of slots, whose size, position and orientation controls the coupling. The

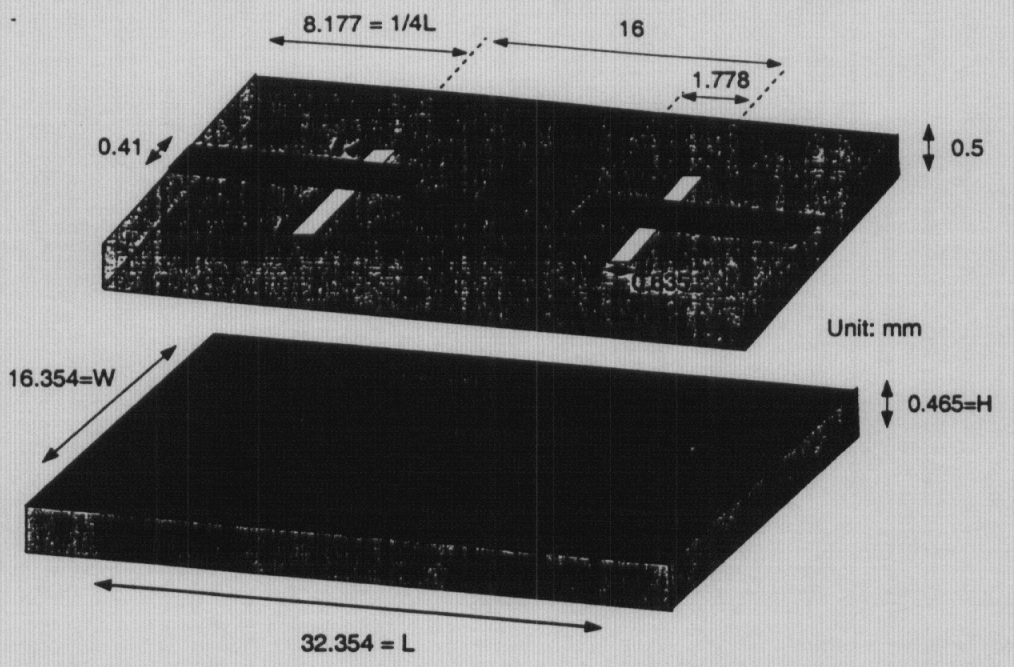


Figure 3.1: The X-Band micromachined resonator.

relative position of the slots with respect to the input and output microstrip lines controls the coupling to the input and output ports. Usually, the lines extend $\lambda_g/4$ beyond the center of the slots. Vertical stacking of the wafers greatly reduces the occupied area when a lot of resonators are needed in a high-Q filter design.

The resonator of Fig. 3.1 is a half-wavelength cavity that supports the dominant TE_{101} mode. For simplicity we will assume that the cavity walls are vertical and, thus, for the given dimensions the resonant frequency can be found from [52]

$$f_{res} = \frac{c}{2\pi}\sqrt{(\frac{\pi}{L})^2 + (\frac{\pi}{W})^2} = 10.277 \ \ GHz \tag{3.1}$$

The resonator was simulated using a hybrid Method of Moments (MoM)/Finite Element (FEM) technique developed by Jui-Ching Cheng [1] and was fabricated using standard micromachining techniques. Two silicon wafers, 500μm thick, with 1.45μm thermally grown oxide deposited on both sides were used [53]. The two microstrip lines on the top wafer were

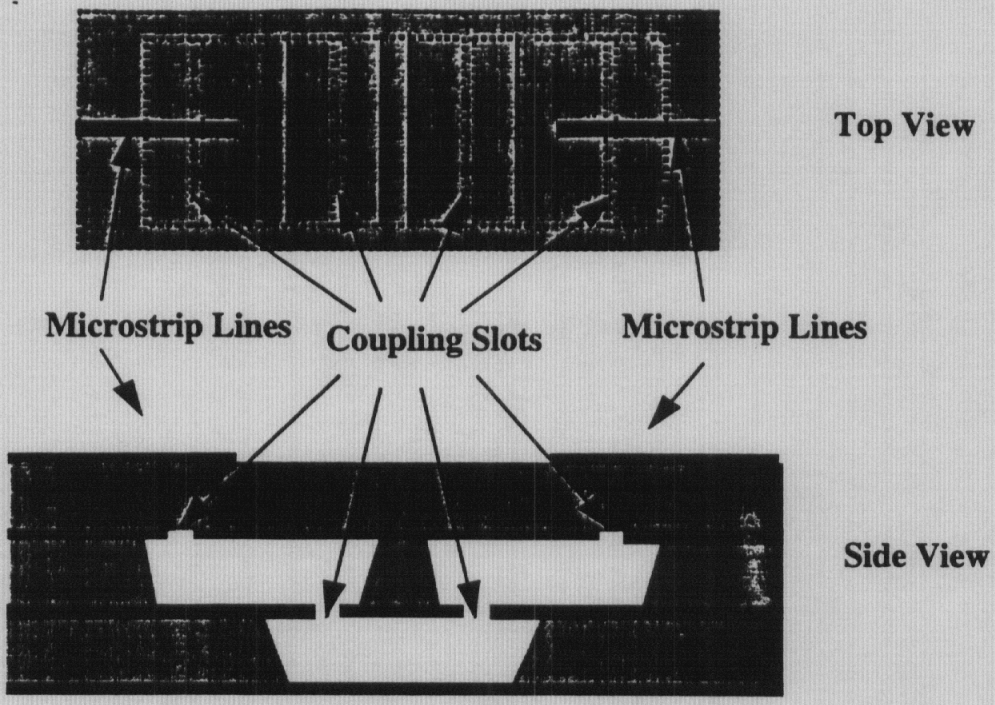


Figure 3.2: The structure of the proposed micromachined bandpass filters.

gold electro-plated with a total thickness of 7.5 μm in order to minimize losses. Infrared alignment was used in order to correctly align the two slots on the back of the wafer with the microstrip lines printed on the other side.

The cavity was fabricated on the second wafer by using chemical anisotropic etching (EDP or TMAH) until a depth of about 465μm was achieved. When the wafer was etched, it was metallized in the evaporator with a total metal (Ti/Al/Ti/Au) thickness of 2μm. The two wafers were then bonded together with silver epoxy glue at a curing temperature of 150°C. The alignment between the two wafers was achieved by opening windows on the top wafer during the etching process to align to marks that were placed on the second wafer. In order to measure the resonator with on-wafer probing, a coplanar waveguide (CPW)-to-microstrip transition (Fig. 3.3) that provides a match to the 50 Ω feeding lines was incorporated. The grounds of the CPW and the microstrip lines are set at an equal

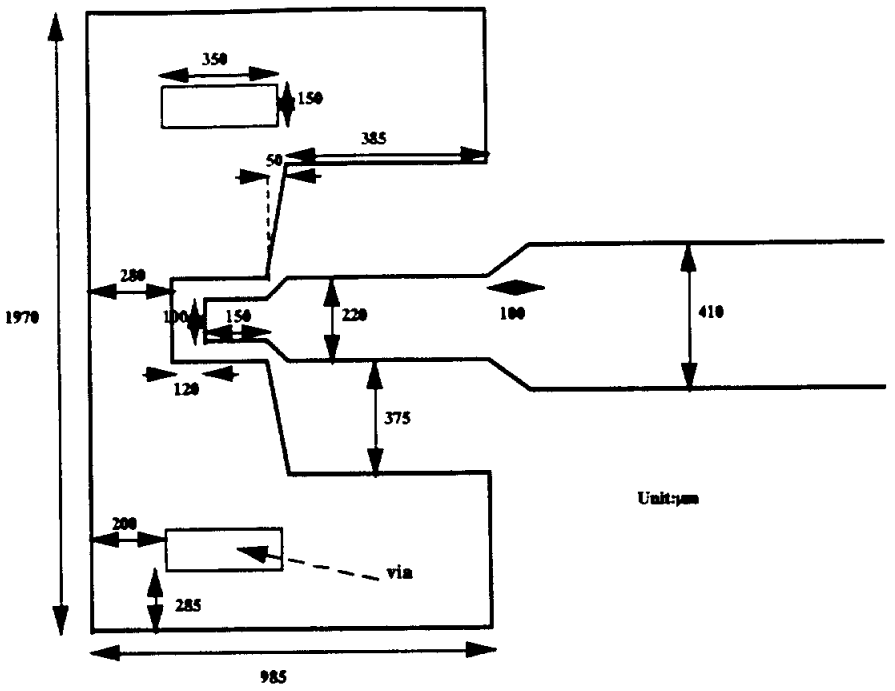


Figure 3.3: CPW-to-microstrip transition for 500μm thick silicon substrate.

potential with the implementation of via holes. Fig. 3.4 shows the measured results for the S-parameters of a 2.48 cm long 50 Ω line on 525 μm thick silicon substrate that employs the transition of Fig. 3.3. As it can be seen, the matching of the CPW to the microstrip line is excellent ($S_{11} \leq -35dB, S_{21} \approx \pm 0.02dB$).

3.2.2 Theoretical and Measured Results

The fabricated resonator of Fig. 3.5 was measured with the help of the HP8510C vector network analyzer and two 150μm pitch GGB probes. The reference planes for the measurement are at the middle of the slots and de-embedding was achieved using a Thru-Reflect-Line (TRL) calibration with the standards fabricated on the same wafer. Simulated and measured results [1] of the entire structure can be seen in Fig. 3.6 where very good agreement is observed. A more detailed measurement around the first resonance (Fig. 3.7)

[1] Simulation done by Jui-Ching Cheng [1].

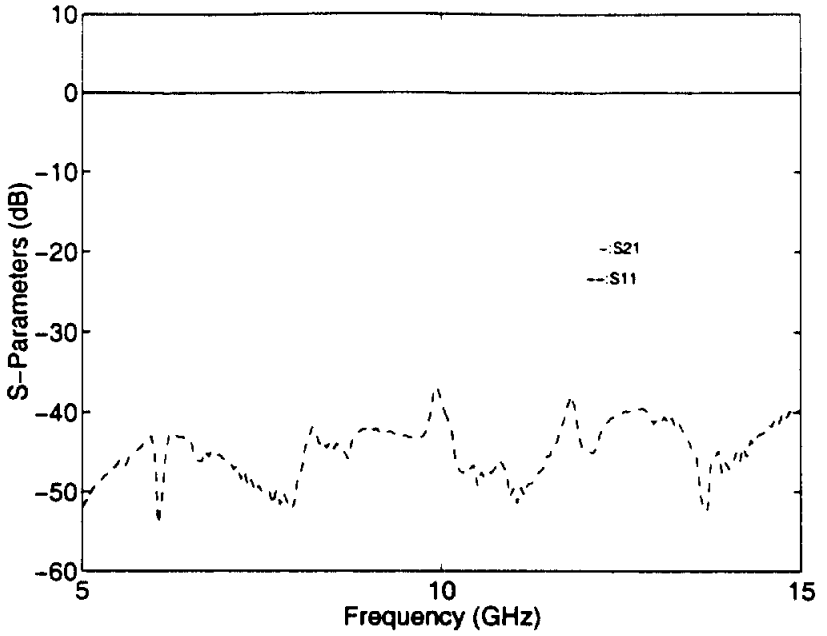


Figure 3.4: Measured results for a 50 Ω microstrip line that implements the transition of Fig. 3.3.

gives a resonant frequency of 10.285 GHz which is very close to that of a cavity with vertical walls, as calculated by equation 3.1. Fig. 3.7 also reveals an excellent agreement between the measured results and the simulations of the hybrid technique. The small difference (1%) in the center frequency is partly due to the finite accuracy in modeling the non-vertical slopes of the cavity and partly to the inherent numerical error of our simulation technique.

Fig. 3.8 [2] shows the z-component electric field density on the bottom of the cavity at the resonant frequency. The field pattern matches well with that of the first resonant mode of a half-wavelength rectangular cavity of similar size. The strongest field is located at the center of the cavity (the figure is drawn according to the physical dimensions of the cavity) where the peak of the standing wave exists, whereas at the four corners the intensity is minimal as expected.

In order to evaluate the unloaded Q (Q_u) of the cavity the losses due to the excess length

[2]Calculation done by Jui-Ching Cheng [1].

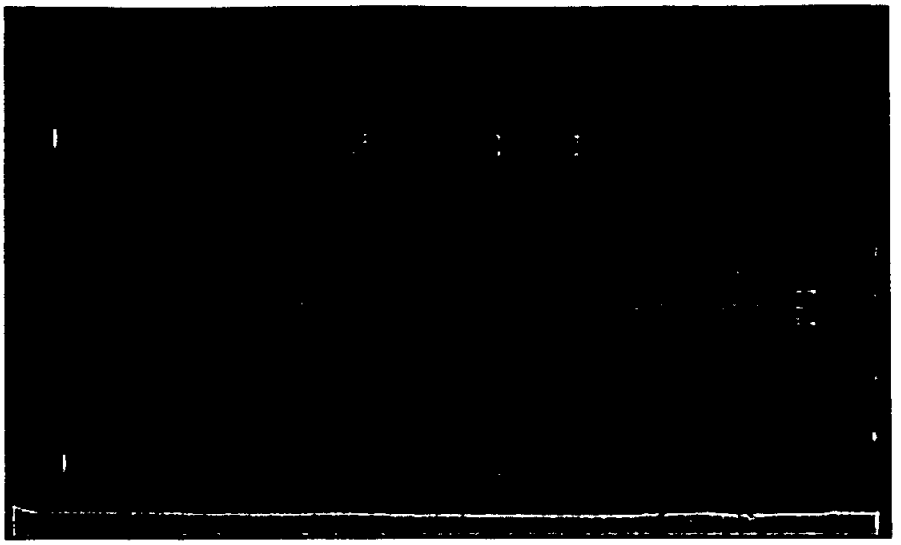


Figure 3.5: Fabricated X-band resonator on two 500μm silicon wafers.

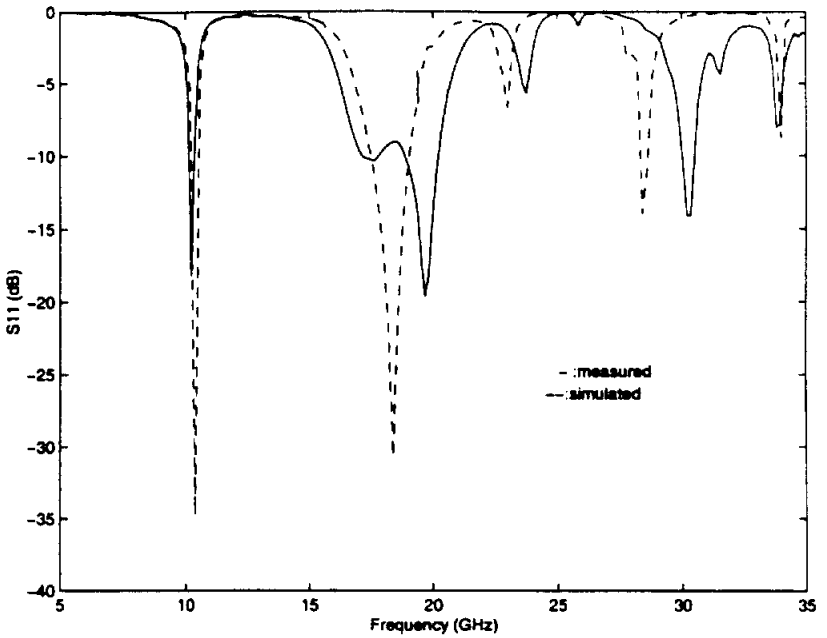
of the lines from the reference planes, that is needed to tune the slots, must be removed. For this reason the ohmic loss on the feeding lines is found from the TRL standards and is used to compute the loss on the two open end stubs extending beyond the center of the slots. For the measured results shown in Fig. 3.7 this loss has already been de-embedded. The loaded Q (Q_l) of the cavity defined as

$$Q_l = \frac{f_{res}}{\Delta f_{3-dB}} \tag{3.2}$$

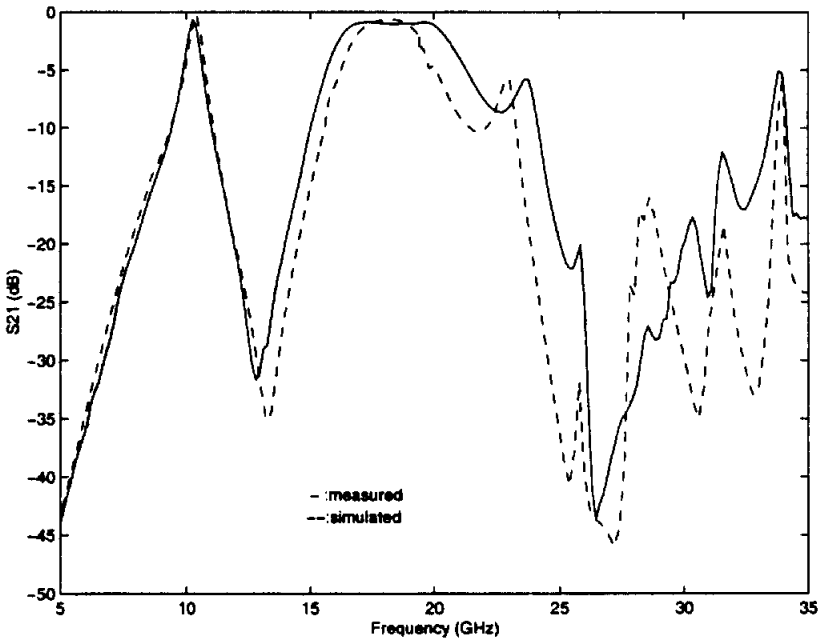
where f_{res}=10.285 GHz is the resonant frequency and Δf_{3-dB}=0.5 GHz is the 3-dB bandwidth, is found equal to 20.57. The external Q of the resonator, Q_e, that includes the input/output loading effects, can be found from [54]

$$S_{21}(dB) = 20log_{10}(\frac{Q_l}{Q_e}) \tag{3.3}$$

where S_{21} was measured to be 0.36$\pm$0.04 dB. The error in the measurement is attributed to the accuracy of the calibration technique. Equation 3.3 gives Q_e=21.44$\pm$0.1. Knowing



(a)



(b)

Figure 3.6: Simulated and measured results for the resonator of Fig. 3.1: (a) return loss and (b) insertion loss

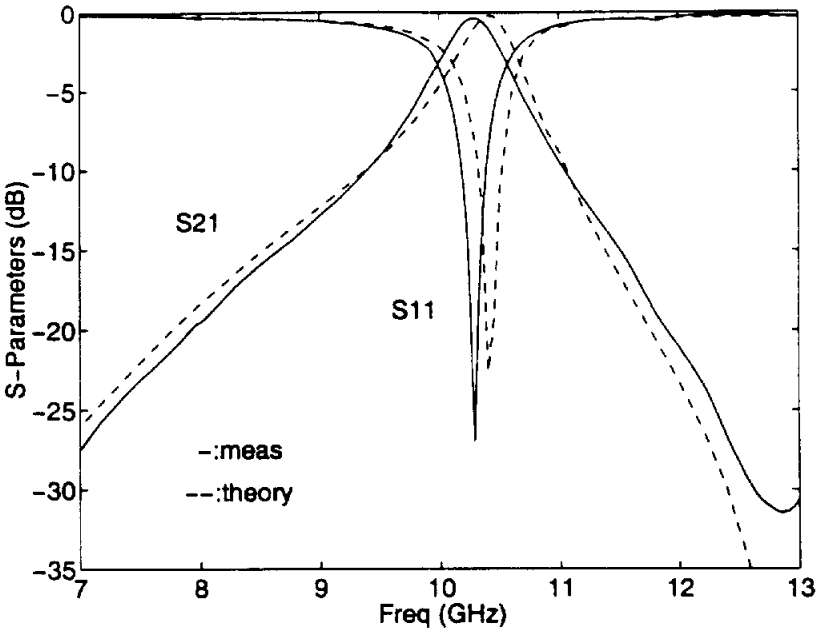


Figure 3.7: Measured and simulated S-parameters for the resonator of Fig. 3.1 around resonance.

Q_e and Q_l we can find Q_u from the known relation

$$\frac{1}{Q_l} = \frac{1}{Q_u} + \frac{1}{Q_e}. \tag{3.4}$$

Using the above definitions and the measured results, Q_u is found to be equal to 506±55. The theoretical value of Q_u for the dominant TE_{101} mode of a rectangular metallic cavity can be calculated from [52]

$$Q_u = \frac{(k_{101}LW)^3 H Z_0}{2\pi^2 R_m (2W^3H + 2L^3H + W^3L + L^3W)} \tag{3.5}$$

where $R_m = \frac{1}{\sigma\delta_s}$ is the resistive part of the surface impedance exhibited by the conducting wall with a conductivity σ and a skin depth $\delta_s = \sqrt{\frac{1}{\pi f_{res}\mu\sigma}}$. For the cavity with the dimensions of Fig. 3.1 and a conductivity of $\sigma = 3.8 \times 10^7 S/m$ (Aluminum) equation 3.5 gives $Q_u \simeq 526$, which is very close to the measured value.

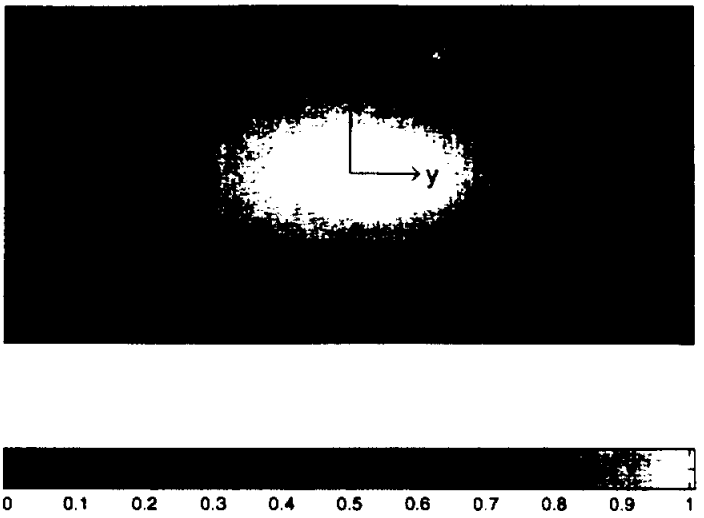


Figure 3.8: Computed z-component of the electric field density on the bottom of the cavity (from Jui-Ching Cheng [1]).

The performance of the proposed micromachined resonator is compared with that of other X-band resonators, both planar and non-planar, and the results are summarized in Table 3.1 (for the first cavity of Table 3.1 see [55]). As seen by this table, the micromachined cavity has a Q similar to a metallic waveguide cavity with the same dimensions, but it has the advantage of maintaining a planar form that allows for easy integration with MIC and MMIC structures. Despite its planar character, the micromachined cavity has a Q that is four times higher than that of traditional microstrip resonators (Q_u=125). Higher values of Q can be achieved with the micromachined resonator if more than one wafer are stacked together (or thicker silicon wafers are used), as indicated both by eq. 3.5 and the first cavity of Table 3.1, where the height H is 10.2 mm in contrast with 0.465 mm of the fabricated circuit. This gives the potential for the realization of planar/monolithic high-Q filters and multiplexers.

type		size (mm x mm x mm)	Q_u
non-planar	metal (rectangular)	19.8x22.9x10.2	8119
	metal (rectangular)	16x32x0.465	526
planar	micromachined cavity	16x32x0.465	506
	membrane-microstrip [54]	5.3x7.1x0.35	234
	microstrip [54]	2.65x3.55x0.5	125

Table 3.1: Comparison of measured Q for several resonators at X-band.

3.3 Thermal Testing

In communication and radar systems that use narrow-band filters and multiplexers, the thermal stability of the different components and sub-systems is of paramount importance. A small drift in the resonant frequency of a high-Q filter can result in out-of-band operation leading to performance deterioration or even system failure. This section presents measurements on the response of the micromachined resonator when operating under different ambient temperatures.

The structure of Fig. 3.1 was tested [3] with an HP8510 and a probe station whose stage temperature could be controlled. The system was calibrated up to the probe tips with an SOLT calibration and the temperature varied from $25°C$ to $145°C$. Due to the nature of the calibration the losses due to the microstrip lines and the CPW-to-microstrip transitions were not de-embedded. Results can be seen in Fig. 3.9, where we observe that the resonant frequency f_{res} = 10.3 GHz does not shift with the increase in temperature but is rather maintained at the same value. The expected change in the dimensions of the cavity due to the temperature variation can be found from [56]:

[3] Measurements performed at M/A-COM Company.

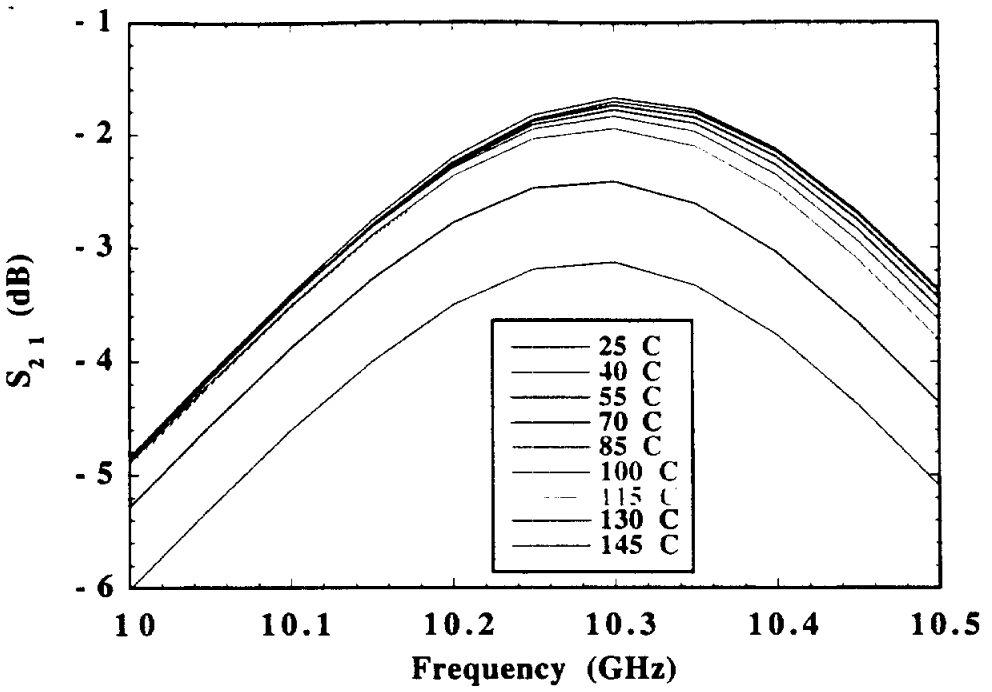


Figure 3.9: Measured insertion loss of the micromachined resonator under different temperatures.

$$l(T_2) = l(T_1) + \alpha l(T_1)(T_2 - T_1) \tag{3.6}$$

where α is the temperature coefficient of expansion, T_1 and T_2 are the initial and final temperatures, respectively, and $l(T_1), l_(T_2)$ are the lengths at the initial and final temperatures, respectively. If we use α= 2.33 $ppm/°C$, which is the temperature expansion coefficient of silicon [18], $T_1 = 25°C$, $T_2 = 145°C$, L(25)=32.354 mm and W(25)=16.354 then equation 3.6 yields L(145)=32.363 mm and W(145)=16.358 mm. When inserted in equation 3.1, the new dimensions of the cavity at a temperature of $145°C$ give a resonant frequency of $f_{res} = 10.274GHz$, which is a change of 0.03% from the initial value and is in good agreement with the measured results. It should be noted here that the resolution of the network analyzer for the thermal testing was 50 MHz. This excellent behavior relative to temperature changes, makes the micromachined resonators ideal for the fabrication of

narrow-band filters that operate under different environment conditions.

Regarding the insertion loss, Fig. 3.9 shows that it increases with temperature (from 1.66 dB to 2.4 dB) with the effect being more pronounced above $115°C$. Up to that temperature the degradation is due to the increased number of intrinsic carriers that reduce the bulk resistivity of the wafer and, thus, increase the dielectric loss of the microstrip lines. From figures 3.2 and 4.4 of [57] for T=$115°C$ $N \approx 4x10^{12}cm^{-3}$ and $\mu \approx 650cm^2/(V-s)$, respectively. If the mobility and the carrier concentration are known then the silicon resistivity can be found from [27]

$$\rho = \frac{1}{q\mu N} = 2.4x10^3 \Omega cm \tag{3.7}$$

The dielectric loss tangent, tanδ, can then be evaluated from equation (2.21) of [47]

$$tan\delta = \frac{\sigma}{\omega\epsilon_o\epsilon_r} = 0.0062 \tag{3.8}$$

where f=10.3 GHz and $\epsilon_r = 11.7$. The dielectric loss of a microstrip line can also be found from equation (4.207) of [47]

$$\alpha_d = \frac{K_o\epsilon_r(\epsilon_{eff}-1)tan\delta}{2\sqrt{\epsilon_{eff}}(\epsilon_r-1)} = 1.55Np/m = 13.5dB/m = 0.0135dB/mm \tag{3.9}$$

where $\epsilon_{eff} = 6.35$. The total length of the two microstrip lines from the probe location to the coupling slots is approximately 23 mm and, therefore, the additional dielectric loss will be 0.31 dB. This result is in very good agreement with the insertion loss difference between $115°C$ and $25°C$, $S_{21}(115) - S_{21}(25) = 2 - 1.67 = 0.33$ dB. For temperatures above $115°C$ the insertion loss increases more rapidly. This is due to the silver epoxy glue that is used to bond the two wafers, whose characteristics change with temperature above $120°C$ where curing takes place. A good solid wafer bonding is critical for the loss of the cavity resonator,

since small gaps between the wafers can cause energy to leak out of the cavity and radiate. Therefore, instead of using silver epoxy glue a more reliable eutectic bonding techique needs to be developed that will assure the low insertion loss of the micromachined resonator at different temperatures. It should be noted here that the thermal testing measurement was only performed once and was not repeated.

3.4 Effects of Slot Positioning on Resonator Performance

For the resonator of Fig. 3.1 the two coupling slots are positioned at 1/4 and 3/4 of the cavity length L from the shorter edges of the resonator. In this section we study the effect of different slot positions on the response of the micromachined structure.

A resonator with the slots located at 3/8L and 5/8L from the shorter edges was fabricated, using two 500 μm thick silicon wafers with PECVD nitride grown on both sides [58]. The depth of the etched cavity was about 470 μm and the metallization thickness was 3 μm. Measurements were done using the HP8510C network analyzer and the TRL calibration technique with the reference planes at the center of the slots (same method as the original resonator), while simulations were run using the HFSS software. A comparison of the simulated and measured results can be seen in Fig. 3.10, where a small discrepancy (1%) in the resonant frequency can be observed. This can be attributed to the inherent numerical error of the simulation technique. The measured resonator exhibits a bandwidth of 2% (210MHz) at a resonant frequency f_{res}=10.525 GHz and an insertion loss of 1.1 dB.

Measured results from both resonators can be seen in Fig. 3.11, where we observe that in the new resonator the bandwidth is reduced by 58% (from 500 to 210 MHz) while the insertion loss is increased by 0.74 dB (from 0.36 to 1.1 dB). This indicates that by changing the position of the slots relative to the center of the cavity, we can change the bandwidth

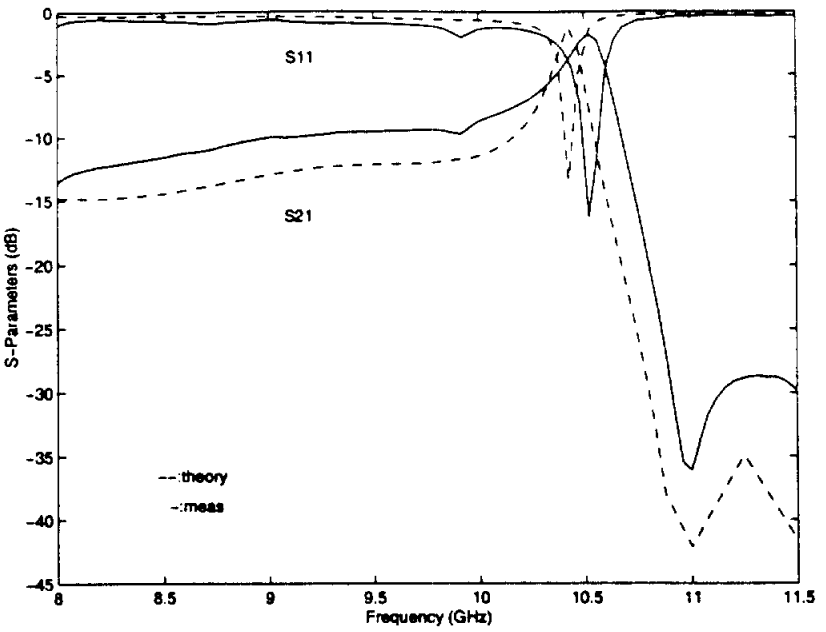


Figure 3.10: Measured and simulated results for the resonator with the slots positioned at 1/8L and 3/8L.

of the resonator at the price of changing the loss at the same time. In the previous case the bandwidth was reduced and the loss was increased, as expected, since the quality factor of the resonator is mainly determined by the propagating mode of the cavity and not the slot positions. However, when the two slots are very close together, evanescent modes can be excited that alter the Q_u of the resonator. A bandwidth greater than 500 MHz can be achieved if the two slots are positioned closer to the cavity edges.

From Fig.3.10 we can also observe a slight asymmetry in the response around the resonance. This is due to the close proximity of the two microstrip lines ($0.4\lambda_g$) which allows power coupling from one to the other directly via substrate modes. In order to eliminate this effect and make the response more symmetric around resonance, we can use on wafer packaging [59] as seen in Fig.3.12 to isolate the microstrip lines from one another both on top and inside the substrate. For this purpose an HFSS simulation was run with one perfect electric conductor on top of the structure and another placed between the two lines shorting

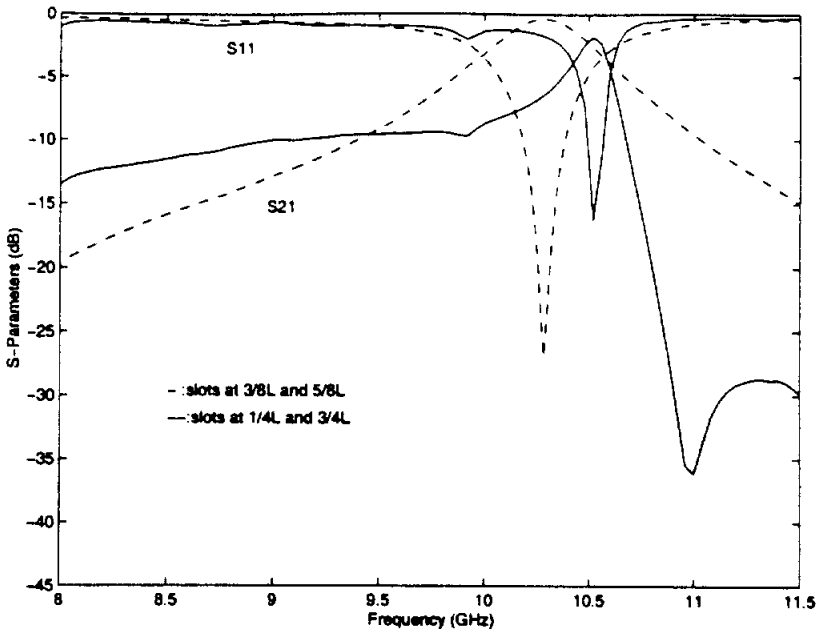


Figure 3.11: Measured results for the two resonators with different slot positions.

the top conductor with the slot ground plane. Fig. 3.13 shows the results of the simulation for the geometry of Fig. 3.12, where it can be seen that packaging reduces the suspected coupling occuring below 10.3 GHz by as much as 4 dB. The small coupling of about -16 dB below 10 GHz can be attributed to evanescent modes that are excited around the slots inside the cavity. These modes cannot be avoided since the slots are so close together.

3.5 Conclusions

A micromachined resonator that consists of a cavity, input and output microstrip lines and coupling slots has been fabricated and tested. Measurements have shown an unloaded quality factor Q_u of 506, a bandwidth of 5% and an insertion loss of 0.36 dB. Thermal testing has demonstrated that the resonant frequency of the structure does not drift when ambient temperature increases. Different positioning of the coupling slots with respect to the center of the cavity has also shown that it is possible to alter the resonator bandwidth at the price

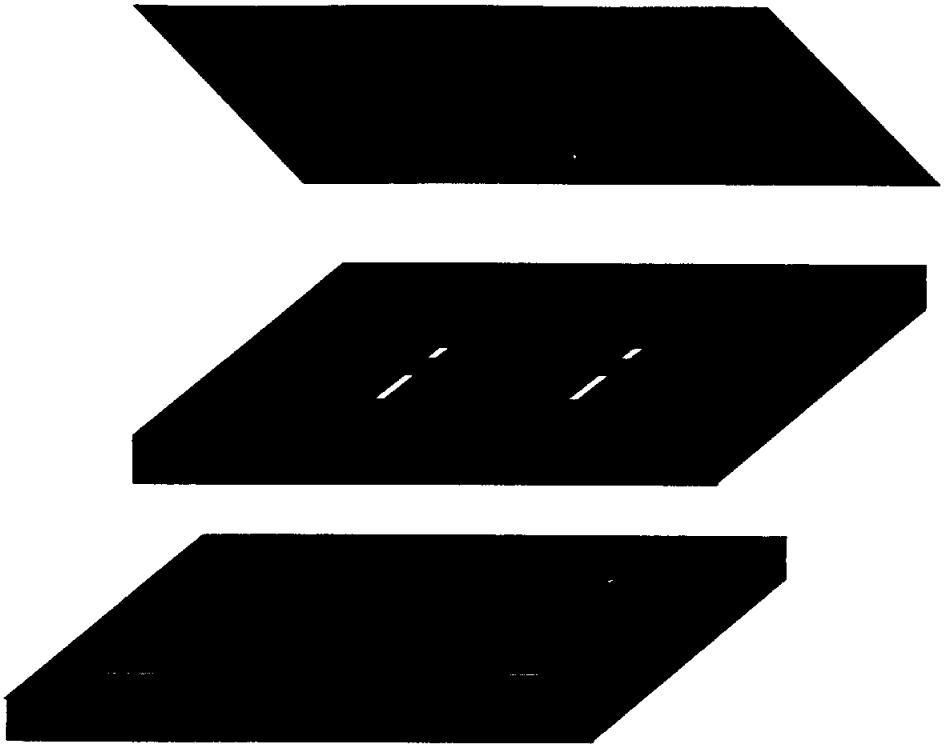


Figure 3.12: Micromachined resonator with on-wafer packaging.

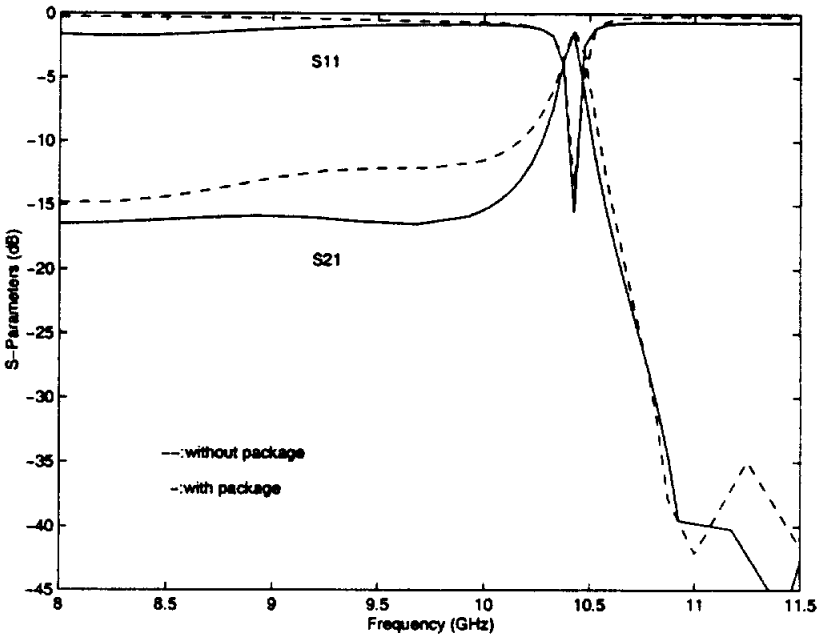


Figure 3.13: Simulation results fot the packaged and non-packaged resonator.

of changing the insertion loss; a 2% bandwidth with a loss of 1.1 dB has been measured for slots located at 3/8L and 5/8L from the shorter edges of the cavity. Implementation of on-wafer packaging is also possible in order to reduce direct coupling between the microstrip lines when they are close together or achieve shielding of the structure and isolation. The resonator presented in this chapter offers the advantage of having a quality factor which is much higher than that of traditional microstrip or stripline resonators, while maintaining the planar character of the circuit and allowing for easy integration with MIC or MMIC structures and active devices. It also offers reduced weight and size and lower cost when compared with waveguide resonant systems. This resonator can be used for the design and fabrication of planar high-Q filters and multiplexers.

CHAPTER 4

GaAs MONOLITHIC MULTIPLIERS

4.1 Introduction

For a monolithic transmit/receive module operating at millimeter and sub-millimeter wavelengths, local oscillator sources are necessary. At lower frequencies transistor sources are available and two terminal devices such as Gunn oscillators provide power up to approximately 150 GHz, but harmonic multipliers are the main RF sources at higher frequencies. A detailed summary and review of multiplier performance can be found in [60], [61]. Most multipliers are based on Schottky barrier diodes with early multipliers using a honeycomb anode chip with a whisker contact across a waveguide mount. Whisker contacted diodes have very low parasitics, but are difficult to handle, can have problems with thermal cycling and vibrations and have performance that is critically dependent on the shape of the whisker. Even with these problems, whisker contacted multipliers were the most common millimeter and submillimeter wave sources until the late 1980s. A typical low power whisker contacted multiplier had 35% efficiency at 98 GHz [62]. In 1987 Bishop et. al. proposed the microchannel structure as an alternative high frequency planar diode [63]. This structure was much easier to handle and could also be used to fabricate multiple diodes for the same

mount. An example of this type of multiplier is given by Rizzi et. al. [64] and has a peak output power of 55 mW at 174 GHz and a peak efficiency of 25% using a balanced combination of two diode pairs. More recently, Erickson [65] has demonstrated a fixed tuned planar four diode doubler centered at 150 GHz that has a 28% peak efficiency, a 3 dB bandwidth of 130-168 GHz and an output power of 25-40 mW. In addition, Potterfield [66] has fabricated a fixed-tuned 40 to 80 GHz doubler employing a linear array of 6 Schottky diodes with 48% efficiency and 80-100 mW of output power. Planar diodes are approaching the performance of their whisker counterparts.

Most millimeter wave multipliers are based on waveguide circuits. Waveguide circuits have the low loss and high Q needed for efficient multiplier operation and can also include tuners and backshorts needed to optimize for peak performance. However, waveguide mounts are complex and become more difficult and expensive to machine with increasing frequency and smaller size. An alternative approach uses many diodes and quasi-optical techniques to greatly increase the power output [67], [68]. This approach allows the power generation and tuning to function on a spatial grid with each grid element having printed tuning elements. The result is usually increased power and reduced efficiency when compared with waveguide multipliers. Another multiplier approach is monolithic or MMIC multipliers. Many similar MMIC multipliers can be fabricated at the same time using integrated circuit fabrication techniques and thus producing low cost circuits. However, planar circuits tend to have higher loss and lower Q when compared to waveguide ones and it is also more difficult to include tuning elements. Even with these limitations, some very useful MMIC multipliers have been reported. Chen et. al. [14] described a planar MMIC multiplier with an output power of 65 milliwatts and an efficiency of 25% at 94 GHz using a microstrip circuit. Bruston [15] has also demonstrated a microstrip based doubler from

160 to 320 GHz with 2.8% efficiency. The latter multiplier, however, suffers from moding problems due to the nature of the transmission line that is used. Filipovic [69] designed a balanced varactor multiplier based on grounded-CPW and slotline transmission media with Schottky varactor diodes that yielded an efficiency of 1% at 90 GHz. CPW technology has also been implemented in the design of a Ka-band (18/36 GHz) FET MMIC doubler that exhibited a maximum conversion gain of 3 to 6 dB [70]. Brauchler [2] used the Finite Ground Coplanar (FGC) line, which is a modified form of the coplanar waveguide, to build a 40 to 80 GHz doubler with 15-16% efficiency, at least 10 GHz bandwidth and 72 mW of output power.

This chapter presents several GaAs FGC line based doublers designed for a higher efficiency and output power in W-band than the ones demonstrated in [2]. The characteristics of FGC lines on GaAs with different geometries and impedances covered with a polyimide overlay for passivation are first presented and compared with similar lines on quartz, which is a low loss substrate. W band multipliers that consist of two Schottky diodes with input Q's of 2 and 3 are then demonstrated and experimental results are compared with simulations. A doubler that has four diodes and can give more output power is also designed and tested. Finally, a method that can increase the efficiency of a doubler by altering the passive circuit design is investigated and experimental results are presented.

4.2 Study of FGC lines

High performance line structures are an important part of MMIC design and fabrication at millimeter-wave frequencies [16], [71]. The lines that are traditionally used in planar circuit design are microstrip and coplanar waveguide. For a given substrate thickness and cross section conventional microstrip lines have increasing dielectric loss with frequency.

One solution to this problem is to use a low loss material such as quartz as a substrate. However, this requires bonding active circuits onto the quartz, which increases fabrication complexity especially at higher frequencies, while at the same time the requirement for thinned substrates is still important to satisfy in order to avoid moding. CPW lines on the other hand can support parallel plate waveguide modes that can be suppressed with the help of via holes. These vias introduce parasitics and increase fabrication complexity.

An alternative transmission line to the ones discussed before is the FGC line, which is a modified Coplanar Waveguide (CPW) structure with improved performance at millimeter wave frequencies [72]. It consists of three strips, one for the signal and two for the ground, similar to the CPW line, but with ground strips that are narrow. The main advantage of the FGC lines is that the cut-off frequency of higher order modes can be controlled in a way that they are far away from the desired band of operation of the structure under test. As a result, parallel plate modes are not excited and vias are not required for ground equalization. The permittivity and attenuation characteristics of FGC lines on GaAs and Si have been extensively investigated by several researchers [73], [2], [74]. Experimental results show that a nearly TEM mode propagates over a wide frequency range (2-118 GHz) and that loss is mainly ohmic. The use of semiconductor substrates, therefore, will have a small effect on the line loss properties. In addition, the implemetantion of full thickness substrates and the elimination of via holes for mode suppression reduces the cost and complexity of MMIC design and fabrication at millimeter-wave frequencies.

Since passivation is an important part of active structure design and fabrication, it is desired to study its effects on the FGC line properties. Polyimide is a well characterized dielectric material that has been extensively used in the past as a passivation layer and as a substrate for the fabrication of microstrip lines [75], [76], [77]. In this section we investigate

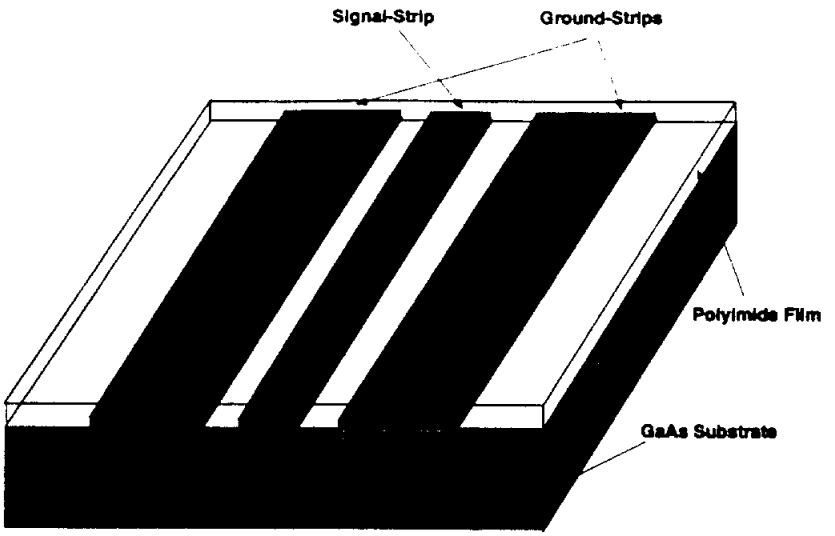


Figure 4.1: FGC lines on GaAs with a polyimide overlay

the effect of a thin polyimide coating on top of the GaAs FGC lines and compare their performance with low loss quartz based lines. The cross section of the fabricated FGC lines can be seen in Fig. 4.1. Four configurations were fabricated and tested: a) FGC lines on GaAs with Z_0=40, 50 and 60 Ω, b) FGC lines on GaAs with a 2 μm thick polyimide overlay and $Z_0 = 50\ \Omega$, c) FGC lines on GaAs with a 3 μm thick polyimide overlay and $Z_0 = 50\ \Omega$ and d) FGC lines on quartz with Z_0=70, 90 and 100 Ω.

4.2.1 Fabrication

The FGC lines were fabricated on a 525 μm thick semi-insulating GaAs wafer and a 165 μm thick quartz wafer. The FGC line signal-strip (w), slot (s) and ground-strip (w_g) widths were 50, 45, 160 μm, respectively and correspond to a 50 Ω line for GaAs substrate and to 90 Ω for quartz substrate. The characteristic impedances were calculated with equations (7.11)-(7.12) of [78] that yield the impedance of a coplanar waveguide line. However, as it was shown in [2] the coplanar strucure confines the electric field near the center of the structure and, thus, truncating the CPW line in a way that does not change the fields

near the outer edge of the ground strip will not significantly change the characteristic impedance, effectivity permittivity and loss of the line. The impedance of the resulting FGC line, therefore, is almost the same as that of a CPW line with the same signal and slot widths for an appropriate ground width.

The lines were created by using standard lift-off process with a total metal thickness of 1 μm. For a metal alloy that consists primarily of gold and aluminum the skin depth at 40 GHz is $\delta_s \approx 0.4\mu m$ and ,therefore, for that frequency the total metal thickness is equal to 2.5 skin depths. After the lines were formed, polyimide Pyralin PI2545 was spun at 4 Krpm and 2.5 Krpm on top of the lines for two GaAs wafers, in order to get a thickness of 2 μm and 3 μm respectively. The pre-cure temperature for the polyimide film was 140° C and the hard-cure 200° C, while the baking time was set to 30 minutes and 3 hours respectively. At the beginning and the end of the FGC lines the polyimide was chemically etched in order to allow the probe tips of the measurement system to be in electrical contact with the lines. The relative dielectric constant of the polyimide film is 3.5. The test FGC lines consisted of a thru line with a length of 1.0 mm, a short with a length of 0.5 mm and 3 delay lines with 1.388 mm, 4.106 mm and 10 mm lengths respectively.

4.2.2 Results and Discussion

All of the mesurements for the FGC line characteristics were performed with an HP8510C network analyzer and a probe station using a variety of RF probes. De-embeding was achieved by performing a Thru-Reflect-Line (TRL) calibration with the help of Multical [30], a measurement program available from NIST. This program also provides the effective dielectric permitivity and attenuation characteristics of the lines under test, from the delay line measurements.

The effective dielectric constant of the various line configurations is shown in Fig. 4.2. As can be seen, the nearly constant behavior of ϵ_{eff} over the entire frequency range indicates the propagation of a nearly pure TEM mode. In addition, we observe that the thin film of polyimide is responsible for a slight increase in ϵ_{eff} for both the 2μm polyimide (1.4%) and the 3μm polyimide (2.8%) when compared to that of bare FGC lines. This result is expected since the polyimide thickness is a very small fraction of the line dimensions and , therefore, the filling factor, q, for the polyimide layer that determines its contibution to the total value of the effective dielectric constant according to equation (7.52) of [78] is almost zero. More intuitively, for such a small thickness compared to the signal and slot widths the amount of electric field lines residing in the polyimide is minimal.

Fig. 4.3 shows the attenuation per physical length for the four different cases. The straight line between 60 and 70 GHz represents a gap in the data. As can be seen, the polyimide increases the attenuattion constant with the effect being more pronounced in W-band (12%) and for the thicker polyimide (23% in W-band). The quartz has the smallest attenuation for all the lines. This lower loss when measured in dB/cm is due to the lower effective dielectric constant and higher characteristic impedance of the FGC line on quartz (90 Ω compared to 50 Ω for GaAs). At 60 GHz, which is the center of the measurement band, the attenuation for the quartz, bare GaAs, 2 μm polyimide overlay and 3 μm polyimide overlay lines is 1.1 dB/cm, 1.7 dB/cm, 2 dB/cm and 2.1 dB/cm , respectively. The results of Figs. 4.2 and 4.3 are in very good agreement with similar results shown in [73], [2], [74] and [75]. Since in most microwave circuits lengths are expressed in terms of guided wavelengths, the attenuation per guided wavelength for the four different lines has been evaluated and is shown in Fig. 4.4. The results are comparable for all four cases with GaAs (bare or with polyimide) being slightly better than quartz. This indicates that the loss of

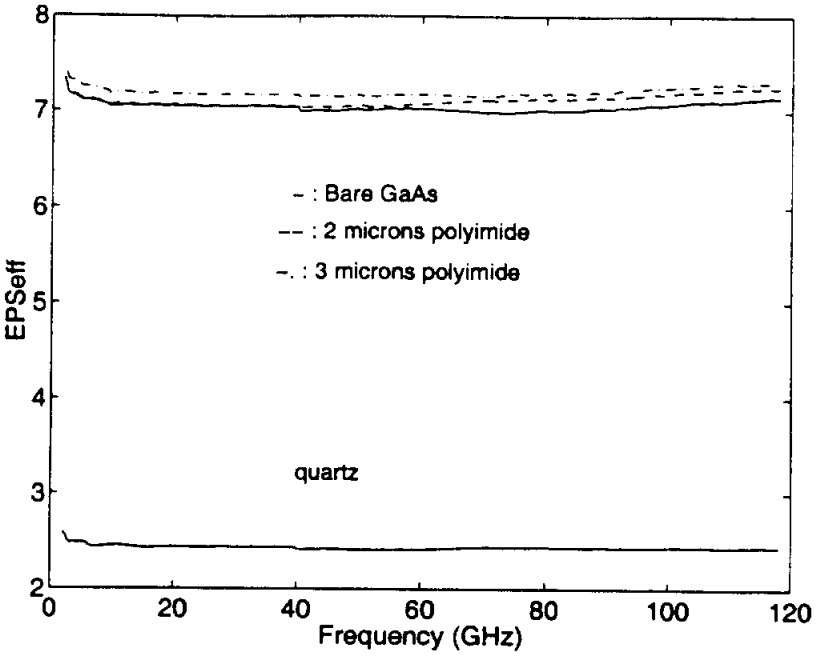


Figure 4.2: Effective dielectric constant vs. frequency for the various FGC lines.

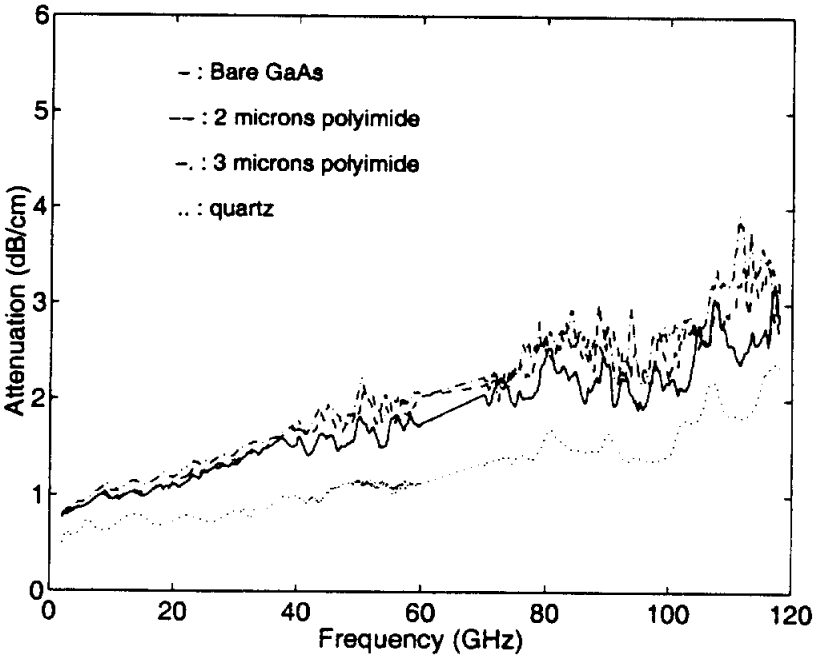


Figure 4.3: Attenuation per physical length vs. frequency for the various FGC lines.

FGC lines is ohmic in nature and independent of the substrate material. As a result, FGC lines are very good candidates for high frequency application circuits, such as multipliers and mixers. Furthemore, we can conclude that the thin layer of polyimide that covers the FGC lines on GaAs for passivation purposes slightly increases the attenuation of the lines.

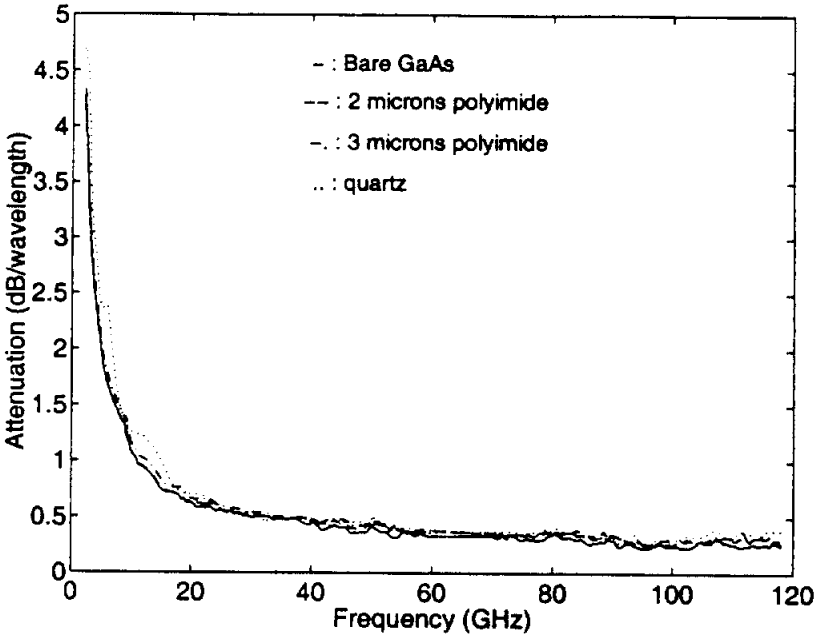


Figure 4.4: Attenuation per guided wavelength vs. frequency for the various FGC lines.

Since the characteristic impedances for the lines investigated were different for GaAs and quartz, additional lines with varying dimensions and impedances were also fabricated. The impedance range for the two substrates corresponds to a convenient range for line fabrication. The line dimensions and the corresponding Z_0 were calculated with the design equations (7.92) of [78] and can be seen in Table 4.1. From the measured attenuation per physical length, the attenuation per guided wavelength was evaluated and can be seen in Fig. 4.5 for GaAs and Fig. 4.6 for quartz. From Fig. 4.5 we observe that the 50 and 60 Ω lines have practically the same attenuation while for the 40 Ω line there is an increase of about 100% at 60 GHz which is the center of the entire frequency range. Similarly, from

Fig. 4.6 we observe that the attenuation for the 90 and 100 Ω lines is almost the same and that the 70 Ω line exhibits a 60% increase from the other two lines at 60 GHz. These results are expected since the line attenuation can increase considerably if the slot width is decreased a lot, as is the case of the 40 Ω and 70 Ω lines on GaAs and quartz, respectively, where the slot width is reduced to a third ($s \approx 15\mu m$) of its initial value (s=45 μm). Similar trends where the total line attenuation almost doubles when s+w/2 is half of its original value have been found by other researchers [79], [80]. We should note here that the small ripple observed in the 90 and 100 Ω lines is due to ripple in the mismatched measurement system.

substrate	w (μm)	s (μm)	Z_0 (Ω)
GaAs	50	15.45	40
GaAs	50	64.5	60
Quartz	50	18.61	70
Quartz	50	64.5	100

Table 4.1: Geometrical characteristics for the fabricated lines.

In order to better understand the behavior of the FGC lines versus impedance, the measured attenuation per physical length data were curve fitted to a $a + b\sqrt{f}$ function and the extracted functions were used in order to evaluate the attenuation per guided wavelength for three different frequency points in the center of each measured band. The final results can be seen in Fig. 4.7 for both quartz and GaAs, where we observe that the attenuation increases as the impedance is decreased. This behavior can be explained from the fact that low-impedance lines have narrow slots and, therefore, the current density at the edges of the slots is higher resulting in more loss. Similar graphs showing the dependence of the

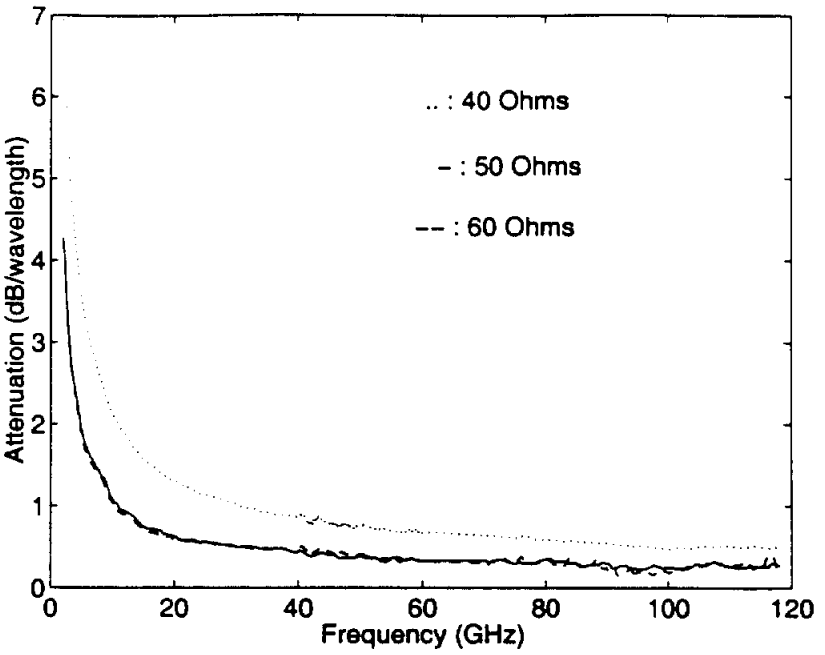


Figure 4.5: Attenuation per guided wavelength for lines on GaAs with different Z_0.

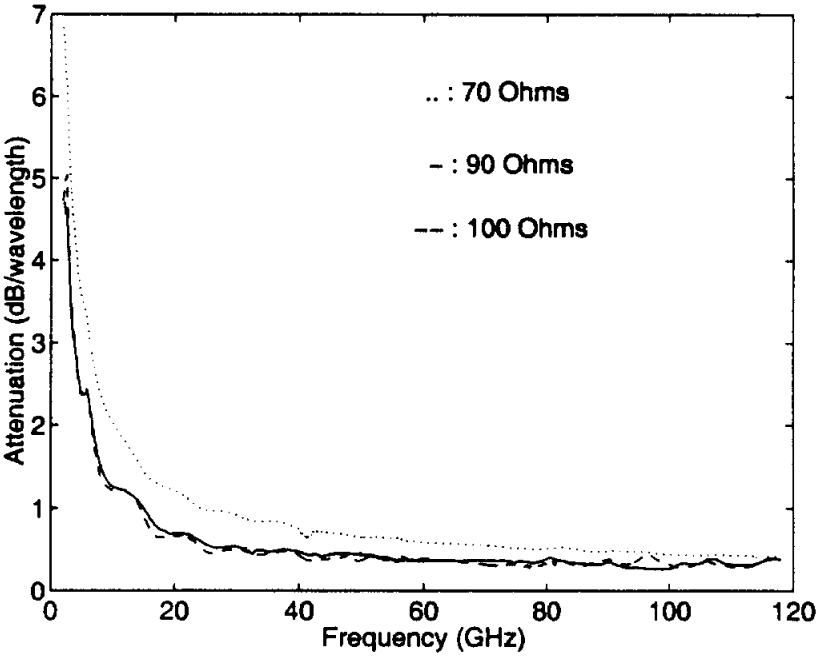


Figure 4.6: Attenuation per guided wavelength for lines on quartz with different Z_0.

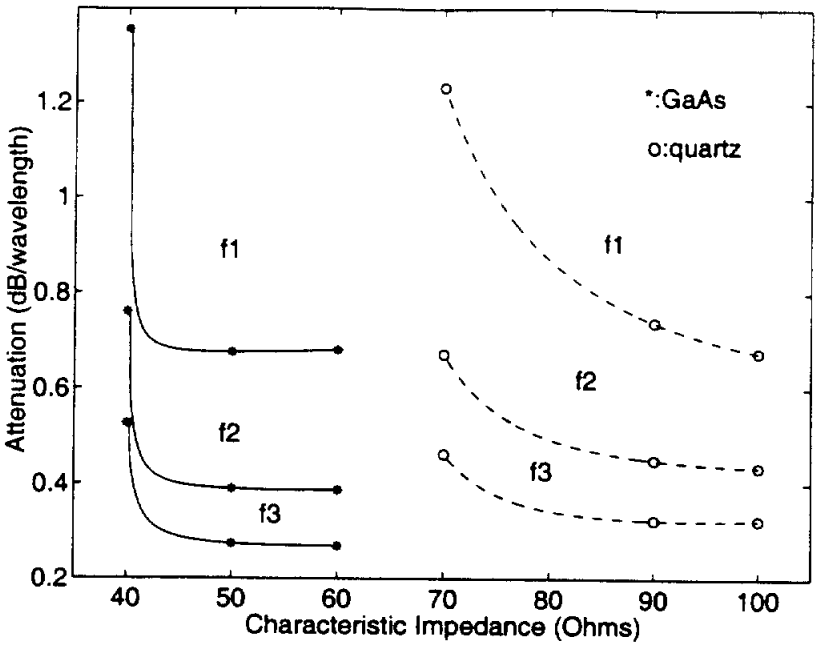


Figure 4.7: Attenuation per guided wavelength vs. characteristic impedance Z_0 for lines on GaAs and quartz at three different frequencies: f_1=19.1 GHz, f_2=50 GHz and f_3=94 GHz.

attenuation on the characteristic impedance of a coplanar line can be found in [78]. In terms of loss in dB/λ_g a 50 or 60 Ω line on GaAs is equivalent to a 90 Ω line on quartz. However, we should note that the 50 Ω and 60 Ω GaAs lines have the same geometrical dimensions with the 90 Ω and 100 Ω lines on quartz respectively, indicating a strong dependence of the total line loss on the geometrical characteristics rather than the substrate material and thickness. This feature makes FGC lines ideal for high frequency MMIC's.

Having found that in terms of loss GaAs and quartz are equivalent for the same FGC geometry, the choice of material for a substrate depends on other design criteria. If low cost is a major issue then quartz can be chosen with the active devices being flip-chip bonded to it. On the other hand if the active devices must be monolithically integrated with the rest of the circuitry, then GaAs is more appropriate with a thin overlay of polyimide for passivation. GaAs is also more suitable for applications above 120 GHz where the flip-chip

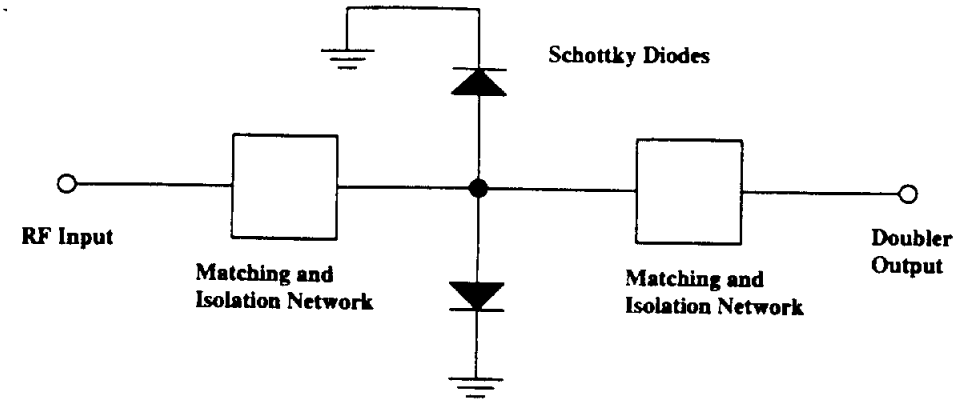


Figure 4.8: Block diagram of the doubler configuration (from F. Brauchler [2]).

bonding process increases fabrication complexity considerably.

4.3 W-Band Doublers

4.3.1 Analysis and Design

The configuration of the multiplier designs was based on two parallel Schottky barrier diodes that give very good efficiency and output power, as shown by Brauchler [2]. As can be seen in Fig. 4.8, the multipliers consisted of two Schottky diodes connected between the signal line and the ground, with appropriate matching and isolation networks at the input and output ports. The matching networks at the input and output ports provide the appropriate conditions in order to match the diode impedance at the fundamental and second harmonic, respectively, while the isolation network at the input side blocks the second harmonic and the isolation network at the output side blocks the fundamental frequency. The goal was to realize multipliers having diodes with input Q's of 2 and 3 and higher efficiencies than the ones presented by Brauchler [2].

A nonlinear multiple reflection program that includes velocity saturation, forward conduction and avalanche breakdown, modified from the code described by East et. al. [81] was

used to design the multipliers. The varactor diode is usually specified and the multiplier is designed around it in conventional multiplier design. In this work, the diode parameters become part of the design process; the operating frequency sets the doping level, and the peak RF voltage swing limited by the breakdown voltage set the active epitaxial layer width. Multiplier operation varies from a resistive mode where the current is dominated by conduction current, to a reactive or varactor mode where the current is dominated by the pumping of the depletion layer capacitance. The diode input Q is a measure of the operating mode. Resistive or low Q multipliers have modest efficiencies and wide bandwidths, while reactive multipliers have higher efficiencies and smaller bandwidths. The impedances in high Q circuits are more sensitive to small variations in the dimensions of the lines in the experimental circuits. High Q multipliers also have a larger RF voltage swing across the active device than a lower Q multiplier, for a given available pump power. This limits the pump power in high Q multipliers [81].

Waveguide multipliers can be designed for higher Q, with modest differences in the design vs. realized impedances adjusted with tuners and backshorts. Similar impedances in an MMIC multiplier are fixed, with the bias point being the only available "tuning". The multiple reflection code was modified to adjust the diode area and bias so that the required embedding impedances could be realized for designs with diode input Q's of 2 and 3. The Q=2 diodes had an epitaxial layer doping of $10^{17}/cm^3$, a thickness of 4000 $\AA$ and an area of 75 μm^2 per diode with a bias tuning voltage of -3.0 V , whereas the Q=3 diodes had an area of 66 μm^2 per diode with a bias tuning voltage of -6.0 V. It should be noted here that there is no fundamental difference between the Q=2 and Q=3 diodes (areas are almost the same) , except for the bias voltage. This can be explained from the fact that $Q \propto 1/R_dC_d$ (R_d and C_d are the diode resistance and capacitance, respectively) and, thus, increasing the Q

requires a smaller R_dC_d product. Since R_d has a modest variaton with the bias voltage and C_d has a much larger one, increasing the applied voltage yields a smaller capacitance C_d and therefore a larger Q [82]. For the multiplier reflection program the series resistance of either diode was assumed to be 2 Ω, which is slightly higher from $R_S = 1.45\Omega$ that equation 1.19 yields for a diode with a 9.6 μm diameter (73 μm^2 area) and the epi layer-parameters mentioned before. The zero bias junction capacitance can be found from equation 1.5 and is 79 fF for the Q=2 diode and 69 fF for the Q=3 diode. The calculated single diode input impedance was 52.3-j100 Ω and 52.4-j160.8 Ω for the Q=2 and Q=3 diode, respectively, at the fundamental frequency. The diode output impedance was 41.2-j56 Ω for the Q=2 diode and 50.4-j96 Ω for the Q=3 diode, at the second harmonic. The reflection program also gave an efficiency of 34% for the Q=2 multiplier and 39% for the Q=3 multiplier.

Once the diode input impedances have been calculated, the passive circuitry that will provide the appropriate matching and isolation can be designed with the help of *Libra*. For simulation purposes the diodes were assumed to be a series combination of a resistor and a capacitor with values found from the known impedances. The design of the multipliers was based on 50 Ω FGC lines at the input and output ports, a second harmonic trap at the input side and a fundamental trap at the output side. High impedance line sections that acted as inductors, connected the main line of the multipliers to the diodes in order to cancel out their average capacitance. A block diagram of the passive circuitry with the diodes can be seen in Fig. 4.9. For a 40 to 80 GHz doubler, the trap at the input side consisted of a $\lambda_g/4$ open stub at 80 GHz connected in parallel with a $\lambda_g/4$ section of line at the same frequency. This combination of $\lambda_g/4$ segments of line, imposes an open for the 80 GHz signal looking towards the input side at the point were the inductive lines are connected to the main 50 Ω line. Similarly, at the output a $\lambda_g/4$ open stub at 40 GHz was connected in parallel with a

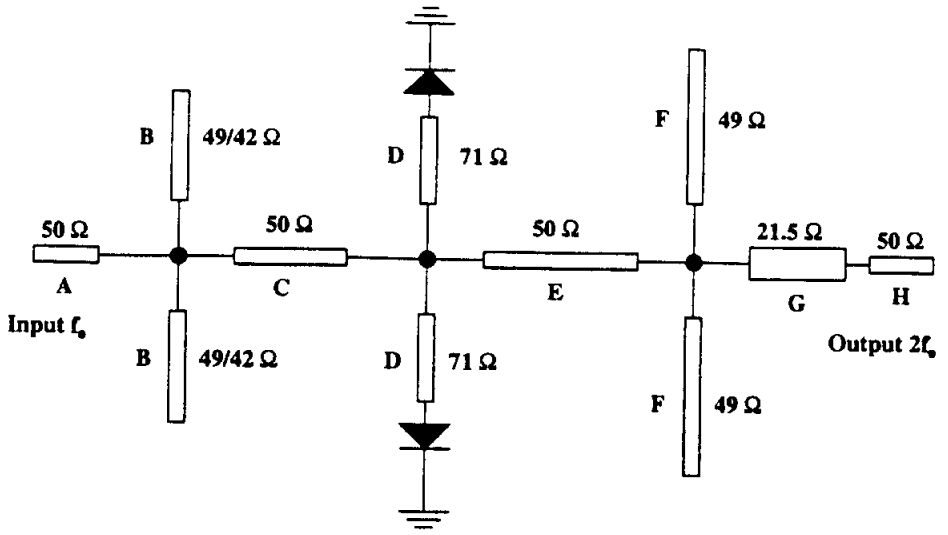


Figure 4.9: Multiplier configuration with passive circuits.

$\lambda_g/4$ section of line at 40 GHz, in order to block the fundamental frequency signal. A low impedance section was also used at the output side in order to match the relatively low real part of impedance of the parallel combination of the two diodes.

The lengths of the different FGC line sections were calculated with *Libra*, where the diodes were modeled as a resistor in series with a capacitor and the line segments were modeled as ideal transmission lines with known characteristic impedance, attenuation and effective dielectric constant. The dimensions of the 50 Ω line were w=50 μm, s=45 μm, w_g = 160μm and correspond to a higher order mode cut-off frequency of approximately 180 GHz. For FGC line sections other than the 50 Ω, the properties and geometrical characteristics can be found in [2]. The purpose of each simulation was to optimize matching of the diodes both at the input and output, while at the same time optimize the blocking capability of the traps. Results for the Q=2 and 3 multipliers are summarized in Tables 4.2 and 4.3, respectively.

When the lengths of the different FGC line sections were determined, the harmonic balance test bench of *Libra* was used to evaluate the efficiency of the multipliers. A schematic

Section	Section Description	w (μm)	s (μm)	Length (μm)
A	50 Ω signal launch structure	50	45	500
B	49 Ω open-end balanced stub	20	20	331
C	50 Ω standard section	50	45	375
D	71 Ω diode feed lines	20	80	210
E	50 Ω standard section	50	45	709
F	49 Ω open-end balanced stub	20	20	709
G	21.5 Ω low impedance section	120	10	300
H	50 Ω signal launch structure	50	45	500

Table 4.2: Geometrical characteristics for the Q=2 multiplier.

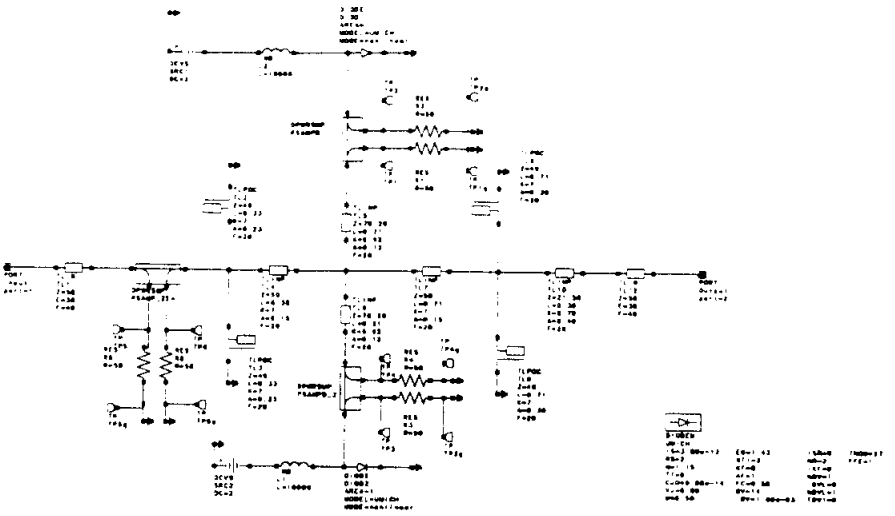
Section	Section Description	w (μm)	s (μm)	Length (μm)
A	50 Ω signal launch structure	50	45	500
B	42 Ω open-end balanced stub	50	19	346
C	50 Ω standard section	50	45	360
D	71 Ω diode feed lines	20	80	268
E	50 Ω standard section	50	45	702
F	49 Ω open-end balanced stub	20	20	682
G	21.5 Ω low impedance section	120	10	307
H	50 Ω signal launch structure	50	45	500

Table 4.3: Geometrical characteristics for the Q=3 multiplier.

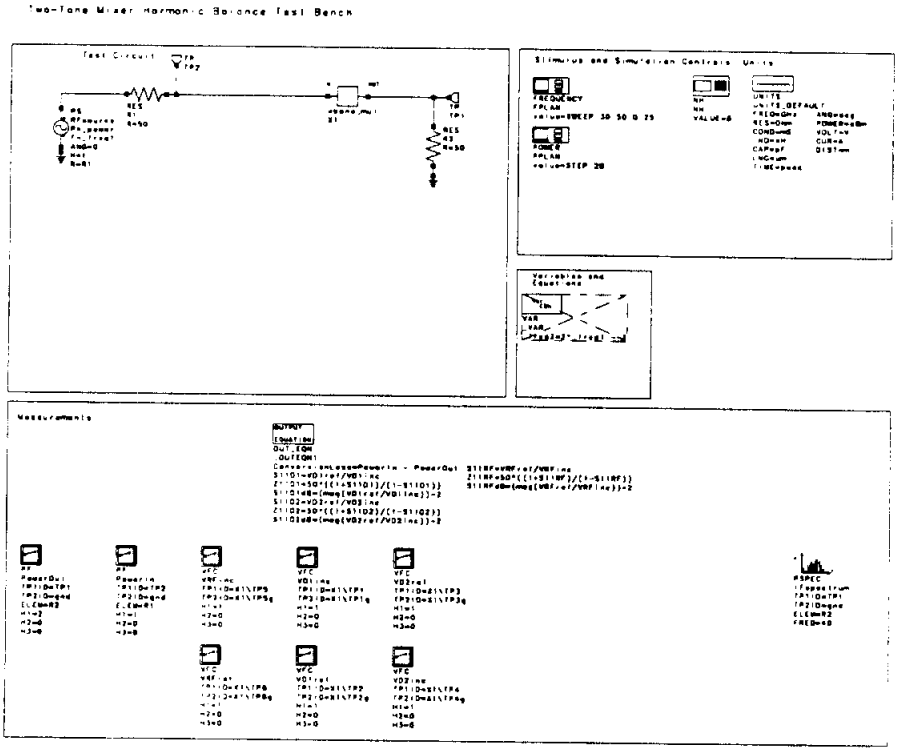
of the test bench can be seen in Fig. 4.10. For this analysis, the Schottky diodes were modeled with their DC parameters (series resistance, zero-bias capacitance, ideality factor and reverse leakage current). Optimum results can be seen in Fig. 4.11, where the Q=2 multiplier yields an efficiency of 20.5% and a bandwidth of 23% (9 GHz) at 39.7 GHz for an input power of 20 dBm and a bias of -2.5 V, while the Q=3 multiplier gives an efficiency of 26% and a bandwidth of 14% (5.5 GHz) at 38.7 GHz for an input power of 17 dBm and a -5 V bias. The efficiencies are lower than the ones given by the multiple reflection program since *Libra* accounts for the losses in the passive circuits as well as any possible mismatches between the diode impedances and the rest of the circuitry. Simulating the Q=2 and Q=3 multipliers without any loss in the various line segments yields an efficiency of approximately 32% and 40%, respectively, for the same bias and diode parameters that were used in the previous simulations.

4.3.2 Measurement System

The system that was used to evaluate the performance of the W-band multipliers can be seen in Figs. 4.12 and 4.13, and consists of two different sub-systems at the input and output sides. More specifically, at the input the HP8510C network analyzer drives the 26-40 GHz mm-wave source module that is connected to a Travelling Wave Tube (TWT) via an attenuator. The attenuator helps control the output power level of the TWT that provides more power at the input of the multipliers in order to get as much efficiency as possible. The output of the TWT is connected to a waveguide system that includes mixers, isolators and attenuators needed for the measurement of the return loss via the analyzer, as well as a 20 dB coupler that is connected to a power meter used for sampling the power provided by the TWT at its output port. The waveguide system is followed by a waveguide-to-coax

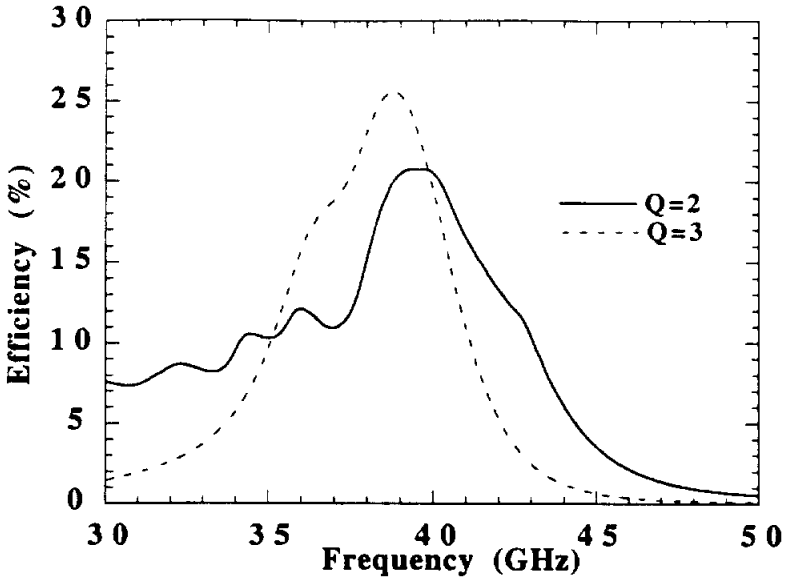


(a)

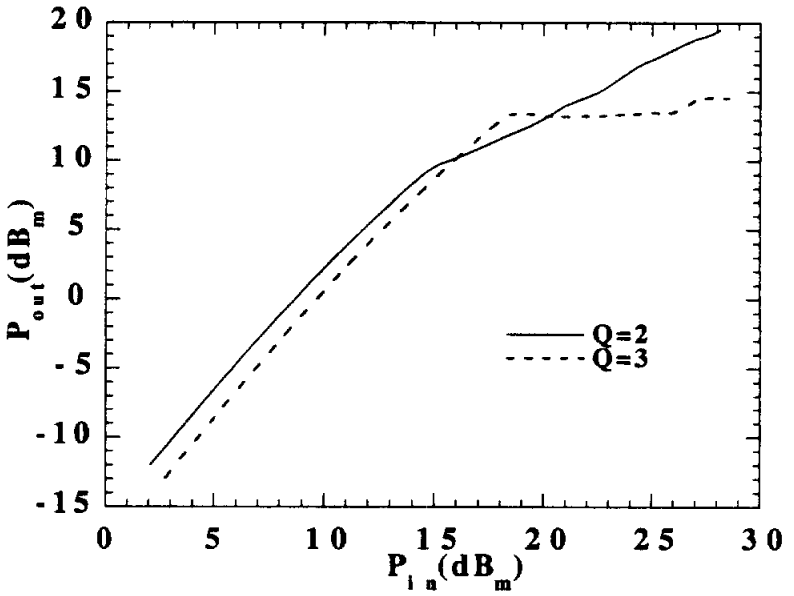


(b)

Figure 4.10: Libra simulation for the W-band multipliers: (a) circuit schematic and (b) harmonic balance analysis test bench.



(a)



(b)

Figure 4.11: Simulation results for the W-band multipliers: (a) efficiency vs. input frequency with an input power of 20 and 17 dBm for Q=2 and 3, respectively and (b) output power vs. input power at f=39.7 and 38.7 GHz for Q=2 and 3, respectively.

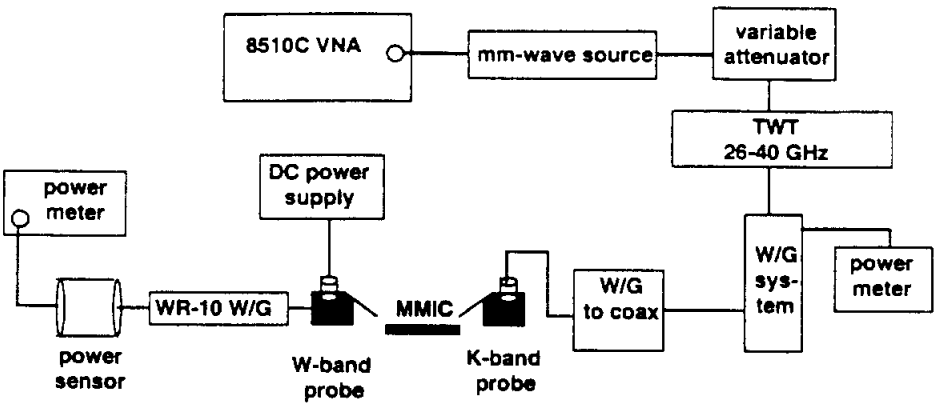


Figure 4.12: Block diagram of the measurement system used to evaluate the performance of W-band doublers.

transition, a coaxial cable and a K-band 150 μm pitch GGB industries probes. The sub-system at the output side consists of a W-band 150 μm pitch probe with a bias-tee that is connected to a long piece of WR-10 waveguide. A DC power supply is connected to the bias tee of the probe with the help of a coaxial cable and is used to reverse bias the Schottky diodes. The output of the WR-10 waveguide is connected to a power sensor from 60-90 GHz followed by a power meter that measures the output power. The combination of the two sub-systems limits the output measurement frequency range from 60 to 80 GHz.

In order to measure the efficiency of the multipliers the losses introduced by the different components must be found so that they can be de-embedded from the measured data. In addition, for return loss measurements the sub-system at the imput needs to be calibrated with one of the known calibration techniques. The losses of the various components are measured first with the HP8510C analyzer. For the input side the system is calibrated at the waveguide flange just before the W/G-to-coax transition with the help of a short, an offset short and a load. Once this is done, the transiton with the cable and the probe are connected. The loss introduced by these three components is evaluated by measuring a planar short, open and 50 Ω load standard at the end of the probe tips. Assuming that

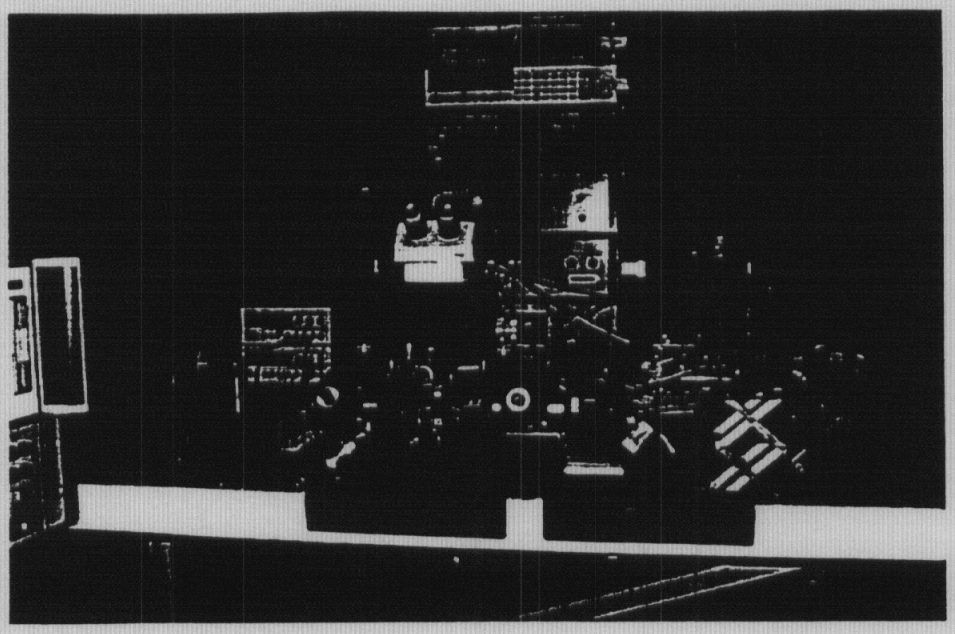


Figure 4.13: Photograph of the actual system that was used for the multiplier measurements.

the three components constitute a system with unknown S-parameters S_{11},S_{22} and S_{21}, measuring the return loss of the three standards yields a system of three equations with three unknowns:

$$S_{11} = \Gamma_{load} \tag{4.1}$$

$$S_{22} = \frac{2\Gamma_{load} - \Gamma_{short} - \Gamma_{open}}{\Gamma_{short} - \Gamma_{open}} \tag{4.2}$$

$$S_{12} = S_{21} = (S_{22} - 1)(\Gamma_{load} - \Gamma_{open}) \tag{4.3}$$

When this system is solved, the loss (i.e. S_{21} when S_{11},S_{22} are below 10 dB) for the input side is found to be about 5.8±0.3 dB from 35 to 40 GHz. Similarly, for the output system the loss is found to be approximately 3 dB.

Once the losses have been found for each frequency point, they can be de-embedded and the input power can be referenced at the end of the probe tips. Similarly, the losses at the output are extracted and the power at the end of the MMIC doubler can be found.

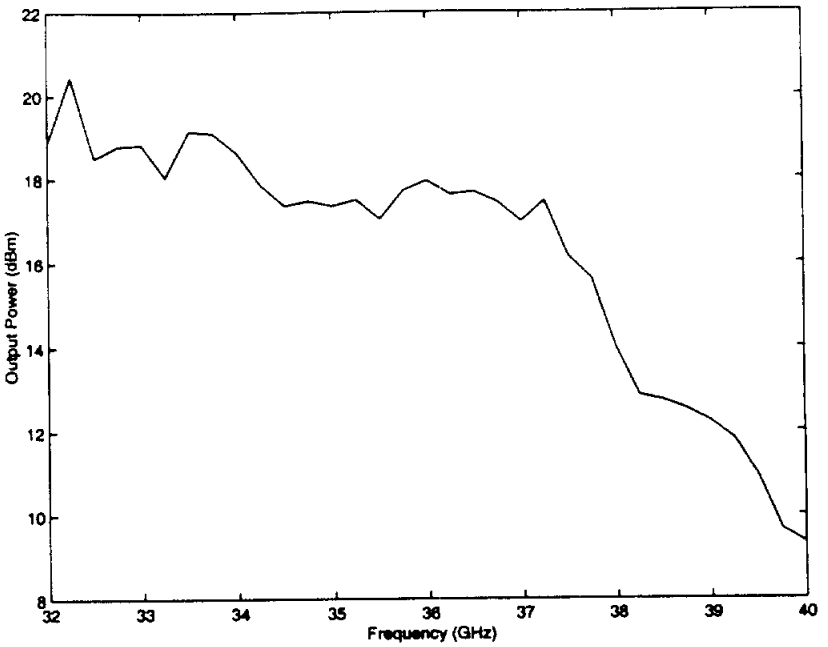


Figure 4.14: Output power vs. frequency of the TWT measured at the flange of the waveguide system for a fixed position of the attenuator.

Knowing both the input and the output power at the two ends of the multiplier allows us to evaluate the efficiency over the entire measured frequency range.

Regarding the measurement of the return loss, the system is calibrated with the help of a one port Short-Open-Load calibration. Since the return loss will be measured with a relatively high input power drive and is also dependent on the frequency response and impedance of the TWT, the output power of the TWT versus frequency is measured first. The input system is calibrated at the waveguide flange and the attenuator is set at a certain position. A second power meter connected to the flange measures the power at that point and the results are shown in Fig. 4.14. From Fig. 4.14 it is clear that the output power of the TWT decreases as the frequency increases in a non-linear way. In order to make, therefore, measurements with a constant input drive the attenuator needs to be adjusted accordingly.

In order to make a return loss measurement versus frequency at a constant input power

level, the frequency range of interest is divided into 3 sub-regions with the criterion that at each sub-region the output response of the TWT will not change a lot (no more than 2 dB). This is necessary because the TWT has a different impedance for different power levels and calibrating the system at a particular power, where the impedance has a certain value, does not guarantee that the correct return loss will be measured at a different power and impedance since the system will have changed. The first sub-region is from 34 to 37.5 GHz, where the power of the TWT is almost constant, and the attenuator is set to provide 20 dBm of input power at 36.25 GHz. The second sub-region is from 37.5 to 38.5 GHz and the attenuator is set to provide the desired power level at 38 GHz, while the third one is from 38.5 to 40 GHz and the reference frequency for the attenuator is 39.25 GHz. Calibrating each sub-region one at a time with the attenuator set to provide a desired input power to the doubler (in this case 100 mW) at the center of the band, ensures that the necessary adjustments to the attenuator value that are required to maintain the desired power level for each frequency point of the band will not affect greatly the calibration coefficients and alter the measured data. In this way, the measurement of the return loss can be done automatically with the help of the HP8510C network analyzer.

4.3.3 Results and Discussion

The Q=2 and Q=3 multiplier circuits, designed for an 80 GHz output frequency, were printed on a semi-insulating GaAs wafer after the doped active layer was etched away (for details on fabrication see appendix B). The total metal thickness of the passive circuits was $1\mu m$, which for a 50 Ω line (w=50 μm, s=45 μm, w_g=160 μm) yields a loss of 1.55 dB/cm at 40 GHz and 2.32 dB/cm at 80 GHz. A picture of the fabricated Q=3 doubler can be seen in Fig. 4.15, while an SEM photo of the Schottky diode can be seen in Fig. 4.16. The

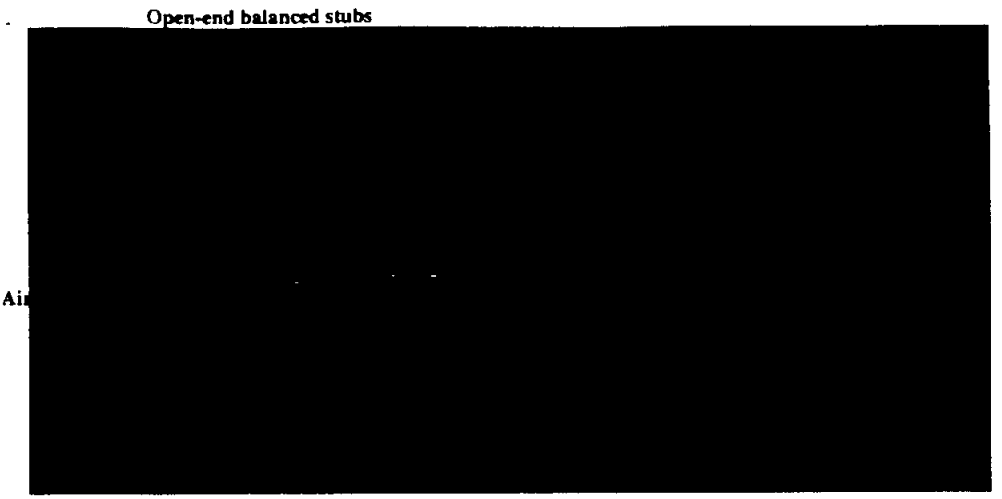


Figure 4.15: Fabricated Q=3 W-band doubler.

DC characteristics of the diodes were measured with an HP4155A semiconductor parameter analyzer and an HP4285A precision LCR meter. The doping profile of the wafer used for the fabrication of the doublers was extracted by measuring the C-V characteristic of a test diode with 220 μm anode diameter, and is shown in Fig. 4.17. As can be seen, the doping density is almost constant and equal to $1.1\text{x}10^{17}/cm^3$ which is very close to the $1\text{x}10^{17}/cm^3$ value quoted by the manufacturer. The built-in voltage potential was also calculated from the capacitance measurement of the test diode to be $V_{bi} = 0.95V$.

The measured C-V characteristics of the Q=2 and Q=3 fabricated diodes are shown in Fig. 4.18, where the actual data are curve fitted to an equation of the form

$$C_t = C_p + \frac{C_{jo}}{\sqrt{1 - \frac{V}{0.95}}} \tag{4.4}$$

where C_t, C_p, C_{jo} are the total, parasitic and zero-bias capacitances , respectively. After curve fitting with equation 4.4, the parasitic and zero-bias capacitances for the Q=2 diode were found to be 19 and 98 fF, respectively.

Results for the Q=2 and Q=3 diodes are summarized in Table 4.4, where we observe

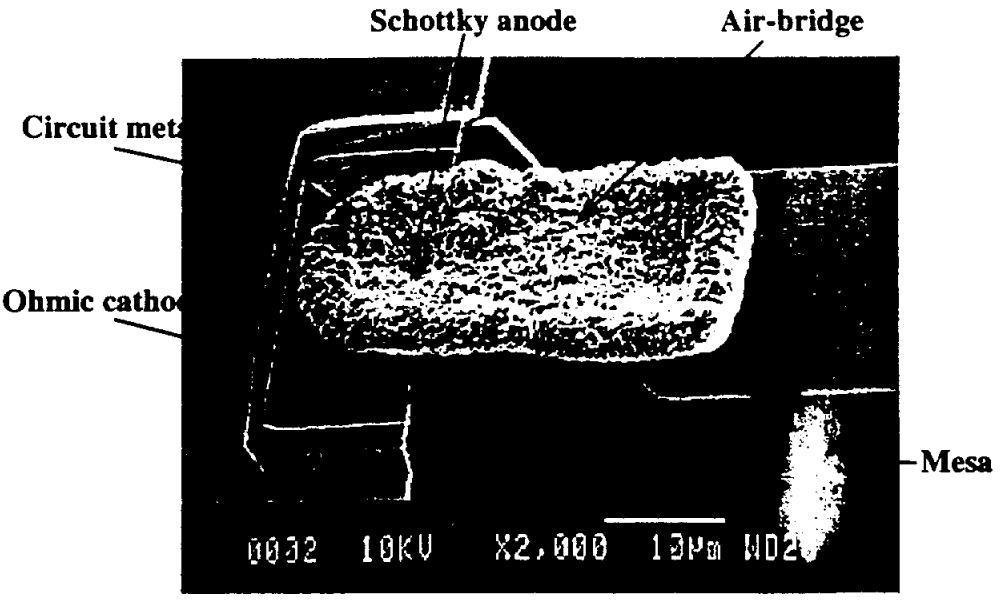


Figure 4.16: SEM photo of fabricated Schottky diode.

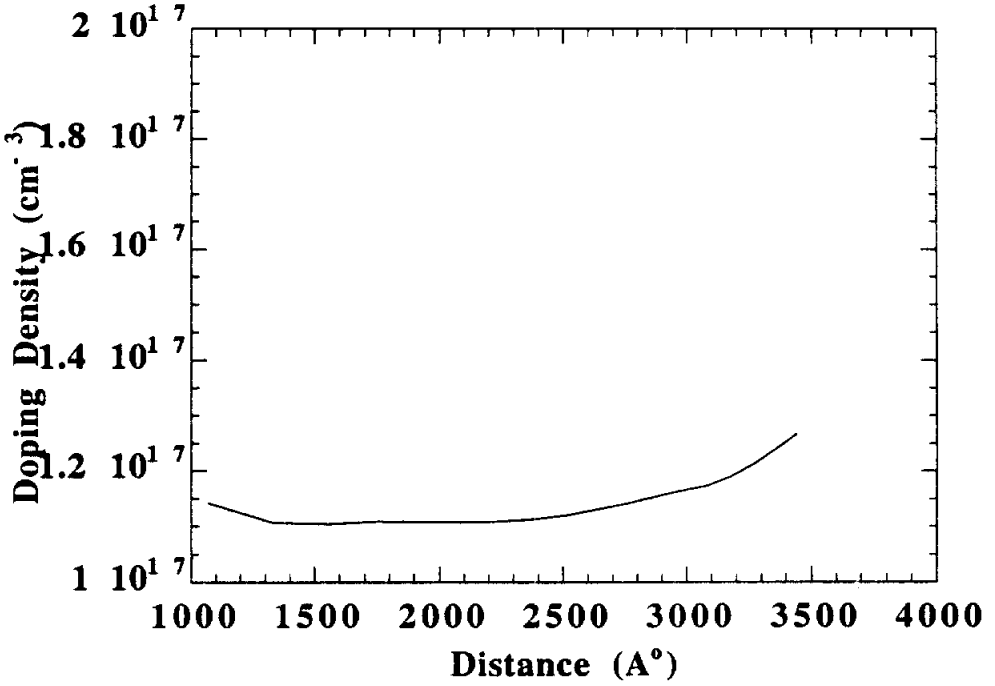


Figure 4.17: Doping profile for the wafer used to fabricate the W-band dou[illegible]s.

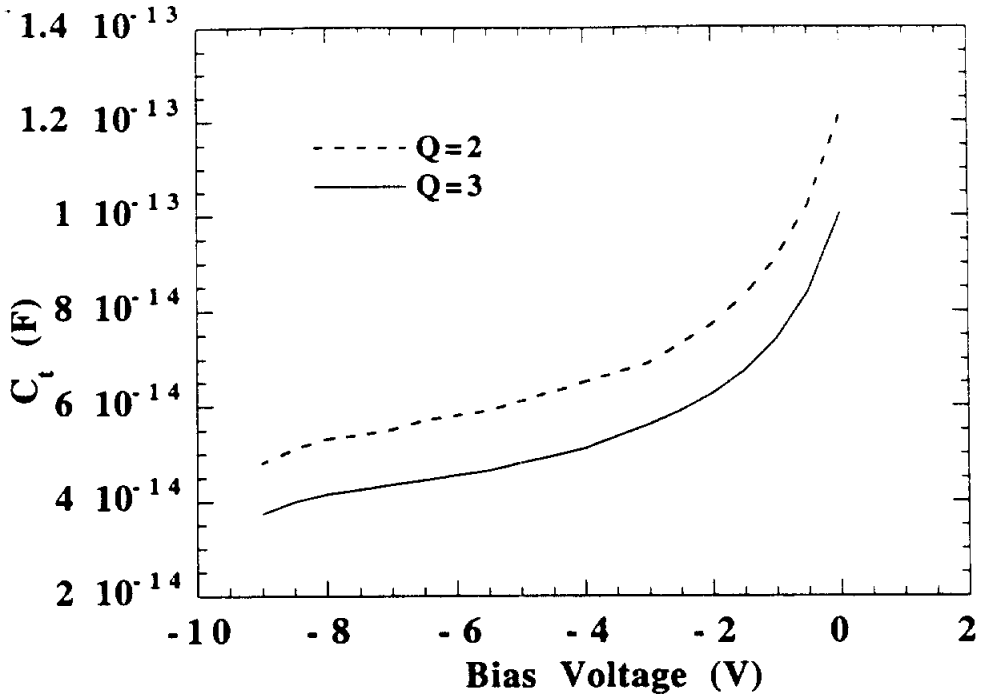
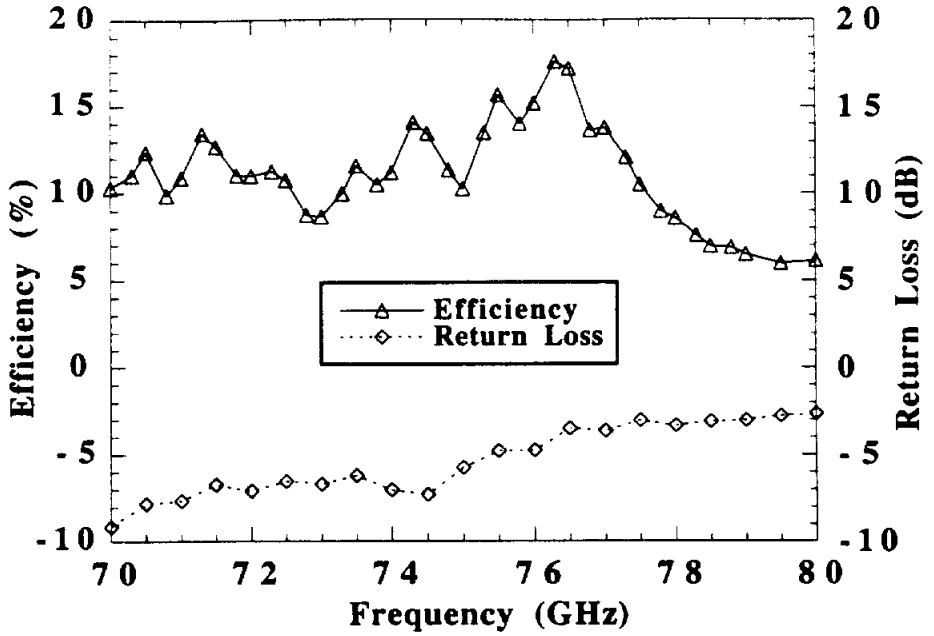


Figure 4.18: Total capacitance vs. bias voltage for the Q=2 and Q=3 diodes.

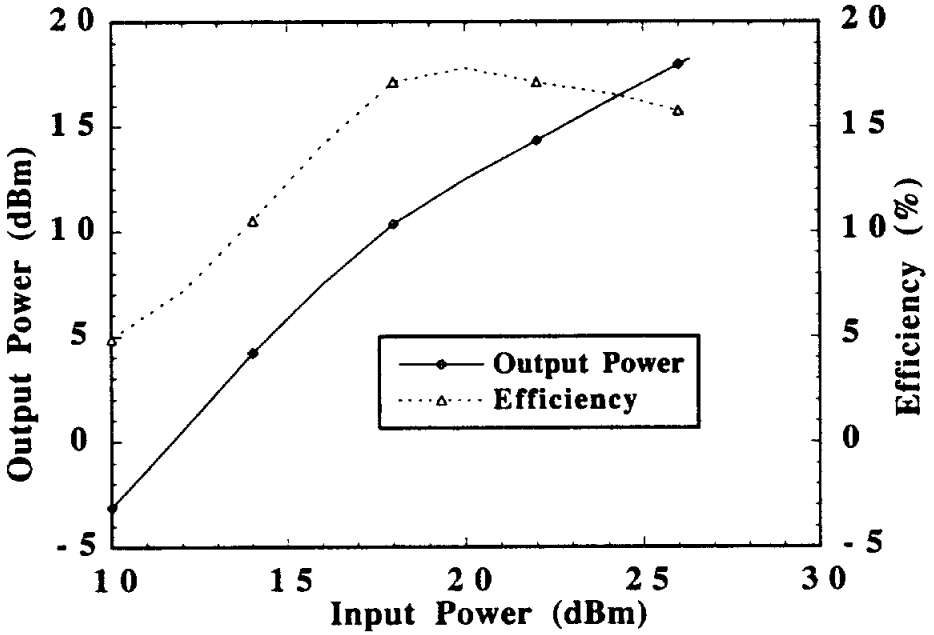
that the zero-bias capacitances are a bit higher than the ones expected for both diodes. This is due to fabrication tolerances in the mask making process that resulted in diode diameters larger by 1.2 μm than the ones anticipated. For the parasitic capacitances an electrostatic simulation of the anode area, the ohmic and the air-bridge in *Maxwell* [83] yields a value around 10 fF. An additional 1-2 fF are expected from the parasitics between the air-bridge and the high-doped n^+ layer. The ratio of the maximum over minimum capacitance, C_{max}/C_{min}, for the Q=2 and 3 diodes ranged from 2.5 to 2.7.

Diode input Q	$R_S(\Omega)$	C_{jo} (fF)	C_p (fF)	η	I_o (fA)	V_{BR} (V)	f_C (GHz)
2	2.2	99	19	1.16	180	-11.8	614
3	2.2	88	13	1.15	185	-11.8	717

Table 4.4: Measured DC characteristics for the W-band fabricated diodes.



(a)



(b)

Figure 4.19: Measured results for the Q=2 doubler: (a) efficiency and return loss vs. frequency for an input power of 20 dBm and (b) output power and efficiency vs. input power at 76.3 GHz.

Measured results for the Q=2 doubler are presented in Fig. 4.19(a) where we observe that a peak efficiency of 17.2% was achieved at 76.3 GHz and a -3.5 V bias with a return loss of -4.5 dB and a -3 dB bandwidth of at least 10% (8 GHz). We should note here that for each frequency point the bias was optimized for maximum efficiency. A comparison between the measurements and the *Libra* simulations of Fig. 4.11(a) reveals a shift in the optimum frequency, that is due partly to the higher junction capacitance which is a result of the enlarged fabricated diode and partly to the parasitic capacitance. The 17.2% measured efficiency is in good agreement with the predicted *Libra* value of 20%. A *Libra* simulation that includes the parasitic capacitance of 19 fF yields an efficiency of approximately 17%, as can be seen in Fig. 4.20, verifying the fact that parasitics tend to degrade the diode performance and overall circuit efficiency. If we account for the 1.5 dB circuit loss at 76 GHz and the -4.5 dB return loss then the de-embedded efficiency becomes 36.5% which is a bit higher than the 34% value calculated by the multiple reflection program. The small discrepancy can be attributed to the sensitivity in the measurement of the return loss for different bias voltages. The ripple that is present in the efficiency measurement is partly due to the coaxial cable of the system set-up and partly to the different bias voltage used at each frequency point for maximum output efficiency (measurements with a waveguide part instead of a coaxial and at a nearly constant voltage level are much smoother as it will be shown in the next section). The suppression of the fundamental frequency measured at the output of the multiplier with the HP8510C was -18 dB. Figure 4.19(a) also shows that the measured return loss increases with frequency. This behavior is typical of a matching network that achieves very good matching of the diode impedance at a particular frequency, with increasing mismatching as the frequency deviates from the optimal point. The expected return loss trend for the Q=2 multiplier can be seen in Fig. 4.21, where we observe that

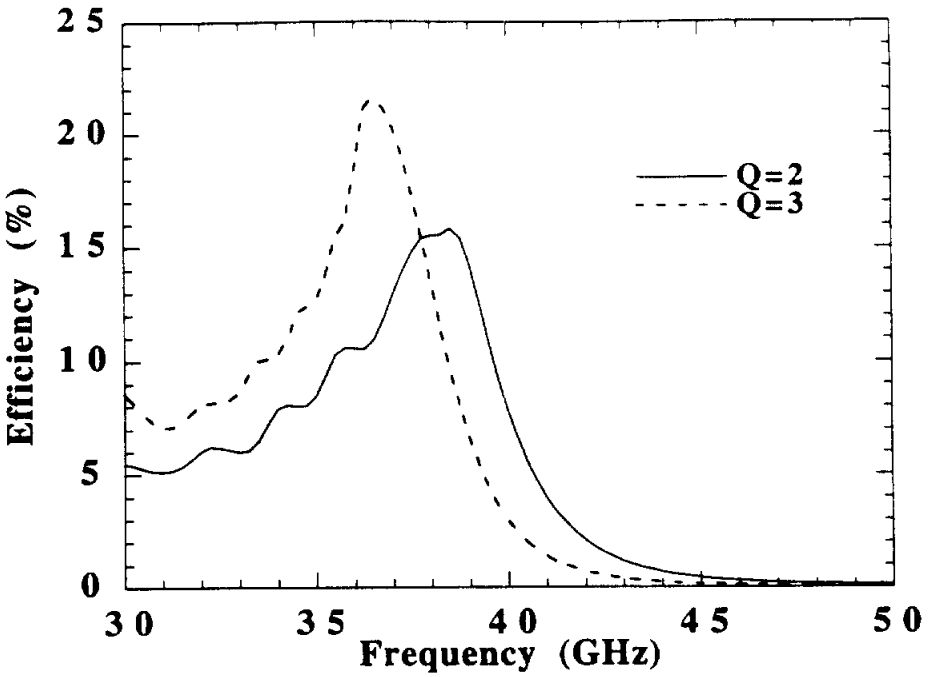


Figure 4.20: Simulated results for the Q=2 and Q=3 doublers with measured diode DC parameters and input power of 20 and 17 dBm, respectively.

a minimum is reached around 34 GHz and beyond that point the return loss increases. Figure 4.21 also reveals that increasing the bias voltage and, thus, the diode input Q tends to degrade the return loss of the multiplier (this effect will be explained later in the chapter). The output power at 76.3 GHz for a varying input power can be seen in Fig. 4.19(b), where a maximum of 66 mW was achieved for an input power of about 26 dBm. In the same figure we can also observe that the efficiency decreases for input power levels greater than 22 dBm with a final value of 15.5% at 26 dBm, due to current saturation in the diodes. The measured output power of 66 mW is in very good agreement with the 70 mW value from the simulated results. Since power availability was limited by the measurement system and the diode burn-out point, evaluation of the multiplier performance at even higher power levels was not possible.

For the Q=3 multiplier the measured results are shown in Fig. 4.22. The peak efficiency

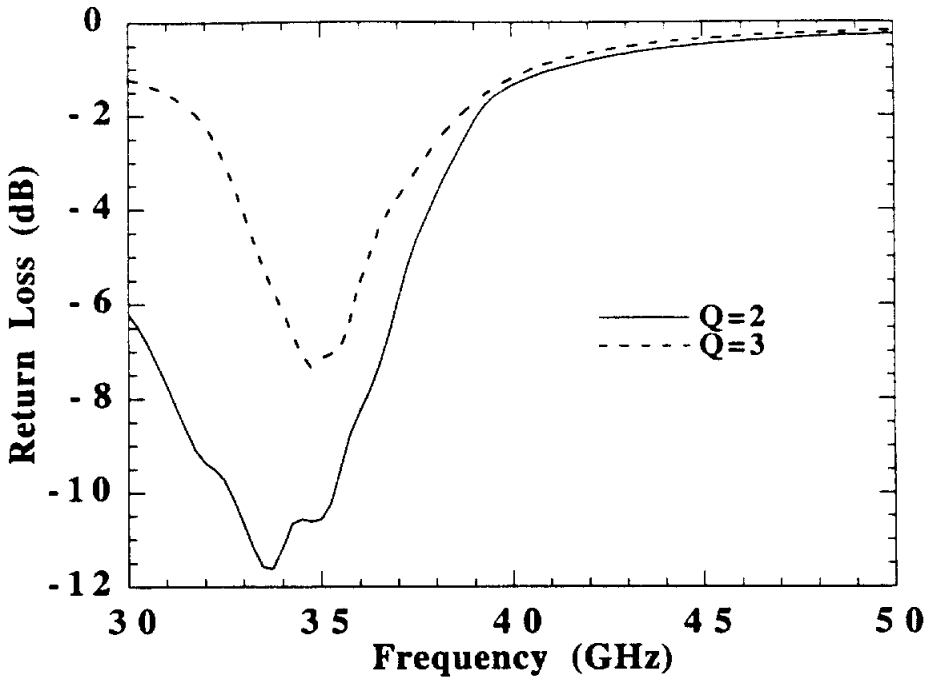
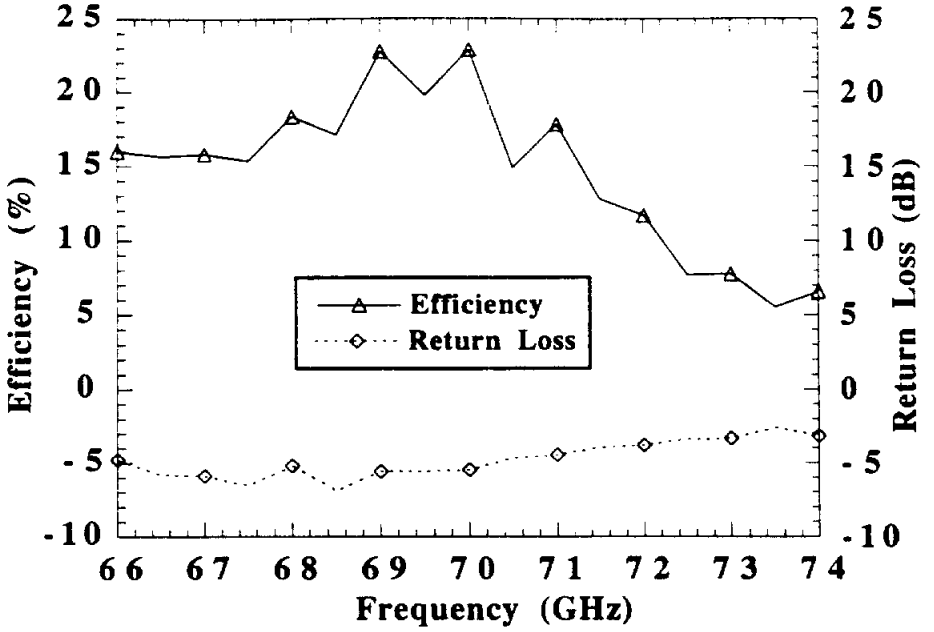
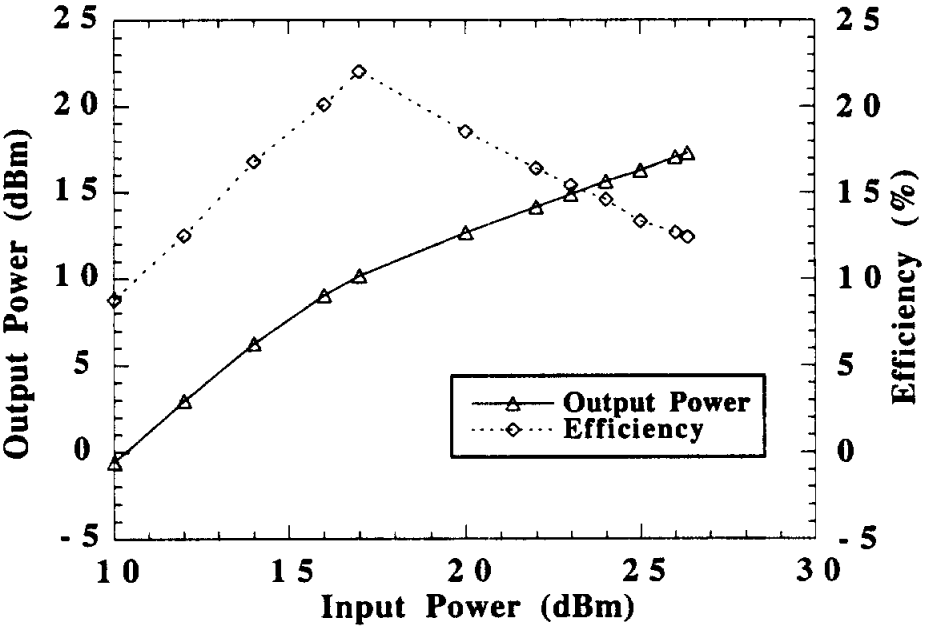


Figure 4.21: Simulated return loss for the Q=2 and Q=3 doublers with measured diode DC parameters and input power of 20 and 17 dBm, respectively.

and return loss were 22.0% and -5 dB, respectively, at 70 GHz and a voltage of -5.5 V while the -3 dB bandwidth was approximately 8.5% (6 GHz). Taking into account the 0.7 dB circuit loss at 70 GHz and the -5 dB return loss, yields an efficiency of 37% which is very close to the 39% value predicted by the reflection program. In addition, the measured efficiency is in good agreement with the 25.5% *Libra* result. The lower measured peak frequency can be attributed to the larger area of the fabricated anode (25% increase) and the parasitic capacitance, as well as the increased sensitivity of the diode impedance to small variations in the dimensions of the lines which makes it more difficult to match it at a specified frequency. A re-evaluation of the doubler's efficiency in *Libra* including the parasitic capacitance of 13 fF yields a value of approximately 22% at 73 GHz, as shown in Fig. 4.20. The input power level for the Q=3 multiplier was 17 dBm, in contrast with the Q=2 multiplier where the input level was 20 dBm. For higher input power levels the efficiency of the Q=3 multiplier



(a)



(b)

Figure 4.22: Measured results for the Q=3 doubler: (a) efficiency and return loss vs. frequency for an input power of 17 dBm and (b) output power and efficiency vs. input power at 70 GHz.

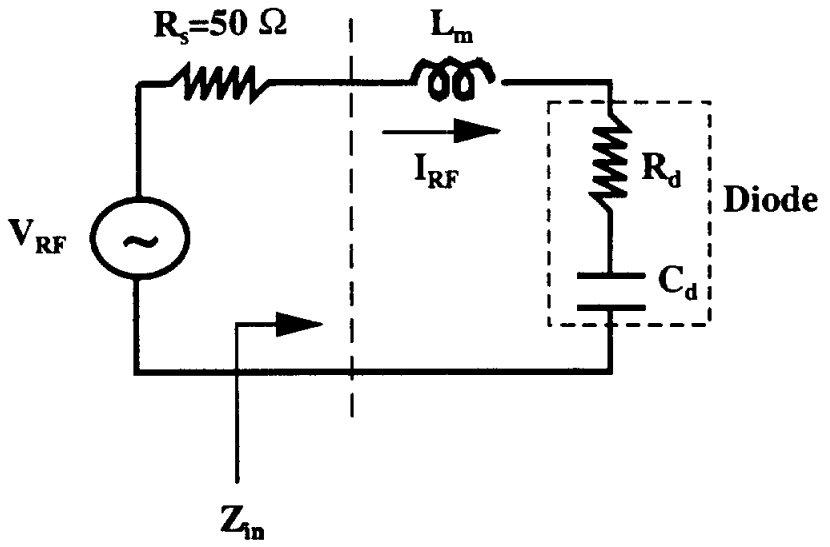
decreased significantly; a 15% value was measured at 24 dBm as can be seen in Fig. 4.22(b). This is expected, since for higher Q's the RF voltage swing across the diode increases for a given available RF power, leading to increased saturation effects in the device and limiting the maximum input power before burn out. If we model the diode as a series resistor and capacitor that is connected to an RF source and a matching impedance, as shown in Fig. 4.23(a), then it is possible to deduce an equation for the voltage accross the diode [82]. The diode Q at the input frequency is $Q_d = X_d/R_d = -1/(\omega C_d R_d)$ and if we assume conjugate matching for maximum power transfer then $R_s = R_d$ and $X_m = \omega L_m = -X_d$. As a result, the current flowing in the loop is $I_{rf} = V_{rf}/(2R_d)$ and the voltage V_d across the diode can be written as

$$V_d = I_{rf} Z_d = \frac{V_{rf}}{2}(1 - jQ_d). \tag{4.5}$$

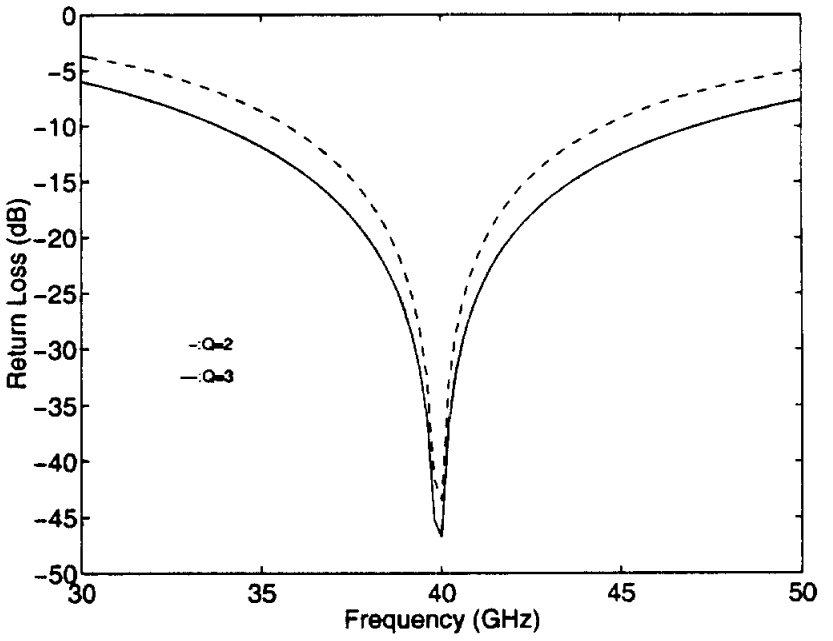
From equation 4.5 it is clear that for a given RF power the voltage across the diode increases as the input Q increases. Therefore, a higher input Q multiplier will have a larger voltage swing that will lead to increased saturation effects in the device.

A maximum output power of approximately 50 mW was measured for an input power of 400 mW. The Q=3 doubler also has a smaller bandwidth than the Q=2, since both the the diode and embedding impedances vary more rapidly with frequency, mismatching the input pump power. In order to better understand this behavior, the return loss bandwidth for an input diode Q of 2 and 3 with an impedance of 50-j100 Ω and 50-j150 Ω at 40 GHz, respectively, was evaluated based on the circuit model of Fig. 4.23(a). The reflection coefficient is given by

$$\Gamma = \frac{Z_{in} - 50}{Z_{in} + 50} = \frac{j(\omega L - \frac{1}{\omega C})}{100 + j(\omega L - \frac{1}{\omega C})} \tag{4.6}$$



(a)



(b)

Figure 4.23: Theoretical analysis for the diode bandwidth: a) equivalent circuit model and b) results based on equation 4.6.

where $L = \frac{1}{\omega^2 C}$ for $\omega = \omega_{match}$. If we plot the amplitude of the reflection coefficient for the Q=2 and 3 diodes used to design the multipliers, then from Fig. 4.23(b) we observe that the -10 dB bandwidth for the Q=2 case (12 GHz) is 1.5 times larger than the Q=3 bandwidth (8 GHz). This is in good agreement with the 1.4 bandwidth ratio that can be found from Fig. 4.20 and the 1.33 ratio of the measured results (8 GHz versus 6 GHz). Higher Q multipliers, therefore, can achieve more efficiency with less bandwidth than lower Q's, but at smaller input power levels resulting in smaller output power due to the saturation effects [82].

4.3.4 A Four Diode Design

This section presents the design, analysis and experimental results of a W-band doubler from 40 to 80 GHz with four Q=2 diodes, that can achieve higher output power. The configuration of such a doubler is similar to the one shown in Fig. 4.9, except that two diodes in series instead of one are connected at each parallel branch, and the addition of a low impedance section at the input for matching purposes (see Fig. 4.24). For the diodes, the assumption is made that each one has the same area as the diodes used in the doubler of the previous section (75 μm^2), and as a result the input impedance at the fundamental is 52-j106 Ω while the output impedance at the second harmonic is 41.2-j56 Ω. The series resistance and zero-junction bias capacitance are also assumed to be 2 Ω and 75 fF, respectively, per diode for analysis purposes.

The matching and isolation networks at the input and output side were first designed in *Libra*, where the diodes were modeled as a series combination of a resistor and a capacitor. Quarter wavelength open-end stubs were placed at the input and output that block the second harmonic and fundamental, respectively. The diodes were connected to the main

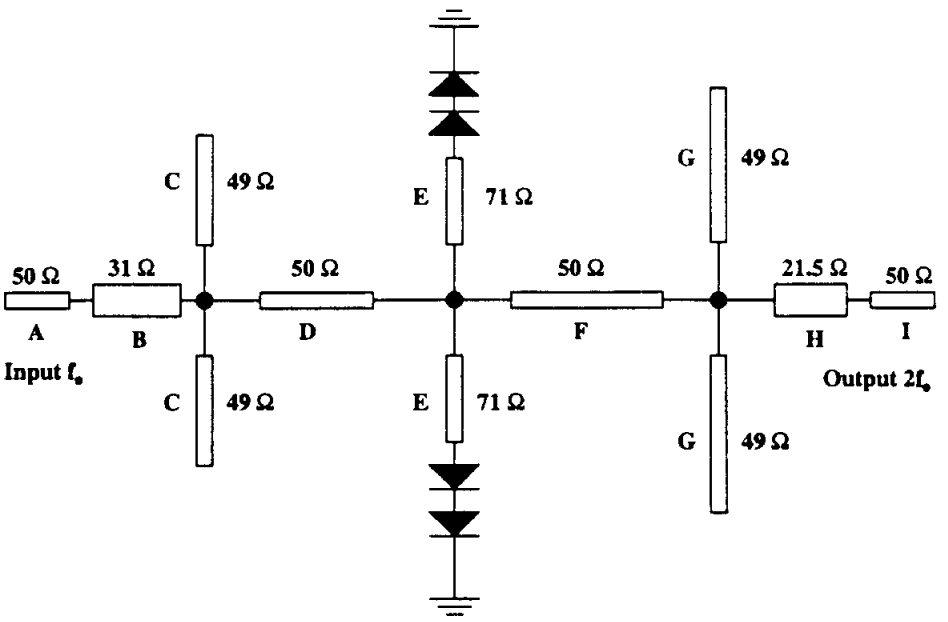
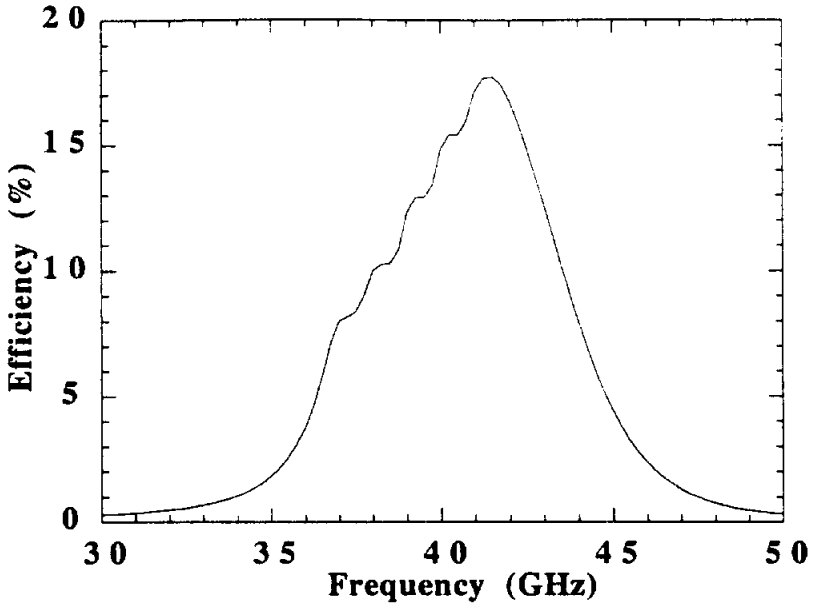


Figure 4.24: Multiplier configuration with passive circuits and four diodes.

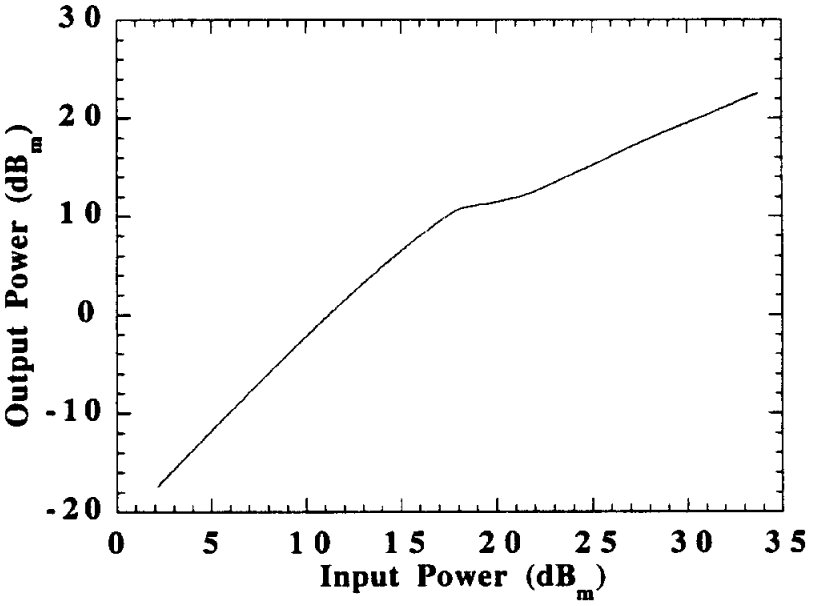
50 Ω line with high impedance inductive lines. In order to achieve a good matching at the input a low impedance section had to be inserted before the open-end stubs that trap the second harmonic. The dimensions and lengths of the various line segments, according to the schematic of Fig. 4.24, can be seen in Table 4.5.

With the lengths of the different line sections specified, the performance of the doubler was simulated in the harmonic balance test bench of *Libra*. Each diode was simulated with a pn junction model of known DC parameters (series resistance, junction capacitance, reverse leakage current etc.). Optimum results can be seen in Fig. 4.25(a), where an efficiency of 18% and a 3 dB bandwidth of 17% are achieved at 41.25 GHz for a bias voltage of -5 V, which is twice the voltage used in the two diode case. Fig. 4.25(b) also shows that an output power of 100 mW or more is feasible for an input power greater than 30 dBm.

The four diode doubler was fabricated on the same wafer that was used for the fabrication of the Q=2 and Q=3 doublers (N_d=1x$10^{17}cm^{-3}$, thickness= 4000 Å), after the active epi-layers were etched away from the diodes. A photograph of the actual doubler can be seen



(a)



(b)

Figure 4.25: Simulated results for the four diode doubler: a) efficiency vs. input frequency for an input power of 20 dBm and b) output power vs. input power at 41.25 GHz.

Section	Section Description	w (μm)	s (μm)	Length (μm)
A	50 Ω signal launch structure	50	45	500
B	31 Ω low impedance section	100	20	660
C	49 Ω open-end balanced stub	20	20	331
D	50 Ω standard section	50	45	354
E	71 Ω diode feed lines	20	80	180
F	50 Ω standard section	50	45	709
G	49 Ω open-end balanced stub	20	20	682
H	21.5 Ω low impedance section	120	10	380
I	50 Ω signal launch structure	50	45	500

Table 4.5: Geometrical characteristics for the Q=2 four diode doubler.

in Fig. 4.26, where we observe low impedance sections both at the input and the output, and a close-up of the diodes in Fig. 4.27. The diode DC characteristics were measured first and results are summarized in Table 4.6. The parasitic capacitance per diode was found to be 21.5 fF, which is a bit higher (10%) than the corresponding value of the Q=2 two diode design.

Diode input Q	$R_S(\Omega)$	C_{jo} (fF)	C_p (fF)	η	I_o (fA)	V_{BR} (V)	f_C (GHz)
2	2.5	90	21.5	1.18	240	-11.5	571

Table 4.6: Measured DC characteristics per diode for the four diode doubler design.

In order to measure the performance of the four diode doubler the system of Fig. 4.12 was reconfigured in a way that the losses of the sub-system at the input are minimized. More specifically, the coaxial cable that connected the waveguide-to-coax transition to the

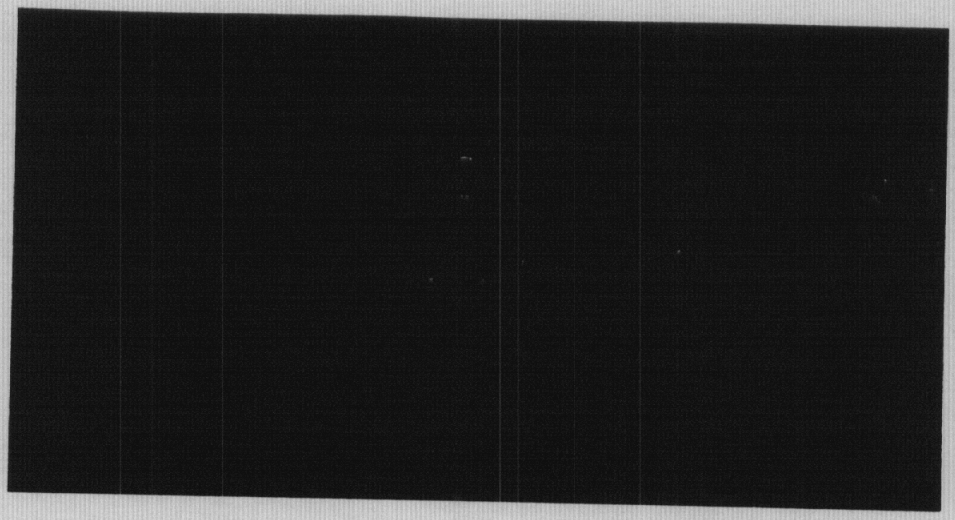


Figure 4.26: Photograph of the fabricated four diode doubler.

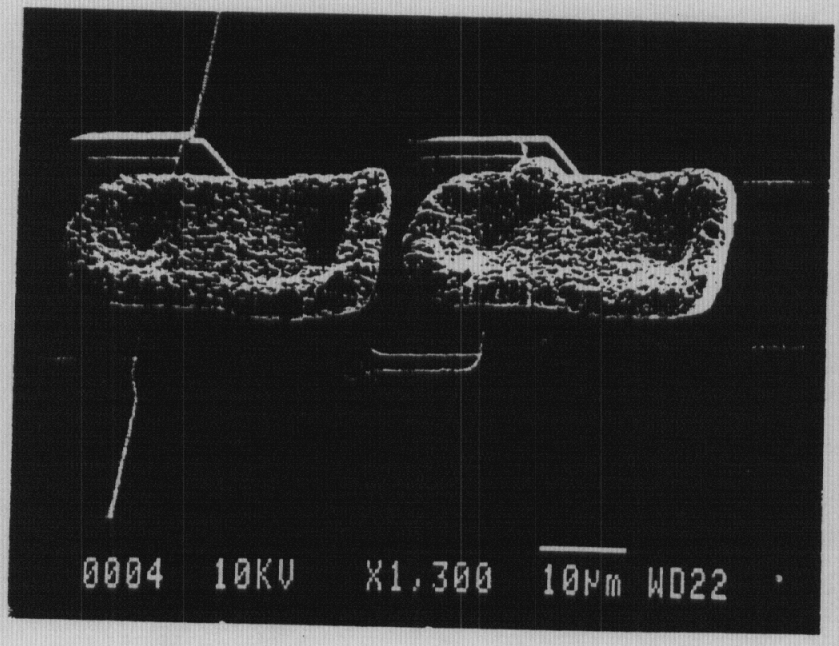
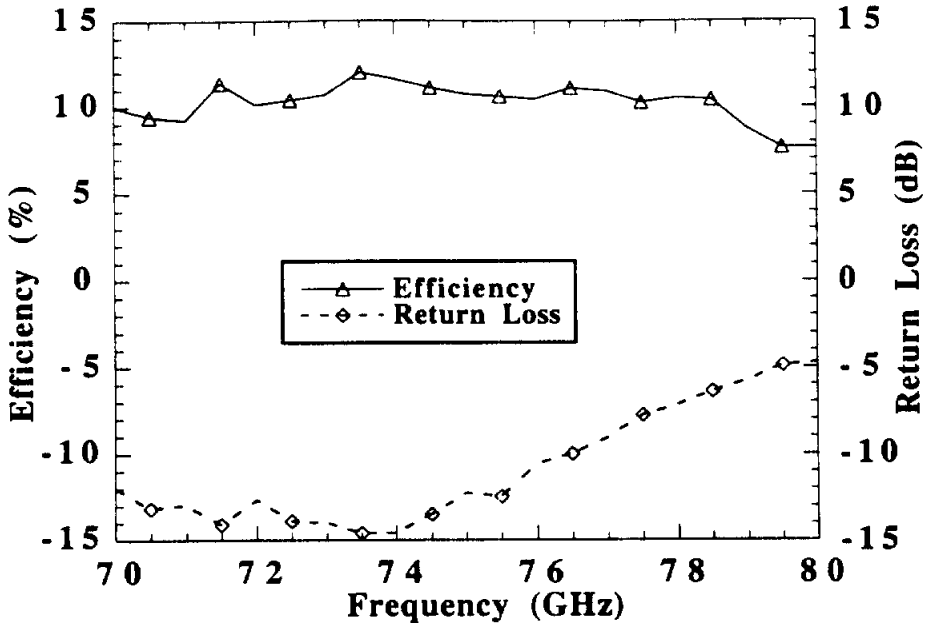


Figure 4.27: SEM photo of two diodes in series.

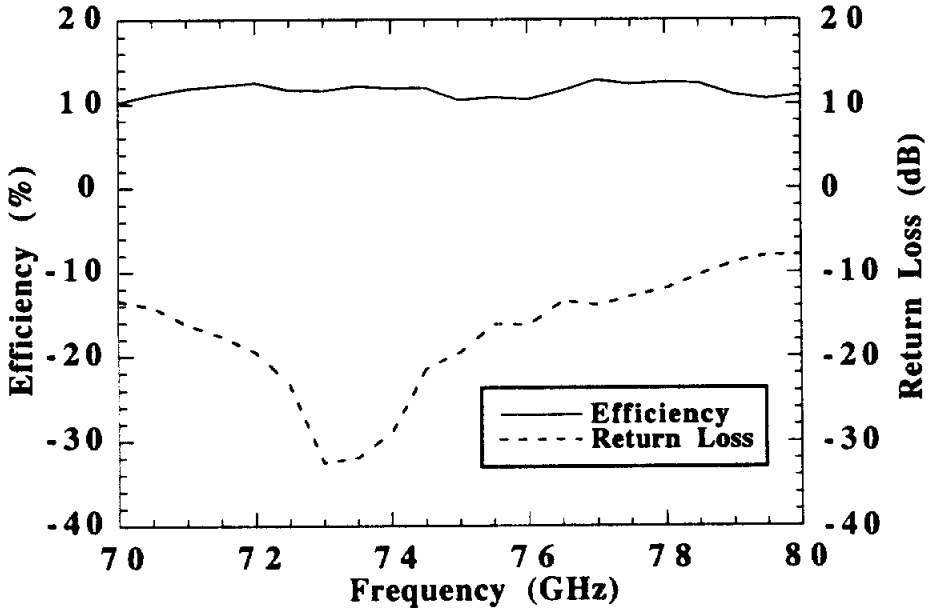
input K-band probe was replaced with WR-28 segments of waveguide. The transition was placed at the end of WR-28 segments and was connected to the GGB probe via a 3.5 mm male-to-male adaptor. With this substitution the losses of the input sub-system were found to be 3.5±0.3 dB and could allow for more available input power. In addition, a WR-10 E-H tuner was placed at the output side after the probe, so as to minimize any mismatches between the output part of the multiplier and the diode impedances. It is expected that the E-H tuner would increase the measured efficiency by a small percentage due to the improved matching conditions at the output side of the monolithic doublers.

Efficiency measurements for the doubler with the dimensions of Table 4.5 can be seen in Figs. 4.28(a), 4.28(b) for an input power of 20 and 23 dBm, respectively. Figure 4.28(a) shows that a 12.5% efficiency was achieved at approximately 74 GHz with a return loss of -15 dB and a minimum bandwidth of 12.5% for an input power of 20 dBm and a bias voltage of -3.5 V. For a 23 dBm input power and the same bias voltage the efficiency did not change significantly but the return loss became better especially for output frequencies above 76 GHz (at 40 GHz return loss went from -5 dB to -9 dB), as seen in Fig. 4.28(b). This means that pumping the four diode combination harder changes the impedances in a way that the input matching is improved, under the condition that the bias voltage does not change substantially. It should also be noted here that the E-H tuner at the output improved the power coming out of the multiplier by 5 to 10%, when compared to the measurement with no tuner.

The measured output power versus input power at 74 GHz is shown in Fig. 4.29, where an output power of 115 mW was achieved for an input of 1130 mW and a -12 bias voltage. Without the E-H tuner the output power for the same input drive was measured to be 105 mW. Both of these measured output powers are the highest reported for a monolithic



(a)



(b)

Figure 4.28: Efficiency and return loss vs. output frequency of the four diode doubler for an input power of: a) 20 dBm and b) 23 dBm.

W-band doubler. The return loss of the doubler for 1130 mW of input was approximately -10 dB, which is higher than the -30 dB value for 200 mW of input. However, at 200 mW the bias voltage is much lower (-3.5 V) than the -12 V value. Several measurements have shown that an increase in the bias of the diodes results in the degradation of the measured return loss. This can be explained from the fact that for a given passive circuit design with the stubs adjusted to match a certain device impedance, increasing the voltage will increase the imaginary part of the diode impedance and therefore deviate from the optimal matching point and deteriorate the return loss. The simulated return loss results of Fig. 4.21 corroborate this explanation, since the Q=3 multiplier that has a higher return loss is biased at a higher (more negative) voltage. A higher imaginary part, however, increases the input Q of the diode and can yield a higher multiplier efficiency. The four diode doubler design gave a higher output power than the two diode one but at a lower efficiency, since the two diodes in series can sustain much more input power before they reach the burn-out point.

A *Libra* simulation of the doubler taking into account the parasitic capacitance and a -3.5 V bias voltage, yields an efficiency of 13% at 39 GHz and 17% bandwidth (see Fig. 4.30), which are in good agreement with the measured results. Therefore, the parasitics and the lower applied voltage decrease the estimated efficiency by approximately 25% (from 18% to 13%).

4.3.5 Improved Designs

In the multiplier designs presented in the previous section, the 50 Ω parallel open end stubs had a different geometry than the standard 50 Ω line. More specifically, for the stubs w=s=20 μm while for the main 50 Ω line w=50 μm, s=45 μm. The smaller slot and center

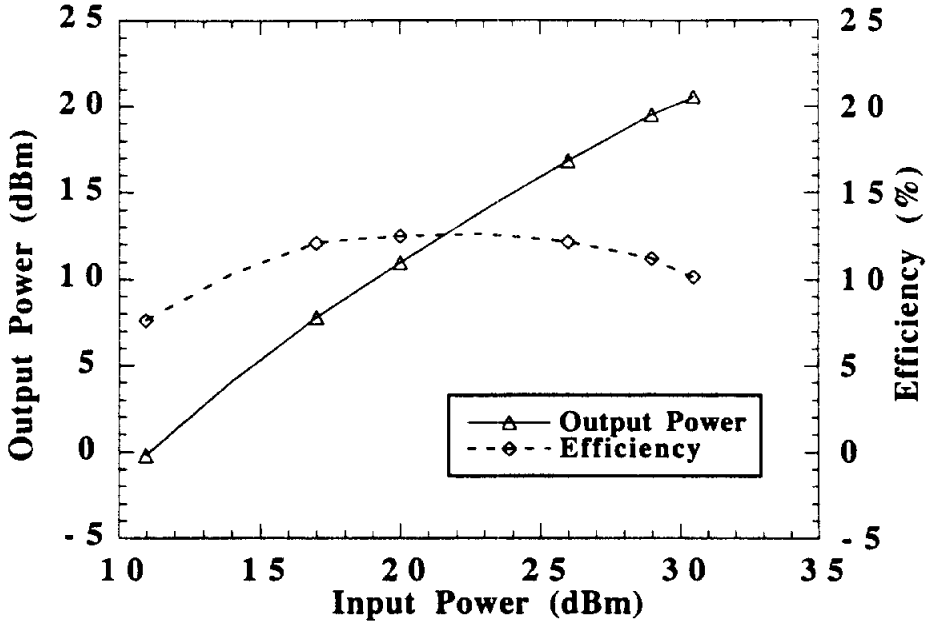


Figure 4.29: Output power and efficiency vs. input power at 74 GHz for the four diode doubler.

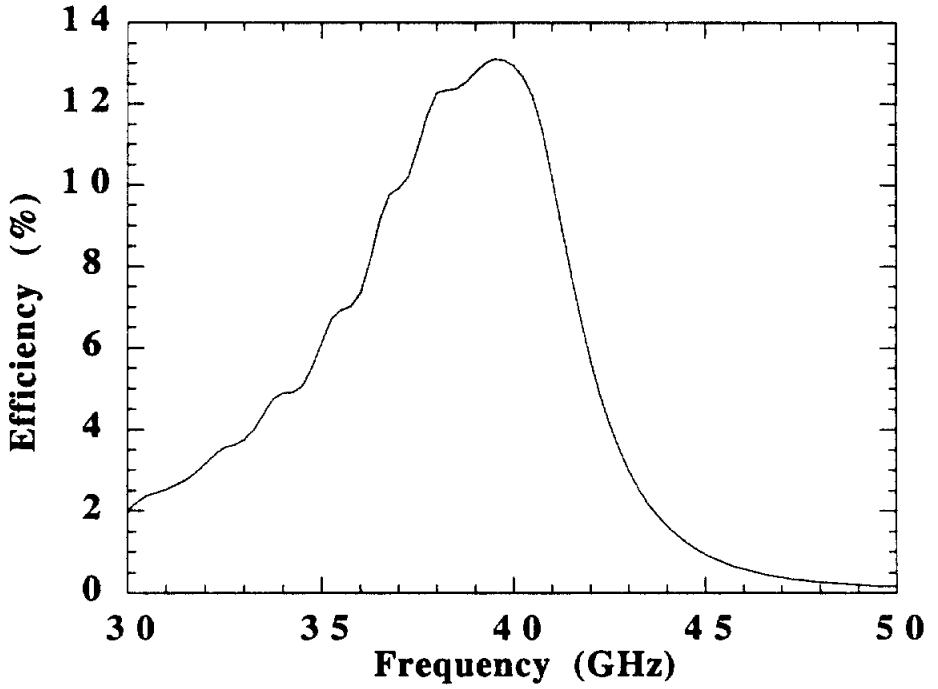


Figure 4.30: Simulation of four diode doubler including the measured diode characteristics for an input power of 20 dBm.

Section	Section Description	w (μm)	s (μm)	Length (μm)
A	50 Ω signal launch structure	50	45	170
B	50 Ω open-end balanced stub	50	45	318
C	50 Ω standard section	50	45	375
D	71 Ω diode feed lines	20	80	210
E	50 Ω standard section	50	45	694
F	50 Ω open-end balanced stub	50	45	709
G	21.5 Ω low impedance section	120	10	300
H	50 Ω signal launch structure	50	45	190

Table 4.7: Geometrical characteristics for the improved Q=2 multiplier.

conductor width increase the attenuation of the stubs to about 0.23 dB/mm at 20 GHz, when the attenuation of the regular 50 Ω line is about 0.12 dB/mm at 20 GHz, almost half the value (both lines have a metalization thickness of $1\mu m$). One way to improve the efficiency of the doublers would be to replace the shunt stubs with new ones that have wider slot and signal line widths, in an effort to reduce the ohmic loss of the circuit. From the 50 Ω FGC lines studied so far the one with w=50 μm, s=45μm and w_g = 160μm has the optimum behavior in terms of loss. For this reason, the output circuit of the doubler with the two different geometries of the stubs was simulated in *Sonnet* (Fig. 4.31), and results indicated a 1-1.5 dB decrease in the total loss around 80 GHz. Such a difference can lead to a 20-25% improvement of the doubler's efficiency.

A doubler design with input diode Q of 2, two diodes and an area of 75 μm^2 per anode was implemented. An epi-layer with a 4000 $\AA$ thickness and a $1x10^{17}cm^{-3}$ doping density, as in the previous section, was assumed. The wafer, however, used for the fabrication of

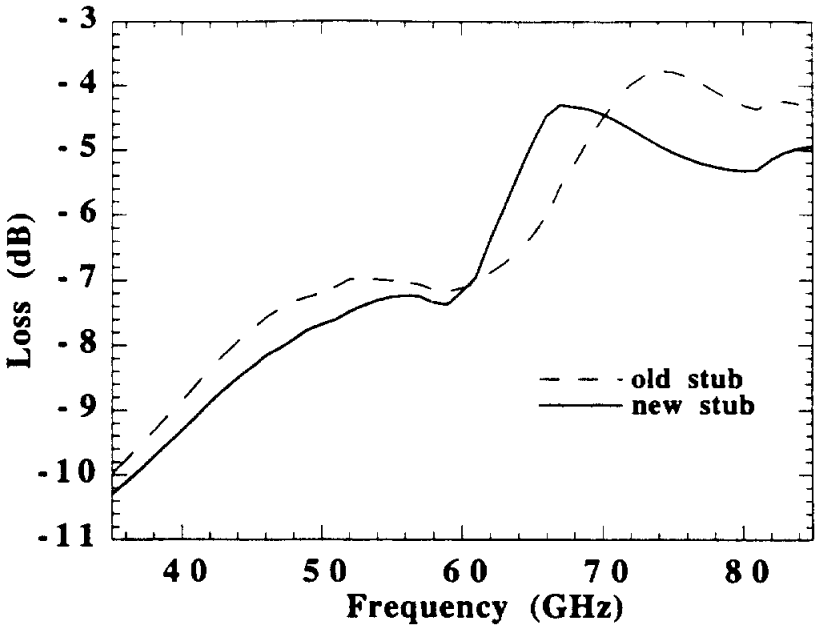
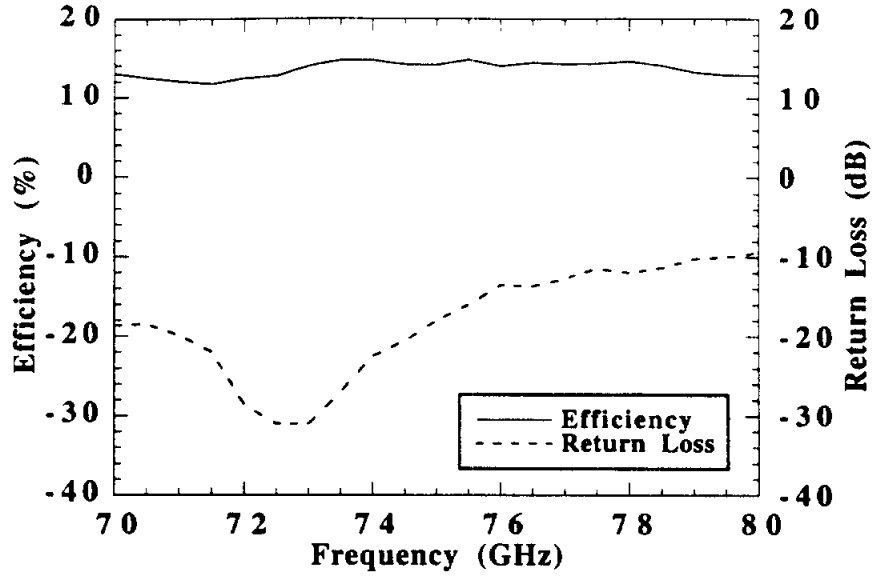


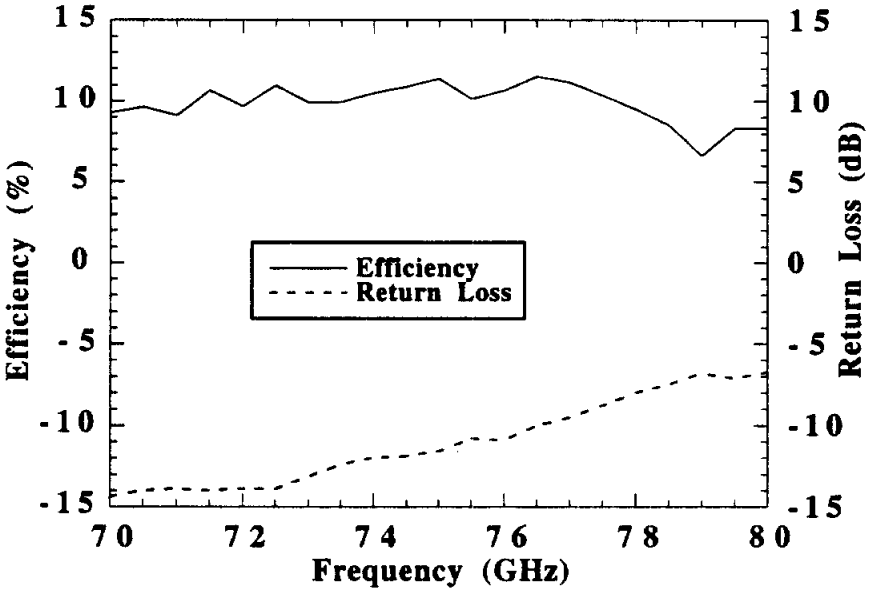
Figure 4.31: Simulated results for the output circuit of the doubler with the wide (new) and narrow (old) stubs.

the new multipliers was different from the wafer used before. The shunt 50 Ω stubs had w=50 μm and s=45 μm, while the line segments at the input and output ports were made shorter. Geometrical characteristics for the new doubler are summarized in Table 4.7. Since the wafer that was used was physically different, the old doubler design was repeated just for comparison purposes.

Efficiency measurements with the same system that was used in the four diode doubler case (only waveguide components at the input and E-H tuner at the output), for the new and old Q=2 design can be seen in Fig. 4.32. The improved doubler design exhibited a 14.8% efficiency at 75.5 GHz and a bias voltage of -2.2 V with a minimum bandwidth of 13.2% (10 GHz) and a -15 dB return loss, while the old design gave an efficiency of 11.5% at 76.6 GHz and a bias voltage of -2.1 V with a 13% minimum bandwidth and a -10 dB return loss. Clearly, the new design has a higher efficiency than the old one, but none of them surpasses the performance of the Q=2 doubler presented in the previous section. When the



(a)



(b)

Figure 4.32: Efficiency and return loss vs. output frequency for doublers fabricated on a new wafer and P_{in}=20 dBm: a) improved Q=2 design and b) old Q=2 design.

doping profile of the new wafer was measured, it was found that the doping density had a value of $0.5x10^{17}cm^{-3}$ instead of $1x10^{17}cm^{-3}$. This is a major difference and for a given anode area a smaller doping can decrease the diode efficiency [82] and alter the diode and embedding impedances. In addition, the optimum bias voltage of the new doublers was around -2 V which is lower than the bias voltage applied to the old ones (-3.5 V for the Q=2 and -5.5 V for the Q=3). Most of the multiplier measurements and the simulations with the multiple reflection program showed an increased efficiency for biases above -3 V, while lower values were achieved for biases between -2 and -1 V. Simulating a 40 to 80 GHz doubler with the multiple reflection program for a doping density of $0.5x10^{17}cm^{-3}$ and a bias voltage of -2 V yields an efficiency of 28% instead of 34% which was the original result. Since the circuit losses are the same in both multipliers if we take into account the -9 dB return loss and the effect of the parasitic capacitance the efficiency is found to be around 13.5%, which is close to the 11.5% measured value. The combination, therefore, of the lower doping concentration and optimum bias point leads to the reduction of the efficiency, when the same design on the old and new wafers are compared. However, when the improved doubler with the wider stubs is compared to the original design and both circuits are fabricated on the same wafer, the new design yields a higher efficiency (25 % increase) proving that further improvement of the multiplier performance is feasible if the passive circuit loss is reduced.

4.4 Conclusions

FGC lines on GaAs with a thin overlay of polyimide were fabricated and tested. Experimental results showed a negligible increase in the effective dielectric constant and a small increase in the attenuation per physical length, when compared with bare FGC lines on

GaAs. The attenuation per physical length of FGC lines on GaAs with or without polyimide was higher than that of FGC lines on quartz. The attenuation per guided wavelength, however, was almost the same for all types of lines investigated in this chapter, indicating that the total loss of FGC lines with the same geometry is independent of the substrate material. This allows for the use of a thin layer of polyimide over FGC lines on GaAs without increasing the total loss in actual circuits while providing passivation at the same time. In addition, the attenuation of the lines decreased in a non linear fashion versus characteristic impedance. As a result, FGC lines with a polyimide overlay can be used in millimeter wave receivers and transmitters fabricated on GaAs, where the active devices are monolithically integrated with the other circuitry and do not need to be flip-chip bonded as in the case of quartz.

Monolithic doublers with two diodes and input Q's of 2 and 3 were also designed, fabricated and tested. The Q=2 multiplier had an efficiency of 17.2% at 76.3 GHz, a minimum bandwidth of 10% and a maximum output power of 66 mW, while the Q=3 multiplier yielded an efficiency of 22% at 70 GHz, a bandwidth of 8.5% and a maximum output power of 50 mW. These are the highest reported values for both efficiency and bandwidth regarding monolithic multipliers. The microstrip doubler designed by Chen [14] yielded an efficiency of 25% at 94 GHz but no bandwidth information was provided. All the monolithic results, however, reported thus far in the literature cannot surpass the performance of waveguide doublers, such as the one by Porterfield [66] where a 48% efficiency and 17% bandwidth were achieved at 80 GHz. The optimum efficiency for the Q=2 design was achieved at a higher input power level from the Q=3 design (20 instead of 17 dBm) since the RF voltage swing accross the diode increases with the quality factor, leading to increased saturation effects in the device for a given available RF power and ,thus, limiting

the maximum input power before burn-out. For this reason, the efficiency of the Q=3 doubler also decreased considerably with increasing input power. Furthemore, the Q=2 doubler had a wider -3 dB efficiency bandwidth than the Q=3 which is expected because the diode and embedding impedances vary more rapidly with frequency, mismatching the input pump power. In addition, a Q=2 doubler with four diodes was designed, fabricated and tested. This doubler exhibited a 12.5% efficiency at 74 GHz with a minimum bandwidth of 12.5%, while the maximum measured output power was 115 mW which is the highest reported for a monolithic doubler in W-band.

Finally, a method to increase the efficiency of the multipliers was presented. By selecting wider slot and signal strips for the open-end stubs the loss of the output circuit decreased by approximately 1 to 1.5 dB at 80 GHz. Efficiency measurements for a new doubler with wider open-end stubs on a low doped wafer ($N_D = 0.5x10^{17}cm^{-3}$) yielded a value of 14.8%, compared to 11.5% for the old doubler (narrow stubs) fabricated on the same low doped substrate.

CHAPTER 5

W-BAND MONOLITHIC MIXER

5.1 Introduction

The receiver of a monolithic transmit/receive system used either for a communication or a radar application, downconverts an incoming RF signal to a much lower intermediate frequency (IF) for further processing (filtering and amplification). Since the goal of the monolithic chip is to have both transmitter and receiver on the same substrate, the sub-harmonic mixer design is ideal for the frequency down-conversion because the local oscillator that provides the fundamental frequency of the multiplier in the transmitter can also be used for mixing in the receiver, assuming that it has an appropriate bandwidth. As a result, there is no need to have two different sources on the chip that operate at different bands. For the sub-harmonic mixer the RF signal is approximately the n-th harmonic of the local oscillator, and if mixing occurs at an even harmonic a non-linear device with an anti-symmetric current-voltage characteristic, such as an anti-parallel pair of Schottky diodes, is typically used [84]. This type of mixer has been used extensively in the millimeter and sub-millimeter wave regions, because its main advantage is the fact that for those regions where LO power is scarce the LO frequency is only half the RF frequency. One drawback,

however, is that the anti-parallel diodes must be pumped at relatively high LO power levels unless a separate bias for each device can be provided [85].

Several researchers have implemented a sub-harmonic mixer design either in a waveguide [86], [87] or quasi-optical [88] configuration, with very good noise temperature and conversion loss performance even at frequencies as high as 640 GHz. For a planar environment, microstrip based designs in W-band have been realized with Schottky diodes [89] and HFET's [90] giving a conversion loss of 10 and 22 dB, respectively. A self-oscillating subharmonic MMIC mixer with microstrip lines and a pHEMT transistor has also given an average measured DSB conversion loss of 15 dB [91] from 70 to 85 GHz. Coplanar integrated balanced mixers using PM-HEMT technology for automotive applications operating at 77 GHz with a conversion loss of about 9 dB have also been demonstrated [92]. More recently, a hybrid sub-harmonic coplanar waveguide mixer on silicon substrate has shown a conversion loss of 7 dB, at an RF of 94 GHz and an LO power of 8.5 dBm, and a DSB noise temperature of 650 K [93].

This chapter presents the analysis and design of a monolithic FGC based sub-harmonic mixer, that is fabricated on the same substrate with a W-band doubler and operates at 80 GHz. The development and experimental results of back-to-back mixer diodes are shown first. The passive circuits necessary for the mixer are also designed, fabricated and tested. Finally, measured and simulated results of the mixer performance are demonstrated.

5.2 Mixer Analysis and Design

The x2 sub-harmonic mixer that will be part of the transmit/receive module is designed to operate at an RF of 76-80 GHz, an IF of 2-4 GHz and an LO of 38-39 GHz. The goal is to downconvert the 76-80 GHz signal produced by the multiplier at the transmitter to

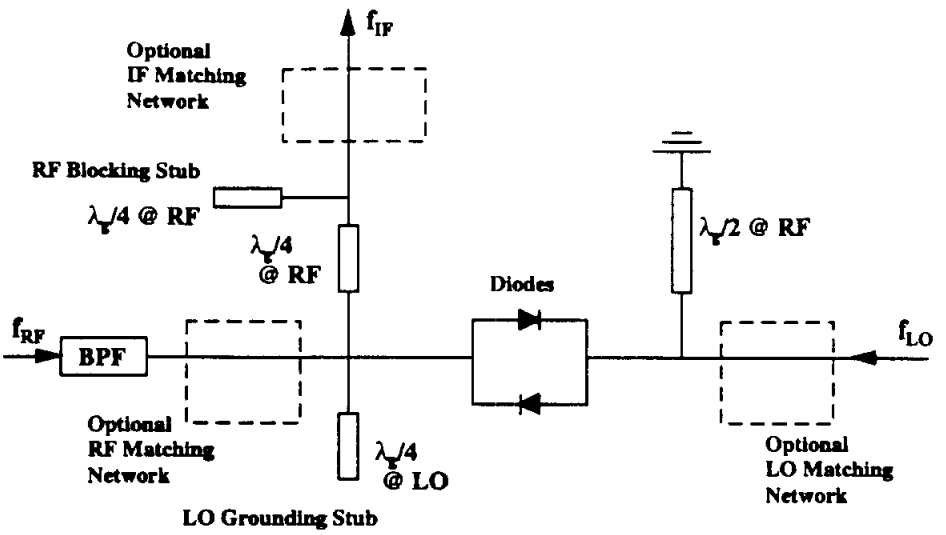


Figure 5.1: Schematic of the monolithic FGC based sub-harmonic mixer (from S. Raman [93]).

an intermediate frequency of 2-4 GHz at the receiver. A schematic of the mixer can be seen in Fig. 5.1 ([93]), where we observe that it consists of a back-to-back pair of diodes, a band-pass filter and several stubs for blocking and isolation at different frequencies. The entire design is monolithic and the transmission media are FGC lines. This is the first attempt to make a monolithic sub-harmonic mixer using finite ground coplanar technology.

Since the mixer will co-exist on the same substrate with a multiplier for the purpose of a transmit/receive module, the epi-layer used for the fabrication of the doubler diodes will also be used for the mixer diodes. This is critical because for optimum mixer performance at millimeter-wave frequencies a thin low-doped (n^-) epi-layer is required in order to minimize the series resistance, whereas for the doubler the epi-layer is usually thicker and of lower doping concentration. As a result, a compromise in the epi-layer parameters and, therefore, in the performance of the transmit/receive module needs to be reached. The W-band multipliers presented in chapter 4 had an n^- layer thickness of 4000 $\AA$ and doping of $1x10^{17}cm^{-3}$. For the sub-harmonic mixer the n^- thickness is 2000 $\AA$ and the doping

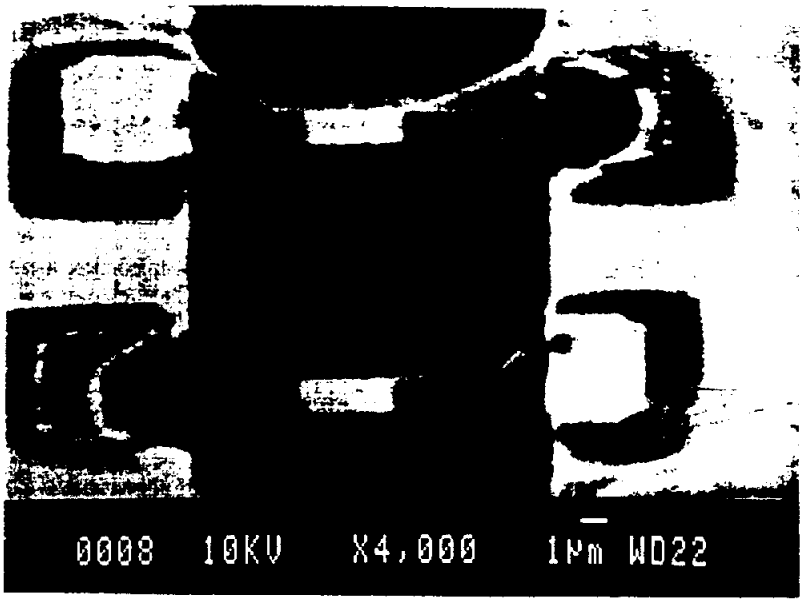
$3x10^{17}cm^{-3}$, although for best results in W-band a 700-900 Å thickness would be ideal. The higher doping density required for the mixer will increase the efficiency of the doubler but lower the output power since saturation effects wil be more pronounced.

The diameter of the mixer diodes, in contrast with the multiplier diodes, is small and equal to 2 μm in order to minimize the R_sC_t product. An even smaller diameter (1 μm) is desirable but fabrication constraints are imposed from the optical lithography system. The diode technology used for the fabrication of the multipliers cannot be implemented in this case because of the very small dimensions. For this reason a new fabrication technique was developed (for details see Appendix C) where the diodes have an etched surface channel-finger design without an air-bridge connecting them to the rest of the circuitry. The latter also contributes to the reduction of the parasitic capacitance caused by the presence of the air-bridge. The n^+ layer of the mixer diodes has a thickness of $2\mu m$ and a doping greater than $5x10^{18}cm^{-3}$. The fabrication procedure for the mixer can be summarized as follows:

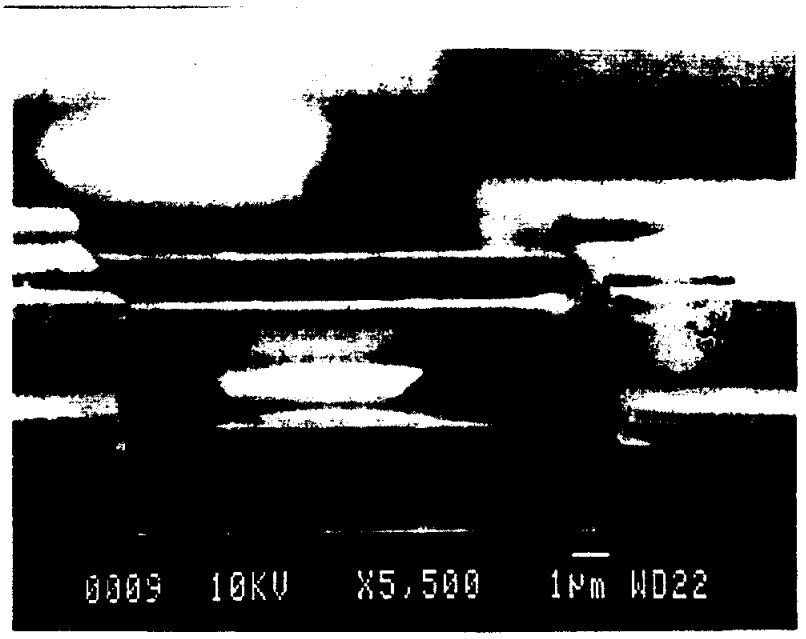
- PECVD Si_xN_y deposition of 2400 Å
- Schottky well formation by RIE etching of Si_xN_y
- Ohmic contact definition with Ni/Ge/Au/Ti/Au deposition
- Finger/anode definition and Ti/Pt/Au evaporation
- Mesa etch to isolate areas around the diodes
- Circuit metal deposition with Ti/Al/Ti/Au deposition
- Surface channel etch to isolate diode fingers
- Air-bridge formation for passive circuits

It should be noted here that the mesa-isolation etch is performed in two steps: in the first step a small rectangular area around the back-to-back diodes is protected and the epi-layers are removed from everywhere except for that rectangular region. This procedure ensures that the passive circuits will be deposited on semi-insulating GaAs and, therefore, the various FGC line segments will exhibit the characteristics shown in chapter 4. During the first etch, however, the diode fingers connecting the anode with the ohmic cathode are not isolated and as a result the diodes will have increased parasitics. For this reason, a second etch that removes the material underneath the diode fingers is performed after the passive circuit deposition. The new fabrication process also includes the formation of electro-plated air-bridges necessary for the passive circuits. To the author's knowledge this is the first time where air-bridges are formed on circuits that include small anode area diodes with fingers suspended in air. This fabrication technique allows for the realization of small channel etched diodes that have low parasitics, and for FGC lines with air-bridges used to suppress undesired modes. The advantages, therefore, from both the improved devices and the FGC lines can lead to enhancement of the overall system performance. A photograph of the fabricated back-to-back diode pair can be seen in Fig. 5.2.

The DC current-voltage characteristic of a 2 μm in diameter anti-parallel Schottky diode pair can be seen in Fig. 5.3, while the C-V measurement of a single diode is shown in Fig. 5.4. The measured data of Fig. 5.4 are curve-fitted with equation 4.4 in order to extract the parasitic and zero-bias junction capacitance of the diode. All of the diode parameters are summarized in Table 5.1. The junction capacitance per anode was 9-10 fF while the parasitic capacitance was 3 fF. The parasitic capacitance C_p is partly due to the capacitance between the region under the diode finger and around the anode and partly between the diode finger and the ohmic contact. For the anti-parallel pair the total parasitics were 6 fF,



(a)



(b)

Figure 5.2: SEM photograph of: a) back-to-back diodes with $2\mu m$ diameter and b) channel under the diode fingers.

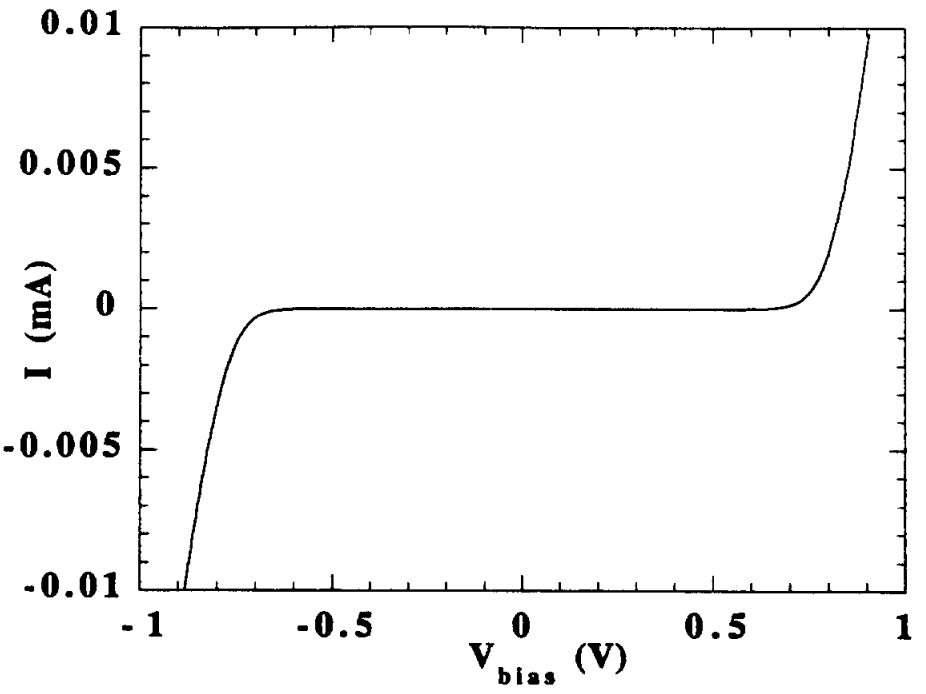


Figure 5.3: Current-voltage characteristic of the anti-parallel pair of Schottky diodes used in the mixer design.

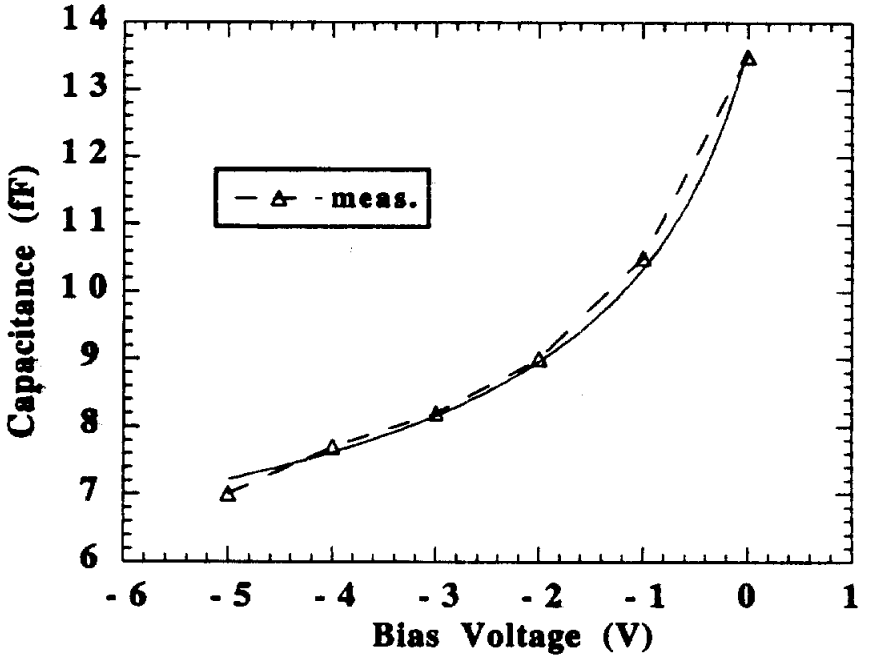


Figure 5.4: Measured capacitance versus bias voltage for a single mixer diode with curve-fitted data.

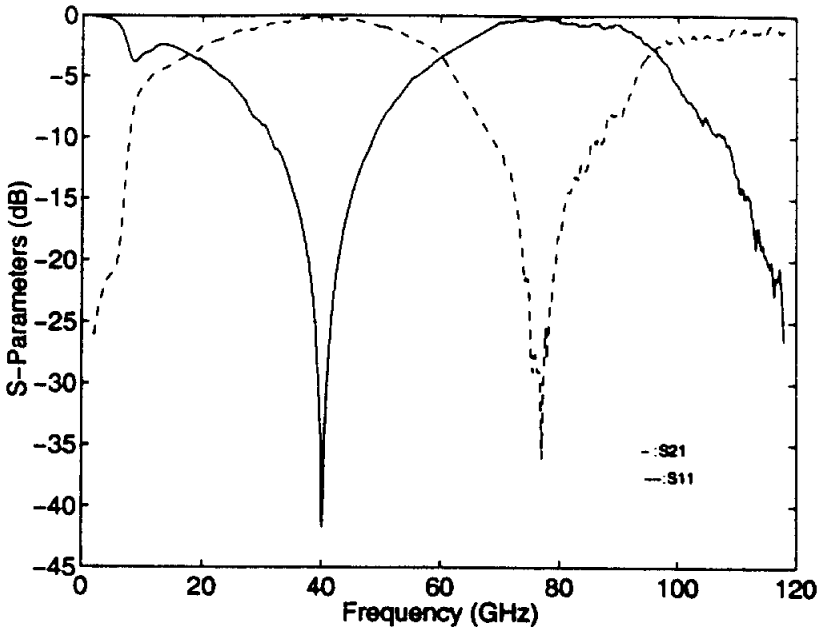
$R_S(\Omega)$	C_{jo} (fF)	C_{totp} (fF)	η	V_{bi} (V)	I_o (fA)	V_{BR} (V)	f_C (GHz)
7	9-10	6	1.19	0.95	35	-7.2	875

Table 5.1: Measured DC characteristics for the mixer diodes.

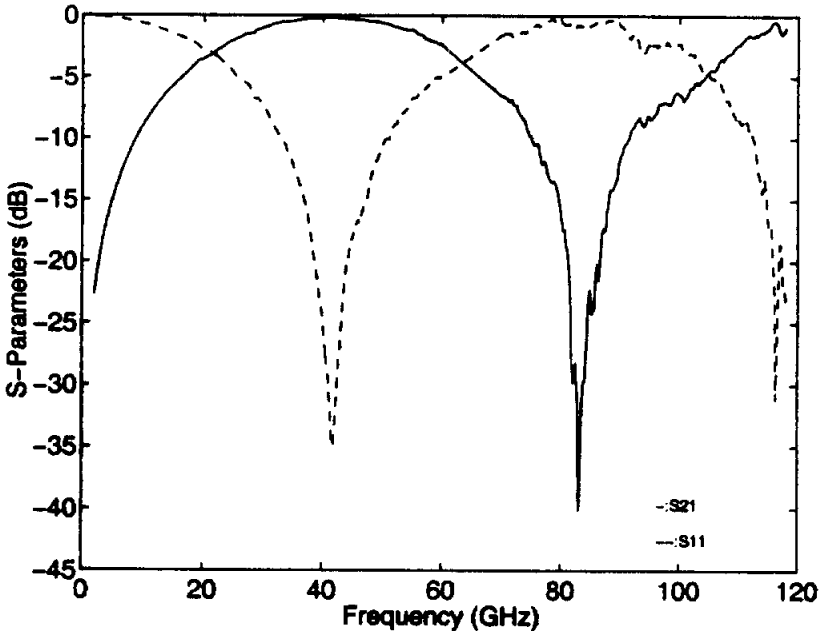
yielding a total capacitance C_t=26 fF. Since the series resistance of the diodes was R_S=7 Ω the figure of merit cut-off frequency of the back-to-back pair was approximately 875 GHz. The junction capacitance of 9-10 fF is slightly higher than the one expected (6-7fF) due to the small increase in the diameter (2.2 μm instead of 2) of the fabricated diodes that results from the various processing steps.

Regarding the passive cicuits of the mixer, at the RF side there is a band-pass filter from 70-90 GHz that prevents IF leakage to the RF port and a $\lambda_g/4$ open-end stub at the LO frequency so that there is good isolation between the RF and LO ports without affecting the RF signal. An RF matching network that matches the diode impedance seen at the RF frequency is optional. At the IF port there is a $\lambda_g/4$ open-end RF blocking stub placed $\lambda_g/4$ away from the diodes, that prevents leakage of the RF signal to the IF path without attenuating the IF signal. At the LO port there is a $\lambda_g/2$ short circuited stub at the RF frequency so that the RF signal does not leak to the LO port, while the LO signal passes unaffected. The addition of matching networks at both the IF and LO ports for matching the IF and LO diode impedances, respectively, is also optional.

The various passive elements of the mixer were realized using FGC line techology with a 50 Ω main line that had w=50 μm, s=45 μm and w_g=160 μm, as in the case of the multipliers. Both the RF and LO grounding shunt stubs had a characteristic impedance of 50 Ω and the same line dimensions with the 50 Ω main line, in contrast with the w=s=20 μm parallel stubs used in the doublers. Several stubs were designed, fabricated and tested



(a)



(b)

Figure 5.5: Measured S-parameters for the: a) LO grounding stub and b) the RF grounding stub.

Stub Design	Length (μm)	Open-circuit Resonance		Short-circuit Resonance	
		f_{res} (GHz)	S_{21} (dB)	f_{res} (GHz)	BW (-10dB)
LO Grounding	726	79.12	-0.24	40.1	43.4% (17.4 GHz)
RF Grounding	708	40.7	-0.13	82.96	19.8% (16.4 GHz)

Table 5.2: Measured characteristics of the shunt stubs used in the mixer design.

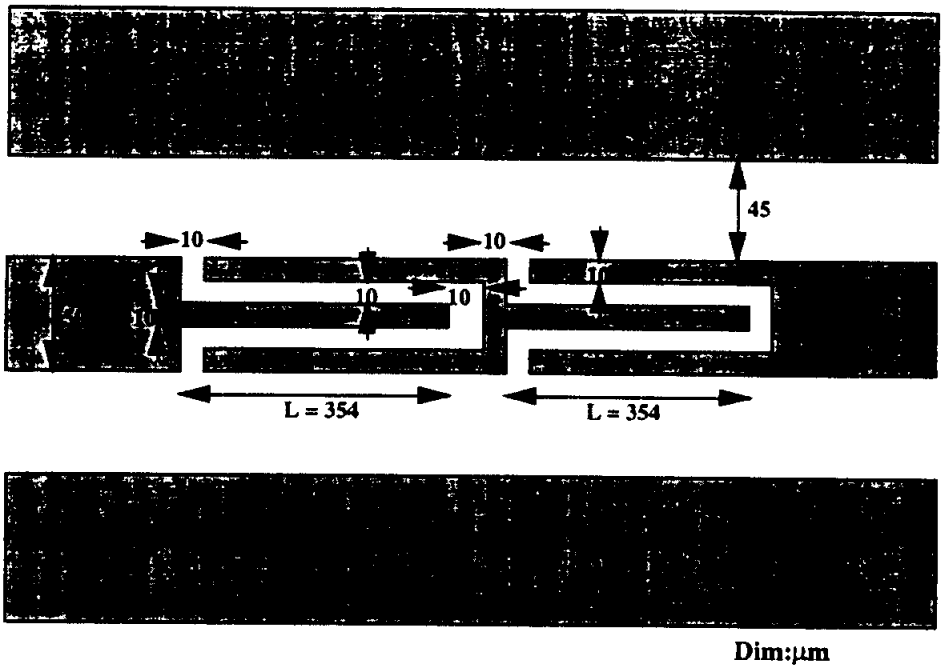
with the goal to achieve as good performance as possible. Measurements for the RF and LO grounding stubs at the LO and RF port, respectively, can be seen in Fig. 5.5, while results are summarized in Table 5.2. The scattering parameters were measured with a TRL calibration and the reference planes were located at the cross-junction of the parallel sections with the main line that connects the two ports. As seen from Table 5.2, the insertion loss for both stubs at the open-circuit resonance is very small, while at the short-circuit resonance the LO grounding stub has twice the bandwidth of the RF grounding stub due to the different resonant frequency ($f_{resLO} \approx f_{resRF}/2$). The effect, therefore, of the stubs on the attenuation of the RF and LO signals traveling towards the diodes should not be substantial and should not deteriorate the mixer performance. It is worthwile to note here that the smaller loss of these stubs when compared with the doubler stubs (0.23 dB/mm at 20 GHz), is due to the fact that the signal line and slot widths are wider than those used in the doubler.

The RF bandpass filter was realized using open-end series stubs [2], [93] that can provide the appropriate bandpass characteristics. Since one section has a relatively wide bandwidth, a two section design was chosen in order to effectively block the IF from leaking at the RF port. A schematic of the filter along with the equivalent circuit model for one open-end stub, which is based on [94], can be seen in Fig. 5.6. Each finger of the stub is $\lambda_g/4$ long at

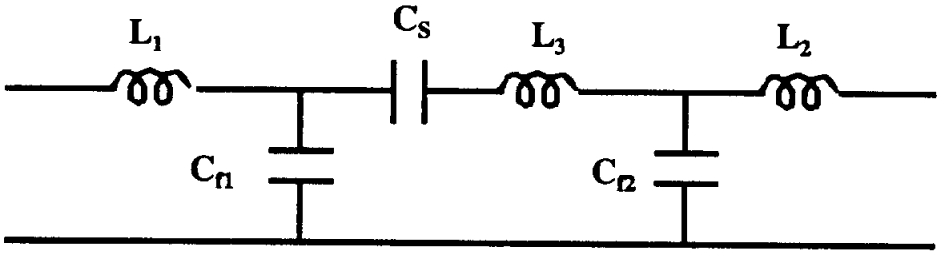
resonance translating an open to a short and thus allowing the signal to pass. At twice the resonant frequency the stub is electrically $\lambda_g/2$ long, maintaining the open character and blocking the corresponding frequency.

For a band-pass centered at 80 GHz the length L of each finger was calculated from $L=\frac{\lambda_g(@80)}{4}= 354\ \mu m$, where an effective dielectric constant of 7 was assumed based on the FGC line results of chapter 4. Since the main 50 Ω line has w=50 μm, s=45 μm and w_g=160 μm the width of the each finger and slot was 10 μm. Due to the increased width, when compared with the filter presented in [93], this filter is expected to have less loss. Simulated results for the filter of Fig. 5.6(a) with *IE3D* can be seen in Fig. 5.7(a), where an insertion loss of 0.43 dB is predicted at 80 GHz with the method of moments technique. Measured results with a TRL calibration for the filter are also shown in Fig. 5.7(a), where an insertion loss between 0.46 and 0.63 dB was achieved between 70 and 90 GHz. The loss at 80 GHz was 0.55 dB while for 2-4 GHz it was -33 to -27 dB, thus, providing an excellent block for the IF signal. The agreement between the simulated and measured data is very good, as witnessed from Fig. 5.7(a).

In order to run a harmonic balance analysis of the mixer in *Libra* the filter response at higher harmonics has to be evaluated. One way to achieve this is to use the model of Fig. 5.6(a) for one stub in a cascaded configuration that represents the two-stub filter, and fit the simulated *IE3D* data with the modeled data in *Libra*. The equivalent circuit model with known element values can then be inserted in the harmonic test bench. Initial values for the lumped resistors, capacitors and inductors can be found from equations (22)-(27) of [94]. Results for the calculated lumped element values of Fig. 5.6(b) are summarized in Table 5.3 and a comparison between the scattering parameters of the *IE3D* simulation and the equivalent circuit simulation in *Libra* can be seen in Fig. 5.7(b).

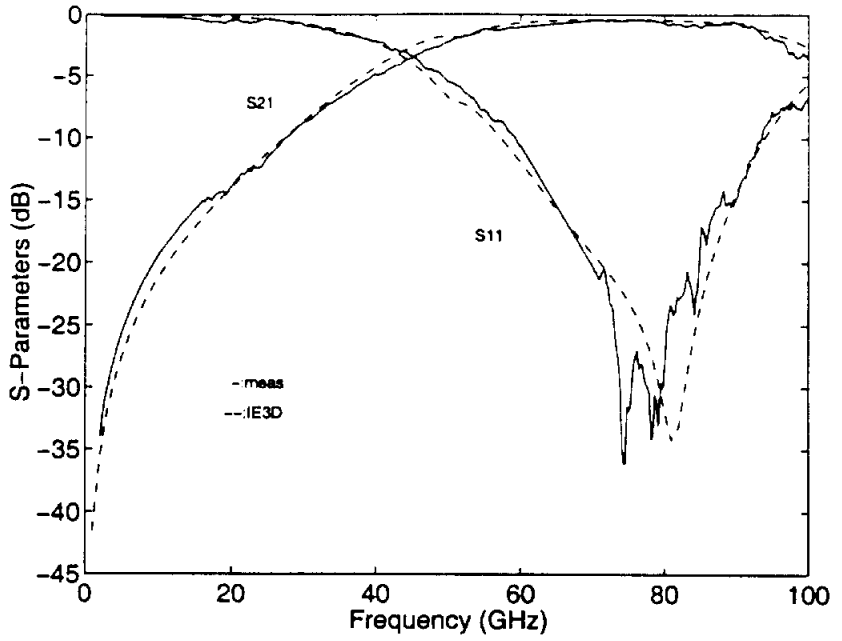


(a)



(b)

Figure 5.6: RF bandpass filter used in the mixer design: a) circuit layout for two stub sections and b) equivalent circuit model for one stub section.



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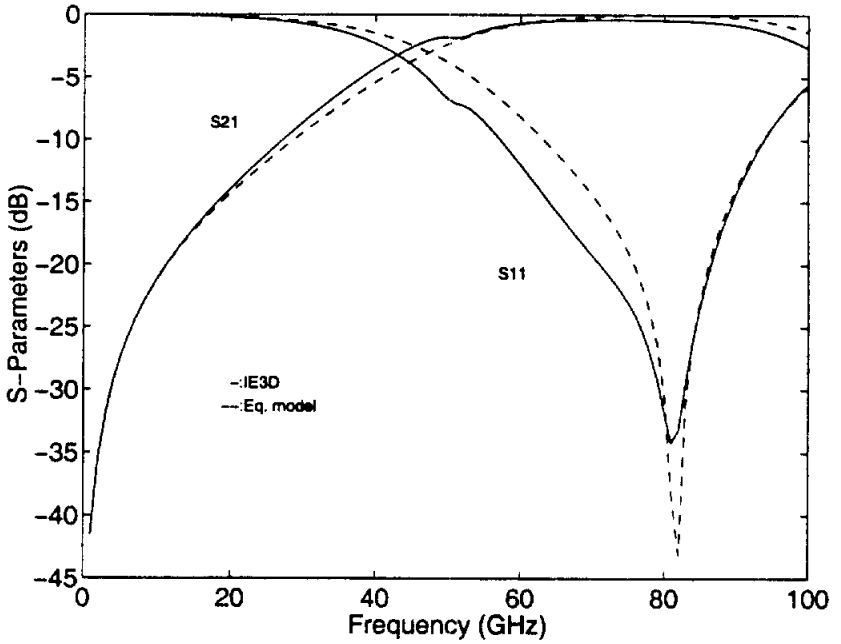
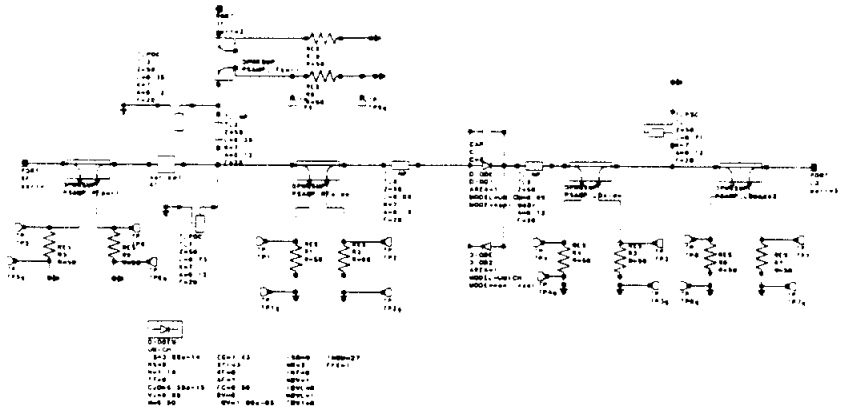


(b)

Figure 5.7: S-parameters vs. frequency for the mixer bandpass filter: a) measured and *IE3D* simulated data and b) *IE3D* simulated and *Libra* equivalent circuit data.



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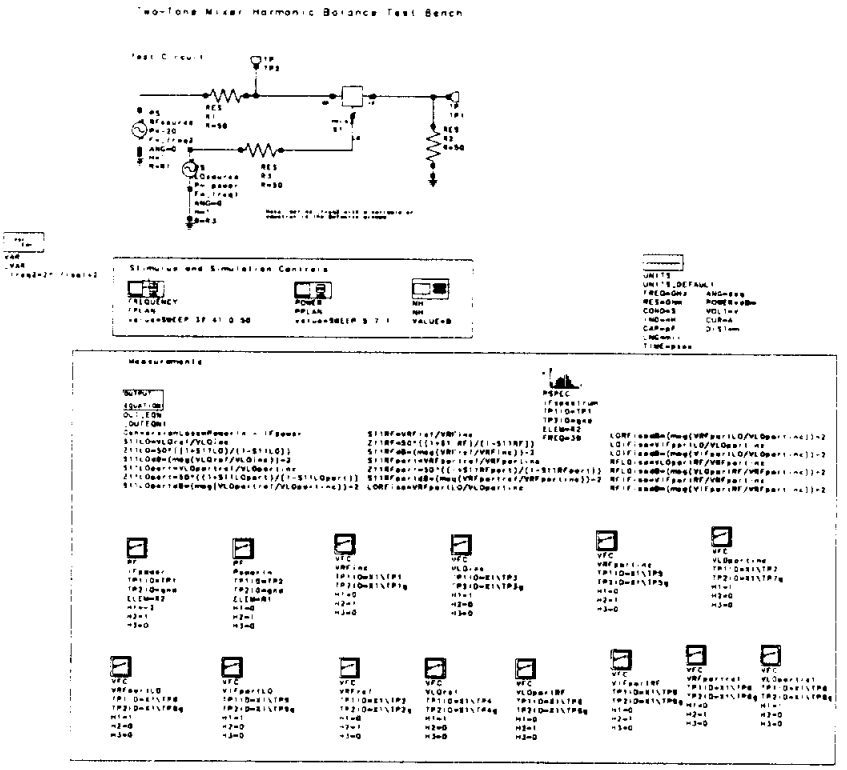


(b)

Figure 5.8: *Libra* simulation for the x2 subharmonic mixer: a) circuit schematic and b) harmonic balance test bench.

L_1 (pH)	C_{f1} (fF)	C_S (fF)	L_3 (pH)	C_{f2} (fF)	L_2 (pH)
64.24	15	43.71	115.75	40	55

Table 5.3: Calculated values for the equivalent circuit model of Fig. 5.6(b).

The next step in the analysis is to perform the harmonic balance simulation in *Libra*, so that the mixer response can be evaluated. This is possible since the various stub lengths, the equivalent circuit of the bandpass filter and the DC diode characteristics are known. Each section of FGC line can be modeled as a physical transmission line with known attenuation and effective dielectric constant, while for the diodes a pn junction model with known DC parameters will be implemented. A test bench, where the mixer is inserted, is created and the LO and RF frequencies are varied accordingly for different LO power levels. The circuit schematic and test bench used in *Libra* can be seen in Fig. 5.8. Results for the conversion loss in the upper side band of the mixer are shown in Fig. 5.9, where a 6.5 dB value is achieved at an RF frequency of 80 GHz, an IF of 4 GHz and an LO power of 6 dBm. The RF and LO diode input impedances were also calculated for the same parameters and found to be Z_{inRF}=27.7+j9.8 Ω, Z_{inLO}=41-j59.5 Ω for P_{LO}=6 dBm, taking into account the transmission line segments that are around the devices. The IF load for the previous results was 50 Ω. Since *Libra* does not yield the IF output impedance a code developed by Kormanyos [88] for subharmonic mixers based on the original code of S. Maas [95] was used. For IF frequencies between 2 and 4 GHz the program yielded an impedance around 56 Ω and the result did not vary with different terminations (short, 50 Ω) of the higher RF and LO harmonics.

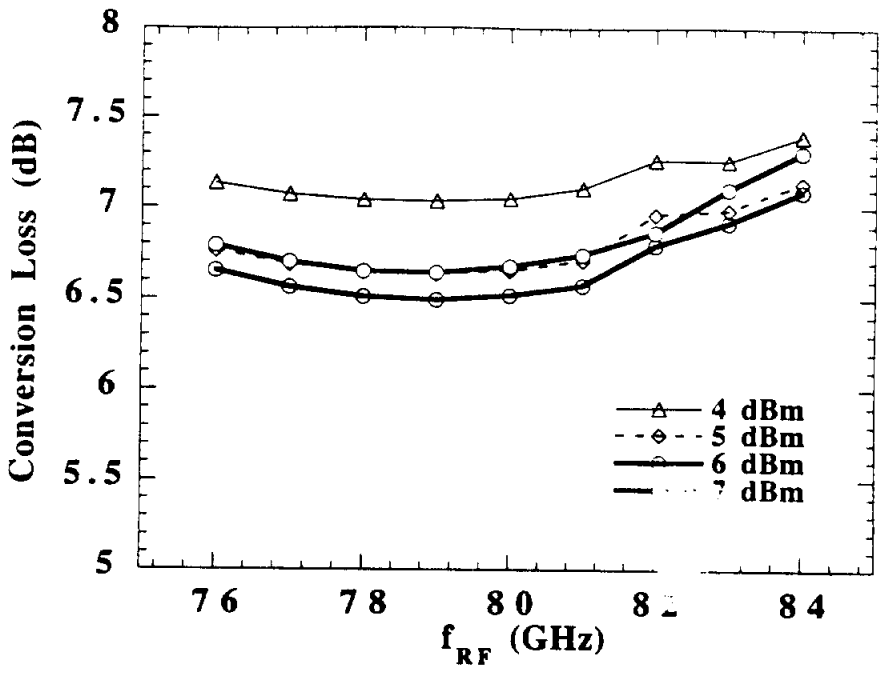


Figure 5.9: Conversion loss vs. RF frequency for different LO power levels.

5.3 Results

The mixer that was designed in the previous section was fabricated on a GaAs wafer with an n^- epi-layer thickness and doping of 2000 $\AA$ and $3\text{x}10^{17}cm^{-3}$, respectively, and a 2 μm thick n^+ layer with a doping greater than $5\text{x}10^{18}cm^{-3}$. The size of the actual circuit was 2.2 mm x 1.9mm and a picture of it can be seen in Fig. 5.10. The metal thickness of the evaporated FGC line segments was 1 μm, which is equal to 2.5 skin depths at 40 GHz and 3.5 at 80 GHz, while the metal thickness of the gold electro-plated air-bridges was 3-3.5 μm. The air-bridges are located at various points in the circuit so that the coupled slotline mode is suppressed and the different stubs are in parallel connection with the main 50 Ω line and not in series.

The measurement system that was used for the on-wafer evaluation of the single-sideband downconversion loss can be seen in Fig. 5.11. The 80 GHz RF signal is provided

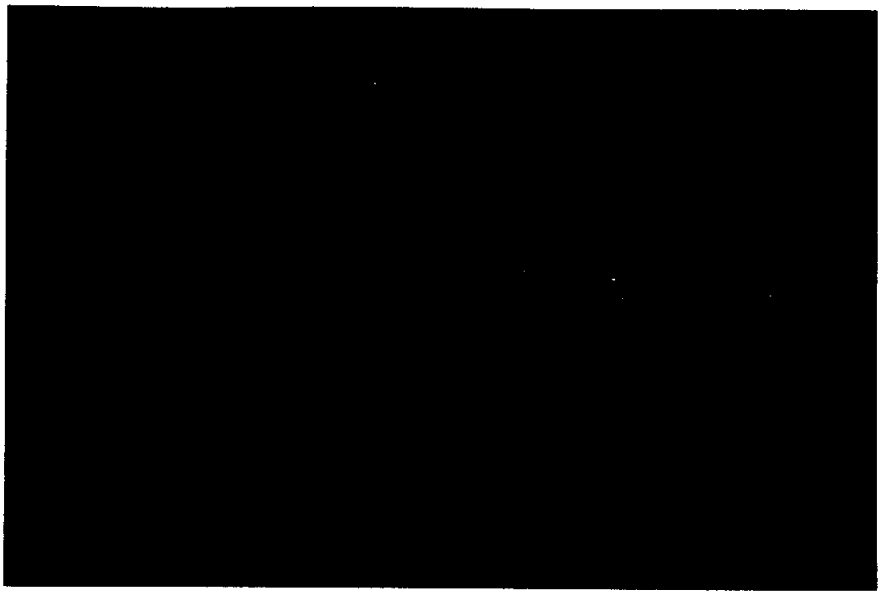


Figure 5.10: Fabricated FGC line monolithic mixer.

by the W85104A mm-wave source module that is connected to the HP8510C network analyzer thru a 10-dB WR-10 directional coupler used for power sampling. In order to comply with the dynamic range of the power meter the thru port of the coupler is connected to the W-band power sensor and the coupled port is used for the RF signal extraction. This configuration is necessary since the power level of the RF signal is around -20 dBm and cannot be measured with accuracy from the Anritsu power sensor and meter. The output of the coupled port is then connected to a long section of WR-10 waveguide that leads to the 120A-BT W-band GGB probe. The 35-40 GHz LO signal is provided by an HP 83640L synthesized source thru a short semi-flexible cable and a K-band GGB probe. It should be noted here that the available LO power level was limited by the specifications of the synthesizer. The IF signal is extracted from a K-band GGB probe that is connected to an HP 8564E spectrum analyzer via a cable. The losses of the various cables, coplanar probes and waveguide sections were extracted by measuring each one of them with either the network or the spectrum analyzer. For the RF and LO port the loss was found to be

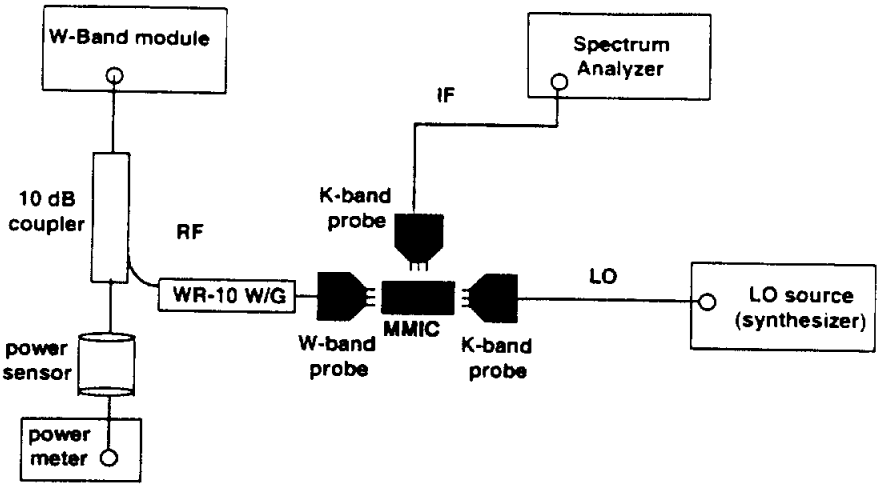
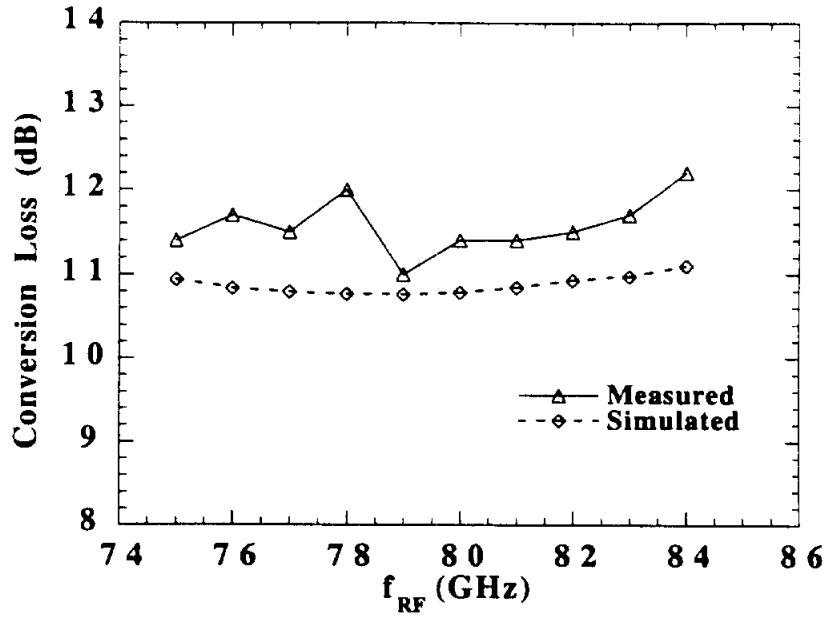


Figure 5.11: Block diagram of the system used for the mixer measurements.

approximately 3 dB while for the IF port the loss was around 1.3 dB. Once the losses are known the measurements can be calibrated at the end of the probe tips, as shown in Fig. 5.10.

The measured single sideband (SSB) conversion loss versus RF frequency for an IF of 4 GHz can be seen in Fig. 5.12(a), where the LO power for each frequency point is the optimum depending on the availability of the synthesizer for that particular point. A minimum conversion loss of 11 dB was achieved at 79 GHz for an LO power of 8.8 dBm, while the 3 dB bandwidth was more than 11% (9 GHz). The very broadband performance of the mixer can be attributed to the fact that there are no matching networks that typically improve the conversion loss but narrow the bandwidth. Fig. 5.12(b) also shows the conversion loss for different LO power levels at an RF of 80 GHz. Due to power limitations the maximum available LO power was around 7.6 dBm and resulted in a conversion loss of 11.3 dB. Comparing the measured results with those of Fig. 5.9, a 4 dB discrepancy in the value of the conversion loss is observed. A DC measurement of the I-V characteristic for the actual diodes on the mixer circuit revealed a high value for the series resistance $R_S = 40\Omega$.



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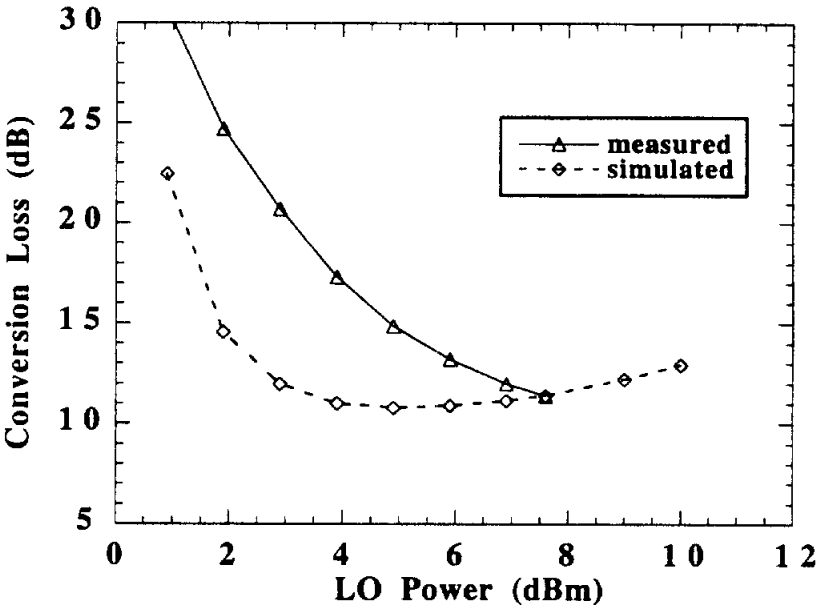


(b)

Figure 5.12: Measured and simulated data for the diode with $R_S = 40\Omega$: a) SSB conversion loss vs. RF frequency for optimum LO power and b) SSB conversion loss vs. LO power at $f_{RF} = 80GHz$.

Simulated results with diodes having the same characteristics as the ones on the measured mixer can be seen in Fig. 5.12, where good agreement can be observed within 0.5 dB. The increased value in the series resistance can be attributed to a yield problem that resulted in performance degradation for several devices. Possible reasons for this problem include insufficient etching of the low-doped layer from the small ohmic cathodes, misalignment between the anode, the cathode and the finger, incomplete removal of the nitride from the anode, as well as a combination of those.

Isolation measurements between the various mixer ports were also performed. For the LO/IF isolation the W-band probe of the RF port was terminated in a 50 Ω load and the rest of the system portrayed in Fig. 5.11 was kept the same. Simulated and measured results can be seen in Fig. 5.13, where the measured isolation was better than 24 dB for LO frequencies between 37 and 40 GHz. From the *Libra* simulations the LO/IF isolation is expected to be better than 25 dB. The LO/RF isolation was measured by terminating the IF port in a 50 Ω load and replacing the W-band probe of the RF port with a K-band probe connected to the spectrum analyzer. Results can also be seen in Fig. 5.13, where an isolation better than 20 dB was achieved between 37 and 40 GHz. It should be noted here that the previous measurements were calibrated at the end of the probe tips by removing the losses of the various components.

5.4 Conclusions

A monolithic FGC based W-band mixer has been designed, fabricated and tested. The epi-layer parameters are the same with those of a monolithic multiplier since the mixer is intended for use in a monolithic transmit/receive module. The choice for the epi-layer thickness and doping, therefore, is a compromise between the optimum one for either a

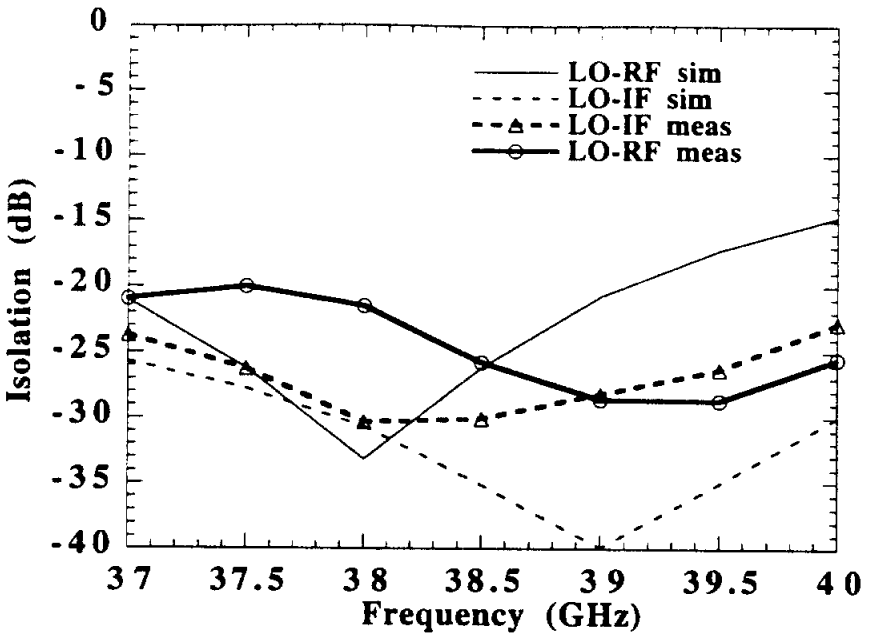


Figure 5.13: Simulated and measured results for the RF/LO and LO/IF isolation of the mixer versus LO frequency.

doubler or a mixer design. In order to achieve diodes with low parasitics and small anode areas a novel fabrication technique that combines channel etched finger type diodes and FGC lines with air-bridges has been implemented. In this technique, once the diodes are formed on the epi-layers a small rectangular area around them is isolated and the active layers are etched from everywhere except for that region, without removing any material underneath the finger. After the deposition of the passive circuits, a second etch creates the channel under the diode fingers and the process ends with the formation of the air-bridges for the various FGC line sections. Measured results for the W-band mixer that was fabricated with this technique and included diodes with a diameter of 2.2 μm, yielded a minimum single sideband conversion loss of 11 dB for an RF of 79 GHz, an IF of 4 GHz and an LO power of 8.8 dBm. The 3-dB bandwidth is also greater than 11% (9 GHz) and covers the entire measurement band (75-84 GHz). The observed discrepancy between the

measured (11 dB) and simulated loss (6.5 dB) was due to a relatively high series resistance of the diodes caused by a device yield problem in the wafer. A mixer with the excellent characteristics of back-to-back diodes measured in other parts of the wafer should give a conversion loss closer to the expected one. The LO-RF and LO-IF isolations of the mixer are better than 25 dB for LO frequencies of 38.5-40 GHz and 37.2-39.5 GHz, respectively.

The mixer presented in this chapter is the first effort of a monolithic W-band FGC line design that can be combined with a monolithic multiplier on the same substrate and have a performance that is comparable with that of state-of-the-art subharmonic mixers. This will allow for the realization of monolithic transmit/receive modules operating at millimeter wavelengths that combine small size, high circuit density and excellent performance.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

This thesis has presented a collection of work on active and passive monolithic microwave integrated circuit structures that can be used in the design of a monolithic transmitter/receiver module for application in radar and communication systems. For the passive elements silicon micromachining was used to enhance the performance of circuits such as antennas and filters, while for the active elements the finite ground coplanar (FGC) line technology was used to design multipliers and mixers on GaAs.

Two techniques that can increase the radiation efficiency of rectangular patch antennas on high index materials were studied. Both of them were based on the removal of dielectric material under the radiating element in an effort to either reduce the effective dielectric constant or suppress the dominant surface wave mode. Measured results for Ku-band patches fabricated on Duroid substrate with the first method showed a bandwidth and efficiency increase of 64% and 28%, respectively, as well as sensitivity of the radiation improvement on the placement of the machined cavity relative to the antenna. This result is the first reported for an increased efficiency rectangular patch antenna that does not

implement dielectric membranes for the suspension of the patch or holes drilled in the substrate. Simulated results with the finite difference time domain technique for the second method exhibited a substantial decrease of the electric field inside the substrate. This is the first attempt to suppress with an analytical based design the TM_0 mode of a rectangular patch antenna on high dielectric constant material.

Micromachining was implemented for the design and fabrication of a monolithic high-Q X-band resonator that consists of microstrip lines, coupling slots and a rectangular cavity. Measured results showed an unloaded quality factor Q_u of 506, a bandwidth of 5%, an insertion loss of 0.36 dB and good thermal stability. Different positioning of the slots with respect to the center of the cavity also showed the possibility to alter the resonator's response; a 2% bandwidth with a loss of 1.1 dB were measured. This is the first report of a fully monolithic resonator that can achieve a quality factor higher than that of traditional planar microstrip or stripline resonators either printed on a dielectric material or suspended in air with the help of a dielectric membrane.

FGC lines on GaAs with a thin overlay of polyimide as well as lines on quartz were studied. Experimental results showed that the polyimide covering the FGC lines has a negligible effect on the dielectric constant and causes a small increase in the attenuation. The total loss also of lines with the same geometry is independent of the substrate material and is mainly ohmic. This is the first report on characteristics of FGC lines with polyimide and on the effect of different substrate material and different geometries.

Monolithic FGC based W-band doublers for higher efficiency and output power were also designed, fabricated and tested. Measurements for a Q=2 doubler with two parallel diodes yielded an efficiency of 17.2% at 76.3 GHz, a minimum bandwidth of 10% and a maximum output power of 66 mW, while for a Q=3 doubler an efficiency of 22% at 70

GHz. a bandwidth of 8.5% and an output power of 50 mW were measured. These values for both the efficiency and bandwidth are the highest reported for monolithic multipliers. The microstrip doubler designed by Chen [14] yielded an efficiency of 25% at 94 GHz but no bandwidth information was provided. All the monolithic results, however, reported thus far in the literature cannot surpass the performance of waveguide doublers, such as the one by Porterfield [66] where a 48% efficiency and 17% bandwidth were achieved at 80 GHz. Measured results for a four diode doubler (two parallel pairs) design showed an efficiency of 12.5% at 74 GHz, a minimum bandwidth of 12.5% and a maximum ouput power of 115 mW which is the highest reported for a monolithic doubler in W-band. In addition, a method to increase the efficiency by reducing the loss of the shunt open-end stubs used in the multipliers was studied. Preliminary measurements showed that a 20-25% improvement is feasible.

Finally, a monolithic FGC line subharmonic mixer in W-band was designed, fabricated and tested. A novel fabrication technique that allows the co-existence of both small and large channel etched finger type diodes with passive circuit air-bridges was implemented. This is the first report of such a fabrication scheme that can be used for the realization of a multiplier and a mixer on the same substrate. Measured results for the mixer yielded a single sideband conversion loss of 11 dB at an RF frequency of 79 GHz, an IF of 4 GHz and an LO power of 8.8 dBm, as well as a 3 dB bandwidth greater than 11%. This is the first report of a monolithic subharmonic mixer in W-band with FGC line technology.

6.2 Future Work

6.2.1 W-Band Micromachined Antennas

The first technique presented in chapter 2 where material is removed only in a portion under the patch antenna and not through all of the substrate, can be implemented for the fabrication of high efficiency planar antennas and arrays in W-band. At such high frequencies power lost to surface waves can be reduced by using thin substrates (typically $\lambda_d/10$) and ,thus, at 94 GHz a 100 μm thick silicon wafer will be needed. The radiation efficiency, however, of a patch on such a thin substrate will be greatly reduced. A solution, therefore, where thick substrates are partly micromachined can be implemented in order to avoid problems associated with thin substrate materials or with dielectric membranes used to suspend the antenna. Preliminary measurements of a micromachined rectangular patch at 94 GHz have shown very encouraging results [96], making this type of antenna very attractive for the vertical integration of antenna arrays at millimeter-wave frequencies.

6.2.2 Micromachined High-Q Filters and Diplexers

The micromachined high-Q resonator presented in chapter 3 of this thesis is the first step for the realization of fully monolithic high-Q filters and diplexers. A possible filter layout was shown in Fig. 3.2, where energy is coupled from the input and output microsrtip lines to the corresponding cavities via slots. Slots are also used to couple energy between the different cavities. An increased number of cavity-resonators is desired in order to achieve a narrow bandwidth response. For a filter design a relationship between the cavity physical parameters (size, slot positions) and an equivalent circuit/electric model is necessary so as to formulate design equations that could be used for the realization of a specific response. Since

alignment and bonding between the different wafers is very critical for the loss performance, techniques that are more reliable and robust need to be found. A eutectic thin-film bonding process that can be incorporated with the rest of the standard fabrication steps would greatly reduce the cost and increase reliability. In addition, if a thin film is used instead of the silver epoxy glue bonding can be more uniform, less lossy and less rough. For better alignment, the pyramidal pits that are created from the anisotropic micromachining can be used as receptacles for microspheres between wafers and greatly increase accuracy. Another possibility is to use very thin fibers going through via-holes created inside the silicon substrate. In order to reduce the size of the cavities but still maintain the narrow-band low-loss characteristics micromachined evanescent mode [97], instead of propagating, filters can be pursued.

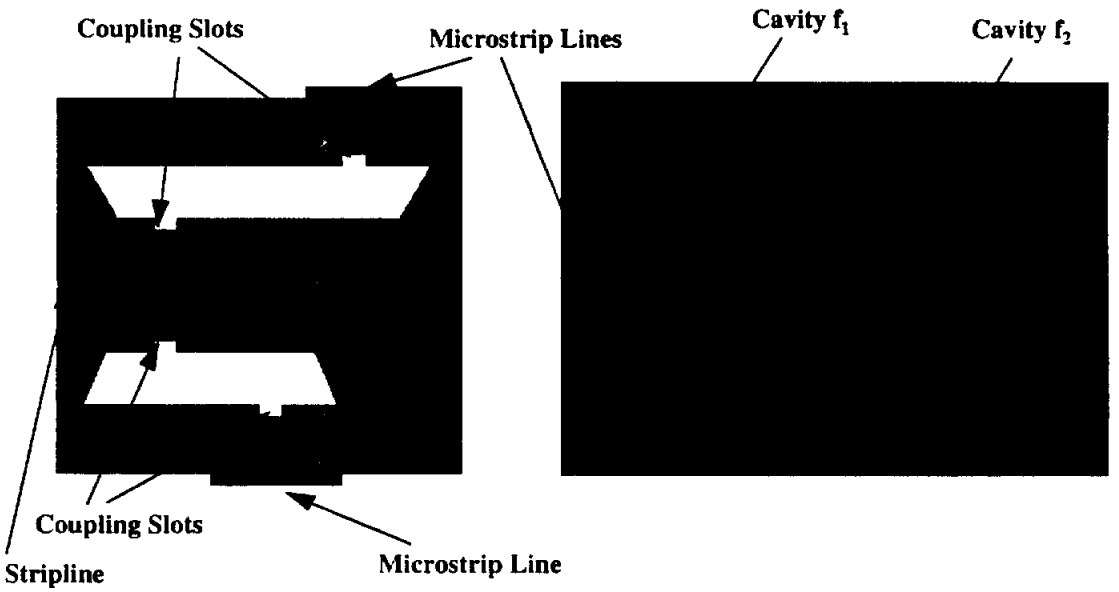


Figure 6.1: Conceptual diagram of a monolithic micromachined diplexer.

For communication systems diplexers that separate the different bands of an incoming RF signal are very important. A monolithic approach with low loss and narrow bandwidth that makes use of micromachining is shown in Fig. 6.1. In this case, a stripline is carrying the

RF signal and two cavities with different sizes and, therefore, different resonant frequencies that are centered around the bands of interest are used to extract the two corresponding signals. Coupling between the stripline and the cavities can be achieved with slots and controlled by their relative location.

6.2.3 Improved and New Multipliers

From the doubler results presented in chapter 4 it is clear the the ohmic or circuit loss limits the performance of FGC based multipliers. Techniques, therefore, or methods that can decrease the passive circuit loss need to be investigated. One approach that was proposed in chapter 4 and was based on the optimum slot and signal width design in terms of loss for the open-end shunt stubs, yielded encouraging results. The fabrication of those improved designs should be repeated on a wafer similar to the one that gave the best overall efficiency for the Q=2 and Q=3 doublers.

Another way to reduce the loss of FGC lines is to micromachine grooves in the slots in an effort to eliminate the dielectric material in the aperture regions, where the electromagnetic fields are concentrated [3] (see Fig. 6.2). Measured results for silicon substrate have shown a loss improvement of up to 1 dB/cm in W-band. GaAs micromachining has been successfully used in the past to fabricate membrane suspended planar antennas for automotive applications [42]. Plating of the FGC lines to a 3 μm thickness (instead of $1\mu m$ that results from the evaporation) can also contribute to reducing the ohmic loss, especially at the input side of the doublers where the skin depth is larger.

For a four diode doubler realization, the low impedance section at the input side necessary for impedance matching further increases the circuit loss (low impedance lines have higher loss as shown in chapter 4). An alternative to this is to design a four diode doubler

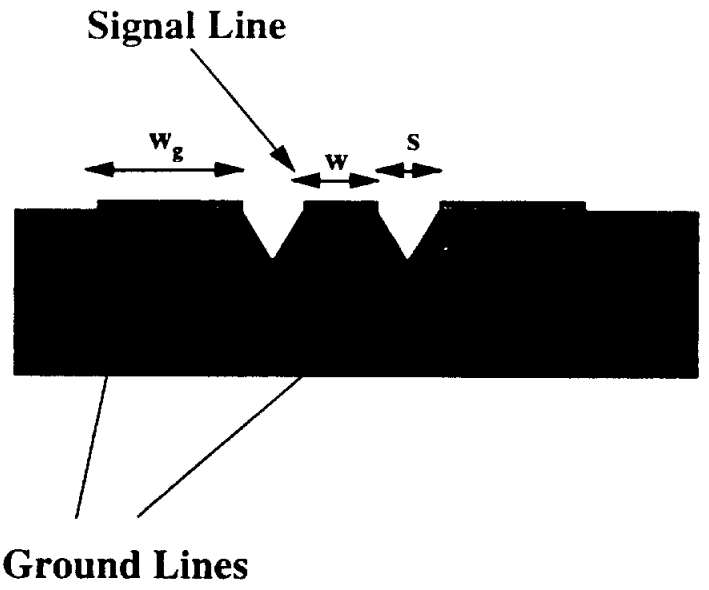


Figure 6.2: Micromachined FGC lines ([3]).

with each diode having twice the area of the previous ones. As a result, the diode impedance will be reduced by a factor of two but the series combination of two diodes will have the same impedance as one smaller diode and, thus, not require the low impedance section at the input for matching. Such a doubler should give an efficiency around 16-17% and achieve an output power higher than 150 mW.

Besides doublers, a monolithic W-band finite ground coplanar tripler can be pursued. Matching and isolation networks at the input and output sides can be implemented with appropriate bandpass filters.

6.2.4 Sub-millimeter Wave Multipliers

One of the advantages of FGC circuits is that they can be easily scaled to higher frequencies. A D-band doubler from 90 to 180 GHz with broadband performance can, therefore, be pursued. Since the novel fabrication technique that was introduced in chapter 5 allows the co-existence of finger type diodes with low parasitics along with air-bridges for the FGC

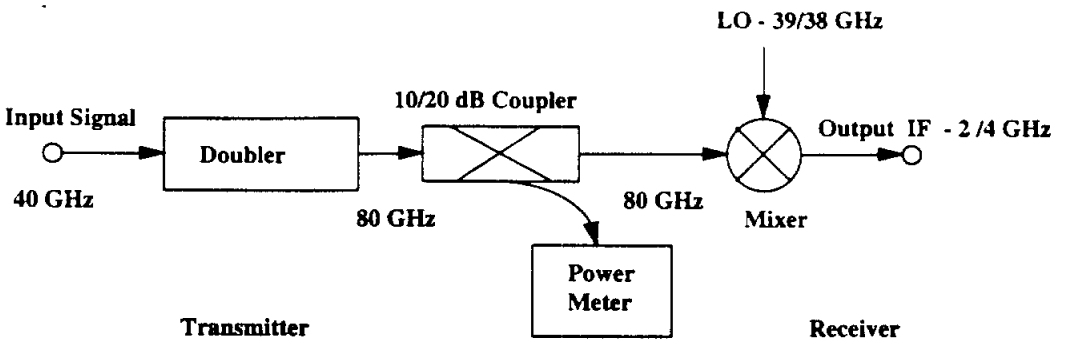


Figure 6.3: Conceptual block diagram of a monolithic multiplier/mixer pair with FGC line technology for on-wafer measurements.

circuits, a D-band doubler design based on this technique would be highly recommended in order to maximize the efficiency. A two diode design where the area of each device is small or a four diode design with larger areas can be implemented. To the author's knowledge a broadband monolithic doubler has not been realized yet in D-band.

6.2.5 Monolithic Transmit/Receive Modules

The novel fabrication technique that was presented in chapter 5 paves the way for the realization of a monolithic FGC based transmitter/receiver in W-band with good performance and wide bandwidth. A design that incorporates a 40 to 80 GHz doubler together with a x2 subharmonic mixer at 80 GHz, as the one shown in Fig. 6.3, can be pursued. A 10/20 dB FGC line coupler is used to sample the RF power that exits the doubler and enters into the mixer, so that on-wafer measurements are possible. Since the same substrate will host both the multiplier and the mixer a compromise in the epi-layer parameters has to be reached. For this reason the mixer fabrication has to be repeated first in order to get the correct diode characteristics and measure the corresponding conversion loss. At the same time a doubler design with channel etched finger type diodes on a low doped layer with 2000 $\AA$ thickness and $3x10^{17}cm^{-3}$ doping needs to be evaluated. The final design that can

be pursued is that of a monolithic transmitter and receiver on separate wafers but with the same parameters that also include micromachined patch antennas for increased radiation efficiency.

APPENDICES

APPENDIX A

QUASI-STATIC MODEL FOR THE EVALUATION OF THE EFFECTIVE DIELECTRIC CONSTANT AND EXPERIMENTAL RESULTS FOR 2 PATCH ANTENNAS ON SILICON

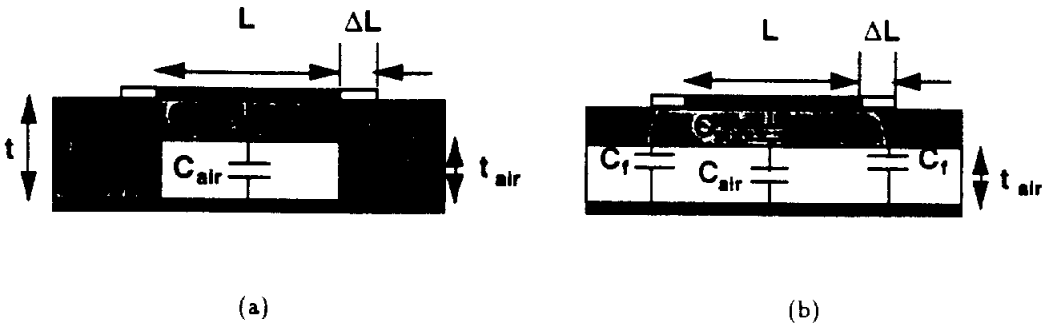
A.1 Calculation of Reduced Dielectric Constant

A cavity model developed by R.F. Drayton [38] is used to predict the effective dielectric constant of the mixed air-silicon region of the micromachined antenna (Fig. A.2) for varying thickness ratios underneath the patch antenna. A quasi-static model, based on series capacitors, is used to determine the patch capacitance in the mixed region (Fig. A.1)

$$C = \frac{\epsilon_{eff} A}{t} \tag{A.1}$$

where $\epsilon_{eff} = \epsilon_{reff}\epsilon_o$. For simplicity the walls of the cavity are asumed to be vertical and the effective dielectric constant (ϵ_{reff}) is estimated by the following expression:

$$\epsilon_{reff} = \epsilon_{cavity}\left(\frac{L + 2\Delta L \frac{\epsilon_{fringe}}{\epsilon_{cavity}}}{L + 2\Delta L}\right) \tag{A.2}$$



(a) (b)

Figure A.1: Capacitor model for the micromachined patch with (a) the radiating edges into the high-index substrate and (b) with the radiating edges over the mixed air-substrate region.

where

$$\frac{\epsilon_{fringe}}{\epsilon_{cavity}} = \frac{\epsilon_{air} + (\epsilon_{sub} - \epsilon_{air})x_{air}}{\epsilon_{air} + (\epsilon_{sub} - \epsilon_{air})x_{fringe}} \tag{A.3}$$

$$\epsilon_{cavity} = \frac{\epsilon_{air}\epsilon_{sub}}{\epsilon_{air} + (\epsilon_{sub} - \epsilon_{air})x_{air}} \tag{A.4}$$

In the above expressions, ϵ_{cavity} represents the relative dielectric constant of the mixed substrate region and ϵ_{fringe} represents the relative dielectric constant in the fringing fields region. Equation A.2 includes the open-end effect extension length ΔL to the antenna which can be found from [44], where ϵ_{fringe} is the permittivity used for the calculation of ΔL. The thickness parameters, x_{air} and x_{fringe}, are ratios of the air to full substrate thickness in the mixed and fringing field regions, respectively. For the silicon micromachined case shown in Fig. A.1(a) x_{fringe} is taken as zero, whereas for the case of Fig. A.1(b) x_{fringe}=x_{air}.

A plot of the theoretical and measured effective dielectric constant versus the air gap thickness for silicon substrate (ϵ_r=11.7) can be found in Fig. A.3 , where an effective dielectric constant of approximately 2.2 is achieved for a mixed air-silicon ratio of 1:1 using the capacitor model (eq. A.2 with ΔL=0) and 3:1 ratio for the capacitor model with ΔL extension length (eq. A.2 with ΔL calculated from [44]). The dimensions for the micromachined patch that was used to produce the results of Fig. A.3 can be found in Table A.1

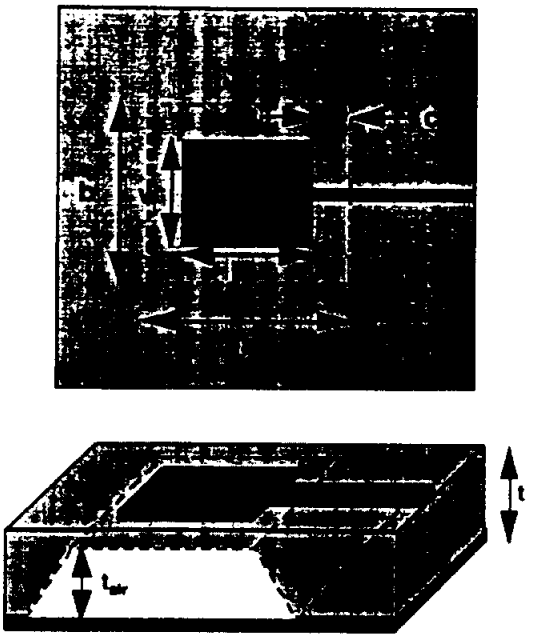


Figure A.2: Geometry of the micromachined patch antenna.

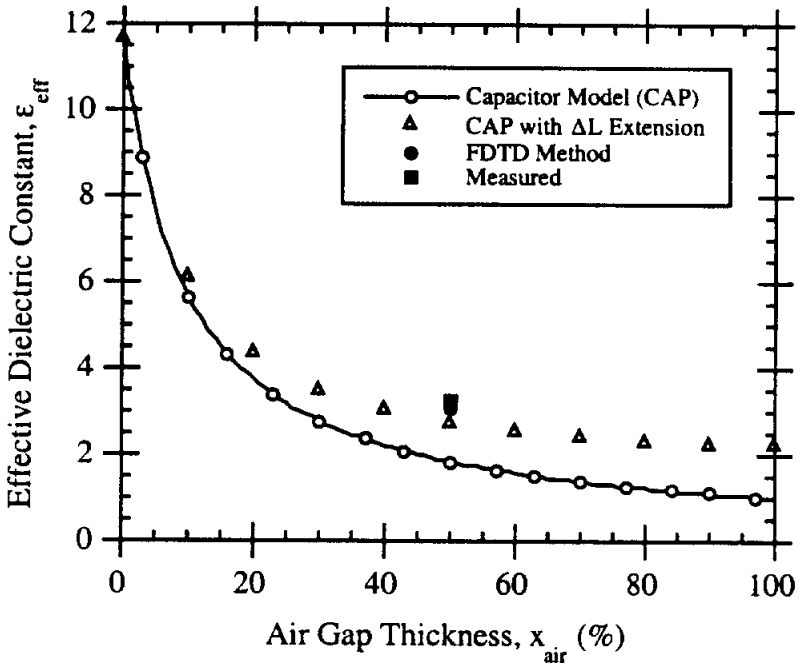


Figure A.3: Effective dielectric constant vs. air-gap thickness for the silicon micromachined patch

(parameters a,b and c are actual values since the walls are assumed vertical). Included also in Fig. A.3 is a data point based on the finite difference time domain model of the micromachined patch geometry. The FDTD calculation was based on a 3-D full-wave scheme that yields the return loss of the micromachined antenna and the effective permittivity of an 1:1 air-silicon substrate for a range of frequencies. Once the resonant frequency is determined from the return loss, the effective permittivity of interest is found. Only one case of air-silicon substrate ratio has been simulated with FDTD in order to validate the quasi-static results for the effective dielectric constrant of the antenna that was fabricated and tested. Regarding the measured ("micromachined") data point of Fig. A.3, the resonant frequency of the fabricated antenna was measured and [98] was used to extract the dielectric constant of the substrate for a patch having the same dimensions as the measured one. In the following section, experimental data will be presented that prove the superiority of this type of micromachined antenna. The conventional and micromachined antennas will be defined as a patch fabricated on a regular substrate or as a patch fabricated on a substrate that has locally reduced index region, respectively.

A.2 K-Band Micromachined Patch

Two antennas were fabricated by R.F. Drayton [38] on silicon, with resonant frequencies in the K-band and air/substrate thickness ratios of 1:1 (see Table A.1 for dimensions). In the silicon micromachined patch (SMP) antenna, the conductor has been electroplated to a metal thickness of approximately 3.2 μm and the substrate is chemically etched (EDP process) in a single etch step underneath the antenna. Since the walls of the resulting cavity are not vertical due to the anisotropic etching, dimensions for a, b and c in Table A.1 represent average values. The lower ground plane is achieved by attaching adhesive

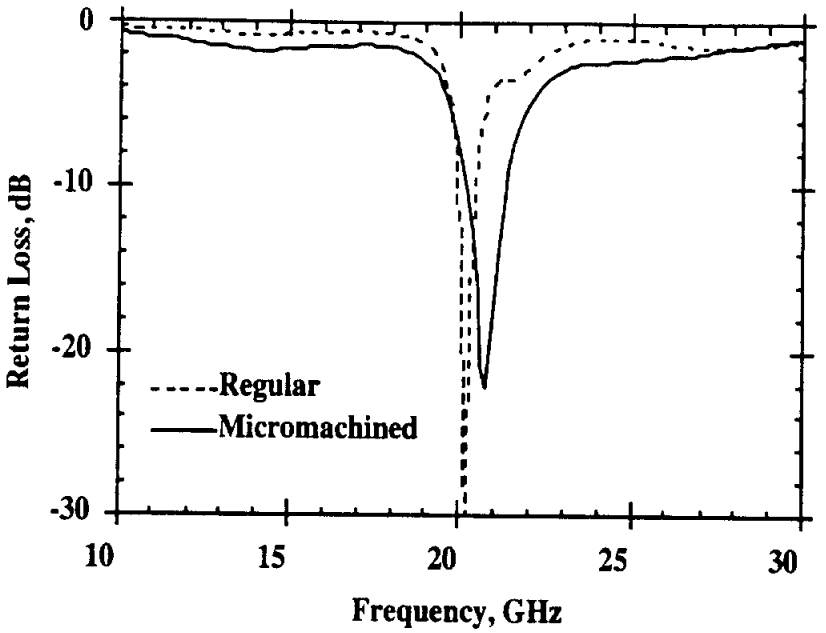


Figure A.4: Return loss measurement of the regular and micromachined patch antenna printed on a full thickness substrate and substrate with mixed air-silicon thickness ratio (1:1), respectively.

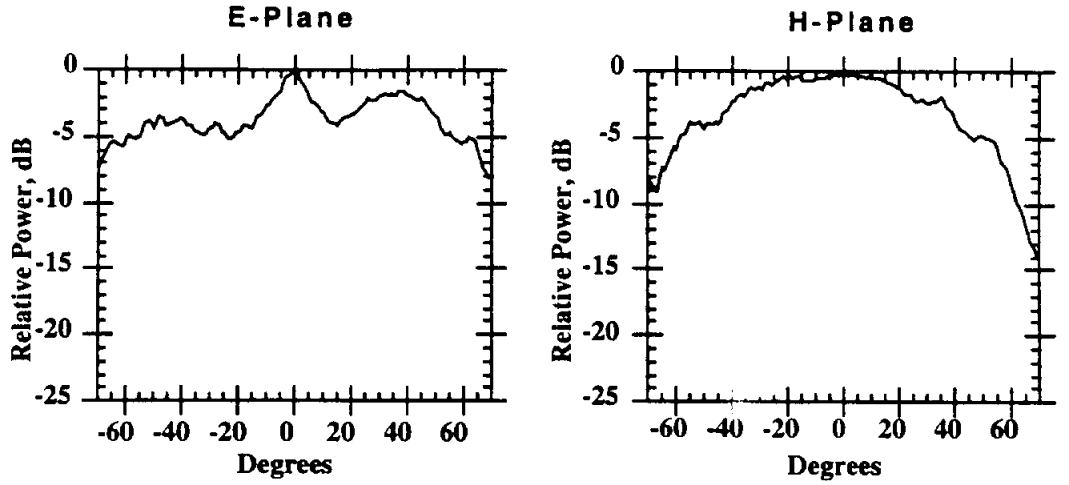
copper tape of 25.4 μm thickness and the size of the silicon substrate where the antennas were fabricated was approximately 2.8 cm x 3 cm. Return loss measurements are shown in Fig. A.4 and were obtained using an HP 8510 Network Analyzer where the bandwidth ($|S11| \leq$ -10 dB) increases from 2.9% for the "regular" antenna to 5% for the SMP. Since bandwidth is inversely proportional to the quality factor, Q,defined as the ratio of total energy stored in the antenna to the energy dissipated or radiated from the antenna, the increase in bandwidth provides the first indicator of an increase in total radiation from the antenna. Efficiency measurements, however, need to be made in order to observe the increase in power radiated into space waves as opposed to power radiated into surface waves.

Radiation patterns were also taken for the two antennas and the results are shown in Fig. A.5 where significant differences in the E-plane pattern are observed, while the H-plane patterns remain similar as expected. For measurement purposes, the silicon substrates that hosted the antennas were mounted on a 5.6 cm x 5 cm metallic holder that served as

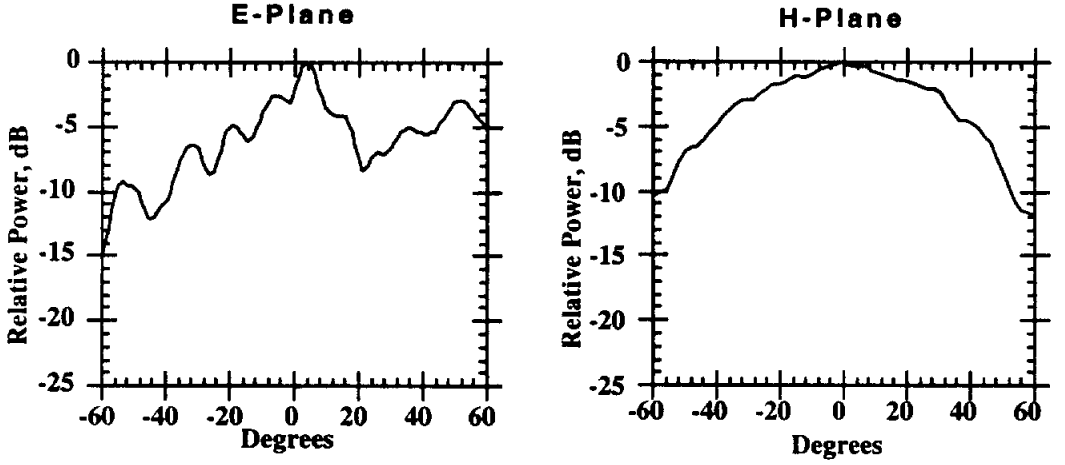
Patch	t(mm)	t_{air}(mm)	L(mm)	w(mm)	a(mm)	b(mm)	c(mm)
Regular	0.355	0	2.019	4.08	0	0	0
Micromachined	0.355	0.165	3.616	3.445	3.616	8.108	0

Table A.1: Design parameters for the antennas on Silicon substrate

the ground plane. The silicon antenna pattern exhibits many ripples, that are due to the diffraction of strong surface waves from the edges of the finite ground plane, in contrast to the micromachined antenna pattern that is much smoother. Conclusive evidence, needed to show the suppression of surface waves, is obtained by evaluating the antenna gain and measured efficiency.



(a)



(b)

Figure A.5: Radiation patterns for (a) the micromachined antenna on Silicon and (b) the regular antenna on Silicon.

APPENDIX B

FABRICATION PROCESS OF W-BAND AND D-BAND MULTIPLIERS

B.1 Wafer Preparation

A cross section of the GaAs wafer used for the fabrication of frequency doublers can be seen in Fig. B.1. The epi layers consist of a 4000 $\AA$ (W band) or 2000 $\AA$ (D band) thick n^- layer with a 10^{17} and $3x10^{17}cm^{-3}$ doping density , respectively, and a 2 μm thick n^+ layer with a doping density greater than $5x10^{18}cm^{-3}$. Both of the previous layers as well as an AlGaAs layer used to stop the etch are supported on a semi-insulating GaAs substrate.

- Clean the wafer in heated Xylene for 2 minutes, Methanol for 1 minute, heated Acetone

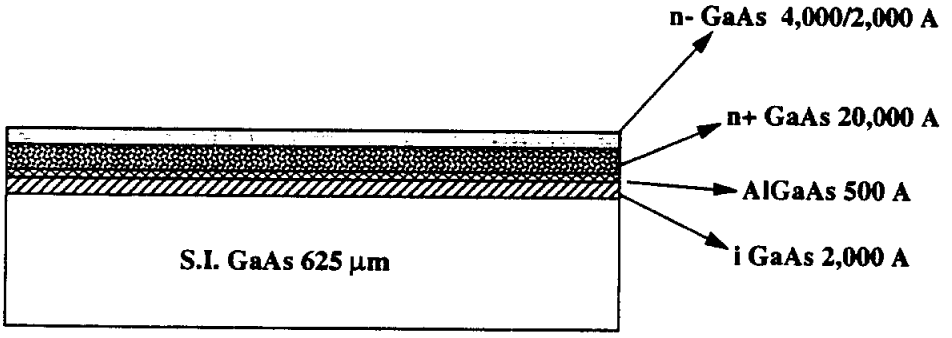


Figure B.1: Cross section of the GaAs wafer used for the fabrication of active structures.

for 2 minutes, and IPA for 1 minute.

- Etch native oxide in BHF for 30 seconds to 1 minute.
- Bake for dehydration on the hot plate at $130°C$ for 2 minutes.

B.2 Ohmic Cathode Contact

- Lithography (image reversal): Spin HMDS adhesion promoter and AZ5214-E photoresist at 4.5 Krpm for 30 seconds each. Pre-bake on the hot plate at $110°C$ for 2 minutes. Remove the edge beaded resist by exposing the edges with the MJB-3 aligner for 45 seconds and developing in AZ-327 MIF for 30 seconds (the intensity of the aligner is set to 20 mW/cm^2). Next, pattern the "ohmic" image by exposing for 3-4 seconds with the MJB-3. Post-bake on the hot plate at $130°C$ for 1 minute. Flood expose with the MJB-3 for 1.2 minutes. Develop the photoresist with AZ-327 MIF developer for 30 seconds. Finally, bake at $110°C$ for 1 minute in order to further strengthen the resist for a BHF dip.
- Remove the photoresist scum in the plasma asher at 80 W and 250 mT of O_2 for 1 minute.
- Etch through the epitaxial low doped layer with $H_3PO_4 : H_2O_2 : H_2O$ (1:1:8) for 20 seconds (2000 $\AA$ thick n^- layer) or 36 seconds (4000 $\AA$ thick n^- layer).
- Etch the native oxide with BHF for 15-20 seconds.
- Deposit ohmic metal layers of Ni/Ge/Au/Ti/Au (250/325/650/450/2500 $\AA$) in the e-beam evaporator.
- Lift-off in heated PRS-1000 photoresist stripper for 60 minutes.

- Anneal the ohmic contacts using hot plates at $240°/405°/240°C$ for 20/40/20 seconds.

B.3 Schottky Anode Definition

- Lithography (image reversal): Spin HMDS adhesion promoter and AZ5214-E photoresist at 4.5 Krpm for 30 seconds each. Pre-bake on the hot plate at $110°C$ for 2 minutes. Remove the edge beaded resist by exposing the edges with the MJB-3 aligner for 45 seconds and developing in AZ-327 MIF for 30 seconds. Next, pattern the "anode" image by exposing for 3-4 seconds with the MJB-3. Post-bake on the hot plate at $130°C$ for 1 minute. Flood expose with the MJB-3 for 1.2 minutes. Develop the photoresist with AZ-327 MIF developer for 30 seconds. Finally, bake at $110°C$ for 1 minute in order to further strengthen the resist for a BHF dip.

- Remove the photoresist scum in the plasma asher at 80 W and 250 mT of O_2 for 1 minute.

- Etch the native oxide with BHF for 15-20 seconds (must load into evaporator no later than 2 minutes).

- Deposit Schottky barrier metal layers of Ti/Pt/Au (500/500/3000 $\AA$) in the e-beam evaporator.

- Lift-off in heated PRS-1000 photoresist stripper for 60 minutes.

B.4 Mesa Etch

- Lithography: Spin HMDS adhesion promoter and AZ5214-E photoresist at 2.5 Krpm for 30 seconds each. Pre-bake on the hot plate at $110°C$ for 2 minutes. Remove the

edge beaded resist by exposing the edges with the MJB-3 aligner for 45 seconds and developing in AZ-327 MIF for 30 seconds. Next, pattern the "etch" image by exposing for 4.5 seconds with the MJB-3. Develop the photoresist with AZ-327 MIF developer for 45 seconds. Finally, hard bake on the hot plate at 130°C for 1 minute.

- Remove the photoresist scum in the plasma asher at 80 W and 250 mT of O_2 for 1 minute.

- Etch mesa with $NH_4OH : H_2O_2$ (1:24) for 25-30 seconds (etch rate is $4\mu m/min$). Rinse but without drying, immediately follow with an oxide etch in $NH_4OH : H_2O$ (1:15) for 15 seconds.

- Remove the photoresist in Acetone and IPA.

B.5 Circuit Printing

- Lithography (image reversal): Spin HMDS adhesion promoter and AZ5214-E photoresist at 2.5 Krpm for 30 seconds each. Pre-bake on the hot plate at 110°C for 2 minutes. Remove the edge beaded resist by exposing the edges with the MJB-3 aligner for 45 seconds and developing in AZ-327 MIF for 30 seconds. Next, pattern the "circuit" image by exposing for 3-4 seconds with the MJB-3. Post-bake on the hot plate at 130°C for 1 minute. Flood expose with the MJB-3 for 1.2 minutes. Finally, develop the photoresist with AZ-327 MIF developer for 20-30 seconds (initially 20 secs and then 5 secs increments).

- Deposit the circuit metal layers Ti/Al/Ti/Au (500/6000/500/3000 $\AA$) in the e-beam evaporator.

- Lift-off in heated PRS-1000 photoresist stripper for 3 hours.

B.6 Air-Bridge Formation

B.6.1 Post Definition

- Lithography: Spin HMDS adhesion promoter and PR1827 photoresist at 3.0 Krpm for 30 seconds each. Pre-bake on the hot plate at $105°C$ for 1 minute. Remove the edge beaded resist by exposing the edges with the MJB-3 aligner for 1 minute and developing in AZ-327 MIF for 45 seconds. Next, pattern the "post" image by exposing for 9-10 seconds with the MJB-3. Finally, develop the photoresist with MF351:H_2O (1:5) developer for 30-45 seconds.

- Remove the photoresist scum in the plasma asher at 80 W and 250 mT of O_2 for 1 minute.

- Contour bake for 2 minutes on a metal block which has been heating in a $130°C$ oven for at least 30 minutes.

- Deposit the plating membrane of Ti/Au/Ti (500/2000/500 $\AA$) in the e-beam evaporator.

B.6.2 Span Definition

- Lithography: Spin PR1827 photoresist only at 3.0 Krpm for 30 seconds. Soft bake in the oven at $80°C$ for 20 minutes. Remove the edge beaded resist by exposing the edges with the MJB-3 aligner for 1 minute and developing in AZ-327 MIF for 45 seconds. Next, pattern the "span" image by exposing for 18-20 seconds with the

MJB-3. Finally, develop the photoresist with MF351:H_2O (1:5) developer for 30-45 seconds.

- Remove the photoresist scum in the plasma asher at 80 W and 250 mT of O_2 for 1 minute.
- Dektak the photoresist profile and record the photoresist height around the air-bridges.
- Remove the top layer of Ti with HF:H_2O (1:10) for 5-6 seconds.
- Electroplate the air-bridges with 2-3μm of Au.

B.6.3 Sacrificial Layer Removal

- Flood expose with the MJB-3 for 3 minutes and develop the photoresist with MF351:H_2O (1:5) developer for 1 minute.
- Remove the top layer of Ti with HF:H_2O (1:10) for 5-6 seconds.
- Remove the middle layer of Au with Au etchant solution for 1 minute.
- Remove the bottom layer of Ti with HF:H_2O (1:10) for 5-6 seconds.
- Remove the first layer of photoresist in heated PRS-1000 resist stripper for 60 minutes.
- If there is photoresist scum then remove with plasma asher at 150 W and 250 mT of O_2 for 5 minutes.

APPENDIX C

FABRICATION PROCESS FOR MONOLITHIC MIXERS AND MULTIPLIERS IN A TRANSMIT/RECEIVE MODULE.

C.1 PECVD Si_xN_y Deposition

- Clean the wafer in heated Acetone for 2 minutes and IPA for 2 minutes.
- Etch native oxide in $NH_4OH : H_2O$ (1:15) for 30 seconds.
- Bake for dehydration on the hot plate at $130°C$ for 2 minutes.
- Si_xNy deposition of 2400 $\AA$ according to table C.1.

C.2 Schottky Well Formation

The pattern is aligned to the edges of the wafer in such a way that the diode fingers are parallel to the slow undercut direction ($\prec 1\bar{1}1 \succ$).

- Lithography (image reversal): Spin HMDS adhesion promoter and AZ5214-E photoresist at 6.5 Krpm for 30 seconds each. Pre-bake on the hot plate at $110°C$ for

Gas/Flow	SiH_4/30 sccm
Gas/Flow	NH_3/6.4 sccm
Gas/Flow	Ar/40 sccm
Pressure	100 mT
Power	20 W
Time	80 min
Temperature	300°C
Thickness	2400 $\AA$
BHF etch rate	850 $\AA$/min
Index of refraction	1.85

Table C.1: PECVD Si_xN_y deposition.

2 minutes. Remove the edge beaded resist by exposing the edges with the MJB-3 aligner for 45 seconds and developing in AZ-327 MIF for 30 seconds (the intensity of the aligner is set to 20 mW/cm^2). Next, pattern the "schottky" image by exposing for 3 seconds with the MJB-3. Post-bake on the hot plate at 130°C for 1 minute. Flood expose with the MJB-3 for 1.5 minutes. Develop the photoresist with AZ-327 MIF developer for 40 seconds. If the small features have not developed then repeat in increments of 10 seconds.

- Reactive Ion Etch (RIE):Dry etch the Si_xN_y from 2400 $\AA$ to 200-300 $\AA$. Not all of the nitride should be removed, because the plasma will damage the GaAs surface. Insert the wafer in the plasma etcher and use O_2 and CF_4 for a total etch time of 3-3.5 minutes. Initially do a 1 min etch and then continue with 20 second etches. The etch depth can be monitored using a Leitz MPV-SP dielectric thickness measurement

system that measures the Si_xN_y in rectangular areas of $100\mu m$ x $300\mu m$. These rectangles should be in different areas of the wafer.

C.3 Ohmic Contact Definition

- Lithography (image reversal): Spin HMDS adhesion promoter and AZ5214-E photoresist at 4.5 Krpm for 30 seconds each. Pre-bake on the hot plate at $110°C$ for 2 minutes. Remove the edge beaded resist by exposing the edges with the MJB-3 aligner for 45 seconds and developing in AZ-327 MIF for 30 seconds. Next, pattern the "ohmic" image by exposing for 3 seconds with the MJB-3. Post-bake on the hot plate at $130°C$ for 1 minute. Flood expose with the MJB-3 for 1.5 minutes. Develop the photoresist with AZ-327 MIF developer for 30 seconds. Finally, bake at $110°C$ for 1 minute in order to further strengthen the resist for a BHF dip.

- Reactive Ion Etch (RIE): Remove the Si_xN_y from the areas of the ohmic contact by doing a 5 min plasma etch.

- Etch through the epitaxial low doped layer with $H_3PO_4 : H_2O_2 : H_2O$ (1:1:8) for 20 seconds (2000 $\AA$ thick n^- layer) or 36 seconds (4000 $\AA$ thick n^- layer).

- Etch the native oxide with BHF for 15-20 seconds. This etch also undercuts the Si_xN_y layer which is beneficial in the reduction of stress when the ohmic contacts will be annealed.

- Deposit ohmic metal layers of Ni/Ge/Au/Ti/Au (250/325/650/450/2500 $\AA$) in the e-beam evaporator.

- Lift-off in heated PRS-1000 photoresist stripper for 60 minutes.

- Anneal the ohmic contacts using hot plates at 240°/405°/240°C for 20/40/20 seconds.

C.4 Finger/Anode Definition

- Lithography (image reversal): Spin HMDS adhesion promoter and AZ5214-E photoresist at 4.5 Krpm for 30 seconds each. Pre-bake on the hot plate at 110°C for 2 minutes. Remove the edge beaded resist by exposing the edges with the MJB-3 aligner for 45 seconds and developing in AZ-327 MIF for 30 seconds. Next, pattern the "finger" image by exposing for 3 seconds with the MJB-3. Post-bake on the hot plate at 130°C for 1 minute. Flood expose with the MJB-3 for 1.5 minutes. Develop the photoresist with AZ-327 MIF developer for 30 seconds. Finally, bake at 110°C for 1 minute in order to further strengthen the resist for a BHF dip.

- Remove the remaining Si_xN_y and native oxide with a BHF etch for 30 seconds (must load into evaporator no later than 2 minutes).

- Deposit Schottky barrier metal layers of Ti/Pt/Au (500/500/3000 $\AA$) in the e-beam evaporator.

- Lift-off in heated PRS-1000 photoresist stripper for 60 minutes.

C.5 Mesa Etch

In this step the epi layers are removed everywhere from the wafer except for small rectangular areas around the diodes. This is necessary so that the passive circuits are sitting on semi-insulating GaAs and not active layers. The finger etch will follow after the circuit deposition. During the design of the mask for this layer, enough space should be left around the diodes in order to minimize the undercut.

- Lithography: Spin HMDS adhesion promoter and AZ5214-E photoresist at 2.5 Krpm for 30 seconds each. Pre-bake on the hot plate at $110°C$ for 2 minutes. Remove the edge beaded resist by exposing the edges with the MJB-3 aligner for 45 seconds and developing in AZ-327 MIF for 30 seconds. Next, pattern the "etch" image by exposing for 4.5 seconds with the MJB-3. Develop the photoresist with AZ-327 MIF developer for 45 seconds. Finally, hard bake on the hot plate at $130°C$ for 1 minute.

- Reactive Ion Etch (RIE): Remove the Si_xN_y from the areas that will be etched by doing a 5 min plasma etch.

- Etch mesa with $NH_4OH : H_2O_2$ (1:24) for 25-30 seconds (etch rate is $4\mu m/min$). Rinse but without drying, immediately follow with an oxide etch in $NH_4OH : H_2O$ (1:15) for 15 seconds.

- Remove the photoresist in Acetone and IPA.

C.6 Circuit Printing

- Lithography (image reversal): Spin HMDS adhesion promoter and AZ5214-E photoresist at 2.5 Krpm for 30 seconds each. Pre-bake on the hot plate at $110°C$ for 2 minutes. Remove the edge beaded resist by exposing the edges with the MJB-3 aligner for 45 seconds and developing in AZ-327 MIF for 30 seconds. Next, pattern the "circuit" image by exposing for 3-4 seconds with the MJB-3. Post-bake on the hot plate at $130°C$ for 1 minute. Flood expose with the MJB-3 for 1.2 minutes. Finally, develop the photoresist with AZ-327 MIF developer for 20-30 seconds (initially 20 secs and then 5 secs increments).

- Deposit the circuit metal layers Ti/Al/Ti/Au (500/6000/500/3000 $\AA$) in the e-beam

evaporator.

- Lift-off in heated PRS-1000 photoresist stripper for 3 hours.

C.7 Finger Etch

In this step the epi layers underneath the fingers of the diodes are etched.

- Lithography: Spin HMDS adhesion promoter and AZ5214-E photoresist at 2.5 Krpm for 30 seconds each. Pre-bake on the hot plate at $110°C$ for 2 minutes. Remove the edge beaded resist by exposing the edges with the MJB-3 aligner for 45 seconds and developing in AZ-327 MIF for 30 seconds. Next, pattern the "finger etch" image by exposing for 4.5 seconds with the MJB-3. Develop the photoresist with AZ-327 MIF developer for 45 seconds. Finally, hard bake on the hot plate at $130°C$ for 1 minute.

- Reactive Ion Etch (RIE): Remove the Si_xN_y from the areas that will be etched by doing a 5 min plasma etch.

- Etch mesa with $NH_4OH : H_2O_2$ (1:24) for 15-20 seconds (etch rate is $4\mu m/min$). Rinse but without drying, immediately follow with an oxide etch in $NH_4OH : H_2O$ (1:15) for 15 seconds.

- Remove the photoresist in Acetone and IPA.

C.8 Air-Bridge Formation

C.8.1 Post Definition

- Lithography: Spin HMDS adhesion promoter and PR1827 photoresist at 3.0 Krpm for 30 seconds each. Pre-bake on the hot plate at $105°C$ for 1 minute. Remove the

edge beaded resist by exposing the edges with the MJB-3 aligner for 1 minute and developing in AZ-327 MIF for 45 seconds. Next, pattern the "post" image by exposing for 9-10 seconds with the MJB-3. Finally, develop the photoresist with MF351:H_2O (1:5) developer for 30-45 seconds.

- Remove the photoresist scum in the plasma asher at 80 W and 250 mT of O_2 for 1 minute.
- Contour bake for 2 minutes on a metal block which has been heating in a 130°C oven for at least 30 minutes.
- Deposit the plating membrane of Ti/Au/Ti (500/2000/500 $\AA$) in the e-beam evaporator.

C.8.2 Span Definition

- Lithography: Spin PR1827 photoresist only at 3.0 Krpm for 30 seconds. Soft bake in the oven at 80°C for 20 minutes. Remove the edge beaded resist by exposing the edges with the MJB-3 aligner for 1 minute and developing in AZ-327 MIF for 45 seconds. Next, pattern the "span" image by exposing for 18-20 seconds with the MJB-3. Finally, develop the photoresist with MF351:H_2O (1:5) developer for 30-45 seconds.
- Remove the photoresist scum in the plasma asher at 80 W and 250 mT of O_2 for 1 minute.
- Dektak the photoresist profile and record the photoresist height around the air-bridges.
- Remove the top layer of Ti with HF:H_2O (1:10) for 5-6 seconds.

- Electroplate the air-bridges with 2-3μm of Au.

C.8.3 Sacrificial Layer Removal

- Flood expose with the MJB-3 for 3 minutes and develop the photoresist with MF351:H_2O (1:5) developer for 1 minute.
- Remove the top layer of Ti with HF:H_2O (1:10) for 5-6 seconds.
- Remove the middle layer of Au with Au etchant solution for 1 minute.
- Remove the bottom layer of Ti with HF:H_2O (1:10) for 5-6 seconds.
- Remove the first layer of photoresist in heated PRS-1000 resist stripper for 60 minutes.
- If there is photoresist scum then remove with plasma asher at 150 W and 250 mT of O_2 for 5 minutes.

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