

Distributed MEMS Transmission Lines

by

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To my family.

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TABLE OF CONTENTS

DEDICATION	ii
ACKNOWLEDGEMENTS	iii
LIST OF TABLES	vii
LIST OF FIGURES	viii
LIST OF APPENDICES	xiv
CHAPTERS	
1 Introduction	1
2 Mechanical Properties of Fixed-Fixed Beams	7
2.1 Spring Constant	7
2.2 Electrostatic Actuation	14
2.3 Stabilization of Electrostatically Actuated Bridges	19
2.4 Frequency Response	23
2.5 Brownian Noise Analysis	24
3 Distributed MEMS Transmission Lines	27
3.1 Fabrication of the DMTL	28
3.2 Analytic Modeling of Distributed Lines	30
3.3 Loss on Distributed Lines	33
3.4 DMTL Circuit Modeling	36
3.5 DMTL Measurements	37
3.6 Comparison of Analytic and Circuit Model	45
3.7 Conclusion	47
4 Distributed MEMS Transmission Line Phase Shifters	49
4.1 Design	50
4.2 Optimization	55
4.2.1 Theory	55
4.2.2 Experiment	64
4.3 W-Band DMTL Phase Shifter	69
4.4 Stabilized DMTL Phase Shifter	78

5	Applications of Distributed MEMS Transmission Lines	81
5.1	Reflective Switches	81
5.1.1	Design and Measurements	83
5.1.2	Switching Speed	87
5.2	Phase Modulators	94
5.3	Phase Verniers	103
5.4	Power Handling Measurement	103
6	Conclusions and Future Work	105
6.1	Very Low Loss Phase Shifters	105
6.2	Wideband Switches	106
6.3	Modulators	107
6.4	Development of High-Q Varactors	108
	APPENDICES	109
	BIBLIOGRAPHY	128

LIST OF TABLES

Table

2.1	Dimensions of bridges used in Figure 2.7.	15
2.2	Quality factors for bridges in Figure 2.16.	24
2.3	Low-frequency rms Brownian-noise position values for the bridges used in Figure 2.16 in $\text{\AA}/\sqrt{\text{Hz}}$	26
3.1	Bragg Frequency Calculations from (3.8) and (3.12)	33
3.2	Fitted Model Parameters for DMTL with $w/s = 30/306 \mu\text{m}$	40
3.3	Fitted Model Parameters for DMTL with $w/s = 60/640 \mu\text{m}$	43
3.4	DMTL parameters for Figure 3.14.	47
3.5	DMTL parameters for Figure 3.15.	47
4.1	Modeling parameters for DMTL in Figure 4.1.	51
4.2	Specifications for examples in Figures 4.3-4.7.	55
4.3	Specifications of the DMTLs used to verify the optimization procedure. . .	64
4.4	Dimensions of the DMTLs used to verify the optimization. The Bragg frequency is calculated using $L_b = 20 \text{ pH}$. $R_b = 0.15 \Omega$ at 30 GHz.	64
4.5	Circuit model parameters for the optimal DMTL ($W = 100 \mu\text{m}$).	66
4.6	Calculated design of an optimized W-band DMTL phase shifter on quartz.	74
4.7	Dimensions for the optimized W-band DMTL phase shifter.	74
4.8	Circuit model parameters for the W-band DMTL phase shifter.	74
4.9	Circuit model parameters for the optimal DMTL with integrated capacitors.	80
5.1	Parameters of the gold bridge used in the calculation of Figure 5.9.	91
5.2	Measured and modeled switching speed in μs ($Q = 2.3$).	94
5.3	Calculated switching speeds, in μs , from the numerical solution for varying Q values.	94
5.4	Measured, theoretical, and modeled RF spectrum of the BPSK signal in dBc.	99
5.5	Parameters of the gold bridge used in the calculation of Figure 5.15.	99
5.6	Parameters of the gold bridge used in the calculation of Figure 5.17.	101
D.1	PECVD Si_xN_y recipe [42].	124
D.2	PECVD Si_xN_y reactive ion etching (RIE) recipe.	125

LIST OF FIGURES

Figure

1.1	Cantilever MEMS bridge in a series configuration along a microstrip or CPW transmission line.	2
1.2	Circuit model for a series capacitive MEMS switch with the capacitance switching from 20 fF to 2 pF.	2
1.3	Circuit simulation of series switch using the model in Figure 1.2.	2
1.4	Fixed-fixed beam MEMS bridge in shunt configuration over a CPW transmission line.	3
1.5	Circuit model for a shunt capacitive MEMS switch with the capacitance switching from 35 fF to 3.5 pF.	3
1.6	Circuit simulation of a shunt switch using the model in Figure 1.5.	3
1.7	Top view of a CPW line periodically loaded by shunt MEMS bridges. . . .	5
2.1	Fixed-fixed beam with concentrated vertical load P	7
2.2	Fixed-fixed beam over a CPW line with the force, $P = \xi l/3$, evenly distributed above the CPW center conductor.	9
2.3	Beam modeled as a stretched wire with concentrated vertical load P	10
2.4	Spring constant of a gold bridge ($E = 80$ GPa, $\nu = 0.42$) with lengths of 200 μm (—) and 400 μm (---). For each bridge length the spring constant is evaluated for biaxial residual stresses of 0, 50, and 100 MPa. The spring constant scales linearly with the bridge width which is held constant at 35 μm . 12	
2.5	Spring constant of an aluminum bridge ($E = 69$ GPa, $\nu = 0.33$) with lengths of 200 μm (---) and 400 μm (---). For each bridge length the spring constant is evaluated for biaxial residual stresses of 0, 50, and 100 MPa. The spring constant scales linearly with the bridge width which is held constant at 35 μm . 12	
2.6	Critical stress of a (a) gold ($E = 80$ GPa, $\nu = 0.42$) and (b) aluminum ($E = 69$ GPa, $\nu = 0.33$) bridge vs. thickness for 200 μm (—) and 400 μm (---) long bridges.	13
2.7	Bridge height versus applied voltage with a zero-bias bridge height of 1.2 μm and 3 μm . The bridge parameters, given in Table 2.1, are chosen to result in a pull-down voltage of 22 V.	14

2.8	Pull-down voltage of a (a) gold ($E = 80$ GPa, $\nu = 0.42$) and (b) aluminum ($E = 69$ MPa, $\nu = 0.33$) bridge vs. bridge thickness for $200\text{ }\mu\text{m}$ (—) and $400\text{ }\mu\text{m}$ (---) long bridges. For each bridge length the pull-down voltage is calculated for biaxial residual stresses of 0, 50, and 100 MPa. The pull-down voltage depends on the bridge height as $g_o^{3/2}$ and g_o is $1.5\text{ }\mu\text{m}$	17
2.9	Pull-down voltage of a (a) gold ($E = 80$ GPa, $\nu = 0.42$) and (b) aluminum ($E = 69$ MPa, $\nu = 0.33$) bridge vs. bridge height for $200\text{ }\mu\text{m}$ (—) and $400\text{ }\mu\text{m}$ (---) long bridges. For each bridge length the pull-down voltage is calculated for biaxial residual stresses of 0, 50, and 100 MPa. The pull-down voltage depends on the bridge height as $g_o^{3/2}$ and g_o is $1.5\text{ }\mu\text{m}$	17
2.10	Variation of bridge capacitance and gap height with applied voltage. The bridge parameters have been adjusted to result in a pull-down voltage of 22 V, a zero-bias bridge capacitance of 20 fF, and a zero-bias height of $1.2\text{ }\mu\text{m}$	18
2.11	Derivative of the bridge capacitance () and bridge height (---), with respect to the applied voltage, vs. the applied voltage. The bridge parameters have been adjusted to result in a pull-down voltage of 22 V.	18
2.12	Stabilization of an electrostatically actuated MEMS bridge through the use of a series feedback capacitor.	19
2.13	Plot of change in bridge height versus applied voltage as the series feedback capacitor is varied from $0.5C_{bo}$ to ∞ . The zero-bias bridge height is $1.2\text{ }\mu\text{m}$	20
2.14	Stabilization of an electrostatically actuated MEMS bridge, in the presence of significant fringing capacitance, through the use of a series feedback capacitor.	21
2.15	Plot of the change in bridge height versus applied voltage as the series feedback capacitor is varied from $0.5C_{bo}$ to ∞ with a fringing capacitance of $C_f = C_{bo}/3$. The zero-bias bridge height is $1.2\text{ }\mu\text{m}$	22
2.16	Frequency response of a (a) gold ($E = 80$ GPa, $\nu = 0.42$, $\rho = 19320\text{ kg/m}^3$) and (b) aluminum ($E = 69$ MPa, $\nu = 0.33$, $\rho = 2700\text{ kg/m}^3$) bridge for $200\text{ }\mu\text{m}$ (---) and $400\text{ }\mu\text{m}$ (---) long bridges over a CPW line with $W = l/3$. For each bridge length the response is calculated for bridge heights of 1, 2, and $3\text{ }\mu\text{m}$. The width is $35\text{ }\mu\text{m}$, the thickness is $1.5\text{ }\mu\text{m}$, and the residual stress is 50 MPa.	25
3.1	Layout of a DMTL constructed of a CPW line with center conductor width W and total CPW width $W+2G$, and MEMS bridges with width w and spacing s . The DMTL is connected to $50\text{ }\Omega$ feedlines and probe pads for testing.	28
3.2	Details of the fabrication process for the MEMS bridges. The illustrations show a cross-sectional view of a DMTL.	29
3.3	General model for a periodically loaded transmission line with series impedance Z_s and shunt admittance Y_p	30
3.4	Lumped element transmission-line model of the DMTL assuming the MEMS bridge can be represented by a capacitor C_b . L_t and C_t are the per unit length inductance and capacitance, respectively, of the unloaded transmission line, and s is the spacing between the MEMS bridges.	32

3.5	Circuit model used for a section in the DMTL simulation where Z_o is the unloaded line impedance, s is the periodic spacing of the MEMS bridges, A is the attenuation in dB/cm of the unloaded line, ϵ_{eff} is the effective dielectric constant of the unloaded line, C_b is the MEMS bridge capacitance, and L_b is the bridge inductance.	37
3.6	Measured loss of a 96 Ω CPW line (with a 5000 Å thick center conductor) and a 61 Ω distributed MEMS transmission line. The loss is backed out of TRL calibration data. The estimated loss is computed from the CPW line loss by multiplying it by a factor of $96/60 = 1.6$	38
3.7	Measured effective dielectric constant of a 96 Ω CPW line and a 61 Ω DMTL.	38
3.8	Measured and simulated S-parameters of a DMTL with 16 30- μ m wide MEMS bridges spaced at 306 μ m (total length = 5.2 mm, $Z = 61 \Omega$, $f_B = 129$ GHz).	40
3.9	Measured S11 from 0-60 GHz for a DMTL with 16 30- μ m wide bridges spaced at 306 μ m.	41
3.10	Measured S11 from 0-60 GHz for a DMTL with 16 30- μ m wide bridges spaced at 306 μ m with the 138 μ m long high-impedance lines de-embedded.	41
3.11	Measured and simulated S-parameters of a DMTL with 16 60- μ m wide MEMS bridges spaced at 640 μ m (total length = 10.8 mm, $Z = 62 \Omega$, $f_B = 62$ GHz).	43
3.12	Measured S11 from 0-60 GHz for a DMTL with 16 60- μ m wide bridges spaced at 640 μ m.	44
3.13	Measured S11 from 0-60 GHz for a DMTL with 16 60 μ m wide bridges spaced at 640 μ m with the 290 μ m high impedance lines de-embedded.	44
3.14	Comparison between the circuit model and analytical model for the DMTL with parameters listed in Table 3.4.	46
3.15	Comparison between the circuit model and analytical model for the DMTL with parameters listed in Table 3.5.	48
4.1	Measured (a) phase shift and (b) S-parameters for a DMTL with 32 30- μ m-wide bridges spaced at 306 μ m (total length = 10.1 mm) for varying bias voltage. The phase shift at 22 V is modeled with the circuit parameters given in Table 4.1.	52
4.2	Capacitance ratio versus maximum reflection coefficient for unloaded-line impedances of 80, 100, and 120 Ω	54
4.3	Calculated phase shift per centimeter vs. the CPW center conductor width at 40 GHz for (a) silicon, (b) quartz, and (c) air with a capacitance ratio of $C_r = 1.2$. The total CPW width is $\lambda_d/8$ and $\lambda_d/5$, at 60 GHz; for each substrate, and the Bragg frequency is set to 120 GHz. The impedance for the corresponding center conductor width is given at the top of each plot.	57
4.4	Measured and calculated loss vs. frequency for a 300 μ m total width unloaded CPW line on quartz with a 100 μ m wide center conductor ($Z_o = 100 \Omega$).	58
4.5	Calculated loss for the unloaded and loaded transmission lines at 40 GHz vs. CPW center conductor width for (a) silicon, (b) quartz, and (c) air substrates. The total CPW width is $\lambda_d/8$ and $\lambda_d/5$, at 60 GHz, for each substrate, and the Bragg frequency is set to 120 GHz.	59

4.6	Loaded transmission line loss and loss due to bridge resistance vs. frequency. The line loss is calculated from Hoffmann's equation for a 300 μm total width CPW line with a 100 μm width center conductor. The Bragg frequency is 120 GHz, the bridge spacing is 197 μm and the bridge capacitance is 34.6 fF.	61
4.7	Calculated phase shift per dB loss at 40 GHz vs. CPW center conductor width for (a) silicon, (b) quartz, and (c) air substrates with a capacitance ratio of $C_r = 1.2$. The total CPW width is $\lambda_d/8$ and $\lambda_d/5$ for each substrate and the Bragg frequency is set to 120 GHz.	62
4.8	Calculated phase shift per dB loss at 40 GHz versus center conductor width for a 300 μm total width CPW line on quartz. The capacitance ratio is varied from 1.2 to 1.5 with a loaded impedance of 48 Ω and a Bragg frequency of 120 GHz.	63
4.9	Unloaded (—) and loaded (---) line loss at 40 GHz. The calculated loaded line loss has been increased by a factor of 1.4 and 1.8, however, it is seen that the factor of 1.8 fits the measured loss best. The impedances for the labeled widths are included for reference.	65
4.10	Calculated phase shift per dB loss at 40 GHz with capacitance ratios of 1.17, 1.3, and 1.5. Measured data points (x) are included for CPW center conductor widths of 50, 100, and 150 μm .	65
4.11	Measured and modeled S-parameters of the $W = 100 \mu\text{m}$ DMTL with 38 bridges (total length = 7.6 mm) at (a) 0 V and (b) a maximum applied bias of 13 V.	67
4.12	Measured and modeled phase shift of the $W = 100 \mu\text{m}$ DMTL at 13 V.	68
4.13	Measured and modeled phase shift per dB loss for the $W = 100 \mu\text{m}$ DMTL showing 90°/dB at 60 GHz or 4 dB loss for 360° phase shift.	68
4.14	Loaded transmission line loss and loss due to bridge resistance vs. frequency. The line loss is calculated from Hoffmann's equation for a 300 μm total width CPW line with a 100 μm width center conductor. The Bragg frequency is 180 GHz, the bridge spacing is 110 μm and the bridge capacitance is 20.7 fF.	70
4.15	Phase shift per dB loss calculated from a Libra circuit simulation of a 32 bridge DMTL on quartz with a capacitance ratio of 1.17 and different bridge resistances specified at 30 GHz and varying as \sqrt{f} .	70
4.16	Calculated phase shift per dB loss versus center conductor width at 100 GHz for a bridge resistances of (a) 0.15 Ω at 30 GHz and (b) 0 Ω . The total CPW width is $\lambda_d/5$ at 100 GHz for each substrate which is 180 μm , 300 μm , and 600 μm for silicon, quartz, and air, respectively. The loaded impedance is 48 Ω , the capacitance ratio is 1.2, and the Bragg frequency is 240 GHz.	72
4.17	Calculated effective dielectric constant for W-band DMTL's versus center conductor width. The relative dielectric constant of silicon (11.9) and quartz (3.78) are shown for reference.	73
4.18	Calculated loss at 100 GHz versus center conductor width. The CPW line loss (—) includes radiation loss while the DMTL line neglects radiation but includes loss due to a 0.15 Ω bridge resistance at 30 GHz (0.27 Ω at 100 GHz).	73

4.19	Measured (2-40 GHz and 75-110 GHz) and modeled S-parameters at (a) 0 V bias and (b) a maximum bias of 26 V for a W-band DMTL phase shifter. The dimensions are listed in Table 4.7 and the circuit parameters are listed in Table 4.8.	75
4.20	Measured and modeled phase shift per dB loss at a maximum bias of 26 V for a W-band DMTL phase shifter. The dimensions are listed in Table 4.7 and the circuit parameters are listed in Table 4.8.	76
4.21	Calculated phase shift per dB loss at 100 GHz with a capacitance ratio of 1.15, 1.3, and 1.5. The measured data point is shown for a center conductor width of 100 μm	76
4.22	Measured loss of a 96 Ω CPW ($W = 100 \mu\text{m}$) and DMTL line. The estimated loss, calculated from (3.20) uses the measured CPW loss to calculate R_s . A bridge resistance of 0.15 Ω at 30 GHz is also included in the estimate. . . .	77
4.23	Optimized DMTL design with integrated capacitors for stabilization of MEMS bridges.	79
4.24	Reduced DC circuit of Figure 4.23 with integrated capacitors, C_s , at both ends of the DMTL.	79
4.25	Optimized 16 bridge DMTL with 1.9 pF integrated series capacitors for stabilization with (a) 0 V and (b) 40 V applied bias.	80
5.1	Measured results of distributed MEMS switches with 8 and 16 30- μm wide bridges spaced at 306 μm in the (a) open position (bridge up) and (b) closed position. The S-parameters for the open position are only shown for the case of the 8 bridge design.	82
5.2	Measured and modeled results for a distributed MEMS switch with 16 60- μm wide bridges spaced at 400 μm in the (a) open position (bridge up) and (b) closed position.	84
5.3	SEM image of the remains of a DMTL after the breakdown voltage of the Si_xN_y was exceeded.	85
5.4	Variation of lower cutoff frequency with different number of sections used in the distributed switch design.	86
5.5	Driver circuit used to provide a 0 to 33 V step to the bias line of the DMTL.	87
5.6	Experimental setup of the switching speed measurement.	88
5.7	Switching speed measurement of a 16 bridge DMTL with a bridge width and spacing of 25 μm and 110 μm , respectively. The bridge height is approximately 0.9 μm and the pull-down voltage is 6 V.	89
5.8	Switching speed measurements of a 16 bridge DMTL with a bridge width and spacing of 25 μm and 110 μm , respectively. The bridge height is 1.5 μm and the pull-down voltage is 21 V.	90
5.9	Numerical solution of the switching speed for step voltages of (a) 33 V, (b) 28 V, and (c) 23 V for a gold bridge with parameters given in Table 5.1. . .	92
5.10	Measured S-parameters of the 96 bridge DMTL at a maximum bias voltage of 6 V. The DMTL is based on the optimized design of Section 4.2.2, although the bridge height is approximately 0.9 μm , rather than 1.2 μm , due to excessive residual stress within the bridges.	96
5.11	Measured phase shift of the 96 bridge DMTL based on the optimized design of Section 4.2.2.	96

5.12	Experimental setup for the heterodyne measurement of the DMTL as a BPSK modulator.	97
5.13	Measured output of the DMTL as a BPSK modulator with a modulation rate of 1 kHz. The RF is at 35 GHz and is mixed down to 10 kHz as shown here. Phase changes can be observed at 0.32 μ s and 0.87 μ s.	98
5.14	Measured RF spectrum of the DMTL as a BPSK modulator with a modulation rate of 1 kHz. The carrier, with no modulation, was measured to be -14.7 dBm.	99
5.15	Numerical simulation of bridge movement under 6 V 1 kHz square wave modulation.	100
5.16	Numerical simulation of bridge movement under 6 V 10 kHz square wave modulation.	100
5.17	Numerical simulation of bridge movement under 60 V 50 kHz square wave modulation for a bridge with dimensions listed in Table 5.17.	101
5.18	DMTL lines measured as phase verniers at 40 GHz. All three lines have 30 μ m wide bridges spaced at 306 μ m with the number of bridges shown in the plot. The insertion loss is 0.51/0.75/1.57 dB for the 8/16/32 bridge DMTLs.	103
B.1	(a) Monopulse radar receiver with (b) a standard monopulse processor using 0°/90° 3 dB couplers.	113
B.2	Example of a planar RF monopulse processor using using 0°/90° 3 dB couplers with 90° delay lines. The output labeled T is terminated in a matched load.	114
B.3	0 dB coupler used in the Monopulse processor; (a) block diagram and (b) simulation using Lange couplers.	114
B.4	Monopulse processor using Lange couplers; (a) layout and (b) simulation.	115
B.5	Simulated group delay from the input ports to (a) $\Delta 1$ and (b) $\Delta 3$	116
B.6	(a) Picture of assembled Lange coupler based monopulse processor and (b) measured response.	117
C.1	Architecture of (a) Current Polarimetric Systems and (b) Proposed IF-Based Polarimetric System.	118
C.2	Schematic of the Passive IF Polarimetric Receiver.	119
C.3	Response of Polarimetric Receiver for (a) Horizontally Polarized Wave and (b) Left-hand Circularly Polarized Wave.	120
C.4	Measured Phase Error for X-band Receiver.	122

LIST OF APPENDICES

APPENDIX

A	Forces on a Capacitor	110
B	An Octave Bandwidth Monopulse Processor	112
C	IF-Based Polarimetric Receivers	118
D	Detailed Fabrication Process	123

CHAPTER 1

Introduction

The field of microelectromechanical systems (MEMS) as applied to microwave and millimeter wave circuits has been expanding rapidly during the 1990's. At first this was driven, to a large extent, by the success of low-frequency MEMS devices and their advantage of low-power operation and integrability with CMOS circuitry. However, the bulk of these low frequency devices are based on polysilicon structures. Unfortunately, polysilicon is a poor microwave material due to its relatively high resistivity which, at microwave frequencies, causes excessive loss. Because of this, most researchers in the field of microwave MEMS devices have used metal structures driven by electrostatic actuation.

Most of the research in microwave MEMS devices, to date, has focused on the development of low-loss low-power control circuits such as single-pole single-throw (SPST) switches and switched-line phase shifters [30, 18, 60]. The advantage of using MEMS devices over FETs or PIN diodes is their extremely low series resistance, on the order of 0.1 to 0.3 Ω as compared to 2 to 6 Ω , and their extremely low drive power requirements, on the order of μW as compared with mW. In addition to this, due to the fact that MEMS devices do not contain a semiconductor junction, with the associated non-linearity, they lack any measurable intermodulation distortion [19].

MEMS switches have been fabricated in fixed-fixed beam, cantilever, and diaphragm configurations with the bridge height typically 3 to 4 μm above the transmission line, resulting in an actuation voltage of 25 to 100 V. Pacheco *et al.* have shown that low voltage actuation of 14 to 16 V can be achieved with a gap height of 3 μm by using serpentine

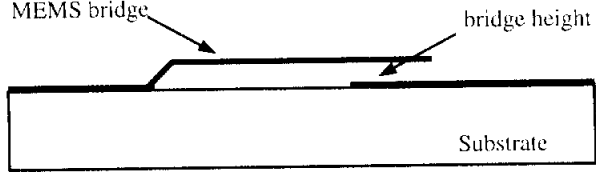


Figure 1.1: Cantilever MEMS bridge in a series configuration along a microstrip or CPW transmission line.

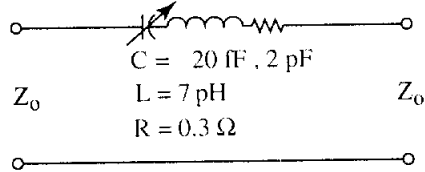


Figure 1.2: Circuit model for a series capacitive MEMS switch with the capacitance switching from 20 fF to 2 pF.

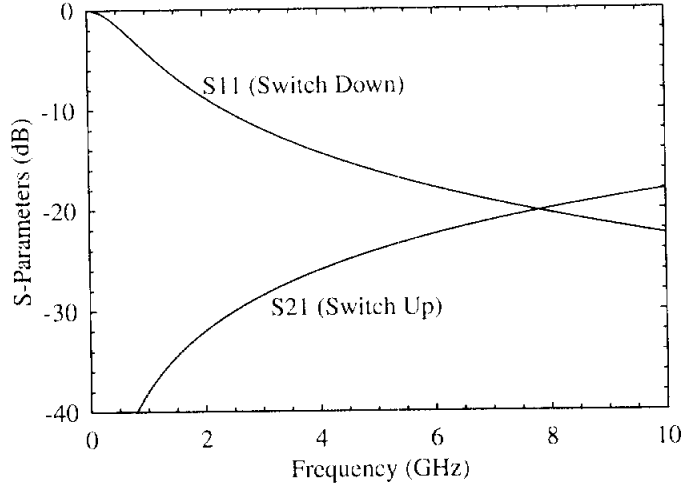


Figure 1.3: Circuit simulation of series switch using the model in Figure 1.2.

cantilever springs at the ends of the beam [38]. The 3 to 4 μm height is necessary in order to reduce the parasitic capacitance of the bridge in the OFF-state (bridge up), and results in a capacitance ratio of 50 to 100 for capacitive switches. MEMS switches have been demonstrated reliably up to 40 GHz with low insertion loss (0.2 to 0.5 dB) and high linearity [30, 19]. The achievable isolation with these switches is typically 20 to 40 dB, depending on the size of the MEMS bridge, with an associated reflection coefficient from -15 to -20 dB.

Current microwave MEMS switches have been designed in both series and shunt configurations with both cantilever and fixed-fixed beams. In the series configuration, shown

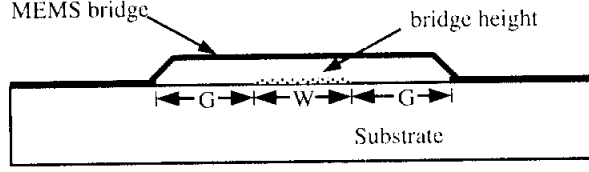


Figure 1.4: Fixed-fixed beam MEMS bridge in shunt configuration over a CPW transmission line.

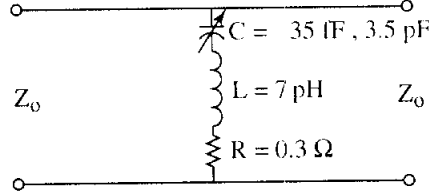


Figure 1.5: Circuit model for a shunt capacitive MEMS switch with the capacitance switching from 35 fF to 3.5 pF.

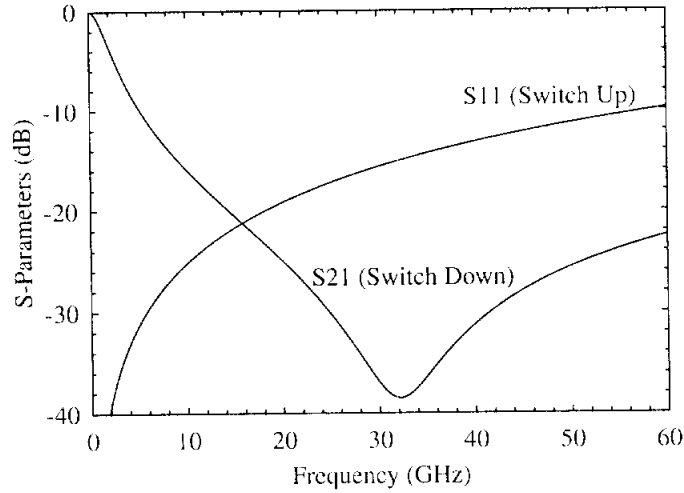


Figure 1.6: Circuit simulation of a shunt switch using the model in Figure 1.5.

in Figure 1.1 with a cantilever beam, the isolation is limited by the parasitic capacitance which allows coupling at high frequencies. This can be seen with a simulation in which the MEMS bridge is represented by a series capacitor-inductor-resistor combination as shown in Figure 1.2. Figure 1.3 shows the circuit simulation for the isolation when the switch is up and the return loss when the switch is down. As can be seen, for the capacitance values used, the performance at low frequencies is limited by the return loss rising to -10 dB around 2 GHz and at high frequencies by the isolation rising above -20 dB around 8 GHz. One of the main problems of series capacitive switches is the high return loss, with the

switch down, in the frequency range where the isolation is greatest, with the switch up. In Figure 1.3, this occurs at 0.1-2 GHz. It is for this reason that metal-to-metal series MEMS switches are used. Yao *et al.* presented a series metal-to-metal MEMS switch for use in systems up to 6 GHz with better than 50 dB isolation up to 4 GHz [60].

The shunt switch configuration is shown in Figure 1.4 with a fixed-fixed beam over a CPW line. In this case, the parasitic capacitance limits the high frequency response when the switch is up by producing unwanted reflections. Again, the MEMS bridge can be modeled by a series capacitor-inductor-resistor combination as shown in Figure 1.5. The circuit simulation of this model is shown in Figure 1.6 where the return loss, when the switch is up, and the isolation, when the switch is down, is shown. As can be seen, the low frequency limit is set by low isolation while the high frequency limit is set by high return loss. Because of the high frequency of operation of the shunt configuration, the inductance in the MEMS bridge resonates with the capacitance as seen in the isolation curve in Figure 1.6. Goldsmith *et al.* [19], have developed a shunt capacitive MEMS switch with 40 dB isolation, with the switch down, and -15 dB return loss, with the switch up, at 40 GHz. Muldavin *et al.* have demonstrated that by using several shunt capacitive MEMS switches, the reflections can be tuned out and higher isolation can be achieved as compared to a single switch. The measured results demonstrate a return loss below -15 dB from DC-40 GHz with an isolation of better than 40 dB from 16-40 GHz [33].

MEMS switch designs have been very similar to standard PIN diode or FET switch networks, with the active device replaced by the MEMS switch. This thesis presents a departure from the traditional approach by incorporating the MEMS switches in distributed transmission line designs. In this approach, a CPW transmission line is loaded periodically with MEMS bridges, as shown in Figure 1.7, which act as shunt capacitors/varactors. The impedance and propagation velocity of the resulting slow-wave transmission line are determined by the size of the MEMS bridges and their periodic spacing. The shunt capacitance associated with the MEMS bridges is in parallel with the distributed capacitance of the transmission line and is included as a design parameter of the loaded line. Thus, the height of the MEMS bridge can be lowered from 3-4 μm to 1-1.5 μm . An immediate advantage of the lowered height is that the pull-down voltage of the MEMS bridge is reduced to 10-

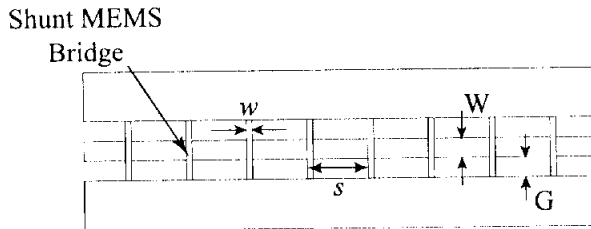


Figure 1.7: Top view of a CPW line periodically loaded by shunt MEMS bridges.

20 V. By using a single analog control voltage to vary the height of the MEMS bridges, the distributed capacitive loading on the transmission line, and therefore its propagation characteristics, can be varied. This results in analog control of the transmission line phase velocity and therefore in a true-time delay phase shifter. Furthermore, if the MEMS bridges are pulled down (to form a very large capacitor), the distributed transmission line results in a wideband switch.

The concept of periodically loaded lines has been researched for use as nonlinear transmission lines since about 1960 [29]. In this case, a CPW transmission line is loaded with millimeter-wave Schottky diodes and is used in voltage-level pulse shaping, picosecond-level sampling, and harmonic multipliers [44, 45]. More recently, the periodically loaded line concept has been used in developing microwave phase shifters using varactor diodes as the capacitive loading [35, 36]. However, diode-based periodically loaded lines are quite lossy at millimeter wave frequencies, due to the series resistance of the Schottky diodes, and cannot be used in low-loss phase shifters and wideband switches above 26 GHz. For these frequencies, MEMS bridges offer excellent performance with very low additional transmission-line losses.

This thesis consists of 5 chapters. Chapter 2 starts off with a basic description of the mechanical properties of fixed-fixed beams as they are used in the distributed MEMS transmission lines (DMTLs). The cantilever bridge is not used in this work, and therefore is not discussed. Chapter 3 covers the theory of periodically loaded lines with extensions for the case of using MEMS bridges as the varactors. Both analytic and circuit models are found which provide for both the design and accurate simulation of the distributed lines. Chapter 4 discusses the application of the distributed MEMS transmission line as a

phase shifter. The design and optimization of the DMTL phase shifter for both 60 GHz and 100 GHz designs is presented. In Chapter 5, additional applications of the DMTL as a switch, phase modulator, and phase vernier are presented. In addition, topics such as the switching speed of the bridges and the power handling of the DMTL is discussed. Chapter 6 concludes the thesis with a discussion of the future directions of research for microwave MEMS devices and the distributed MEMS transmission line. Several appendices are included for completeness. The first appendix covers the derivation of the electrostatic force on a capacitor. The next two appendices cover work related to a monopulse radar receiver where the indirect motivation for investigating MEMS based millimeter wave phase shifters came from. The last appendix is the detailed process used for the fabrication of the distributed MEMS transmission lines.

CHAPTER 2

Mechanical Properties of Fixed-Fixed Beams

The fixed-fixed beam bridge is used quite often in RF MEMS applications. For this reason, it is important to develop a model for understanding the mechanical operation of the bridge. In this chapter, a first-order model will be developed for the operation of a fixed-fixed beam under electrostatic actuation as well as the effect of Brownian noise.

2.1 Spring Constant

If the operation of the fixed-fixed beam is limited to small deflections, the mechanical behavior can be modeled using a linear spring constant, k (N/m). This spring constant is composed of two parts. One part, k' , is due to the stiffness of the bridge which accounts for the material characteristics such as Young's modulus, E (Pa), and the moment of inertia, I (m^4). The other part of the spring constant, k'' , is due to the biaxial residual stress, σ (Pa), within the beam which is typically a result of the fabrication process used to define

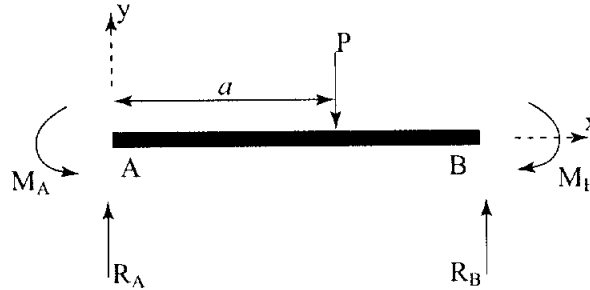


Figure 2.1: Fixed-fixed beam with concentrated vertical load P .

the beam.

The expression for the spring constant of a fixed-fixed beam with a concentrated vertical load, P (N) in Figure 2.1, is found from the deflection versus load position given by [43]:

$$\begin{aligned} EI \frac{d^2 y}{dx^2} &= M_A + R_A x & \text{for } x \leq a \\ y &= \frac{M_A x^2}{2EI} + \frac{R_A x^3}{6EI} & \text{for } x \leq a \\ M_A &= -\frac{Pa}{l^2} (l-a)^2 \\ R_A &= \frac{P}{l^3} (l-a)^2 (l+2a) \end{aligned} \quad (2.1)$$

where l is the length of the beam, M_A (N·m) is the reaction moment at the left end, and R_A (N) is the vertical reaction at the left end. The moment of inertia, I , for a rectangular cross-section is given by $wt^3/12$ where w is the width of the beam and t is the thickness of the beam.

In MEMS applications, the load is typically distributed across the beam and the deflection of the beam at the center is used to determine the spring constant. By substituting $x = l/2$ into (2.1), the deflection at the center is found for a concentrated load at point a . To find the deflection for a distributed load, the principle of superposition is used. For instance, in the case where the load is distributed across the entire beam, the deflection is found by evaluating the integral:

$$y = \frac{2}{EI} \int_{l/2}^l \frac{\xi}{48} (l^3 - 6l^2 a + 9la^2 - 4a^3) da \quad (2.2)$$

where ξ is the load per unit length so that the total load is $P = \xi l$, and the expressions for M_A and R_A have been substituted into (2.1). Since the structure is symmetric, the integral is evaluated from $l/2$ to l and multiplied by 2. When this integral is evaluated the spring constant is found to be:

$$k' = -\frac{P}{y} = -\frac{\xi l}{y} = \frac{32Ewt^3}{l^3} \quad (2.3)$$

For the case of a fixed-fixed beam over a CPW line, the force is approximated as being evenly distributed above the CPW center conductor as shown in Figure 2.2. For this case, the integral in (2.2) would have to be reevaluated with new limits. In this work, the center

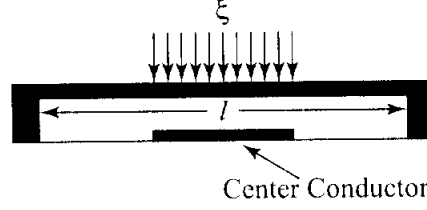


Figure 2.2: Fixed-fixed beam over a CPW line with the force, $P = \xi l/3$, evenly distributed above the CPW center conductor.

conductor is typically a third of the length of the bridge (or beam) which gives a spring constant of:

$$k' = \frac{32Ewt^3}{l^3} \left(\frac{27}{49} \right) \quad (2.4)$$

This spring constant is smaller since the same total load is concentrated more towards the center of the beam where it is less stiff than at the ends.

The part of the spring constant due to the biaxial residual stress within the beam is derived from modeling the beam as a stretched wire as shown in Figure 2.3. It should be noted that this model only applies for tensile stress. The biaxial residual stress, σ , results in a force, S , [15]:

$$S = \sigma(1 - \nu)tw \quad (2.5)$$

pulling on both ends of the beam, where ν is Poisson's ratio. When a vertical force (P) is applied, the beam is deflected by an amount u at the location of the applied force. This deflection stretches the beam which increases the stress in the beam and thus the force pulling on the ends increases to [57]:

$$S + \frac{AE\Delta_1}{a} \quad \text{and} \quad S + \frac{AE\Delta_2}{(l-a)} \quad (2.6)$$

where Δ_1 and Δ_2 are the lengths by which the beam is stretched on either side of the vertical load, P , and are given by:

$$\begin{aligned} \Delta_1 &= \sqrt{a^2 + u^2} - a \\ \Delta_2 &= \sqrt{(l-a)^2 + u^2} - (l-a) \end{aligned} \quad (2.7)$$

By equating the applied force, P , with the forces in the beam, projected onto the vertical direction, and assuming a small deflection, the following equation can be found for u :

$$u = \frac{Pa(l-a)}{Sl} \quad (2.8)$$

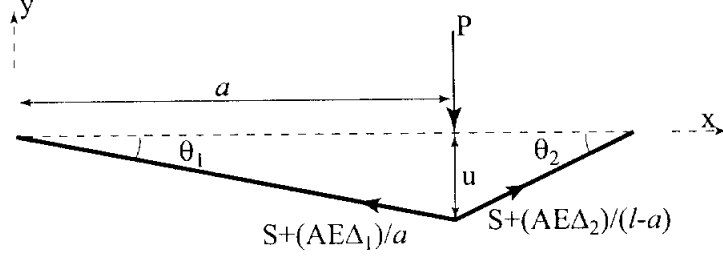


Figure 2.3: Beam modeled as a stretched wire with concentrated vertical load P.

in which the additional force due to Δ_1 and Δ_2 has been neglected. From this equation, the deflection at the center of the beam ($x = l/2$) is found to be:

$$y = -\frac{P}{2S}(l - a) \quad (2.9)$$

The deflection for a load distributed across the entire beam ($P = \xi l$) can now be found by evaluating the integral:

$$y = -2 \int_{l/2}^l \frac{\xi}{2S}(l - a)da \quad (2.10)$$

where symmetry has been used in setting up the integral. The spring constant is found to be:

$$k'' = -\frac{\xi l}{y} = \frac{8S}{l} = \frac{8\sigma(1 - \nu)wt}{l} \quad (2.11)$$

Once again for the case of a fixed-fixed beam over a CPW line, the distributed force is only located over the center conductor. The spring constant for a center conductor width equal to a third of the length of the bridge is:

$$k'' = \frac{8\sigma(1 - \nu)wt}{l} \left(\frac{3}{5}\right) \quad (2.12)$$

Again, the spring constant is smaller due to the load being more concentrated at the center where the beam is more easily moved.

The total spring constant is the sum of the contributions from the beam stiffness and the biaxial residual stress, and for a load distributed across the entire beam is:

$$k = k' + k'' = \frac{32Ewt^3}{l^3} + \frac{8\sigma(1 - \nu)wt}{l} \quad (2.13)$$

which is the same model reported in [37]. For a beam over a CPW line with the center conductor a third of the length of the beam, the spring constant is given by:

$$k = \frac{32Ewt^3}{l^3} \left(\frac{27}{49} \right) + \frac{8\sigma(1-\nu)wt}{l} \left(\frac{3}{5} \right) \quad (2.14)$$

A more general expression for the spring constant of a bridge over a CPW line is given by:

$$k = \frac{32Ewt^3}{l^3} \left(\frac{1}{2 - (2-x)x^2} \right) + \frac{8\sigma(1-\nu)wt}{l} \left(\frac{1}{2-x} \right) \quad (2.15)$$

where $x = W/l$ and W is the width of the CPW center conductor. Thus the spring constant for a concentrated load at the center of the beam is found when $x = 0$, and for a centered load distributed over a third of the beam when $x = 1/3$ which results in (2.14).

Figures 2.4 and 2.5 demonstrate the variation in the spring constant using (2.14), for gold and aluminum bridges respectively, as the thickness, t , is varied for lengths of 200 and 400 μm and residual stresses of 0, 50, and 100 MPa.

For the case where the residual stress within the beam is compressive, the model for k'' is no longer valid. The primary concern with compressive stress is the tendency for the beam to buckle. Due to the stiffness of the beam, a certain amount of compressive stress can be withstood before buckling occurs. This stress, known as the critical stress, is given for a fixed-fixed beam by [15]:

$$\sigma_{cr} = \frac{\pi^2 Et^2}{3l^2(1-\nu)} \quad (2.16)$$

The variation in the critical stress with thickness for 200 and 400 μm long bridges made of gold and aluminum is shown in Figures 2.6(a) and 2.6(b), respectively. It is seen that for a bridge thickness of 1 to 2 μm and a length of 400 μm , a compressive stress of 4 to 12 MPa for gold and 2 to 8 MPa for aluminum can be tolerated. For a shorter length of 200 μm and a thickness of 2 μm , a gold bridge can withstand 45 MPa while an aluminum bridge can withstand 34 MPa. However, the shorter length bridge results in a much higher pull-down voltage as discussed in section 2.2.

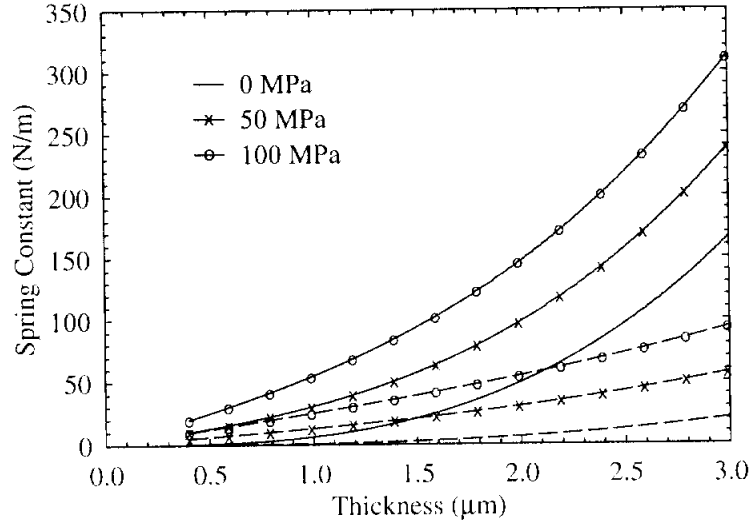


Figure 2.4: Spring constant of a gold bridge ($E = 80$ GPa, $\nu = 0.42$) with lengths of $200\ \mu\text{m}$ (—) and $400\ \mu\text{m}$ (---). For each bridge length the spring constant is evaluated for biaxial residual stresses of 0, 50, and 100 MPa. The spring constant scales linearly with the bridge width which is held constant at $35\ \mu\text{m}$.

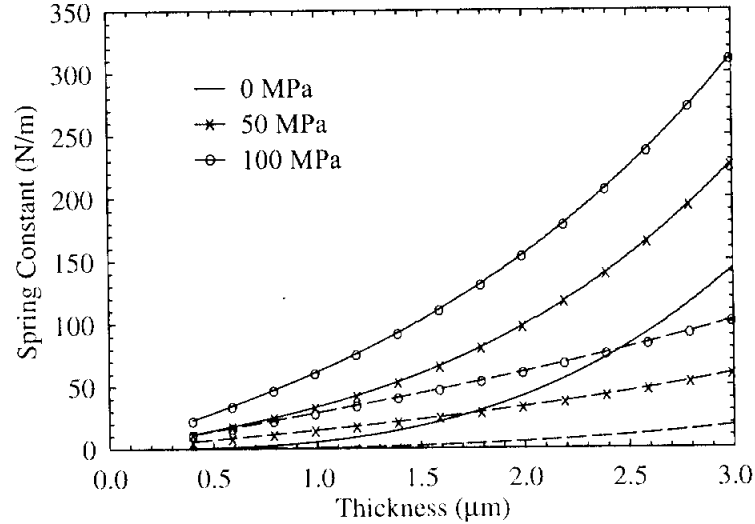
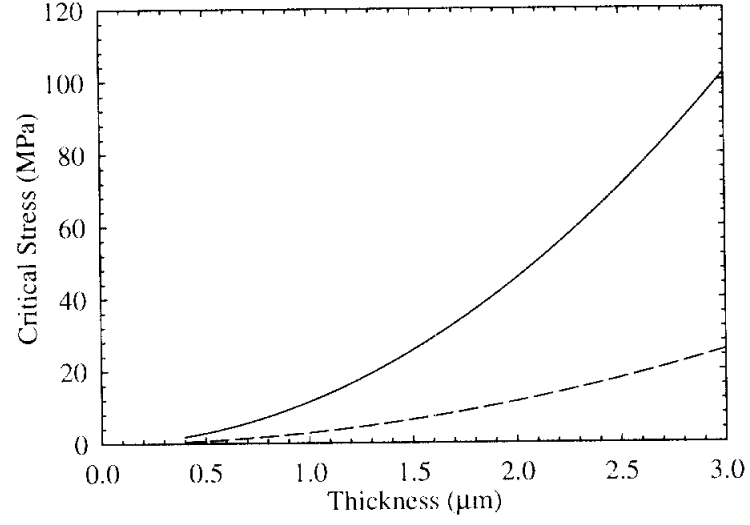
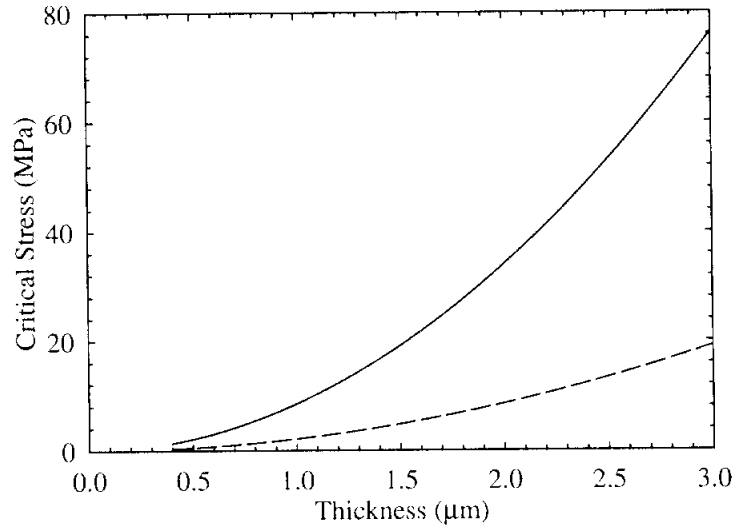


Figure 2.5: Spring constant of an aluminum bridge ($E = 69$ GPa, $\nu = 0.33$) with lengths of $200\ \mu\text{m}$ (—) and $400\ \mu\text{m}$ (---). For each bridge length the spring constant is evaluated for biaxial residual stresses of 0, 50, and 100 MPa. The spring constant scales linearly with the bridge width which is held constant at $35\ \mu\text{m}$.



(a)



(b)

Figure 2.6: Critical stress of a (a) gold ($E = 80$ GPa, $\nu = 0.42$) and (b) aluminum ($E = 69$ GPa, $\nu = 0.33$) bridge vs. thickness for $200 \mu\text{m}$ (—) and $400 \mu\text{m}$ (---) long bridges.

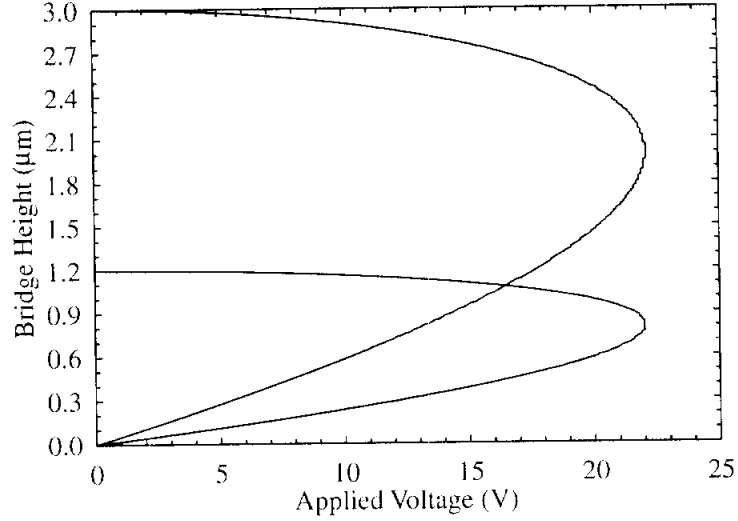


Figure 2.7: Bridge height versus applied voltage with a zero-bias bridge height of $1.2 \mu\text{m}$ and $3 \mu\text{m}$. The bridge parameters, given in Table 2.1, are chosen to result in a pull-down voltage of 22 V.

2.2 Electrostatic Actuation

When a voltage is applied between the bridge and center conductor of a CPW line, an electrostatic force is induced on the bridge. This is the well known electrostatic force which exists on the plates of a capacitor under an applied voltage [28]. In order to approximate this force, the bridge over the center conductor is modeled as a parallel plate capacitor. Although the actual capacitance is about 20-30% larger due to fringing fields, the model will provide an understanding of how electrostatic actuation works.

If the width of the bridge is w and the width of the CPW center conductor is W , then the parallel plate capacitance is:

$$C = \frac{\epsilon_o W w}{g} \quad (2.17)$$

where g is the height of the bridge above the center conductor. The force applied to the bridge is found by considering the power delivered to a time-dependent capacitance and is given by [61]:

$$F = \frac{1}{2} V^2 \frac{dC(g)}{dg} = -\frac{1}{2} \frac{\epsilon_o W w V^2}{g^2} \quad (2.18)$$

where V is the voltage applied between the bridge and center conductor.

This electrostatic force is distributed across the section of bridge above the center con-

Table 2.1: Dimensions of bridges used
in Figure 2.7.

$g_o(\mu\text{m})$	1.2	3.0
$l(\mu\text{m})$	300	600
$w(\mu\text{m})$	35	70
$t(\mu\text{m})$	2.5	2.5
$\sigma(\text{MPa})$	1.0	0.50

The bridges are both made of gold with $E = 80 \text{ MPa}$, $\nu = 0.42$, and $\rho = 19320 \text{ kg/m}^3$.

ductor and therefore we can use the spring constant given by (2.14) to determine the distance which the bridge moves with the applied force given by (2.18). Equating the applied electrostatic force with the mechanical restoring force, due to the stiffness of the bridge, it is found that:

$$\frac{1}{2} \frac{\epsilon_o W w V^2}{g^2} = k(g_o - g) \quad (2.19)$$

where g_o is the zero-bias bridge height. Solving this equation for the voltage results in:

$$V = \sqrt{\frac{2k}{\epsilon_o W w} g^2 (g_o - g)} \quad (2.20)$$

The graph of bridge height versus applied voltage, shown in Figure 2.7, shows two possible bridge heights for every applied voltage. This is a result of the bridge becoming unstable at $\frac{2}{3}g_o$. This instability is due to positive feedback in the electrostatic actuation which can be understood by considering the electrostatic force in terms of the electric field applied to the charge on the bridge [14, 61]:

$$F = \frac{QE}{2} \quad (2.21)$$

where Q is the charge on the bridge and $E = V/g$ is the electric field due to the applied voltage. When the constant voltage source (infinite charge pump) is increased, the force is increased due to an increase in the charge. Simultaneously the increased force decreases the bridge height which increases the capacitance, and thus the charge, as well as the electric field. At $\frac{2}{3}g_o$, the increase in the electrostatic force is much greater than the increase in the restoring force resulting in the bridge becoming unstable.

The electrostatic force necessary to pull the bridge down is given by $F = kg_o/3$. For the examples given in Figure 2.7, with dimensions given in Table 2.1, the spring constants

are 29 N/m and 7.5 N/m for the 1.2 μm and 3 μm high bridge, respectively. Thus, the electrostatic force necessary to pull these bridges down is 12 μN for the 1.2 μm high bridge and 7.5 μN for the 3 μm high bridge. This can be compared with the acceleration needed to pull the bridges down completely given by:

$$a = \frac{kg_o}{m} \quad (2.22)$$

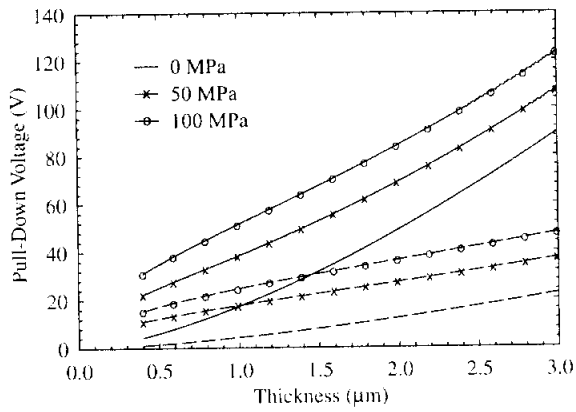
where the spring constant should be calculated using (2.13) since the force due to acceleration is evenly distributed across the bridge. For the examples given in Figure 2.7, with a mass of 0.51 μg and 2.0 μg , the accelerations are $13000\times$ and $2100\times$ the Earth's gravitational acceleration, respectively.

By taking the derivative of (2.20) with respect to the bridge height and setting that to zero, the height at which the instability occurs is found to be exactly two-thirds the zero-bias bridge height. Substituting this value back into (2.20), the “pull-down” voltage is found to be:

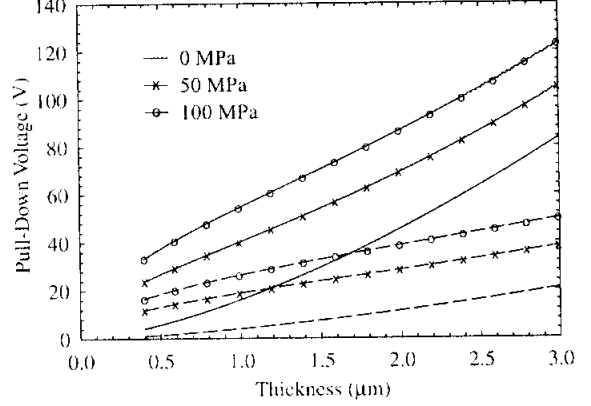
$$V_p = V(2g_o/3) = \sqrt{\frac{8k}{27\epsilon_o W w} g_o^3} \quad (2.23)$$

Figure 2.8 shows the variation in pull-down voltage with bridge thickness for gold and aluminum bridges with lengths of 200 μm and 400 μm and residual stresses of 0, 50, and 100 MPa, calculated using (2.23) and (2.14). It can be seen that the variation of the pull-down voltage with thickness is much greater for a shorter bridge. Figure 2.9 shows the variation in pull-down voltage with bridge height from which it can be seen that the variation is higher for higher residual stress. It should be noted that although (2.23) shows a dependence on the bridge width, w , the pull-down voltage is independent of the bridge width since the spring constant, k , varies linearly with w (see (2.14)).

By using (2.20) and varying g from g_o to $\frac{2}{3}g_o$, the bridge height versus applied voltage characteristics can be found. From this calculation, the parallel-plate capacitance versus bridge height is determined and is plotted in Figure 2.10. It is seen that as the applied voltage approaches the pull-down voltage (22 V), the bridge capacitance changes very rapidly and reaches a value of $1.5C_{bo} = 30$ fF at 22 V, where $C_{bo} = 20$ fF is the zero-bias bridge capacitance. This can be seen very clearly in Figure 2.11 which shows the derivative of the capacitance and bridge height with respect to the applied voltage. Due to the bridges

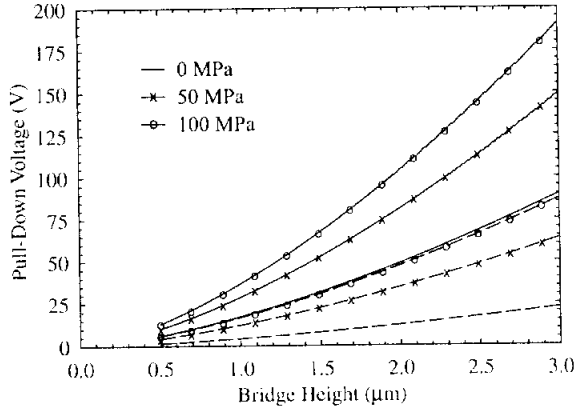


(a)

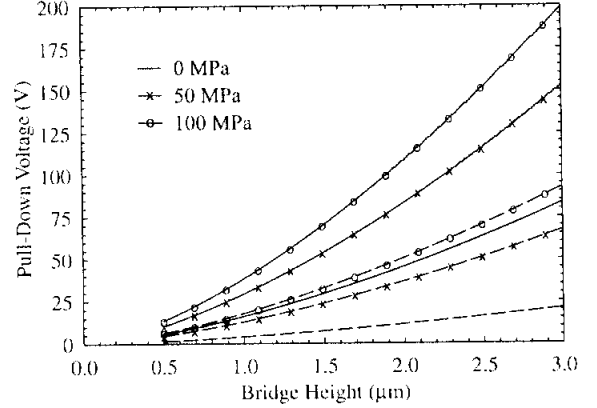


(b)

Figure 2.8: Pull-down voltage of a (a) gold ($E = 80$ GPa, $\nu = 0.42$) and (b) aluminum ($E = 69$ GPa, $\nu = 0.33$) bridge vs. bridge thickness for 200 μm (—) and 400 μm (---) long bridges. For each bridge length the pull-down voltage is calculated for biaxial residual stresses of 0, 50, and 100 MPa. The pull-down voltage depends on the bridge height as $g_o^{3/2}$ and g_o is 1.5 μm .



(a)



(b)

Figure 2.9: Pull-down voltage of a (a) gold ($E = 80$ GPa, $\nu = 0.42$) and (b) aluminum ($E = 69$ GPa, $\nu = 0.33$) bridge vs. bridge height for 200 μm (—) and 400 μm (---) long bridges. For each bridge length the pull-down voltage is calculated for biaxial residual stresses of 0, 50, and 100 MPa. The pull-down voltage depends on the bridge height as $g_o^{3/2}$ and g_o is 1.5 μm .

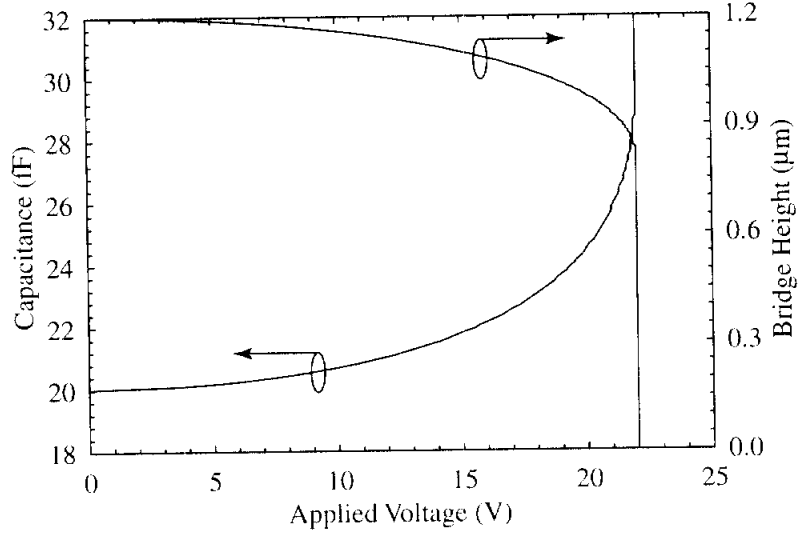


Figure 2.10: Variation of bridge capacitance and gap height with applied voltage. The bridge parameters have been adjusted to result in a pull-down voltage of 22 V, a zero-bias bridge capacitance of 20 fF, and a zero-bias height of 1.2 μm .

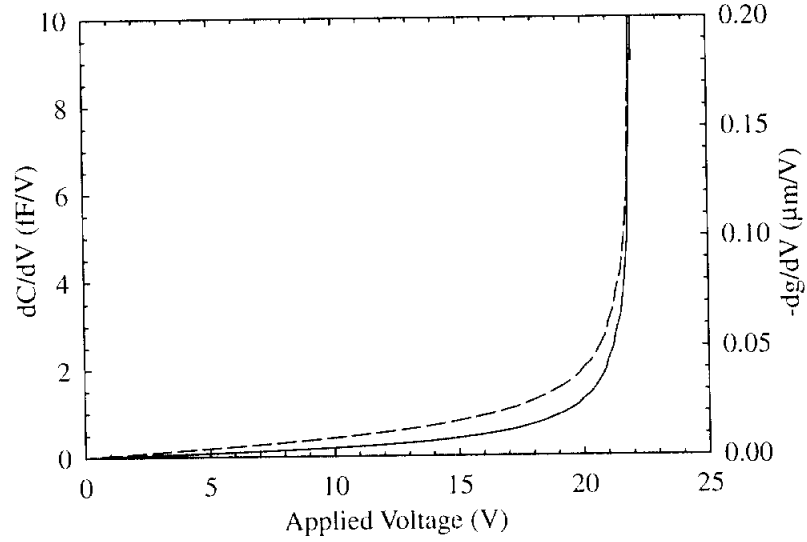


Figure 2.11: Derivative of the bridge capacitance (—) and bridge height (---), with respect to the applied voltage, vs. the applied voltage. The bridge parameters have been adjusted to result in a pull-down voltage of 22 V.

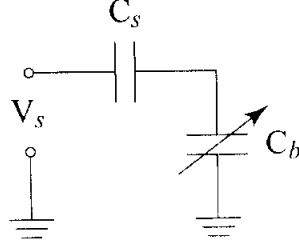


Figure 2.12: Stabilization of an electrostatically actuated MEMS bridge through the use of a series feedback capacitor.

instability at $2g_o/3$, it is not possible in practice to achieve this 50% increase in the bridge capacitance. Instead, the applied voltage must be limited to 20-21 V which gives a capacitance of $C_b = 25$ -26 fF, or a 25-30% increase in the zero-bias bridge capacitance.

2.3 Stabilization of Electrostatically Actuated Bridges

It has been demonstrated that by placing a series capacitance in the DC path of the MEMS bridge capacitor, as shown in Figure 2.12, the instability in the electrostatic actuation can be reduced and even eliminated [48]. This can be understood from a feedback point of view. The applied voltage, V_s , is divided between the two capacitors such that the voltage across the MEMS capacitor is:

$$V = \frac{V_s}{1 + C_b/C_s} \quad (2.24)$$

where $C_b = \epsilon_o A/g$ is the MEMS capacitor and C_s is the fixed series capacitor. As V_s is increased, the voltage applied to the MEMS capacitor increases, causing the bridge to pull down and C_b to increase. This results in the positive feedback, discussed in section 2.2, and the resulting instability at $\frac{2}{3}g_o$. However, in the series (stabilization) configuration shown in Figure 2.12, the increase in C_b results in less voltage across C_b (and more across C_s), thereby achieving negative feedback.

The position at which the instability now occurs is determined by first finding the force on the MEMS capacitor in terms of V_s , solving for V_s , and taking the derivative of V_s with respect to the bridge height. The force on the bridge is found by considering the change in energy of both capacitors with respect to the bridge height, g :

$$F = \frac{dU}{dg} = \frac{V_s^2}{2} \frac{d}{dg} \left(\frac{C_b C_s}{C_b + C_s} \right) = -\frac{\epsilon_o A V_s^2}{2(g + Kg_o)^2} \quad (2.25)$$

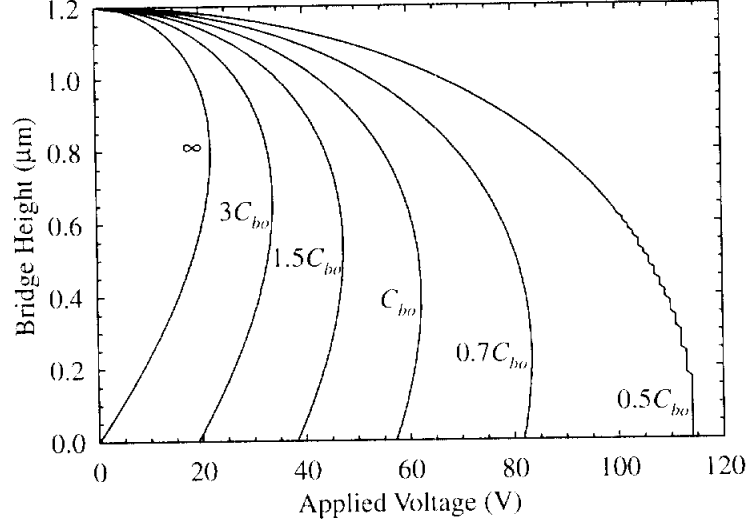


Figure 2.13: Plot of change in bridge height versus applied voltage as the series feedback capacitor is varied from $0.5C_{bo}$ to ∞ . The zero-bias bridge height is $1.2 \mu\text{m}$.

where $K = C_{bo}/C_s$, and $C_{bo} = \epsilon_o A/g_o$ is the zero-bias bridge capacitance. By equating this force with the force due to the stiffness of the bridge, $F = k(g_o - g)$, the applied voltage can be solved in terms of the bridge height, g :

$$V_s = \sqrt{\frac{2kg_o^3}{\epsilon_o A} \left(\frac{g}{g_o} + K \right)^2 \left(1 - \frac{g}{g_o} \right)} \quad (2.26)$$

By taking the derivative of (2.26) with respect to g and setting it to zero, the position of the instability is found to be:

$$g_p = \frac{g_o}{3}(2 - K) \quad (2.27)$$

From this equation, it is seen that for $K = 0$ (ie. no series feedback capacitor), the instability occurs at the expected height of $2g_o/3$. However, if $K = 2$ or $C_s = C_{bo}/2$, then the instability point is eliminated altogether ($g_p = 0$).

This increase in the stable region of an electrostatically actuated bridge does not come without a price. The voltage required to pull the bridge completely down is also increased. The new pull-down voltage can be found by substituting (2.27) back into (2.26) resulting in:

$$V_{sp} = \sqrt{\frac{8kg_o^3}{27\epsilon_o A} (1 + K)^3} \quad (2.28)$$

which is seen to be the standard pull-down voltage, given by (2.23), increased by a factor of $(1 + K)^{3/2}$. Thus, if the instability is completely removed by setting $K = 2$, then the

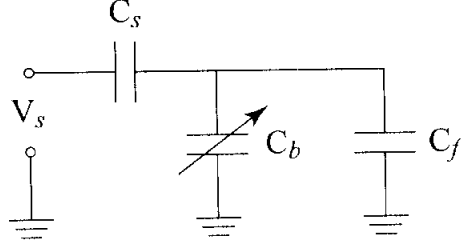


Figure 2.14: Stabilization of an electrostatically actuated MEMS bridge, in the presence of significant fringing capacitance, through the use of a series feedback capacitor.

pull-down voltage is increased by a factor of 5.2. For the example used in section 2.2, this would increase the pull-down voltage from 22 V to 114 V. Figure 2.13 shows the change in bridge height versus applied voltage as the series capacitance is varied from $0.5C_{bo}$ to ∞ (ie. a short circuit). As can be seen, if twice the initial pull-down voltage is acceptable, then a series capacitance of $C_s = 1.7C_{bo}$ ($K = 0.6$) can be used, resulting in stable operation up to $0.5g_o$.

While in some cases it may be possible to isolate a single capacitor without a large fringing field component, in most cases, and particularly with the distributed MEMS transmission lines, fringing fields can be very large. If a capacitor is placed in parallel with the variable MEMS capacitor as shown in Figure 2.14, it is found that the effect of the series feedback capacitor is reduced, and the instability point must be solved again.

The force on the capacitor is again determined from the change in energy with respect to g :

$$F = \frac{dU}{dg} = \frac{V_s^2}{2} \frac{d}{dg} \left(\frac{C_s C_b + C_s C_f}{C_s + C_f + C_b} \right) = - \frac{\epsilon_o A V_s^2}{2 (g (1 + C_f/C_s) + K g_o)^2} \quad (2.29)$$

where C_f is the fixed capacitance to ground in parallel with the MEMS capacitor. Setting this force equal to the restoring force of the bridge, the applied voltage is found to be:

$$V_{sf} = \sqrt{\frac{2kg_o^3}{\epsilon_o A} \left(\frac{g}{g_o} \left(1 + \frac{C_f}{C_s} \right) + K \right)^2 \left(1 - \frac{g}{g_o} \right)} \quad (2.30)$$

It should be noted that this equation reduces to (2.20) when $C_s = \infty$, and to (2.26) when $C_f = 0$ as expected. By taking the derivative of (2.30) with respect to g and setting it to

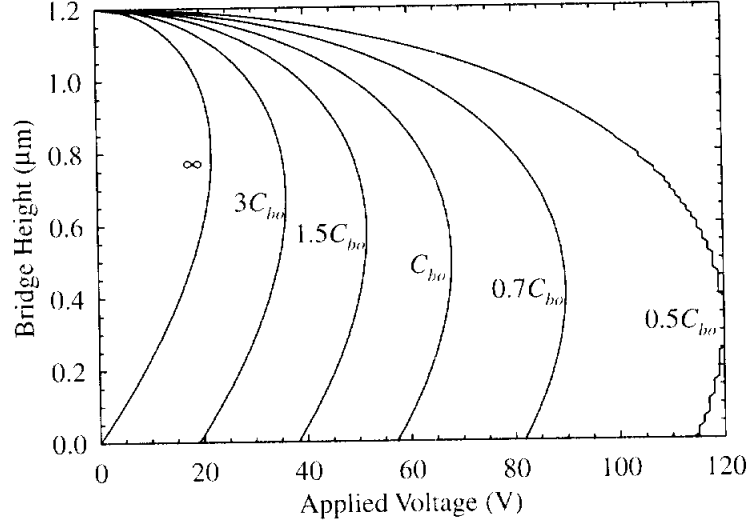


Figure 2.15: Plot of the change in bridge height versus applied voltage as the series feedback capacitor is varied from $0.5C_{bo}$ to ∞ with a fringing capacitance of $C_f = C_{bo}/3$. The zero-bias bridge height is $1.2 \mu\text{m}$.

zero, the modified instability position is:

$$g_{pf} = \frac{g_o}{3} \left(2 - \frac{K}{1 + C_f/C_s} \right) \quad (2.31)$$

Setting $g_{pf} = 0$, it is found that the series capacitance would have to be:

$$C_s = \frac{C_{bo}}{2} - C_f \quad (2.32)$$

From this equation it is seen that if the fringing capacitance is larger than half the zero-bias bridge capacitance, it is no longer possible to completely eliminate the instability. The pull-down voltage is also affected by the fringing capacitance and is found to be:

$$V_{sfp} = \sqrt{\frac{8kg_o^3}{27\epsilon_o A} \frac{(C_s + C_f + C_{bo})^3}{C_s^2 (C_s + C_f)}} \quad (2.33)$$

Figure 2.15 shows the change in the bridge height versus applied voltage with a fixed parallel capacitance $C_{bo}/3$. The series capacitance is again varied from $0.5C_{bo}$ to ∞ , however, it can be seen that even at $0.5C_{bo}$, the instability is still present at $0.32 \mu\text{m}$ while the pull-down voltage has been increased to 120 V (from an initial value of 22 V). Since the parallel capacitance is less than $0.5C_{bo}$, it is possible to completely eliminate the instability by setting the series capacitance to $C_{bo}/6$. However, according to (2.33), this would increase the pull-down voltage by a factor of 27 or to 594 V making the device unusable.

2.4 Frequency Response

The frequency response of a fixed-fixed beam is useful for determining the mechanical bandwidth over which the beam can be used as well as the effect which thermal noise will have. The frequency response can be determined by starting with the equation for the dynamic response which according to d'Alembert's principle is given by [57]:

$$m \frac{d^2 x}{dt^2} + b \frac{dx}{dt} + kx = f_{ext} \quad (2.34)$$

where x is the bridge height, m is the bridge mass, b is the damping coefficient, and f_{ext} is an external force. By using Laplace transforms, the frequency response is found to be:

$$\frac{X(j\omega)}{F(j\omega)} = \frac{k^{-1}}{1 - (\omega/\omega_o)^2 + j\omega/(Q\omega_o)} \quad (2.35)$$

where $\omega_o = \sqrt{k/m}$ is the resonant frequency and $Q = k/(\omega_o b)$ is the quality factor of the resonant beam. For the resonant frequency when the bridge is over a CPW line with a center conductor that is a third of the length of the bridge, the spring constant given in (2.14) can be used. The resulting expression for the case of no residual stress, $\sigma = 0$, is given by:

$$f_o = 0.668 \frac{t}{l^2} \sqrt{\frac{E}{\rho}} \quad (2.36)$$

where ρ^1 is the density of the bridge material. As can be seen, the resonant frequency can be increased by either increasing the thickness or decreasing the length of the beam. However, it must be remembered that these changes will also affect the actuation voltage needed to pull the beam down. If tensile stress is present in the beam, the complete expression for the spring constant, given in (2.14), would have to be used when calculating the resonant frequency.

The quality factor of the beams is determined by several different variables such as the pressure, temperature, and intrinsic material dissipation. Since the beams used in this work are operated at atmospheric pressure, the quality factor is dominated by squeeze-film damping [1]. Under this condition, an approximation for the quality factor of the fixed-fixed beam is given by [23]:

$$Q^{-1} = \frac{\mu (wl/2)^2}{\sqrt{E\rho} t^2 g^3} \quad (2.37)$$

¹The density of gold and aluminum is 19320 kg/m³ and 2700 kg/m³, respectively [58].

where μ^2 is the viscosity of air. It is seen that the quality factor is strongly dependent upon the bridge height, g^3 variation, and the thickness, t^2 variation. Figures 2.16(a) and (b) show the variation in the frequency response for gold and aluminum bridges, respectively. The calculation is carried out using (2.14) for the spring constant with 50 MPa residual stress and for bridge lengths of 200 and 400 μm . For each bridge length, bridge heights of 1, 2, and 3 μm are used. The variation in the quality factor is seen by the amplitude change at the resonant frequency and the values are given in Table 2.2. In addition, it is seen that although the resonant frequency for aluminum is higher than for gold, due to the significant difference in their respective densities, gold has a higher quality factor.

Table 2.2: Quality factors for bridges in Figure 2.16.

	Gold		Aluminum	
$g_o(\mu\text{m})$	200 μm	400 μm	200 μm	400 μm
1	0.40	0.10	0.14	0.035
2	3.2	0.81	1.1	0.28
3	11	2.7	3.8	0.95
$f_o(\text{kHz})$	85	36	230	100

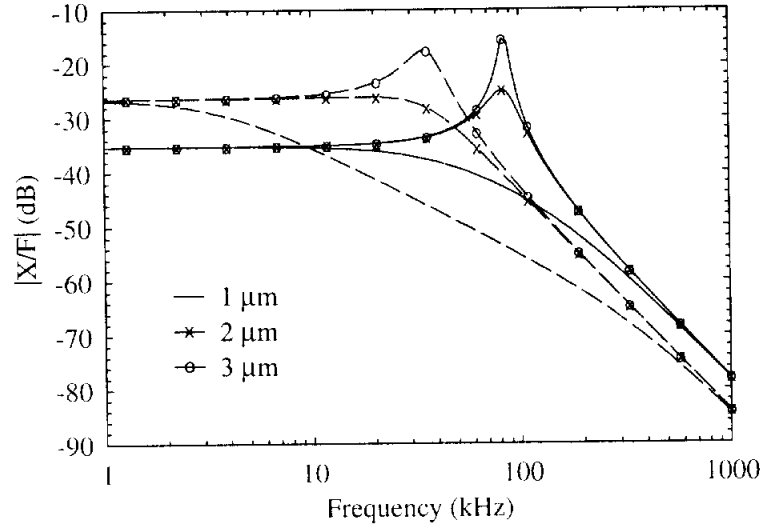
2.5 Brownian Noise Analysis

Any time a dissipation mechanism, such as the $b\dot{x}$ term, is present in a system, there is a corresponding noise source [26]. In the case of the mass-spring system, this noise source is Brownian noise which can be included by setting f_{ext} in (2.34) to represent a noise force ($f_{ext} = f_n$).

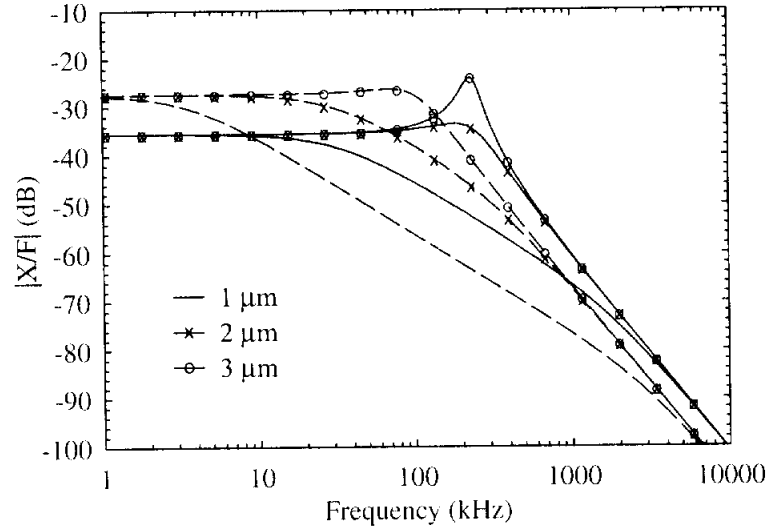
It is possible to derive an expression for the Brownian noise force by using the principle of equipartition of energy [26]. According to this principle, every mode in a system which is in thermal equilibrium and contributes a quadratic term to the energy such as kinetic, spring potential, or rotational kinetic will have an average energy equal to $\frac{1}{2}k_B T$, where k_B is Boltzmann's constant ($1.38 \cdot 10^{-23}$ J/K). Thus, for the fixed-fixed beam the following equation must be satisfied in thermal equilibrium:

$$\frac{1}{2}k\overline{x^2} = \frac{1}{2}k_B T \quad (2.38)$$

²The viscosity of air is $1.79 \cdot 10^{-5}$ Pa·s at atmospheric pressure and 288 K [58].



(a)



(b)

Figure 2.16: Frequency response of a (a) gold ($E = 80$ GPa, $\nu = 0.42$, $\rho = 19320$ kg/m³) and (b) aluminum ($E = 69$ GPa, $\nu = 0.33$, $\rho = 2700$ kg/m³) bridge for 200 μ m (—) and 400 μ m (---) long bridges over a CPW line with $W = l/3$. For each bridge length the response is calculated for bridge heights of 1, 2, and 3 μ m. The width is 35 μ m, the thickness is 1.5 μ m, and the residual stress is 50 MPa.

In order to find an expression for f_n , the mean-square of the position must be found using the transfer function given by (2.35) and integrating over all frequencies:

$$\begin{aligned}\overline{x^2} &= \frac{\overline{f_n^2}}{k^2} \int_0^\infty \frac{1}{\left[1 - (\omega/\omega_o)^2\right]^2 + \omega^2/(Q\omega_o)^2} df \\ &= \frac{\overline{f_n^2}}{f_n^2} \frac{\omega_o Q}{4k^2}\end{aligned}\quad (2.39)$$

in which it has been assumed that the noise force is frequency independent over the bandwidth of the vibrational mode of the beam. Upon substituting (2.39) into (2.38), the noise force is found to be:

$$\overline{f_n} = \sqrt{4bk_B T} \quad (\text{N}/\sqrt{\text{Hz}}) \quad (2.40)$$

which is immediately recognized as being analogous to the equivalent noise voltage of a resistor with the resistance, R , equal to the damping coefficient, b .

Referring the Brownian noise force to the beam position using (2.35), the equivalent mean square position is found to be:

$$\overline{x_n^2} = \frac{4bk_b T}{k^2} \frac{1}{\left[1 - (\omega/\omega_o)^2\right]^2 + \omega^2/(Q\omega_o)^2} \quad (\text{m}^2/\text{Hz}) \quad (2.41)$$

From which it can be seen that bridges with large spring constants and low damping coefficients will result in a low Brownian noise position. For the devices shown in Figure 2.16 the low-frequency rms Brownian noise positions are given in Table 2.3 from which it is seen that there is very little difference between the gold and aluminum bridges. The low equivalent noise position is primarily due to the stiffness of the bridges and thus the Brownian noise, for the applications used in this work, is insignificant.

Table 2.3: Low-frequency rms Brownian-noise position values for the bridges used in Figure 2.16 in $\text{\AA}/\sqrt{\text{Hz}}$.

	Gold		Aluminum	
$g_o(\mu\text{m})$	200 μm	400 μm	200 μm	400 μm
1	$2.4 \cdot 10^{-4}$	$1.2 \cdot 10^{-3}$	$2.4 \cdot 10^{-4}$	$1.2 \cdot 10^{-3}$
2	$8.5 \cdot 10^{-5}$	$4.4 \cdot 10^{-4}$	$8.5 \cdot 10^{-5}$	$4.2 \cdot 10^{-4}$
3	$4.6 \cdot 10^{-5}$	$2.4 \cdot 10^{-4}$	$4.6 \cdot 10^{-5}$	$2.3 \cdot 10^{-4}$

CHAPTER 3

Distributed MEMS Transmission Lines

Distributed circuits have been used in many devices including filters [41], traveling-wave amplifiers [44], phase shifters [36], and non-linear transmission lines [44]. The concept is very useful because the parasitics of the discrete components, such as the gate-to-source capacitance of transistors in traveling-wave amplifiers, or the capacitance of Schottky diodes in non-linear transmission lines, are included as part of the periodic transmission line, thereby resulting in very wideband operation. The transmission-line dimensions can also be designed such that the resulting periodic transmission line will have a $50\ \Omega$ characteristic impedance.

The distributed MEMS transmission line (DMTL) consists of a high impedance line ($> 50\ \Omega$) capacitively loaded by the periodic placement of MEMS bridges. This could be done with many different types of transmission lines, however it is most easily implemented using coplanar waveguide (CPW) transmission lines. Figure 3.1 shows the top view of a typical DMTL used in this work. The MEMS bridges have a width w , a length $l = W + 2G$, and a thickness t . The periodic spacing between the bridges, s , and the number of bridges vary depending upon the application. The DMTL is connected to probe pads via $50\ \Omega$ CPW feedlines for the purpose of testing.

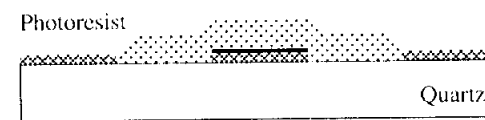
A result of creating a periodic structure is the existence of a cut-off frequency or Bragg frequency, f_B , near the point where the guided wavelength approaches the periodic spacing of the discrete components [47]. In many of the distributed circuits mentioned, this cut-off frequency can be designed such that it will not limit the device performance since the discrete components will have a comparable maximum frequency [44]. In the case of the



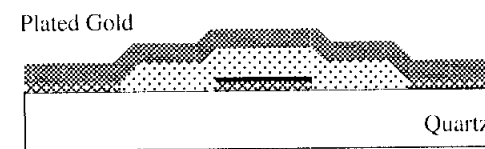
(a)



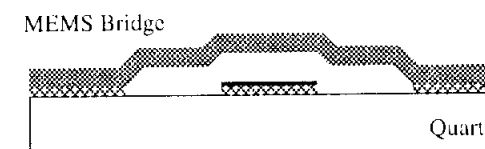
(b)



(c)



(d)



(e)

Figure 3.2: Details of the fabrication process for the MEMS bridges. The illustrations show a cross-sectional view of a DMTL.

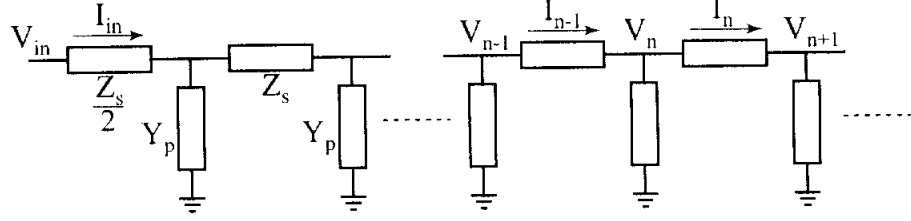


Figure 3.3: General model for a periodically loaded transmission line with series impedance Z_s and shunt admittance Y_p .

wafer in a solvent. At this point, the wafer cannot be air dried because the surface tension of the liquid will pull the MEMS bridges down, causing them to stick to the substrate. Therefore, the wafer is placed in denatured ethanol and a critical-point drying system is used to release the MEMS bridges [see Fig. 3.2(e)][34].

For the purpose of testing, a short section of high impedance line is added at either end of the DMTL. The periodic segments of the DMTL consist of a high impedance line of length s with the MEMS bridge in the center of the section. The extra length of line at either end is $(s - w)/2$ long, for most of the designs, and contains the transition from the $50 \, \Omega$ feedlines to the DMTL as shown in Figure 3.1.

3.2 Analytic Modeling of Distributed Lines

The general model for a periodically loaded transmission line is shown in Figure 3.3 [44]. Assuming a complex propagation constant $\gamma = \alpha + j\beta$, where α is the attenuation *per section* and β is the phase *per section*, a forward traveling wave is represented by:

$$V_{n+1} = V_n e^{-\gamma} \quad (3.1)$$

Using Figure 3.3, the voltages and currents are found to be:

$$V_n = \frac{I_{n-1} - I_n}{Y_p} \quad (3.2)$$

$$I_{n-1} = \frac{V_{n-1} - V_n}{Z_s} \quad \text{and} \quad I_n = \frac{V_n - V_{n+1}}{Z_s}$$

Substituting the current equations for I_{n-1} and I_n into the voltage equation for V_n , the following equation is found [44]:

$$1 + \frac{Z_s Y_p}{2} = \frac{V_{n-1} + V_{n+1}}{2V_n} = \frac{e^{\gamma} + e^{-\gamma}}{2} = \cosh(\gamma) \quad (3.3)$$

which relates the propagation constant, γ , to the series impedance and shunt admittance of the line. Using these equations, the characteristic impedance of the line can be found from $Z = V_{in}/I_{in}$, or moving to the middle of the line:

$$\begin{aligned} Z &= \frac{V_{n+1/2}}{I_n} = \frac{V_{n-1} - 2V_n + V_{n+1}}{V_n - V_{n+1}} \frac{1}{Y_p} - \frac{Z_s}{2} \\ &= \frac{Z_s e^{\gamma/2}}{2 \sinh(\gamma/2)} - \frac{Z_s}{2} \end{aligned} \quad (3.4)$$

where $V_{n+1/2} = V_n - I_n Z_s/2$. It is important to define the characteristic impedance at a point of symmetry in order to find the correct impedance value. Using the half-angle formula for the hyperbolic sine in (3.4), the characteristic impedance of the loaded line is found to be [44]:

$$Z = \sqrt{\frac{Z_s}{Y_p}} \sqrt{1 + \frac{Z_s Y_p}{4}} \quad (3.5)$$

If a section of length s of unloaded transmission line is used with characteristic impedance Z_o and effective dielectric constant ϵ_{eff} then $Z_s = j\omega s L_t$ and $Y_p = j\omega s C_t$, where $C_t = \sqrt{\epsilon_{eff}}/(cZ_o)$ and $L_t = C_t Z_o^2$ are the per unit length capacitance and inductance, respectively, of the unloaded transmission line. Substituting these values into (3.5) will give:

$$Z = \sqrt{\frac{L_t}{C_t}} \sqrt{1 - \frac{\omega^2 s^2 C_t L_t}{4}} = \sqrt{\frac{L_t}{C_t}} \sqrt{1 - \left(\frac{\omega}{\omega_B}\right)^2} \quad (3.6)$$

where $\omega_B = 2/(s\sqrt{L_t C_t})$ is the Bragg frequency, or the frequency at which the characteristic impedance goes to zero, indicating that no power transfer can occur at this frequency. Since this example is for an unloaded line, the length of the section s can be made arbitrarily small, and as $s \rightarrow 0$ it is found that $\omega_B \rightarrow \infty$ and $Z \rightarrow \sqrt{\frac{L_t}{C_t}} = Z_o$ as is expected for an unloaded line.

For the distributed MEMS transmission line, the MEMS bridge can be modeled as a shunt capacitor, resulting in a loaded-line model as shown in Figure 3.4 where C_b is the shunt capacitance due to the MEMS bridge, and s is the periodic spacing of the bridges. Using this model the series impedance is $j\omega s L_t$ and the shunt admittance is $j\omega(sC_t + C_b)$. The characteristic impedance found using (3.5) is given by:

$$Z = \sqrt{\frac{sL_t}{sC_t + C_b}} \sqrt{1 - \frac{\omega^2}{4} sL_t (sC_t + C_b)} = \sqrt{\frac{sL_t}{sC_t + C_b}} \sqrt{1 - \left(\frac{\omega}{\omega_B}\right)^2} \quad (3.7)$$

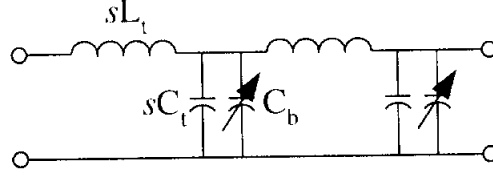


Figure 3.4: Lumped element transmission-line model of the DMTL assuming the MEMS bridge can be represented by a capacitor C_b . L_t and C_t are the per unit length inductance and capacitance, respectively, of the unloaded transmission line, and s is the spacing between the MEMS bridges.

By setting this impedance to zero and solving for ω , the Bragg frequency is found to be:

$$\omega_B = \frac{2}{\sqrt{sL_t(sC_t + C_b)}} \quad (3.8)$$

It can be seen that well below the Bragg frequency, the impedance of the line is given by $\sqrt{L/C}$ where $L = sL_t$ and $C = sC_t + C_b$.

The time delay per section of the loaded-line is determined from (3.3) by assuming a lossless line and using the model in Figure 3.4 [44]:

$$\begin{aligned} v &= \frac{s}{\tau} = \frac{\omega s}{\beta} \\ &= \frac{\omega s}{\cos^{-1}(1 - 2\omega^2/\omega_B^2)} \\ &= \frac{s}{\sqrt{sL_t(sC_t + C_b)} \left(1 + \frac{\omega^2}{6\omega_B^2} + \dots\right)} \end{aligned} \quad (3.9)$$

where τ is the time delay *per section*. At frequencies well below the Bragg frequency, the phase velocity can be approximated as s/\sqrt{LC} . From (3.9) it is seen that by varying the MEMS bridge capacitance, C_b , the phase velocity of the transmission line can be varied resulting in a variable delay line or true-time delay (TTD) phase shifter.

In reality, the MEMS bridge cannot be entirely modeled by a single capacitor due to the presence of some inductance and resistance in the bridge. In the circuit modeling of measured DMTLs (see Section 3.5), it is found that the inductance is large enough to have a very noticeable effect on the device performance while the effect of the resistance is almost negligible.

When an inductance, L_b , is included in series with the bridge capacitance, the shunt

admittance becomes:

$$Y_p = j\omega s C_t + \frac{j\omega C_b}{1 - \omega^2 L_b C_b} \quad (3.10)$$

and the equation for the characteristic impedance becomes:

$$Z = \sqrt{\frac{s L_t}{s C_t + \frac{C_b}{1 - \omega^2 L_b C_b}}} \sqrt{1 - \frac{\omega^2 s^2 L_t C_t}{4} - \frac{\omega^2 s L_t C_b}{4(1 - \omega^2 L_b C_b)}} \quad (3.11)$$

Setting this equation to zero and solving for ω , the resulting Bragg frequency is found to be:

$$\begin{aligned} \omega_B &= \sqrt{\frac{b - \sqrt{b^2 - 4ac}}{2a}} \\ a &= s^2 L_t C_t L_b C_b \\ b &= s^2 L_t C_t + s L_t C_b + 4 L_b C_b \\ c &= 4 \end{aligned} \quad (3.12)$$

For most of the DMTLs designed in this work, the inductance in the bridge has been found to be 10-30 pH. Table 3.1 shows the calculated Bragg frequencies versus several values of bridge inductance for a line with an unloaded impedance of 100 Ω , an unloaded effective dielectric constant of 2.5, a periodic spacing of 200 μm , and a bridge capacitance of 40 fF. As can be seen, including the series inductance of the bridge has a significant effect on the position of the Bragg frequency.

Table 3.1: Bragg Frequency Calculations from (3.8) and (3.12)

L_b (pH)	f_B (GHz)
0	137.9
10	123.3
20	111.9
30	102.9

$Z_o = 100 \Omega$, $\epsilon_{eff} = 2.5$, $s = 200 \mu\text{m}$,
 $C_b = 40 \text{ fF}$.

3.3 Loss on Distributed Lines

Anytime a transmission line is loaded such that the impedance is changed, the loss of the line is also changed due to a change in the amount of current on the line for the same

amount of power. For example, if a high impedance line is capacitively loaded to a lower impedance, the current on the lower impedance line will be higher, thus increasing the I^2R losses. This can be seen directly by considering the complex propagation constant for a lossy transmission line. If the transmission line is represented by series inductance and resistance per unit length, L_t and R_t , and by a shunt capacitance and admittance per unit length, C_t and G_t , respectively, then the propagation constant is given by [10]:

$$\gamma = [(R_t + j\omega L_t)(G_t + j\omega C_t)]^{1/2} \quad (3.13)$$

For a low loss line where $R_t \ll \omega L_t$ and $G_t \ll \omega C_t$, the propagation constant can be approximated as:

$$\gamma \approx j\omega \sqrt{L_t C_t} + \frac{1}{2} \sqrt{L_t C_t} \left(\frac{R_t}{L_t} + \frac{G_t}{C_t} \right) = \alpha + j\beta \quad (3.14)$$

Assuming the characteristic impedance can be approximated by $Z = \sqrt{L_t/C_t}$, the attenuation constant α is:

$$\alpha = \frac{R_t}{2Z} + \frac{G_t Z}{2} \quad (3.15)$$

In a planar transmission line such as microstrip or CPW, R_t represents conductor loss while G_t represents dielectric loss. For the lines considered in this work (on low-loss substrates at mm-wave frequencies), the conductor loss dominates and the attenuation constant can be approximated as $\alpha = R_t/(2Z)$. Thus, a change in the characteristic impedance from a high impedance to a low impedance will increase the loss by a factor of the ratio of the impedances.

The transmission loss can also be included in the model of the distributed MEMS transmission line (Figure 3.4) by including a resistance R_s in series with the line inductance, sL_t . In this case the series impedance becomes $Z_s = j\omega sL_t + R_s$. To find the attenuation constant, (3.3) is expanded to give:

$$\begin{aligned} \cosh \gamma = \cosh \alpha \cos \beta + j \sinh \alpha \sin \beta &= 1 - \frac{\omega^2 LC}{2} + j \frac{\omega R_s C}{2} \\ &= 1 - 2 \left(\frac{\omega}{\omega_B} \right)^2 + j \left(\frac{\omega}{\omega_B} \right) \frac{R_s}{Z} \end{aligned} \quad (3.16)$$

where $L = sL_t$, $C = sC_t + C_b$, and the low frequency approximations have been used for ω_B and Z . By equating the real parts and assuming α is small ($\cosh \alpha \approx 1$), the equation

for the phase delay per section is found to be $\beta = \cos^{-1}(1 - 2\omega^2/\omega_B^2) \approx 2\omega/\omega_B$. To find the attenuation per section, the imaginary parts are equated giving:

$$\sinh \alpha \approx \alpha = \frac{(\omega/\omega_B)R_s/Z}{\sin(2\omega/\omega_B)} \approx \frac{R_s}{2Z} \quad (3.17)$$

where Z is now the impedance of the loaded line. This result matches what was derived earlier in the unloaded case. The only difference is that in the unloaded case, α is the attenuation per unit length (Np/m), while in the distributed case, α is the attenuation per section (Np).

The effect of a series resistance in the bridge can be taken into account by placing a resistor R_b in series with the bridge capacitance in Figure 3.4. In this case, (3.3) becomes:

$$\begin{aligned} \cosh(\alpha + j\beta) &= 1 + \frac{j\omega s L_t}{2} \left(j\omega s C_t + \frac{j\omega C_b + \omega^2 R_b C_b^2}{1 + \omega^2 R_b^2 C_b^2} \right) \\ &\approx 1 - 2 \left(\frac{\omega}{\omega_B} \right)^2 + j \left(\frac{\omega}{\omega_B} \right)^3 \frac{4R_b}{Z} \left(\frac{C_b}{sC_t + C_b} \right)^2 \end{aligned} \quad (3.18)$$

where $\omega_B = 2/\sqrt{sL_t(sC_t + C_b)}$, $Z = \sqrt{sL_t/(sC_t + C_b)}$ and a low frequency approximation has been used for $1 + \omega^2 R_b^2 C_b^2 \approx 1$. Using $\omega < \omega_B$, the propagation constant is found to be:

$$\begin{aligned} \alpha + j\beta &= \cosh^{-1} \left[1 - 2 \left(\frac{\omega}{\omega_B} \right)^2 + j \left(\frac{\omega}{\omega_B} \right)^3 \frac{4R_b}{Z} \left(\frac{C_b}{sC_t + C_b} \right)^2 \right] \\ &\approx j \frac{2\omega}{\omega_B} + \frac{R_b Z C_b^2 \omega^2}{2} \end{aligned} \quad (3.19)$$

Combining this loss with the transmission line loss, the total loss *per section* for a distributed MEMS transmission line is [44]:

$$\alpha = \frac{R_s}{2Z} + \frac{R_b Z C_b^2 \omega^2}{2} \quad (3.20)$$

For a line with an unloaded impedance of 100 Ω , an unloaded effective dielectric constant of 2.5, a periodic spacing of 200 μm , a bridge capacitance of 40 fF, a loss of 0.6 dB/cm at 20 GHz for the unloaded line, and a bridge resistance of 0.1 Ω at 30 GHz the loss from the transmission line is 1.6 and 2.5 dB/cm at 30 and 60 GHz respectively, while the loss from the bridge resistance is 0.05 and 0.28 dB/cm at 30 and 60 GHz. Thus, for these typical parameters, the loss is dominated by the transmission line loss.

Radiation loss is also present in an unloaded CPW line on a thick dielectric substrate because the wave velocity of the transmission line is greater than the phase velocity of the waves in the dielectric [46]. This loss is given by:

$$\begin{aligned}\alpha_{rad} &= \left(\frac{\pi}{2}\right)^5 \frac{1}{\sqrt{2}} \frac{(1 - \epsilon_r)^2}{\sqrt{1 + \epsilon_r}} \frac{f^3 S^2}{c^3 K(k) K(k')} \\ k &= \frac{W}{S} \\ k'^2 &= 1 - k^2\end{aligned}\tag{3.21}$$

where $S = W + 2G$ is the ground-to-ground spacing of the CPW line and $K(k)$ is the complete elliptic integral of the first kind. This radiation into the substrate occurs primarily around the angle:

$$\cos \psi = k_z / k_d\tag{3.22}$$

where k_z is the propagation constant of the line and k_d is the propagation constant in the dielectric. For the DMTLs used in this work, the wave velocity of the transmission line is slower than the phase velocity of the dielectric. Therefore the angle necessary to phase match the wave on the transmission line to the wave in the dielectric, ψ , becomes imaginary indicating that radiation, and therefore radiation loss, cannot occur. This will be discussed further in Section 4.3.

3.4 DMTL Circuit Modeling

Although the analytic model presented in section 3.2 provides a good general understanding of the operation of distributed lines, it is desirable to have a circuit model as well which can be used in a linear circuit simulator. The simulator used for the modeling of the DMTLs is HP EESof's Libra². Using the circuit elements available in Libra, the model shown in Figure 3.5 was developed for a single section of the DMTL. The model consists of a section of physical transmission line to represent the unloaded CPW line and a capacitor-inductor series combination shunted across the transmission line to represent the MEMS bridge. The entire DMTL is modeled in the simulator by cascading the necessary number of sections along with the added lengths of high impedance line at the ends. In

²HP EESof Communications Design Suite v6.0, Hewlett-Packard Company, Santa Clara, CA, 1995.

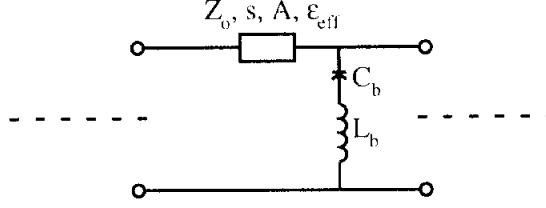


Figure 3.5: Circuit model used for a section in the DMTL simulation where Z_o is the unloaded line impedance, s is the periodic spacing of the MEMS bridges, A is the attenuation in dB/cm of the unloaded line, ϵ_{eff} is the effective dielectric constant of the unloaded line, C_b is the MEMS bridge capacitance, and L_b is the bridge inductance.

this approach, the unloaded line impedance, Z_o , the spacing of the MEMS bridges, s , the number of sections, n , and the effective dielectric constant of the unloaded line, ϵ_{eff} , are determined from the physical dimensions of the DMTL being modeled. The unloaded line attenuation, A , bridge capacitance, C_b , and bridge inductance, L_b , are all varied to fit the model to the measured data. The attenuation in the physical transmission line model is specified at a particular frequency and then follows a \sqrt{f} variation.

3.5 DMTL Measurements

Measurements of the DMTLs were taken using an HP8510C for 2-40 GHz and an HP8510C with a U-band millimeter-wave test set for 40-60 GHz. The measurements were calibrated using NIST's MultiCal³ TRL calibration routine and TRL standards fabricated on-wafer. MultiCal de-embeds the effective dielectric constant and loss from the measured TRL lines. Therefore, a comparison of the DMTLs with the unloaded CPW lines can be made by constructing the necessary TRL standards in both types of lines. The unloaded CPW lines used for this purpose are 96Ω lines ($W = G = 100 \mu\text{m}$) with a 5000 \AA thick center conductor and the DMTLs used these same 96Ω lines with $30 \mu\text{m}$ wide bridges spaced at $306 \mu\text{m}$, resulting in a Bragg frequency of approximately 124 GHz. Figure 3.6 shows the loss and Figure 3.7 shows the effective dielectric constant for both TRL calibrations.

The dashed line in Figure 3.6 is an estimate of the DMTL loss calculated by multiplying

³MultiCal is a registered trademark of NIST, 325 Broadway, Boulder, CO 80303.

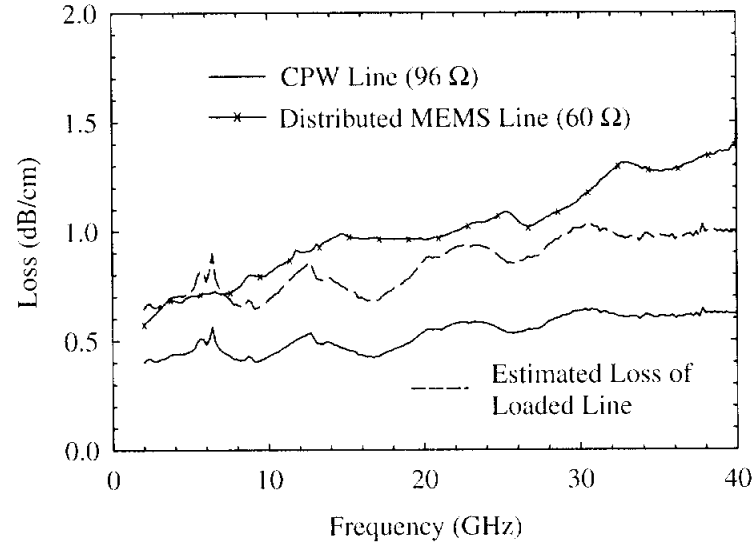


Figure 3.6: Measured loss of a 96 Ω CPW line (with a 5000 Å thick center conductor) and a 61 Ω distributed MEMS transmission line. The loss is backed out of TRL calibration data. The estimated loss is computed from the CPW line loss by multiplying it by a factor of $96/60 = 1.6$.

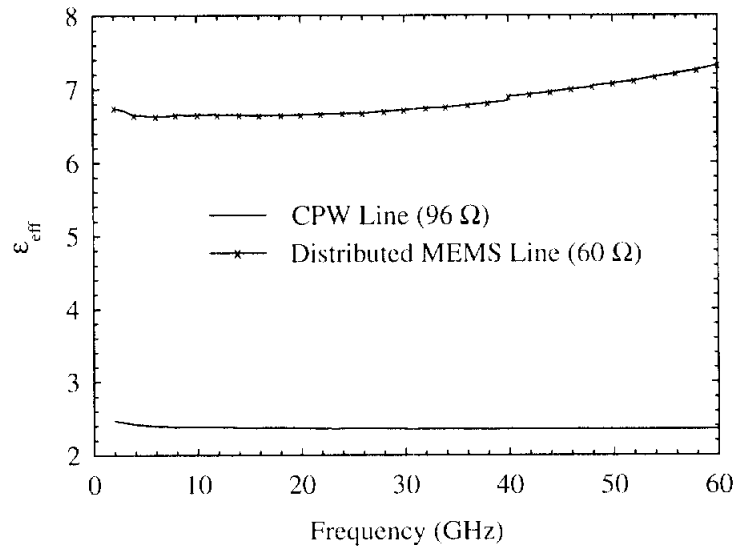


Figure 3.7: Measured effective dielectric constant of a 96 Ω CPW line and a 61 Ω DMTL.

the measured loss of the 96 Ω CPW line by the ratio of the unloaded impedance to the loaded impedance $96/60 = 1.6$. As can be seen, this estimate works fairly well at the lower frequencies, but tends to underestimate the loss at higher frequencies. This is most likely due to the added loss in the bridges and the extension lengths (see Fig. 3.1) which are not accounted for in the estimate.

The measured effective dielectric constant of the unloaded CPW lines has an average value of 2.37 and is nearly invariant with frequency. This value agrees very closely with the static value of 2.34 computed using the static-field solver, Maxwell⁴ 2D. In comparison, the measured effective dielectric constant of the DMTL with the extension sections (see Fig. 3.1) is 6.7 from 18-33 GHz and slowly rises to 7.3 at 60 GHz.

Using a TRL calibration of the CPW feedlines with the reference planes as shown in Figure 3.1, DMTLs with different width bridges and periodic spacing were measured. Figure 3.8 shows the measured S-parameters of a line with 16 30- μm wide MEMS bridges spaced at 306 μm (total length = 5.17 mm) with a nominal MEMS bridge height of 1.5 μm and a bridge thickness of 2.5 μm . The loaded line impedance ($Z = 61 \Omega$) is calculated from the first peak in S11, knowing that the line is behaving as a quarter-wave transformer at this frequency. The loading capacitance, C_b , is therefore calculated to be 24 fF from (3.7), using the static values of $Z_o = 96 \Omega$ and $\epsilon_{eff} = 2.37$ ($W = G = 100 \mu\text{m}$) to obtain L_t and C_t . This capacitance agrees very well with the value of $C_b = 23.8$ fF found by simulating a single MEMS bridge using the static-field solver, Maxwell 3D. The 23.8 fF bridge capacitance can be broken into a parallel-plate capacitance, $C_{||} = \epsilon A/d = 17.7$ fF, and a fringing capacitance, $C_f = 6.1$ fF. Thus, the fringing capacitance is quite high ($\sim 26\%$) and cannot be neglected in the analysis of the DMTLs.

Using the circuit model given in section 3.4 and fitting it to the measured data, the parameters listed in Table 3.2 are found. The simulated S-parameters found using this fitted model are plotted along with the measured data in Figure 3.8 from which it is seen that excellent agreement is obtained from 0 to 60 GHz. Using $C_b = 25$ fF and $L_b = 23$ pH, the calculated effective dielectric constant, from (3.9), is 6.0 which underestimates the TRL de-embedded value of 6.7.

⁴Maxwell is a registered trademark of Ansoft Corp., Pittsburg, PA, 15219

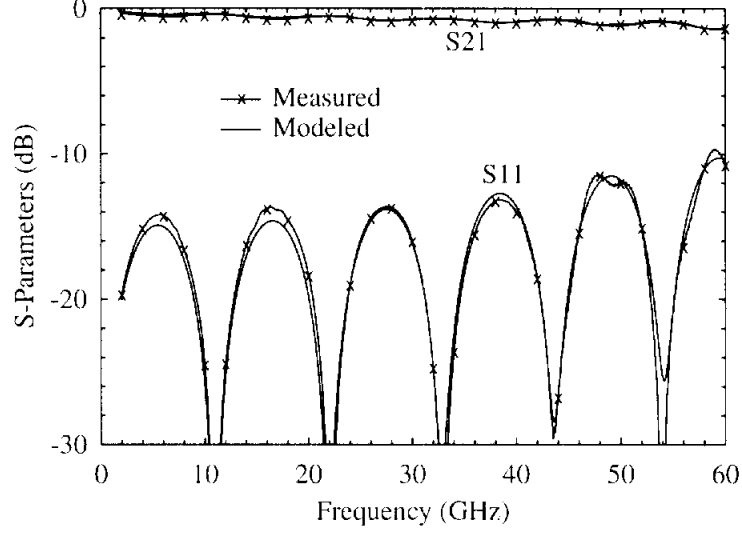


Figure 3.8: Measured and simulated S-parameters of a DMTL with 16 30- μm wide MEMS bridges spaced at 306 μm (total length = 5.2 mm, $Z = 61 \Omega$, $f_B = 129 \text{ GHz}$).

Table 3.2: Fitted Model Parameters for DMTL with $w/s = 30/306 \mu\text{m}$

C_b	25 fF
L_b	23 pH
$A(@ 20 \text{ GHz})$	0.52 dB/cm

Set parameters are: $Z_o=96 \Omega$, $\epsilon_{eff}=2.37$, $n=16$.

The effective dielectric constant can also be calculated using two adjacent nulls in S11 and the total length ($l = 5.17 \text{ mm}$) of the distributed line. A value of 6.8-7.1 is obtained up to 40 GHz which agrees well with the TRL measured value of 6.7. The reason for the discrepancy between the measured value and that calculated from (3.9) is due to the added length of high impedance line at either end of the DMTL, mentioned in section 3.1, which is included in the measured line. The effect of this added length of line can be seen in the reflection coefficient plotted on a Smith chart in Figure 3.9. At low frequencies, the input impedance is seen to circle around 60Ω , as is expected of a 61Ω line bound by two 50Ω ports. However as the frequency increases, the input impedance circles a point in the inductive part of the Smith chart. According to (3.11), the characteristic impedance of a distributed line should remain real as the frequency increases from zero to the Bragg frequency. In order to verify that the characteristic impedance of the DMTL does remain

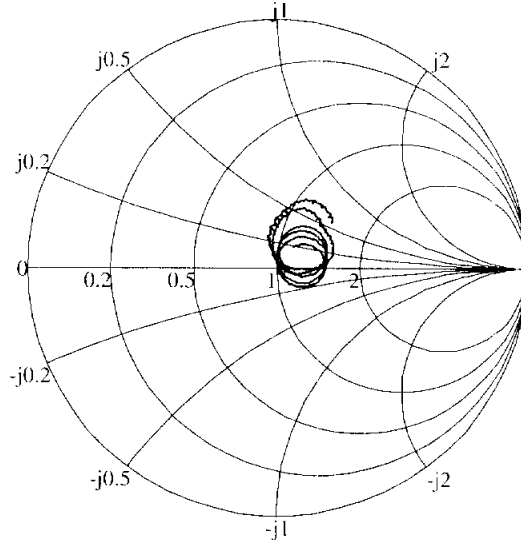


Figure 3.9: Measured S11 from 0-60 GHz for a DMTL with 16 30- μm wide bridges spaced at 306 μm .

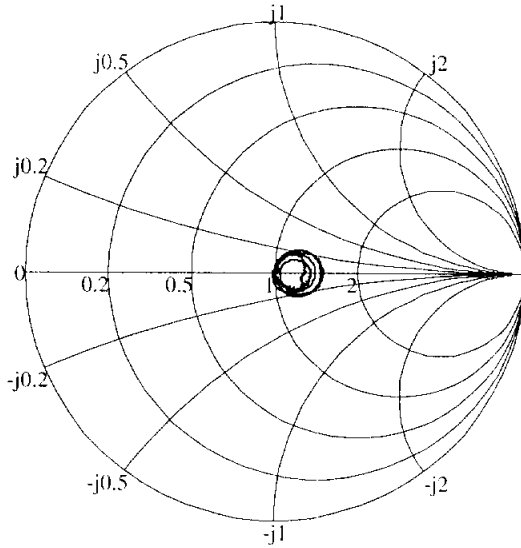


Figure 3.10: Measured S11 from 0-60 GHz for a DMTL with 16 30- μm wide bridges spaced at 306 μm with the 138 μm long high-impedance lines de-embedded.

real with frequency and that the imaginary part of the center of the circles seen in Figure 3.9 is a result of the added lengths of line at the input and output of the DMTL, these lines are de-embedded from the measured data using ABCD matrices. If the measured data, with the added line lengths, is given by $[M]$, then the de-embedded data, $[S]$, is given by:

$$\begin{aligned} [L][S][L] &= [M] \\ [S] &= [L]^{-1}[M][L]^{-1} \end{aligned} \quad (3.23)$$

where $[L]$ is the ABCD matrix for the length of high impedance line. For the 30/306 μm line, the added length is $(s - w)/2 = 138 \mu\text{m}$. Using Libra to generate the S-parameters for the 138 μm length of 96 Ω line with $\epsilon_{eff} = 2.37$, the de-embedded data is plotted in Figure 3.10. It is now seen that the input impedance does circle the real axis from 2-60 GHz, indicating a real characteristic impedance of the DMTL. The characteristic impedance also decreases slightly with frequency, as predicted by (3.7).

This de-embedded data can now be used to find the effective dielectric constant by using a new total line length of $16 \times 306 \mu\text{m} = 4.9 \text{ mm}$. The first three adjacent nulls in S11 give 6.06-6.36 which is in much closer agreement with the calculated value of 6.00 from (3.9). The calculated Bragg frequency of this line, using $C_b = 25 \text{ fF}$ and $L_b = 23 \text{ pH}$, is 114 GHz from (3.12). Using the circuit model with parameters listed in Table 3.2, Libra gives a Bragg frequency of 124 GHz. The added lengths of line at either end of the DMTL have almost no effect on the Bragg frequency.

The measurement shown in Figure 3.11 is of a DMTL with 16 60- μm wide MEMS bridges spaced at 640 μm (total length = 10.8 mm). The loaded line impedance is 62 Ω determined from the first peak in S11 at 2.8 GHz. The calculated MEMS bridge capacitance from (3.7) is $C_b = 48 \text{ fF}$, which agrees fairly well with the value obtained from the static-field solver, Maxwell 3D, of $C_b = 42.5 \text{ fF}$ ($C_{||} = 35.4 \text{ fF}$, $C_f = 7.1 \text{ fF}$). The difference could be due to a slight bowing in the MEMS bridge causing the height to be less than 1.5 μm .

Fitting the circuit model to the measured data, the parameters listed in Table 3.3 are found. The simulated results, shown in Figure 3.11, are seen to be in excellent agreement with the measured data and show that the circuit model is valid even when approaching the Bragg frequency of the line. The calculated effective dielectric constant for $C_b = 48 \text{ fF}$ and

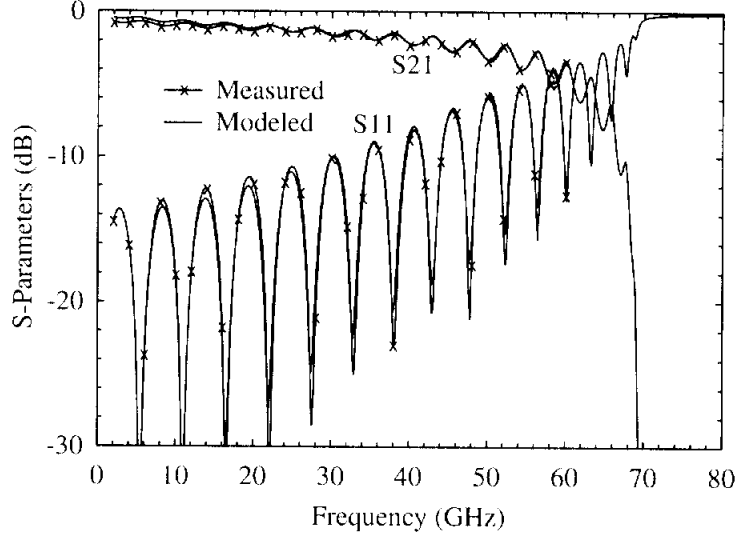


Figure 3.11: Measured and simulated S-parameters of a DMTL with 16 60- μm wide MEMS bridges spaced at 640 μm (total length = 10.8 mm, $Z = 62 \Omega$, $f_B = 62 \text{ GHz}$).

Table 3.3: Fitted Model Parameters for DMTL with $w/s = 60/640 \mu\text{m}$

C_b	48 fF
L_b	14 pH
$A(@ 20 \text{ GHz})$	0.6 dB/cm

Set parameters are: $Z_o=96 \Omega$, $\epsilon_{eff}=2.37$, $n=16$.

$L_b = 14 \text{ pH}$ is 5.7 while the measured value obtained from adjacent nulls in S11 is 6.2-6.5. After de-embedding the extension lines at either end of the DMTL, the effective dielectric constant is calculated from the measured data to be 5.7-6.1 ($l = 16 \times 640 \mu\text{m} = 10.2 \text{ mm}$) which is in agreement with the value calculated from (3.9).

According to (3.11), the characteristic impedance of this line should go from 62Ω at low frequencies to 50Ω at 35 GHz and then to 0Ω at 61 GHz. However, the measured results in Figure 3.11 show no indication, in the form of the peak of S11 falling below -30 dB, that the characteristic impedance of the loaded line goes through 50Ω . This is also an effect of the added lengths of line at either end of the DMTL. Figure 3.12 shows that the input-impedance circles are centered on points in the inductive part of the Smith chart and thus the centers never pass through 50Ω on the Smith chart. For this case, the line lengths at either end of the DMTL are 290 μm long. When these lines are de-embedded from the measured data, using the ABCD matrix approach, the results seen in Figure 3.13 are

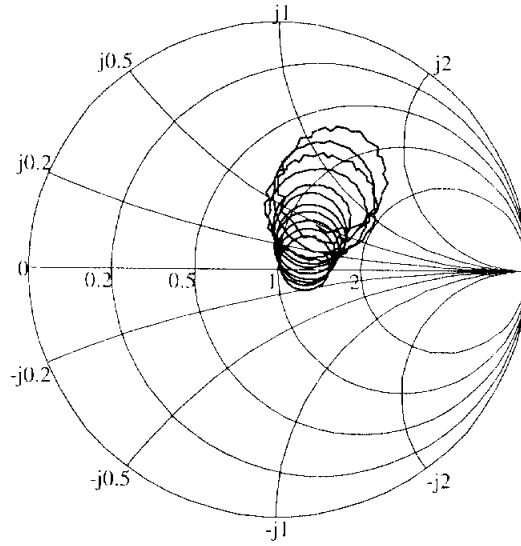


Figure 3.12: Measured S_{11} from 0-60 GHz for a DMTL with 16 $60\text{-}\mu\text{m}$ wide bridges spaced at $640\text{ }\mu\text{m}$.

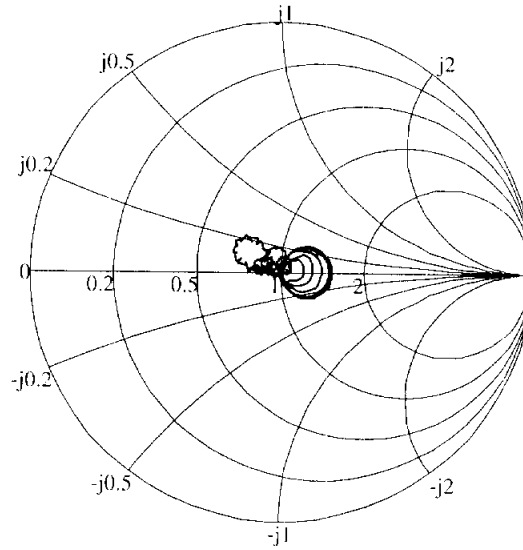


Figure 3.13: Measured S_{11} from 0-60 GHz for a DMTL with 16-60 μm wide bridges spaced at $640\text{ }\mu\text{m}$ with the $290\text{ }\mu\text{m}$ high impedance lines de-embedded.

found. It is seen that the input impedance is always centered on the real axis, and that the measured loaded-line impedance does indeed pass through the center of the Smith chart. However, the measured loaded-line impedance does not reach $50\ \Omega$ until 45 GHz rather than the predicted frequency of 35 GHz using (3.11).

Although the impedance of this line is approximately the same as the first line ($\sim 62\ \Omega$), this line has a much lower calculated Bragg frequency, 61 GHz according to (3.12), due to the larger loading capacitance and periodic spacing. The Libra circuit model, using the values given in Table 3.3, gives a value of 70 GHz as seen in Figure 3.11. An important observation is that both distributed lines (Figure 3.8 and Figure 3.11) show that the peak of the reflection coefficient approaches -10 dB at approximately half of the Bragg frequency when the added high impedance lines at either end of the DMTL are $(s - w)/2$ long. This is important when designing DMTLs for a specific frequency range.

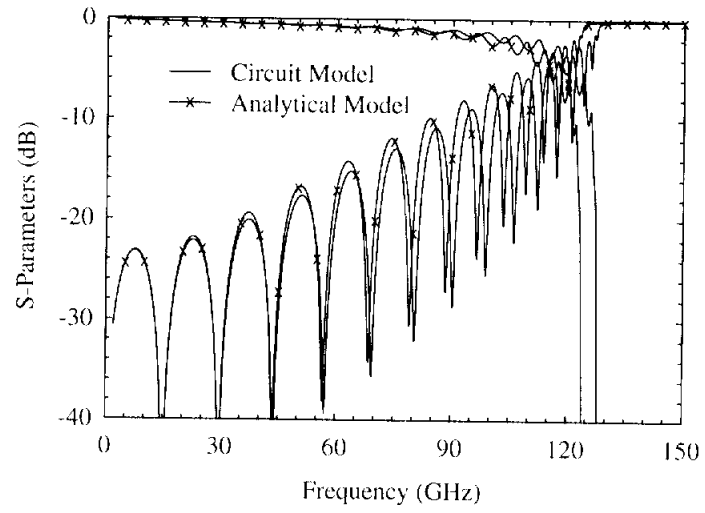
3.6 Comparison of Analytic and Circuit Model

In order to quantify the accuracy of the analytic model given in (3.3) and (3.5), the LC equivalent model is used to derive the S-parameters which are given by:

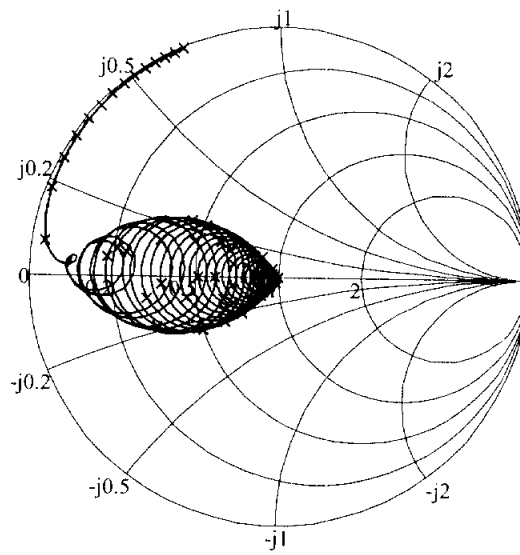
$$S = \begin{bmatrix} 0 & e^{-\gamma n} \\ e^{-\gamma n} & 0 \end{bmatrix} \quad (3.24)$$

where γ is the propagation constant per section and n is the number of sections in the DMTL. These S-parameters are referenced to the characteristic impedance of the DMTL given by (3.11). In order to compare these S-parameters with the Libra circuit simulation, they must be referred to $50\ \Omega$. This is done by converting the S matrix in (3.24) to a Z matrix and then back to an S matrix with a reference impedance of $50\ \Omega$.

The DMTL parameters for the first comparison are given in Table 3.4 with the S-parameters shown in Figure 3.14. As can be seen for this DMTL, the analytic model gives a good approximation up to 90 GHz and is reasonable even up to the Bragg frequency. This DMTL has a low-frequency characteristic impedance of $47\ \Omega$ and an effective dielectric constant of 10. The Bragg frequency calculated from the analytical model is 124 GHz while the circuit model results in a simulated value of 128 GHz.



(a)



(b)

Figure 3.14: Comparison between the circuit model and analytical model for the DMTL with parameters listed in Table 3.4.

Table 3.4: DMTL parameters for Figure 3.14.

Z_o	96 Ω
ϵ_{eff}	2.37
s	197 μm
C_b	34 fF
L_b	20 pH
A(@ 20 GHz)	0.52 dB/cm
n	16

Table 3.5: DMTL parameters for Figure 3.15.

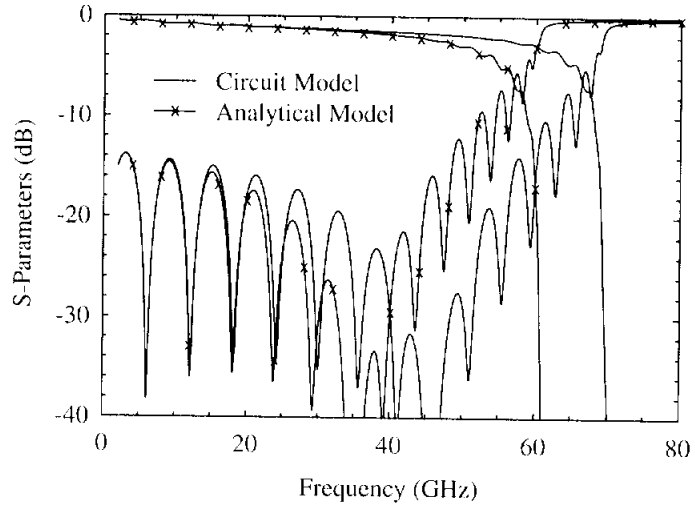
Z_o	96 Ω
ϵ_{eff}	2.37
s	640 μm
C_b	48 fF
L_b	14 pH
A(@ 20 GHz)	0.6 dB/cm
n	16

The parameters for the second comparison are given in Table 3.5 with the S-parameters shown in Figure 3.15. The low frequency impedance of this line is 62 Ω and the dip in S11 due to the impedance passing through 50 Ω is seen in both models. The effective dielectric constant at low frequencies is 5.7. The analytic model gives a good approximation up to 30 GHz, however, beyond that the models diverge rather quickly. The analytic model gives a calculated Bragg frequency of 61 GHz while the circuit model gives a simulated Bragg frequency of 70 GHz. This cannot be seen on a Smith chart representation since there is no frequency reference for the plotted data.

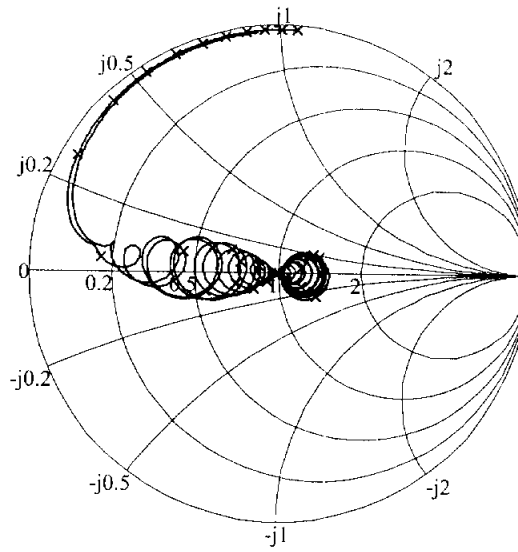
In general, the accuracy of the analytic model improves with both shorter periodic sections and increased loading. The increased accuracy with shorter periodic sections is due to the lumped elements, $s \cdot C_t$ and $s \cdot L_t$, giving a better approximation to the transmission line. The increased accuracy due to the increased loading is a result of the bridge capacitance having a more dominant affect so that the error in the lumped element approximation of the transmission line does not carry as much weight in the analysis.

3.7 Conclusion

Distributed MEMS transmission lines have been developed and tested up to 60 GHz. The DMTLs are fabricated using CPW lines on a quartz substrate with MEMS bridges periodically spaced across the line. An analytic model and a circuit model have been developed. The analytic model gives a good approximation of the performance at frequencies well below the Bragg frequency and can provide a reasonable approximation up to the Bragg frequency. This model provides an invaluable tool for designing DMTLs. The circuit model



(a)



(b)

Figure 3.15: Comparison between the circuit model and analytical model for the DMTL with parameters listed in Table 3.5.

has been shown to model the DMTL very well, even at frequencies approaching the Bragg frequency. The circuit model consists of a physical length of transmission line for the CPW line and a capacitor-inductor series combination to model the MEMS bridge. The circuit model has also been used to quantify the accuracy of the analytic model.

CHAPTER 4

Distributed MEMS Transmission Line Phase Shifters

This chapter presents the design and optimization of distributed MEMS transmission line (DMTL) phase shifters. The development of electronically variable phase shifters has been driven primarily by their usefulness in phased array radars, although they are now used in a wide range of systems including communications and measurement instrumentation [27].

Most phase shifters currently used can be divided into either ferrite phase shifters or semiconductor device phase shifters. The ferrite based phase shifters typically work well from 3 GHz to 60 GHz with switching times on the order of a few microseconds to tens of microseconds [21, 22]. Most ferrite based phase shifters are not monolithic and require large switching energies but can handle kilowatts of RF power [9]. Recently, there has been research into the use of the ferroelectric material barium strontium titanate [$\text{Ba}_{1-x}\text{Sr}_x\text{TiO}_3$ (BSTO)] to produce planar phase shifters [12]. The recent results demonstrate $44^\circ/\text{dB}$ insertion loss at 14.3 GHz, however, these devices require very high bias voltages (250-400 V) and suffer from increased losses above 20 GHz [56].

On the other hand, semiconductor device based phase shifters have been used up to 100 GHz with switching times well under $1\ \mu\text{s}$ [2, 7, 16, 27, 32, 39, 49, 52, 59]. These devices are either hybrid or monolithic with switching powers on the order of milliwatts. The hybrid devices (p-i-n or varactor diodes) can handle up to a kilowatt of RF power, however, the monolithic devices can only handle RF power on the order of milliwatts to one watt [27].

There are many different designs for the semiconductor device based phase shifters.

Some of the more prominent designs are switched-line phase shifters [52], loaded-line phase shifters [49, 2], branchline or 3-dB coupler based phase shifters [39, 7, 59], and high-pass/low-pass phase shifters [32]. The loaded-line and high-pass/low-pass type phase shifters are inherently limited to at most 67% bandwidth, whereas the switched-line phase shifter is true-time delay with the bandwidth limited by the high-frequency operation of the switches. Typical figures of merit for the semiconductor device based phase shifters are $144^\circ/\text{dB}$ at 1 GHz [32], $211^\circ/\text{dB}$ at 12 GHz [16], $86^\circ/\text{dB}$ from 16-18 GHz [7], $60^\circ/\text{dB}$ at 60 GHz [39], and $41^\circ/\text{dB}$ at 94 GHz [59]. Also, Goldsmith has shown 4-bit switched line phase shifters using MEMS switches with an average performance of $279^\circ/\text{dB}$ at 10 GHz and $138^\circ/\text{dB}$ at 35 GHz [17].

Recently another type of true-time delay phase shifter, known as the distributed phase shifter, has been investigated by Nagra *et al.* [35, 36]. Another demonstration, albeit with poor performance, is presented in [62]. These devices are very similar to the distributed MEMS transmission lines, but use varactor diodes rather than MEMS bridges for the variable capacitance. The phase shifters developed by Nagra *et al.* have shown good performance with $86^\circ/\text{dB}$ insertion loss at 20 GHz, or 4.2 dB insertion loss for 360° phase shift. However, the millimeter wave performance of these devices is severely limited by the series resistance of the diodes which is typically 2-6 Ω , and the integration of the phase shifter on GaAs substrates.

4.1 Design

As mentioned in Section 3.2, the DMTL can be used as a true-time delay (TTD) phase shifter since a change in the MEMS bridge capacitance changes the phase velocity of the line (see (3.9)). The change in the bridge capacitance is achieved by applying a single bias voltage to the center conductor of the DMTL with the CPW ground planes acting as a DC ground as well. This application is demonstrated in Figure 4.1(a) which shows the phase shift versus frequency, for varying bias voltages, of a DMTL with 32 $30\text{-}\mu\text{m}$ wide bridges spaced at $306\text{ }\mu\text{m}$. The unloaded line impedance is $96\text{ }\Omega$ ($W = 100\text{ }\mu\text{m}$ and $S = 300\text{ }\mu\text{m}$) with an effective dielectric constant of 2.37. As can be seen, the phase shift increases linearly

Table 4.1: Modeling parameters for DMTL in Figure 4.1.

$C_b(0 \text{ V})$	28 fF
$C_b(22 \text{ V})$	32.6 fF
L_b	18 pH
$A(@ 20 \text{ GHz})$	0.6 dB/cm

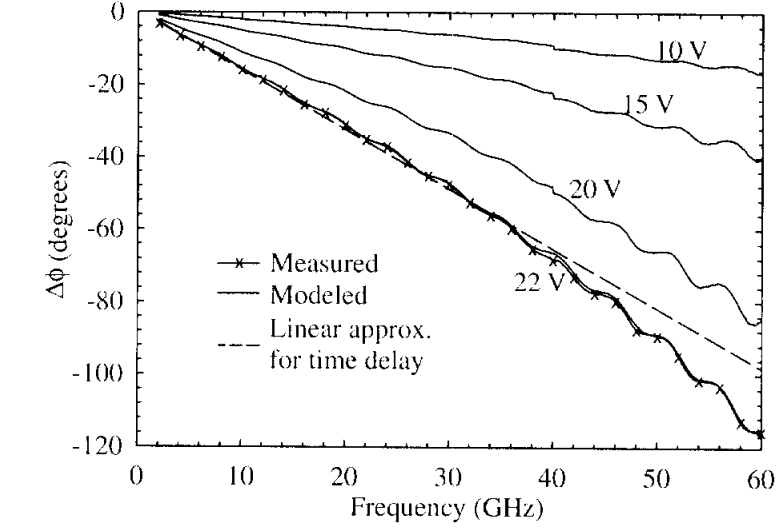
with frequency as expected for a TTD type phase shifter. There is some deviation from this linear increase at the upper end of the frequency range which is a result of approaching the Bragg frequency at 120 GHz. The maximum phase shift is 118° at 60 GHz with an associated insertion loss of 2.1 dB. The maximum time delay, at a bias voltage of 22 V, is 4.5 ps using the *linearly* extrapolated value of -98° at 60 GHz.

The change in the phase velocity is also manifested in the spacing of the nulls in the reflection coefficient seen in Figure 4.1(b). The reflection coefficient of the DMTL under 22 V bias has more closely spaced nulls indicating that the line is electrically longer than when the bias is 0 V. Since the physical length of the DMTL has not changed, the phase velocity of the line has decreased, as expected. The effective dielectric constant, calculated from the first three nulls in the reflection coefficient, is found to change from 7.2 at 0 V to 8.3 at 22 V. Using the circuit model presented in Section 3.4, the phase shift can be modeled as shown in Figure 4.1(a) using the parameters given in Table 4.1. It is seen that the match between the measured and modeled phase shift is nearly perfect.

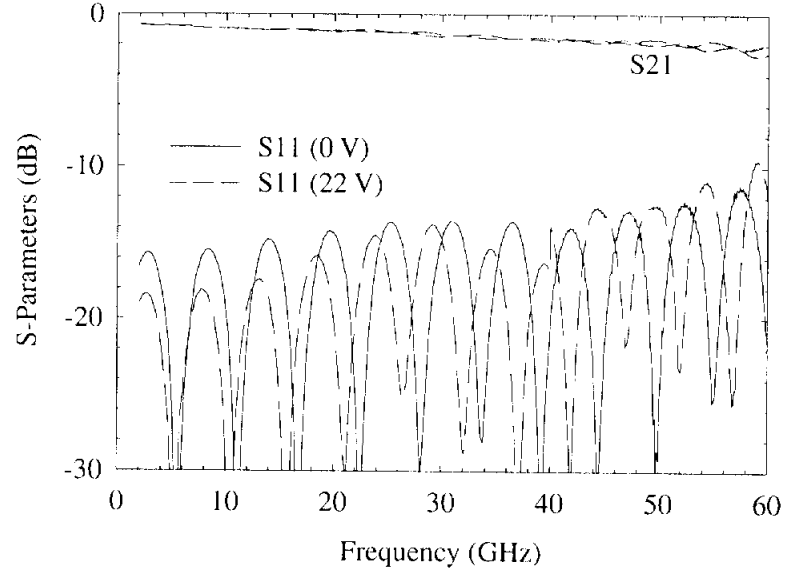
In addition to effecting the phase velocity, the change in bridge capacitance also changes the characteristic impedance, as indicated in (3.7). This effect can be seen in Figure 4.1(b) in which the peak in the low-frequency reflection coefficient at 2.7 GHz is seen to change from -15.7 to -18.4 dB. This peak in reflection coefficient occurs at a frequency where the DMTL is a quarter-wave length long and the input impedance, seen from the 50Ω feedline, is at a maximum given by [41]:

$$Z_{in} = \frac{Z^2}{50} \quad (4.1)$$

where Z is the characteristic impedance of the DMTL. Thus, the characteristic impedance of the DMTL in Figure 4.1 changes from 59Ω at 0 V to 56Ω at 22 V. It should be noted that although this is the same DMTL design as shown in Section 3.5, the impedance is calculated



(a)



(b)

Figure 4.1: Measured (a) phase shift and (b) S-parameters for a DMTL with 32 $30\text{-}\mu\text{m}$ -wide bridges spaced at $306\text{ }\mu\text{m}$ (total length = 10.1 mm) for varying bias voltage. The phase shift at 22 V is modeled with the circuit parameters given in Table 4.1.

to be 59 Ω rather than 61 Ω . In addition, the modeled zero-bias bridge capacitance is 28 fF rather than 25 fF. These differences are most likely due to process variations in the bridge height resulting in a slightly different loading capacitance.

The measured DMTL in Figure 4.1 has a capacitance ratio (C_{max}/C_{min}) of 1.16, so the impedance change is relatively small. However, if this capacitance ratio could be made much larger (5-10), the characteristic impedance of the DMTL would change by significant amounts causing undesirably large reflection coefficients. In this case, the DMTL should be designed such that the variation in characteristic impedance results in the same maximum allowable reflection coefficient in the low and high bridge capacitance states. For example, if it is desired to have the maximum reflection coefficient remain below -15 dB, then the characteristic impedance should be 60 Ω in the low capacitance state and 42 Ω in the high capacitance state. In general, the upper and lower bounds of the characteristic impedance, for a given reflection coefficient, are given by:

$$Z_{lu} = 50 \left(\frac{1 + S_{11}}{1 - S_{11}} \right)^{1/2} \quad \text{and} \quad Z_{ld} = 50 \left(\frac{1 - S_{11}}{1 + S_{11}} \right)^{1/2} \quad (4.2)$$

where Z_{lu} and Z_{ld} are the DMTL characteristic impedances for the low and high bridge capacitance states, respectively. Using (3.7), the minimum and maximum bridge capacitances are found to be:

$$C_{min} = \frac{sL_t}{50^2} \left(\frac{1 - S_{11}}{1 + S_{11}} \right) - sC_t \quad \text{and} \quad C_{max} = \frac{sL_t}{50^2} \left(\frac{1 + S_{11}}{1 - S_{11}} \right) - sC_t \quad (4.3)$$

From these equations the capacitance ratio, $C_r = C_{max}/C_{min}$, is found to be:

$$C_r = \frac{C_{max}}{C_{min}} = \frac{Z_o^2 \left(\frac{1+S_{11}}{1-S_{11}} \right) - 50^2}{Z_o^2 \left(\frac{1-S_{11}}{1+S_{11}} \right) - 50^2} \quad (4.4)$$

where $Z_o = \sqrt{L_t/C_t}$ is the characteristic impedance of the unloaded transmission line. Figure 4.2 shows this capacitance ratio versus the maximum allowable reflection coefficient for different unloaded-line impedances. It should be noted that the capacitance *ratio* is independent of the substrate dielectric constant. Also, this calculation is based on the low-frequency impedance and does not account for the effects of approaching the Bragg frequency shown in Section 3.5. It is seen that the usable capacitance ratio for a maximum reflection of -13 dB is around 3 for a 100 Ω unloaded impedance.

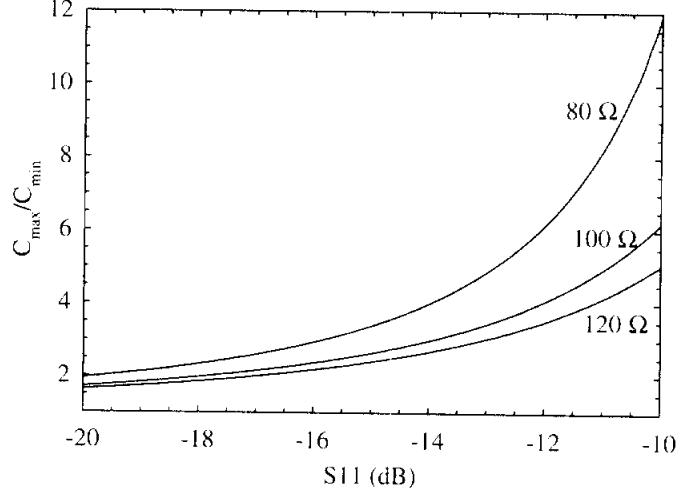


Figure 4.2: Capacitance ratio versus maximum reflection coefficient for unloaded-line impedances of 80, 100, and 120 Ω .

Of more importance for the DMTL phase shifter is the position of the Bragg frequency. The Bragg frequency, given by (3.8), dictates the upper frequency limit of the phase shifter. In this work, the upper frequency limit is defined to be where the return loss hits -10 dB. As was noted in Section 3.5, the peak reflection coefficient approaches -10 dB at approximately half the Bragg frequency, when the extension lengths at both ends of the DMTL are $(s-w)/2$ long. In addition, the Bragg frequency is dependent on the bridge capacitance such that the bandwidth should be defined using C_{max} rather than C_{min} since C_{max} will result in a lower Bragg frequency. A good example is Figure 4.1(b) where it is seen that the reflection coefficient at 22 V starts out below the 0 V case, but gradually rises above the 0 V case to -10 dB near 60 GHz, for a DMTL with a Bragg frequency of 120 GHz at 22 V bias.

The design of a DMTL phase shifter requires the specification of the bandwidth or Bragg frequency, substrate or dielectric constant, unloaded impedance, and loaded impedance. From these specifications, the bridge capacitance and spacing can be determined from (3.7) and (3.8), and are given by:

$$s = \frac{Z_{lu}}{\pi f_B \sqrt{L_t (C_r L_t - (C_r - 1) C_t Z_{lu}^2)}} \quad (4.5)$$

$$C_{bo} = s \left(\frac{L_t}{Z_{lu}^2} - C_t \right) \quad (4.6)$$

where in (3.8) the bridge capacitance and inductance have been set to $C_b = C_r \cdot C_{bo}$ and

$L_b = 0$, respectively. The per unit length inductance and capacitance, L_t and C_t , are given by [41]:

$$C_t = \frac{\sqrt{\epsilon_{r,\text{eff}}}}{cZ_o} \quad \text{and} \quad L_t = C_t Z_o^2 \quad (4.7)$$

in which $\epsilon_{r,\text{eff}}$ is the effective dielectric constant of the unloaded transmission line and c is the free-space velocity. For the case where the DMTL is constructed using a CPW line, Z_o and $\epsilon_{r,\text{eff}}$ can be related to the physical CPW line parameters by a conformal mapping [20]:

$$Z_o = \frac{\eta_o K(k')}{4\sqrt{\epsilon_{r,\text{eff}}} \cdot K(k)} \quad (4.8)$$

$$\epsilon_{r,\text{eff}} = \frac{\epsilon_r + 1}{2} \quad (4.9)$$

$$k = W/S$$

$$k' = \sqrt{1 - k^2}$$

where W and S are the center conductor width and total width of the CPW line, respectively, η_o is the free-space impedance, and $K(k)$ is the complete elliptic integral of the first kind. Using these equations, the DMTL phase shifter can be designed to a set of specifications. This initial design is then simulated using the Libra circuit model as discussed in Section 3.4. The Libra circuit model will give a more accurate value of the Bragg frequency from which the design can be fine tuned, using iterative methods, to the desired specifications.

4.2 Optimization

4.2.1 Theory

The optimization method used in this section is based on the work of Rodwell *et al.* [45, 44] which presented the first known analysis of loss in distributed non-linear CPW lines. The distributed line analysis was significantly extended to optimize for best phase shift by Nagra *et al.* [36]. In this thesis, we apply a method similar to Nagra to the case of

Table 4.2: Specifications for examples in Figures 4.3-4.7.

Z_{lu}	48 Ω
f_B	120 GHz
C_r	1.2

MEMS bridges to obtain the *maximum amount of phase shift for the minimum amount of insertion loss* in distributed MEMS phase shifters. In order to carry out this optimization, analytic expressions for both the phase shift per unit length and the insertion loss per unit length must be found. In addition, a set of design constraints must be specified which, for this optimization, are listed in Table 4.2. The choice of 48Ω for the zero-bias loaded impedance, Z_{ln} , is a compromise between higher phase shift but increased return loss and reduced bandwidth for a lower loaded impedance. The Bragg frequency in Table 4.2 is set to 120 GHz in order to limit the return loss to -10 dB up to 60 GHz as discussed in Section 4.1, while the capacitance ratio was determined to be 1.2 from previous DMTL measurements. The optimization analysis is carried out for silicon, quartz, and air substrates with the total width of the CPW, S , chosen to be approximately $\lambda_d/8$ and $\lambda_d/5$ at the maximum operating frequency of 60 GHz. A total width of $\lambda_d/8$ is typical for CPW designs in order to limit radiation loss, however, as mentioned in Section 3.3, the DMTL should not suffer from radiation loss and therefore a larger total width, $\lambda_d/5$, is usable.

Phase Shift

The phase shift is found from the change in the phase constant given by:

$$\begin{aligned}\Delta\phi &= \beta_1 - \beta_2 \\ &= \omega \left(\frac{1}{v_1} - \frac{1}{v_2} \right)\end{aligned}\tag{4.10}$$

Using the capacitance ratio, C_r , and (3.9) for the phase velocity, the phase shift is found to be:

$$\begin{aligned}\Delta\phi &= \omega\sqrt{L_t C_t} \left(\sqrt{1 + \frac{C_{bo}}{sC_t}} - \sqrt{1 + \frac{C_r C_{bo}}{sC_t}} \right) \\ &= \frac{\omega Z_0 \sqrt{\epsilon_{r,eff}}}{c} \left(\frac{1}{Z_{ln}} - \frac{1}{Z_{ld}} \right)\end{aligned}\tag{4.11}$$

Using this equation and (4.5)-(4.9), the phase shift per centimeter versus the center conductor width is calculated for DMTLs on silicon, quartz, and air at 40 GHz for the specifications listed in Table 4.2. As can be seen in Figure 4.3, the phase shift is much larger for narrow center conductor widths (high impedance). This is due to the larger loading capacitance per unit length, C_{bo}/s , needed to load the line to 48Ω and therefore the change in bridge

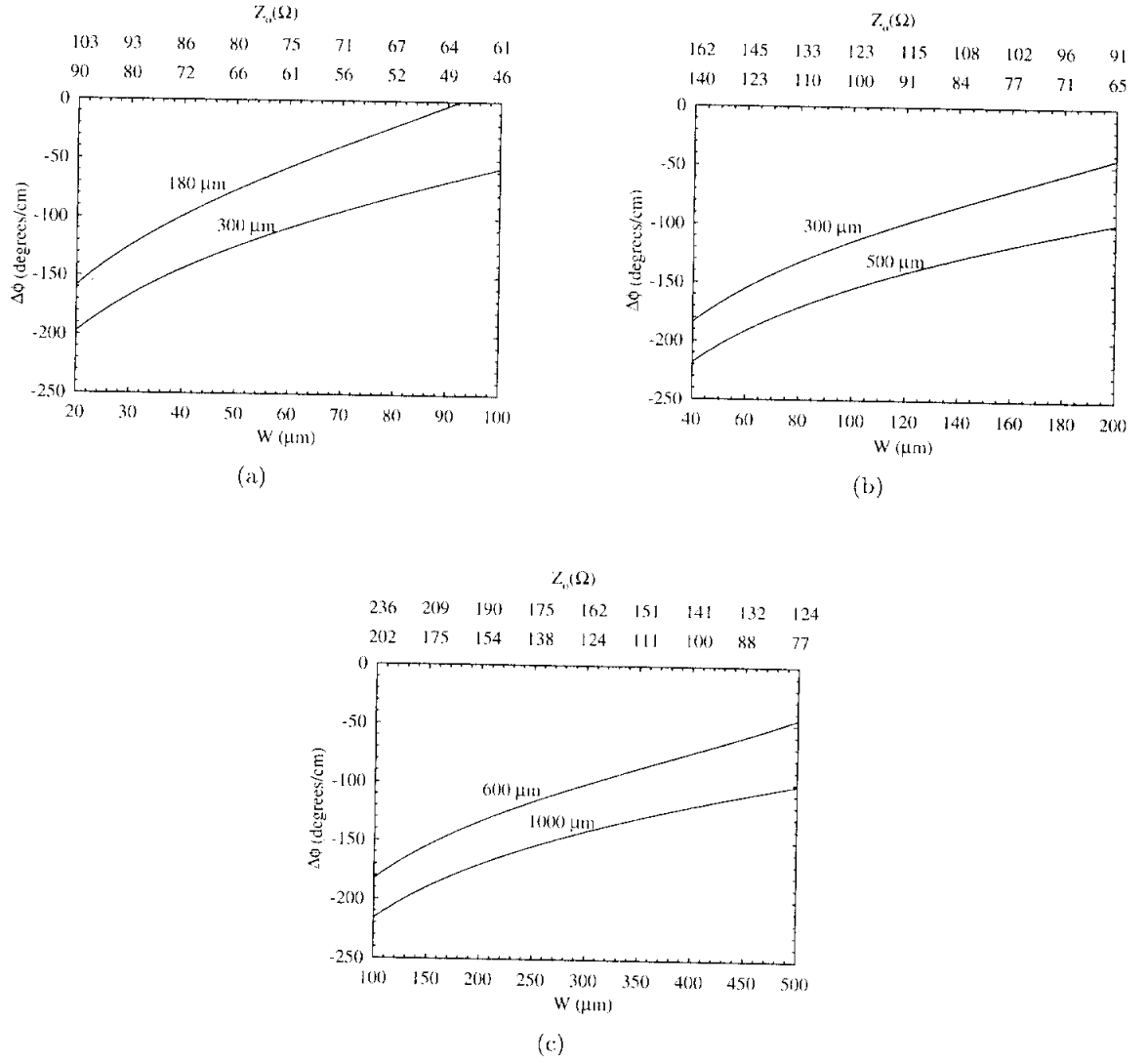


Figure 4.3: Calculated phase shift per centimeter vs. the CPW center conductor width at 40 GHz for (a) silicon, (b) quartz, and (c) air with a capacitance ratio of $C_r = 1.2$. The total CPW width is $\lambda_d/8$ and $\lambda_d/5$, at 60 GHz, for each substrate, and the Bragg frequency is set to 120 GHz. The impedance for the corresponding center conductor width is given at the top of each plot.

capacitance (from C_{bo} to $1.2 \cdot C_{bo}$) has a larger effect on the phase velocity. In addition, it is observed that for the same substrate, the two different total CPW widths give the same phase shift for the same impedance. For instance, on quartz the 300 μm total width line with a center conductor width of 100 μm and the 500 μm total width line with a center conductor width of 167 μm have an impedance of 100 Ω and a corresponding phase shift of

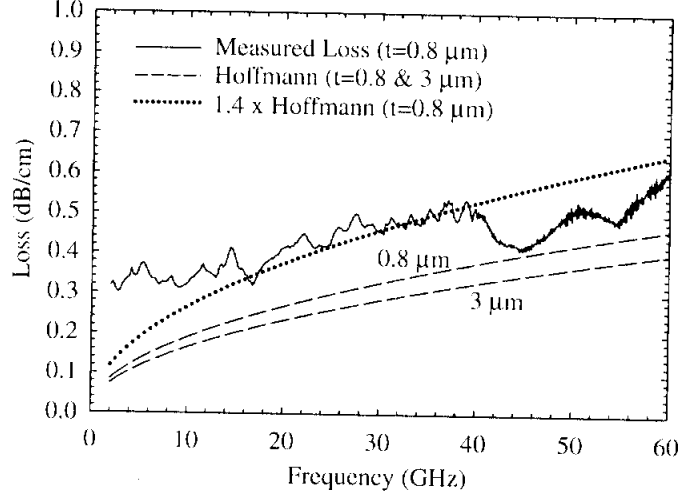


Figure 4.4: Measured and calculated loss vs. frequency for a 300 μm total width unloaded CPW line on quartz with a 100 μm wide center conductor ($Z_o = 100 \Omega$).

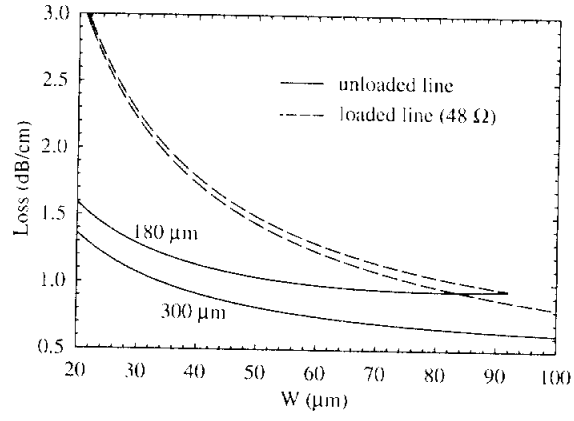
-115°/cm. The curve for silicon with a 180 μm total width line is seen to hit zero degrees at a center conductor width of 92 μm , which corresponds to an unloaded impedance of 48 Ω resulting in $C_{bo}/s = 0$ and no phase shift.

Loss

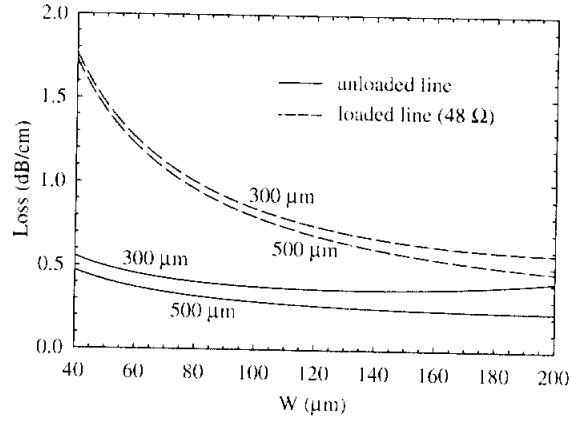
The transmission line loss for the unloaded CPW line is found from a conformal mapping technique and is given by Hoffmann [20]:

$$\alpha = \frac{8.686 \cdot 10^{-2} R_s \sqrt{\epsilon_{r,\text{eff}}}}{4\eta_o S K(k) K(k') (1 - k^2)} \cdot \left[\frac{2S}{W} \left\{ \pi + \ln \left(\frac{4\pi W(1 - k)}{t(1 + k)} \right) \right\} + 2 \left\{ \pi + \ln \left(\frac{4\pi S(1 - k)}{t(1 + k)} \right) \right\} \right] \quad (\text{dB/cm}) \quad (4.12)$$

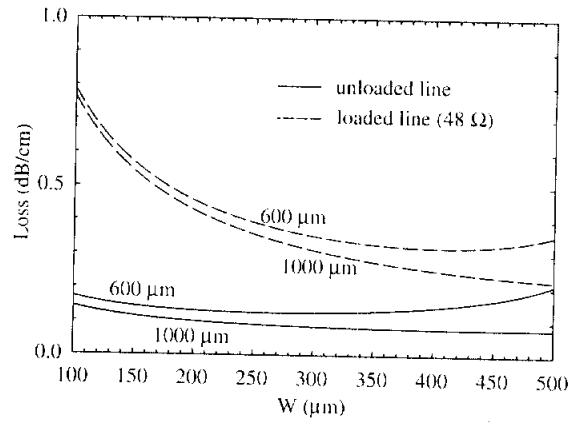
where t is the metal thickness, R_s is the surface resistance given by $R_s = \sqrt{\pi f \mu_o / \sigma}$, and σ is the conductivity of the metal. It should be noted that this equation significantly underestimates the measured loss of the CPW line on quartz. Figure 4.4 shows the measured and calculated loss versus frequency for a 300 μm total width CPW line on quartz with a 100 μm wide center conductor ($Z_o = 100 \Omega$). The CPW line is 8000 Å of gold with a conductivity of $3.3 \cdot 10^{-7}$ S/m. Significantly less loss can be obtained, particularly at low frequencies, if a 3 μm thick center conductor is used. In this case, the center conductor



(a)



(b)



(c)

Figure 4.5: Calculated loss for the unloaded and loaded transmission lines at 40 GHz vs. CPW center conductor width for (a) silicon, (b) quartz, and (c) air substrates. The total CPW width is $\lambda_d/8$ and $\lambda_d/5$, at 60 GHz, for each substrate, and the Bragg frequency is set to 120 GHz.

between the MEMS bridges would be electroplated to $3\text{ }\mu\text{m}$ while the section underneath the MEMS bridge would remain $8000\text{ }\text{\AA}$ thick. This was not done in this work for simplicity in fabrication, but will be done in future work (see Chapter 6). The line loss calculated from (4.12) is for a metal thickness of $0.8\text{ }\mu\text{m}$ which, at 40 GHz , is 1.8 skin depths. However, according to (4.12) and Figure 4.4, if the metal thickness is increased to $3\text{ }\mu\text{m}$ the loss would decrease by a factor of 1.15 *independent* of frequency. This is known to be incorrect since the loss depends on the skin depth, and once the metal thickness reaches several skin depths, it will cease to decrease with increased thickness. Thus, (4.12) should not be used to predict the loss performance of the line, but more as a guide to predict the *trend of loss* versus center conductor width.

As can be seen, the equation from Hoffmann must be increased by a factor of 1.4, in this case, in order to match the measured results. Notice that above 40 GHz the unloaded CPW line is starting to radiate and this results in an adverse effect on the calibration standards and loss estimation using the TRL technique. The phase shift per dB loss derived in this section uses (4.12) without any modification and thus predicts much better performance than will actually be achieved. However, it is believed that the loss versus center conductor width trend is correct and thus, (4.12) can be used to find the optimal center conductor width.

The loaded loss is calculated, as discussed in Section 3.3, by multiplying α by the ratio of the unloaded impedance, Z_o , to the loaded impedance, Z , given in (3.7). The loaded impedance in the high capacitance state, Z_{ld} , is used since this gives the maximum loss due to the fact that it is the lowest impedance state. There is not a large change in the line loss since the line impedance is only changing by $3\text{-}4\text{ }\Omega$ for a capacitance ratio of 1.2. If the capacitance ratio is increased to 1.5, then the impedance change goes up to $7\text{-}8\text{ }\Omega$. In this case, the DMTL, which starts at a loaded impedance of $48\text{ }\Omega$, will change to a loaded impedance of $40\text{-}41\text{ }\Omega$ when bias is applied. This will result in a -13 to -14 dB reflection loss which is still within the design constraint of -10 dB . However, it may be desirable to reduce the reflection loss by changing the zero-bias loaded impedance to $52\text{ }\Omega$ so that the $7\text{-}8\text{ }\Omega$ impedance change will not adversely effect the phase shifter performance.

Figure 4.5 shows the calculated line loss at 40 GHz for the unloaded and loaded CPW

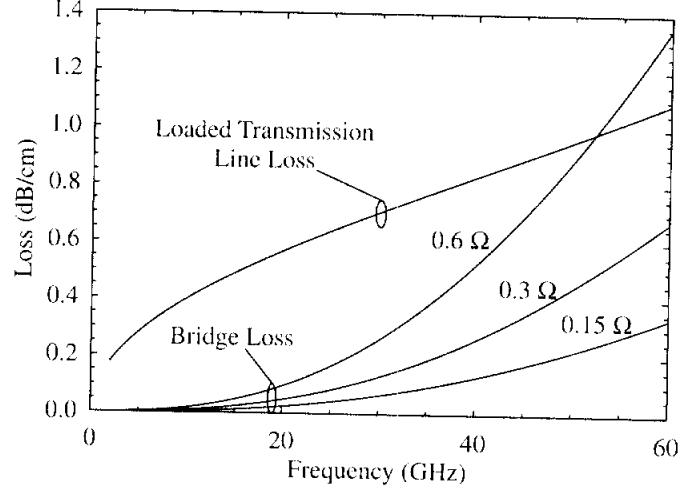
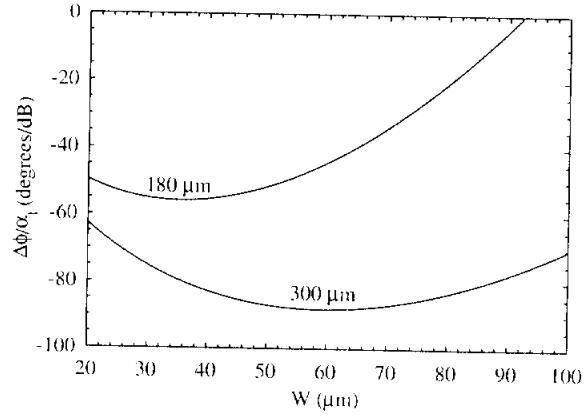


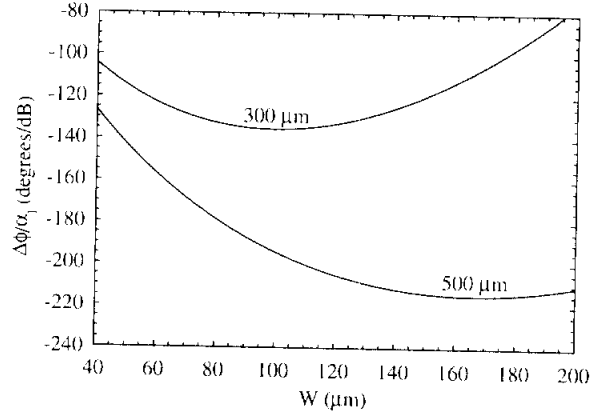
Figure 4.6: Loaded transmission line loss and loss due to bridge resistance vs. frequency. The line loss is calculated from Hoffmann's equation for a $300\text{ }\mu\text{m}$ total width CPW line with a $100\text{ }\mu\text{m}$ width center conductor. The Bragg frequency is 120 GHz , the bridge spacing is $197\text{ }\mu\text{m}$ and the bridge capacitance is 34.6 fF .

line for silicon, quartz, and air using the specifications listed in Table 4.2 and $8000\text{ }\text{\AA}$ of gold ($\sigma = 3.3 \cdot 10^{-7}\text{ S/m}$) for the metal thickness, t . As expected, the unloaded line loss increases as the dielectric constant increases due to smaller CPW line dimensions. In addition, the loaded line loss for silicon, with a $180\text{ }\mu\text{m}$ total CPW width, converges with the unloaded line loss at a center conductor width of $92\text{ }\mu\text{m}$ where the unloaded line impedance is $48\text{ }\Omega$ and the capacitive loading goes to zero.

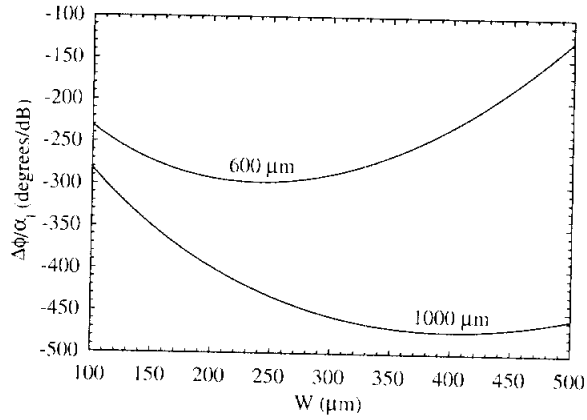
In the calculations of the loaded loss the bridge resistance has been ignored. This is acceptable for calculations up to 60 GHz since, as discussed in Section 3.3, the loss due to a bridge resistance of $0.15\text{ }\Omega$ at 30 GHz is 5% of the total loss of the loaded line at 30 GHz and 15% at 60 GHz . The loss due to the bridge resistance versus frequency is shown in Figure 4.6 for bridge resistances of 0.15 , 0.3 and $0.6\text{ }\Omega$. The calculation is for a $300\text{ }\mu\text{m}$ total width CPW line with a $100\text{ }\mu\text{m}$ width center conductor ($Z_o = 100\text{ }\Omega$) loaded to $48\text{ }\Omega$ and a Bragg frequency of 120 GHz . The line loss is calculated from (4.12) and then multiplied by the ratio of change in impedance to arrive at the loaded loss. It is seen that the distributed phase shifter is line loss limited up to 60 GHz for bridge resistances of 0.15 and $0.3\text{ }\Omega$, whereas for a $0.6\text{ }\Omega$ bridge resistance, the bridge loss starts to dominate above 50 GHz .



(a)



(b)



(c)

Figure 4.7: Calculated phase shift per dB loss at 40 GHz vs. CPW center conductor width for (a) silicon, (b) quartz, and (c) air substrates with a capacitance ratio of $C_r = 1.2$. The total CPW width is $\lambda_d/8$ and $\lambda_d/5$ for each substrate and the Bragg frequency is set to 120 GHz.

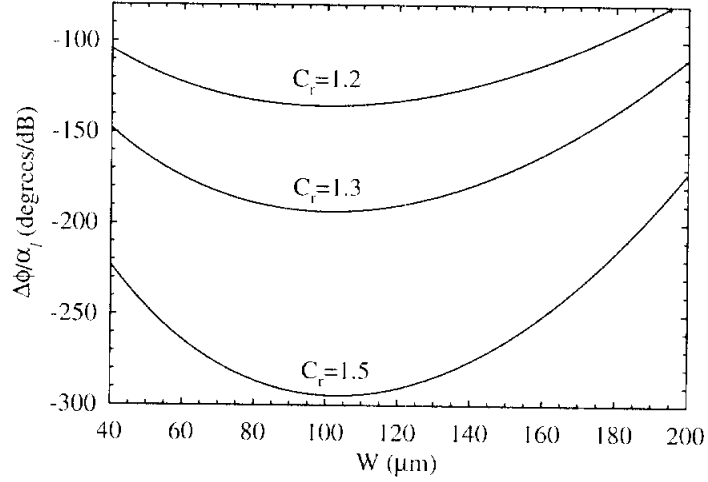


Figure 4.8: Calculated phase shift per dB loss at 40 GHz versus center conductor width for a 300 μm total width CPW line on quartz. The capacitance ratio is varied from 1.2 to 1.5 with a loaded impedance of 48 Ω and a Bragg frequency of 120 GHz.

Optimization

The optimal center conductor width (and unloaded impedance) is found by dividing the phase shift per centimeter by the loss per centimeter to find the phase shift per dB loss. Figure 4.7 shows the calculation at 40 GHz for silicon, quartz, and air substrates for a capacitance ratio of 1.2. The optimum center conductor width is seen to occur at 36 μm ($S = 180 \mu\text{m}$) and 60 μm ($S = 300 \mu\text{m}$) for silicon at an unloaded impedance of 75 Ω , 100 μm ($S = 300 \mu\text{m}$) and 167 μm ($S = 500 \mu\text{m}$) for quartz at an impedance of 100 Ω , and 240 μm ($S = 600 \mu\text{m}$) and 400 μm ($S = 1000 \mu\text{m}$) for air at an impedance of 141 Ω . Also, the optimal phase shift per dB loss increases as the dielectric constant decreases and is $-56^\circ/\text{dB}$ ($S = 180 \mu\text{m}$) and $-88^\circ/\text{dB}$ ($S = 300 \mu\text{m}$) for silicon, $-136^\circ/\text{dB}$ ($S = 300 \mu\text{m}$) and $-215^\circ/\text{dB}$ ($S = 500 \mu\text{m}$) for quartz, and $-297^\circ/\text{dB}$ ($S = 600 \mu\text{m}$) and $-473^\circ/\text{dB}$ ($S = 1000 \mu\text{m}$) for air.

As seen from (4.11) and (4.12), the phase shift increases linearly with frequency and the loss increases as \sqrt{f} , due to R_s . Therefore, the phase shift per dB loss will increase as \sqrt{f} . Thus, for the 300 μm total width line on quartz the phase shift per dB loss increases from $-96^\circ/\text{dB}$ to $-136^\circ/\text{dB}$ to $-166^\circ/\text{dB}$ at 20, 40, and 60 GHz, respectively.

The phase shift per dB loss can be considerably improved if the capacitance ratio, C_r , is increased to 1.3 or 1.5. This is seen in Figure 4.8 in which the calculated phase shift per dB

Table 4.3: Specifications of the DMTLs used to verify the optimization procedure.

Z_{lu}	48 Ω
f_B	120 GHz
S	300 μm
C_r	1.2

Table 4.4: Dimensions of the DMTLs used to verify the optimization. The Bragg frequency is calculated using $L_b = 20$ pH. $R_b = 0.15 \Omega$ at 30 GHz.

$W(\mu\text{m})$	50	100	150
$C_{bo}(\text{fF})$	37.9	33.8	28.6
$s(\mu\text{m})$	150	197	249
$w(\mu\text{m})$	80	35	17
$f_B(\text{GHz})$	119	122	127

loss versus center conductor width is plotted for a 300 μm total width CPW line on quartz with varying capacitance ratios. The maximum phase shift per dB loss is increased from $-136^\circ/\text{dB}$ to $-194^\circ/\text{dB}$ and $-295^\circ/\text{dB}$ for capacitance ratios of 1.2, 1.3, and 1.5, respectively. Therefore, it is necessary to obtain a large capacitance ratio for very low loss performance.

4.2.2 Experiment

In order to verify the position of the optimal center conductor width, three DMTL designs were fabricated on quartz with center conductor widths of 50, 100, and 150 μm with the specifications listed in Table 4.3. Using the design equations (4.5)-(4.9), the bridge capacitances and spacings for the three center conductor widths are calculated and shown in Table 4.4. When using the design equations, the bridge inductance is neglected, however this inductance has been shown, in Section 3.2, to have a large effect on the Bragg frequency. Therefore, in order to account for this effect, the Bragg frequency used in (4.5) is set to 140 GHz rather than the specified 120 GHz. The Bragg frequency is then calculated, including a bridge inductance of 20 pH, using (3.12). A constant bridge inductance is used, regardless of the bridge width, due to the fact that the bridge inductance is a weak function of the bridge width [33]. As can be seen in Table 4.4, the Bragg frequency is close to 120 GHz for all three cases. The bridge height for these designs is 1.2 μm and the bridge widths are determined using the static-field solver Maxwell 3D, with the results given in Table 4.4. Figure 4.9 shows the calculated loaded and unloaded loss at 40 GHz, with $C_r = 1.17$, as well as the measured data points. The measured unloaded line loss is approximately a factor of 1.4 higher than the loss calculated from (4.12) as seen in Figure 4.4. However, as seen in Figure 4.9,

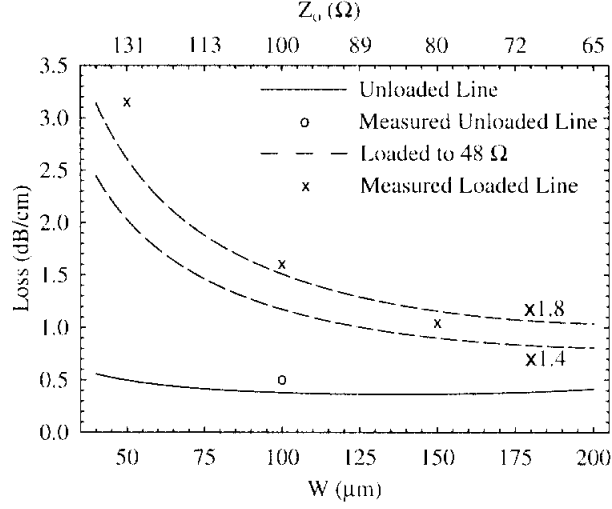


Figure 4.9: Unloaded (—) and loaded (---) line loss at 40 GHz. The calculated loaded line loss has been increased by a factor of 1.4 and 1.8, however, it is seen that the factor of 1.8 fits the measured loss best. The impedances for the labeled widths are included for reference.

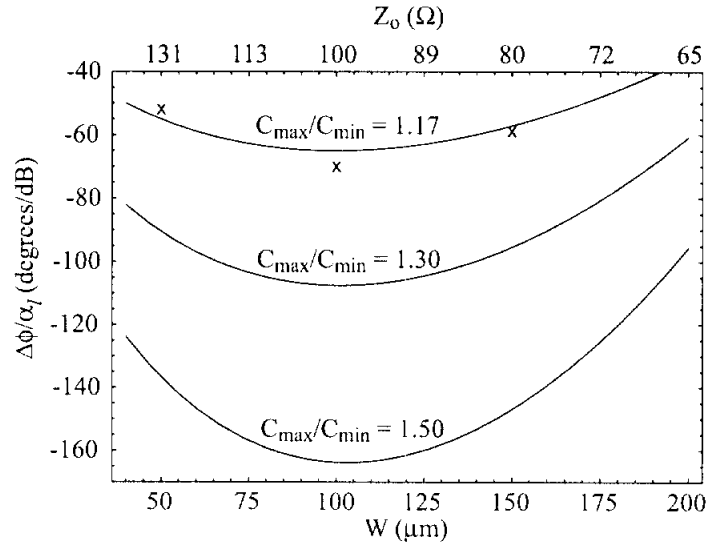


Figure 4.10: Calculated phase shift per dB loss at 40 GHz with capacitance ratios of 1.17, 1.3, and 1.5. Measured data points (x) are included for CPW center conductor widths of 50, 100, and 150 μm .

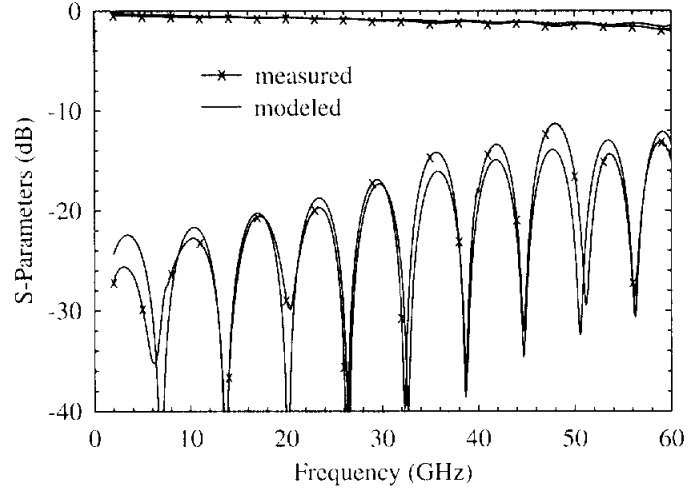
Table 4.5: Circuit model parameters for the optimal DMTL ($W = 100 \mu\text{m}$).

$C_{bo}(0 \text{ V})$ (fF)	34.6
$C_{bo}(13 \text{ V})$ (fF)	40.6
L_b (pH)	11
A @ 20 GHz (dB/cm)	0.46
Z_{lu} (Ω)	47
Z_{ld} (Ω)	45

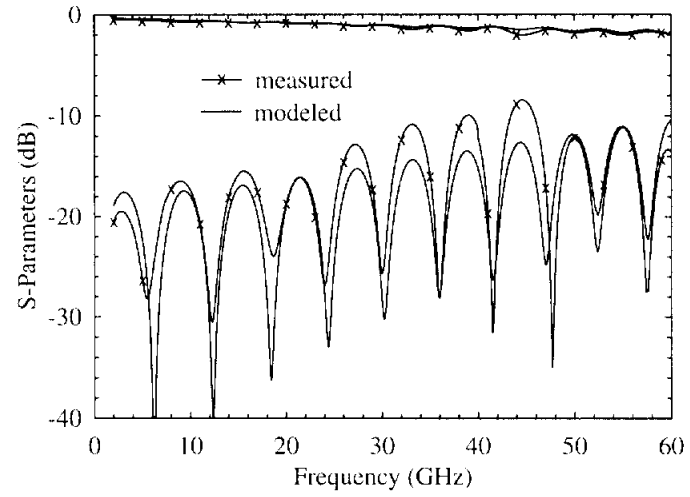
the calculated loaded loss, using the same factor of 1.4, does not match the measured loaded loss. Instead, a factor of 1.8 matches the measured results. The reason for the difference in the multiplication factor is unknown. The difference could be due to additional loading effects, such as a change in the current distribution on the transmission line, which are not accounted for in the formulation of the loaded line loss. It should also be mentioned that Muldavin *et al.* have shown that the bridge resistance does not vary much with bridge width and thus, a constant bridge resistance of 0.15Ω at 30 GHz is used for all three cases in Table 4.4 [33].

Figure 4.10 shows the calculated phase shift per dB loss for capacitance ratios of 1.17, 1.3, and 1.5 at 40 GHz. The results of the measured DMTLs, with a capacitance ratio of 1.17, are seen to verify the position of an optimal point at $100 \mu\text{m}$ for the center conductor width, and the phase shift per dB for the optimal line ($W = 100 \mu\text{m}$) is measured to be $-70^\circ/\text{dB}$ at 40 GHz. The calculated phase shift per dB loss, based on the *measured* line loss, for capacitance ratios of 1.3 and 1.5 show that the performance of the DMTL can be greatly increased to $-108^\circ/\text{dB}$ and $-164^\circ/\text{dB}$, respectively, which is the equivalent of 3.3 dB and 2.2 dB insertion loss for 360° phase shift at 40 GHz.

Figure 4.11 shows the measured and modeled S-parameters for the optimal DMTL phase shifter with a $100 \mu\text{m}$ center conductor at 0 V and its maximum bias voltage of 13 V. The parameters used in the circuit model are listed in Table 4.5. As can be seen, the zero-bias bridge capacitance, C_{bo} is very close to the designed value of 33.8 fF and the return loss rises up to -10 dB at 60 GHz, when the maximum bias is applied, as desired. The discrepancies between the measured and modeled data seen in the return loss are most likely due to small variations in the bridge height among the 38 bridges used in this DMTL.



(a)



(b)

Figure 4.11: Measured and modeled S-parameters of the $W = 100 \mu\text{m}$ DMTL with 38 bridges (total length= 7.6 mm) at (a) 0 V and (b) a maximum applied bias of 13 V.

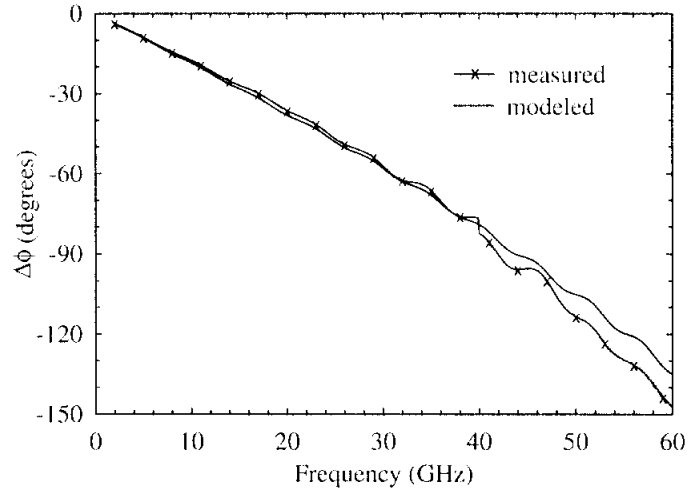


Figure 4.12: Measured and modeled phase shift of the $W = 100 \mu\text{m}$ DMTL at 13 V.

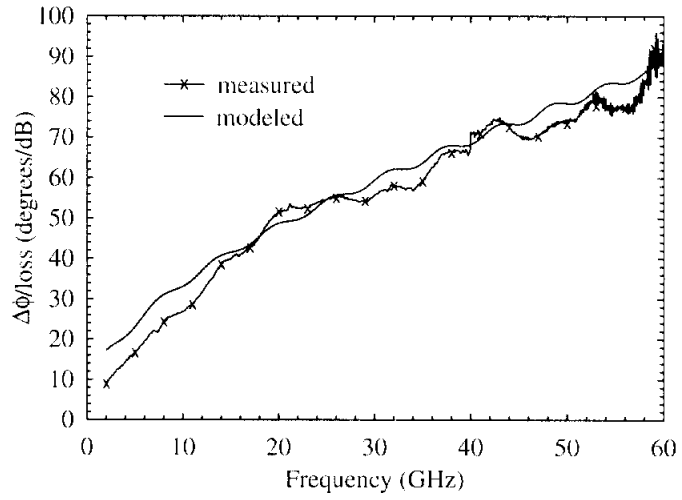


Figure 4.13: Measured and modeled phase shift per dB loss for the $W = 100 \mu\text{m}$ DMTL showing $90^\circ/\text{dB}$ at 60 GHz or 4 dB loss for 360° phase shift.

The measured and modeled phase shift are shown in Figure 4.12 with excellent agreement between the two data. The maximum measured phase shift is 148° at 60 GHz which corresponds to a time delay of 6.8 ps. Dividing the measured phase shift by the measured insertion loss, with the reflection loss removed, results in the plot shown in Figure 4.13 in which the modeled data is again shown to be in good agreement with measurement. It is seen that $70^\circ/\text{dB}$ at 40 GHz and $90^\circ/\text{dB}$ at 60 GHz are achieved with this line. Thus, this DMTL is capable of giving 360° phase shift at 40 GHz with 5.1 dB loss and at 60 GHz with 4 dB loss.

The phase shift per dB is seen to increase with frequency as \sqrt{f} which is in agreement with theory since the loss increases as \sqrt{f} and the phase shift increases as f . However, this only holds true so long as the loss due to the bridge resistance remains small compared to the transmission line loss. Once the loss due to the bridge begins to become significant it increases as $f^{5/2}$ (assuming R_b increases as \sqrt{f}), as shown in (3.20) and Figure 4.6, and will quickly dominate the phase shift per dB loss, causing it to decrease with frequency.

This phase shifter was designed to operate up to 60 GHz ($S = 300\ \mu\text{m}$, $W = 100\ \mu\text{m}$, $t = 8000\ \text{\AA}$, $f_B = 120\ \text{GHz}$), and therefore, at 10 or 20 GHz, does not give optimal phase shifter performance. If the DMTL is redesigned to operate up to 20 GHz, a much higher phase shift per dB loss could be achieved up to this frequency since the design would dictate a wider CPW total width and a much thicker metal, resulting in a reduced unloaded line loss. Also, the capacitive loading would be increased such that the Bragg frequency would be 40 GHz rather than 120 GHz as it is for the 60 GHz design.

4.3 W-Band DMTL Phase Shifter

The design procedure for a W-band phase shifter is identical to that given in the previous section, however, there are some additional effects which must be taken into consideration at higher frequencies. One such effect is loss due to the bridge resistance, which becomes significant at W-band frequencies as demonstrated in Figures 4.14 and 4.15. In Figure 4.14, the loss due to bridge resistance versus frequency is shown for bridge resistances of 0.15, 0.3, and $0.6\ \Omega$. The calculation is for a $300\ \mu\text{m}$ total width CPW line with a $100\ \mu\text{m}$ center

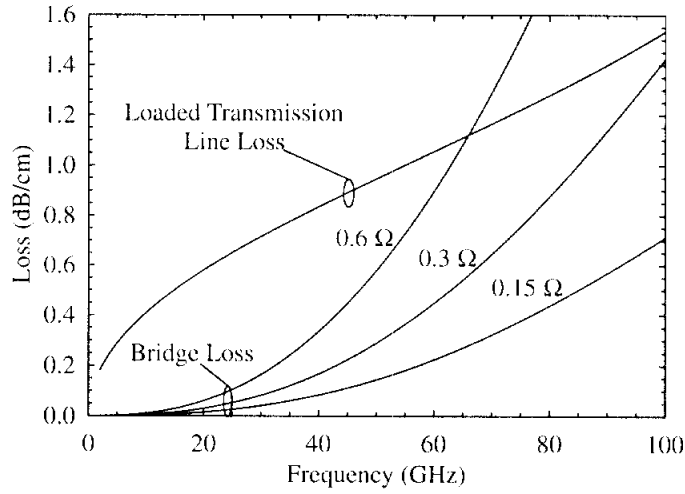


Figure 4.14: Loaded transmission line loss and loss due to bridge resistance vs. frequency. The line loss is calculated from Hoffmann's equation for a $300\text{ }\mu\text{m}$ total width CPW line with a $100\text{ }\mu\text{m}$ width center conductor. The Bragg frequency is 180 GHz , the bridge spacing is $110\text{ }\mu\text{m}$ and the bridge capacitance is 20.7 fF .

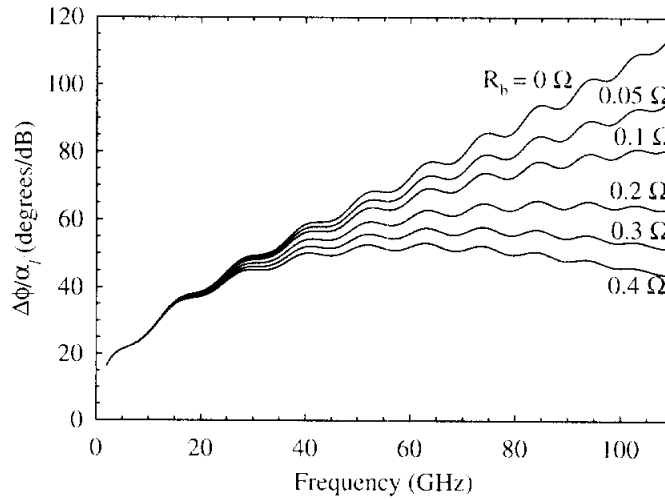
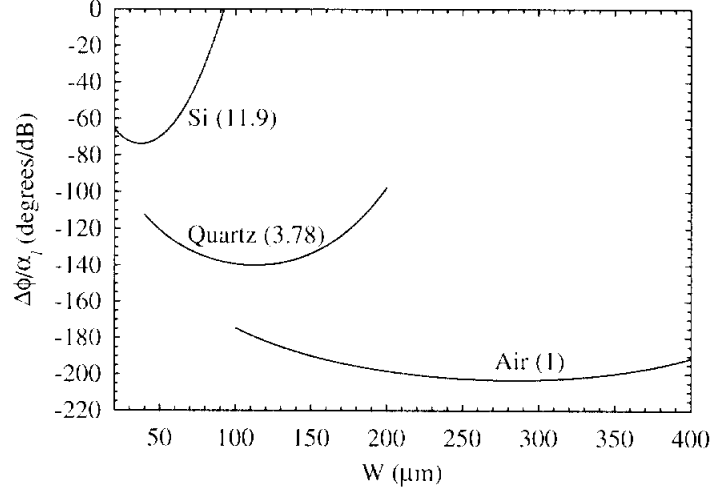


Figure 4.15: Phase shift per dB loss calculated from a Libra circuit simulation of a 32 bridge DMTL on quartz with a capacitance ratio of 1.17 and different bridge resistances specified at 30 GHz and varying as \sqrt{f} .

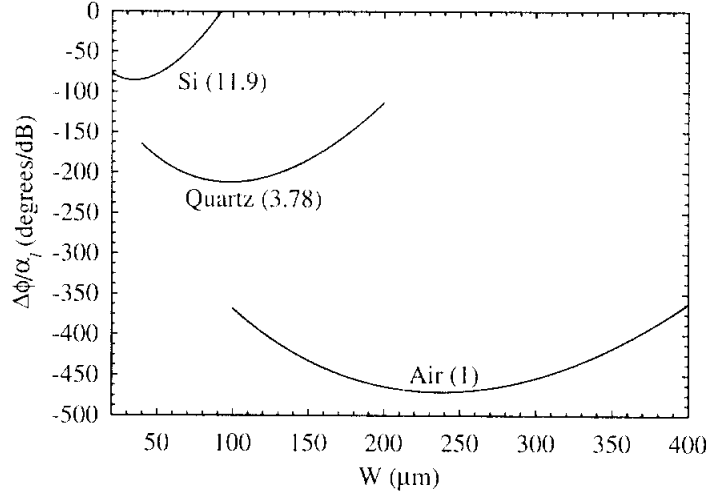
conductor width ($Z_o = 100 \, \Omega$) loaded to $48 \, \Omega$ and a Bragg frequency of 180 GHz. The line loss is calculated from (4.12) and then multiplied by the ratio of change in impedance to arrive at the loaded loss. It is seen that the distributed phase shifter is line-loss limited up to 100 GHz for bridge resistances of 0.15 and $0.3 \, \Omega$ where as for a $0.6 \, \Omega$ resistance the bridge loss starts to dominate above 65 GHz. In Figure 4.15 a Libra circuit simulation has been carried out for a 32 bridge DMTL with an unloaded impedance of $96 \, \Omega$, an effective dielectric constant of 2.37, a loaded impedance of $48 \, \Omega$, a capacitance ratio of 1.17, and different bridge resistances, R_b , specified at 30 GHz and varying as \sqrt{f} . It is seen that as the bridge resistance increases, the phase shift per dB loss starts to level off and can even decrease with frequency for the higher resistances. The phase shift per dB loss drops from $115^\circ/\text{dB}$ at 110 GHz for no bridge resistance, to $80^\circ/\text{dB}$ for a $0.1 \, \Omega$ bridge resistance, and to $44^\circ/\text{dB}$ for a $0.4 \, \Omega$ bridge resistance.

This additional loss also has an effect on the optimization curve used to determine the optimal center conductor width. Figure 4.16 shows the calculation of the optimal center conductor width for silicon, quartz, and air substrates with a total CPW width of $\lambda_d/5$ at 100 GHz, a loaded impedance, Z_{lu} , of $48 \, \Omega$, a capacitance ratio of 1.2, a Bragg frequency of 240 GHz, and a bridge resistance of $0.15 \, \Omega$ at 30 GHz ($0.27 \, \Omega$ at 100 GHz) in Figure 4.16a and $0 \, \Omega$ in Figure 4.16b. It is seen in Figure 4.16a that the optimal center conductor width for silicon is $37 \, \mu\text{m}$, for quartz is $113 \, \mu\text{m}$, and for air is $283 \, \mu\text{m}$ compared with $36 \, \mu\text{m}$, $100 \, \mu\text{m}$ and $240 \, \mu\text{m}$ in Figure 4.16b, respectively. Although the bridge resistance has not altered the optimal center conductor width by very much, the phase shift per dB has changed significantly. Thus, in general, the bridge resistance can be safely ignored for *circuit design* purposes (choosing the center conductor width), but must be taken into account in the circuit model and when evaluating the phase shifter performance (calculating phase shift per dB loss).

Another effect which must be considered at W-band is radiation from the DMTL. As mentioned in Section 3.3, when the effective dielectric constant of the DMTL is above the relative dielectric constant of the substrate, the DMTL should not be able to radiate due to slow-wave propagation. As seen in Figure 4.17, this condition is satisfied for the entire range of center conductor widths for quartz and up to $55 \, \mu\text{m}$ ($Z_o = 63 \, \Omega$) for silicon. Using



(a)



(b)

Figure 4.16: Calculated phase shift per dB loss versus center conductor width at 100 GHz for a bridge resistances of (a) $0.15 \, \Omega$ at 30 GHz and (b) $0 \, \Omega$. The total CPW width is $\lambda_d/5$ at 100 GHz for each substrate which is $180 \, \mu\text{m}$, $300 \, \mu\text{m}$, and $600 \, \mu\text{m}$ for silicon, quartz, and air, respectively. The loaded impedance is $48 \, \Omega$, the capacitance ratio is 1.2, and the Bragg frequency is 240 GHz.

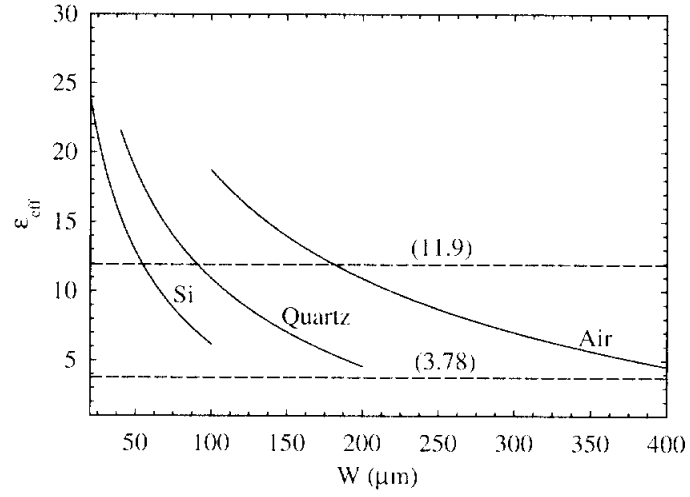


Figure 4.17: Calculated effective dielectric constant for W-band DMTL's versus center conductor width. The relative dielectric constant of silicon (11.9) and quartz (3.78) are shown for reference.

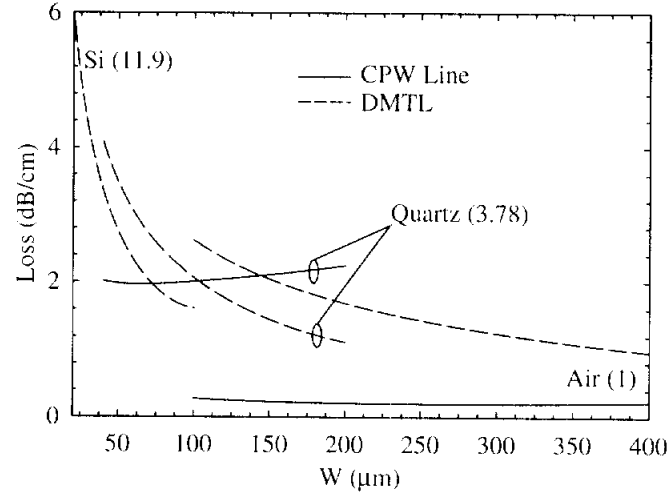


Figure 4.18: Calculated loss at 100 GHz versus center conductor width. The CPW line loss (—) includes radiation loss while the DMTL line neglects radiation but includes loss due to a $0.15 \, \Omega$ bridge resistance at 30 GHz ($0.27 \, \Omega$ at 100 GHz).

Table 4.6: Calculated design of an optimized W-band DMTL phase shifter on quartz.

$W(\mu\text{m})$	100
$S(\mu\text{m})$	300
$C_{bo}(\text{fF})$	19
$s(\mu\text{m})$	110
$f_B(\text{GHz})(L_b = 20 \text{ pH})$	192

Table 4.7: Dimensions for the optimized W-band DMTL phase shifter.

$W(\mu\text{m})$	100
$S(\mu\text{m})$	300
$C_{bo}(\text{fF})$	20.7
$s(\mu\text{m})$	110
$w(\mu\text{m})$	25
$f_B(\text{GHz})(L_b = 20 \text{ pH})$	186

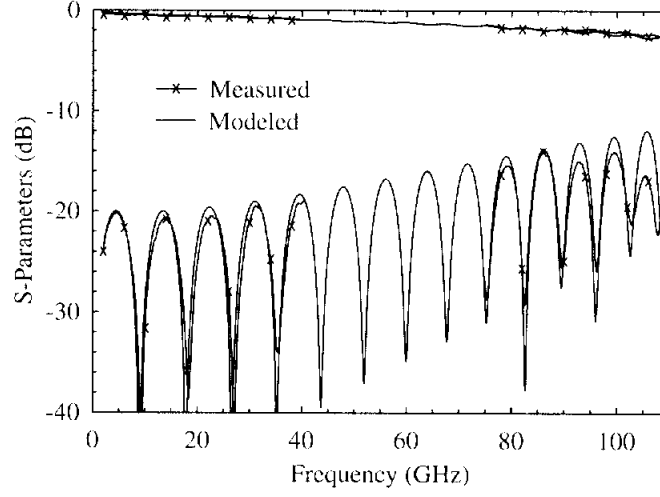
(3.21) and (4.12) the loss for the unloaded CPW lines at 100 GHz, *including* radiation loss, is calculated and shown in Figure 4.18. The unloaded CPW line loss for silicon starts at 6 dB/cm and therefore is not shown. The DMTL loss *neglects* radiation and is calculated at 100 GHz using (3.20) with a bridge resistance, R_b , of 0.15Ω at 30 GHz which increases as \sqrt{f} . The unloaded CPW line loss for quartz is seen to cross over the corresponding DMTL loss at a center conductor width of $105 \mu\text{m}$. Thus, if the DMTL does, in fact, not radiate, then it could exhibit *lower* loss than the unloaded CPW line.

Using equations (4.5)-(4.9), a DMTL on quartz is designed for operation up to 100 GHz with a total CPW width of $300 \mu\text{m}$ and a zero-bias loaded impedance of 48Ω . The resulting design is given in Table 4.6 where the effect of neglecting the bridge inductance has been offset by increasing the Bragg frequency used in (4.5) to 250 GHz. As seen in Table 4.6, the calculated Bragg frequency, assuming a 20 pH bridge inductance, is 192 GHz. Using the static-field solver Maxwell 3-D, a bridge width of $25 \mu\text{m}$ at a height of $1.5 \mu\text{m}$ is found to give a bridge capacitance of 20.7 fF. As shown in Table 4.7, the resulting Bragg frequency, assuming an inductance of 20 pH, is 186 GHz with the Libra circuit simulation showing a Bragg frequency of 189 GHz which is close to the desired Bragg frequency of 200 GHz.

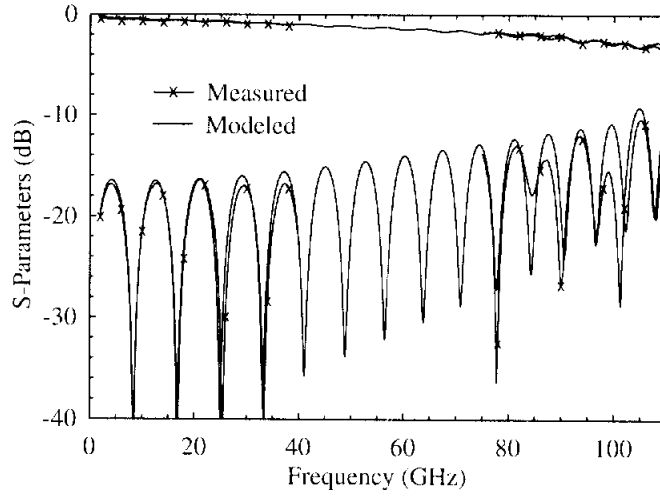
The W-band DMTL is measured using an HP8510C for 2-40 GHz and an HP8510C with W-band millimeter-wave test set for 75-110 GHz. The measured and modeled results

Table 4.8: Circuit model parameters for the W-band DMTL phase shifter.

$C_{bo}(0 \text{ V}) (\text{fF})$	20.7
$C_{bo}(26 \text{ V}) (\text{fF})$	23.7
$L_b (\text{pH})$	22
$A @ 20 \text{ GHz} (\text{dB/cm})$	0.5
$R_b @ 30 \text{ GHz} (\Omega)$	0.15



(a)



(b)

Figure 4.19: Measured (2-40 GHz and 75-110 GHz) and modeled S-parameters at (a) 0 V bias and (b) a maximum bias of 26 V for a W-band DMTL phase shifter. The dimensions are listed in Table 4.7 and the circuit parameters are listed in Table 4.8.

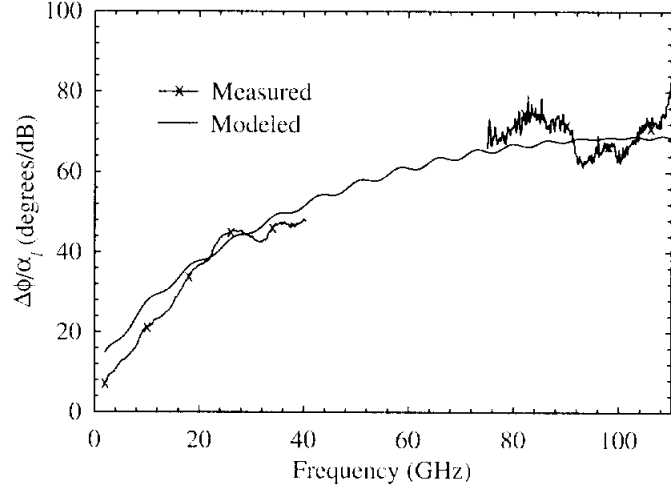


Figure 4.20: Measured and modeled phase shift per dB loss at a maximum bias of 26 V for a W-band DMTL phase shifter. The dimensions are listed in Table 4.7 and the circuit parameters are listed in Table 4.8.

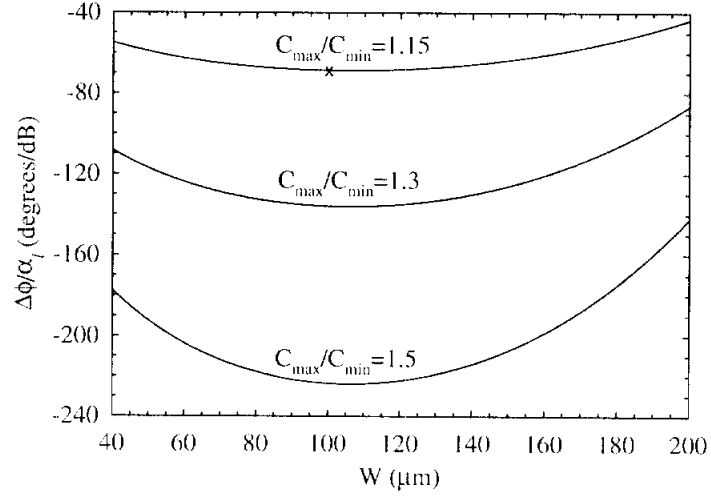


Figure 4.21: Calculated phase shift per dB loss at 100 GHz with a capacitance ratio of 1.15, 1.3, and 1.5. The measured data point is shown for a center conductor width of 100 μm .

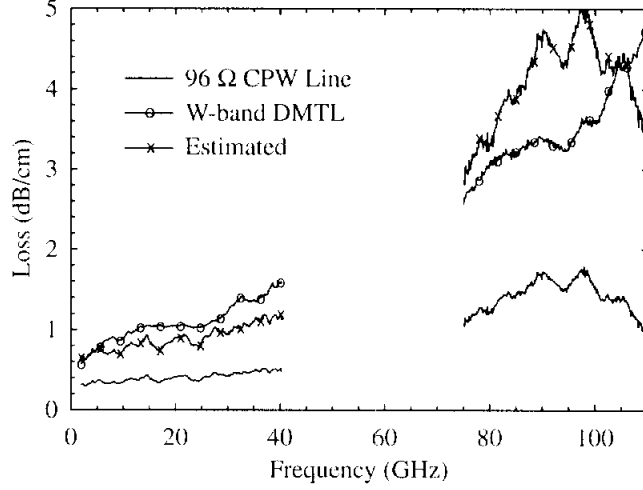


Figure 4.22: Measured loss of a $96\ \Omega$ CPW ($W = 100\ \mu\text{m}$) and DMTL line. The estimated loss, calculated from (3.20) uses the measured CPW loss to calculate R_s . A bridge resistance of $0.15\ \Omega$ at 30 GHz is also included in the estimate.

of a 48 bridge DMTL are shown in Figure 4.19 with the circuit model parameters listed in Table 4.8. The S-parameters are shown for 0 V and the maximum applied bias of 26 V, and show very good agreement with the design. The pull-down voltage of this line is just over 26 V with a corresponding capacitance ratio of 1.15. This capacitance ratio is lower than previously observed which is believed to be due to higher levels of compressive stress within the bridges and increased non-uniformity across the wafer. The measured phase shift per dB loss, seen in Figure 4.20, shows a fairly constant level of nearly $70^\circ/\text{dB}$ from 75-110 GHz, or 5 dB loss for 360° phase shift at W-band. The modeled data shows good agreement using a bridge resistance of $0.15\ \Omega$ at 30 GHz which scales as \sqrt{f} .

Figure 4.21 shows the calculated phase shift per dB loss for capacitance ratios of 1.15, 1.3, and 1.5 at 100 GHz and a bridge resistance of $0.15\ \Omega$ at 30 GHz. The calculated loss from (4.12) is increased by a factor of 1.8 in order for the calculated results to match measurements as discussed in Section 4.2.1. The result of the measured DMTL, with a capacitance ratio of 1.15 is in agreement with the adjusted calculated value. The calculated phase shift per dB loss for capacitance ratios of 1.3 and 1.5 show that the performance of the W-band DMTL can be increased to $-136^\circ/\text{dB}$ and $-224^\circ/\text{dB}$, respectively, which is the equivalent of 2.6 dB and 1.6 dB insertion loss for 360° phase shift at 100 GHz.

The measured loss in dB/cm for the unloaded $96\ \Omega$ CPW line ($S = 300\ \mu\text{m}$ and $W =$

100 μm), and the W-band DMTL are shown in Figure 4.22. It is seen that above 90 GHz, the unloaded line begins to exhibit large variations in loss and no longer increases with frequency. This is indicative of leakage into higher-order modes. However, it is also seen that the DMTL loss steadily increases with frequency. In addition, using the unloaded line loss to find the series resistance, R_s , and assuming a bridge resistance, R_b , of 0.15 Ω at 30 GHz, (3.20) can be used to estimate the loss of the DMTL. This estimate is shown in Figure 4.22 and exhibits much higher loss at W-band than the measured DMTL.

4.4 Stabilized DMTL Phase Shifter

As mentioned in Section 2.3, the MEMS bridges can be stabilized by the inclusion of a series capacitance in the bias path. For the DMTLs, this can be achieved through the use of integrated capacitors in the center conductor at both the input and output of the DMTL as shown in Figure 4.23. If these capacitors are identical, then the DC circuit can be reduced to Figure 4.24 where the total length of the DMTL is $l = n \cdot s + (s - w)$. From this figure it is seen that the second integrated capacitor must be included as part of the fixed capacitance parallel to C_b so that $C_f = l \cdot C_t + C_s$. Using (2.33), it is found that the pull-down voltage of the DMTL will be increased by the factor:

$$\sqrt{\frac{(2C_s + lC_t + nC_{bo})^3}{C_s^2(2C_s + lC_t)}} \quad (4.13)$$

From this equation it is seen that if C_s is very large, then the *minimum* increase in the pull-down voltage is 2. This is a result of the integrated capacitor at both ends of the DMTL being identical.

For the optimized DMTL, presented in Section 4.2, with 16 bridges, the total bridge capacitance is $16 \cdot C_{bo} = 541$ fF and the total transmission line capacitance is $l \cdot C_t = 177$ fF ($l = 3.3$ mm). The pull-down voltage for this line is around 13 V. Since the bias-tees used in the experimental setup have a maximum bias voltage of 40 V, the pull-down voltage should not be increased by more than a factor of 3. Using (4.13) with these values, the series capacitance can be solved for numerically giving a value of $C_s = 1.04$ pF. From (2.31), the new position of the instability is found to be 0.7 μm rather than 0.8 μm for the unstabilized

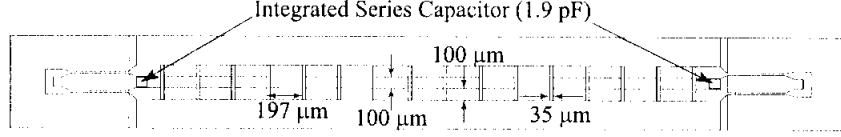


Figure 4.23: Optimized DMTL design with integrated capacitors for stabilization of MEMS bridges.

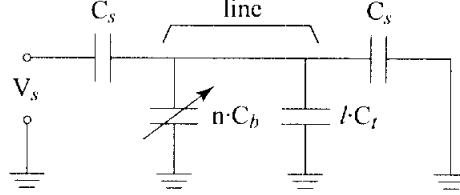
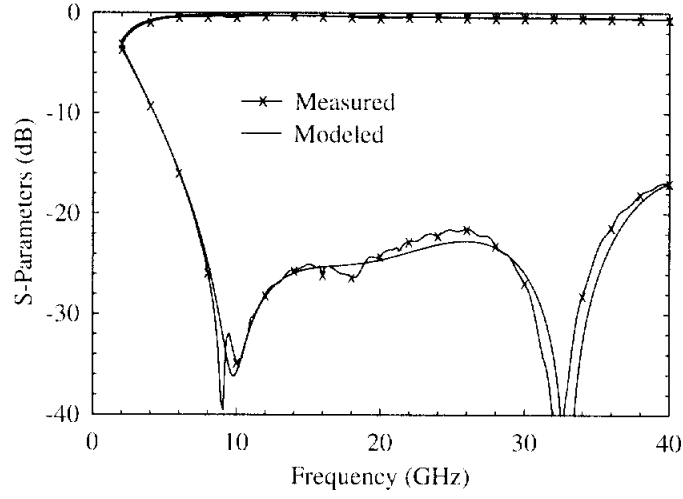


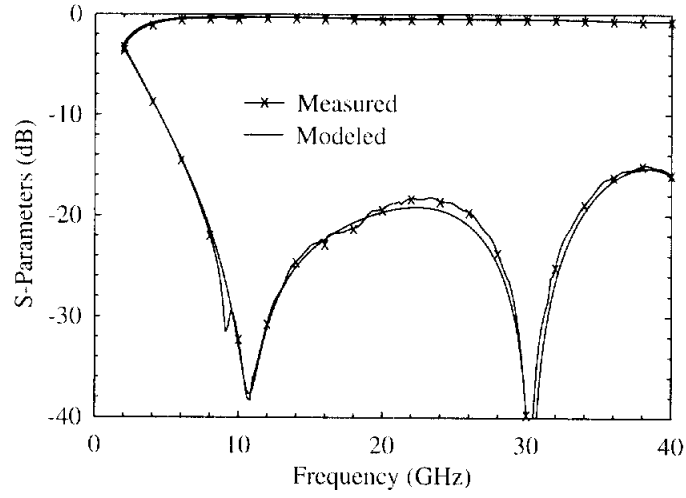
Figure 4.24: Reduced DC circuit of Figure 4.23 with integrated capacitors, C_s , at both ends of the DMTL.

line. This results in a *theoretical* increase in the capacitance ratio from 50% to 70%.

Figure 4.25 shows the measured and modeled results of the optimized 16 bridge DMTL with 1.9 pF integrated series capacitors for both 0 V and 40 V applied bias. The circuit parameters used in the model are given in Table 4.9. It is seen that the change in bridge capacitance is only slightly greater than 12% at 40 V. According to (4.13), the pull-down voltage should have been increased by a factor of 2.5 or to 33 V since the original pull-down voltage of these bridges is 13 V. The pull-down voltage is measured from standard DMTLs fabricated on the same wafer. The reason for the discrepancy between the theoretical pull-down voltage of 33 V and the measured result is believed to be due to charging of the dielectric used in the integrated capacitors. As the dielectric charges up by trapping electrons, the bias voltage becomes partially shielded causing the voltage across the bridges to drop. This effect has been observed in the measurement of these lines in the form of the phase shift of the line decreasing with time at a constant applied bias.



(a)



(b)

Figure 4.25: Optimized 16 bridge DMTL with 1.9 pF integrated series capacitors for stabilization with (a) 0 V and (b) 40 V applied bias.

Table 4.9: Circuit model parameters for the optimal DMTL with integrated capacitors.

$C_{bo}(0 \text{ V})$ (fF)	33
$C_{bo}(40 \text{ V})$ (fF)	37.1
L_b (pH)	24
A @ 20 GHz (dB/cm)	0.52
C_s (pF)	1.9

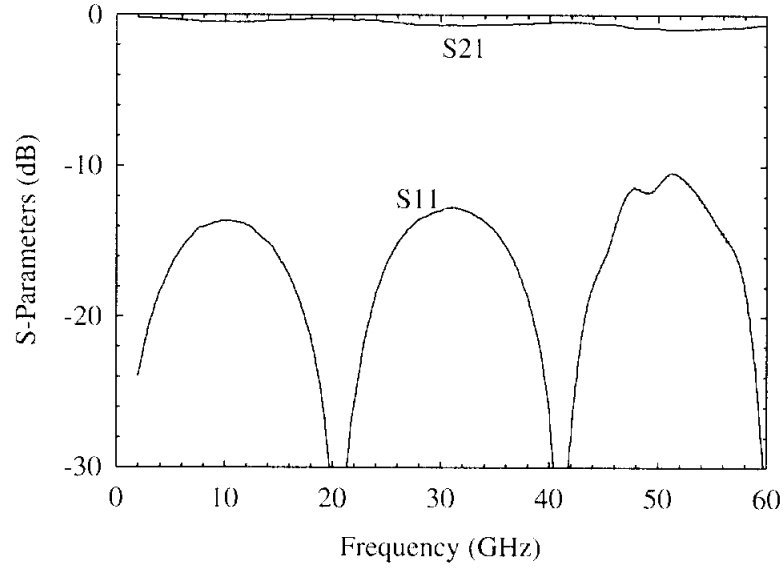
CHAPTER 5

Applications of Distributed MEMS Transmission Lines

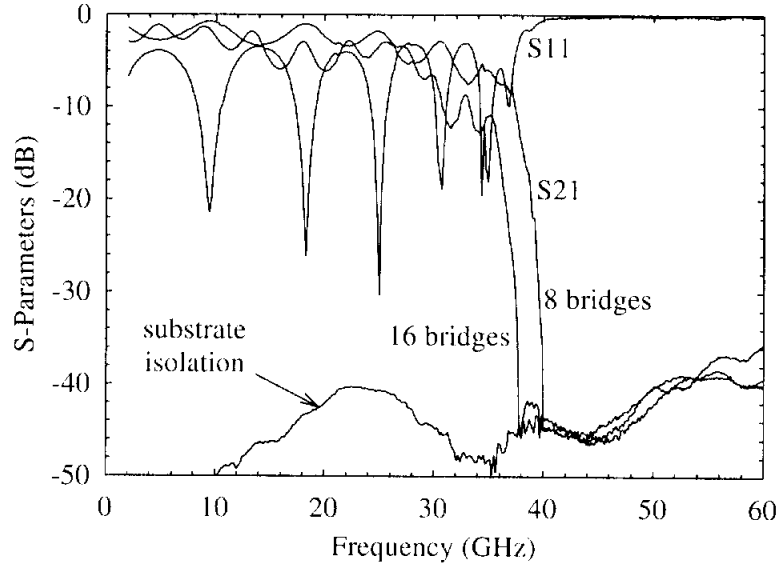
Although the focus of this thesis is on the application of distributed MEMS transmission lines as low-loss millimeter-wave phase shifters, there are a number of other applications in which DMTLs can be useful. Some of the more significant applications are reflective switches, phase modulators, and phase verniers. This chapter presents the results of using DMTLs for these applications, but no attempt is made to achieve the best performance.

5.1 Reflective Switches

Millimeter-wave switches are an essential element in radar and communications systems. Typically, their function is to switch between the transmit and receive modules, or to switch an antenna beam in Rotman lenses or focal-plane designs. Recent results of W-band GaAs PIN diode switches for automotive radars have demonstrated 1.6 dB loss with 20 dB isolation over a 10 GHz bandwidth centered at 80 GHz [5]. Also, hybrid GaAs PIN diode switches with an insertion loss of 0.6 dB and an isolation of -16 dB have been demonstrated at 94 GHz. Switches are also used in instrumentation units, such as vector network analyzers, and require 60-80 dB of isolation. These are typically built using PIN diodes and have an insertion loss of -10 dB from 40-60 GHz [8]. One way to achieve high isolation and low insertion loss is to use the distributed MEMS transmission line as a switch. The wideband distributed MEMS switches measured in this work only operate to 60 GHz; however, it is believed that high performance can also be achieved at W-band frequencies (ie. >60 dB isolation with <2 dB insertion loss).



(a)



(b)

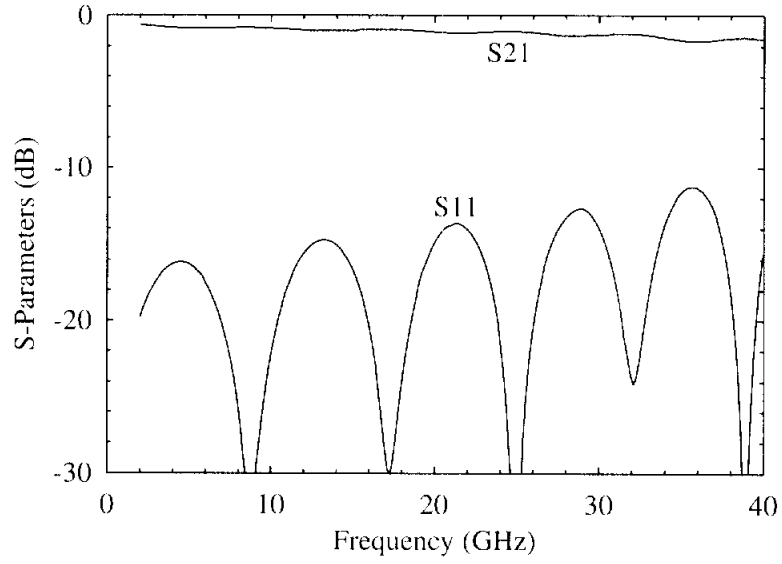
Figure 5.1: Measured results of distributed MEMS switches with 8 and 16 $30\text{-}\mu\text{m}$ wide bridges spaced at $306\text{ }\mu\text{m}$ in the (a) open position (bridge up) and (b) closed position. The S-parameters for the open position are only shown for the case of the 8 bridge design.

5.1.1 Design and Measurements

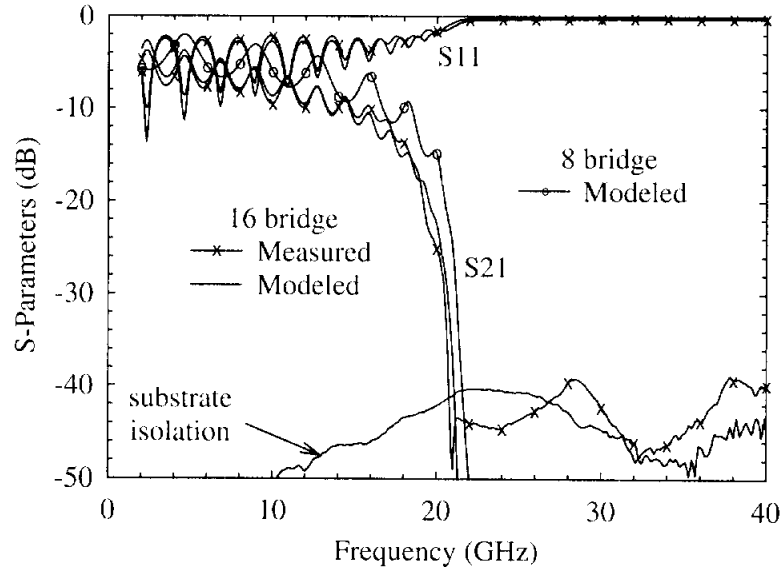
The DMTL switch works by applying a bias voltage greater than the pull-down voltage. This causes the MEMS bridges to be clamped down on top of the center conductor with the Si_xN_y layer separating them. Thus, the MEMS bridge capacitance is greatly increased and an RF short to ground is obtained above a certain frequency. The upper frequency of the distributed switch is determined by the Bragg frequency when the bridges are up. As was noted at the end of Section 3.5, acceptable performance ($S_{11} < -10$ dB) can be obtained up to about half of the Bragg frequency.

Figure 5.1 shows results for DMTLs with 8 and 16 30- μm width bridges spaced at 306 μm (total length = 2.7 mm and 5.2 mm, respectively) resulting in a loaded impedance of 60 Ω . The Bragg frequency for these lines is 129 GHz which limits their upper frequency of operation to approximately 65 GHz. The insertion loss, with the bridges in the up position, is 0.4 to 0.6 dB for 8 bridges, and 0.7 to 1.3 dB for 16 bridges, at 30 to 60 GHz, respectively. In this case, the center conductor thickness is only 5000 Å, and a much better insertion loss could be achieved for a 3 μm thick center conductor. When the bridges are pulled down with a DC voltage of 30 to 35 V ($V_p=23$ V), the cutoff frequency is 40 GHz for the 8 bridge design and 38 GHz for the 16 bridge design, giving an operational bandwidth of 40 to 65 GHz. The switch isolation is limited to around 45 dB by CPW line radiation into the substrate. The substrate isolation is found by measuring the insertion loss between two CPW short circuits separated by 1 mm. Notice that the 8 and 16 bridge designs result in nearly the same response, indicating that it is not necessary to design the distributed switch with more than 8 bridges.

Figure 5.2 shows results for a DMTL with 16 60- μm wide bridges spaced at 400 μm (total length = 6.7 mm) resulting in an impedance of 43 Ω . The Bragg frequency is 69 GHz, which limits the upper frequency of operation to approximately 35 GHz. However, the measured S-parameters indicate that the switch can be used to 40 GHz. The insertion loss, with the bridges in the up position, is 0.9 to 1.4 dB for 20 to 40 GHz. Again, the center conductor thickness is only 5000 Å, and a much better insertion loss could be achieved for a 3 μm thick center conductor. When the bridges are pulled down with a voltage of 15 to 20 V



(a)



(b)

Figure 5.2: Measured and modeled results for a distributed MEMS switch with 16 $60\text{-}\mu\text{m}$ wide bridges spaced at $400\text{ }\mu\text{m}$ in the (a) open position (bridge up) and (b) closed position.

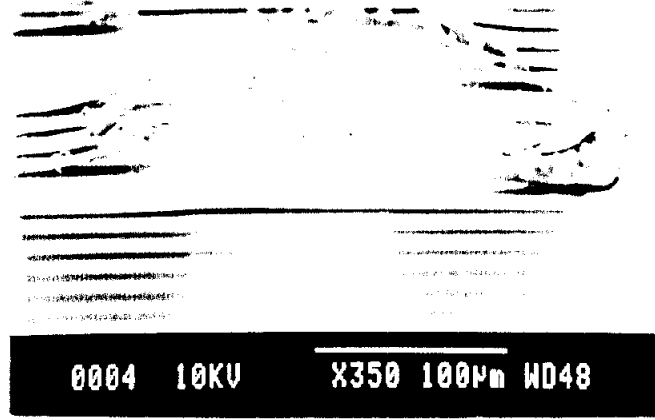


Figure 5.3: SEM image of the remains of a DMTL after the breakdown voltage of the Si_xN_y was exceeded.

($V_p=6$ V), the cutoff frequency is 21 GHz, which results in an operational bandwidth of 21 to 40 GHz.

The closed switch results shown in Figure 5.2a are successfully modeled using the Libra circuit model discussed in Section 3.4. The pulled-down bridge capacitance and the bridge inductance are 0.9 pF and 12 pH, respectively. The capacitance ratio is $0.9/0.075=12$. It is seen that excellent isolation is achieved even for such a low capacitance ratio due to the distributed approach of the switch. The transmission line attenuation needed to fit the data is 1.1 dB/cm at 20 GHz. This is double the value used previously in Chapter 4 (0.55 dB/cm at 20 GHz) and is believed to be due to the additional losses of the large capacitors formed by the MEMS bridge, 1000 Å of Si_xN_y , and the CPW center conductor. Using this model, the performance of a switch with 8 bridges was simulated with the results also shown in Figure 5.2a. Obviously, it is more efficient to use 8 bridges since this design will result in half the insertion loss (0.5-0.7 dB for 20 to 40 GHz and much less if $t = 3 \mu\text{m}$) for the same “sharp” response and operating bandwidth. The switch isolation is again limited by the CPW line substrate radiation.

It should be noted that the closed switch in Figure 5.1 could not be modeled successfully because a high enough bias voltage could not be applied to these switches in order to obtain a uniform down capacitance in every bridge. The bias voltage is limited by the breakdown

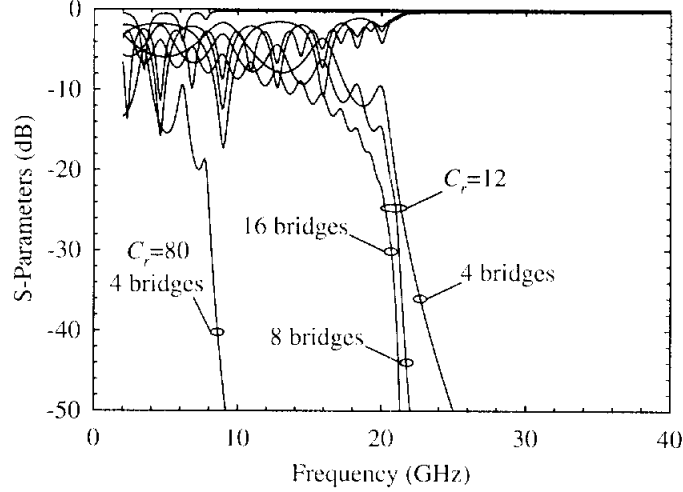


Figure 5.4: Variation of lower cutoff frequency with different number of sections used in the distributed switch design.

voltage of the Si_xN_y which is approximately 35 V for a 1000 Å thick layer. Figure 5.3 is an SEM image of a DMTL after the dielectric breakdown voltage was exceeded. The bridges and center conductor metals are not thick enough to handle any appreciable current and simply melt, causing catastrophic failure of the device. The silicon nitride thickness was later increased to 2000 Å in order to avoid dielectric breakdown and to avoid pin-holes in the MIM capacitors used in Section 4.4. The closed switch in Figure 5.2a has a pull-down voltage of 6 V; so an applied bias of 20 V is sufficient to obtain uniform capacitance values along the transmission line.

Figure 5.4 shows the variation in the cutoff frequency between distributed switch designs with 4, 8, and 16 bridges. As can be seen, the 4, 8, and 16 bridge designs give nearly the same cutoff frequency. The primary limitation in the current distributed MEMS switch is the capacitance ratio. If a capacitance ratio of 80-100 is used, instead of a capacitance ratio of 12 achieved with these switches, then the corner frequency will be pushed down to below 10 GHz as seen in Figure 5.4, and the bandwidth of the distributed switch will increase to around 50 GHz (10-65 GHz). The distributed switches are designed by choosing either the upper or lower frequency cutoff and then designing the spacing and bridge capacitance to achieve the desired Bragg frequency in either the up state, for the upper cutoff frequency, or the down state, for the lower cutoff frequency.

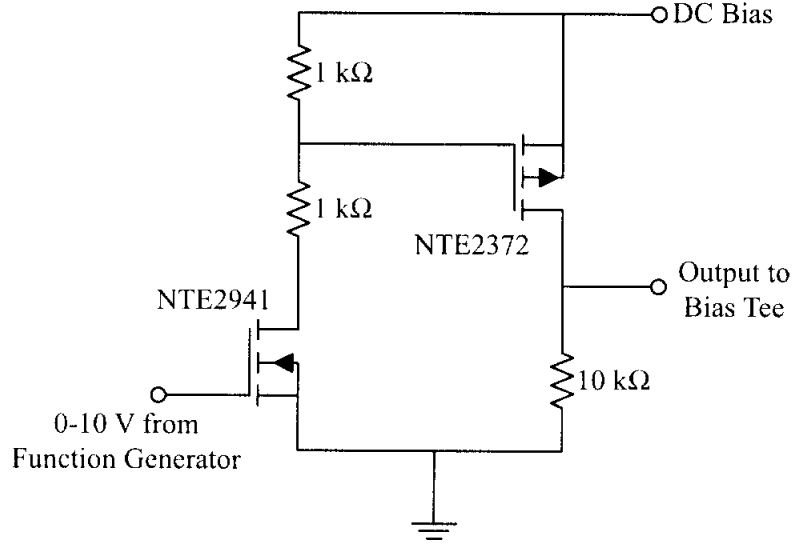


Figure 5.5: Driver circuit used to provide a 0 to 33 V step to the bias line of the DMTL.

5.1.2 Switching Speed

The switching speed is measured by applying a step voltage on the bias of the DMTL and measuring the change in the power transmitted through the DMTL using a diode detector. The experimental setup is shown in Figure 5.6.

The RF frequency generator is set to 35 GHz with 10 dBm output power for the switching speed tests done in this work. The RF power at the output of the DMTL is measured using a diode detector with waveguide transition. The bias is supplied by a driver circuit, shown in Figure 5.5, in order to achieve a 0 to 30 V step function. The function generator is only able to deliver a 0 to 15 V step function which is insufficient for devices with a 20 V pull-down voltage. The bias-tees have a maximum bias voltage rating of 40 V, therefore, the bias is limited to 33 V due to inductive peaking which swings the step voltage up to 40 V during switching. A step from 0 to 10 V on the gate of the N-channel MOSFET causes the gate voltage of the P-channel MOSFET to drop from the DC bias voltage to approximately half the DC bias voltage and consequently turning the PMOS device on. This causes the output of the driver circuit to step from 0 V to the DC bias voltage minus a 2 V source to drain voltage drop across the P-channel MOSFET. The driver circuit is charging a large capacitive load and therefore the current path must be low resistance in order to obtain a fast rise time. The on resistance of the P-channel MOSFET is around 1.5Ω , as per the

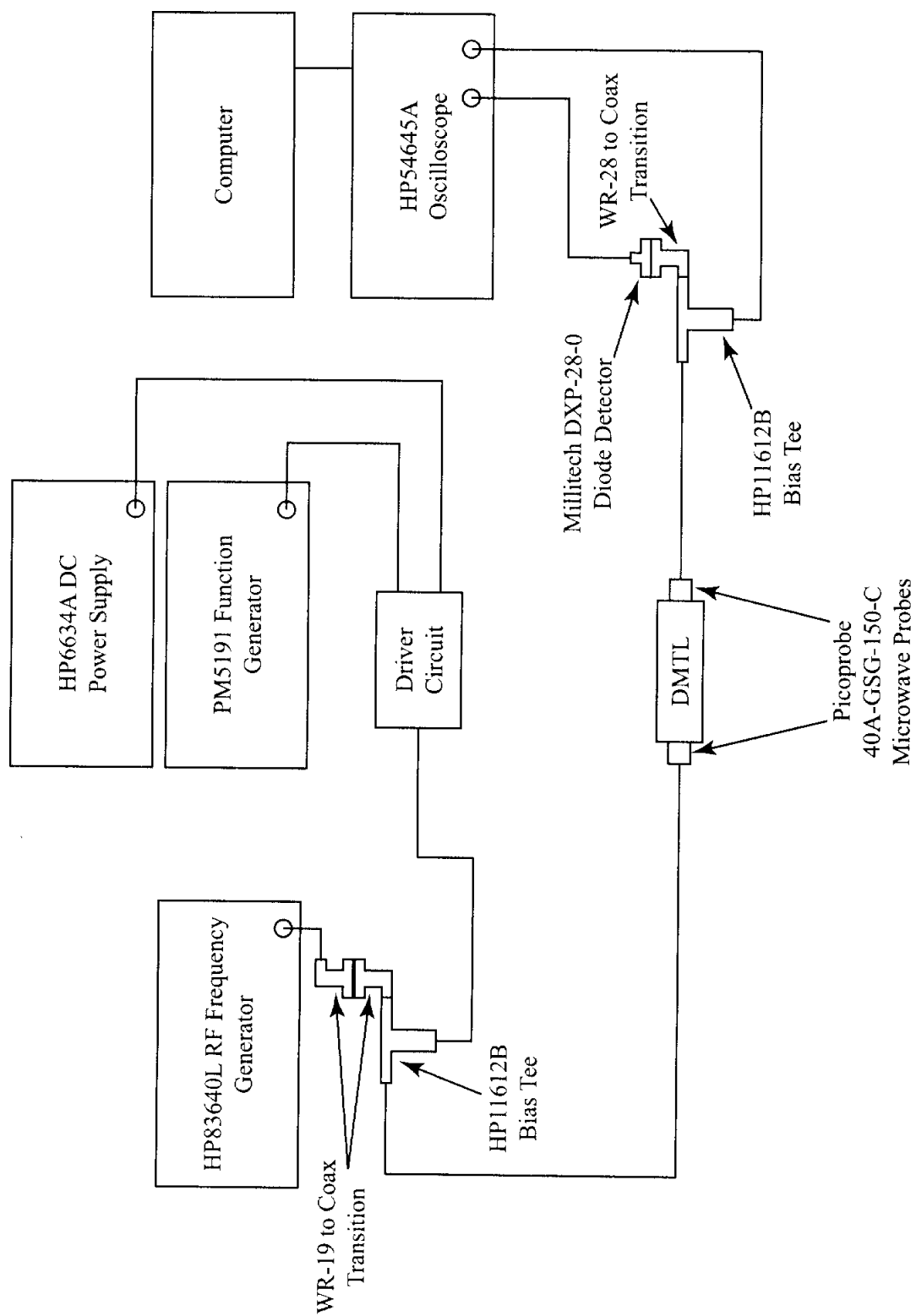


Figure 5.6: Experimental setup of the switching speed measurement.

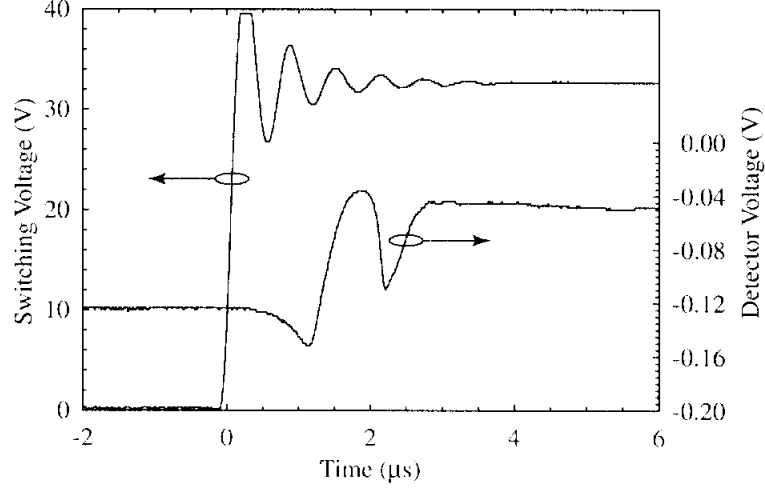
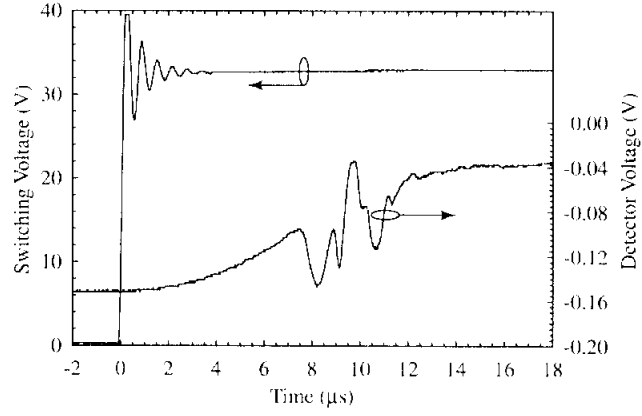


Figure 5.7: Switching speed measurement of a 16 bridge DMTL with a bridge width and spacing of $25\text{ }\mu\text{m}$ and $110\text{ }\mu\text{m}$, respectively. The bridge height is approximately $0.9\text{ }\mu\text{m}$ and the pull-down voltage is 6 V .

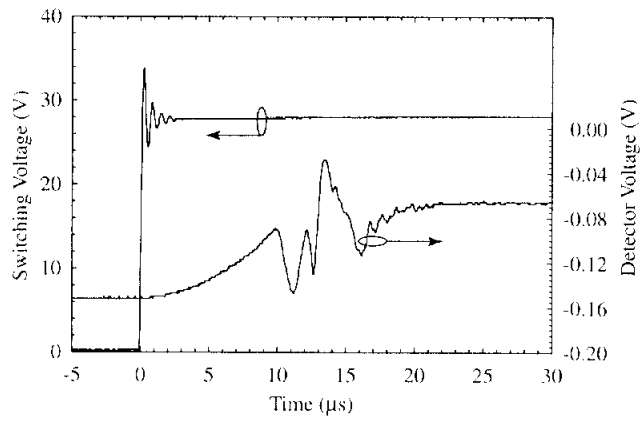
manufacturer's data sheet, resulting in a measured rise time of 0.2 V/ns or 150 ns for a 30 V step with all cables attached (capacitive load taken into account). This is acceptable since the response time of the bridges is expected to be on the order of a few microseconds. When the voltage at the gate of the N-channel MOSFET drops back to 0 V the output also drops to 0 V , however, the capacitive load is discharged through the $10\text{ k}\Omega$ resistor and thus the fall time is much slower ($\sim 700\text{ }\mu\text{s}$). Therefore, only the pull-down switching time is measured with this setup.

The back-to-back waveguide-to-coax transitions at the output of the RF generator act as a low frequency block, and are needed to prevent modulation of the RF signal by leakage of the step voltage through the bias-tee as well as possible damage to the source. The oscilloscope is triggered using the step voltage, and records the response of the detector diode.

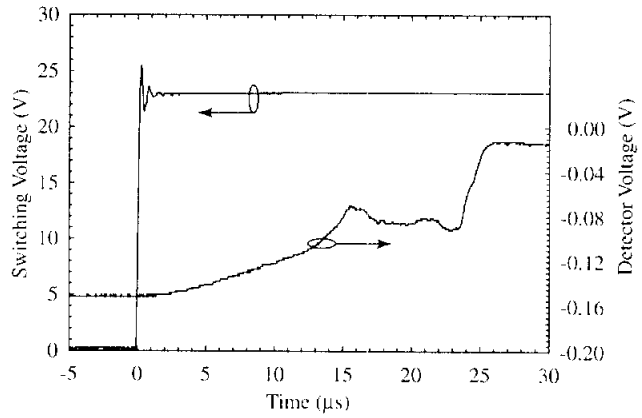
The first DMTL measured has 16 $25\text{-}\mu\text{m}$ wide bridges spaced at $110\text{ }\mu\text{m}$. The bridge height was intended to be $1.5\text{ }\mu\text{m}$, however this particular wafer had higher compressive stress in the bridges than normal resulting in the bridges being buckled down to approximately $0.9\text{ }\mu\text{m}$. Figure 5.7 shows a measured switching time of $2.7\text{ }\mu\text{s}$ for this DMTL with an applied step voltage of 33 V . The switching time is measured from $0\text{ }\mu\text{s}$, where the step voltage hits 5 V , to the time at which the detector voltage reaches 95% of its final value.



(a)



(b)



(c)

Figure 5.8: Switching speed measurements of a 16 bridge DMTL with a bridge width and spacing of $25\ \mu\text{m}$ and $110\ \mu\text{m}$, respectively. The bridge height is $1.5\ \mu\text{m}$ and the pull-down voltage is $21\ \text{V}$.

Table 5.1: Parameters of the gold bridge used
in the calculation of Figure 5.9.

w	25 μm	W	100 μm
l	300 μm	Q	2.6
t	2.2 μm	f_o	27.6 kHz
g_o	1.5 μm	V_p	21.3 V

The DMTL measured in Figure 5.7 never recovered from being switched and so no further measurements could be made on this device.

Figure 5.8 shows the switching speed measurements of the same DMTL design on a wafer with the correct bridge height of 1.5 μm . The pull-down voltage for these bridges is 21 V. In this case, the DMTL returns to its initial state after the bias is released and so multiple measurements were made. As can be seen, the switching speed increases from 13.6 μs to 19.7 μs and then to 25.1 μs as the DC actuation voltage is decreased from 33 V to 28 V and then to 23 V. The slower switching speed is due to the fact that the bridges are farther away (1.5 μm instead of 0.9 μm), and also because the *force* able to be applied to the bridges is less. As seen in Figures 5.7 and 5.8, there are voltage transients between the switching voltage being applied at $t = 0 \mu\text{s}$ and the final value of the detector voltage. These are most likely due to the dynamics of 16 bridges being actuated simultaneously and the differences in how each bridge moves. Some of the transients may be due to bouncing of the bridge off of the dielectric layer. Another possibility is parametric effects of the time changing capacitance causing some modulation of the RF power level.

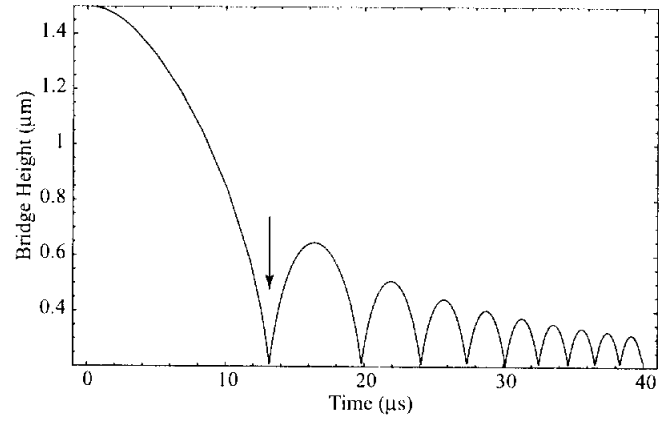
The switching speed can be modeled using the differential equation of motion given by (2.34) where the external force is electrostatic:

$$m \frac{d^2x}{dt^2} + b \frac{dx}{dt} + kx = -\frac{1}{2} \frac{\epsilon_o W w V^2}{g^2} \quad (5.1)$$

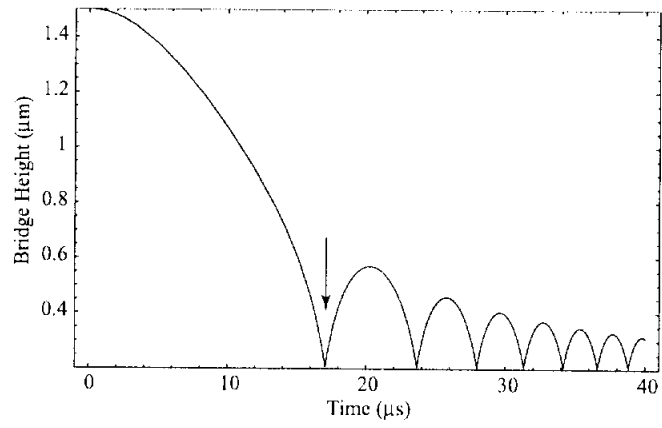
where the damping coefficient is given by $b = k/(\omega_o Q)$. Using Mathematica¹, this differential equation can be solved numerically for varying DC actuation voltage conditions.

Figure 5.9 shows the numerical solution of (5.1) in which a contact force has been added to simulate the effect of hitting the silicon nitride [6]. The parameters of the contact force are chosen to result in stable numerical solutions and do not reflect any realistic modeling

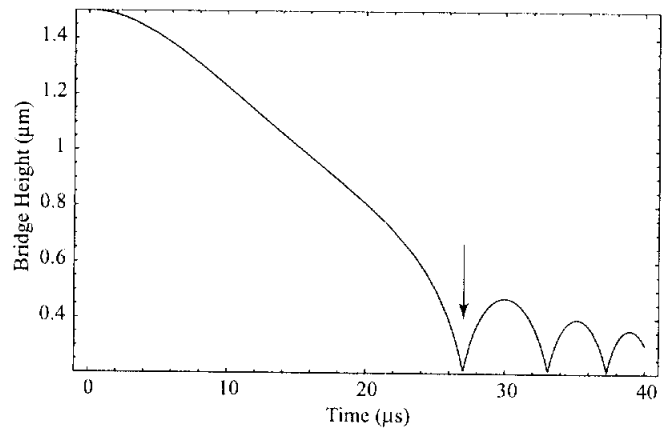
¹Wolfram Research, Inc. 100 Trade Center Drive Champaign, IL 61820, USA



(a)



(b)



(c)

Figure 5.9: Numerical solution of the switching speed for step voltages of (a) 33 V, (b) 28 V, and (c) 23 V for a gold bridge with parameters given in Table 5.1.

of the silicon nitride surface. The parameters of the gold bridge are given in Table 5.1. It should be noted that the spring constant has been reduced from 13.9 N/m (calculated using the bridge geometry) to 9.6 N/m, in order to account for the compressive stress within the beam, such that the calculated pull-down voltage matches the measured value. The quality factor is dominated by squeeze-film damping and is given by [23]:

$$Q^{-1} = \frac{\mu (wl/2)^2}{\sqrt{E\rho} t^2 g^3} \quad (5.2)$$

where μ is the viscosity of air. The solution has been carried out for step voltages of 33, 28, and 23 V with, as seen in Figure 5.9, switching speeds of 13, 17, and 27 μ s, respectively. The bounces seen after the initial contact of the bridge are due to the contact force parameters and do not simulate the actual dynamics of the switch coming in contact with the silicon nitride. The switching speed was also calculated for a step voltage of 50 V with a resulting switching speed of 7.8 μ s. Thus, in order to achieve a fast switching time, the actuation voltage needs to be well above the pull-down voltage.

A closed form expression for the switching speed can be found by approximating the electrostatic force as being a constant magnitude of:

$$F = \frac{\epsilon_o W w V^2}{2g_o^2} \quad (5.3)$$

and ignoring the damping coefficient. Then (5.1) reduces to:

$$m \frac{d^2 x}{dt^2} + kx = F \quad (5.4)$$

The switching time can be solved assuming the bridge is at rest and a step voltage from 0 to V volts is applied at time $t = 0$. This results in:

$$t_s = \sin^{-1} \left(\frac{2mg_o^3}{\epsilon_o W w V^2} \right) \quad (5.5)$$

where t_s is the switching time and m is the bridge mass.

A comparison of the measured, numerical model, and closed form model switching speeds is shown in Table 5.2. It is seen that the numerical model gives a very good approximation to the switching speed at each voltage level. The closed form model, in this case, overestimates the switching speed slightly. However, this is for the case in which the Q of the bridge is 2.6.

Table 5.2: Measured and modeled switching speed in μs ($Q = 2.3$).

Voltage	Measured	Numerical Model	Closed Form Model
50 V	-	7.8	6.7
33 V	12.1	13	15.5
28 V	18.6	17	21.5
23 V	25.5	27	31.8

Table 5.3: Calculated switching speeds, in μs , from the numerical solution for varying Q values.

Voltage	$Q=2.3$	$Q=1$	$Q=0.2$
50 V	7.8	8.7	16.6
33 V	13	15.9	42
28 V	17	22	70

Keeping all other parameters constant, the numerical solution will change if the Q is varied, however the closed form solution, which ignores the damping coefficient, will stay constant. Table 5.3 shows that for quality factors below 1, the closed form solution begins to greatly underestimate the numerical solution. As seen from (5.2), the Q will vary with changes in the air viscosity (or a change in air pressure) and the density of the bridge material.

5.2 Phase Modulators

In Chapter 4 it was demonstrated that the DMTL could be used as a phase shifter capable of achieving more phase shift simply by increasing the length of the line. Thus, a binary phase shift keying (BPSK) modulator can be designed by using a line with 180° phase shift. The DMTL provides some unique characteristics for a phase modulator in that it requires very little drive power compared to most semiconductor based phase shifters. However, it is limited in how fast it can modulate due to the mechanical motion of the bridge.

Measurements

Using the optimized design of Section 4.2.2, a DMTL with 96 bridges was designed to give over 180° phase shift at 35 GHz and above. The measured DMTL, shown in Figures 5.10 and 5.11, has a bridge height of approximately $0.9 \mu m$ rather than the intended $1.2 \mu m$ due

to high residual stress within the bridges. This results in a much lower pull-down voltage of 6 V rather than 13 V seen in Section 4.2.2. However, as can be seen from the S-parameter and phase shift measurements, this line is still useful for demonstrating a BPSK modulator.

The experimental setup for the measurement of the DMTL as a BPSK modulator is shown in Figure 5.12. The modulating signal is a 1 kHz square wave with a magnitude of 6 V and DC bias of 3 V. This signal is coupled onto the DMTL center conductor using a bias tee. It is important to note the use of a back-to-back waveguide to coax transition between the bias tee and the RF frequency generator. Although the bias tee will prevent DC from passing through to the frequency generator it will not completely block the modulation signal from reaching the frequency generator. This is potentially a problem because the modulation signal could cause unwanted modulation of the RF signal before it enters the DMTL. With the back-to-back transition in place, the modulation signal is far below cutoff (31.36 GHz for WR-19), and thus is not able to reach the frequency generator. The RF is set to 35 GHz and the IF is chosen to be 10 kHz. Thus, the local oscillator signal to the harmonic mixer is set to 17.5 GHz minus 5 kHz.

The measured IF signal is shown in Figure 5.13, from which the phase changes can be seen at 0.37 msec and 0.87 msec. Since the modulating signal is a 1 kHz square wave, phase changes occur at twice that rate, or every 0.5 ms as seen in Figure 5.13. The change in amplitude for the different phase states is very small, and is most likely due to a combination of changes in the insertion loss and return loss of the DMTL when the bias is applied.

The RF spectrum of the modulated signal is measured by taking the output of the DMTL through another back-to-back waveguide to coax transition and into a spectrum analyzer. Figure 5.14 shows the measured spectrum with an RF of 35 GHz and a 1 kHz square wave modulation. The carrier at the output of the DMTL, with no modulation, was measured to be -14.7 dBm. As can be seen from the measured spectrum, the carrier is suppressed by 25 dB as expected for a BPSK spectrum. The measured power levels of the modulation spectrum, in dB below the carrier (dBc), are shown in Table 5.4.

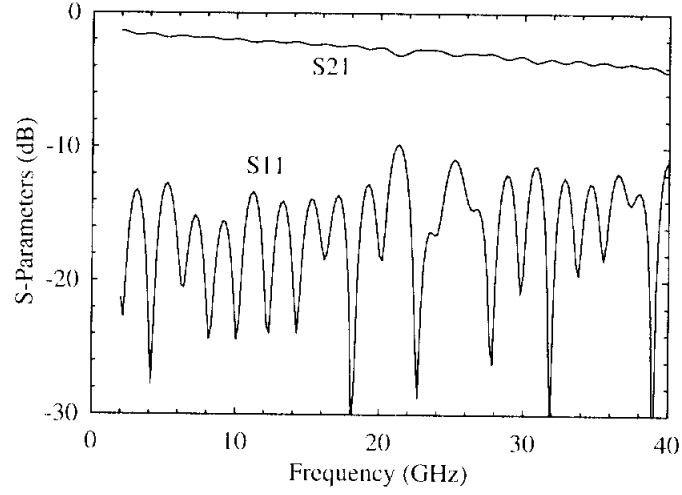


Figure 5.10: Measured S-parameters of the 96 bridge DMTL at a maximum bias voltage of 6 V. The DMTL is based on the optimized design of Section 4.2.2, although the bridge height is approximately $0.9\ \mu\text{m}$, rather than $1.2\ \mu\text{m}$, due to excessive residual stress within the bridges.

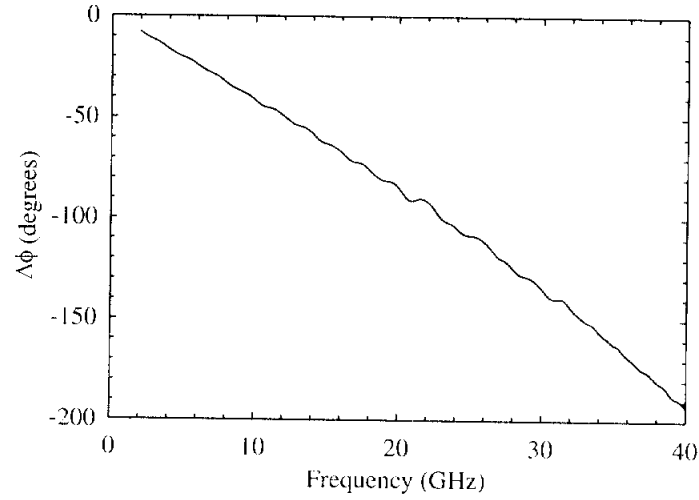


Figure 5.11: Measured phase shift of the 96 bridge DMTL based on the optimized design of Section 4.2.2.

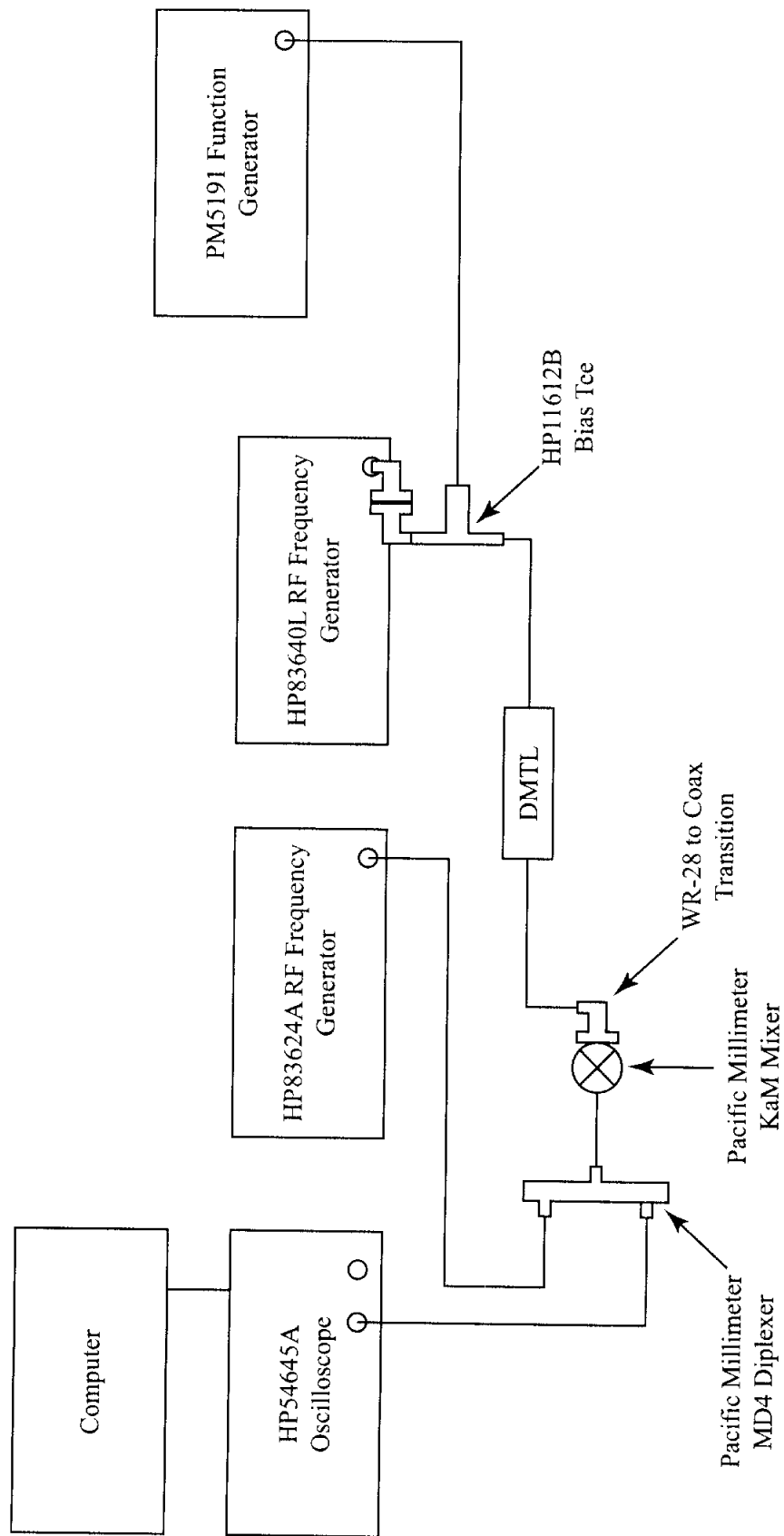


Figure 5.12: Experimental setup for the heterodyne measurement of the DMTL as a BPSK modulator.

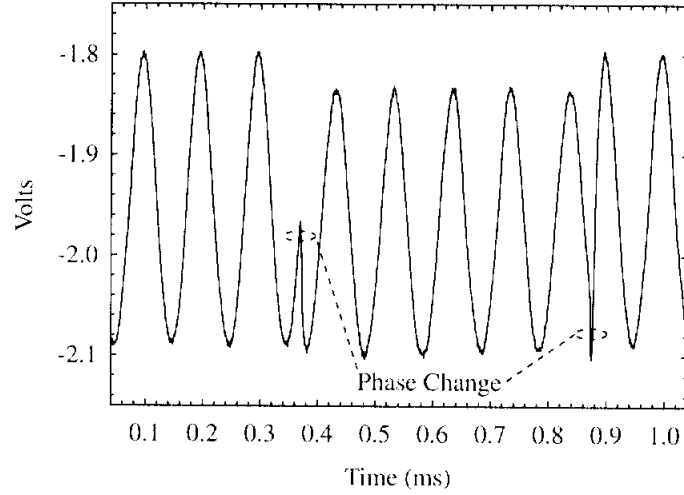


Figure 5.13: Measured output of the DMTL as a BPSK modulator with a modulation rate of 1 kHz. The RF is at 35 GHz and is mixed down to 10 kHz as shown here. Phase changes can be observed at 0.32 μ s and 0.87 μ s.

Modeling

The theoretical spectrum of a phase modulated signal can be broken into Fourier components, assuming a periodic modulation signal, given by [11]:

$$c_n = f_m \int_0^{T_m} e^{jm_p(t) - jn\omega_m t} dt \quad (5.6)$$

where f_m is the modulation rate, $T_m = 1/f_m$, n is the harmonic number, and $m_p(t)$ is the modulation signal. BPSK modulation is phase modulation with a square wave modulation signal with a phase deviation of 180° . Evaluating (5.6) under these conditions, the theoretical spectrum of a BPSK signal is found. The calculated values are given in Table 5.4 from which it is seen that the measured values given in Table 5.4 match reasonably well.

Using the differential equation of motion given by (5.1), a numerical solution for the bridge movement with time can be found as shown in Figure 5.15. The parameters of the bridge used in this calculation are given in Table 5.5 where the spring constant has been reduced from 19.5 N/m to 5.0 N/m to account for the compressive stress within the bridge. The reason the Q is lower than that shown in Table 5.1 is that the bridge height is 0.9 μ m rather than 1.5 μ m and also because the bridge width is 35 μ m rather than 25 μ m. From the solution for the bridge height versus time, (4.11) can be used to determine the phase which is the modulation signal, $m_p(t)$, used in (5.6). As can be seen in Figure 5.15, the rise time of

Table 5.4: Measured, theoretical, and modeled RF spectrum of the BPSK signal in dBc.

Harmonic	f_{-9}	f_{-7}	f_{-5}	f_{-3}	f_{-1}	f_0	f_1	f_3	f_5	f_7	f_9
Measured (dBc)	-23.5	-22.8	-20.3	-13	-3	-25	-5	-14.8	-17.8	-20.8	-24.3
Theoretical (dBc)	-23	-20.8	-17.9	-13.5	-3.9	$-\infty$	-3.9	-13.5	-17.9	-20.8	-23
Modeled (dBc)	-27.4	-23.4	-18.8	-13	-3.1	-26	-5.1	-15.1	-19.4	-22.1	-24.2

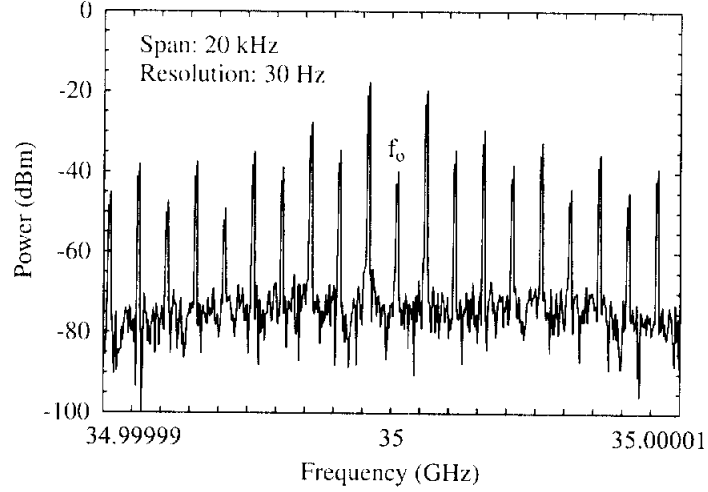


Figure 5.14: Measured RF spectrum of the DMTL as a BPSK modulator with a modulation rate of 1 kHz. The carrier, with no modulation, was measured to be -14.7 dBm.

the bridge is faster than the fall time. This is the source of the difference in the magnitudes between the positive and negative harmonics of the measured spectrum (Table 5.4). The calculated harmonic levels from the numerical model are also shown in Table 5.4 which demonstrate nearly the same imbalance in the positive and negative harmonic levels.

Since the resonant frequency of the bridges in this DMTL is only 16.8 kHz, the modulation frequency could not be pushed much above 1 kHz without excessive distortion of the BPSK signal. Figure 5.16 shows the numerical solution for this same DMTL driven with a 10 kHz modulation signal with an amplitude of 6 V. It is seen that the bridge can not even reach 0.7 μm before the actuation voltage returns to 0 V. However, if the bridge

Table 5.5: Parameters of the gold bridge used in the calculation of Figure 5.15.

w	35 μm	W	100 μm
l	300 μm	Q	0.55
t	2.2 μm	f_o	16.8 kHz
g_o	0.9 μm	V_p	6.1 V

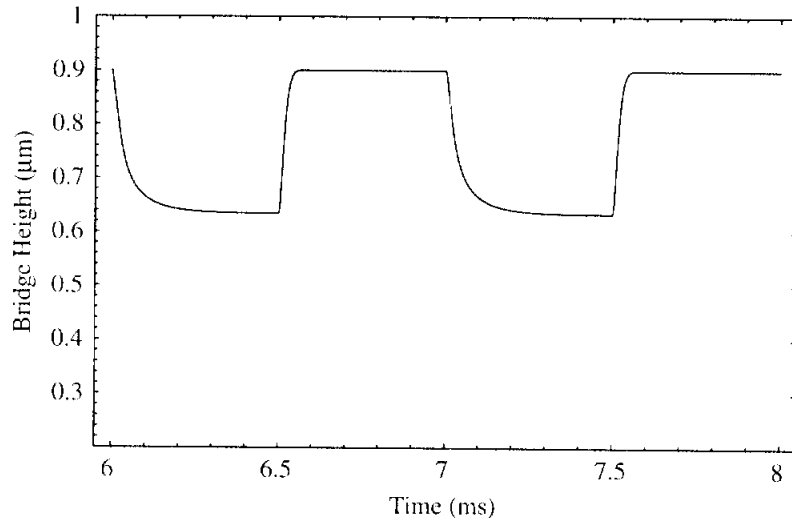


Figure 5.15: Numerical simulation of bridge movement under 6 V 1 kHz square wave modulation.

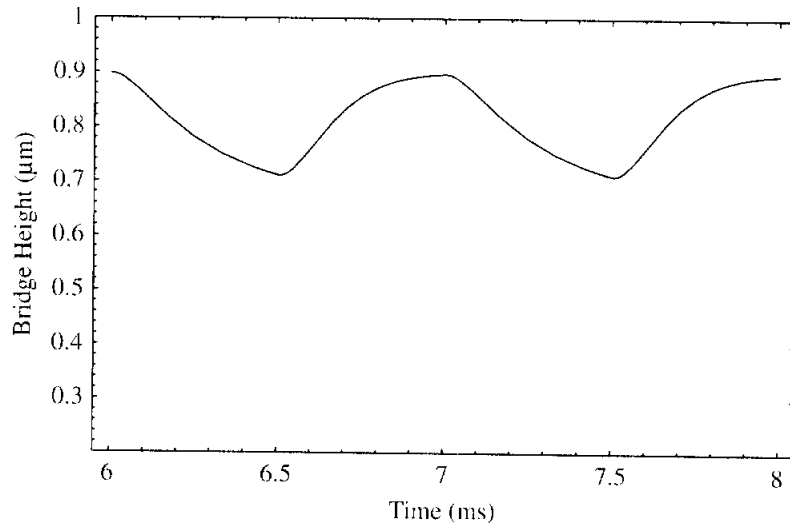


Figure 5.16: Numerical simulation of bridge movement under 6 V 10 kHz square wave modulation.

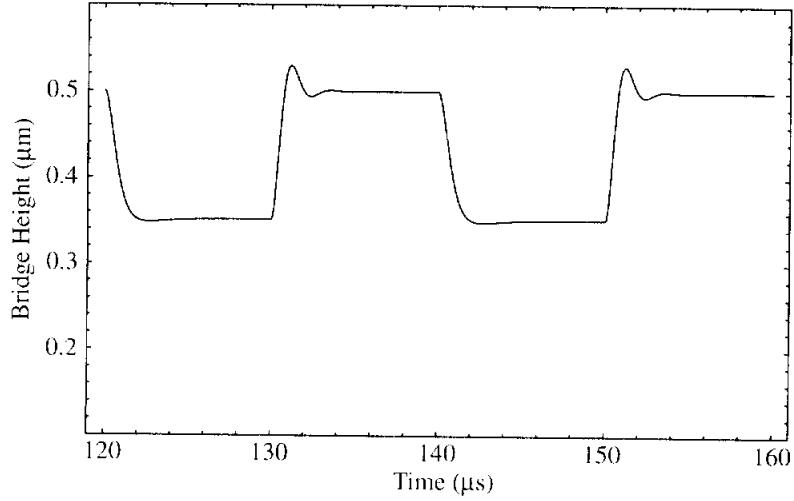


Figure 5.17: Numerical simulation of bridge movement under 60 V 50 kHz square wave modulation for a bridge with dimensions listed in Table 5.17.

Table 5.6: Parameters of the gold bridge used in the calculation of Figure 5.17.

w	35 μm	W	75 μm
l	100 μm	Q	1.1
t	3.5 μm	f_o	476 kHz
g_o	0.5 μm	V_p	60.4 V

design is altered to achieve a higher resonant frequency, the usable modulation rate can be greatly increased. Such a design using a gold bridge is given in Table 5.6 with the simulated bridge movement shown in Figure 5.17. The spring constant of this bridge is 2117 N/m due to a much shorter length and larger thickness. The residual stress for the design is set to 0 MPa. With such a large spring constant, the bridge height had to be reduced to 0.5 μm and the resulting pull-down voltage is still 60 V. Thus, this design could be used as a BPSK modulator capable of delivering 100 kps data rate.

Drive Power

The average drive power required by the DMTL can be found from determining the total energy, required to move the bridges and to charge the capacitance, and multiplying it by the frequency of modulation. The energy required to charge the capacitance of the line and bridges is given by:

$$U_C = \frac{1}{2} C_{tot} V^2 \quad (5.7)$$

where C_{tot} includes the bridge capacitance in the down state as well as the transmission line capacitance and is given by $C_{tot} \approx n \cdot C_r \cdot C_{bo} + n \cdot s \cdot C_t$. The energy required to move one bridge is found by integrating the force needed over the distance moved:

$$U_b = \int_{2g_o/3}^{g_o} \frac{\epsilon_o W w V^2}{2g^2} dg = \frac{\epsilon_o W w V^2}{4g_o} = \frac{1}{4} C_{bo} V^2 \quad (5.8)$$

where the maximum possible distance has been used to provide an upper bound on the energy. The total required power is therefore:

$$P = n f V^2 \left(\frac{1}{4} C_{bo} + \frac{1}{2} C_r C_{bo} + s C_t \right) \quad (5.9)$$

where f is the frequency of modulation.

For the 96 bridge DMTL with a bridge height of 0.9 μm , bridge spacing of 197 μm , and transmission line capacitance of 53 pF/m, the zero bias bridge capacitance is approximately 47 fF based on the low frequency reflection coefficient. Assuming a capacitance ratio of 1.2, the total capacitance to be charged is $96(1.2 \times 47 + 197 \times 0.053) \cdot 10^{-15} = 6.4$ pF. Thus, the total energy required is given by:

$$\left(\frac{4.5 \cdot 10^{-12}}{4} + \frac{6.4 \cdot 10^{-12}}{2} \right) \cdot 36 = 0.156 \text{ nJ} \quad (5.10)$$

With a 1 kHz modulation rate, the average drive power is $\sim 0.16 \mu\text{W}$, which is extremely low. If the actuation voltage needed is increased to 25 V, the average drive power increases to 2.7 μW for a 1 kHz modulation rate and 27 μW for a 10 kHz modulation rate. This is still a much lower drive power than semiconductor device phase modulators exhibit, which is typically on the order of a few milliwatts or more [27].

If the high frequency design given in Table 5.6 is used, which has a calculated parallel-plate zero-bias capacitance of 46 fF, with the same spacing and CPW line dimensions, the total energy becomes:

$$\left(\frac{4.4 \cdot 10^{-12}}{4} + \frac{6.3 \cdot 10^{-12}}{2} \right) \cdot 60^2 = 15.3 \text{ nJ} \quad (5.11)$$

which is two orders of magnitude larger due to the 60 V actuation voltage required to modulate the bridges. With the 50 kHz modulation rate, the average drive power becomes 0.77 mW.

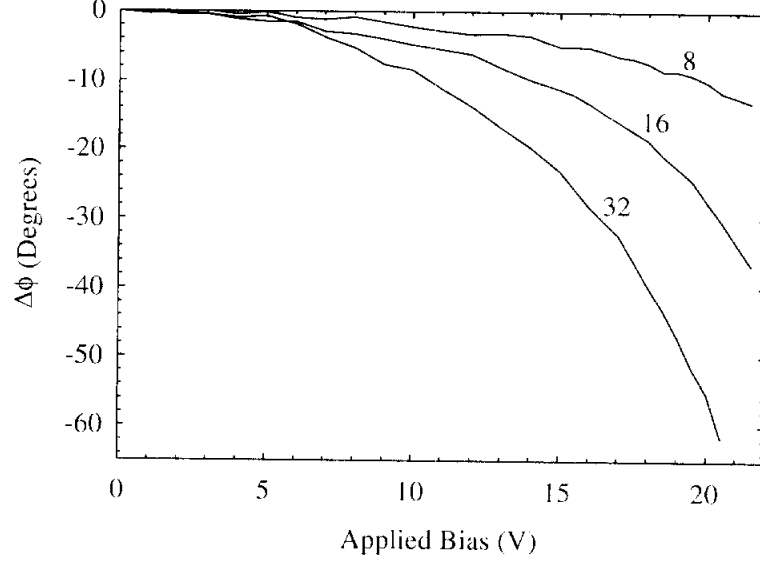


Figure 5.18: DMTL lines measured as phase verniers at 40 GHz. All three lines have $30\text{ }\mu\text{m}$ wide bridges spaced at $306\text{ }\mu\text{m}$ with the number of bridges shown in the plot. The insertion loss is 0.51/0.75/1.57 dB for the 8/16/32 bridge DMTLs.

5.3 Phase Verniers

Figure 5.18 shows the operation of the DMTLs as phase verniers at 40 GHz. The measurement was done on three lines with identical bridge widths ($30\text{ }\mu\text{m}$) and spacings ($306\text{ }\mu\text{m}$). The number of bridges on each line is labeled in the plot. As can be seen from the measurement, $12^\circ/36^\circ/62^\circ$ phase shift at 40 GHz can be achieved over a 21 V bias control for the 8/16/32 bridge DMTLs with minimal insertion loss. Thus, very fine control of the phase (0° - 36°) can be achieved with less than 0.5 dB insertion loss with 8000 Å gold lines. This is well suited for applications in which a digital master clock drives several direct digital synthesizers to achieve true time delay over a large array of antenna elements. A phase vernier is then needed to fine tune the phase between the receiver/transmitter modules at each antenna element.

5.4 Power Handling Measurement

The power handling of the DMTL can be limited by either the current density on the transmission line causing excessive heating or by the MEMS bridges being pulled down due to the average RF voltage on the line. Since the electrostatic force attracts the bridge

towards the center conductor with either a positive or negative voltage, it is as if the RF voltage was rectified and the average voltage level of the rectified sine wave due to the RF power on the line is pulling on the bridge.

The average voltage of a rectified sine wave is given by:

$$V_{avg} = \frac{1}{T} \int_0^{T/2} V_p \sin(\omega t) dt = \frac{V_p}{\pi} \quad (5.12)$$

where $T = 2\pi/\omega$. The RF power in terms of the peak voltage, V_p is given by:

$$P = \frac{V_p^2}{2Z} \quad (5.13)$$

where Z is the characteristic impedance of the DMTL and is typically near 50 Ω . Using (5.12), the RF power on the DMTL can be written as:

$$P = \frac{\pi^2 V_{avg}^2}{2Z} \quad (5.14)$$

Using this equation, the predicted RF power level at which the DMTL, with a 6 V pull-down voltage, will be pulled down is 3.6 W while for a pull-down voltage of 20 V, the RF power level is 39.5 W.

Power measurements were carried out on DMTLs with pull-down voltages from 6 V to 20 V. The power source was an X-band (8-12 GHz) TWT amplifier and the maximum output power delivered to the DMTL was approximately 7 W. However, even at this power level, none of the DMTLs tested had the bridges pull down due to the RF voltage. What was found is that after pumping 7 W through the DMTL, the pull-down voltage had increased. For the line with an initial pull-down voltage of 6 V, the pull-down voltage increased to 20 V. The DMTL with an initial pull-down voltage of 20 V ended up with a pull-down voltage above 40 V and could not be accurately measured due to bias tee limitations. It is believed that the large amount of RF current passing down the line heated up the bridges such that some amount of annealing occurred resulting in a higher pull-down voltage. The heating of the bridges was certainly made worse by the low thermal conductivity of quartz which is 0.014 W/cm-K, compared to the thermal conductivity of silicon which is 1.5 W/cm-°C [53].

CHAPTER 6

Conclusions and Future Work

This thesis presented the application of MEMS bridges to periodically loaded lines and focused on the use of this distributed MEMS transmission line as a millimeter wave phase shifter. Optimized phase shifters were developed at 60 GHz with a maximum performance of $90^\circ/\text{dB}$ or 360° phase shift with only 4 dB loss, and 100 GHz with $70^\circ/\text{dB}$ or 360° phase shift with only 5.1 dB loss. These are the lowest loss millimeter wave phase shifters reported to date. In addition, the distributed MEMS transmission line was applied as a broad band switch with better than 40 dB isolation over bandwidths of 20-40 GHz and 40-60 GHz. Also, a BPSK phase modulator was demonstrated with at a modulation rate of 1 kHz and a required drive power of less than $2 \mu\text{W}$. All of these devices have great potential for advancing the functionality of millimeter wave systems, particularly when low power consumption is required.

6.1 Very Low Loss Phase Shifters

As was noted repeatedly in Chapter 4, the performance of the DMTL phase shifter is primarily limited by the small variation in bridge capacitance that could be achieved using electrostatic actuation in the region before the bridges are pulled down. One attempt made at increasing this variation in bridge capacitance was to increase the stable actuation region by incorporating series capacitors in the bias path of the DMTL. Unfortunately, due to dielectric charging, the increased capacitance variation was never achieved. This problem has been reported by other researchers using capacitive MEMS switch technology and is

certainly one area for future research.

In addition to this, it was noted that the variation that could be achieved, ~ 1.2 , is less than the theoretical variation of 1.5. There are several possible reasons for this difference including variations in bridge thickness and residual stress. These variations are primarily a result of non-uniformity across the wafer due to the fabrication process.

One solution to this problem is to use the MEMS bridge in a digital mode rather than analog. Thus, the applied voltage is either above the pull-down voltage with an associated down-state capacitance or there is no applied voltage with an associated up-state capacitance. Using this approach, the capacitance ratio can be designed to be 2 or 3 to give the largest phase shift for the maximum allowable return loss as discussed in Section 4.1. However, in order to achieve the necessary phase resolution, several bits are needed as in a switched line phase shifter.

In addition to using the digital phase shift, the loss can be further reduced, thus enhancing the phase shifter performance, by designing the distributed line using microstrip rather than CPW. Using the combination of digital phase shift and microstrip, for low loss, the DMTL phase shifter should be able to achieve $360^\circ/\text{dB}$ at 35 GHz or 1 dB loss for 360° phase shift.

Such incredible performance would certainly lead to new innovative designs for phased array systems. In current phased array systems, there is a PA/LNA chip at each antenna element in order to limit the effect of the loss in the phase shifters. However, with 1 dB insertion loss or less, the number of PA/LNA chips needed could be reduced by using one chip for several antenna elements. This would greatly reduce the cost of large phased array systems which typically have thousands of antenna elements.

6.2 Wideband Switches

Although it was shown that the distributed MEMS transmission line could be used for wideband high isolation switching, the results were limited, again, by the fabrication process. The capacitance ratio for the switches was only 10-12 and thus, the change in the Bragg frequency was limited. If a capacitance ratio of 80-100, as reported by industry,

is used, then the change in the Bragg frequency would be much larger and result in a bandwidth of 40 or 60 GHz. Also, the isolation was shown to be limited by leakage through substrate modes. Several techniques could be used to lower the effect of substrate modes including judicious layout to limit the coupling between the two sides of the switch, as well as the use of micromachining/micropackaging to increase the isolation [3].

The distributed line is not necessarily the best switch design, depending on the performance criteria. A more compact design can be achieved by using two tuned bridges as presented by Muldavin *et al.* This technique has already been shown to result in -40 dB isolation from 20 to 40 GHz with a capacitance ratio of 40 and a pull-down voltage of 15 V [33]. Muldavin *et al.* have also shown a cross bridge design using 4 MEMS bridges with a capacitance ratio of 45 results in better than 50 dB isolation over a bandwidth of 12-40 GHz.

All of these switch designs are reflective in nature. However, it is possible, using the distributed line approach, to design an absorptive switch such that when the switch is down, rather than appearing as a short circuit, the switch is matched to $50\ \Omega$. Such absorptive type switches are important for use with power amplifiers and VCO's where it may be damaging to the active device if the power was reflected back into the output by the switch.

6.3 Modulators

Low drive power phase modulators are very useful in applications requiring battery operation where power is at a premium. As shown in Chapter 5, the DMTL phase modulator can be designed to operate up to 100 kbps by appropriately designing the MEMS bridge, with an associated drive power of less than 0.8 mW. If a lower data rate of 30 kbps is acceptable, then the MEMS bridge can be redesigned such that the drive power is on the order of $10\ \mu\text{W}$. Thus, extremely low power communications systems can be designed which would greatly extend battery lifetimes.

The DMTL phase modulators presented in this thesis are much larger than need be. By using a 3 dB hybrid coupler, such as a Lange coupler, a phase modulator can be constructed which requires only a few MEMS varactors. Thus, the drive power requirements can be even further reduced while maintaining very good linearity and low insertion loss.

6.4 Development of High-Q Varactors

Varactors can be used in a number of applications including tunable filters and voltage controlled oscillators (VCOs) [3, 13]. Traditionally, varactor diodes have been used in these applications, however, the filter and VCO performance suffer from the relatively high series resistance. Thus, a MEMS varactor is extremely useful due to its very low series resistance.

In the case of tunable filters, the MEMS varactor could be used with an interdigitated filter in which the varactors load the resonant elements to tune the resonant frequency. As shown by Brown, the series resistance of the varactor can very quickly destroy the quality factor of the resonant transmission line [3]. Thus, the low series resistance of a MEMS varactor would give much greater filter performance. Tunable filters which maintain excellent filter performance will greatly enhance the functionality of receiver systems and reduce the need for space consuming filter banks.

The phase noise of VCOs is inversely proportional to the quality factor of the resonant circuit [13]. Thus, a high-Q MEMS varactor could yield tunable oscillators which maintain very good phase noise characteristics. VCOs are a critical component in modern wireless communications systems, particularly as more multi-function systems are designed. By enabling VCOs which maintain very good phase noise performance, tunability can be introduced into many more systems which, until now, have not been able to use VCOs due to stringent phase noise requirements.

APPENDICES

APPENDIX A

Forces on a Capacitor

The derivation of the electrostatic force on a capacitor is often misunderstood and is not always immediately obvious. One very useful source for this derivation is Electromagnetic Field Theory: a problem solving approach, by Markus Zahn [61]. The derivation is quoted here for reference:

Consider a capacitor that has one part that can move in the x direction so that the capacitance depends on the coordinate x :

$$q = C(x)v \tag{A.1}$$

The current is obtained by differentiating the charge with respect to time:

$$\begin{aligned} i &= \frac{dq}{dt} = \frac{d}{dt} [C(x)v] = C(x) \frac{dv}{dt} + v \frac{dC(x)}{dt} \\ &= C(x) \frac{dv}{dt} + v \frac{dC(x)}{dx} \frac{dx}{dt} \end{aligned} \tag{A.2}$$

Note that this relation has an extra term over the usual circuit formula, proportional to the speed of the moveable member, where we expanded the time derivative of the capacitance by the chain rule of differentiation. Of course, if the geometry is fixed and does not change with time ($dx/dt = 0$), then (A.2) reduces to the usual circuit expression. The last term is due to the electro-mechanical coupling.

The power delivered to a time-dependent capacitance is

$$p = vi = v \frac{d}{dt} [C(x)v] \tag{A.3}$$

which can be expanded to the form

$$\begin{aligned} p &= \frac{d}{dt} \left[\frac{1}{2} C(x) v^2 \right] + \frac{1}{2} v^2 \frac{dC(x)}{dt} \\ &= \frac{d}{dt} \left[\frac{1}{2} C(x) v^2 \right] + \frac{1}{2} v^2 \frac{dC(x)}{dx} \frac{dx}{dt} \end{aligned} \quad (\text{A.4})$$

where the last term is again obtained using the chain rule of differentiation. This expression can be put in the form

$$p = \frac{dW}{dt} + f_x \frac{dx}{dt} \quad (\text{A.5})$$

where we identify the power p delivered to the capacitor as going into increasing the energy storage W and mechanical power $f_x dx/dt$ in moving a part of the capacitor:

$$W = \frac{1}{2} C(x) v^2, \quad f_x = \frac{1}{2} v^2 \frac{dC(x)}{dx} \quad (\text{A.6})$$

Using (A.1), the stored energy and force can also be expressed in terms of the charge as

$$W = \frac{1}{2} \frac{q^2}{C(x)}, \quad f_x = \frac{1}{2} \frac{q^2}{C^2(x)} \frac{dC(x)}{dx} = -\frac{1}{2} q^2 \frac{d[1/C(x)]}{dx} \quad (\text{A.7})$$

APPENDIX B

An Octave Bandwidth Monopulse Processor

B.1 Introduction

The monopulse processor is a critical component in monopulse radar systems. It forms the sum and difference channels (azimuth and elevation) from four antenna inputs as shown in Figure B.1(a). The sum, difference in azimuth, and difference in elevation signals are used to determine the angular position of the target relative to boresight[50]. The monopulse configuration is the standard technique used for high accuracy tracking with typical applications including airport traffic control, aircraft defense, and ship defense.

Waveguide monopulse processors have typically been designed using $0^\circ/180^\circ$ 3 dB couplers (waveguide magic-tees). However, $0^\circ/180^\circ$ 3 dB couplers cannot be used in planar circuits due to the positioning of the sum and difference ports. As a result, $0^\circ/90^\circ$ 3 dB couplers are used with 90° delay lines to synthesize the monopulse pattern as shown in Figure B.1(b)[25]. One critical problem when implementing this configuration as a planar circuit is the crossover of the two lines in the center of the processor. Jackson, et al. solved this problem by unfolding the processor such that the feeds from the antennas are in the center of the processor as shown in Figure B.2[25]. However, this configuration is not viable for applications in which a dual-polarized antenna is used.

In this work, the cross-over problem is solved using a 0 dB coupler as shown in Figure B.3(a)[55]. The 0 dB coupler is formed by cascading two $0^\circ/90^\circ$ couplers and allows the two signals in the middle of the monopulse processor to cross over one another without

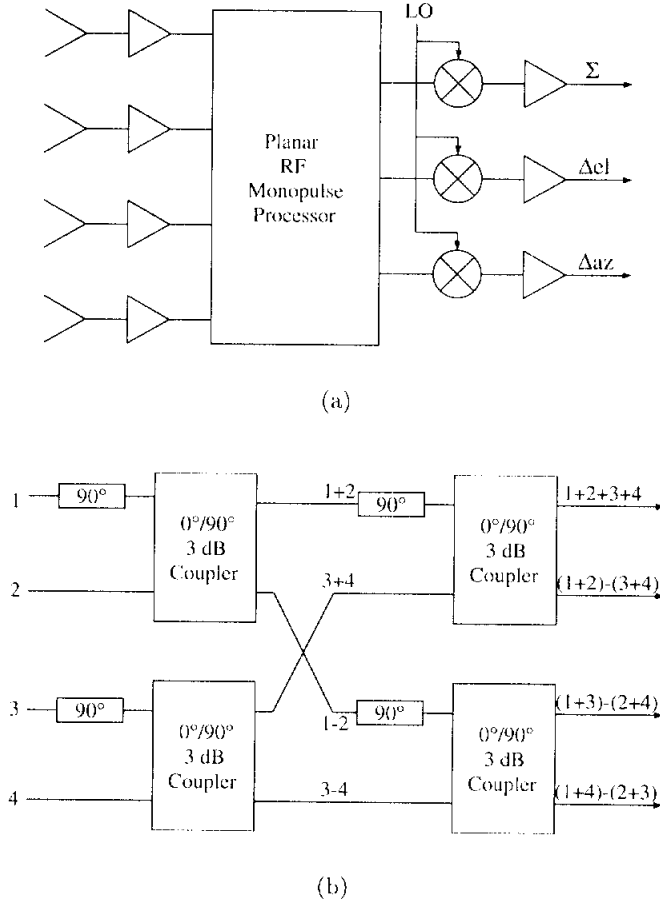


Figure B.1: (a) Monopulse radar receiver with (b) a standard monopulse processor using $0^\circ/90^\circ$ 3 dB couplers.

coupling. Figure B.3(b) shows the circuit simulation of the 0 dB coupler implemented using Lange couplers. As can be seen, the coupler allows the cross-over of the two signals with better than 16 dB isolation over an octave bandwidth. The 0 dB coupler also delays each of the signals by 90° which eliminates the need for the two 90° lines in the standard monopulse configuration.

The wideband monopulse processor is an excellent choice for the new IF-based monopulse processors first proposed by Ling *et al.*[31]. In this configuration, the RF channels are amplified, mixed down to an IF, amplified again and then sent to the monopulse processor. The IF-based monopulse processor reduces the complexity of the RF front-end and enables the use of additional amplification at the IF to reduce the effects of loss in the processor. This novel monopulse processor allows a wideband millimeter-wave signal to be processed

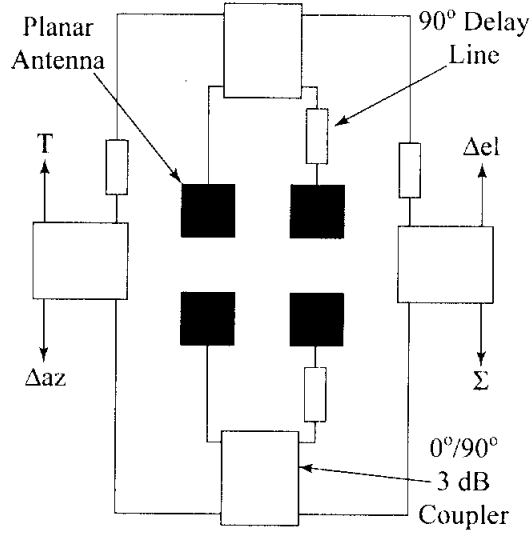


Figure B.2: Example of a planar RF monopulse processor using using 0°/90° 3 dB couplers with 90° delay lines. The output labeled T is terminated in a matched load.

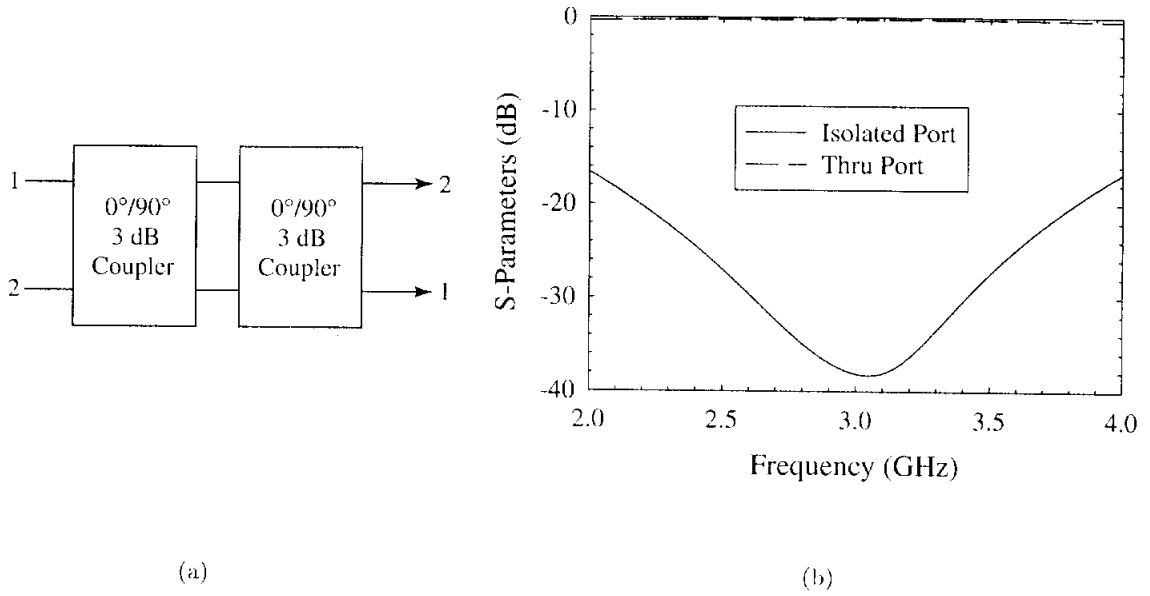


Figure B.3: 0 dB coupler used in the Monopulse processor; (a) block diagram and (b) simulation using Lange couplers.

at low IF frequencies (2-4 GHz).

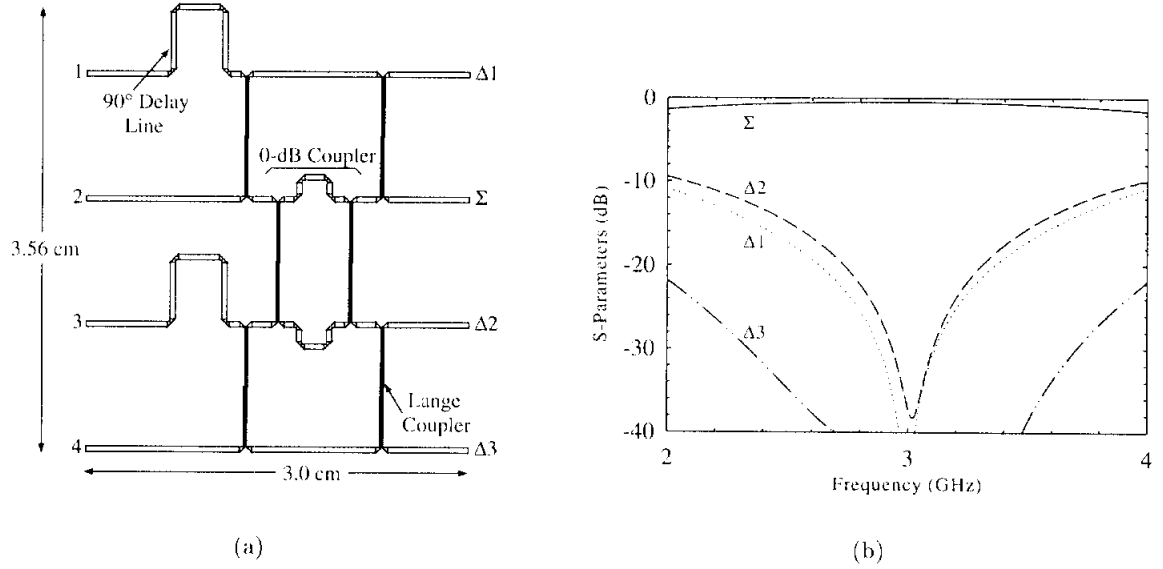


Figure B.4: Monopulse processor using Lange couplers; (a) layout and (b) simulation.

B.2 Design and Measurements

In order to achieve the largest possible bandwidth, the monopulse processor was designed using Lange couplers for the $0^\circ/90^\circ$ 3 dB couplers. As can be seen from Figure B.4(a), this results in an elegant and compact design. The processor was designed for a $525\ \mu\text{m}$ high resistivity silicon substrate and simulated using HP EEsof's Libra¹. The simulated results shown in Figure B.4(b) demonstrate a difference port with a 20 dB null-depth over a 2 GHz bandwidth centered at 3 GHz and a sum pattern with a 1 dB variation over the bandwidth. The remaining two difference ports are of standard bandwidth due to the dispersion effects of the input 90° delay lines.

In order to understand why $\Delta 3$ has such a wideband null, the group delay of each input port to $\Delta 1$ and $\Delta 3$ was simulated. As can be seen in Figure B.5(a), the group delay from ports 1 and 4 are very close and thus, the difference of these ports will be very low over the entire bandwidth. However, the group delay from ports 2 and 3 are not very close at all and diverge away from the center frequency. This is the cause of the narrowband null in $\Delta 1$. By comparison, the delays in Figure B.5(b) show that ports 1 and 2 are close enough together to form a good null and they stay close together across the entire bandwidth. Ports 3 and

¹HP EEsof Release 6.0, July 1995

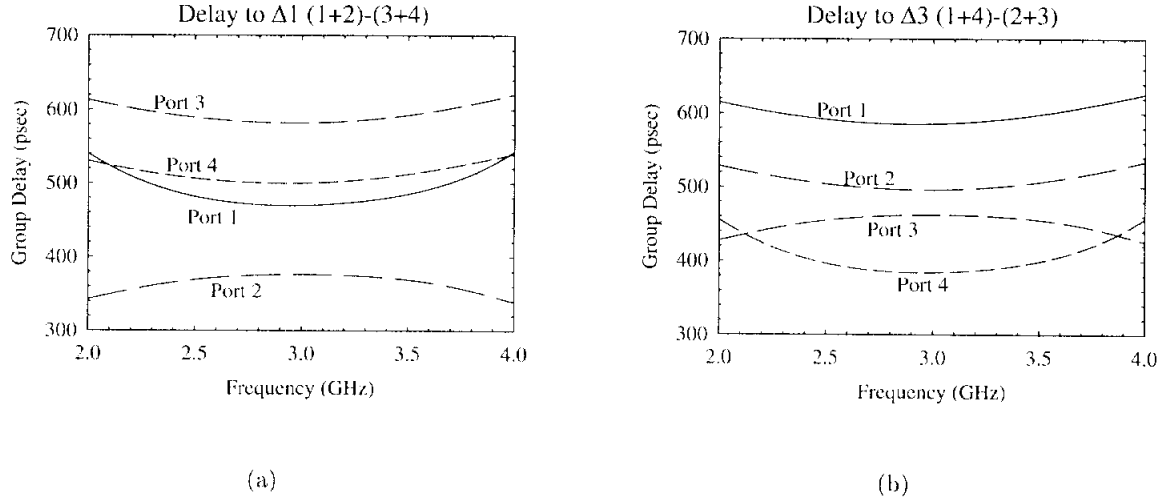
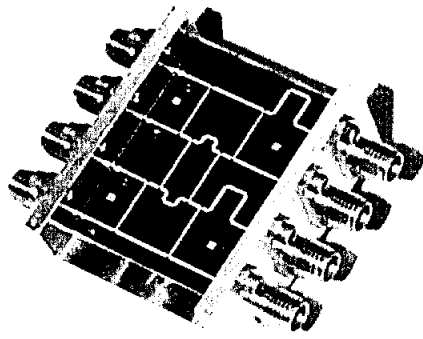


Figure B.5: Simulated group delay from the input ports to (a) $\Delta 1$ and (b) $\Delta 3$.

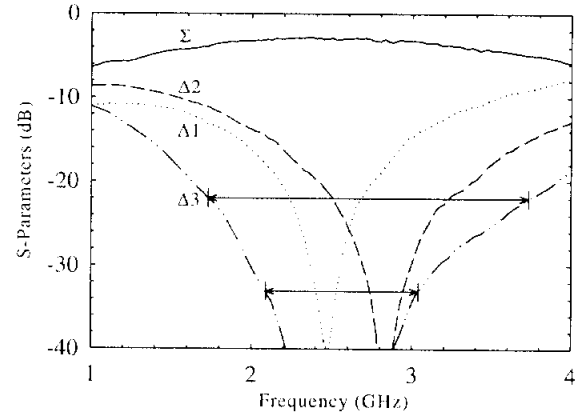
4 are close at the center frequency and get closer away from the center frequency. Thus, $\Delta 3$ maintains a good null across the entire octave bandwidth.

The width of the lines in the Lange coupler is $29 \mu\text{m}$ and the separation between the lines is $39 \mu\text{m}$. The couplers are 9.46 mm long and the 50Ω lines are all 0.43 mm wide. The microstrip transmission lines are gold plated to a thickness of $3 \mu\text{m}$ and the ground plane is gold plated to a thickness of $6 \mu\text{m}$. The input and output lines are all spaced 1 cm apart which allows SMA connectors to be used without the need for additional spacing. An aluminum mount is used to hold the silicon wafer and connectors, and the connections between the SMA connectors and the microstrip lines are made with silver epoxy. The fully assembled monopulse processor is shown in Figure B.6(a).

The monopulse processor was tested using a Mini-Circuits 2-4 GHz 4-way power divider and an HP 8720 vector network analyzer. As can be seen from Figure B.6(b), the center frequency of the monopulse processor is shifted down in frequency to 2.6 GHz . However, even with this shift in frequency, a wideband difference port is obtained with an 18 dB null over 2 GHz and a 30 dB null over 0.95 GHz . The shift in the measured frequency response is due to phase error in the Lange couplers. The increased loss in the measured data is due to the connectors and skin effect losses since the transmission lines are only 1.2-2.4 skin depths thick from 1-4 GHz.



(a)



(b)

Figure B.6: (a) Picture of assembled Lange coupler based monopulse processor and (b) measured response.

B.3 Conclusion

We have demonstrated a wideband Lange coupler based monopulse processor centered at 2.6 GHz with an 18 dB null over a 2 GHz bandwidth. This design can be scaled up to X-band or K-band in order to obtain much greater bandwidths (8-16 GHz, 20-40 GHz) if necessary. The monopulse processor has also proved to be very useful in the new IF-based monopulse systems, allowing the processing of 2 GHz wideband signals from a 94 GHz radar system.

APPENDIX C

IF-Based Polarimetric Receivers

C.1 Introduction

Polarimetric radars from L-band to W-band are widely used for remote-sensing, tracking, and target discrimination applications [54]. Current polarimetric radars use a dual-polarized antenna (microstrip or waveguide type) connected to a set of LNA's, variable attenuators, and phase shifters as shown in figure C.1(a). The processed H (horizontal polarization) and V (vertical polarization) signals are summed to give a particular polarization state depending on the setting of the variable attenuators and phase shifters. Since the RF polarimetric circuits are expensive, multiple polarization states are not formed simultaneously. This is not acceptable for applications in which a quick measurement of multiple polarizations is required, such as smart munition seekers or advanced automotive radars.

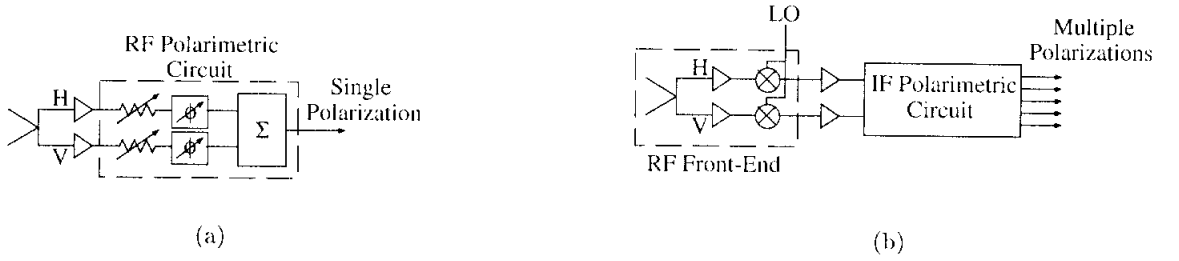


Figure C.1: Architecture of (a) Current Polarimetric Systems and (b) Proposed IF-Based Polarimetric System.

In order to provide low-power multiple polarimetric measurements, the system shown

in figure C.1(b) is proposed as a means of forming many polarization states at the IF frequency. The advantage of this system is that low-cost low-power silicon-based IF circuits can be used to perform most of the processing and many different polarization states can be formed simultaneously. This architecture also allows the IF frequency, used to perform the polarimetric processing, to be independent of the RF frequency. Thus, the same IF polarimetric processor can be used with different RF front-ends. The disadvantage with this system is the larger fractional bandwidth which the received signal has at IF frequencies compared to RF frequencies. However, it is possible to build an IF network which yields an accurate polarization measurement for a fractional bandwidth of 20%. Since current radars have a bandwidth of 50 to 250 MHz, it is seen that an IF network centered at 2 GHz can process a 400 MHz bandwidth signal.

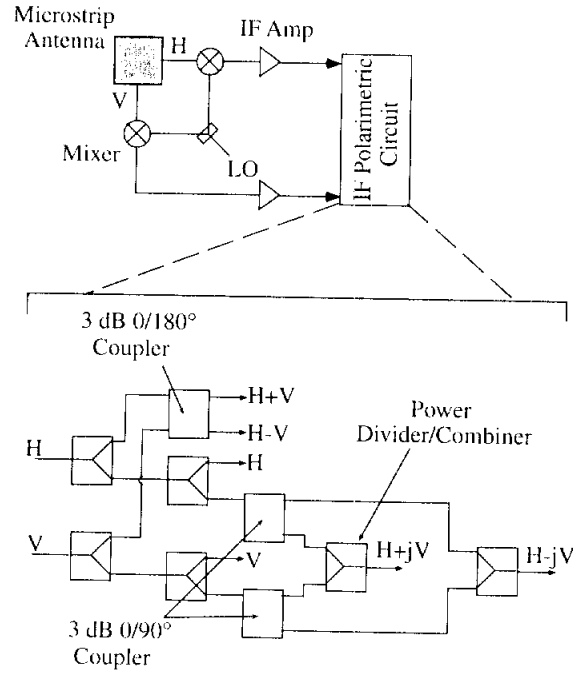


Figure C.2: Schematic of the Passive IF Polarimetric Receiver.

C.2 Experiment

The polarimetric receiver is composed of a 9.8 GHz dual-polarized microstrip antenna, fabricated on a 0.51 mm thick $\epsilon_r = 2.2$ Duroid substrate¹, followed by two balanced mixers with a measured SSB conversion loss of 6 dB. The mixers are fed with an LO frequency of 9.6 GHz, resulting in an IF frequency of 200 MHz. All of the IF couplers, amplifiers and switches used for the IF circuitry are low-cost components purchased from Mini-Circuits². The IF polarimetric processor can be completely integrated on silicon, including all necessary amplifiers and switches up to 1 - 2 GHz [4]. This will reduce the cost even further and also increase the available bandwidth of the system.

The IF polarimetric circuit that has been tested is shown in figure C.2. It is based on the concept of a six-port junction in which the relative phase and amplitude between the two input signals can be determined from four different amplitude measurements [24]. In this case, six different measurements have been used in order to decrease the error in the polarization measurement.

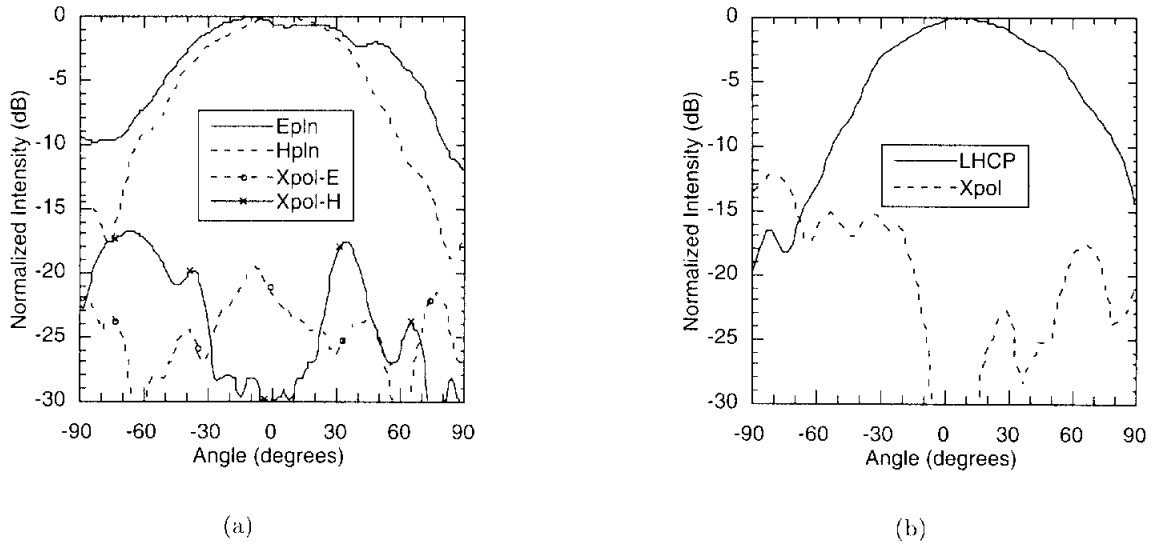


Figure C.3: Response of Polarimetric Receiver for (a) Horizontally Polarized Wave and (b) Left-hand Circularly Polarized Wave.

To verify the operation of the polarimetric receiver, two tests are performed. The first

¹Rogers Corp., 100 S. Roosevelt Ave., Chandler, AZ 85226 USA.

²Mini-Circuits, P.O. Box 350166, Brooklyn, NY 11235-0003 USA

measures various antenna patterns where the measurements are taken from the output ports of the IF polarimetric circuit. The second test transmits many different polarizations and measures the error in the incident polarization calculated from the amplitude measurements taken at the IF output ports. For both of these tests, an X-band quad-ridged horn is used as the transmitting antenna. The transmitted polarization is set by adjusting low-loss coaxial line stretchers placed in the feed-lines of the quad-ridged horn. The coaxial line stretcher physically changes the length of the line and is therefore equivalent to a MMIC phase shifter in the sense that it adjusts the phase of the signal.

C.3 Results

The received patterns for a horizontally polarized transmitted wave and a left-hand circularly polarized transmitted wave measured at the IF ports are shown in figures C.3(a) and C.3(b), respectively. The measured patterns show the typical traits of a microstrip antenna. For the linearly polarized wave the E-plane pattern falls to -10 dB at 90° , and the H-plane pattern is -15 dB at 90° . The cross-pol. for the microstrip antenna was measured to be -23 dB and so the increased cross-pol. seen here is due to the presence of the RF and IF circuitry around the antenna. For the circularly polarized wave, the cross-pol. increases significantly near $\pm 90^\circ$ (as expected) due to the difference between the E and H-plane patterns.

To obtain accurate polarization measurements, the system is calibrated to eliminate phase and amplitude imbalances in the IF couplers. The calibration is performed by transmitting six different known polarizations and then calculating the necessary calibration coefficients from the measured response. Figure C.4 shows the results of the calibrated and uncalibrated measurements. As can be seen, the calibrated system works well and gives a $\pm 5^\circ$ error in the measured polarization at the IF ports. This error is limited by the accuracy of the transmitting system. The jumps in the uncalibrated curve are due to using different output ports of the IF polarization circuit to find the incident polarization.

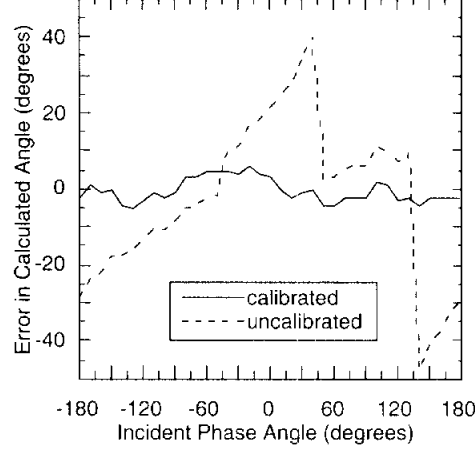


Figure C.4: Measured Phase Error for X-band Receiver.

C.4 Conclusion

The idea of using IF based polarimetry for applications in which a quick polarization measurement is needed while maintaining low power consumption has been proposed. The advantage of this architecture is that low-cost low-power silicon-based IF circuits can be used to implement the polarimetric processing. Bandwidth should not be a problem since the IF circuits can be designed to operate at 1 - 2 GHz. This idea has been successfully demonstrated with an X-band system, and can be implemented with any RF frequency.

APPENDIX D

Detailed Fabrication Process

This appendix discusses the fabrication process used for the distributed MEMS transmission lines discussed in this thesis. The process used determines, to a large extent, the mechanical properties of the MEMS bridges since the residual stress within the released structures can have a large effect on these properties. This process is based on using quartz wafers and thus includes some steps intended to deal with the particular problems associated with fabricating on quartz.

1. Wafer Cleaning:

- (a) Immerse the wafer for 15 minutes in 1:1 $\text{H}_2\text{SO}_4\text{:H}_2\text{O}_2$ (Piranha Etch). Cascade rinse in deionized (DI) H_2O for 5 minutes.
- (b) Blow dry with N_2 . Dehydrate bake on a 130°C hotplate for 2 minutes.
- (c) Clean in a 250 mT O_2 Plasma at 150 W for 3 minutes.

2. CPW metal lift-off:

- (a) Evaporate 200 Å Ti (This step is necessary in order to obtain good adhesion and the correct lift-off profile for the AZ 5214 PR on quartz).
- (b) Spin coat with AZ 5214 PR at 3000 rpm for 30 sec.
- (c) Soft bake on a 105°C hotplate for 1 min.
- (d) Align a clear-field mask, exposing areas where the metal is to be lifted off. Expose at 20 mW/cm^2 for 4.5 sec.

Table D.1: PECVD Si_xN_y recipe [42].

Gas/Flow	$\text{SiH}_4/100$ sccm
Gas/Flow	$\text{NH}_3/10$ sccm
Gas/Flow	$\text{N}_2/990$ sccm
Gas/Flow	$\text{He}/900$ sccm
Pressure	700 mT
RF Power	100 W
Temperature	400° C
Time	12 min.
Thickness	2000 Å

- (e) Hard bake on a 130° C hot plate for 1 min.
 - (f) Flood expose for 1.5 min. at 20 mW/cm².
 - (g) Develop in AZ 327 MIF for 50 sec. Rinse in DI H₂O and dry with N₂.
 - (h) Evaporate 300/8000 Å Ti/Au (8000 Å Au is necessary in order to reduce loss since the CPW center conductor is not electroplated in this process).
 - (i) Soak in acetone (ACE) overnight in order to lift-off undesired metal.
 - (j) Rinse in isopropyl alcohol (IPA). Dry with N₂.
3. Plasma Enhanced Chemical Vapor Deposition (PECVD) of Si_xN_y :
- (a) Clean in a 250 mT O₂ Plasma at 150 W for 3 minutes (This step is critical for removing a film left by the AZ 5214 PR.)
 - (b) Deposit Si_xN_y using recipe listed in Table D.1.
 - (c) Clean in ACE and IPA. Dry with N₂.
 - (d) Spin coat with Hexamethyldisilazane (HMDS) adhesion promoter and Shipley 1813 PR at 3.5 krpm for 30 sec. each.
 - (e) Soft bake on a 105° C hotplate for 1 min.
 - (f) Align a clear field mask, exposing areas where the Si_xN_y is to be removed. Expose for 5 sec. at 20 mW/cm².
 - (g) Develop in 1:5 MF351:DI for 1 min. Rinse in DI and dry with N₂.
 - (h) Hard bake on a 130° C hotplate for 2 min.

Table D.2: PECVD Si_xN_y reactive ion etching (RIE) recipe.

Gas/Flow	CF ₄ /40 sccm
Gas/Flow	O ₂ /1 sccm
Pressure	100 mT
RF Power	100 W
Time	7 min.

- (i) Etch Si_xN_y in a CF₄ and O₂ plasma using the recipe shown in Table D.2 (This etch will also remove some or all of the 200 Å Ti layer).
 - (j) If any of the 200 Å Ti layer is remaining, remove it in 1:10 HF:DI.
 - (k) Remove the resist in a 250 mT O₂ plasma at 150 W for 3 min.
 - (l) Clean in ACE and IPA. Dry with N₂.
4. Metal electroplating and MEMS bridge formation:
- (a) Spin coat with Shipley 1813 PR at 3-5 krpm for 30 sec. to form the sacrificial resist layer which defines the bridge height (the thickness of the resist is from 1.5-1.16 μm after the hard bake).
 - (b) Soft bake on a 105 ° C hotplate for 1 min. 10 sec.
 - (c) Align a dark field mask, exposing areas to be electroplated except any areas beneath bridges or circuit metal regions which are not electroplated. Expose for 5 sec. at 20 mW/cm².
 - (d) Develop in 1:5 MF351:DI for 1 min. Rinse in DI and dry with N₂.
 - (e) Hard bake on a 130° C hotplate for 2 min. 30 sec. (It is important to drive out all of the solvents from the resist in order to avoid problems with bubbling when the next resist layer is applied).
 - (f) Evaporate electroplating seed layer 500/2000/500 Å Ti/Au/Ti.
 - (g) Spin coat Shipley 1813 PR at 3 krpm for 30 sec. (resist thickness is approximately 1.6 μm).
 - (h) Soft bake in 80° C oven for 20 min.

- (i) Align a dark field mask exposing areas to be electroplated, including the air bridges. Expose for 5 sec. at 20 mW/cm².
- (j) Develop in 1:5 MF351:DI for 1 min. Rinse in DI and dry with N₂.
- (k) Etch the exposed top Ti layer in 1:10 HF:DI for approximately 6 sec. Rinse in DI and dry with N₂.
- (l) Electroplate 2.5-3 μm of gold using a current of 6 mA with a plating rate of $\sim 0.12 \mu\text{m}/\text{min}$. (with this solution, higher plating current tends to give more compressive stress in the bridges, which can cause buckling). The gold plating solution used is Aurall 305¹ at a temperature of 50° C and stirred with a magnetic stir rod.
- (m) Rinse in DI and dry with N₂.
- (n) Flood expose the top layer of resist for 1.5 min. at 20 mW/cm².
- (o) Develop in 1:5 MF351:DI for 1 min. Rinse in DI and dry with N₂.
- (p) Strip the Ti/Au/Ti seed layer. The Ti is etched in 1:10 HF:DI for approximately 6 sec. The gold is etched in TFA Gold Etchant ($\sim 28 \text{ \AA}/\text{sec}$. at room temperature). Rinse in DI between each etch. Care must be taken when etching the gold seed layer since the gold etch will also attack the electroplated gold and at a much higher etch rate than the evaporated gold ($\sim 2\text{-}4\times$ faster). This is most critical for the bridges since if the bridge thickness becomes too small, the bridge could buckle due to compressive stress.
- (q) Rinse in DI and dry with N₂.
- (r) Remove the sacrificial resist layer by soaking in PRS-2000 overnight. At this point, the wafer cannot be air dried because the surface tension of the evaporating liquid will pull the released bridges down to the substrate causing them to stick [28].
- (s) Rinse in DI for 5 min.

¹The patent on the Aurall 305 gold process is held by LeaRonald Inc. 272 Buffalo Ave. Freeport, NY 11520

5. Release of MEMS bridges:

- (a) Transfer from DI to IPA and then to fresh IPA to remove all DI.
- (b) Transfer to Ethanol and then to fresh Ethanol to remove all IPA. The release process uses liquid CO₂ which is miscible with Ethanol but not IPA.
- (c) Transfer to Critical Point Dryer chamber filled with Ethanol and secure chamber.
- (d) Cool chamber down to -20° C.
- (e) Replace Ethanol with liquid CO₂ by filling and purging the chamber with liquid CO₂ several times.
- (f) Completely fill the chamber with liquid CO₂ and turn on heater.
- (g) Once the chamber pressure and temperature have risen above the CO₂ critical point (1073 psi and 31.1° C), the pressure is gradually reduced, while maintaining a constant temperature of ~ 35° C, such that the super fluid transitions directly to a gas [34].
- (h) Clean in a 250 mT O₂ plasma at 150 W for 3 min.

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