

HIGH-POWER MILLIMETER-WAVE PLANAR DOUBLERS

Guan-Leng Tan and Gabriel M. Rebeiz

EECS Department, The University of Michigan, Ann Arbor, MI 48109-2122

gtan@umich.edu, rebeiz@umich.edu

Abstract

This paper presents two different planar doubler designs for mm-wave applications. The doublers are fabricated using two Schottky varactor diodes in series for high power operation. The high-Q design ($Q = 6$) results in a conversion loss of 6.4 dB at an output frequency of 72-73 GHz. The low-Q design ($Q = 1.6$) results in a conversion loss of 9.6 ± 0.7 dB from 64-78 GHz at -2 V bias, and delivers 71 mW at 74 GHz for an input power of 490 mW (conversion loss of 8.4 dB, at optimal bias of -7 V). The output power shows no sign of saturation, and is limited to 71 mW due to the input source power. The results are quoted "on-chip" and are state of the art for mm-wave planar multipliers. The application areas are in automotive collision avoidance radars and mm-wave communication systems.

Introduction

Automotive radars and mm-wave communication systems typically require between 10 and 100 mW of RF power at the transmit antenna. This can be achieved using waveguide-based doublers [1], but these components are expensive to manufacture and are not compatible with a low cost planar process. Another approach is to use either HEMT amplifiers or varactor doublers. HEMT amplifiers are expensive to manufacture and are not readily available. Planar doublers offer a simple solution and have been extensively used at mm-wave frequencies. Recently, MMIC doublers have been developed with excellent conversion loss (6-9 dB), but these

doublers either begin to saturate in the 50mW range [2], or require a relatively complicated fabrication procedure [3].

This paper presents a simple planar design capable of high power operation. The doubler is integrated on a quartz substrate using a microstrip implementation for low loss operation, and a hybrid approach is used to attach the diode chip to the substrate. Quartz is chosen since it is compatible with the M/ACOM GMIC (Glass MIC) process [4], [5] and with LTCC substrates. The doubler is based on a series design as shown in Fig. 1. The series design is much easier to model than the shunt approach, and does not require via-holes. Also, one can easily use two varactor diodes in series for high power applications without changing the doubler configuration (other than the matching networks).

Design

The doubler is built using two GaAs Schottky varactor diodes in series (see Fig. 1), each with $R_s=2.7-4 \Omega$, $C_{j0}=80$ fF and $C_p=12-16$ fF. The cutoff frequency of the diode, given by $f_c = 1/[2\pi R_s(C_{j0} + C_p)]$, is 430-640 GHz. The diodes are designed by Dr. Imran Mehdi at the NASA Jet Propulsion Laboratory [6],[7] using a wafer with a doping level of $1 \times 10^{17} \text{ cm}^{-3}$ and a 4800 Å thick n-epilayer. In order to reduce the parasitic resistance, the anode is designed as a $3.0 \times 20.0 \mu\text{m}$ rectangular strip instead of the conventionally used circular configuration. No channel etching is required in this process, thus allowing for very short finger lengths along with arbitrary

circuit configurations. The Schottky contact and the air-bridge/finger are fabricated in one step to avoid any alignment and parasitic capacitance issues. The series diodes are integrated on the same chip with dimensions of $175 \times 100 \mu\text{m}$. The input impedance of the low-Q design, calculated using a harmonic balance program Libra [8], is $50.6 - j80.8 \Omega$ at 37 GHz, and $20.2 - j42.3 \Omega$ at 74 GHz. This is done for an input power of 100 mW and a bias voltage of -2 V for the diode chip.

The design of the doubler has two goals: 1) high-efficiency operation and 2) a compact circuit with no via-holes. To achieve this, a microstrip line is used on a $101.4 \mu\text{m}$ ($\lambda_d/20$ at 74 GHz) thick quartz substrate (Fig. 1). The open straight stub at the output of the doubler is $\lambda/4$ long at f_{in} and presents a short at the diode chip terminal. This allows all the input power to be dissipated in the diode (when well matched). Also, a $\lambda/4$ long (at f_o) open stub is placed in the input circuit at a distance of $\lambda/2$ (at f_0) from the diode. This presents a short at f_o at the diode chip terminal at the input port, and the power generated by the diode at f_0 is directed towards the output port. A wideband radial stub is used in the input and output circuit to match the diode impedance to 50Ω .

The input and output circuits are first designed with Libra microstrip models. Then, the circuits are simulated in IE3D [9], including the cpw-to-microstrip transitions, and the dimensions of the stubs and T-junctions are optimized to result in the right impedance transformation. The process is iterative but very fast since the input and output circuits are small and simple to analyze. Two designs are implemented: A high-Q narrowband design with low conversion loss, and a low-Q wideband design with 2-3 dB of additional conversion loss. The high-Q design is designed to operate at an input power of 30-50 mW with a bias of -5 V for the diode chip. The low-Q design is designed to operate at an input power of 100-200 mW.

Fabrication and Measurements

The microstrip circuit is fabricated using 8000

Å of evaporated gold. A single mask layer is required since no air bridges or via holes are used in the design. The diode chip is attached to the circuit using silver epoxy. The circuit is connected to the measurement set-up using cpw probes, and bias-tees are used at the input and output ports. The loss of the cpw-to-microstrip transition is 0.1 dB at 37 GHz and 0.3 dB at 74 GHz, and is calibrated out of the measurements. The reference planes for the measured data is therefore the beginning of the microstrip line and is shown in Fig. 1.

The measured conversion loss for both designs is shown in Fig. 2. The high-Q design is measured at an input power of 32 mW, while the low-Q design is measured at an input power of 100 mW. The measurements agree well with theory, and result in a conversion loss of 6.4 dB for the high-Q design, and around 9.6 dB for the low Q design over a very wide bandwidth. The bias voltage is -5 V and -2 V, respectively, and is held constant in the swept frequency measurement.

As expected, the high-Q design saturates at a relatively low input power (30-40 mW) and the conversion loss increases to 9-10 dB for an input power of 100-300 mW. The maximum output power achieved with the high-Q design is 32 mW.

On the other hand, the low-Q design is a high-power design, and the conversion loss is 8.4 dB for an input power of 200-500 mW when the bias voltage is adjusted for minimum conversion loss. This results in an output power of 71 mW at 74 GHz (Fig. 3), which is excellent for a planar mm-wave doubler. The associated bias voltage is -7 V for the diode chip. The input and output return loss is less than -10 dB for an input power of 100-200 mW. The output power shows no sign of saturation for an input power of 500 mW. The measured results are obtained without the use of input/output E/H tuners. If the multiplier is used as a stand alone unit, and the input and output transition losses are included, then the results degrade by 0.4 dB.

The rejection of the fundamental signal at the

output port follows closely the response of the resonant straight stub and is shown in Fig. 4 for the low-Q design. A rejection of better than 20 dB is achieved for an output frequency of 71.5-76.5 GHz. At 74 GHz, the stub is resonant and the rejection is 28 dB.

To our knowledge, there is no planar doubler at mm-wave frequencies which provides this level of output power in a small compact circuit (we are excluding the quasi-optical multiplier grids which are not compatible with low-cost automotive systems).

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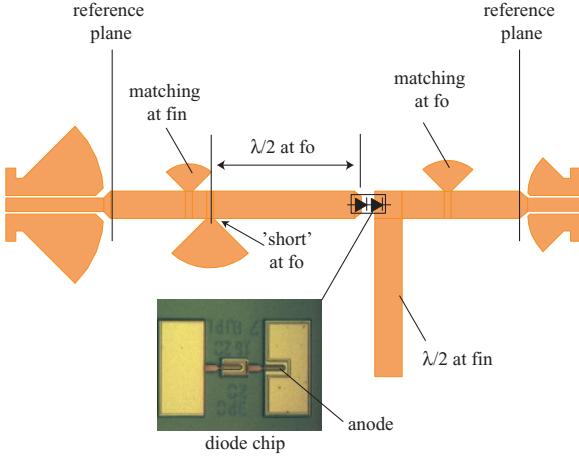


Figure 1: Layout of the low-Q doubler in microstrip form.

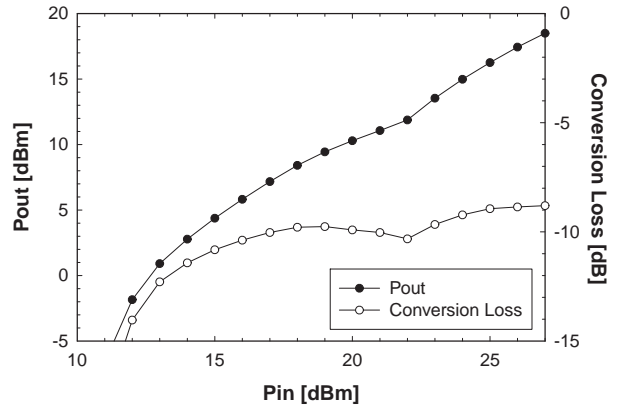


Figure 3: Measured output power and conversion loss of the low-Q doubler at an output frequency of 74 GHz.

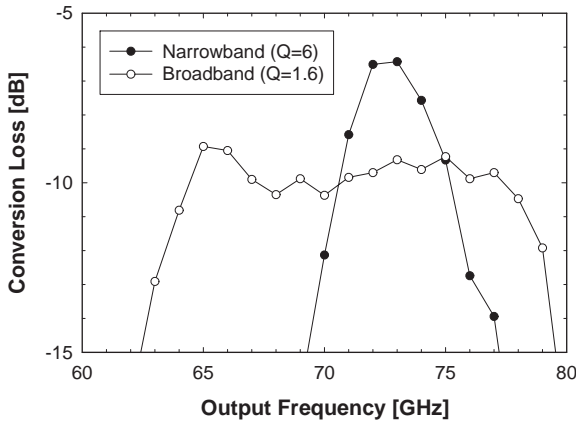


Figure 2: Measured conversion loss of the doublers at fixed bias voltage (-5 V for narrowband design and -2 V for broadband design).

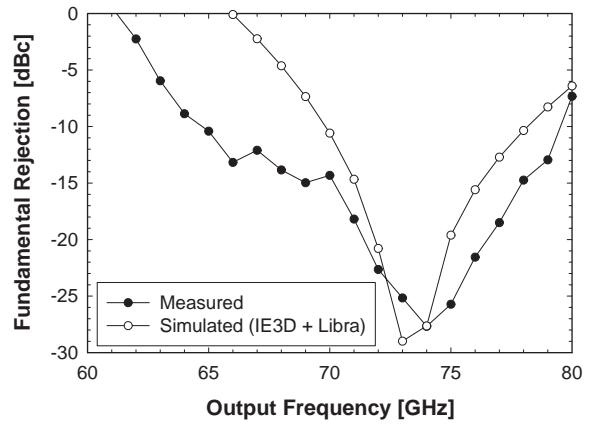


Figure 4: Measured and simulated fundamental rejection for the low-Q doubler.