25.2 An Ultra-Low-Power 9.8GHz Crystal-Less UWB Transceiver with Digital Baseband Integrated in 0.18μm BiCMOS

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Future biomedical and internet-of-things applications are driving the volume of wireless sensors into the cubic-mm regime. At the mm-scale, complete integration is necessary, and operation within the limits of a micro-battery becomes a primary challenge [1]. With CMOS scaling and ultra-low-power circuits reducing battery volume, the antenna and crystal quickly become the largest components in a cubic-mm node. Higher-frequency operation and silicon-based timing circuits are critical to integrate these components. This paper presents a fully-integrated 9.8GHz impulse-radio ultra-wideband (IR-UWB) radio with an on-chip 2mm monopole and the option of wire-bonding to an off-chip antenna. The crystal is replaced with a novel temperature-compensated relaxation oscillator. Due to modern mm-scale battery limitations, the peak current draw must be <100μA [2], far below typical radio power consumption. Furthermore, external capacitors are too large for mm-scale nodes; thus, duty-cycling only at the packet level is not an option. This IR-UWB radio includes current-limiting at the battery supply, and the integrated modem duty-cycles the RF front-end at the bit-level in order to operate from integrated storage capacitance. Finally, many recent transceivers operate at <1V [3,4]; however the voltage of a micro-battery is 3.2~4.1V [2] and integrated conversion efficiency is <80% [1,5]. Thus, this radio is designed to operate the RF blocks over the entire battery voltage range.

The architecture for the IR-UWB radio is shown in Fig. 25.2.1. The transmitter (TX) and receiver (RX) operate at the battery voltage, through a current limiter (CL) to protect the micro-battery from over-current and under-voltage. An internal storage capacitor allows higher current draws from the TX and RX during duty-cycled operation. Digital baseband blocks operate from a 1.2V V_{DD} to reduce power consumption. To survive on the limited resources of the micro-battery, all blocks on the radio have a low-power sleep state. RF and other analog blocks are duty-cycled at the bit level by the baseband controller, while baseband blocks are duty-cycled at the packet level by a separate sleep controller. The sleep controller remains on continuously unless an under-voltage condition occurs. The sleep controller begins and ends the wake-up procedure for each packet via I2C communication with modified I/Os to eliminate pull-up resistors. The I2C controller provides bidirectional communication with other stacked die in a sensor node.

The receiver uses the non-coherent, energy-detection architecture shown in Fig. 25.2.2. Four RF gain stages amplify the 9.8GHz UWB pulses before downconverting with a squaring mixer. The signal then passes through a baseband gain stage before the signal path is split. Along one path, the pulses are passed directly to a comparator. The other path lowpass filters (LPFs) the signal to provide an auto-zeroed, DC-compensated reference level for comparison. A reset signal enables fast settling of the LPF for fast RX turn-on. Finally, a continuous-time latching comparator with controllable hysteresis digitizes the incoming pulses. BJTs are used for higher RF gain efficiency (g_m/I_C), while the RF gain stages are stacked in order to reuse current and better utilize the supply voltage. The RF center frequency is tunable via 4 binary-weighted control bits. After RF amplification, the signal is self-mixed to DC using a common emitter amplifier with resistive load as a squaring mixer.

To reduce both power and area, the radio includes a relaxation oscillator with a modified RC network and a single-ended hysteretic comparator for on-chip clocking (Fig. 25.2.3). The RC network adds an additional zero in the transfer function from *R2* over conventional relaxation oscillators, providing an additional degree of freedom for temperature compensation. As temperature increases, the initial step at *t=0* from the zero increases, but the time constant of the exponential decay also increases, offsetting the step and resulting in a constant time, *T*, to trigger the switching threshold, V_H, so that the overall period remains unchanged. The comparator consists of two stacked inverters with hysteresis levels set by *R3* and *R4*. Stacking the FETs reduces leakage power while the oscillator is asleep, and a 5b capacitor bank is added to the oscillator for one-time process calibration of frequency. The oscillator has a measured variation of 1% over a range of 0°C to 50°C that allows the TX and RX to be heavily duty-cycled between pulses in order to give the on-chip storage capacitor time to fully recharge and also sufficient accuracy to maintain network synchronization.

Transmitted pulses are generated by the combined VCO and PA shown in Fig. 25.2.4. An LC cross-coupled topology is chosen for fast turn-on time, and the transformer-coupled scheme boosts the signal swing delivered to the antenna. The area of the internal matching network between the VCO and PA is reduced by direct transformer coupling. The TX is enabled by the baseband controller through a digital pulse generator. The pulse generator has a 4b tuning range of 1.2ns to 6.0ns, and when enabled, the TX delivers a 700mV_{pp} pulse to a 50Ω load (Fig. 25.2.4). The center frequency is tuned via a 7b capacitor bank. The cross-coupled capacitors control the oscillating signal magnitude on the base terminals and are designed so that voltage swing never exceeds the breakdown voltage of the BJTs. While the TX is generating a pulse, the internal power supply voltage on the storage capacitor drops approximately 200mV due to current limiter protection. Between pulses, the storage capacitor recharges. The tail device is large, such that it enters the saturation region fast once the TX EN signal is high. A 60mA current is drawn from the VCO when it begins oscillating; however, due to the high on-to-off current ratio of the BJTs (>10^8), the sleep power of the TX is 170pW.

The radio was fabricated in 0.18μm BiCMOS with MIM capacitors. The PSD of the TX is shown in Fig. 25.2.5. The TX has a tuning range of 9 to 12GHz, and when tuned to 9.8GHz, the TX has a peak output power of 0.9dBm and satisfies the FCC mask. At a 30kb/s data rate, the average power of the TX is only 22.4μW at 3.6V. The magnitude response of the RX, shown in Fig. 25.2.5, is tuned to 9.8GHz. At a 10^{-3} BER, the RX has a sensitivity of -67dBm and a 30kb/s data rate while consuming an average of 37μW from a 3.6V supply with 6% duty-cycling (Fig. 25.2.5). The modem uses PPM and includes early/late tracking of pulses for each PPM window to maintain synchronization. At a 3MHz oscillation frequency, the entire baseband system consumes 269μW, of which the clock consumes 12.7μW. The CL has a 6-to-38μA tuning range (Fig. 25.2.5), which is sufficient for sustained operation of the TX and RX. The CL consumes only 223nW, yielding a 94% efficiency. Each block consumes <1nW while asleep by carefully including thick-oxide headers on all blocks, making this system ideal for heavily duty-cycled cubic-mm sensor nodes. A complete performance summary is provided in Fig. 25.2.6. The die occupies approximately 2.73mm^2, dominated by the modem (Fig. 25.2.7). The entire radio is designed to operate from just the 7 pads on the left edge to enable die stacking; the remaining pads are for debugging and may be left open.

Acknowledgements:
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References:
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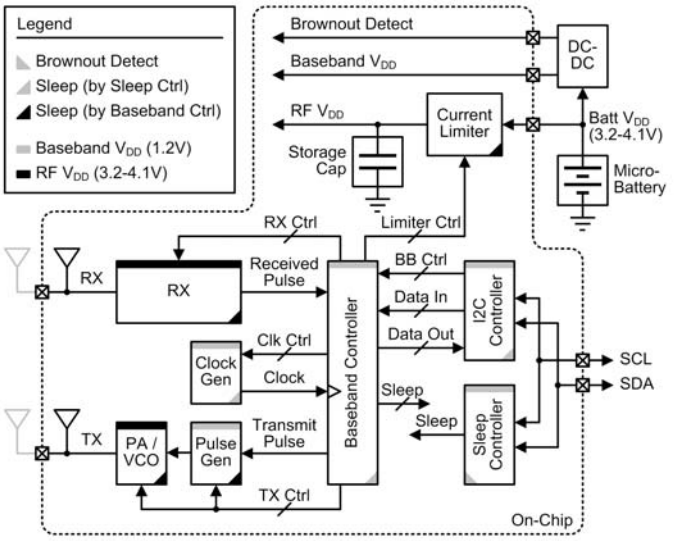

Figure 25.2.1: System block diagram of the entire crystal-less UWB radio.

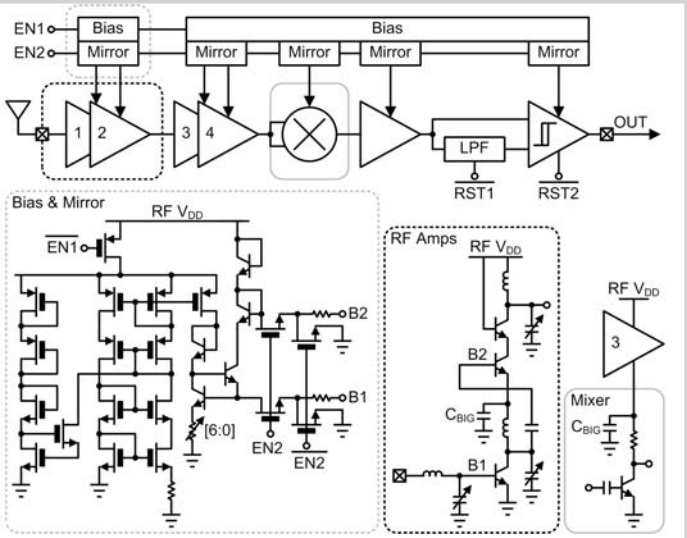

Figure 25.2.2: Receiver architecture along with schematics of biasing, two RF amplifiers, and the mixer.

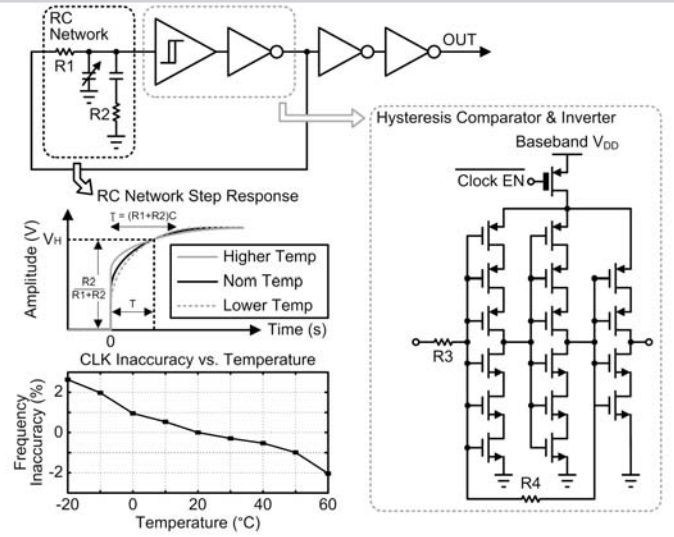

Figure 25.2.3: Schematic of the relaxation oscillator along with the step response of the RC network and measured frequency variation.

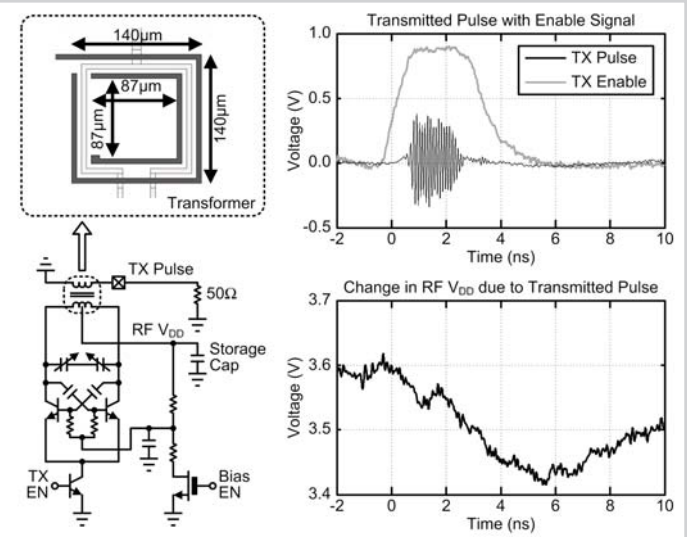

Figure 25.2.4: Schematic of the transmitter and the layout of the custom transformer along with a measured TX pulse.

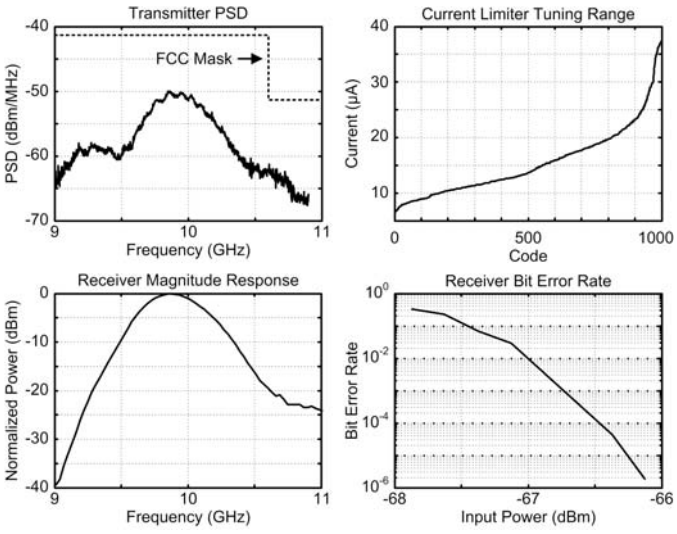

Figure 25.2.5: Highlighted measurement results of the transmitter, current limiter, and receiver.

General	Process	0.18µm BiCMOS
	Modulation	PPM
	Total Area	2.73mm^2
	Data Rate	30kb/s
	RF Voltage	3.2-4.1V
	Baseband Voltage	1.2V
	Sleep Power	1.0nW @3.6V 1.8nW @1.2V
Baseband System	Active Power	269µW @3MHz
	Clock	13µW @3MHz
	I2C & Sleep Ctrl	10µW
	Baseband Ctrl	246µW @3MHz
	Area	0.97mm^2
	Clock	0.04mm^2
	I2C & Sleep Ctrl	0.18mm^2
	Baseband Ctrl	0.75mm^2
Clock	Frequency	3MHz
	Supply Sensitivity	±1.5% @±4% V_{DD}
	Temp Sensitivity	±1.0% @0 to 50°C
	Temp Coefficient	-584ppm/°C

Receiver	Average Power	37µW @3.6V
	Sleep Power	347pW @3.6V
	Center Frequency	9.7-10.2GHz
	Area	0.61mm^2
	Sensitivity	-67dBm @10^{-3} BER
Transmitter	Average Power	22.4µW @3.6V
	Sleep Power	170pW @3.6V
	Center Frequency	9-12GHz
	Area	0.11mm^2
	Output Power	0.9dBm
	Pulse Width	1.2-6.0ns
Current Limiter	Active Power	223nW @3.6V
	Sleep Power	550pW @3.6V
	Area	0.04mm^2
	Output Current	6-38µA
	Temp Sensitivity	-34nA/°C
	Line Sensitivity	0.21µA/°C
	Efficiency	94% @3.6V

Figure 25.2.6: Summary of the radio performance.

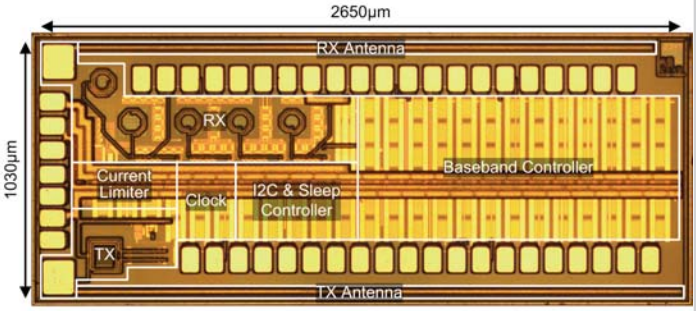

Figure 25.2.7: Die photo.

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