A 1900MHz-Band GSM-Based Clock-Harvesting Receiver with -87dBm Sensitivity

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***Abstract* — A 0.13µm CMOS clock-harvesting receiver is presented which extracts a 21Hz clock embedded within the GSM standard for the wake-up of a wireless sensor network. In active mode, the receiver achieves -87dBm sensitivity with 57µs of jitter at the output while consuming 126µW. The receiver is optimized for heavy duty-cycling with a sleep-mode power consumption of only 81pW.**

***Index Terms* — Analog integrated circuits, GSM, wireless sensor networks, wake-up receiver, clock-harvesting receiver.**

I. Introduction

Wake-up receivers (WRXs) are used in wireless sensor networks (WSNs) to conserve node energy. They allow the nodes in a WSN to operate in a low-power sleep mode and use a wireless signal to wake the nodes up. A traditional WRX remains on continuously during sleep mode, waking-up the node after a signal is broadcast *within* the WSN [1]-[2].

Unlike traditional WRXs, this paper presents a clock-harvesting receiver (CRX). It is designed to extract a 21Hz signal embedded within every broadcast channel (BCH) of the GSM mobile phone standard for the wake-up of a WSN. The CRX wakes up a node based on an *external* GSM signal, eliminating the need for a high-power synchronization beacon generated within the energy-constrained WSN. Furthermore, this CRX is designed with a <100pW sleep mode to enable a hierarchical synchronization strategy. This allows the CRX to be coarsely duty-cycled (for example by an on-node <1nW program-and-hold timer [3]), and fully-powered only momentarily around the 21Hz GSM clock edges. By aligning each node to the arrival of the next GSM-harvested clock edge, the entire WSN is synchronized and may selectively enable communication radios based on higher-layer network policies.

This work presents the entire design of a fully-characterized CRX starting in Section II with a discussion of the requirements for a wake-up source and the system architecture of the CRX. In Section III, we describe the circuit topologies used in the receiver and then report measured results in Section IV. Finally, we conclude with a demonstration of the CRX extracting a clock from a local GSM cell signal.

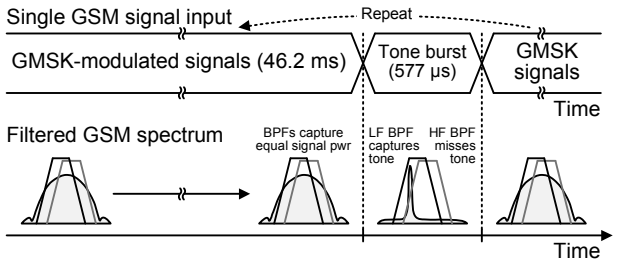

Fig. 1. Method of operation in time. Lower-frequency (LF) and higher-frequency (HF) BPFs perform sub-channel selection.

II. System Overview

This section provides an overview of GSM-based synchronization, the system operation of the CRX and its architecture, and intermediate frequency selection.

A. GSM-Based Synchronization

GSM was selected as a wake-up source because it provides a pervasive and practical signal for use in a WSN. Only one broadcast channel exists per provider per GSM cell, and that channel operates at a dedicated frequency. Furthermore, channels in neighboring cells are allocated frequencies that minimize adjacent-channel interference, simplifying filter requirements. Based on RSSI measurements throughout our 5-story building, the typical received power of a BCH ranges from -65dBm to -95dBm, with the strongest being in the 1900MHz band.

B. System Operation

Fig. 1 outlines the operation of the receiver in time. The GSM standard employs Gaussian minimum-shift keying (GMSK) and other modulation schemes with pseudo-GMSK spectrums to modulate bursts of data in time [4]. Approximately every 46ms, a pure sinusoidal tone is transmitted on the GSM broadcast channel. This tone burst lasts for 577µs at an offset frequency of 67.7kHz from the center of the channel; otherwise, data is transmitted with a spectrum occupying the entire 200kHz channel. The bandpass filters (BPFs) in the CRX are tuned to overlapping halves of this BCH. When data is transmitted by a GSM cell, power is spread over the entire

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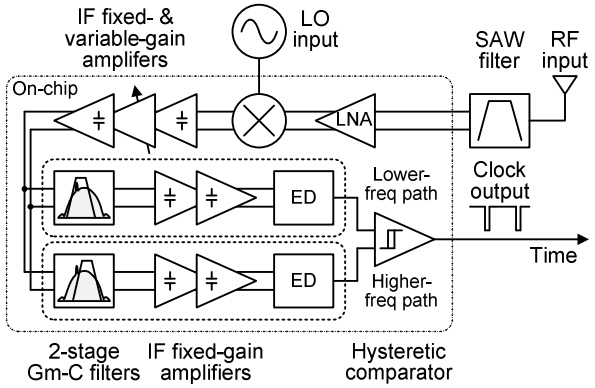

Fig. 2. Block diagram of the clock-harvesting receiver.

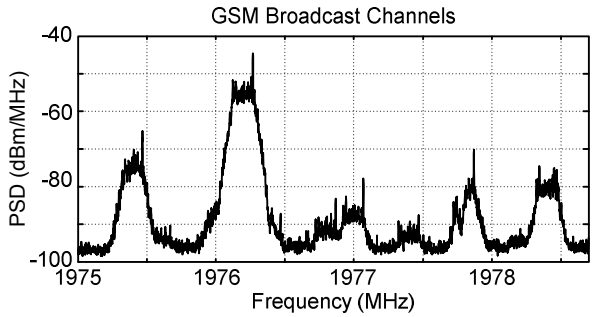

Fig. 3. Measured GSM broadcast channel separation.

channel, passing equal signal levels through each BPF. During a tone burst, however, the signals captured along the two filter paths differ. At the envelope detector (ED) outputs, this difference in signal powers results in a voltage difference greater than the hysteresis level on the comparator, toggling the comparator output.

C. System Architecture

Fig. 2 outlines the system architecture of the proposed CRX (clock-harvesting receiver). An off-chip SAW filter selects the entire 1900MHz PCS band, such that any GSM broadcast channel operating in the band can serve as a clock source. The input is amplified and down-converted to an intermediate frequency (IF) of 250kHz. Channel selection is done by using different fixed LO frequencies and filtering at IF. Fixed- and variable-gain amplifiers at IF provide gain control. Following amplification, the signal is split into two paths, each with two Gm-C BPF stages that perform sub-channel selection. Each path then amplifies and envelope detects the signal. The voltages at the output of each ED are applied to a hysteretic comparator, generating a digital clock output from the harvested GSM signal.

D. Intermediate Frequency Selection

In a typical cellular network, the strongest channels in one geographic location do not sit in adjacent frequency

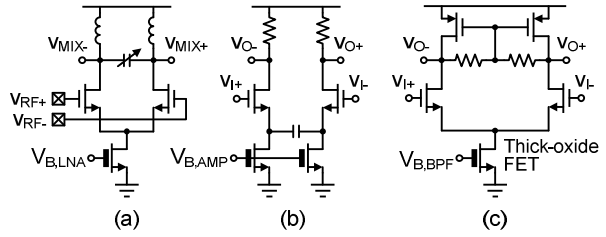

Fig 4. Schematic of the (a) LNA, (b) IF amplifier, and (c) Gm amplifier. Each stage has a thick-oxide tail FET for low leakage currents.

channels (Fig. 3). Based on lab measurements, the worst case is an 800kHz separation between high-power channels; thus, a low IF of 250 kHz was selected. The IF is low enough so that the image created from down-conversion lies in a low-power adjacent channel. A low IF also lowers the quality factor requirements on the BPFs, decreasing power consumption. At the same time, the IF is high enough such that flicker noise remains low.

III. Circuit Design

The clock-harvesting receiver consists of circuits that provide four primary functions: band selection and down-conversion, gain, clock detection, and sleep-power minimization.

A. Band Selection & Down-Conversion

A SAW band-select filter provides single-to-differential conversion and AC-couples directly to an un-matched fully-differential LNA with inductive loading (Fig. 4a). The inductors are sized to maximize their impedance in the band-of-interest, and a varactor was added in order to tune center frequency. The varactor is sized to account for process variation while still passing every channel in the 1900-MHz band. The LNA is AC-coupled to a double-balanced Gilbert mixer. The entire front-end is fully-differential in order to shut-off bias currents in sleep mode and provide common-mode rejection. The LO is generated off-chip and is used to select the desired GSM broadcast channel. The BPFs at IF have a measured tuning range that allows for up to 161ppm in frequency drift from the LO while still maintaining proper receiver functionality. A low-power FBAR-based LO should be able to meet these requirements by selecting a FBAR to target a specific GSM channel [5].

B. Low-Power & Variable Gain

To reduce active power in the receiver, the system has only one RF gain stage before mixing down to a low IF. Once the signal is at IF, amplification is provided by four differential fixed-gain amplifiers and one variable-gain

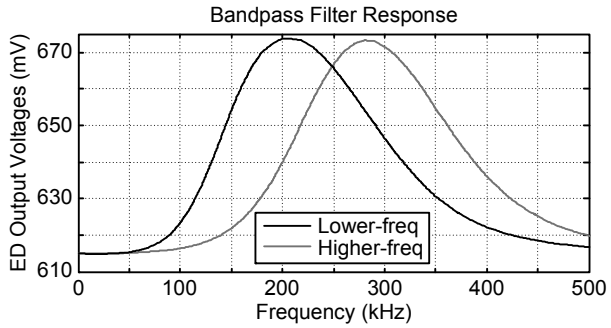

Fig. 5. Magnitude response of the bandpass filters.

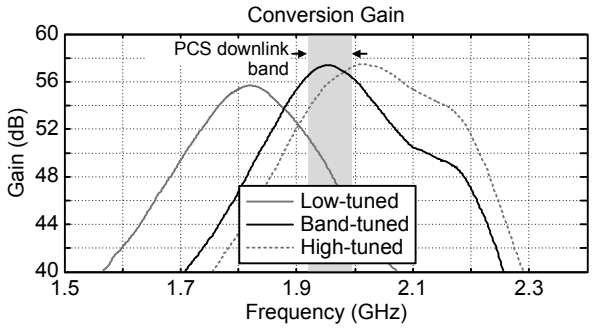

Fig. 6. Conversion gain for different tunings of the varactor.

amplifier (VGA). Each fixed-gain amplifier has a split-source topology with capacitive-coupling (Fig. 4b) [1],[6]. The capacitive-coupling eliminates accumulated offset voltages, so that common-mode feedback is not necessary.

The VGA circuit is a differential amplifier with split-tail current. The topology is based on an unfolded version of [7]. The topology provides a large input tuning range, so that fixed off-chip voltage tuning can provide stable on-chip gain.

C. Clock Detection

To detect the clock embedded in the GSM standard, the amplified IF signal is split into two paths: lower- and higher-frequency paths. Each signal path has a 2-stage Gm-C BPF tuned to overlapping halves of a GSM channel.

Each Gm-C stage consists of a differential 2nd-order filter with unit transconductors for better matching. The unit transconductors consist of differential pairs with PMOS load and resistive CMFB (Fig. 4c). The capacitors in each path and stage are sized to provide a Butterworth response, and unit MIM capacitors are used for better matching. The magnitude response of each BPF is tuned to equalize the received power through overlapping halves of the GSM channel during data bursts and to maximize received power differences during tone bursts.

The bandwidths of the BPFs along the lower- and higher-frequency paths are 121kHz and 118kHz, respectively. They are optimally determined by system simulations to minimize the clock error rate (CER), defined as the number of clock errors to the number of correct clock outputs (Fig 5) [8]. Additionally, the use of two wideband filters decreases quality factor requirements over the detection method proposed in [8], reducing the power required to filter the GSM channel.

To eliminate instantaneous differences at the output of the EDs, the two paths are capacitively-coupled together. The received signal powers through each path are then compared using a 2-stage continuous-time comparator with controllable hysteresis from four digital control bits.

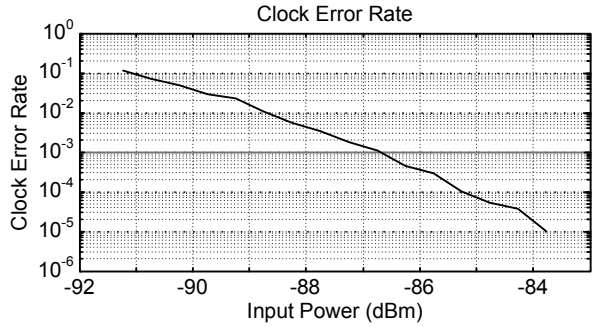

Fig. 7. Clock error rate vs. input power.

D. Sleep-Power Minimization

In heavily duty-cycled operation, sleep-mode energy dominates active-mode energy. Thus, thick-oxide tail devices were added to every stage in the receiver in order to minimize sleep-mode leakage currents (Fig. 4). Using thick-oxide tail devices, however, increases active-mode energy due to the larger headroom requirements for the high-threshold voltage devices. Thus, sizing of the thick-oxide devices was done to maximize the ratio between active-mode and sleep-mode current.

IV. Measurement Results

The clock-harvesting receiver was fabricated in 0.13µm CMOS with MIM capacitors. The entire receiver operates from a single 1V supply. The conversion gain of the CRX is shown in Fig. 6 at three differently tuned varactor voltages in the LNA. The peak conversion gain measured at sensitivity is 57dB, and gain-control is achieved by tuning the VGA and the tail bias currents of each stage. The LNA can be tuned over a frequency range of 1.82 to 2.03GHz, which completely covers the 1900MHz band, enabling the selection of any broadcast channel in the US.

The measured CER (clock error rate) is shown in Fig.7. At a CER of 10^{-3}, the peak sensitivity is -87dBm with a total power consumption of 126µW, of which the front-end consumes 98µW and the baseband consumes 28µW. At a reduced sensitivity of -60dBm and 10^{-3} CER, the total

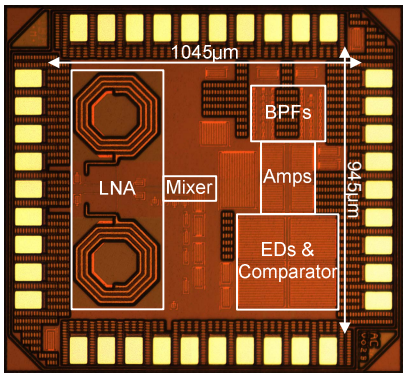

Fig. 8. Die micrograph.

power consumption of the receiver can be reduced to 67µW. Proper operation was verified at input powers up to -5dBm. The measured jitter at peak sensitivity is 57µs, but this reduces to 2µs at higher input powers. In sleep mode, the leakage power of the system is just 81pW. The start-up time from sleep mode to active mode is roughly 500µs, limited by slewing at the ED outputs.

The measured signal-to-interference ratio (SIR) is -7dB at a CER of 10^{-3} for an interfering channel centered 800kHz above the desired channel (expected worst-case interferer). Thus, the clock embedded in the highest power broadcast channel always can be harvested, assuming a typical GSM channel allocation policy. The core circuit area occupies approximately 0.99mm^2 (Fig. 8), and a harvested clock output from the CRX is shown in Fig. 9 from the 1976.2MHz GSM broadcast channel of a local tower. A performance summary is provided in Table 1 along with a comparison to recent WRXs.

Table 1. Measured receiver performance and comparison.

	This Work		[1]	[2]	[6]
Process	0.13µm		90nm	90nm	65nm
Type of RX	Clock-harvest		Wake-up	Wake-up	Wake-up
V_{DD}	1.0V		0.5V	0.5V	1.2V
Area	0.99mm^2		0.1mm^2	0.36mm^2	0.2mm^2
Sensitivity	-87dBm		-72dBm	-80dBm	-87dBm
P_{Active} | P_{Sleep}	126µW	81pW	52µW	51µW	415µW
$P_{Front-End}$	98µW	56pW	8µW	51µW	199µW
$P_{Baseband}$	28µW	25pW	24µW		
LO Accuracy	161ppm		10^5ppm	N/A	5x10^3ppm

V. Conclusion

A clock-harvesting receiver is presented that is capable of extracting a 21Hz clock embedded within the GSM standard for the wake-up of a wireless sensor network. The advantage of this approach is that the signal is pre-existing and pervasive; therefore, the WSN does not have to generate it. Measurements show that the receiver achieves -87dBm sensitivity while consuming only 126µW. In sleep-mode, the power consumption is 81pW. Functionality of the CRX was verified by extracting a clock from the broadcast channel of a local cell tower.

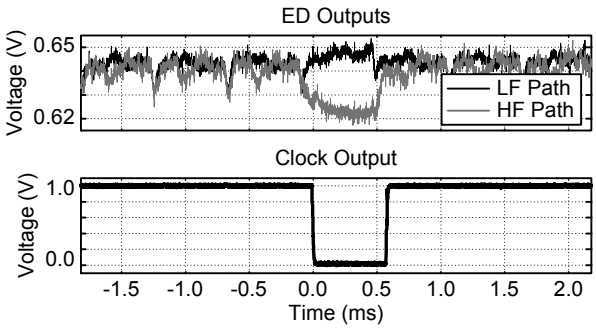

Fig. 9. Harvested-clock from a local GSM broadcast channel.

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References

[1] N. Pletcher, S. Gambini, and J.M. Rabaey, "A 2GHz 52µW Wake-Up Receiver with -72dBm Sensitivity Using Uncertain-IF Architecture," *ISSCC Dig. Tech. Papers*, pp. 524-525, 633, Feb. 2008.

[2] X. Huang, et al., "A 2.4GHz/915MHz 51µW Wake-Up Receiver with Offset and Noise Suppression," *ISSCC Dig. Tech. Papers*, pp. 222-223, Feb. 2010.

[3] Y-S. Lin, D. Sylvester, and D. Blaauw, "A 150pW Program-and-Hold Timer for Ultra-Low Power Sensor Platforms," *ISSCC Dig. Tech. Papers*, pp. 326-327, Feb. 2009.

[4] European Telecommunications Standards Institute, *Global System for Mobile Communications*, Tech. Spec., 145 Series, v. 8.0.0.0, Release 8, Feb. 2009.

[5] Y.H. Chee, A.M. Niknejad, and J. Rabaey, "A Sub-100µW 1.9-GHz CMOS Oscillator Using FBAR Resonator," *IEEE RFIC Symp.*, pp. 123-126, Jun. 2005.

[6] S. Drago, et al., "A 2.4GHz 830pJ/bit Duty-Cycled Wake-Up Receiver with -82dBm Sensitivity for Crystal-Less Wireless Sensor Nodes," *ISSCC Dig. Tech. Papers*, pp. 224-225, Feb. 2010.

[7] C.-H. Wu, C.-S. Liu, and S.-L. Liu, "A 2GHz CMOS Variable-Gain Amplifier with 50dB Linear-in-Magnitude Controlled Gain Range for 10GBase-LX4 Ethernet," *ISSCC Dig. Tech. Papers*, pp. 484-485, 541, Feb. 2004.

[8] J.K. Brown and D.D. Wentzloff, "Harvesting a Clock from a GSM Signal for the Wake-Up of a Wireless Sensor Network," *IEEE Intl. Symposium on Circuits and Systems*, pp. 1500-1503, Jun. 2010.