A Clock-Harvesting Receiver Using 3G CDMA Signals in the 1900-MHz Band

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***Abstract*—A clock-harvesting receiver is presented, which extracts a 1.2-kHz clock embedded within the third-generation code-division multiple-access standard for the wake-up of a wireless sensor network. The energy-detection-based receiver was fabricated in 0.13-μm CMOS and designed for low-power heavily duty-cycled operation. In active mode, the receiver has a measured sensitivity of −73 dBm while consuming only 298 μW. The harvested-clock output has 7 μs of root-mean-square jitter at the sensitivity level, which improves with higher received power. In sleep mode, the receiver consumes only 44 pW with a start-up time of 80 μs.**

***Index Terms*—Analog integrated circuits, code-division multiple access (CDMA), clock-harvesting receiver (CRX), synchronization, wake-up receiver (WRX), wireless sensor networks (WSNs).**

I. Introduction

SOCIETY has been a witness and a participant in an ongoing computing revolution as new classes of computing technology have displaced older technologies as the dominant market force, i.e., from mainframes decades ago to smartphones today. With the rise of each new class, the systems have become smaller and more ubiquitous than their predecessors [1]. As this trend continues, wireless sensor networks (WSNs) are widely perceived as the next major class of computing technology. WSNs have garnered interest for a variety of potential applications, including infrastructure and health monitoring [2], [3]. These applications, however, require sensor nodes with both long lifetimes and small volumes, which results in highly energy-constrained systems. To alleviate this problem, energy usage must be reduced in the sensor node. In particular, the energy used by the communication radio and the system clock can easily dominate the overall system energy usage in continuous operation. Since both components maintain synchronization across the WSN, reducing their power consumption can greatly improve node lifetime [4].

After a discussion of several different synchronization techniques in Section II, this brief then discusses the design and measurements of a fully characterized clock-harvesting receiver (CRX) for synchronizing a WSN from an existing wireless standard. Section III presents a system overview, which includes a discussion of the code-division multiple-access (CDMA) standard, the operation of the receiver, and its architecture. Section IV then describes important circuit design decisions before presenting the measured results in Section V. Finally, this brief is concluded in Section VI.

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II. Synchronization Techniques

The standard approach to reducing synchronization energy in a low-power wireless device is to duty-cycle the communication radio and to schedule communications using a high-accuracy on-node timer. The Bluetooth Low Energy standard, for example, uses this technique to reduce communication intervals between a central device and a peripheral device to as low as 31 mHz [5]. ZigBee also employs a similar technique in beacon-enabled personal area networks (PANs) so that peripheral devices can duty-cycle their radio [6]. Unfortunately, high-accuracy timers still consume considerable power, which mitigates some of the energy savings that might be expected by duty-cycling the radios.

Another standard approach is to eliminate scheduling completely. For example, ZigBee permits nonbeacon-enabled PANs that follow this procedure [6]. The coordinator remains on continuously so that the peripheral device can remain off until it wishes to wake up and transmit data to the coordinator. This approach eliminates synchronization overhead, but it assumes an asymmetric communication link since the coordinator must remain on continuously. In addition, this approach is not feasible for peer-to-peer networks. Therefore, alternative approaches have been proposed.

An alternative solution is to replace constant on-node high-accuracy timing with network-wide synchronization using a wake-up receiver (WRX) [7], [8]. Unlike traditional receivers, WRXs do not continuously communicate with other nodes; instead, they simply monitor the wireless channel for a high-power beacon signal. Because WRXs are designed to detect simple high-power beacons, the receivers can be low power, and the rest of the node can remain asleep. When a wake-up signal is sent over the WSN, all of the nodes can detect this synchronization event and communicate with one another as part of higher network policies [see Fig. 1(a)]. As a result, a WRX enables fully asynchronous interrupt-based communication.

Unfortunately, a WRX assumes that a high-power wake-up beacon is readily available, which can be detected across the entire WSN. For applications spanning large distances such as structural health monitoring on bridges [2], this may be unreasonable for the energy-constrained network. Therefore, it would be advantageous to use a WRX for interrupt-based communication while eliminating the need to broadcast the wake-up beacon from within the energy-constrained WSN. Fortunately, with

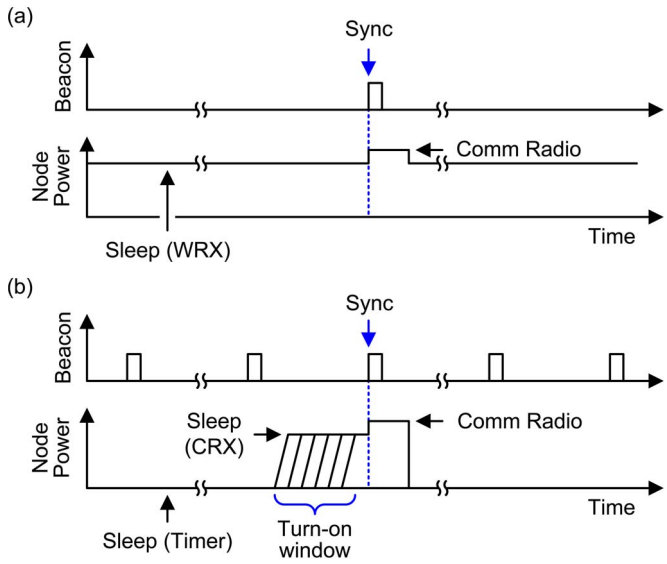

Fig. 1. Two different network synchronization strategies. (a) Single wake-up beacon that requires an always-on WRX. (b) Intermittent clock beacon that permits a duty-cycled CRX.

the pervasiveness of modern wireless standards, a WRX can instead harvest a digital clock from an existing wireless standard such as Wi-Fi, broadcast television (TV), or cellular signals. We call this a CRX. If all nodes in a WSN harvest and synchronize to the same existing wireless signal, by transitivity they will be synchronized to each other. Furthermore, TV and cellular signals are broadcast at high power from antennas placed high above ground. Therefore, the signals span long distances and can be used to synchronize very sparse WSNs.

If possible, however, we would like to reduce synchronization energy even further by employing the CRX as part of a hierarchical synchronization strategy. Instead of leaving the CRX on continuously like a WRX, we can duty-cycle the CRX with a less-accurate subnanowatt timer [9]. Thus, the CRX is on only around incoming clock edges, whereas the CRX remains asleep if otherwise [see Fig. 1(b)]. The subnanowatt timers in the WSN only need to be sufficiently accurate to ensure a turn-on window between two harvested-clock beacons. In addition, the receiver must be designed with a low-power sleep state that does not dominate the timer power.

This brief presents the first CRX designed to harvest a 1.2-kHz clock embedded within the idle slot of the 3G CDMA mobile phone standard. Unlike the Global System Mobile Communications (GSM) CRX that we previously reported in [10], this receiver does not require a local oscillator (LO) to extract the CDMA-based clock, providing a complete circuit solution. Like the previously published CRX, the receiver is designed to be coarsely duty-cycled and only awoken momentarily around the incoming clock edges from the CDMA broadcast. With a harvested-clock edge, the nodes in the WSN are synchronized and may selectively enable communication radios based on higher layer network policies.

III. System Overview

This section describes the relevant attributes of the 3G CDMA standard that are utilized in the operation of this CRX.

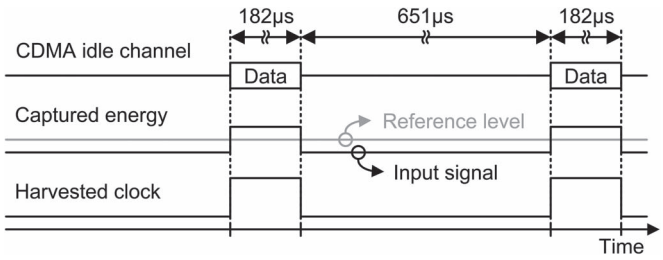

Fig. 2. CDMA signaling and clock extraction versus time. Data during idle slots in the 3G CDMA standard is on–off keyed.

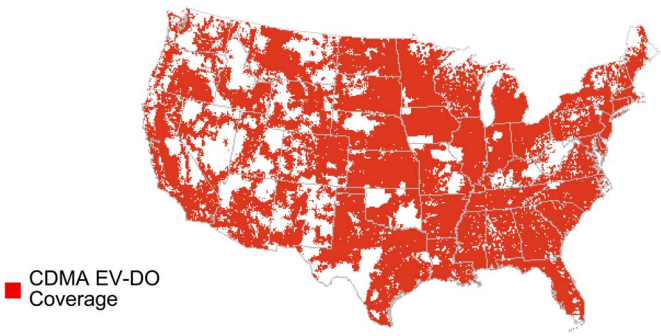

Fig. 3. Verizon Wireless 3G CDMA U.S. coverage map in 2011 [13].

This section then provides an overview of the system architecture employed to harvest a clock from the standard.

A. System Operation

This receiver extracts a clock from the 3G CDMA standard for the wake-up of a WSN. The 3G CDMA standard, formally known as the CDMA2000 Evolution-Data Optimized family of standards, uses a pseudorandom code to spread the transmitted signal into 1.25-MHz channels [11]. Power is adjusted on the broadcast side to ensure a constant channel power, simplifying receiver detection. The standard employs time-division multiplexing, dividing channels into slots (see Fig. 2). During idle slots, medium access control (MAC) and pilot data are the only information transmitted, and no user data is transmitted. Thus, the channel looks like an on–off keyed signal with an on period of 182 μs and an off period of 651 μs. A digital output pulse then can be generated by capturing the energy in the channel over time and by comparing it with a reference level. Because slots run continuously on the CDMA channel, a sequence of digital pulses is seen at the output, creating a 1.2-kHz clock. When users are present, the active slots assigned to a user are interpolated so that idle slots exist even on an occupied channel. Thus, only channels at full utilization do not have idle slots. Fortunately, this event is extremely rare because it is not also desired by the wireless carrier.

The 3G CDMA standard is a pervasive signal, making it a good option for sensor network wake-up. Seven major bands exist worldwide, including the 850- and 1900-MHz bands in the U.S. The 1900-MHz band was selected for this CRX based on signal strength measurements in our laboratory. Many major worldwide markets have 3G CDMA coverage, including the U.S., China, and India. The U.S. coverage map for 3G CDMA from Verizon Wireless is shown in Fig. 3.

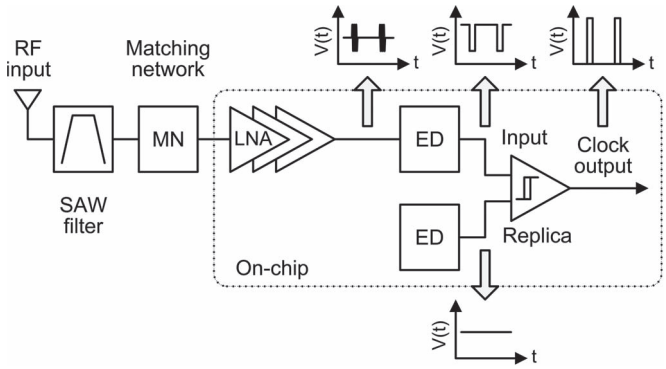

Fig. 4. Block diagram of the CRX.

B. System Architecture

The proposed CRX has the system architecture depicted in Fig. 4. The received signal is passed through an off-chip filter, which selects the desired portion of the 1900-MHz Personal Communications Service (PCS) band. The single-ended signal then is sent through a matching network and onto the chip. Next, the signal goes through three cascaded RF amplifiers, which can be tuned to provide gain control. After amplification, the signal is downconverted directly to dc using an envelope detector (ED). The ED along the main signal path provides the input to the hysteretic comparator, whereas a replica ED provides the reference signal. The comparator output is a digital clock harvested from a 3G CDMA signal.

C. Nonlinear Downconversion

The receiver architecture is nonlinear, which eliminates the need for an accurate high-power LO at RF and an external crystal. At the same time, nonlinear downconversion requires large RF signals before squaring to stay above the noise. Thus, nonlinear architectures require more RF gain over linear architectures to achieve similar sensitivities for gain-limited systems. By eliminating the external crystal, however, this CRX has a complete circuit solution that consumes a smaller volume.

D. Frequency Selection

A narrow-band filter with a high quality factor is required for the proper functionality of this receiver. The filter must select only the desired 3G CDMA channels while rejecting all other channels in the 1900-MHz band to prevent saturation of the front end. Based on laboratory measurements for our area, the desired 3G CDMA channels make up an entire block of spectrum defined by the Federal Communications Commission in the PCS band. Thus, the filter can be relatively wideband and realizable while still rejecting interfering signals within the band-like GSM channels.

While this architecture does place significant requirements on the filter, there are several advantages to this approach. First, the filter itself can be passive, requiring no power from the energy-constrained node. Second, an energy-detection-based receiver eliminates the need for an LO, which is required in [10]; therefore, a filter is the only additional component required. Finally, typical RF systems often require off-chip filtering anyway to prevent saturation of the receiver front end, leaving node complexity unchanged.

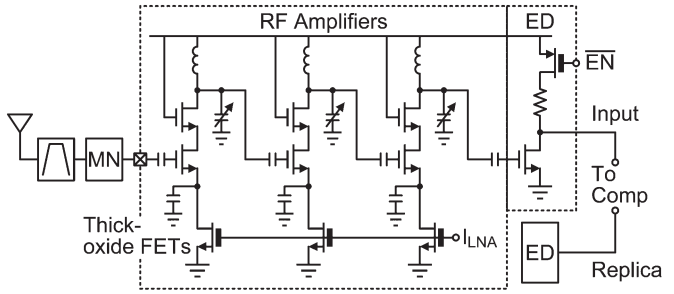

Fig. 5. Schematic of the cascoded RF amplifiers and the EDs. Every current path includes a thick-oxide tail FET for low leakage currents while asleep.

IV. Circuit Design

The circuits in this CRX have four major functions: RF gain, downconversion, clock detection, and sleep-power minimization.

A. Block Selection and RF Gain

An external filter selects the desired block of spectrum before sending the signal to a matching network and then on-chip. The matching network maximizes the power delivered to the receiver and provides additional channel selectivity over typical on-chip solutions. The network consists of a series capacitor and a shunt inductor. Once the signal arrives on-chip, it is ac-coupled directly to the input of a single-ended RF amplifier with LC load. The input amplifier is one of three identically sized RF amplifiers that together provide the RF gain for the receiver. The amplifiers are cascoded to reduce Miller effects at the input node of each stage and reduce feedthrough between stages. A single-ended implementation is employed to save power. Current biasing is accomplished with the use of thick-oxide tail FETs for low leakage current in sleep mode. To prevent gain degeneration in the RF amplifiers, capacitors were added to create an ac-short across the biasing FETs. The LC load is implemented with a varactor to provide frequency tuning.

B. Downconversion

The receiver directly downconverts the RF signal to dc using an ED for energy detection (see Fig. 5). The ED is implemented using a single-ended common-source amplifier, and downconversion is achieved by utilizing the inherent squaring relationship found in the drain current expression, where $i_D \propto v_{GS}^2$. The squaring effect results in direct conversion to dc. For duty-cycled operation, a thick-oxide header is placed above the load resistor. When the receiver is on, the header adds finite resistance; however, this on-resistance is small relative to the load resistance so that it has no effect on performance. When the receiver is asleep, however, the thick-oxide FET is turned off and the header stops the current flow to reduce sleep-mode power consumption.

C. Clock Detection and Harvesting

The downconverted signal is sent into a two-stage continuous-time comparator with hysteresis for clock harvesting (see Fig. 6). Two additional inverters buffer the output and drive the clock off-chip. The comparator inputs are set

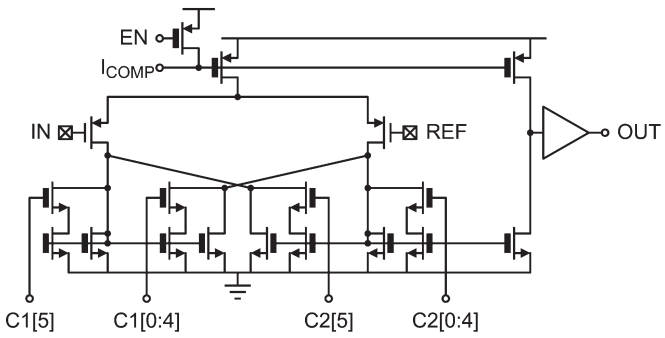

Fig. 6. Schematic of the continuous-time comparator with hysteresis.

by matched EDs to ensure equal input voltages, and large capacitors are placed on the input nodes of the comparator to prevent spurious switching at the output. The replica ED, the comparator, and the output buffer all use thick-oxide FETs to minimize power consumption while asleep. The comparator is disabled in sleep mode by pulling I_{COMP} to the positive supply rail with a PMOS keeper. The hysteresis levels are tunable from 12 digital control bits that are connected to pads for off-chip calibration.

D. Sleep-Power Minimization

This receiver is designed to operate as part of a tiered synchronization strategy along with a low-power timer. When the CRX is heavily duty-cycled, however, sleep-mode energy dominates active-mode energy. Thus, thick-oxide tail devices were added to every stage in the receiver to minimize sleep-mode leakage currents (see Fig. 5). Using thick-oxide tail devices, however, increases active-mode power by more than 20% due to the additional headroom requirements for high-threshold voltage devices. Thus, sizing of the thick-oxide devices was done to maximize the ratio between active-mode and sleep-mode currents.

V. Measurement Results

The CRX was fabricated in a 0.13-μm CMOS process with varactors, metal–insulator–metal capacitors, and inductors. The conversion gain of the receiver with an external matching network is plotted versus frequency in Fig. 7 at three different input power values. Due to the nonlinear downconversion of the ED, the gain through the receiver varies with input power. The S11 of the receiver is better by -10 dB in the 1900-MHz band due to the matching network, and the center frequency of the receiver is tuned to maximize gain in the 1900-MHz band. Consequently, it is tuned to the upper edge of the band. With an input signal of -50 dBm, the peak conversion gain is 37 dB.

The clock error rate (CER) of the CRX is shown in Fig. 8, where the CER is defined as the number of clock errors divided by the expected number of clock outputs. At 10^{-3} CER, the sensitivity is -73 dBm based on the average measured power of an idle slot using an Agilent U2000A power sensor. More specifically, the received power is -67 dBm during the 182 μs of pilot and MAC data followed by 651 μs of no received signal power (see Fig. 2) per the 3G CDMA standard, yielding an average received power of -73 dBm. The CRX has a total power consumption of 298 μW. The front end consumes 295 μW

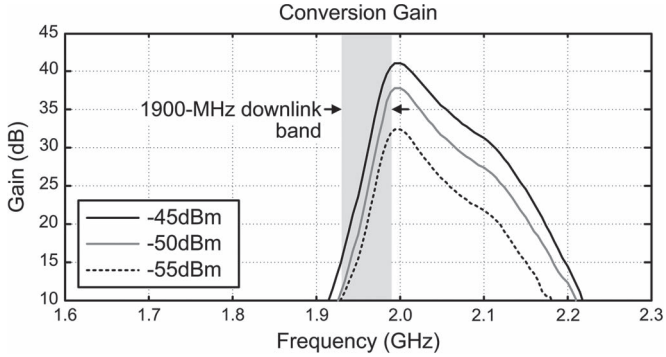

Fig. 7. Conversion gain for different receive power values.

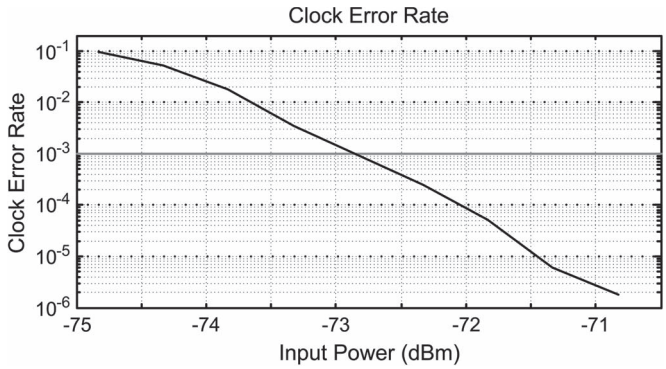

Fig. 8. CER versus input power.

or slightly greater than 98 μW per RF gain stage, assuming that there is no mismatch. The EDs and the comparator, meanwhile, consume 2.3 and 0.5 μW, respectively. The measured root-mean-square jitter at peak sensitivity is 7 μs and the delay through the receiver is 27 μs.

The CRX power consumption can be adjusted using the tail bias currents of the RF gain stages. As power consumption varies, the gain and sensitivity of the receiver also vary due to the nonlinearity of the squaring mixer (see Fig. 9). Furthermore, the receiver is gain limited; therefore, the gain and sensitivity scale together. The black curve in Fig. 9 is the measured gain of the receiver as power consumption varies. This curve also represents the expected sensitivity of the CRX for the same power consumption. Sensitivity was measured at four different power levels marked by the gray boxes. Thus, the desired tradeoff between power consumption, gain, and sensitivity for a particular usage model can be determined using Fig. 9. Using these measurement results, a closed-form expression was empirically determined to predict receiver sensitivity S with an R^2 value of better than 0.99, by varying the power P consumed by the CRX, as shown in the following:

$$S = -24.52\ln(P) + 66.7 \tag{1}$$

where P is in microwatts and S is in decibel-milliwatts.

Proper operation was verified at input power up to -4 dBm, which corresponds to the maximum deliverable power from our vector signal generator. The measured leakage power of the system is just 44 pW in sleep mode and the start-up time from sleep mode to active mode is approximately 80 μs.

The receiver operates from a single 0.75-V supply and the core circuits occupy approximately 0.89 mm^2 (see Fig. 10).

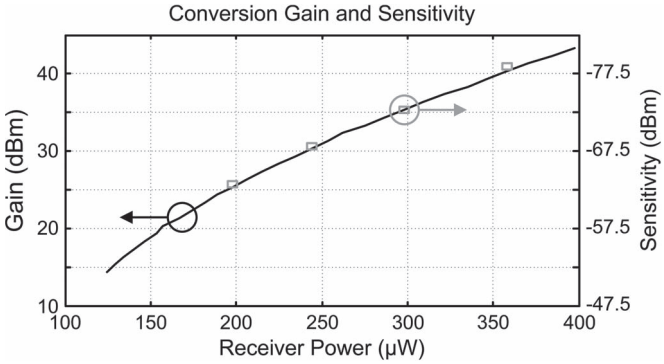

Fig. 9. Receiver gain and sensitivity at 10^{-3} CER versus active power.

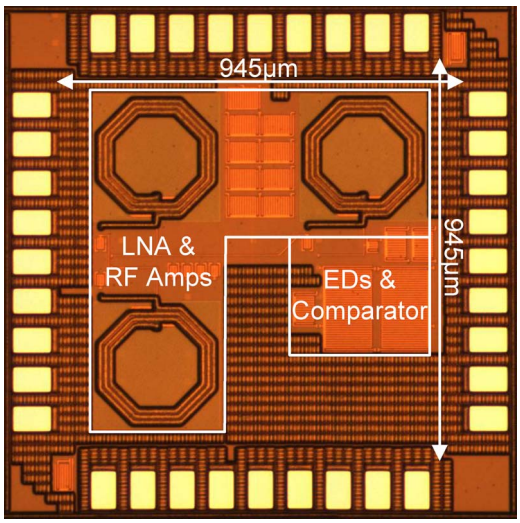

Fig. 10. Die photo.

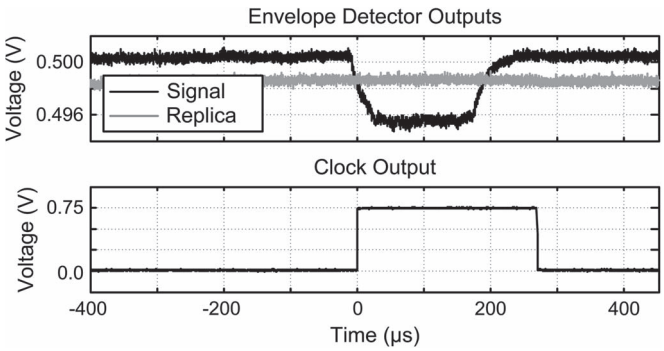

Fig. 11. Harvested-clock from a 3G CDMA channel.

The comparator hysteresis levels can be configured via six bits for each edge transition that ensures small enough steps to maximize performance while still providing large steps to account for mismatch. The levels can be varied from -12 to $+28$ and -9 to $+32$ mV on the positive and negative edge transitions, respectively. These hysteresis tuning ranges can account for mismatch across multiple dies based on simulation results. A harvested-clock output from the CRX is shown in Fig. 11, along with the ED voltage outputs.

The measured receiver performance is summarized in Table I, and when compared with these recent works, this CRX would require less total energy for synchronization, assuming heavily duty-cycled operation due to its low sleep power.

TABLE I
MEASURED RECEIVER PERFORMANCE AND COMPARISON

	This Work		[7]	[10]	
Process	0.13μm		90nm	0.13μm	
Type of RX	Clock-harvest		Wake-up	Clock-harvest	
V_{DD}	0.75V		0.5V	1.0V	
Area	0.89mm^2		0.1mm^2	0.99mm^2	
Sensitivity	-73dBm		-72dBm	-87dBm	
P_{Active}| P_{Sleep}	298μW	44pW	52μW	126μW	81pW
$P_{Front-End}$	295μW	39pW	8μW	98μW	56pW
$P_{Baseband}$	3μW	5pW	24μW	28μW	25pW
LO Accuracy	N/A		10^5ppm	161ppm	
Start Time	80μs		Unknown	500μs	

VI. CONCLUSION

A CRX has been presented, which is designed to wake up and synchronize a WSN by extracting a 1.2-kHz clock embedded within the 3G CDMA standard. With a CRX, the wake-up source is preexisting and pervasive; thus, the signal does not have to be generated within the WSN, saving energy. This CRX does not require a high-frequency LO, which simplifies the receiver design and further saves node energy. Based on measurement results, the CRX consumes only 298 μW and has a sensitivity of -73 dBm at a CER of 10^{-3}. The power consumption can be tuned to optimize performance. In sleep mode, the power consumption is only 44 pW.

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