A 300nW Near-Threshold 187.5 - 500 kHz Programmable Clock Generator for Ultra Low Power SoCs

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***Abstract* — We present a 187kHz to 500kHz ADPLL-based clock generator that consumes 300nW from a 0.5V VDD, has a jitter <0.1% and was implemented in a 0.13µm CMOS process. The entire ADPLL was implemented using standard digital design flows and automatic place and route (APR). Moreover, an integrated crystal oscillator (31.25 kHz) is included and serves as the reference for the PLL. Therefore, this is a complete clocking solution for ultra-low power near-threshold SoCs.**

***Index Terms* — Clock Generators, SoC, System-on-chip, Crystal Oscillator, Phase-locked loops, PLLs, ADPLLs, Ring Oscillators, Digitally Controlled Oscillators, Dual Loop.**

I. Introduction

Significant research efforts are being focused on ultra-low power (ULP), small form factor mobile devices for applications such as health monitoring and the internet of things (IoT). These applications seek to extend battery life and/or achieve energy autonomy through energy harvesting and ULP design. Reducing the supply voltage (VDD) of digital circuits, typically near or below V_{th}, is an effective way to save power. An architectural technique to further optimize power consumption is to dynamically scale the supply voltage (DVS) based on workload. However, DVS varies gate delays exponentially below V_{th}, requiring dynamic frequency scaling in order to account for performance variations caused by voltage scaling [1,2]. Therefore, there's a growing need for low-voltage, stable, and programmable at run-time ULP clock generators (CKGEN). A number of sub-µW CKGEN solutions have already been reported, but they all lack programmability and therefore cannot offer dynamic frequency scaling [2]. Current programmable CKGENs are targeted towards high frequency and are too high power for NTC SoCs. A popular solution for clock programmability in microcontrollers is to generate the highest desired

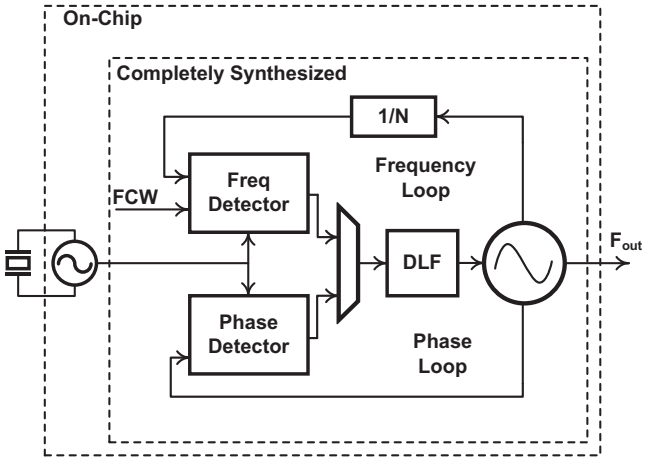

Figure 1: The overall architecture of the clock generator

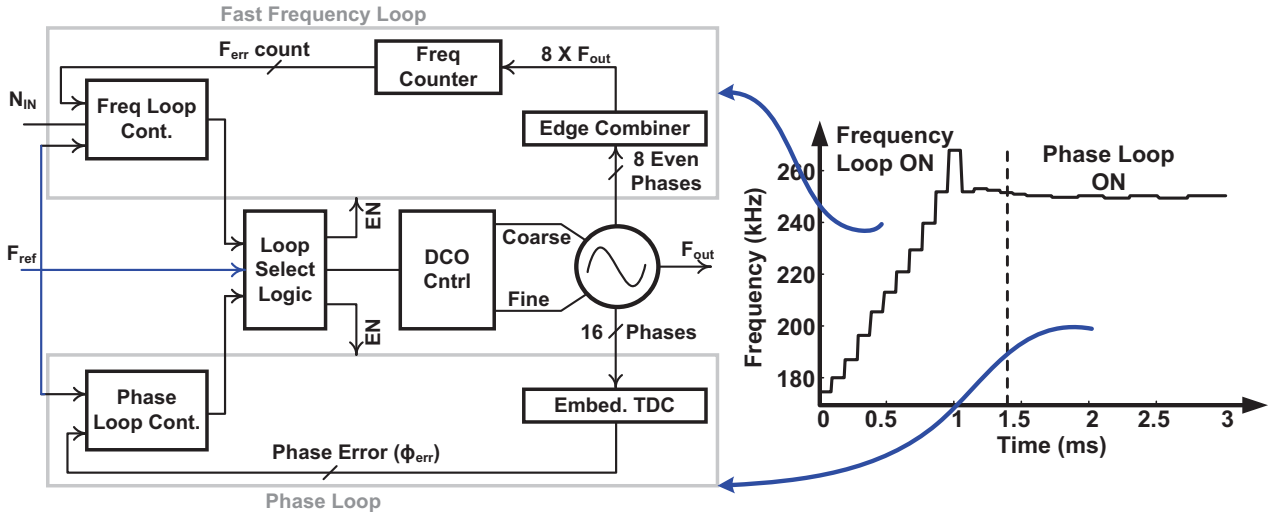

Figure 2: Details of frequency and phase loops and the step response

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frequency with a crystal oscillator and then a divider generates lower frequencies. However, this is not a low-power solution, and cannot achieve the best possible performance as the phase noise degrades proportional to N^2, where N is the divider ratio. Finally, IoT applications demand low-cost solutions, which for IC design translates to small form factor, ease of integration and test, and minimal off-chip components. For these reasons, all-digital architectures leveraging the digital design flow are highly desirable. In this paper, we present a 187.5 kHz to 500 kHz ADPLL-based CKGEN that consumes 300nW from a 0.5V VDD, has a jitter <0.1% and was implemented in a 0.13µm process. The entire ADPLL was completely implemented using standard digital design flows and automatic place and route (APR). Moreover, an integrated crystal oscillator (31.25 kHz) is included and serves as the reference frequency for the PLL. Therefore, this is a complete CKGEN solution for ULP NTC platforms.

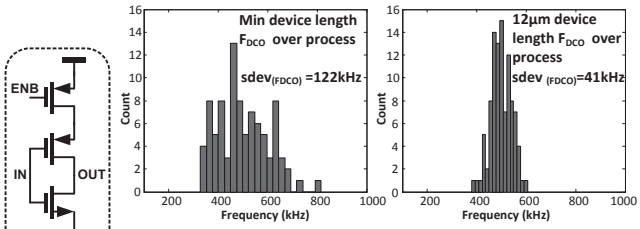
II. ADPLL Architecture

Figure 1 shows the overall architecture of the CKGEN which consists of an off-chip crystal with an integrated on-chip oscillator, and a dual-loop ring-based ADPLL. The ADPLL features two mutually exclusive loops: a frequency acquisition loop and a fine phase locking loop. The loop-select state machine (Figure 2) toggles between the loops as needed. This state machine monitors the previous four phase corrections and determines the frequency error. When the error is above 4 kHz, the frequency loop is enabled. This uses an edge combiner to produce an 8X oversampled frequency, which increases resolution and ensures frequency locking to the correct harmonic before switching over to the phase loop. When the measured frequency error is below 4 kHz, the phase loop is enabled and the frequency loop is power-gated to save power. Because the correct harmonic is found first, the phase loop can be dividerless to save power. It consists of an embedded TDC which reuses the ring oscillator as the delay line, resulting in further power and area savings.

A fast locking algorithm first performs coarse tuning within 32 reference cycles. In total, the locking time for the largest frequency error is 38-45 reference cycles. The PLL step response is shown in Figure 2 which illustrates how lock is achieved with the frequency and phase loops.

III. Circuit Details

PVT variations are magnified in near or sub-V_{th} operation. Large PVT variations require an oscillator with large tuning range in order to ensure lock, but large tuning range results in high power consumption.



Parameter	@ minL		@ L= 12 µm	
	Slow	Fast	Slow	Fast
$V_{ov}^2 = (V_{GS}-V_{th})^2$	0.0036	0.0729	0.1369	0.2421
V_{ov}^2 Ratio	20.25		1.8	

Figure 3: Effect of increasing transistor length on the PVT variations

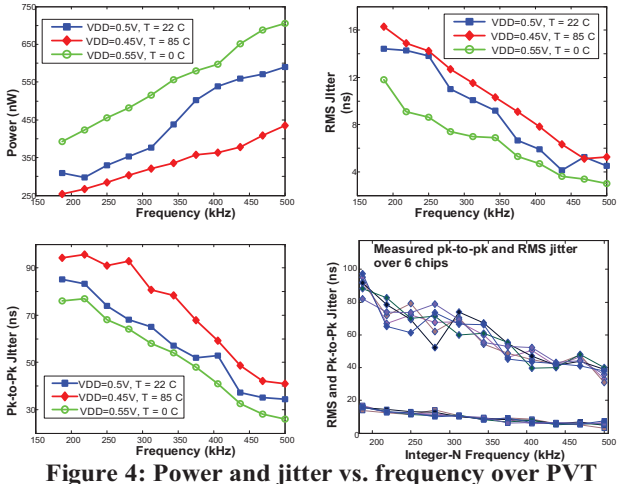


Figure 4: Power and jitter vs. frequency over PVT

Therefore, it's desirable to reduce the impact of PVT variations on the DCO to reduce the required DCO tuning range. Zero-V_{th} or dynamic V_{th} (connecting the body to the gate) transistors are options to reduce the impact of PVT, but these solutions are either high leakage or not amenable to digital design flows. PVT variations mainly impact the overdrive voltage (V_{ov} = V_{GS} - V_{th}), and therefore the drive strength of the delay cells in a ring oscillator. Figure 3 lists V_{ov}^2 in two extreme operating corners (slow-slow, 0.45V, 85ºC and fast-fast, 0.55V, -40ºC). As shown Figure 3, V_{ov}^2 is 20 times larger in the fast corner than in the slow corner for a minimum length device. However, V_{th} decreases as the channel length is increased, and Figure 3 shows V_{ov}^2 only increases by 1.8X between the same corners for 12 µm length devices. Figure 3 also compares the frequency distribution over process for two different near-Vth 500kHz DCOs. The frequency spread over process for a DCO with minimum sized inverters is 3 times as large as that of a 12 µm inverter-based DCO. This means that the DCO tuning range to calibrate out the PVT variations can shrink by roughly 3X by using long-channel devices, resulting in power savings by roughly the same factor. Using long channels to reduce PVT impact is also amenable to a digital design flow, synthesis, and APR.

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Table 1: Comparison to prior work

Performance Metric	This Work		[3] VLSI '10	[5] JSSC '12	[6] JSSC '09
	@ Min F_{out}	@ Max F_{out}			
VDD	0.5 V		1	-	1
Process	0.13 µm		90 nm	55 nm	90nm
Area (mm^2)	0.07 (PLL) + 0.13(XO)		0.27	0.16	0.037
F_{out}	187.5 kHz	500 kHz	5 MHz	216 MHz	2GHz
RMS Jitter	12.3 ns	4.7 ns	49.7 ps	8.05 ps	1.6 ps
Power	300 nW	570 nW	11.3 µW	10.5 mW	7 mW
Energy/Cycle (pJ)	1.6	1.1	2.26	48.6	3.5
Architecture	ADPLL, APR-ed, + XO		DCO only	-	DLL
F_{ref}	31.25 kHz		N/A	27 MHz	500 MHz
Reference Included	Yes		No Reference	No	No

The entire ADPLL was described using structural and behavioral Verilog, synthesized, and APR'd using standard digital CAD tools. This design methodology is much faster than full-custom layout, and also reduces the power and area.

III. Measurement Results

Figure 4 shows the power consumption, peak-to-peak jitter and RMS jitter over the entire frequency range (N=6 to N=16). Six different chips were tested to observe any process variations. Additionally, power and jitter were also measured at extreme temperature (0°C and 85°C) and VDD (0.45V and 0.55V) corners. The power consumption for the entire operating range is below 700nW, which scales with frequency from 300nW to 600nW under nominal operating conditions. It is worth noting here that the jitter measurements are those of the entire CKGEN system (crystal + PLL) and the RMS jitter at the lowest frequency is 0.025%. Figure 5 shows the phase noise at N=11. Table 1 shows that this CKGEN is the most efficient at 1.1pJ/cycle. Lastly, the die photo is given in Figure 6.

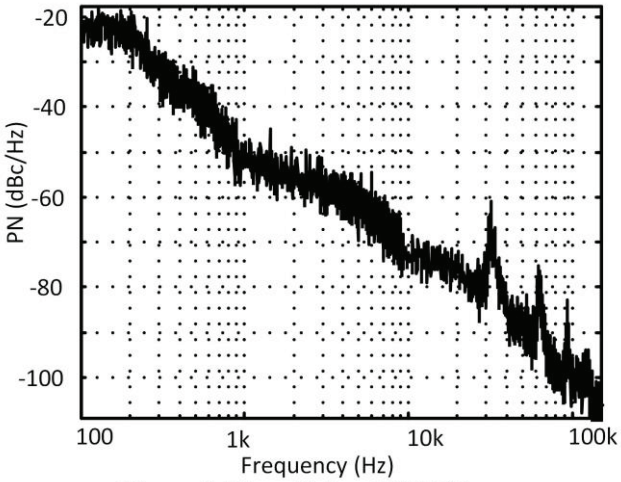

Figure 5: Phase Noise at 343 kHz

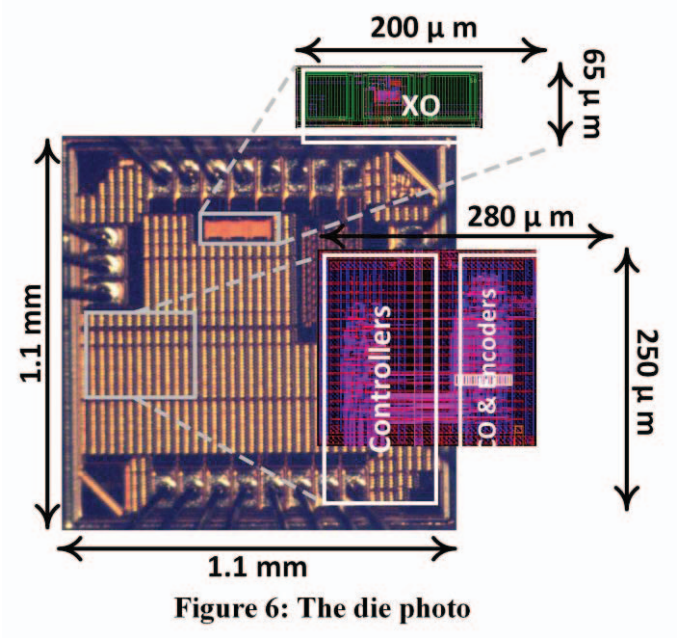

Figure 6: The die photo

VII. Conclusion

In conclusion, a complete clocking solution for low-voltage, ultra-low power systems-on-chip is presented. The entire ADPLL was implemented using digital-design flows in a 0.13µm CMOS process, consumes 300 nW at 187 kHz, and has a jitter < 0.1%. A novel dual-loop ADPLL architecture is proposed in order to eliminate the divider – resulting in extremely low power consumption without performance degradation.

Acknowledgements

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