An Automatically Placed-and-Routed ADPLL for the MedRadio Band using PWM to Enhance DCO Resolution

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***Abstract* — An all-digital phase-locked loop for the MedRadio bands is presented. This ring oscillator based ADPLL was entirely designed and placed-and-routed using digital design flows and was fabricated in a 65 nm CMOS process. Pulse width modulation of the DCO control signals is introduced as a technique to improve the resolution of the DCO to 59 kHz/LSB. This ADPLL operates as a subsampling integer-N frequency synthesizer from 400 to 460 MHz, and consumes 2.1 mA from a 1 V supply, with an rms jitter of 13.3 ps.**

***Index Terms* — Phase-Locked Loops, Ring Oscillators, DCOs, ADPLLs, Synthesizable.**

I. Introduction

All-digital phase-locked loops (ADPLLs) are preferred for frequency generation over traditional analog PLLs to take advantage of process scaling [1-4]. ADPLL architectures offer area savings by eliminating large loop filters, reconfigurability of the loop gain and bandwidth, and are mostly portable across processes. However, ADPLL performance inherently suffers due to TDC and DCO quantization errors which contribute to the in-band and out-of-band phase noise [1]. Moreover, most ADPLLs use DACs and $\Delta\sum$ modulators (DSM) to improve the DCO resolution, which require carefully matched custom design.

The next logical step for ADPLLs is to utilize digital synthesis and automatic place-and-route (APR) flows to simplify the design phase and facilitate easier integration with SoCs. Some traditionally mixed-signal systems such as ADCs and ADPLLs are already being implemented with digital synthesis tools [3,4]. This paper presents a sub-sampling, integer-N ADPLL. What distinguishes this ADPLL from others is that it was completely designed and APR-ed using digital design flows. A second contribution of this paper is a technique of pulse-width-modulating (PWM) the DCO control signals to enhance DCO resolution, replacing the traditional DAC and DSM. The PWM technique has the advantage of introducing no spurs, and allows DCO tuning with 59kHz steps. An adaptive digital loop filter (DLF) [5] is implemented to allow a large lock-in range as well as have low bandwidth to suppress TDC noise. The ADPLL FoM is -218dB at 403MHz, and covers the entire MedRadio range (401 to 457MHz).

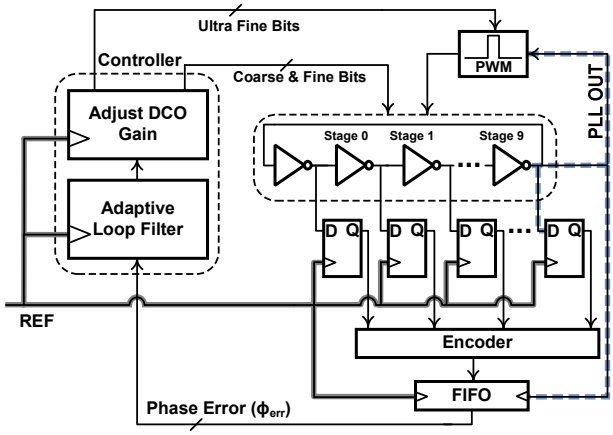

Figure 1: ADPLL overall architecture

The rest of the paper is organized as follows. Section II discusses the overall architecture of the PLL, and a discussion of the sub-blocks is given in Section III. Next, the PWM-based DCO resolution enhancement technique is explained in Section IV. The design methodology for this ADPLL with digital design flows is explained in section V. Measurement results are highlighted in Section VI and Section VII concludes the paper.

II. Overall Architecture

Fig. 1 shows the ADPLL architecture with PWM-based resolution enhancement technique. It consists of a ten stage ring DCO, embedded TDC, adaptive DLF and DCO controller. The adaptive DLF observes the TDC output (Φ_{err}) over a programmable measurement window, and then a decision by the DCO controller state machine is made whether to increment or decrement the frequency. The default setting for the measurement window is 100 reference cycles, but can be programmed through a scan chain. The DCO controller sends a 20b coarse, 20b fine and 7b ultrafine frequency control word to the DCO. The coarse and fine control bits are thermometer encoded and the ultrafine frequency bits are binary encoded.

The entire ADPLL is cell-based and the layout APR-ed, including the DCO and TDC, which introduces systematic mismatch in wiring capacitance. The most critical is the stage-to-stage mismatch that causes a bounded differential non-linearity in the TDC. The TDC output is processed in

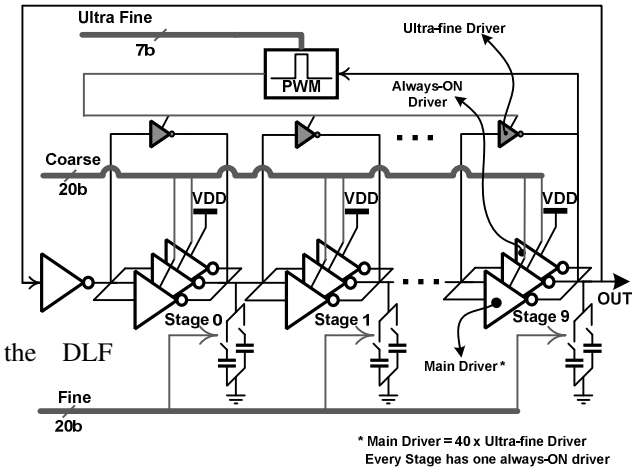

Figure 2: Detailed schematic of the DCO and PWM based resolution enhancement technique

in order to mitigate the effect of mismatches as discussed later in Section III C.

III. Circuit Design

A. Phase Detection Scheme: Embedded TDC

The phase detection scheme is based on an embedded TDC [1]. The embedded TDC samples all ten phases of the DCO every rising edge of the reference, and encodes the error signal into a 5b output (Φ_{err}). If there is a difference between f_{ref} and f_{dco} (Δf), the internal edges of the DCO will slide with respect to the reference edge, and the Φ_{err} observed by the TDC will be a cyclic phase measurement. The slope of Φ_{err} represents the magnitude and sign of Δf. When Δf is small, the TDC resolution is further enhanced by counting (8b counter) the number of f_{ref} cycles for which Φ_{err} stays at one state, and the resultant TDC LSB becomes $T_{dco}/2^{13}$ (~300 fs at 403MHz). The 5b embedded TDC combined with 8b phase counter in the controller effectively provide 13b phase resolution. Typically, ADPLLs require the TDC step to be normalized to T_{dco}. This is because the TDC step is independent of the DCO frequency, and the loop gain varies as a function of DCO frequency – an undesirable non-linearity. However, in the embedded TDC architecture, the TDC step size depends on the delay per stage of the DCO and therefore, the step size tracks the DCO period and eliminates the need for TDC step normalization.

B. Digitally Controlled Oscillator

Fig. 2 illustrates the architecture of the DCO with PWM circuit driving the control of all ultra-fine drivers together. The detailed schematic of the cells used in the DCO and the PWM are shown in Fig. 3. The unit main driver cell is a differential pair with cross coupled PMOS loads which can be turned on/off by the EN signal. The unit switch-capacitor cell is a transmission gate loaded

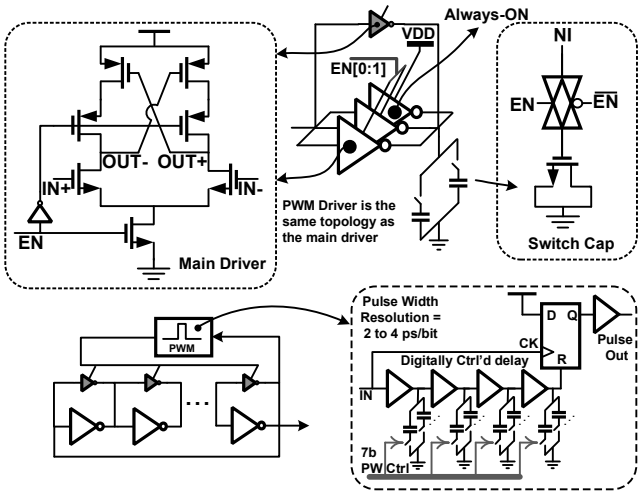

Figure 3: Details of DCO cells

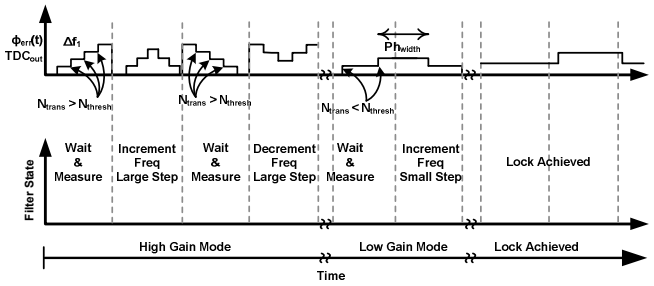

Figure 4: Adaptive filter states as a function of time

with an NMOS device. The unit ultra-fine driver cell is a 40X weaker version of the main driver. These three are the only custom cells in the entire ADPLL, and have the same pitch as the standard cells. A 7b PWM signal is generated using the same driver and switch-capacitor cells as in the DCO. The DCO features three different step sizes; coarse, fine and ultra-fine. It can be tuned with 9MHz/bit coarse steps, and 1.2MHz/bit fine steps. The coarse steps are set by turning parallel main drivers on/off while the fine tuning is done by enabling parallel switch-capacitor cells. The enable of each coarse/fine cell is independently indexed by the controller.

C. Adaptive Digital Loop Filter

The adaptive DLF has low and high gain modes. For large Δf (difference between f_{ref} and f_{dco}), the loop operates in the high gain mode and Δf is measured and used to adjust the loop gain. The loop switches to low gain mode when Δf reaches a target value, after which the gain is adjusted based on the phase measurement. The operation of the adaptive DLF and DCO controller is illustrated by a timing diagram in Fig. 4. The DLF observes Φ_{err} over a measurement window, and determines the gain mode automatically based on Δf. When Δf is large, larger bandwidth is desired to settle fast. The loop filter measures the number of transitions (N_{trans}) in Φ_{err}, essentially differentiating Φ_{err} to obtain Δf. N_{trans} represents the magnitude, and the direction of the transition

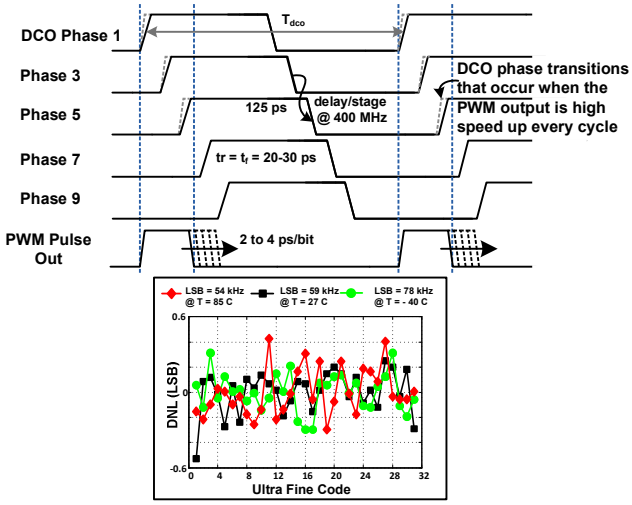

Figure 5: Principle of operation of resolution enhancement technique, and the measured DNL of ultra fine frequency tuning using the PWM-based technique

(up/down) represents the sign of Δf. Based on N_{trans}, the DLF performs a linear search for the appropriate DCO step size. A programmable N_{thresh} defines the boundary between low gain and high gain modes. Small Δf is defined by the number of Φ_{err} transitions in one measurement window being less than 10. In this case, higher resolution is desired and the DLF automatically switches to low gain mode. In low gain mode, the phase error is measured by counting the number of reference cycles between two transitions of Φ_{err} to get the phase width (Ph_{width}). This represents how long it takes for the DCO edge to slide from one phase to the next; therefore, it represents Δf. Once the Ph_{width} is known, a linear search chooses one of four small DCO step sizes. The entire DLF is implemented on chip. This adaptive DLF allows a lock-in range of ±30 MHz. When the PLL output is locked to the reference, the Φ_{err} behaves like a bang-bang phase detector and frequency is controlled with an ultra-fine LSB (59 kHz) around the desired frequency.

In the high gain mode, the effect of stage-to-stage mismatch is alleviated by measuring the slope of Φ_{err} (N_{trans}) over multiple reference cycles. This way, any differential non-linearity in the DCO due to stage-to-stage mismatch is averaged because the total delay (sum of individual delays) always equals T_{dco}.

IV. DCO Resolution Enhancement

The principle of operation of the PWM technique is shown in Fig. 5. Referring to Fig. 2, an ultra-fine driver 40x weaker than the main drivers is connected in parallel to each stage of the DCO. This technique enhances DCO resolution as follows: the PWM generates synchronous pulses from the DCO output at the DCO frequency, which enable all ten ultra-fine drivers together for only a fraction of T_{dco}. As an edge propagates through the DCO, only the transitions, or fractions of transitions, that overlap the PWM pulse in time will be sped up by the ultra-fine driver. All other transitions will be unaffected (illustrated in Fig. 5). The frequency increases as a function of the pulse width. Because the PWM signal is applied every DCO period, the pulse modifies the DCO's internal edges the same way every cycle, thus changing its frequency by a small amount. The primary advantage of PWM control is it finely tunes the frequency of the DCO without producing spurs, unlike traditional LSB dithering which toggles between larger frequency steps and introduces spurs which are then rejected using a DSM. Therefore, this technique replaces the DAC and DSM. The measured DNL of ultra-fine (PWM) tuning as a function of temperature is presented in Fig. 5. The worst case DNL at 403MHz is -0.55 LSB. Finally, this coarse/fine tuning combined with PWM control decouples the resolution versus tuning range tradeoff, and the DCO is able to have small quantization error as well as a wide tuning range.

V. Design Methodology

The design methodology is illustrated in Fig. 6, which utilizes automated digital flows to accelerate the design phase. The first step is to identify the core, tri-state unit cells that will be arrayed to form a digitally tunable delay element, and design and layout these unit cells with the standard cell pitch. The unit cells are roughly the size of a D flip-flop standard cell. These cells are then integrated with the synthesis and APR flows. Once the cells are integrated, an HDL description of the entire ADPLL is used to synthesize and APR it. The tools are also used to create macros for sub-blocks to achieve a moderate

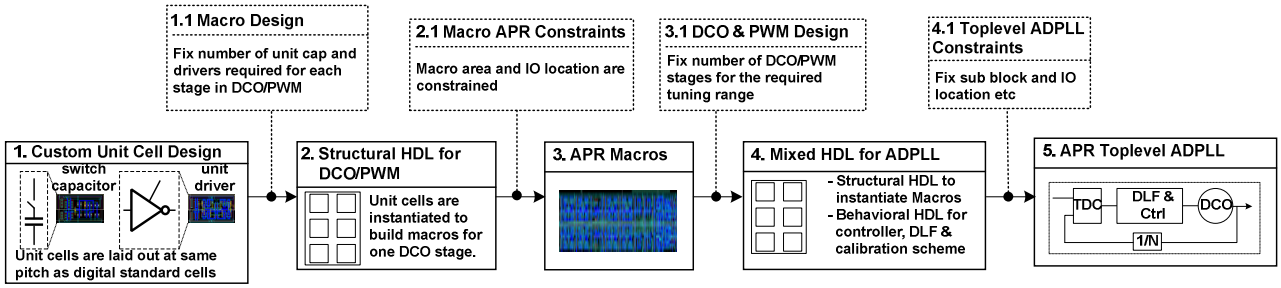

Figure 6: The design methodology for the ADPLL

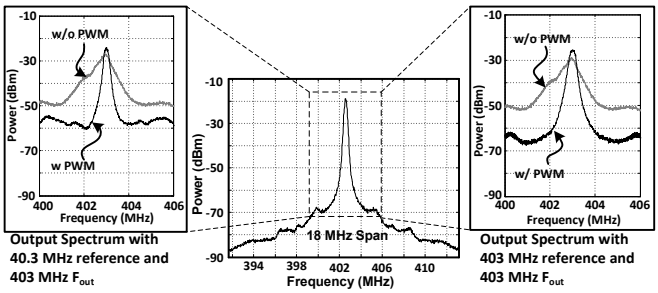

Figure 7: ADPLL output spectrum with and without PWM resolution enhancement technique @ 403 MHz and output spectrum at @ 403 MHz with 40.3 MHz reference

$$FoM = 20\log\left(\frac{\sigma_t}{1s}\right) + 10\log\left(\frac{P}{1mW}\right)$$

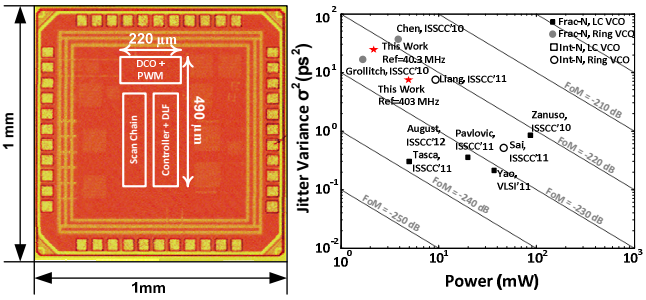

Figure 8: ADPLL die photo and FoM comparison

amount of matching in the layout. For example, in this ADPLL, a macro for one stage of the DCO was first APR'd that included three main drivers and two switch capacitor cells. This marco was then instantiated in HDL ten times to create a ten-stage DCO. This methodology significantly accelerates the design phase because most of the design decisions are made at the architectural level, therefore design iterations are completely automated. Moreover, the number and complexity of required design rule checks grows exponentially with scaling, but with this methodology, this challenge is mostly handed over to the tools.

VI. Measurement Results

This ADPLL performs integer-N synthesis without a divider by subsampling the TDC output for division ratios greater than one. The division ratio (N) can be programmed by a frequency control word in the controller. The in-band phase noise is -98dBc/Hz for f_{ref}=403MHz (N=1 and BW = 140 kHz) and -87dBc/Hz for 40.3MHz (N=10 and BW = 40 kHz).

Fig. 7 shows the output spectrum for f_{out}=403MHz for 403MHz and 40.3MHz reference frequencies. The PLL output in lock state with and without PWM-based resolution enhancement is shown. This results in 14dB and 11dB improvements in in-band phase noise for 403MHz and 40.3MHz reference frequencies, respectively, with a measured rms period jitter of 7.9 ps and 13.3 ps. The ADPLL is implemented in a 65nm CMOS process, and occupies an active area of 0.1 mm^2. It covers the MedRadio bands and consumes 2.1mA and 3.3mA from a 1.0V supply for N of 10 and 1 respectively. The PWM block consumes 770µW and occupies 93x110µm. The overall FoM of this PLL is compared with state-of-the-art ADPLLs in Fig. 8. The die photo is also shown in Fig. 8. Table I compares more specific performance metrics of this work to some recently published state-of-the-art ADPLLs.

Table I: ADPLL Performance Comparison

	This Work		ISSCC'10 [1]	JSSC'11 [2]	ISSCC'12
F_{REF} (MHz)	403	40.3	26	544	108/72/36
F_{OUT}(MHz)	403	403	800	0.7 - 3.5	3100
RMS Jitter	7.9 ps	13.3 ps	21.5 ps	1.6 ps	1.01 ps
PN (dBc/Hz)	-98 @ 1MHz	-87 @ 1MHz	-98 @ 1MHz	-116 @ 1MHz	-
Area	0.1 mm^2	0.1 mm^2	0.05 mm^2	0.36 mm^2	0.32 mm^2
Power	3.3 mA	2.1 mA	2.66 mA	1.6 mA	27.5/26.8/ 25.8 mA
VDD	1	1	1.1-1.3	1	1.2
Architecture	ADPLL	ADPLL	ADPLL	Highly Digital	ADPLL
DAC & ΔΣ	No	No	DAC & ∑Δ	Multiple DACs	DAC
Technology	65 nm	65 nm	65 nm	90 nm	65 nm

VII. Conclusion

A subsampling integer-N ADPLL that was completely designing used digital design flows was presented. This methodology significantly simplifies the design phase for ADPLLs and is amenable to process scaling. A PWM based DCO resolution enhancement technique is introduced which improves the DCO resolution to 59 kHz/LSB. This resolution enhancement is implemented at the DCO frequency, unlike traditional dithering, and therefore does not introduce any spurs. The FoM of this APR'd ADPLL is -214 dB, which is comparable to state-of-the-art ADPLLs not using digital design flows.

Acknowledgement

This research was supported by the U.S. Army Research Laboratory under contract W911NF and prepared through collaborative participation in the Microelectronics Center of Micro Autonomous Systems and Technology (MAST) Collaborative Technology Alliance (CTA).

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