Transactions Briefs

Characterization of the Proximity Effect from Tungsten TSVs on 130-nm CMOS Devices in 3-D ICs

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***Abstract*— The proximity effect of tungsten-filled through-silicon-vias (TSVs) on the threshold voltage and mobility of CMOS devices due to mismatch in thermal expansion coefficients is modeled and verified with measurements. Test structures fabricated in a two-layer 130-nm CMOS 3-D integrated circuit process are measured and compared with 3-D finite element method simulations. Results show that the threshold voltage is not affected by TSVs, whereas mobility is affected by up to 10% for devices within 4 μm of a TSV.**

***Index Terms*— 3-D IC, proximity effect, thermal stress, through-silicon-via (TSV).**

I. Introduction

3-D integrated circuit (IC) integration can simultaneously achieve smaller form factor, lower power, and higher performance by reducing the parasitic inductance and capacitance of interconnect. Among the proposed 3-D interconnect methods, through-silicon-vias (TSVs) are a promising solution to enhance bandwidth in VLSI systems due to their high density and low loss.

Fabricating high aspect ratio vias within a silicon substrate and achieving high yield have been huge challenges for CMOS technology [1]. In addition, although the TSV technology provides new opportunities for circuit designers, it requires new considerations during the circuit design. They should be aware of not only the electrical performance of TSVs such as their parasitic capacitance, resistance, and inductance, but also the performance change of active devices that are placed in close proximity to TSVs.

There have been concerns that the proximity of a TSV to a device such as a transistor can impact its electrical performance, and the proximity effect of TSVs on devices was reported in [2]–[5]. TSV processes have multiple categories defined by their processing steps, including via-first, via-last, and via-middle. Furthermore, different materials can be used for TSVs such as Cu, W, and polysilicon. This diversity produces varied results of the impact of TSVs on other devices, and experimental research for other cases is required.

This brief presents a study of the proximity effect for via-middle tungsten-filled cylinder-shaped TSVs using a 3-D IC process from Tezzaron [7]. A two-layer test structure with TSVs was fabricated with a 130-nm CMOS process to evaluate the proximity effect of TSVs on MOSFETs. The key parameters of different-sized p-channel MOS (pMOS) and n-channel MOS (nMOS) devices were measured to characterize the impact of TSV proximity and provide guidelines for design with the specified TSVs.

Manuscript received August 1, 2012; revised February 10, 2013 and May 26, 2013; accepted July 25, 2013. Date of publication September 6, 2013; date of current version August 21, 2014. This work was supported by the DARPA Young Faculty Award. The work of S. Han was supported by the Samsung Scholarship.

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Digital Object Identifier 10.1109/TVLSI.2013.2279639

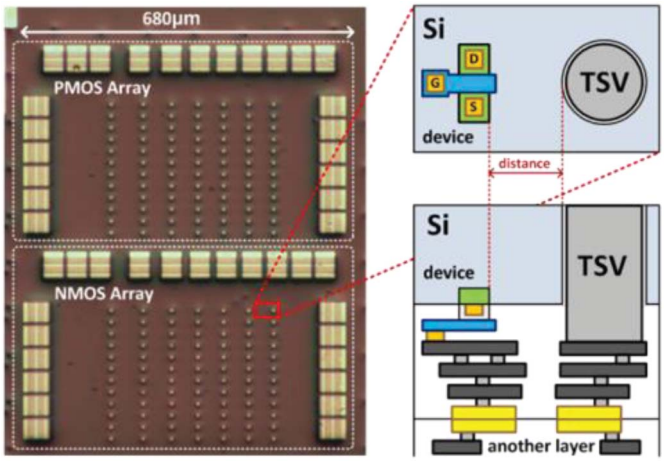

Fig. 1. Die-photo of the test structure and schematic of one cell which consists of one MOSFET and one TSV. Top and cross-sectional views.

II. Applications and Problems

Compared with 3-D packages such as edge wire bonding and interposers, TSVs allow a high density of vertical interconnects between IC layers that can be placed anywhere on the IC and not just along the perimeter. In addition, a TSV allows shorter interconnect having smaller parasitic capacitance, inductance, and resistance. Because of the smaller parasitics, a TSV enables high-speed and low-power interconnects. Thus, by using TSVs, the total bandwidth of chip-to-chip communication can be enhanced significantly.

However, a TSV has some process difficulties compared to a conventional planar CMOS process such as yield since it is a relatively new technology, and there has been being active research to improve the TSV process. In addition, while it is known that TSVs will affect the performance of devices located near them, the research on the proximity of TSVs is still immature; the observation, cause of the effect, and its processing solution are currently insufficient. According to prior work [4], [6], thermal expansion and stress due to coefficient of thermal expansion (CTE) mismatch is the major reason for the TSV proximity effect, which is difficult to resolve in a CMOS fabrication process. Therefore, for now the proximity effect of a TSV should be considered as a consequence of TSV technology, and a circuit designer should take it into consideration, especially in the layout stage, to avoid unintended performance variation of the circuits.

III. Test Structure

The TSVs in this brief are fabricated with a via-middle process from Tezzaron [7]. After front-end of line processing, TSV holes are etched part-way into the substrate and W is deposited into these SiO_2 lined holes. Once a wafer is completed including backend of line processing, two wafers are stacked face-to-face using Cu-metal micropad bonding. To implement vertical interconnect to additional wafers or to wire-bonding pads, the top die is then thinned from the backside to expose the TSVs.

Test structures have been fabricated in this process with two arrays for pMOS and nMOS devices as shown in Fig. 1. Active devices and

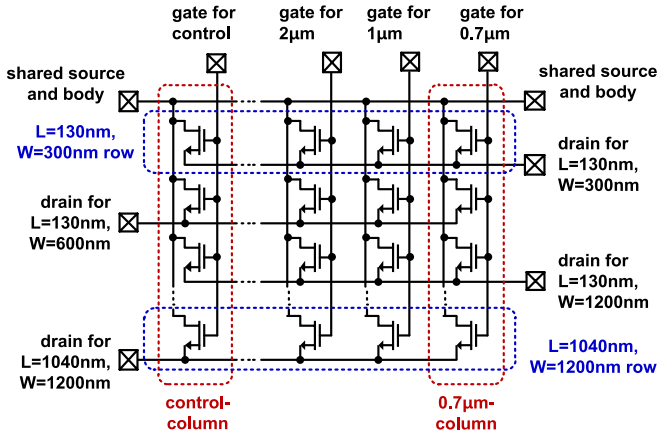

Fig. 2. Schematic of the test structure (one array).

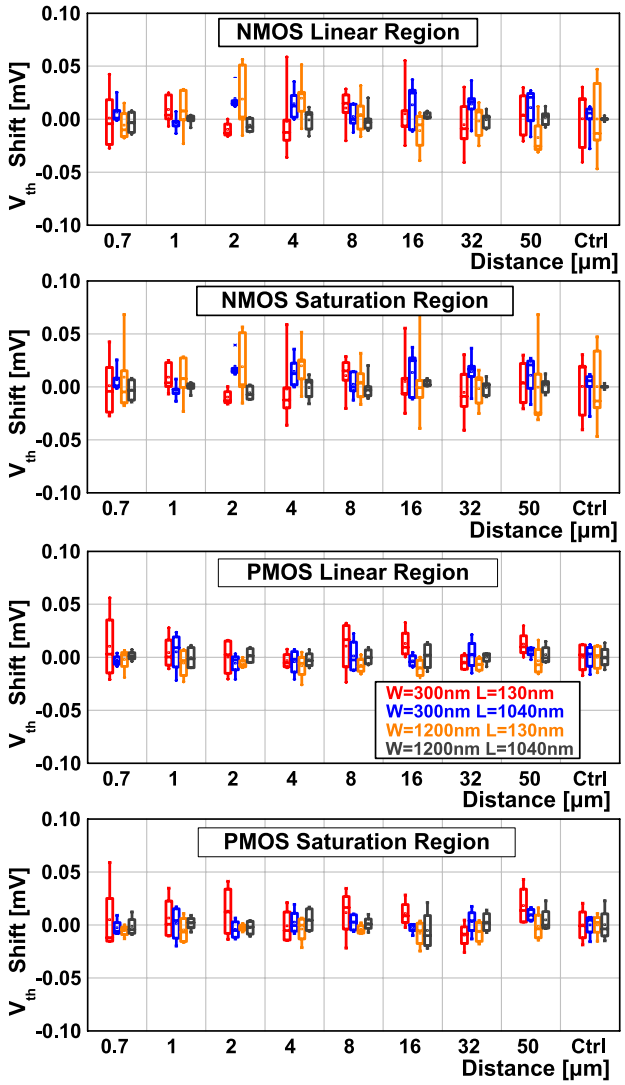

Fig. 3. Measurement results of V_{TH} shift. No V_{TH} shift observed in nMOS pMOS devices.

TSVs for characterization are implemented on the top layer. Probe pads to access the devices are made on the thinned backside of the top die and connected to metal layers inside of the top die with multiple TSVs. The channels of all devices are placed in the vertical direction

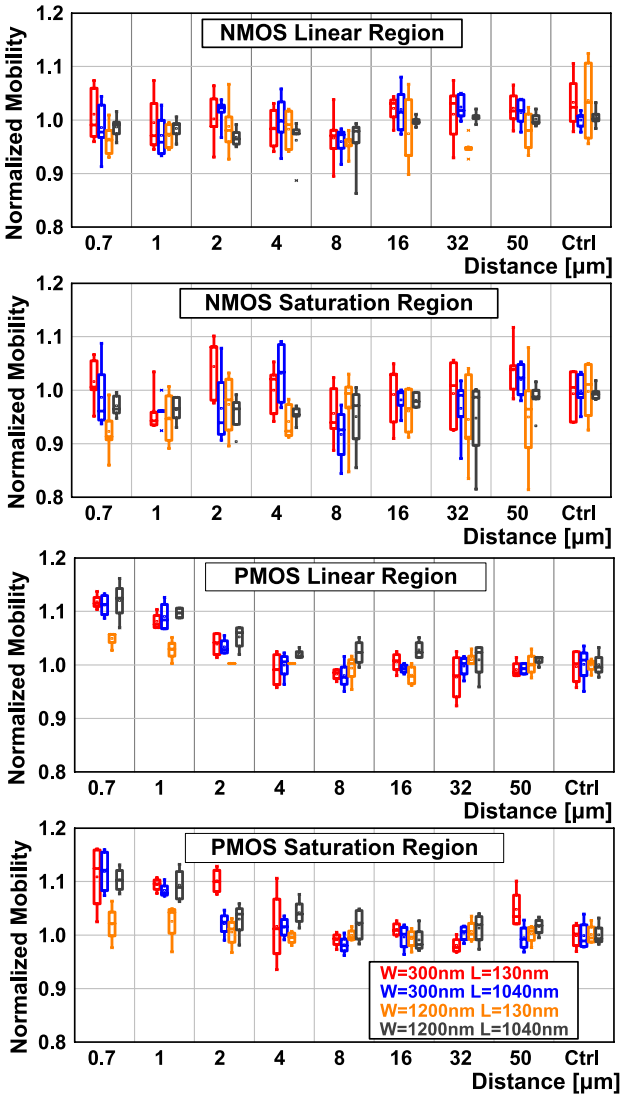

Fig. 4. Measurement results of mobility change. Electron mobility shows no trends, and hole mobility is increased by up to 10%.

in Fig. 1. The TSV is a cylindrical shape with a diameter of 1.2 μm and height of 6 μm after the wafer-thinning process. The 3-D IC process is based on the chartered 130-nm CMOS process.

The schematic of the test structure is shown in Fig. 2. Each array has 12 rows and nine columns. Every column corresponds to one of eight distances between a TSV and a FET that range from 0.7 to 50 μm. The array also includes control FETs without TSVs nearby. Each row represents one among 12 combinations of the channel width from 300 to 1200 nm and the channel length from 130 to 1040 nm. This results in a total of 216 combinations. One column has 12 different-sized FETs, and they share one dc probe pad connected to the gates of the FETs. One row has nine equal-sized FETs sharing one dc probe pad connected to the drains of the FETs. The source and body terminals of all FETs are connected to a shared dc probe. Other peripheral circuits, for instance, a scan chain, mux, or ADC, are not implemented to allow more accurate measurements of the device performance using instead off-chip equipment.

IV. Measurement Results

V_{TH} and carrier mobility are the two main characteristics of devices that we will focus on since they are easily affected by variations

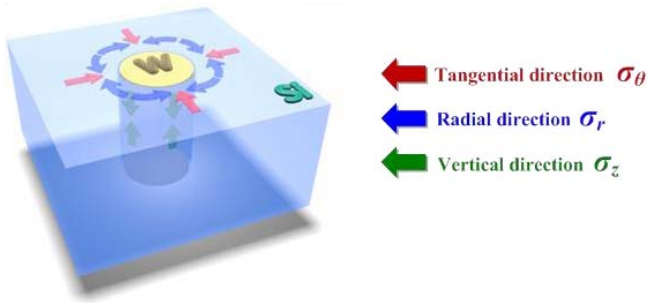

Fig. 5. Stress direction due to CTE mismatch.

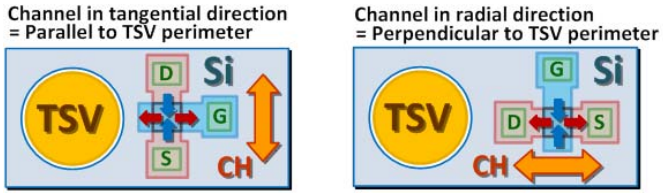

Fig. 6. Stress direction due to CTE mismatch.

such as process, temperature, and supply voltage. To characterize each device, its V_{TH} and mobility was calculated from the $I_{DS} - V_{GS}$ curve, which was measured with an Agilent 4156C semiconductor parameter analyzer and dc probes. V_{GS} is swept from 0 to 1.5 V with 15 mV steps for $V_{DS} = 10$ mV (linear region) and $V_{DS} = 1.5$ V (saturation region), respectively. Both the V_{TH} and the mobility are extracted by the maximum g_m method [8] and normalized to values extracted from the control case FETs without TSVs nearby.

Fig. 3 shows the V_{TH} shift observed in the devices. In both nMOS and pMOS devices, the V_{TH} shift is unnoticeable. Fig. 4 shows the observed mobility change. While electron mobility change is not observed, hole mobility increases significantly as the distance between the pMOS device and TSV is reduced below 4 μm. Different widths and lengths of the devices make no noticeable difference in the V_{TH} shift or mobility change, and no remarkable difference is observed between linear and saturation region. As a result, only hole mobility near a TSV is affected, therefore, to keep mobility change below 5%, a keep-away-zone of 4 μm should be considered.

V. Analysis

Mobility changes are most likely due to the mismatch in the CTE between silicon and tungsten. The CTE of silicon (Si: 2.7 ppm/°C) is smaller than that of tungsten (W: 4.3 ppm/°C), which adds strain to the Si surrounding the TSV as the wafer cools after fabrication [6]. W is deposited at ~400 °C and has a larger CTE than Si. At room temperature, the W shrinks more than the surrounding Si, which causes compressive stress σ_θ in the tangential direction to the TSV, tensile stress σ_r in the radial direction to the TSV, and compressive stress σ_z in the vertical direction as shown in Fig. 5.

According to the piezoresistance model, the hole and electron mobility in semiconductors change with stress direction and strength because of the anisotropic energy band structure [9], [10]. The impact of these stresses depends on the orientation of the devices. While device channels drawn in the radial direction will suffer from compressive longitudinal stress and transverse tensile stress, devices with channels drawn in the tangential direction will suffer from tangential stress and longitudinal compressive stress. Therefore, device channels in the radial and tangential direction will suffer from opposite directions of stress in the (100) plane (σ_{xx}, σ_{yy}) and common stress in the [100] direction (σ_{zz}) as shown in Fig. 6.

TABLE I
Information on the Tezzaron TSV Process

Parameter		Value
Wafer crystal orientation		Standard (100), <110>
TSV dimension		W = 1.2μm, L = 6μm
SiO_2 linear thickness		100nm
Process condition (temperature)	W fill deposition	425°C
	SiO_2 linear deposition	400°C
	Cooling	25°C

TABLE II
Homogeneous Material Properties

Material	Young's modulus E (GPa)	Poisson's ratio, ν
SiO_2	71.4	0.16
Si	131	0.278
W	411	0.29
Cu	115	0.343

VI. Modeling

To verify this, 3-D finite element method (FEM) modeling is performed. COMSOL is used to characterize the thermal stress around a single TSV incorporating detailed process information on Tezzaron technology. Table I summarizes the information of the Tezzaron TSV technology used for modeling.

The parameters describing material properties should be set carefully. Since COMSOL has material libraries having default values as shown as Table II, these are used without modification except for the most critical parameter, the orthotropic stiffness matrix. This is given below, which describes the wafer crystal orientation and gives the stress/strain relationships depending on Young's modulus (E), Poisson's ratio (υ), and the shear modulus (G) in the x, y, z Cartesian axes [11], [12]

$$\begin{bmatrix}\sigma_{xx}\\ \sigma_{yy}\\ \sigma_{zz}\\ \sigma_{yz}\\ \sigma_{zx}\\ \sigma_{xy}\end{bmatrix} = \begin{bmatrix} \frac{1-\upsilon_{yz}\upsilon_{zy}}{E_yE_z\Delta} & \frac{\upsilon_{yx}+\upsilon_{yz}\upsilon_{zy}}{E_yE_z\Delta} & \frac{\upsilon_{zx}+\upsilon_{yx}\upsilon_{zy}}{E_yE_z\Delta} & 0 & 0 & 0 \\ \frac{\upsilon_{xy}+\upsilon_{xz}\upsilon_{zy}}{E_zE_x\Delta} & \frac{1-\upsilon_{zx}\upsilon_{yx}}{E_zE_x\Delta} & \frac{\upsilon_{yz}+\upsilon_{yz}\upsilon_{xy}}{E_zE_x\Delta} & 0 & 0 & 0 \\ \frac{\upsilon_{xz}+\upsilon_{xy}\upsilon_{yz}}{E_xE_y\Delta} & \frac{\upsilon_{yz}+\upsilon_{xz}\upsilon_{yx}}{E_xE_y\Delta} & \frac{1-\upsilon_{xy}\upsilon_{yz}}{E_xE_y\Delta} & 0 & 0 & 0 \\ 0 & 0 & 0 & G_{yz} & 0 & 0 \\ 0 & 0 & 0 & 0 & G_{zx} & 0 \\ 0 & 0 & 0 & 0 & 0 & G_{xy} \end{bmatrix} \cdot \begin{bmatrix}\varepsilon_{xx}\\ \varepsilon_{yy}\\ \varepsilon_{zz}\\ \varepsilon_{yz}\\ \varepsilon_{zx}\\ \varepsilon_{xy}\end{bmatrix} \quad (1)$$

where

$$\Delta = \frac{1 - \upsilon_{xy}\upsilon_{yx} - \upsilon_{yz}\upsilon_{zy} - \upsilon_{zx}\upsilon_{xz} - 2\upsilon_{xy}\upsilon_{yz}\upsilon_{zx}}{E_xE_yE_z}.$$

The default orthotropic stiffness matrix for silicon in COMSOL is the ⟨110⟩ direction whose three axes are at [100], [010], and [001]. This matrix should be modified for a standard (100)/⟨110⟩ wafer [12]

$$E_x = E_y = 169 \text{ Gpa}, \quad E_z = 130 \text{ Gpa} \quad (2)$$

$$\upsilon_{yx} = 0.36, \quad \upsilon_{zx} = 0.28, \quad \upsilon_{xy} = 0.064 \quad (3)$$

$$G_{yz} = G_{zx} = 79.6 \text{ Gpa}, \quad G_{xy} = 50.9 \text{ Gpa} \quad (4)$$

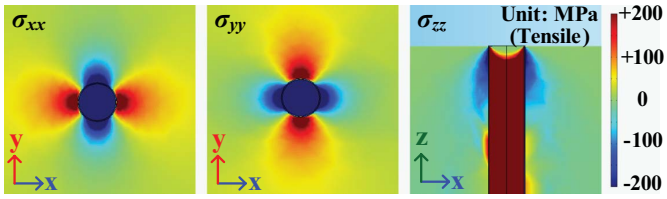

Fig. 7. Stress along the x-, y-, and z-axis.

TABLE III
PIEZORESISTIVE COEFFICIENTS OF DOPED SILICON

Material	ρ_0 [Ω·cm]	π_{11} [10^{-11}/Pa]	π_{12} [10^{-11}/Pa]	π_{44} [10^{-11}/Pa]
n-Si	11.7	-102.2	53.7	-13.6
p-Si	7.8	6.6	-1.1	138.1

$$\begin{bmatrix}\sigma_{xx}\\ \sigma_{yy}\\ \sigma_{zz}\\ \sigma_{yz}\\ \sigma_{zx}\\ \sigma_{xy}\end{bmatrix} = \begin{bmatrix}165.7 & 35.7 & 64.1 & 0 & 0 & 0\\ 35.7 & 165.7 & 64.1 & 0 & 0 & 0\\ 64.1 & 64.1 & 165.7 & 0 & 0 & 0\\ 0 & 0 & 0 & 79.6 & 0 & 0\\ 0 & 0 & 0 & 0 & 79.6 & 0\\ 0 & 0 & 0 & 0 & 0 & 50.9\end{bmatrix}\begin{bmatrix}\varepsilon_{xx}\\ \varepsilon_{yy}\\ \varepsilon_{zz}\\ \varepsilon_{yz}\\ \varepsilon_{zx}\\ \varepsilon_{xy}\end{bmatrix}. \quad (5)$$

With these settings, the FEM modeling is performed, and Fig. 7 shows the results. σ_{xx} and σ_{yy} are drawn on the x–y plane (top view on a TSV), and σ_{yzz} is on the x–z plane (cross section of a TSV). The blue gradient means compressive stress, and tensile stress is expressed as the red gradient. The result shows the tensile radial stress and the compressive tangential stress. As described previously, the CTE mismatch induces tensile σ_r, compressive σ_θ, and compressive σ_z stresses. In this simulation, σ_r is 200 MPa, and σ_θ is 200 MPa, and σ_z is negligible. Because the factional resistivity is changed with small mechanical stress [10], at stresses less than 1 GPa, the linear piezroresistance model can be used as follows [13], [14]:

$$(\text{mobility change}) = \pi_L \cdot \sigma_L + \pi_T \cdot \sigma_T + \pi_V \cdot \sigma_{zz} \quad (6)$$

where σ_L, σ_T, and σ_{zz} are the longitudinal, transverse, and vertical stresses, respectively, and π_L, π_T, and π_V are the piezoresistive coefficients, respectively. The values of σ_L, σ_T, and σ_{zz} can be obtained from a FEM simulation. The π coefficients are material properties explaining the relationship between the stress and the induced resistivity change. Table III shows three different π coefficients for an n-doped and p-doped silicon substrate [15]. Also, Table IV shows the relation between three π coefficients (π_{11}, π_{12}, and π_{44}) and the effective piezoresistive coefficients for Cartesian coordinates (π_L, π_T, and π_V), which is necessary for the linear piezoresistance model [16], [17].

From the equations, longitudinal, transverse, and vertical piezoresistive coefficients for Cartesian coordinates or the linear piezroresistance model can be expressed as follows:

$$(\text{Longitudial piezoresistive coefficient}) = \pi_L = \frac{\pi_{11}+\pi_{12}+\pi_{44}}{2} \quad (7)$$

$$(\text{Transverse piezoresistive coefficient}) = \pi_T = \frac{\pi_{11}+\pi_{12}-\pi_{44}}{2} \quad (8)$$

$$(\text{Vertical piezoresistive coefficient}) = \pi_V = \pi_{12}. \quad (9)$$

Finally, all piezoresistive coefficients for the linear piezroresistance can be expressed as shown in Table V.

With the thermal stress and piezoresistive coefficients, Fig. 8 shows the FEM simulation results of the hole and electron mobility change due to stress direction and strength. Each plot expresses mobility change near one TSV by color gradients in x–y direction. The red gradient shows larger mobility, and the blue means smaller. The result shows the hole mobility increases in the radial direction of a TSV whereas it decreases in the tangential direction. There is no noticeable

TABLE IV
EFFECTIVE PIEZORESISTIVE COEFFICIENTS DEPENDING ON THE CHANNEL AND STRESS DIRECTIONS OF (100)/<110> WAFER

Channel (φ')	Stress (Φ)	π_{eff}
[110] (φ'=45°)	[110] (Φ=45°)	$(\pi_{11}+\pi_{12}+\pi_{44})/2$
[110] (φ'=45°)	[$\bar{1}$10] (Φ=135°)	$(\pi_{11}+\pi_{12}-\pi_{44})/2$
[100] (φ'=0)	[010] (Φ=90°)	π_{12}

TABLE V
PIEZORESISTIVE COEFFICIENTS FOR BULK SILICON OF (100)/<110> WAFER

Carrier	π_L [10^{-11}/Pa]	π_T [10^{-11}/Pa]	π_{12} [10^{-11}/Pa]
electron	-31.6	-17.6	53.7
hole	71.8	-66.3	-1.1

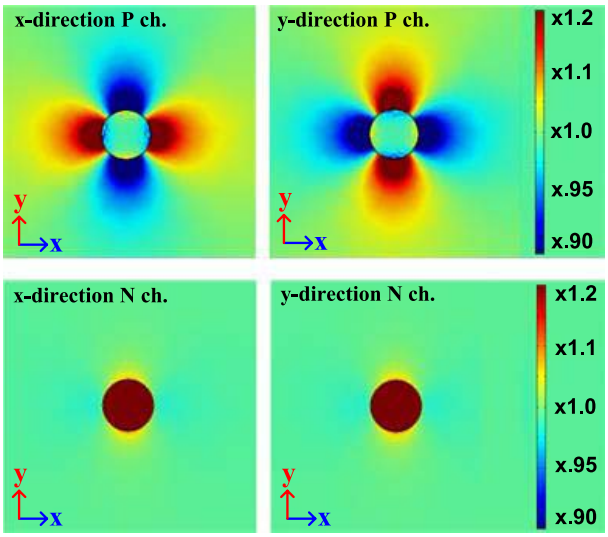

Fig. 8. Mobility change of pMOS and nMOS.

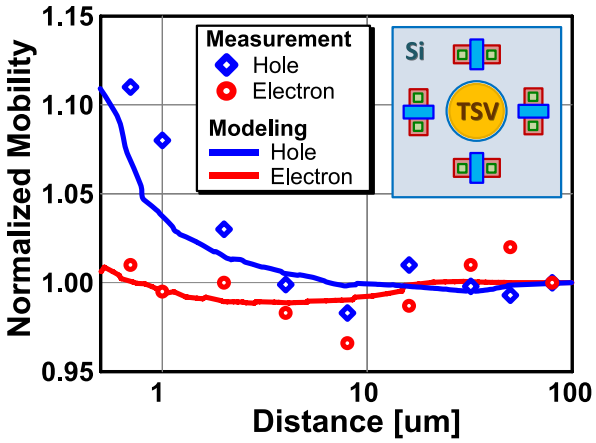

Fig. 9. Comparison of measured and modeling results of channels in tangential direction.

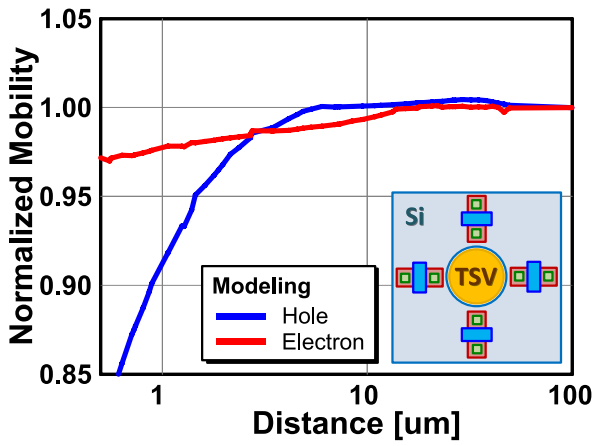

Fig. 10. Comparison of modeling results of channels in radial direction.

change of the hole mobility, and the diagonal directions of TSVs are stress-free, and there is no resulting mobility change. In addition, the affected area whose radius is less than 3× of a TSV diameter is affected by the TSV proximity.

From the results, mobility changes depending on the distance are extracted, which show good agreement with measurements as depicted in Figs. 9 and 10 for tangential and radial device channels, respectively. For comparison, Cu TSVs were also simulated in the same environment, and these simulation results show much more severe mobility change compared with W TSVs due to the lager CTE mismatch between Si (2.7 ppm/°C) and Cu (17.7 ppm/°C) [18].

VII. Conclusion

In summary, the threshold voltage is not significantly affected by TSVs, whereas mobility is affected by as much as 10% for devices within 4 μm of a W TSV in the Tezzaron 3-D IC process. This impact is a function of the device orientation, as well as proximity to a TSV. A keep-away-zone of at least 4 μm should be considered for minimal impact on device performance. Because this TSV proximity effect is due to the relative resistivity change by the mechanical stress induced by CTE mismatch, the relative impact would not be significantly affected by process-voltage-temperature variation.

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