A 60 GHz Antenna-Referenced Frequency-Locked Loop in 0.13 μm CMOS for Wireless Sensor Networks

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***Abstract*—This paper presents a 60 GHz frequency-locked loop (FLL) for wireless sensor network applications. The FLL incorporates an on-chip patch antenna as both a radiator and a frequency reference, realizing a compact and low-cost solution for non-coherent energy detection radios. To further reduce the size of a wireless sensor node, the area beneath the patch antenna ground plane is utilized for analog and digital baseband circuitry integration. A sensor array was implemented beneath the antenna ground plane to measure the spatial coupling from the antenna to the circuitry beneath it. The FLL is fabricated in a 0.13 μm CMOS technology. The operating frequency is locked to the maximum-efficiency point of the antenna with a mean of 59.34 GHz and standard deviation of 195 MHz over process variation. The circuit and antenna occupies 2.85 mm^2 and consumes 29.6 mW.**

***Index Terms*—60 GHz, CMOS, crystal replacement, frequency reference, integrated antenna, wireless sensor networks (WSNs).**

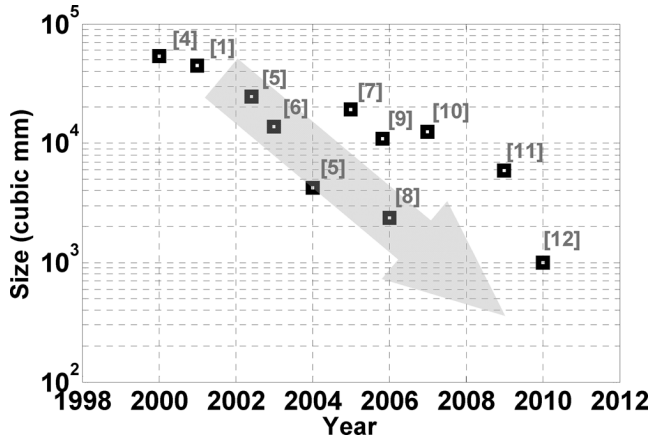

Fig. 1. Trend on size reduction of integrated WSN systems.

I. Introduction

THE tendency towards smaller wireless sensor network (WSN) nodes has opened the possibility of ubiquitous and unobtrusive sensing applications [1]–[3]. Over the past decade, researchers in both academia and industry have reduced the size of fully-integrated WSN systems by nearly two orders of magnitude. Fig. 1 summarizes the sizes of WSN node prototypes published in literature or commercially available versus year, showing the trend in size reduction of integrated WSNs [1]. Vanishingly-small, fully-integrated systems at the cubic millimeter scale represent the future of WSNs [1], [2], but present several integration challenges that may not be solved by CMOS scaling alone.

Conventionally, a WSN node is equipped with a radio transceiver, antenna, digital microcontroller, sensors, energy source such as a battery, and a crystal reference. Among all these building blocks, the RF front end and antenna could be scaled down in size by operating at a higher frequency due to the inverse proportional relationship to wave length. The digital circuitry could be scaled down in size by using advanced processes. Sensors for monitoring inertia, temperature, imaging, gravimetry, and chemical reactions can be integrated with CMOS technology on one silicon substrate [13]. The required battery volume could be reduced with the use of low-power or heavily duty-cycled circuit design [14], and thin film zinc/silver oxide batteries can be fabricated today that fit a 1 mm^2 form factor. However, there is currently no clear path to shrinking the size of the crystal reference oscillator and integrating it in a CMOS process with low power and low cost. Therefore, the crystal reference is one of the bottlenecks to realizing an extremely small WSN node, and crystal replacement with, e.g., CMOS or MEMS oscillators is currently an active area of research. Additionally, an external antenna, requiring custom packaging, is an obstacle that prohibits scaling to 1 mm^3 volumes.

In order to eliminate the bulky off-chip components and further reduce the size of a fully-integrated WSN node, we present a solution of using a 60 GHz on-chip patch antenna as both the radiator and frequency reference in this paper. The natural resonant frequency of the patch antenna serves as the frequency reference. At 60 GHz, the guided wave length is around 2.5 mm in silicon, which is comparable to the size of the active circuit blocks (e.g., radio, processor, and memory), and it operates in the 57–64 GHz industrial, science, and medical (ISM) band approved for unlicensed communication by Federal Communications Commission (FCC). The resonant frequency is mainly determined by the physical dimensions of the patch antenna, and the standard deviation, σ, due to process variation is around 1100 ppm. This accuracy level is suitable for, e.g., low-rate communication with a non-coherent energy-detection receiver. With the antenna reference, we fabricated a frequency-locked

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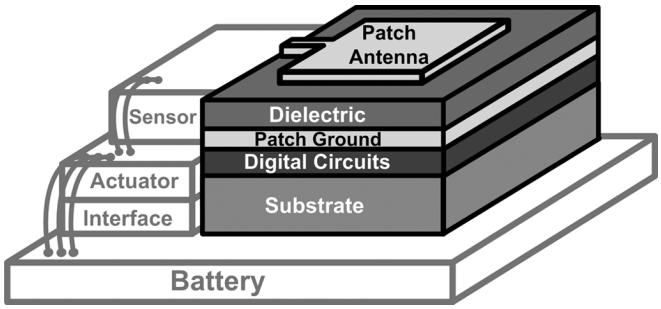


Fig. 2. Miniature, fully-integrated wireless sensor node system.

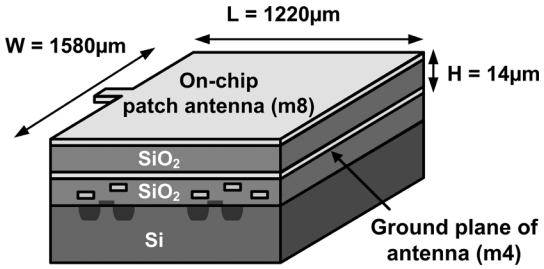


Fig. 3. Dimensions of the 60 GHz patch antenna.

loop (FLL) circuit to track the reference frequency for RF synchronization. Furthermore, the area beneath the patch antenna ground plane is investigated for containing additional circuits for higher integration. The mutual coupling between the antenna and the circuits beneath are tested by a coupling sensor array and a clock generator with a 16 node H-tree, showing that the 60 GHz patch antenna and the digital clock switching circuitry routed beneath the patch antenna can functionally work with the antenna ground plane shielding. Fig. 2 depicts the concept of a miniature WSN node system. By integrating the antenna, frequency reference, RF front end, and digital circuitry onto the same die, a form factor of 1 mm^3 is feasible.

This paper is organized as follows. Section II presents the design and analysis of the antenna reference. The FLL architecture and building blocks are described in Section III. Section IV discusses the mutual coupling effect between the antenna and the digital circuitry beneath, and Section V summarizes the measurement results.

II. Antenna Reference

A. Patch Antenna Design

As an on-chip radiator, the patch antenna topology is chosen because its ground plane shields the patch antenna from the lossy substrate in standard CMOS processes, and thus provides higher radiation efficiency than non-shielded integrated antennas. Moreover, the patch antenna is also a good candidate for system integration due to the reusable area beneath the ground plane for high noise margin digital circuits. In our design, we first determine how many metal layers are typically needed for digital circuit routings. The distance between the patch metal layer (top-metal M8) and the ground metal layer determines the height of the patch antenna. The tradeoff between radiation efficiency and height are discussed in [15]. The

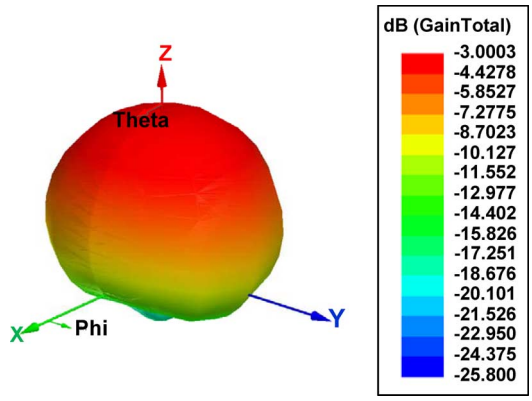


Fig. 4. Radiation pattern of the on-chip patch antenna.

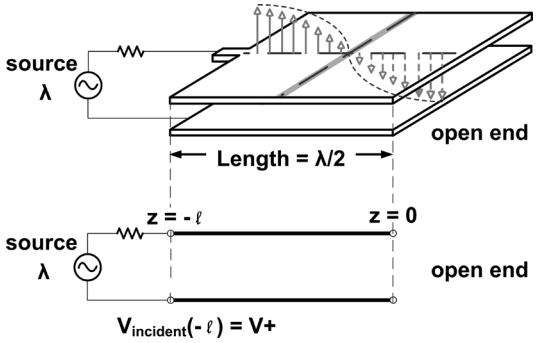


Fig. 5. Simplified lossless transmission line model of the patch antenna.

analysis suggests that lower antenna height (or a higher metal layer ground plane) results in lower radiation efficiency. In this design, Metal 4 is used as the ground plane, resulting in an antenna height of 14.1μm. Based on simulations, using Metal 4 for the ground plane instead of Metal 1 reduces the radiation efficiency by 15%, but frees up three metal layers for routing of circuits beneath the antenna. With the center frequency, f_0, dielectric constant of the silicon dioxide (SiO_2), ε_r, and the height h, we can calculate the width, W, of the patch antenna by antenna theory

$$W = \frac{c}{2f_o\sqrt{\frac{(\varepsilon_r+1)}{2}}} \tag{1}$$

where c is the speed of light [16]. With the calculated W, we can find the effective dielectric constant, $\varepsilon_{\text{reff}}$

$$\varepsilon_{\text{eff}} = \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2}\left(1+12\frac{h}{W}\right)^{-1/2}. \tag{2}$$

It follows that the length of the patch antenna, L is

$$L = \frac{c}{2f_o\sqrt{\varepsilon_{\text{reff}}}} - 0.824h\frac{(\varepsilon_{\text{eff}}+0.3)\left(\frac{W}{h}+0.264\right)}{(\varepsilon_{\text{eff}}-0.258)\left(\frac{W}{h}+0.8\right)}. \tag{3}$$

Note that the size of the ground plane is greater than the patch dimensions by approximately six times the height all around the periphery to achieve results similar to that of an infinite ground plane [16]. Fig. 3 illustrates the final dimensions of the patch antenna. The resonant frequency is mainly determined by the width and length which can be verified by back calculating for

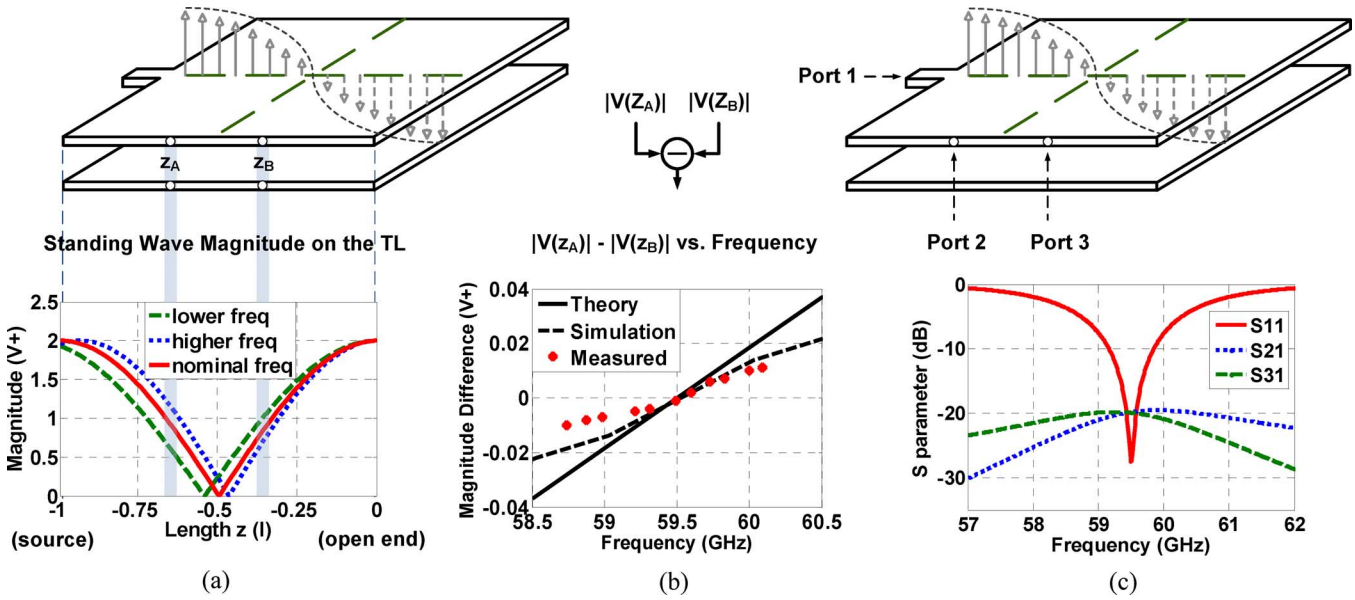


Fig. 6. Center frequency detection of the antenna reference: (a) standing wave magnitudes along the length for three frequencies at source, (b) the difference in magnitude of two taps Z_A and Z_B versus frequency, (c) S-parameter analysis of the 3-port antenna reference.

f_0 from (1)–(3) when W and L are known. The 3σ process variation parameters on length and width of the top metal layer are on the order of 400 ppm of the antenna parameters, resulting in the same order of accuracy of the resonant frequency of the patch antenna, determined by the first-order antenna theory. The simulated antenna radiation pattern is shown in Fig. 4. The simulation results include the effects of required dummy filling for meeting local metal density requirements, and show the center frequency is 60.54 GHz with a bandwidth of 920 MHz. The peak antenna gain is -3 dB while the efficiency at resonance is 15.6%.

B. Resonant Frequency Detection

To detect the resonant frequency of the antenna reference, we will need to understand the physical phenomena on the patch antenna when it is resonating. A simplified lossless transmission line model is adopted for this analysis. Fig. 5 shows the transmission line model corresponding to the patch antenna along the length axis. We may consider the patch antenna a very wide transmission line, with the feed point being the source terminal, while the other edge behaves as the open end. When the source frequency is exactly at the resonant frequency, the length of the transmission line is equal to $\lambda/2$, and a standing wave pattern is generated by the superposition of the incident wave from the source and the reflected wave from the load. Under these conditions, the patch antenna radiates at its peak efficiency value. The source end and open end have the strongest electric fields, and those are the radiation edges. Note that there is an electrical null located in the center of the length axis (e.g., $z = -l/2$), shown as the solid shaded area in Fig. 5. The amplitude of the standing wave on the transmission line as a function of the length can be written in the general form [17]

$$V(z) = V^+ \left(e^{-j\beta z} + \Gamma e^{j\beta z}\right) \tag{4}$$

where V^+ is the incident wave magnitude at $z = 0$, β is the propagation constant $2\pi/\lambda$, and Γ is the voltage reflection coefficient. When the load is open, Γ equals 1, thus the magnitude of the standing wave reduces to

$$|V(z)| = \left|V^+\right| \sqrt{[2 + \cos(2\beta z)]}. \tag{5}$$

Fig. 6(a) shows the magnitude plot of three standing wave patterns corresponding to three different source frequencies. Due to the open end boundary condition and different λ according to frequencies, the location of the electrical null moves along the transmission line length as frequency changes. When the source frequency is lower than the resonant frequency, the electrical null moves toward the source end. On the other hand, the electrical null will move toward the open end if the source frequency is higher than the resonant frequency. By monitoring the difference in voltage magnitudes at two taps Z_A and Z_B on the patch antenna that are equally spaced away from the center, a monotonic curve passing through zero can be traced out for resonance detection. Fig. 6(b) shows three monotonic curves, the solid line is derived from the lossless transmission line model, assuming perfect matching over the frequency band. The dashed line is obtained from Ansoft HFSS full-EM simulations of the three port antenna reference setup in Fig. 6(c), showing the discrepancy due to the limited bandwidth of the patch antenna. Measured results are shown as dots in Fig. 6(b), which follow the same trend as the simulation. Fig. 6(c) also shows the S-parameter analysis. $S21$ and $S31$ represent the ratio of power delivered onto Z_A and Z_B from the antenna feed point at Port 1. The two tap nodes are designed to be high impedance nodes, so that they do not load the patch antenna significantly, but provide enough voltage swing for the following envelope detectors to measure the standing wave magnitude. Simulation results show only 2% of the power delivered onto the patch antenna is lost on the two tap nodes.

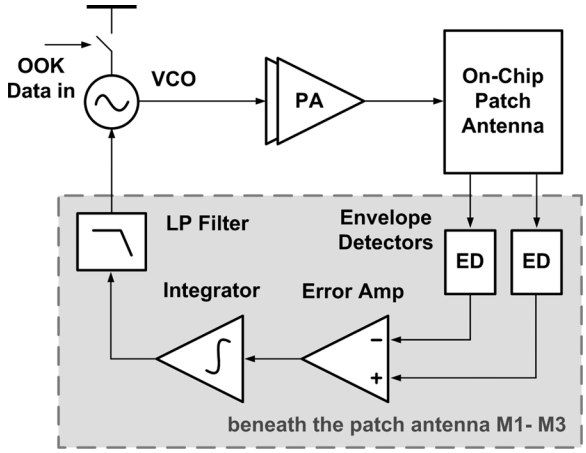


Fig. 7. Block diagram of the 60 GHz FLL.

The locations of the two taps are also important. A wider separation between the two taps provides a larger slope of the monotonic curve, thus a larger controller gain in the FLL and more accurate resonant frequency detection. However, the frequency locking range over which the sensed voltage magnitude difference remains monotonic is inversely proportional to the separation between taps. Therefore, if the separation is too wide for a target frequency range, the monotonic characteristic no longer applies, which could result in instability in the FLL. Furthermore, the two envelope detectors would be placed far away from each other on the chip, causing mismatch from separation within the single wafer [18], and thus affecting the accuracy of tracking the resonant frequency. In the final layout of the antenna reference, the two taps are equally spaced 110 μm away from the length center, resulting in a calculated locking range of 8.5 GHz. Another factor that will affect the locking range of the antenna reference is the antenna bandwidth. A larger bandwidth implies a wider locking range. In this case, the antenna bandwidth is around 1 GHz, which provides sufficient range for covering process variation of the patch antennas.

III. Frequency-Locked Loop

Fig. 7 shows the block diagram of the 60 GHz FLL. The FLL mainly consists of two parts; a feed-forward RF part and a feedback baseband part. The RF part comprises a differential VCO, a buffered output of the VCO, a power amplifier (PA), and the on-chip patch antenna reference. The baseband part functions as a PI controller, and has two envelope detectors, an error amplifier, an integrator and a loop filter. The VCO signal is amplified by the PA, and radiated through the antenna. The frequency of the VCO is regulated by the feedback baseband part. The VCO is designed to be on-off keying (OOK) modulated by power gating with header device, so that the FLL can serve as a simple low-rate OOK transmitter. Note that the baseband circuits highlighted in Fig. 7 are placed beneath the patch antenna ground plane using Metal 1 to Metal 3 routing layers. The optimal placement and routing to reduce crosstalk between the RF and baseband components will be discussed in Section IV.

A. VCO, Buffers, and PA

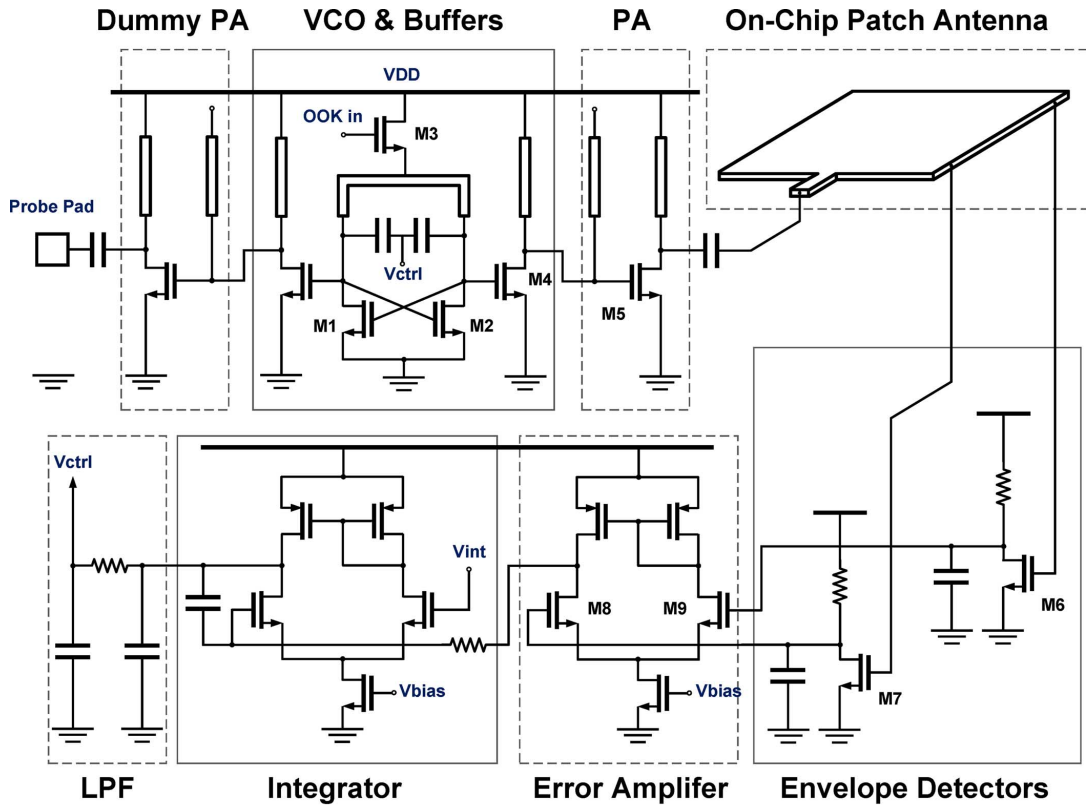
Fig. 8 shows the schematic of the 60 GHz FLL. The VCO uses a cross-coupled pair topology with an LC resonator. The resonator is realized by a half-wavelength transmission line at the top metal layer, and the simulated Q-factor of the resonator is 15 at 60 GHz. The frequency tuning is achieved by a pair of thin oxide NMOS varactors. One of the differential VCO outputs feeds the signal onto the patch antenna through a common source stage buffer and a PA. The PA is designed for maximum power delivery, using the top metal layer for high-Q transmission lines for matching. Ideally, we want to probe the signal at the antenna input, where the FLL output is. However, the pad and probing might destroy the matching condition between the PA and the antenna, so the secondary output of the differential VCO is used for testing, and is connected to an RF probe pad through a dummy PA. In this way, we can monitor the FLL output frequency. However, the absolute output power is not available through direct measurement due to an extra 500 μm routing that is necessary for the on-chip probing pads setup. The simulated FLL output frequency and power are 60.12 GHz and -3.6 dBm, respectively. The measured power consumption of the VCO core, buffers, and PA are 8.8, 2.6, and 16.0 mW, respectively.

B. Envelope Detector

The envelope detectors sense the magnitude of the standing wave on the antenna, and down-convert the signal from 60 GHz to DC. An active envelope detector topology is used for larger output voltage levels, which is a class-AB biased amplifier with parallel RC load at the output [19]. The bias of the two envelope detectors is critical, and the connection through the patch antenna ensures the DC voltage at both gates of the envelope detectors are the same. The setup also makes sure the patch antenna is not DC floating when it is operating. Moreover, large devices are used and they are laid out in close proximity to lower the mismatch between the two envelope detectors [18]. The simulated offset voltage of the envelope detector inputs due to process variation is 190 μV, corresponding to a frequency offset of roughly 6 MHz. By changing the bias gate voltage and the drain current, the input node of the envelope detectors can be designed as high impedance nodes, so that the two taps on the edge of the patch antenna do not significantly affect the standing wave pattern. The measured power consumption of one envelope detector is 670 μW.

C. Error Amplifier, Integrator, and Loop Filter

The error amplifier provides the difference and controller gain for the FLL. It is an amplifier with a differential input and an active load for single-ended output. 20 dB of gain and 300 MHz bandwidth is obtained from this stage. The simulated offset voltage at the input of the error amplifier is 52 μV, corresponding to a frequency offset of roughly 11 MHz. The integrator introduces a pole at DC, minimizing the steady state error between the FLL output and the natural resonant frequency of the patch antenna. Bias conditions of the error amplifier, envelope detectors and the integrator must be considered together for the proper input voltage range and gain margin. The loop filter stabilizes the FLL and is realized by a distributed



M1	M2	M3	M4	M5	M6	M7	M8	M9
12.8	12.8	50.0	6.4	26.0	50.0	50.0	18.0	18.0
0.12	0.12	0.12	0.12	0.12	0.48	0.48	1.00	1.00

Fig. 8. Schematic of the 60 GHz FLL.

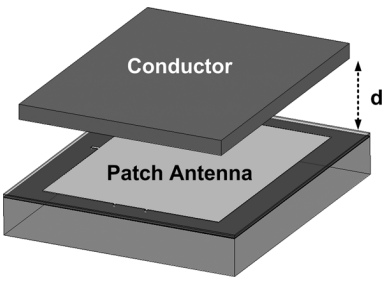


Fig. 9. Proximity effect setup of the patch antenna.

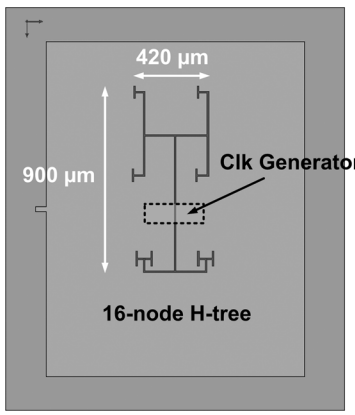


Fig. 10. 16-node clock H-tree beneath the antenna ground plane.

resistive transmission line with metal comb capacitor units with a self-resonant frequency above 60 GHz. The cutoff frequency of the loop filter is designed to be 100 MHz.

D. Proximity Effect on the Patch Antenna

In practical applications, the properties of the antenna will be affected by application-specific scenarios in which objects are placed near the radiating element. This will affect communication in two ways: 1) similar to any radio, the transmitted signal will be attenuated by the interfering object and 2) specific to this antenna-referenced FLL, the resonant frequency of the antenna will shift and the FLL will track the shift. In the latter case, the transmission line theory still applies, but the center frequency and the bandwidth will change. Fig. 9 shows a simulation setup for characterizing the proximity effect when a conductor appears in close proximity to the antenna. Full-EM simulations show that when a copper patch of the same size of the patch antenna is placed directly in front of the antenna at a distance of 500 μm, the center frequency shifts by 67.6 MHz (0.1%). This value is equivalent to the 1σ standard deviation on center frequency due to process variation alone, and is not enough to compromise FCC compliance in the 60 GHz ISM band. The bandwidth is also impacted by the metal in front of the antenna, and it reduces by 17%. The frequency shifts caused by nearby

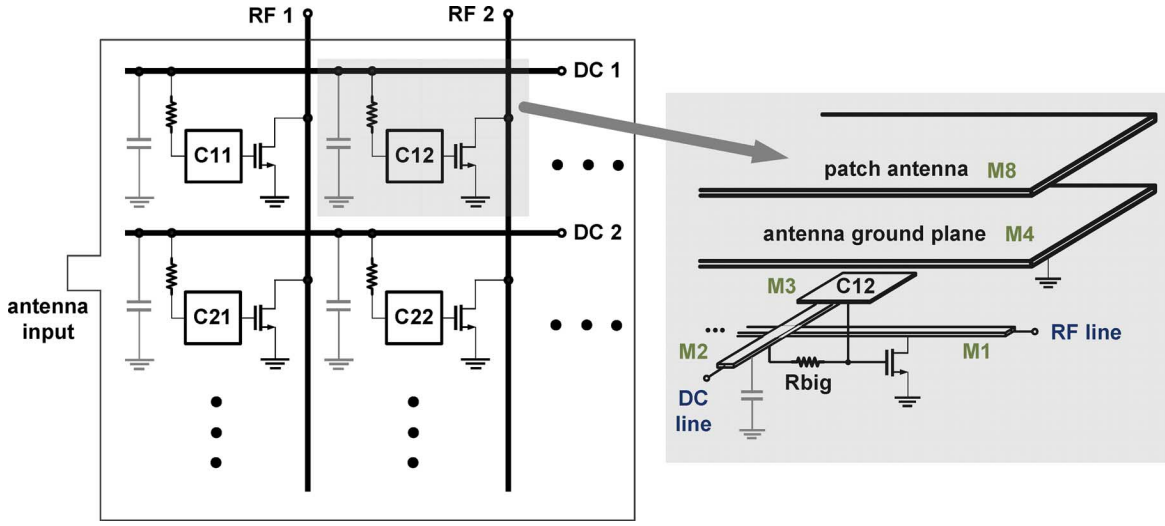


Fig. 11. 60 GHz coupling sensor array.

metal and by process variation are uncorrelated, so the center frequency of a blocked antenna has the same distribution due to process variation as the unblocked one, but with a shifted mean. Therefore, including worst-case 3σ process variation and the effects of interfering metal 500 μm away, two patch antennas can still communicate with each other.

Moreover, the case when a strong interfering signal is incident on the antenna should be considered. An interfering signal with random phase could cause constructive or destructive interference to the standing wave pattern on the patch antenna. A patch antenna is a relatively narrow band filter, so the interference which is close to the center frequency is most likely to be picked up by the antenna. Simulation results show that when we introduce an interference tone that is 1% lower in frequency and 50% lower in power level than the VCO output but with different phases, the transmitter output shifts -5% away from the nominal value. While this high of power typically would not be seen in a WSN of these nodes, this does place limitations on the proximity of this transmitter to other high-power 60 GHz radiators.

IV. Circuitry Beneath the Patch Antenna

Because the patch antenna and the baseband circuits beneath are working simultaneously in the FLL, the crosstalk between them is important, and it is a general issue for system integration as well. Coupling can happen in two directions. A digital signal operating beneath the ground plane could be picked up by the patch antenna, and then radiated, causing the chip to exceed the FCC noise emission mask. On the other hand, the 60 GHz RF signal on the patch may couple to the baseband circuits causing malfunction of the feedback loop, digital logic, or memory. We know the patch ground plane helps with shielding. However, a more detailed discussion and experiments on spatial placement and routing are presented in this section.

A. Coupling From Circuits Beneath to the Antenna

The digital clock and full-Vdd logic switching are considered low frequency noise sources to the RF signal on the patch antenna. In order to verify the shielding ability of the antenna ground plane, we fabricated a replica patch antenna over a clock generator with a 16-node clock distribution tree on a separate die, which is shown in Fig. 10. The clock generator is a 5-stage ring oscillator with a center frequency around 400 MHz. The H-tree is located in the middle of the patch antenna, using Metal 3 as the routing layer. There are repeaters every 100 μm along the tree, and it occupies an area of 420 μm$\times$ 900 μm. The experimental result shows that, when a 1.2 V_{pp}, full-swing, 322 MHz clock signal is running on the H-tree, we are able to detect the presence of the clock signal using a RF probe pad connected to a Metal 1 trace that capacitively couples to the clock H-tree. This step is to make sure the clock is running. Then we move the probe a port on the replica patch antenna at Metal 8. With 10 kHz resolution bandwidth and a noise floor level of -98.2 dBm, we did not observe the 322 MHz clock signal or its harmonics on the patch antenna. The -98.2 dBm noise floor is far below the -41.3 dBm/MHz noise emission mask allowed by the FCC. The experiment shows that the low-frequency noise coupled from the circuit beneath onto the patch antenna is negligible due to the ground plane shielding.

B. Coupling From the Antenna to the Circuit Beneath

The circuits beneath the antenna ground plane need good isolation to function correctly. At 60 GHz, it is assumed that the electric field distribution on the antenna dominates the coupling between the patch and substrate; in other words, the magnitude of coupling will follow the standing wave pattern along different locations beneath the antenna. In order to verify this, we fabricated a coupling sensor array under the replica patch antenna to measure the coupling magnitude at different locations beneath the antenna. Fig. 11 shows a schematic of 4 sensor cells of the coupling sensor array (not drawn to scale). In the test chip, there are 8 by 7 cells, a total number of 56 sensors, spread over half of the antenna-covered area.

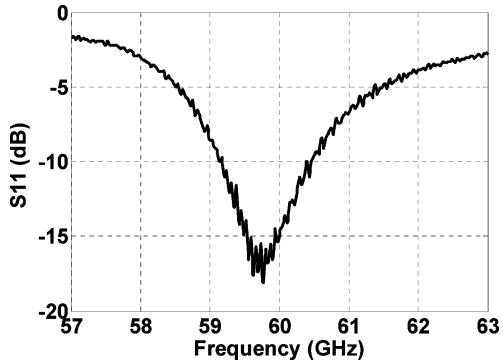


Fig. 12. Measured $S11$ of the replica patch antenna.

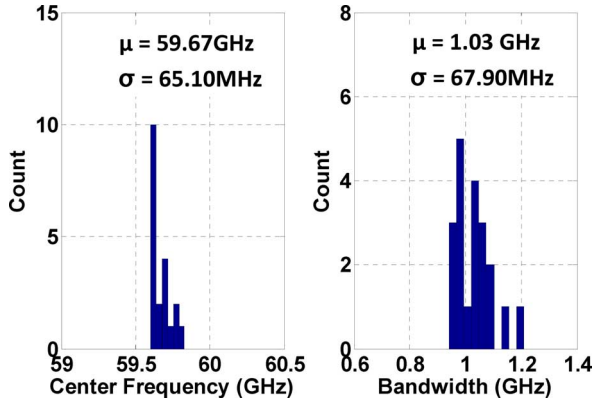


Fig. 13. Antenna resonant frequency and bandwidth distribution over 20 replicas.

Each sensor cell has a 60 μm$\times$ 60 μm sensor pad at Metal 3 (directly below the Metal 4 ground plane) and an amplifying transistor, with the drain of the transistors connect to a RF line at Metal 1 and the gate of the transistors connect to a DC line through a large resistor. The goal of the circuit is to sense the coupling signal individually at each sensor pad. The pads are drawn at the Metal 3 layer so that the strongest coupling is sensed. The RF line, the most sensitive signal trace, is on the Metal 1 layer, reducing the global coupling directly from the antenna to the RF line. The RF output is connected to Port 2 of an Agilent E8361A vector network analyzer (VNA), while providing a DC bias through a bias tee, and with Port 1 connected to the replica antenna input shown in Fig. 11 through on-chip probing. The DC lines are orthogonal to the RF lines for probing purposes, and there are large capacitors connecting from the DC lines to ground to reduce global coupling onto the DC lines and then onto the RF lines. There is also a column of dummy sensors that contains one RF line and 8 DC lines providing different sensor cell gain numbers for calibration. Because we use the same bias voltage for all of the sensor cells, the gain differences mainly come from different load impedances according to the locations where the sensor cells connect their drain terminals to the RF line. We use the dummy sensors to characterize the impact of the different load impedances.

When measuring sensor cell C11 (see Fig. 11), we first probe RF line 1 and measure the $S21$ when the whole array is turned off, and then measure the $S21$ again when RF line 1 and DC line 1 are providing the bias for cell C11. The latter $S21$ is denoted as $S21'$ and there is a general relationship

$$S21_{\mathrm{xy}} + C_{\mathrm{xy}} \times G_{\mathrm{y}} = S21'_{\mathrm{xy}}. \tag{6}$$

Where $S21_{\mathrm{xy}}$ is the $S21$ when cell C_{xy} is selected but the DC bias is off, and C_{xy} is the coupling signal that corresponds to that sensor cell, which is the desired result. G_y is the gain of the y^{th} sensor cell from the dummy sensor cell column. $S21'_{\mathrm{xy}}$ is the $S21$ when cell C_{xy} is selected and the DC bias of the cell is also on. By (6), we can measure and calibrate out the coupling noise from other locations to obtain the small coupling signal C_{xy}. The algorithm relies on the sensitivity of the VNA, because the coupling signal C_{xy} is predicted to be on the order of at least -50 dB [15]. Moreover, the gain of the dummy sensor is not high at 60 GHz without proper matching. So the magnitude difference of $S21_{\mathrm{xy}}$ and $S21'_{\mathrm{xy}}$ may be small. The Agilent E8361A network analyzer has a dynamic range of 94 dB and a trace noise smaller than 0.006 dB from 10 MHz to 67 GHz [20]. The measurement results are shown in Section V.

V. Measurement Results

A. Antenna Reference

In order to test the antenna resonant frequency and bandwidth, we fabricated a second chip in the same 0.13 μm CMOS process that has a replica patch antenna with the same dimensions as the one in the FLL. Twenty of the replica antennas were tested, and Fig. 12 shows one of the measured $S11$ plots of the antenna with a frequency span of 6 GHz. The center frequency is around 59.8 GHz with a bandwidth of 1.2 GHz. Fig. 13 shows the distribution on measured resonant frequency and bandwidth over 20 replica patch antennas. The mean and standard deviation of the center frequency is 59.7 GHz and 65.1 MHz, respectively. The mean and standard deviation of the bandwidth is 1.03 GHz and 67.9 MHz, respectively. This results in a 3σ variation in center frequency of 3270 ppm, ensuring it is FCC compliant in the 60 GHz ISM band. In order for the transmitter to reliably communicate with, e.g., an energy-detection receiver with an identical patch antenna (not included in this work), process variation should not cause the transmitter frequency to fall outside the bandwidth of the receiving antenna. Assuming a worst-case 3σ variation on all parameters from process variation, the frequency response of two patch antennas would overlap. Based on the measured $S11$ of 20 dies from a single wafer, no missed alignment between two antennas was observed.

B. Coupling Sensor Array

Fig. 14 shows the surface plot of the attenuation of a 60 GHz signal coupled to the area beneath the antenna ground plane measured by the sensor array described in Section IV-B. The x- and y-axis correspond to the coordinates of the physical locations under the antenna. The measured results from the 56 coupling sensors covers half of the antenna, and we mirror the results and plot them in a white mesh format because of the perfect symmetry for the antenna. Compared with the simulated results, the measurement has a general 20 to 25 dB increase in magnitude. This is likely due to the measurement accuracy of

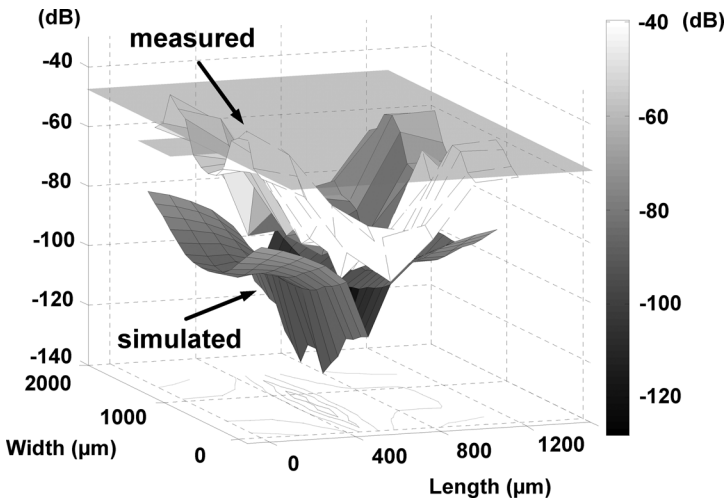


Fig. 14. Surface plot and contour of 60 GHz signal coupled from M8 patch antenna to M1 and the white mesh is the mirrored plot from the measured half.

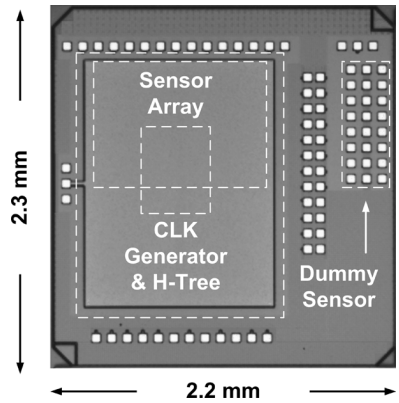


Fig. 15. Micrograph of the die for characterization.

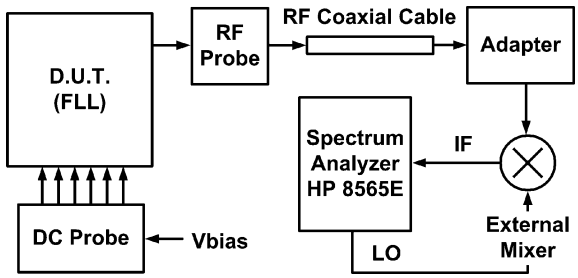


Fig. 16. Test setup for the 60 GHz FLL.

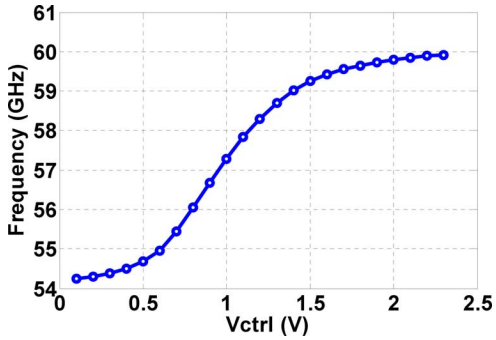


Fig. 17. Tuning range of the VCO in the FLL.

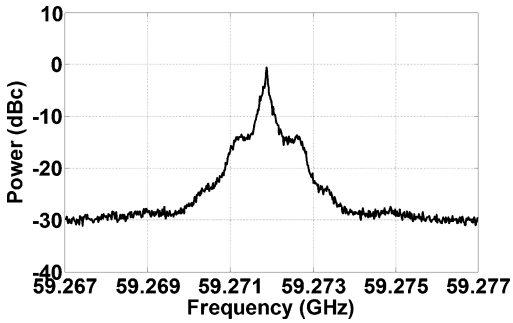


Fig. 18. Output spectrum of the FLL in 10 MHz span.

a very small coupling ratio. Even with calibration, a small difference on $S21$ or the gain of the dummy sensor cell measurement will cause large offsets in the coupling calculation from (6). However, the measured result has a similar coupling shape and contour to the simulated result. It not only verifies the impact of the standing wave pattern on the coupling effect, but also provides a guideline for placing and routing the circuits beneath the ground plane for minimum coupling. Fig. 15 shows the micrograph of the die used for characterization. It has the replica patch antenna, 60 GHz coupling sensor array, clock generator, and the 16-node H-tree. The sensor array occupies an area of 800×1200 μm.

C. Frequency-Locked Loop

The FLL is fabricated in a 0.13 μm CMOS process and the power consumption (excluding the dummy PA to test pads) is 29.6 mW. Fig. 16 illustrates the test setup for characterizing the 60 GHz FLL. Fig. 17 shows the tuning range of the VCO in the FLL, which covers $\pm 3\sigma$ of the patch antenna resonant frequency. The output spectrum measured with a 10 MHz span while the FLL is locked is shown in Fig. 18. The locked frequency is at 59.27 GHz, which is within the variation of the replica antenna. There are no reference spurs in the output spectrum, which would typically appear in a frequency synthesizer with a crystal reference multiplied by a PLL [14]. Fifteen FLLs

TABLE I
FLL PERFORMANCE SUMMARY

	[21]	[22]	[23]	This Work
Type	PLL	Frequency Synthesizer	OOK TX	FLL
Technology	90nm CMOS	90nm CMOS	90nm CMOS	0.13μm CMOS
Power	88.0mW	80.0mW	183.0mW	29.6mW
Frequency	75GHz	60GHz	60GHz	60GHz
Antenna	N/A	N/A	Off-Chip	On-Chip
Area	0.80mm^2	0.95mm^2	0.43mm^2	2.85mm^2
Active Circuit Area	0.80mm^2	0.95mm^2	0.43mm^2	0.64mm^2

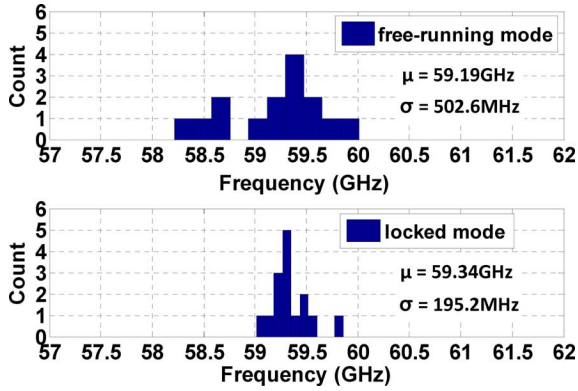


Fig. 19. Frequency distribution of the FLL in different modes.

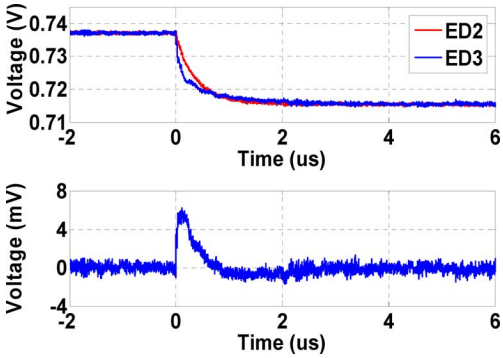


Fig. 21. Transient response of the two envelope detector outputs when turning the FLL on and the envelope outputs difference for settling time characterization.

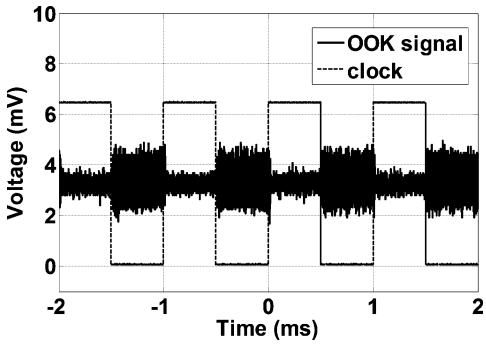


Fig. 20. OOK modulating the VCO at 1 kbps.

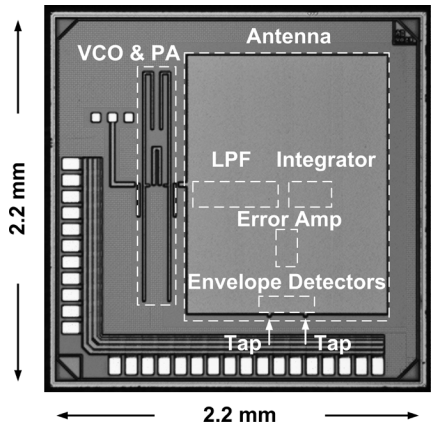


Fig. 22. Die micrograph of the 60 GHz FLL.

from a single wafer were tested, and Fig. 19 compares the frequency distribution of the free-running VCO when the feedback loop is off, and when operating in locked mode. The mean center frequency is 59.34 GHz, with a standard deviation of 195 MHz. Compared to the 503 MHz standard deviation of the free-running VCO, the FLL provides an improvement in frequency variation, while eliminating the need for an external reference and tracking the peak-efficiency frequency of the integrated antenna. We can compare this antenna reference technique to using an open-loop fixed LC oscillator, which would have benefits of simplicity and lower power consumption than the FLL approach. However, some extent of post-process calibration will be required with the fixed LC oscillator to account for process variation (even though CAD tools can provide accurate predictions of the resonant frequency for both an LC tank and a patch antenna). In the fixed LC oscillator case, calibration of the center frequency requires 60 GHz measurements, which is not cost-effective (e.g., 60 GHz divider) and is time consuming (e.g., RF testing). The antenna reference therefore provides a cost-effective method for closed-loop regulation of the transmitting frequency to the peak efficiency point of the antenna.

Fig. 20 shows the FLL Tx signal when the VCO is being OOK modulated at 1 kbps. The signal amplitude is small because it is down-converted through a passive harmonic mixer which has an uncalibrated attenuation; therefore, this plot simply verifies the OOK functionality. Fig. 21 shows the two envelope detector

output signals when the FLL is OOK modulated and the difference of the two envelope detector outputs as the error signal. The settling time is around 3 μs once the loop is turned on; therefore, the VCO can be powered on and FLL locked during every bit transmission for data rates less than around 200 kbps. The measured results of the FLL are summarized in Table I and compared with a state-of-the-art PLL, frequency synthesizer and OOK transmitter. While a frequency synthesizer requires a crystal reference, this antenna-referenced FLL performs closed-loop frequency regulation without any off-chip components. A die micrograph of the FLL is shown in Fig. 22. The FLL occupies 1.60×1.78 mm^2 without pads.

VI. Conclusion

A FLL in a 0.13 μm CMOS process using an on-chip patch antenna as both the radiator and the frequency reference has been demonstrated. The proposed technique efficiently integrates the antenna, eliminates the need for a crystal reference, is FCC compliant, and ensures the node transmits at the antenna's peak efficiency. The substrate beneath the antenna is shielded by an intermediate metal layer ground plane, freeing up space for active circuits and routing beneath the patch. By integrating circuits in CMOS underneath the patch, and stacking the die on e.g., a thin-film battery, a fully integrated, cost-effective, mm^3-scale WSN node is feasible.

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