An Ultra-Low-Power 9.8 GHz Crystal-Less UWB Transceiver With Digital Baseband Integrated in 0.18 μm BiCMOS

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***Abstract*—This paper presents a fully-integrated IR-UWB radio, designed to operate within the limits of mm-scale micro-battery for cubic-mm sensor nodes. It includes an RF front-end, battery current limiter, baseband modem with I2C interface, and temperature-compensated relaxation oscillator for frequency generation without a crystal. The peak current draw from a modern mm-scale battery must be <100 μA, below a radio's active power consumption. Thus, duty-cycling the radio only at the packet level is not an option, and so this IR-UWB radio includes an integrated modem which duty-cycles the RF front-end at the bit-level. A current limiter protects the battery from over-current conditions, and the radio operates from on-chip storage capacitance that is recharged between bits. The radio operates at 30 kb/s with a center frequency of 9.8 GHz. It consumes 291 μW average power in transmit mode while broadcasting 0.1 dBm pulses, and 306 μW in receive mode with a sensitivity of –77 dBm. The area of the radio is 2.73 mm².**

***Index Terms*—CMOS, I2C, radio transceivers, UWB, wireless sensor networks.**

I. Introduction

THE continual evolution of computing devices has changed daily life significantly over the past several decades. Mainframe computers from the 1950s previously occupied large rooms due to their substantial size and provided the basic data computation for hundreds of employees in a company. Nowadays, smartphones have become the platform of personal computing, as predicted by Bell's Law [1]. Bell defines a computer class as a set of computers with similar cost, programming environment, network, and user interface, where each class undergoes a standard product life cycle of growth and decline. Based on prior market trends, a new computer class has come into existence approximately every decade, and each successive class has had a 100× reduction in volume (Fig. 1). In addition, each successive class has resulted in a reduction in unit cost and an increase in the volume of production [2]. Various applications, such as sensing, wireless communication, digital identification, and un-obtrusive surveillance, have driven the computing devices to a more compact regime (cubic-mm-scale) with higher production volumes compared to prior computing classes. Wireless sensor networks (WSNs) are perceived as the next big step in this decades-long trend toward smaller, more ubiquitous computing. They are projected to reach quantities of 1000 sensors per person by 2017 [3].

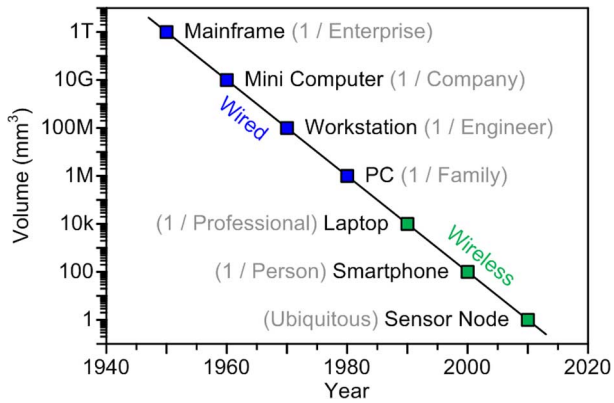

Fig. 1. The long-term trend in computer scaling over the years [1].

WSNs applications vary widely in different fields. However, it is apparent that the hardware design plays an important role for specific purposes. Compact hardware size along with long lifetime is generally desirable, nonetheless, quite challenging. Fig. 2 shows the block diagram of a typical WSN node. An integrated WSN node generally has several sensors, a digital signal processor (DSP) and controller, voltage regulation for power management, a radio frequency (RF) front-end and antennas for wireless communication, a battery as the energy source, and a crystal for frequency reference. Among these building blocks, the crystal reference and power source have been the most difficult to integrate into silicon [4], thus hindering the miniaturization towards cubic-mm scale WSNs.

A frequency reference provides a stable timing reference over process, voltage and temperature (PVT) variations for RF and clock synchronization of a communication system. The required timing accuracy depends on the system specifications [5] and can be achieved in different ways. A quartz crystal is the most common source of frequency reference. It provides excellent stability with PVT variations. However, their volume does not

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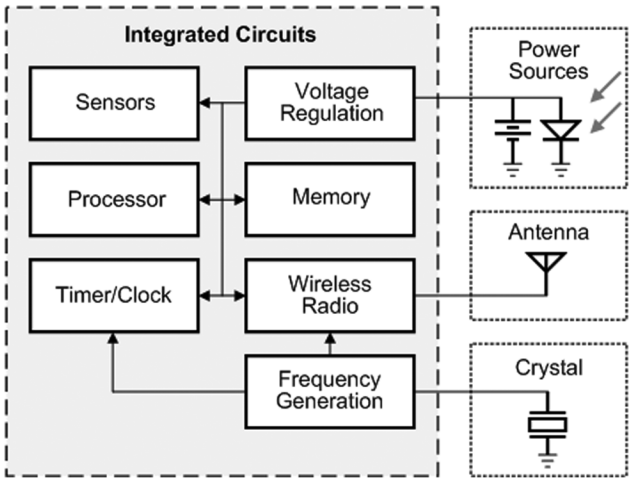

Fig. 2. Block diagram of a typical WSN node.

scale down with process or frequency, and they require a piezoelectric process which is incompatible with monolithic integration. In order to get stable oscillation out of crystals, a certain amount of driving power is still necessary [6]. Therefore, the bulky size and cost of system integration become one of the bottlenecks for implementing crystals in mm-scale WSN nodes.

Micro-batteries are commercially available today with volumes approaching 0.2 mm^3. However, they have limited capacity because of the small volume. Furthermore, peak current and capacity directly trade off in solid-state batteries, and because capacity is typically maximized, the peak current of micro-batteries is small (i.e. high output resistance) [7]–[11]. For example, an $1.38 \times 0.85 \times 0.15$ mm custom lithium-ion (Li-ion) battery from Cymbet Corporation, the capacity is 1 μAh (Fig. 3) and the maximum measured discharge current is 10 μA [7]. The average power consumption must be <1 nW for a one year node lifetime—therefore, leakage current is critical. These limitations present a direct challenge to the radio circuits, which typically consume > 100 μW when active. In order to function under this constraint, the node must be duty-cycled heavily; it must harvest energy from other sources; or the battery capacity must improve significantly. From a circuit design point-of-view, energy usage must also be reduced by clever circuit techniques.

In order to realize a fully-integrated wireless node at the mm-scale that operates off a micro-battery, this paper presents a 9.8 GHz impulse-radio ultra-wideband (IR-UWB) radio in a 0.18 μm BiCMOS technology. The use of a SiGe process provides higher breakdown voltages, higher transconductances, and higher current on/off ratios when compared to standard CMOS processes in general. These criteria are crucial for a radio design with a high supply voltage and low sleep power. This radio includes current-limiting at the battery supply to prevent it from exceeding the peak current of the battery, which would degrade capacity and lifespan. The charge coming from the battery is stored on a local storage capacitor, so that it can be discharged at higher currents for a short amount of time when the RF front-end is enabled and recharged between bits. IR-UWB communication is chosen because the pulse-based modulation scheme naturally provides the smallest duty-cycling ratio [12]. The integrated modem of the radio duty-cycles the RF front-end at the bit-level, and is controlled through an I2C controller. The crystal reference is replaced with a temperature-compensated relaxation oscillator. The RF operation frequency is at 9.8 GHz considering the tradeoff between the circuit power consumption and antenna size. Finally, this radio is designed to operate the RF blocks over the entire battery voltage range of $3.2 \sim 4.1$ V [7].

This paper is organized as follows. Section II presents the design and analysis of the IR-UWB transceiver. The temperature-compensated clock generator is described in Section III. Section IV discusses the current limiter, and Section V described the baseband controller. Finally, Section VI summarizes the measurement results before some concluding remarks.

II. IR-UWB Transceiver Design

The architecture for the IR-UWB radio is shown in Fig. 4. The receiver (RX) and transmitter (TX) operate at the battery voltage (3.2–4.1 V), through a current limiter (CL) to protect the micro-battery from over-current and under-voltage conditions. An internal 3 nF storage capacitor made of MIM layers allows higher current draws from the TX and RX during duty-cycled operation. Digital baseband blocks operate from a 1.2 V $\mathrm{V_{DD}}$ to reduce power consumption, regulated by a power management IC stacked above the radio (a separate die). The baseband controller consists of a finite state machine (FSM) and memory for transmitting and receiving data. To survive on the limited resources of the micro-battery, all blocks on the radio have a low-power sleep state. RF and other analog blocks are duty-cycled at the bit level by the baseband controller, while baseband blocks are duty-cycled at the packet level by a separate sleep controller. The sleep controller remains on continuously unless an under-voltage condition occurs. The sleep controller begins and ends the wake-up procedure for each packet via I2C communication. The I2C controller has modified I/Os with keeper latches to eliminate pull-up resistors, and provides bidirectional communication with other stacked die in a mm-scale sensor node.

A. Transmitter

The TX operates over the entire supply voltage range of a micro-battery, generates tunable pulse durations and center frequencies, and draws its active power from the on-chip local storage capacitor when transmitting. During a pulse, the TX draws the maximum on-current from the capacitor to generate the largest possible signal. Within the FCC mask of -41.3 dBm/MHz, the output power is maximized to provide maximum communication distance. Therefore the maximum transmit power is limited by the on-chip capacitor size (3 nF), and the maximum pulse repetition frequency (PRF) is set by the peak battery drawn current. The TX and RX share the same local storage capacitor, so the node may either transmit or receive data at any given time. To generate a pulse, the baseband controller sends a positive edge-triggered transmit enable step, TX_en. This edge is pulse-position modulated (PPM) by the digital baseband to encode the data. The pulse generator then converts the step into a pulse with a 4-bit tunable pulse generator with a range of 1.2 ns to 6.0 ns. This pulse then

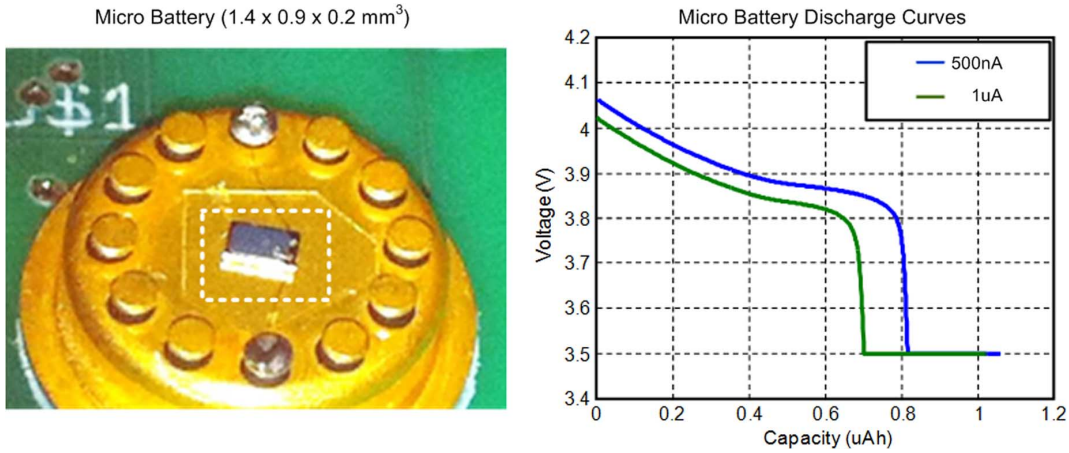

Fig. 3. Micrograph of the Cymbet micro-battery and its discharge curves.

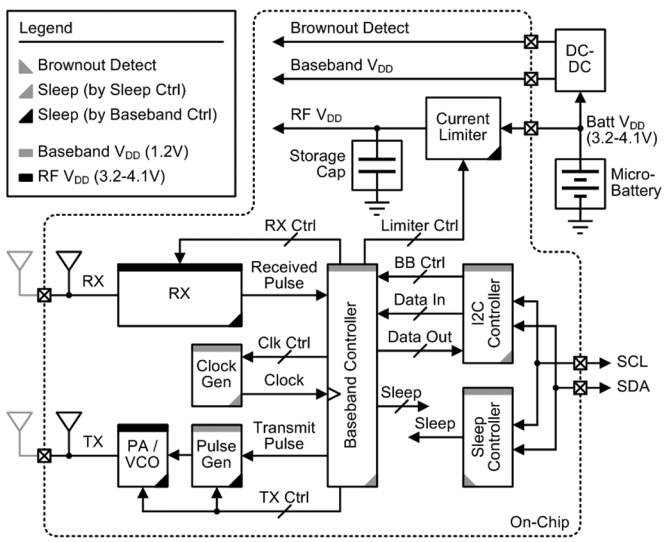

Fig. 4. System block diagram of the entire crystal-less UWB radio.

enables the TX front-end. The TX front-end consists of a combined voltage-controlled oscillator (VCO) and power amplifier (PA). The VCO/PA block operates at the RF supply voltage for higher output power during the short period of on-time.

Fig. 5 shows the schematic of the TX. The LC cross-coupled topology is chosen for fast turn-on time. In addition, the transformer-coupled scheme boosts the output signal swing. The area of the internal matching network between the VCO and PA is reduced by direct transformer coupling. The dimensions of the transformer are specified in Fig. 5. The inductances and coupling coefficient for the primary and secondary are 270 pH, 900 pH, and 0.66 respectively, from HFSS simulations. In order for the baseband controller to calibrate the center frequency, a capacitor bank with 3-bits of coarse tuning and 4-bits of fine tuning is implemented and shown in Fig. 5. The capacitor bank targets a tuning range of 8 GHz to 12 GHz, which is $\pm 10\%$ of the center frequency, so that the TX can be tuned to align with the RX. The capacitor, $\mathrm{C_c}$, controls the oscillating signal magnitude on the base terminals, and it is designed so that the voltage swing will never exceed the breakdown voltage of $\mathrm{Q_1}$ and $\mathrm{Q_2}$ at RF $\mathrm{V_{DD}}$. The bias circuit sets the base voltage, $\mathrm{V_b}$ and current of the cross-coupled pair $\mathrm{Q_2}$ and $\mathrm{Q_3}$.

While the TX is generating a pulse, the voltages at the local storage capacitor will drop. While the recharge current of the capacitor is set by the CL, the charging time for $\mathrm{V_b}$ is set by $\mathrm{R_c}$ and $\mathrm{R_b}$. The tail device $\mathrm{Q_1}$ is large, such that it enters the saturation region quickly once the $\mathrm{V_{tail}}$ signal is high. 60 mA of current is drawn from $\mathrm{Q_1}$ when the VCO begins oscillating. However, because of the high on-to-off current ratio of the bipolar transistors $(> 10^8)$, the sleep power of the TX is sub-nA. Note that the efficiency of the TX is 0.5% by simulation. In order to achieve a fast turn-on time for bit-level duty-cycling, the PA is replaced by a VCO with direct transformer-coupling to the output. As a result, the settling time of the PA is eliminated for the fastest possible turn-on time, but it requires a large bias current to achieve adequate output power. In the proposed transceiver, the TX and RX are not on simultaneously. Since the TX is only on and drawing current for $\sim$2 ns for each pulse, it does not deplete the stored energy in the capacitor. Therefore, the goal was to draw maximum current during a pulse so that output power is maximized for the longest communication distance rather than the highest efficiency.

B. Receiver

The RX includes RF gain stages, down-conversion, and pulse detection for PPM communication. The receiver amplifies and digitizes UWB pulses using the architecture shown in Fig. 6. Four RF gain stages amplify the incoming 9.8 GHz UWB pulses before down-converting them to DC using a squaring mixer. The signal then passes through a baseband gain stage before the signal path is split. Along one path, the UWB pulses are passed directly to the comparator while a low-pass filter (LPF) provides an auto-zeroed reference level along the other path. Finally, a continuous-time latching comparator with controllable hysteresis digitizes the incoming pulses and latches the output until it is reset at the next clock cycle.

The schematic of the RX along the signal path is shown in Fig. 7. The received RF signal is sent on-chip then amplified by four common emitter amplifiers with LC loads. The amplifiers use BJTs instead of FETs for higher gain efficiency $(\mathrm{g_m/I_C})$ and lower leakage currents. To improve stage-to-stage isolation

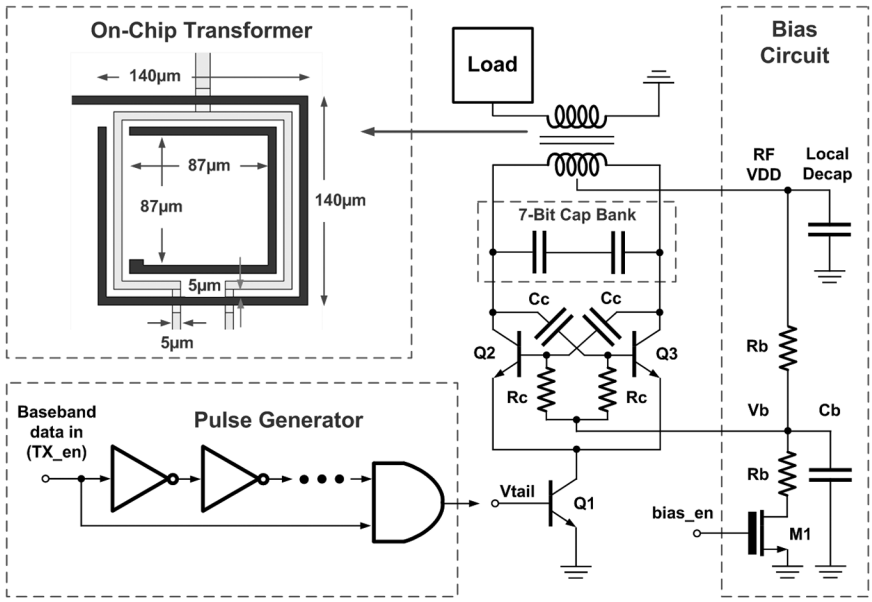

Fig. 5. Schematic of the UWB TX.

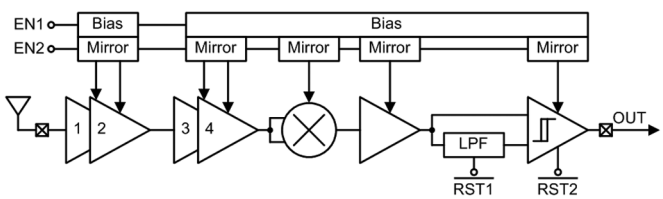

Fig. 6. Block diagram of the UWB RX.

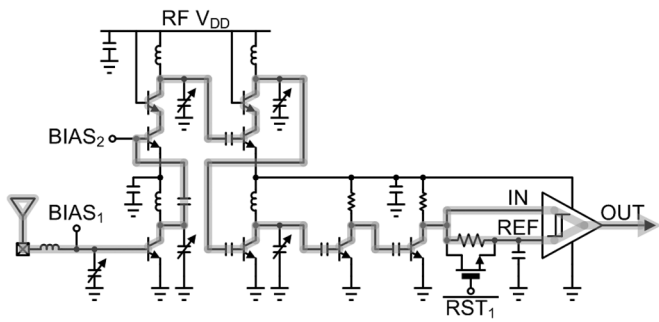

Fig. 7. Schematic of the RX along signal path.

and minimize feed through, cascoding is employed on the 2nd and 3rd gain stages. Based on simulation results, the four RF amplifiers can provide 34 dB of gain before down conversion. Load capacitance is adjusted via four binary-weighted control bits to tune the center frequency. After RF amplification, the signal is self-mixed to DC using a common emitter amplifier with resistive load, while a second amplifier provides additional baseband gain. The two stages are AC-coupled together to simplify biasing, but this results in some lost signal energy. The wideband nature of a UWB pulse, however, ensures that most of the energy is recovered. The baseband signal then is passed to the input of a continuous-time hysteretic comparator for broad band pulse detection. Low-pass filtering is accomplished with a RC network. The RC network also creates an auto-zeroed comparator reference level which provides interference rejection of in-channel continuous-time, constant-energy signal. However, because this is an energy-detection architecture, the peak signal power to interference ratio (SIR) at the detector during a pulse must always be positive. As long as the peak pulse power is roughly twice an interfering tone power at the detector, the RX can reliably detect the pulses. The filtering and amplification before the detector will help improve the SIR for out-of-band interferes by lowering the amount of interfering power that reaches the detector, however SIR must still always be positive. The filtering in this RX comes from the RF front end, which is shown in Fig. 15.

The entire signal path of the receiver consists of two parallel current paths operating at the battery voltage (Fig. 7). Each current path consists of two stacked gain stages in order to reuse current and to better utilize the available headroom. Large capacitors are placed between the stacked stages to create an AC ground at 9.8 GHz. While this stacked configuration does improve efficiency, it also couples the current usage of the stacked gain stages with those referenced to ground. Stacked gain stages also increase the complexity of the bias circuits, as shown in Fig. 8. Biasing is provided by two constant-G_m biases, two stacked BJT current mirrors, and two non-stacked BJT current mirrors. The constant-G_m bias circuits are designed to provide constant gain across temperature, and to reduce supply sensitivity, the circuits are cascoded. The bias currents then get mirrored onto the BJT circuits. The mirrored current ratio is tuned via a 7-bit switch which shunts across a stack of series resistors connected to the emitter of a BJT. Base current compensation is employed for better current matching, and diode-connected BJTs ensure sufficient headroom is left for the cascoded devices where necessary.

The receiver is single-ended to maximize gain and sensitivity while satisfying the stringent battery constraints. Though a single-ended topology provides worse power supply rejection,

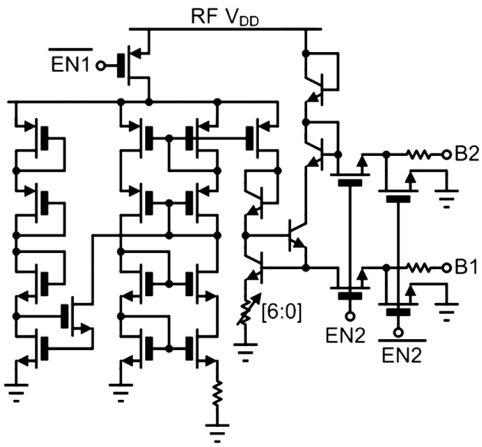

Fig. 8. Schematic of bias generation circuit for the RX.

the problem is mitigated by adding large capacitors to the RF supply voltage and to the middle of each gain stack. In addition, the bias circuits in Fig. 8 provide suitable current control to mitigate common-mode voltage concerns.

Finally, several design decisions were made to ensure fast turn-on time. First, a reset signal was added across the LPF at the input to the comparator to enable fast settling during turn-on (Fig. 7). Second, pass-gate logic was employed between the bias networks and signal path. Not only is the pass-gate logic fast, but it also cuts off the current paths to ground from the large capacitors between the stacked gain stages (Fig. 8). Once the capacitors become are allowed to charge by the baseband controller at the start of a packet, they remain charged during the duty-cycled operation of the RX.

III. Temperature-Compensated Clock Generator

To reduce both power and area, the radio includes a relaxation oscillator with a modified RC network and a single-ended hysteretic comparator for on-chip clocking. The schematic of the relaxation oscillator is shown in Fig. 9. Like conventional relaxation oscillators, this one employs an inverting hysteresis comparator with switching thresholds of V_H and V_L, which define the charging and discharging levels of the RC network. The transfer function of the RC network is

$$T_{RC}(s) = \frac{1 + sR_2C}{1 + s(R_1 + R_2)C}. \quad (1)$$

With an additional resistor R_2, the RC network adds an additional zero $(-1/R_2C)$ in the transfer function over conventional relaxation oscillators, providing an additional degree of freedom for temperature compensation. As the rail-to-rail hysteresis comparator toggles its output, a step response will be triggered at the output the RC network. The step response has two segments, an instantaneous step and an exponential decay, which is different from a single RC step response that appears in the conventional relaxation oscillator. When the step input arrives at $\mathrm{t} = 0$, the voltage across capacitor, C, cannot change instantaneously, so the voltage of the top plate and bottom plate go up together. This explains the initial step segment of the output response. Applying the initial-value theorem of the Laplace transform to the transfer function, we can further calculate the initial step amplitude as $R_2/(R_1 + R_2)$ if the input step has a normalized amplitude of unity. The amplitude of the initial step increases as temperature increases, due to different temperature coefficients of the two resistors. However, the time constant of the exponential segment also increases with temperature, offsetting the effect of the initial step and resulting in a constant time, T, to trigger the switching threshold, V_H. As a result, the overall period remains unchanged as shown in Fig. 9. Eventually, the temperature dependence of the relaxation oscillator can be decreased by selecting resistors in the RC network with different temperature coefficients so that the step response segments offset one another. The segments can be satisfied by using resistors with temperature coefficients of the same sign, but different magnitude. This characteristic is beneficial in modern CMOS technologies with limited resistor options.

The comparator consists of two stacked inverters that serve as a high gain amplifier with hysteresis levels set by R_3 and R_4 in a resistive feedback topology. Stacking the FETs reduces leakage power while the oscillator is asleep, and a 5-bit capacitor bank is added to the oscillator for one-time process calibration of frequency variation. Note that the capacitor bank will not severely load the RC network since its capacitance is small relative to C, so the temperature compensation scheme still dominates within the frequency tuning range. The oscillator is designed to have a frequency variation of 1% over the main operation temperature range. With 1% accuracy in the oscillator, the TX and RX can be heavily duty-cycled between pulses in order to (1) give the on-chip storage capacitor time to fully recharge and (2) still provide sufficient accuracy to maintain network synchronization. This accuracy specifically targets the requirements the non-coherent PPM modulation used with this radio.

IV. Current Limiter

Fig. 10 shows the system level architecture of the CL. In this diagram, the PNP bipolar transistor senses the current drawn from the battery as an increase in its base-to-emitter voltage, generated by the I-R drop over a tunable resistor. When the current drawn from the battery induces an I-R drop large enough to turn on the bipolar device, current begins to flow through the resistor, increasing the voltage at the non-inverting terminal of the feed-forward error-amplifier. In response, the amplifier increases its output voltage, increasing the resistance of the PMOS pass device and limiting the current through it. The current limit is tuned by digitally calibrating the value of the tunable resistor. The local storage capacitor, C_S, provides the charge from which a load can draw high currents in excess of the battery's sourcing capability. The tunable resistor, R_{TUNE}, can be calibrated to adjust the current limit sourced from the battery. Thus, the load may draw high current during pulses from C_S while the current limiter "trickle-charges" C_S between pulses.

The schematic of the CL is shown in Fig. 11 and includes a supply and temperature insensitive bias generation circuit used to generate the reference, adapted from [13]. To save power, this current has been mirrored to generate the reference voltage, V_{REF}. Using a supply independent current helps ensure that the reference voltage will remain constant over supply variation. This current is passed through a bipolar device and a polysilicon

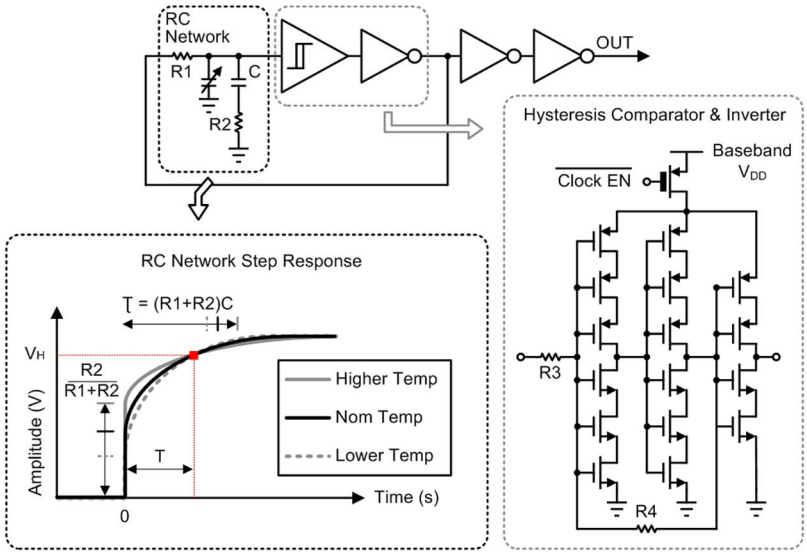

Fig. 9. Schematic of the temperature-compensated relaxation oscillator.

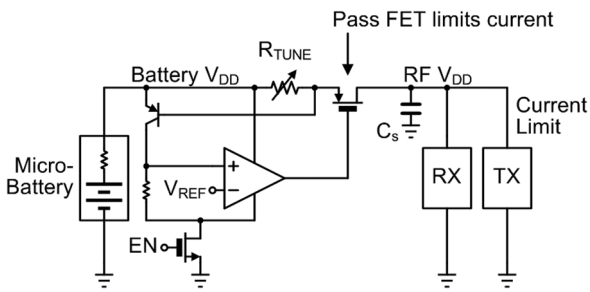

Fig. 10. Current limiter system architecture.

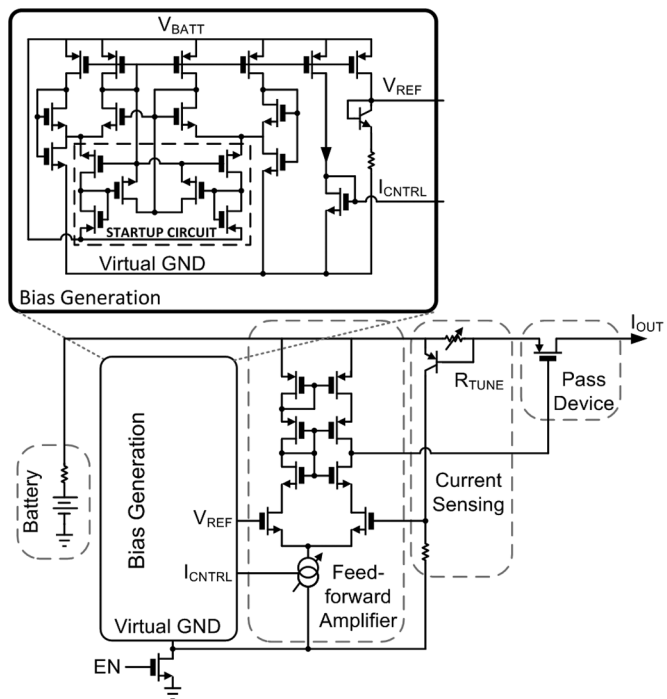

Fig. 11. Schematic of the current limiter.

resistor in order to generate the desired voltage at the output. By choosing these devices such that the temperature response is opposite that of the pass device, the current through the CL is made less sensitive to temperature variations. All devices in this design are enabled with NFET footers to better ensure a deeper cutoff, lower power, and lower leakage currents. In addition, NFET footers simplify the level conversion between the baseband controller operating at 1.2 V and the CL operating at the battery voltage.

Fig. 11 also illustrates the cascoded error amplifier. This topology was chosen because the mirrors are self-biasing and do not require cascode bias generation, thus decreasing the power consumption. The current consumed by this amplifier must be kept as small as possible to increase the efficiency of the CL. This reduces the transconductance of the input devices, lowering the overall gain of the amplifier. Headroom is not a prohibiting factor because this amplifier operates directly from the battery voltage, so stacked devices at the output are used to increase output resistance and compensate for the low transconductance due to the small bias current. The bias current can be tuned using a mirror DAC to increase the bandwidth of the amplifier in order to ensure quick response to pulsed current draw by the TX.

V. Baseband Controller

As previously mentioned, the RX and TX must be duty-cycled between incoming pulses and operate on a total average current of $< 100\ \mu$A from the battery, which requires their active windows to be synchronized with each other over the channel. The baseband processor (BBP) is in charge of synchronizing the RX and the TX, as well as modulating and demodulating the signals, tuning all the other RF/analog blocks, and communicating with the higher layers of the WSN node. Fig. 12 shows a high-level state diagram of the transmission and reception processes. The transmission and reception processes begin

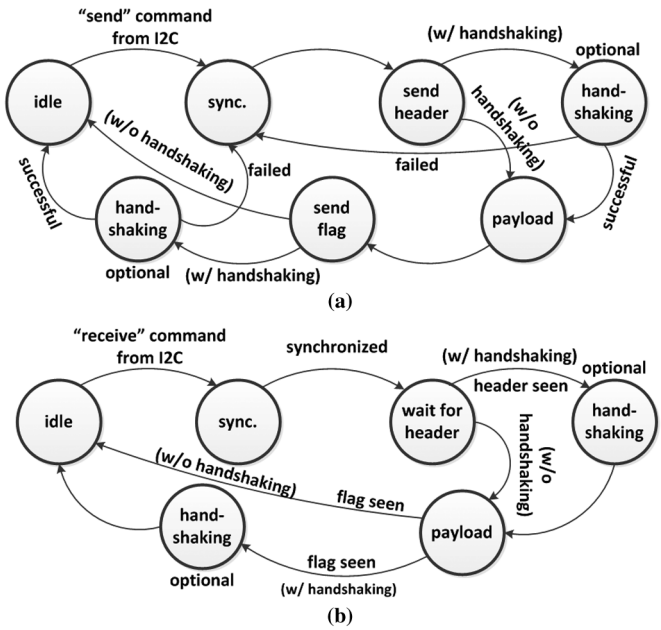

Fig. 12. High level state diagram for (a) transmission, (b) reception.

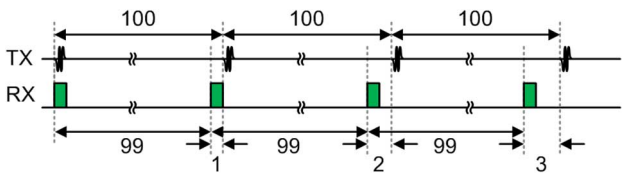

Fig. 13. Bit-level active window of the RX when its clock is 1% faster than the TX clock; the transmitted pulses are not being tracked by the RX.

with a signal from the I2C controller to wake up the BBP and start communication. In the case of transmission, a preamble is first sent, which is a sequence of pulses that the receiver will synchronize to. After the preamble, a header flag is transmitted to indicate the start of the payload, after which data transmission begins immediately, or the BBP goes through an optional handshaking with the RX before doing so. After the data payload is transmitted, another flag is sent to indicate the end of the packet, and another optional handshaking is done before returning to idle. In the case of reception, the BBP first enters an acquisition mode where an active window is moved each bit cycle until continuous pulses from the TX are seen, after which, the RX locks its active window to that of the TX (coarse tracking). The receiver goes through the same steps as the transmitter, while keeping its active window locked on that of the TX throughout the whole transmission process, assuming a maximum of 1% clock drift.

The preamble is a long sequence of 1's. The RX has a searching window that is shifted until this window overlaps the synchronization pulses. Since the data is known to be a sequence of 1 s, the RX locks its window on the position corresponding to a bit 1. After initial synchronization, the clock drift can cause the RX to lose lock. Fig. 13 shows an example of how the receiver can lose synchronization with the TX due to a 1% clock drift. Thus, the RX must track phase to keep its

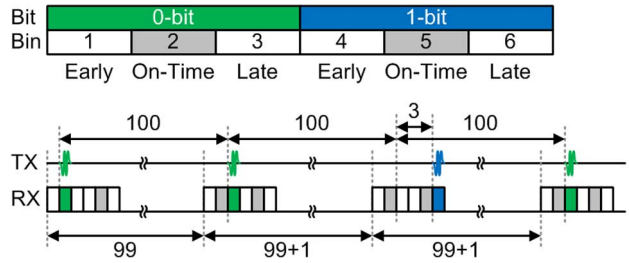

Fig. 14. Bit-level active window of the RX when its clock is 1% faster than the TX clock. The transmitted PPM pulses are being tracked by the receiver to maintain synchronization and a constant duty-cycling ratio of 6%.

window locked on the transmitted pulses throughout the entire transmission process.

The size of the active window of the RX is chosen based on the duty-cycle and the maximum difference between the TX/RX clocks. For a 1% duty-cycle and a maximum of 1% clock drift, a 6-clock-cycle window is sufficient to keep the RX locked throughout the process. This window has designated positions for the 0 and 1 data pulses. Once initially locked, the RX expects to receive a pulse corresponding to a 0 bit during the second clock cycle of the window, and a pulse corresponding to a 1 bit during the fifth cycle. These positions are highlighted (as grey) in the RX windows shown in Fig. 14. The 1% clock drift can cause the TX pulses to arrive one clock cycle earlier or later than their designated positions, in which case the RX adjusts its reception window accordingly. For instance, if a pulse arrives at the third cycle as shown in Fig. 14, the RX assumes that the data is a 0 bit and concludes that it is one clock cycle ahead of the TX. The BBP then compensates for the difference in the next bit cycle. This process can continue throughout the whole data transmission.

VI. Measurement Results

The radio was fabricated in 0.18 μm BiCMOS technology with MIM capacitors. The RX and TX front-ends operate at the battery voltage of 3.2–4.1 V. Digital processing and scan blocks operate at 1.2 V to reduce dynamic power consumption.

A. Receiver

The magnitude response of the RX, shown in Fig. 15, is tuned to 9.8 GHz to maximize the performance. The RX can also be tuned anywhere from 9.0 GHz to 10.0 GHz to ensure the center frequency of the RX can be aligned with the TX for communication. Conversion gain is impossible to measure with the available test structures, so the magnitude response has been normalized. The RX has a bandwidth of greater than 500 MHz which ensures that the entire signal power is received and amplified. At a 10^{-3} BER and 30 kb/s data rate, the RX has a measured sensitivity of -77 dBm and a peak power of -34.7 dBm. With 34 dB of RF gain (by simulation), the signal at the input of the rectifier is -0.7 dBm or 290 mVpk. In addition, the RX consumes an average of 37 μW from a 3.6 V supply with 6% duty-cycling ratio (Fig. 16). The RX is also duty-cycled during initial acquisition. According to simulations, the worst case for the RX to lock is

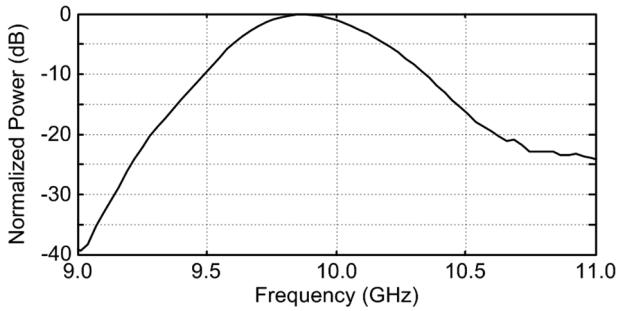

Fig. 15. Measured magnitude response of the RX.

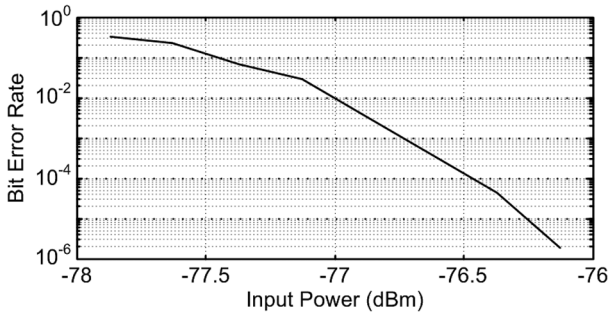

Fig. 16. BER curve vs. input power level.

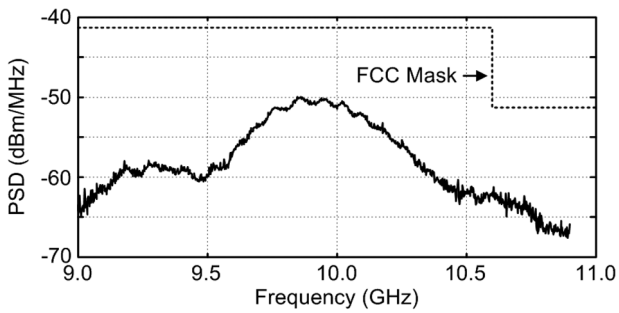

Fig. 17. PSD at TX output.

after 2500 cycles, which corresponds to 842 us. The measured leakage power of the RX is 168 pW.

B. Transmitter

The power spectral density (PSD) of the TX output loaded with a 50 Ω resistor is shown in Fig. 17. The center frequency of the pulses can be digitally tuned as shown in Fig. 18. The tuning mechanism plus UWB signaling ensure RF synchronization over PVT variations without crystals. When tuned to 9.8 GHz, the TX has a peak output power of 0.1 dBm and satisfies the FCC mask. At a 30 kb/s data rate, the average power of the TX is only 22.4 μW at 3.6 V. Fig. 19 is the transient response between pulses of the RF V_{DD} on the on-chip storage capacitor. The TX output swing is around 710 mV_{pp}, and the RF V_{DD} drops by 0.2 V during every pulse but recharges from the micro-battery before the next pulse arrives, showing that the TX can fully operate off the on-chip local decap. The measured leakage power of the TX is 170 pW.

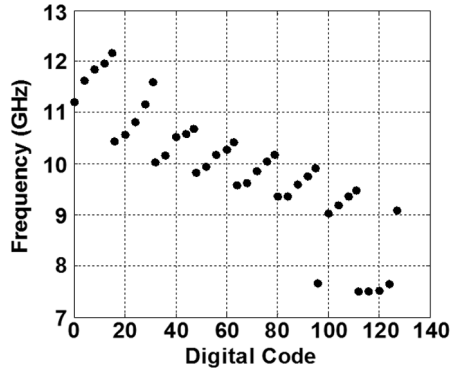

Fig. 18. Tuning range of the TX.

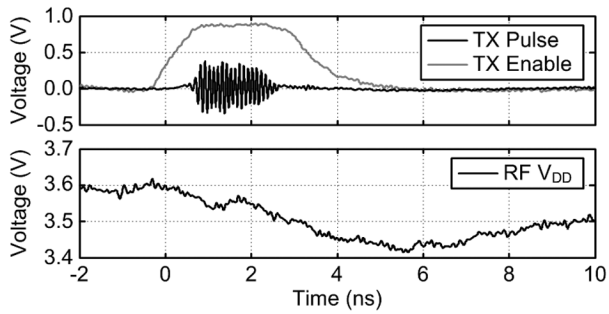

Fig. 19. Transient responses of the TX.

C. Temperature-Compensated Relaxation Oscillator

The nominal clock frequency is 3.02 MHz while consuming 12.7 μW of power from a 1.2 V supply voltage. Fig. 20 shows the frequency stability of the oscillator over the temperature range of $-20°C$ to $60°C$, showing an inaccuracy of 1% over a range of $0°C$ to $50°C$, corresponding to a temperature coefficient of -584 ppm/°C. The accuracy of the oscillator allows the TX and RX to be heavily duty-cycled between pulses in order to give the on-chip storage capacitor time to fully recharge and also sufficient accuracy to maintain network synchronization. The frequency variation is $\pm 1.5\%$ with a $\pm 4\%$ change in supply voltage. Before the relaxation oscillators are deployed for cubic-mm WSN applications, they need a one-time frequency calibration over process variation so that they are aligned. With the 5-bit capacitor bank, the frequency tuning range is from 3.00 MHz to 4.08 MHz, which is sufficient for calibration over process variation. The oscillator is compared with other compact oscillators that target low-power monolithic applications in Table I.

D. Current Limiter

Fig. 21 shows the measured tuning range of the CL. The current has been tuned from 6.0 μA to 37.5 μA with an average resolution of 32 nA. The line sensitivity is 0.21 μA/V. At room temperature, the current is limited to 10 μA for a base-emitter voltage of approximately 200 mV on the PNP device, resulting in a drop-out voltage of around 200 mV. The temperature coefficient is -34 nA/°C. The current reference produces a current of 16 nA. When tuned to 10 μA at room temperature (23°C), V_{REF} exhibits a line sensitivity of 0.64%/V with a temperature coefficient of 2.2 mV/°C. The efficiency of the current limiter

TABLE I
SUMMARY OF THE RELAXATION OSCILLATOR PERFORMANCE

	This Work	[14]	[15]
Process	0.18µm BiCMOS	65nm CMOS	65nm CMOS
Type	Relaxation Osc.	Relaxation Osc.	Wienbridge Osc.
Frequency	3MHz	0.15MHz	6MHz
Power	13µW	51µW	66µW
Area	0.03 mm^2	0.20 mm^2	0.03 mm^2
Freq. Variation	±1.0% @ 0 to 50°C	±0.5% @ -55 to 125°C	±0.4% @ 0 to 100°C
Temp. Coefficient	-584ppm/°C	-18ppm/°C	86ppm/°C
Supply Sensitivity	±1.5% @ ±4% V_{DD}	0.1% @ 23% V_{DD}	N/A

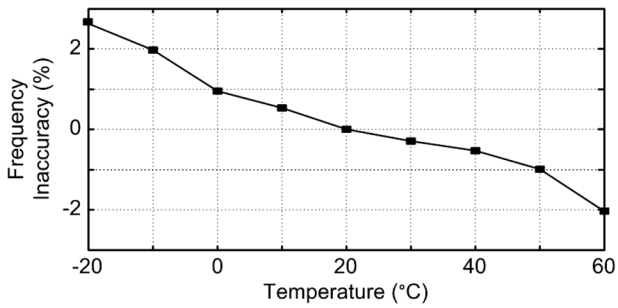

Fig. 20. Frequency inaccuracy of the relaxation oscillator over the temperature range.

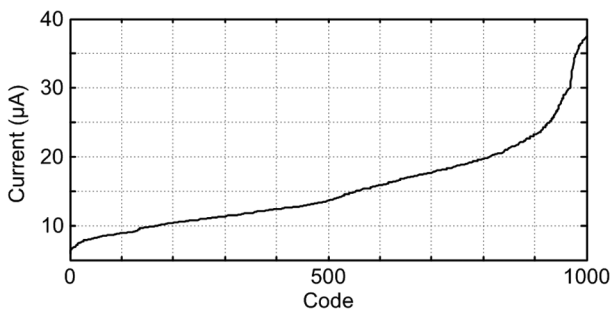

Fig. 21. Current limiter tuning range.

increases for large current limits. It is also noted that efficiency degrades at small load impedances. This is because small load impedance requires the PMOS be large to compensate, resulting in larger power consumption in the CL. The approximate efficiency of the current limiter 94% at room temperature, a 3.6 V nominal V_{DD}, and a 200 mV dropout voltage. The leakage power of the current limiter is 550 pW.

E. Radio in a Stacked System

Each block in the radio consumes $<$1 nW while asleep by carefully including thick-oxide headers/footers on all blocks, making this system ideal for heavily duty-cycled cubic-mm sensor nodes. A complete performance summary is provided in Table II. The die occupies approximately 2.73 mm^2, dominated by the modem (Fig. 22). The entire radio is designed to operate from just the 7 pads on the left edge to enable die stacking; the remaining pads are for debugging and have internal pull-down resistors so they may be left open. We have compared the proposed radio with recently published UWB radios in Table III. The proposed radio is the only one to operate at the battery voltage range and includes an entire baseband controller. In order to demonstrate that the radio can be integrated in a cubic-mm scale WSN node, a heterogeneous die-stacking system is implemented in Fig. 23. It contains the crystal-less IR-UWB radio, two Li-ion micro batteries (EnerChip CBC005), digital system control CPU, inductor-less power management unit, decoupling capacitor to supply large peak currents to the radio, and an on-board antenna. By folding the monopole on-board antenna, it can be minimized to a total electric length of $0.08\lambda_0$. The off-chip antenna occupies an area of 1.95 mm^2 on an RT/Duroid 5880 substrate. The standalone node with no external connections demonstrated node-to-base-station communication up to 2.5 m, and sustained autonomous operation on the micro battery for 17 minutes, transmitting a total of 255 packets during that time with no recharging between transmissions. Fig. 24 shows the measured power consumption profile of a basic transmission. The entire radio layer is duty-cycled between transmission packets with an enable/disable sequence controlled by the CPU on the control layer. The startup sequence is initiated when the CPU wakes up the radio's I2C module, which handles all communications between the control layer and the radio layer. The CPU first activates the clock and initiates the radio controller, holding it in reset. After the clock stabilizes, the controller is released from reset; the CPU transmits configuration and packet data and sends the instruction to initiate transmission. The radio controller then enables the CL to charge the integrated storage capacitor on the RF supply and activates the TX. Immediately following transmission, the power down sequence begins. The CL is disabled which drops the current draw to 150 pA and deactivates the transmitter via power-gating. The radio controller and clock are put to sleep, and finally, the I2C module is deactivated except for a sleep controller which monitors the I2C lines for the next wakeup.

VII. CONCLUSION

A fully-integrated IR-UWB radio in 0.18 μm BiCMOS technology has been demonstrated to operate within the limits of mm-scale micro-battery for miniaturized WSN nodes. The lifetime limitations due to battery capacity and peak current drawn are solved by current-limiting at the battery supply and duty-cycling the RF front-end at the bit-level so that the RF can operate from the integrated storage capacitor. At a 30 kb/s data rate,

TABLE II
SUMMARY OF THE RADIO PERFORMANCE

General	Process	0.18μm BiCMOS
	Modulation	PPM
	Total Area	2.73mm^2
	Data Rate	30kb/s
	RF Voltage	3.2-4.1V
	Baseband Voltage	1.2V
	Sleep Power	1.0nW @3.6V 1.8nW @1.2V

Baseband	Active Power	269μW
	Clock	13μW
	I2C & Sleep Ctrl	10μW
	Baseband Ctrl	246μW

Clock	Frequency	3MHz
	Supply Sensitivity	±1.5% @±4% V_{DD}
	Temp Sensitivity	±1.0% @0 to 50°C
	Temp Coefficient	-584ppm/°C

RX Frontend	Average Power	37μW @3.6V
	Sleep Power	347pW @3.6V
	Center Frequency	9.7-10.2GHz
	Sensitivity	-67dBm @10^{-3} BER

TX Frontend	Average Power	22.4μW @3.6V
	Sleep Power	170pW @3.6V
	Center Frequency	9-12GHz
	Output Power	0.1dBm
	Pulse Width	1.2-6.0ns

Current Limiter	Active Power	223nW @3.6V
	Sleep Power	550pW @3.6V
	Output Current	6-38μA
	Temp Sensitivity	-34nA/°C
	Line Sensitivity	0.21μA/V
	Efficiency	94% @3.6V

TABLE III
COMPARISON OF STATE-OF-THE-ART RADIOS

		This Work	[16]	[17]	[18]	[19]
General	Process	0.18μm BiCMOS	0.18μm CMOS	0.18μm CMOS	90nm CMOS	65nm CMOS
	Modulation	PPM	BPSK	PPM	OOK	PPM
	Center Frequency	9.8GHz	7.8GHz	8GHz	4GHz	5.6GHz
	RF Voltage	3.2-4.1V	1.8V	1.8V	Unknown	1.2V
	Sleep Power	1.0nW @3.6V	Unknown	Unknown	Unknown	Unknown
	Total Area	2.73mm^2	4.5mm^2	16.7mm^2	1.7mm^2	0.3mm^2
	Data Rate	30kb/s	31Mb/s	300Mb/s	150kb/s	1Mb/s
	Baseband Controller	Yes	No	No	No	Yes
RX	Average Power	306μW @3.6V	403mW	137mW	77μW	290μW
	Sensitivity (10^{-3} BER)	-77dBm	-70dBm	-76dBm	-79dBm	-53dBm
TX	Average Power	291μW @3.6V	46mW	99mW	8.8μW	25μW
	Output Power (peak)	0.1dBm	N/A	-2dBm	-0.4dBm	6dBm

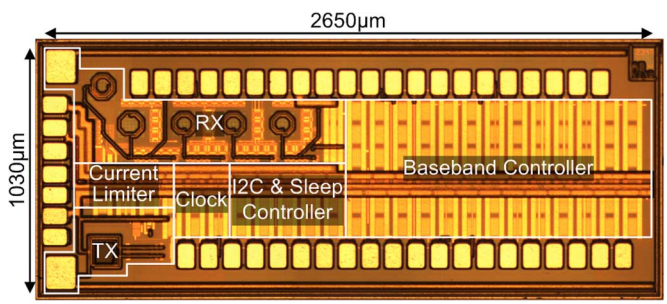

Fig. 22. Die photo of the radio.

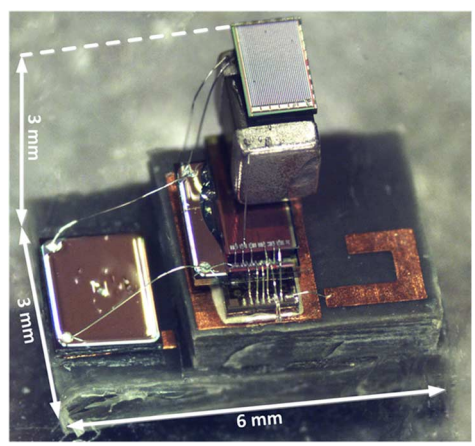

Fig. 23. Photo of the cubic-mm stacked WSN system.

the RX has a sensitivity of -77 dBm (10^{-3} BER) and consumes an average power of 37 μW. Meanwhile, the TX has a peak output power of 0.1 dBm and average power of 22.4 μW. The proposed techniques efficiently integrate the radio with a

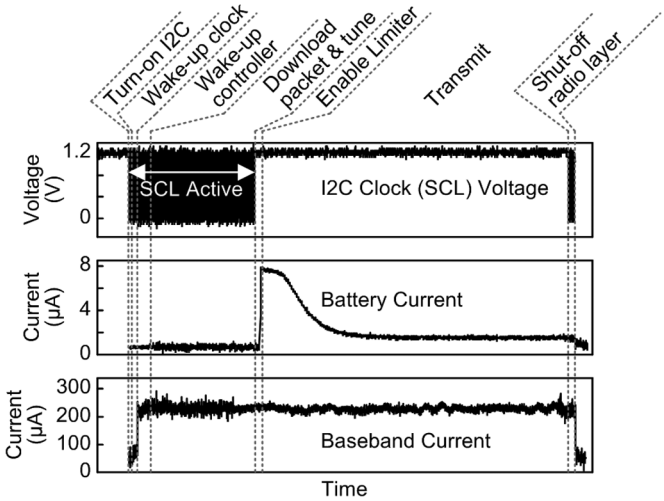

Fig. 24. Power consumption profile of the radio layer in a basic transmission cycle.

baseband modem and eliminate the need for a crystal reference. The radio is FCC compliant, and its tunability ensures communication over PVT variation. This radio is ideal for integration into a heterogeneous die stack including a micro-battery, solar cell, processor, sensors and power management unit to form a cubic-mm-scale WSN node.

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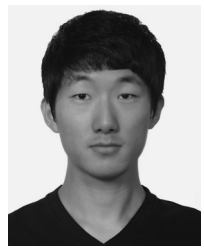

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