A 1.2-MHz 5.8-μW Temperature-Compensated Relaxation Oscillator in 130-nm CMOS

Kuo-Ken Huang and David D. Wentzloff

***Abstract*—This brief presents a low-power temperature-compensated relaxation oscillator in 130-nm CMOS for cubic millimeter wireless sensor node applications. An RC network is proposed for the oscillator, which introduces a zero in the transfer function, creating an additional degree of freedom in the step response used for frequency–temperature compensation. This approach uses conventional CMOS resistor and capacitor options and is fully integrated. The oscillator has a measured nominal frequency of 1.24 MHz with 1.0% variation from $-20\,^{\circ}$C to $60\,^{\circ}$C. It occupies an area of 0.02 mm^2 and consumes 5.8 μW of active power with a leakage power of 440 pW.**

***Index Terms*—CMOS technology, low-power electronics, oscillators, wireless sensor networks.**

I. Introduction

WIRELESS sensor networks (WSNs) today are composed of centimeter-scale devices that, at a basic level, include a battery, sensor, processor, memory, radio, and some form of timing reference—typically a crystal oscillator. The scaling trend of WSNs suggests that cubic millimeter sensor nodes are on a near-term horizon, and nodes of this form-factor have been recently demonstrated [1]. These vanishingly small devices will enable ubiquitous sensing platforms for environmental, biomedical, military, and industrial applications [1]–[5]. To achieve this, the nodes must be designed for long-term unobtrusive deployment over large temperature variations.

Power consumption, size, and frequency stability of the timing reference for wireless communication are major concerns in a cubic millimeter WSN node. At the millimeter scale, microbatteries have limited capacity (1 μAh) and peak discharge current (< 10 μA) [2]. This leads to severe challenges on the cubic millimeter WSN circuit design. While crystal-based oscillators are typically used as a timing reference due to their immunity to PVT variation, the size of off-chip crystals is an obstacle for cubic-millimeter-scale system integration, and frequency robustness of crystals comes at the expense of power [6]. As an alternative, monolithic crystal-less oscillators recently have been reported for WSN applications [6], [7]. With low power consumption and small silicon area, these fully integrated frequency references maintain temperature compensation over a wide range, without relying on a bulky off-chip crystal.

In this brief, a low-power CMOS relaxation oscillator is presented with a modified RC network and a single-ended hysteresis comparator. The RC network proposed in this brief adds one additional zero in the transfer function of a conventional relaxation oscillator. This additional degree of freedom allows for temperature compensation of the step response, with a demonstrated variation of 1%. This accuracy is specifically targeting wireless communication using noncoherent energy detection radios, which are common for WSN node systems, and this accuracy is sufficient for a receiver to track during demodulation. The oscillator design is primarily focused on reducing the power consumption and the area while providing sufficient accuracy, both of which are factors in cubic millimeter WSN nodes.

This brief is organized as follows. Section II presents the design and analysis of the proposed RC network. The oscillator design is described in Sections III and IV summarizes the measurement results.

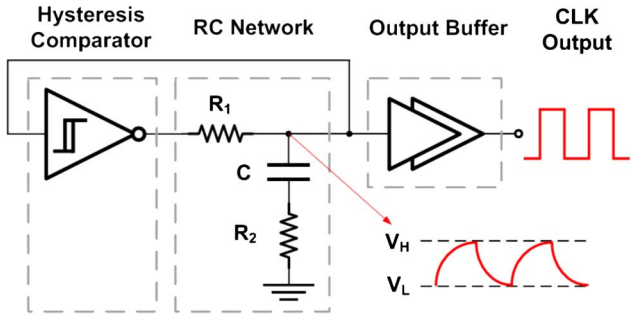

Fig. 1. Block diagram of the proposed oscillator.

II. RC Network of the Oscillator

Fig. 1 shows the block diagram of the proposed oscillator. Like conventional relaxation oscillators, this one employs an inverting hysteresis comparator with switching thresholds of V_H and V_L, which define the charging and discharging levels of the RC network. When the output of the hysteresis comparator is high, capacitor C of the RC network is being charged until the voltage becomes larger than V_H. Then the output of the comparator flips to the low state and discharges C until the

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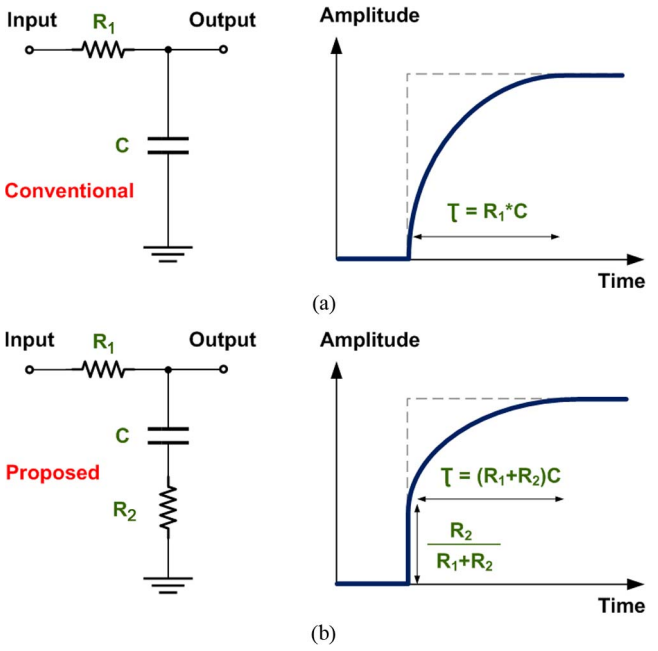

Fig. 2. Step response of the (a) conventional RC network and (b) proposed RC network.

voltage reaches V_L. Oscillation is achieved through back-and-forth charging and discharging processes, and the frequency is determined by the resistance and the capacitance of the RC network.

Fig. 2(a) shows the step response of the conventional RC network, which consists of R_1 and C only. The transfer function is

$$T_{\text{convention}}(s) = \frac{1}{1 + s(R_1 C)}. \tag{1}$$

The time constant $\tau(R_1 C)$ and, therefore, the frequency vary depending on the temperature coefficients of the resistor and the capacitor. The network proposed in this brief adds an additional resistor R_2, as shown in Fig. 2(b), and the transfer function becomes

$$T_{\text{proposed}}(s) = \frac{1 + sR_2 C}{1 + s(R_1 + R_2)C} \tag{2}$$

introducing a zero in the transfer function. By the initial-value theorem of a Laplace transform [8], the step response when $t = 0$ is

$$\lim_{t \to 0} f(t) = \lim_{s \to \infty} s \cdot T_{\text{proposed}}(s) \cdot \frac{1}{s} = \frac{R_2}{(R_1 + R_2)}. \tag{3}$$

In other words, the step response of the proposed RC network has two segments, the step at $t = 0$ followed by the exponential transient, before the voltage reaches steady state. Assuming that the magnitude of the input step is 1, the magnitude of the output step is $R_2/(R_1 + R_2)$ at $t = 0$, and the time constant of the exponential transient is $(R_1 + R_2)C$.

In CMOS technologies, resistors and capacitors typically have monotonic temperature coefficients with the same polarity. The temperature coefficient of capacitors (MIM and metal comb capacitors), however, is often small compared with resistors. With the proposed RC network, the two segments

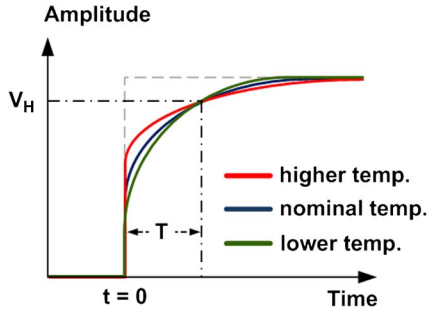

Fig. 3. Step response of the RC network at different temperatures.

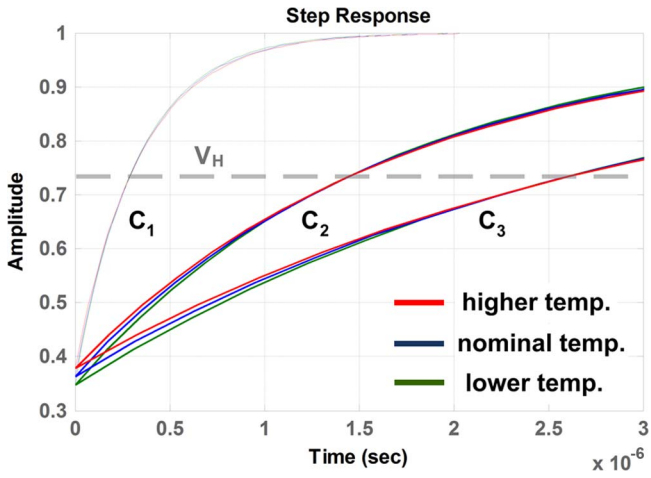

Fig. 4. Step response of the RC network with three capacitances at three temperatures.

in the step response have different temperature dependence if different resistor types are used for R_1 and R_2. As a result, the temperature dependence of the relaxation oscillator can be decreased by selecting resistors with different temperature coefficients so that the two-step response segments are offsetting. Fig. 3 shows the step response of the proposed RC network at different temperatures. As temperature increases, the initial step at $t = 0$ increases, but the time constant of the exponential decay also increases, offsetting the step increase and resulting in a constant time T to trigger the switching threshold V_H. The same trend applies as temperature decreases; the initial step decreases while the time constant also decreases, so that the overall period remains unchanged. Unlike conventional approaches that decrease the temperature dependence with a combination of resistors with positive and negative temperature coefficients [6], [9], the proposed RC network provides more degrees of freedom on resistor selections. The temperature coefficients of the resistors do not need to be opposite polarity, so that the RC network is not limited to a few resistor options with negative temperature coefficients in conventional CMOS technology, and can be optimized instead for area and process variation.

The RC network design can be further explored following the time-domain approach in (3). By the Laplace transform, the step response of the proposed RC network is [8]

$$y(t) = 1 - \left(\frac{R_1}{R_1 + R_2}\right) e^{\frac{-t}{(R_1 + R_2)C}}. \tag{4}$$

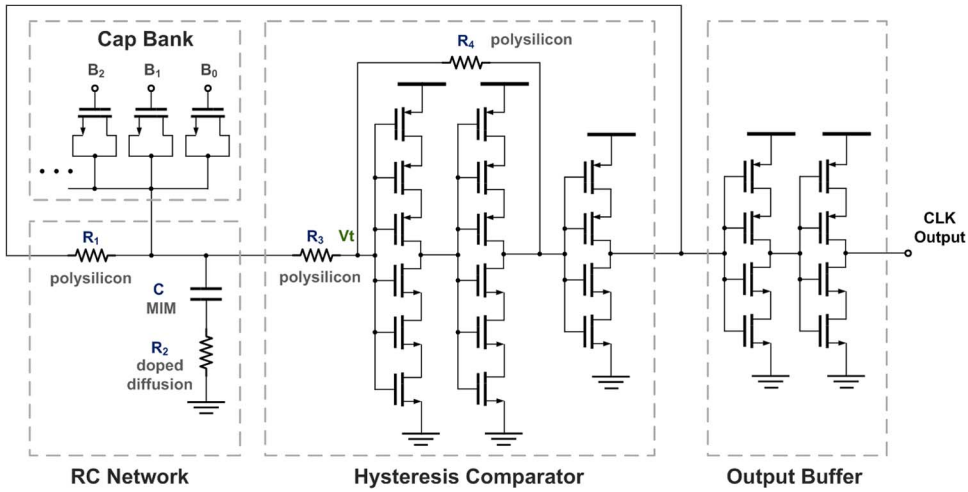

Fig. 5. Schematic of the proposed oscillator.

Considering the case in which V_H is equal to 3/4 of the unit step, then the time t when the step response is equal to the threshold voltage can be solved as

$$t = (R_1 + R_2)C * \ln\left(\frac{4R_1}{R_1 + R_2}\right). \quad (5)$$

Note that R_1 and R_2 are functions of temperature T and are equal to $R_{1\text{nom}}[1 + \text{TC}_1(T - T_{\text{nom}})]$ and $R_{2\text{nom}}[1 + \text{TC}_2(T - T_{\text{nom}})]$, respectively, where $R_{1\text{nom}}$, $R_{2\text{nom}}$, TC_1, TC_2, and T_{nom} are the R_1 value at nominal temperature, the R_2 value at nominal temperature, the temperature coefficient of R_1, the temperature coefficient of R_2, and the nominal temperature, respectively. In (5), t defines the period of oscillation and, therefore, the oscillation frequency. In order to know the temperature dependence of t, the derivative of t with respect to T is obtained as

$$\frac{\partial t}{\partial T} = C\left[\text{TC}_1 * R_{1\text{nom}} * \frac{R_2(t)}{R_1(t)} - \text{TC}_2 * R_{2\text{nom}} * \frac{R_2(t)}{R_1(t)} - (\text{TC}_1 * R_{1\text{nom}} + \text{TC}_2 * R_{2\text{nom}}) \ln\left(\frac{1}{4} + \frac{1}{4}\frac{R_2(t)}{R_1(t)}\right)\right]. \quad (6)$$

Although there is no explicit solution for (6), it is still a first-order implicit expression for choosing resistor values if the temperature coefficients are known. With the negative terms in (6), the temperature dependence is smaller than the case of a conventional RC network, which is equal to $C^* \ln(4)^* \text{TC}^* R_{\text{nom}}$ (directly proportional to TC and R_{nom}). In general, R_1 is chosen to have a smaller temperature coefficient and R_2 to have a larger temperature coefficient. As a result, by tuning the combination of R_1, R_2, C, V_H, and V_L, the period of the proposed RC network will remain fairly constant over a wide temperature range.

According to the step response analysis, we can change C for frequency tuning without losing the temperature-compensated character because C only appears in the exponential transient segment of the step response and will not change the offset over temperature. Fig. 4 shows the step responses for three C values C_1, C_2, and C_3 at different temperatures. The time constant of the exponential segment changes; thus, the oscillation frequency changes. However, the switching threshold at which temperature variation is compensated is always the same, maintaining compensation with the ability to tune frequency.

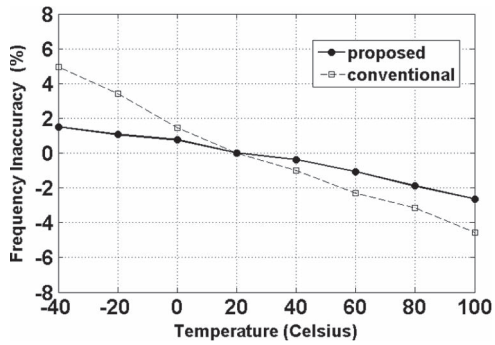

Fig. 6. Measured oscillation frequency inaccuracy over temperature.

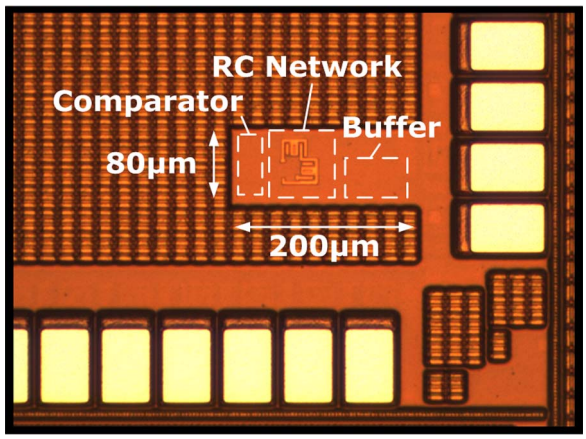

Fig. 7. Die photo of the proposed oscillator.

III. Oscillator Design

The schematic of the proposed oscillator is shown in Fig. 5. R_1 is a p^+-polysilicon 24-kΩ resistor, whereas R_2 is an n^+-doped diffusion resistor of 28-kΩ, and C is a MIM capacitor. The modeled temperature coefficients are 77, 1810, and 15 ppm/°C, respectively. A 5-bit capacitor bank is added to

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	[6]	[7]	[10]	[11]	This work
Technology	130nm CMOS	65nm CMOS	65nm CMOS	180nm CMOS	130nm CMOS
Frequency (MHz)	3.2	0.15	6	10	1.2
Power (μW)	38.0	51.0	66.0	80.0	5.8
Area (mm^2)	0.073	0.200	0.030	0.220	0.016
Freq. Variation (%) with Temp.	±0.25 @ 20 to 60°C	±0.5 @ -55 to 125°C	±0.43 @ 0 to 100°C	±0.4 @ -20 to 100°C	±1.8 @ -40 to 80°C
Temp. Coefficient	125 ppm/°C	-18 ppm/°C	86 ppm/°C	57 ppm/°C	-296 ppm/°C
Supply Sensitivity (%)	±0.4 @ 1.4 to 1.6V	1.2/V	N/A	±0.05 @ 1.2 to 3V	±1.8 @ 1.01 to 0.99V
RMS Jitter	1456 ppm	N/A	N/A	N/A	2781 ppm
Freq. Tuning Range (%)	±40	N/A	N/A	N/A	±12
Leakage Power (pW)	N/A	N/A	N/A	N/A	440
FOM (dB)	165	141	173	170	167

the oscillator for one-time process calibration of frequency. Note that the capacitor bank will not severely load the RC network since its capacitance is small relative to C; thus, the temperature-compensation scheme still dominates within the frequency tuning range. The single-ended hysteresis comparator is realized with three stacked inverters and two resistors. The stacked transistors help minimize the leakage power while the oscillator is in sleep mode, which is important for cubic millimeter WSN node applications [1], [2]. The first two stacked inverters with R_3 and R_4 serve as a high gain amplifier with resistive feedback, providing a sharp transition for the step response and the proper value of V_H and V_L. Assume that the output of the hysteresis comparator is at ground and the input of the last inverter is V_{DD}, then the voltage Vt between R_3 and R_4 can be described in terms of comparator input Vin as

$$\text{Vt} = \text{Vin} + \left(\frac{R_3}{R_3 + R_4}\right)(V_{DD} - \text{Vin}). \tag{7}$$

When Vt is equal to $V_{DD}/2$, which is the switching threshold of the stacked inverters, we can solve for the V_L

$$\text{Vin} = V_L = \left(\frac{R_4 - R_3}{2R_4}\right)V_{DD}. \tag{8}$$

Similarly, when the comparator output is V_{DD}, Vt then becomes

$$\text{Vt} = \left(\frac{R_4}{R_3 + R_4}\right)\text{Vin}. \tag{9}$$

In addition, V_H can be solved by applying Vt that is equal to $V_{\rm DD}/2$, i.e.,

$$\text{Vin} = V_H = \left(\frac{R_4 + R_3}{2R_4}\right)V_{DD}. \tag{10}$$

In this design, R_4 is twice the value of R_3, so that V_H is around $(3/4)V_{\rm DD}$ and V_L is around $(1/4)V_{\rm DD}$ no matter what the supply voltage is. This gives the oscillator immunity to V_{DD} variation. The last inverter flips the polarity for charging and discharging the RC network to create the oscillation. The single-ended oscillator topology tends to be more vulnerable to supply variation and temperature, mostly from V_L and V_H tripping at the hysteresis comparator. The simulated results show 3.5% and 0.5% on V_L and V_H tripping at 10% supply variation, with -0.9% and 0.7% variation for V_L and V_H at 60 °C and -20 °C, respectively. However, the single-ended topology significantly reduces the power consumption from differential hysteresis comparators. Finally, the output buffer drives the clock output.

IV. MEASUREMENT RESULTS

The proposed oscillator is fabricated in a standard 130-nm CMOS technology. The nominal clock frequency is 1.24 MHz while consuming only 5.8 μW of power from a 1-V supply voltage. The frequency variation is 1.8% with a 1% change in supply voltage. The RMS jitter is 2781 ppm at 20 °C, and the leakage power is 440 pW when the oscillator is in sleep mode. Fig. 6 compares the frequency stability of the proposed oscillator with an oscillator using the conventional RC network over the temperature range of -40 °C to 100 °C, showing roughly twice inaccuracy improvements. Over a range of -20 °C to 60 °C, the oscillator has only 1% variation in frequency, corresponding to a temperature coefficient of -296 ppm/°C. Before the relaxation oscillators are deployed for cubic millimeter WSN applications, they need a one-time frequency calibration over process variation so that they are aligned. With the 5-bit capacitor bank, the frequency tuning range is $\pm 12\%$ or 1.06–1.32 MHz, which is enough for the calibration over process variation. Note that the temperature compensation still applies over the frequency tuning range. The die photo is shown in Fig. 7. The relaxation oscillator occupies an area of 80 μm $\times$ 200 μm without pads. The measured performance of the proposed relaxation oscillator is summarized and compared with other state-of-the-art oscillators in Table I. In order to fairly compare with the oscillators, we defined a figure-of-merit (FOM) as

$$\text{FOM} = 10\log\left(\frac{f^2}{\text{power} * \text{area} * |TC|}\right). \tag{11}$$

V. CONCLUSION

A low-power temperature-compensated relaxation oscillator for cubic millimeter WSN applications is designed and fabricated in a standard 130-nm CMOS process. An RC network of

the oscillator is proposed with a transmission zero for temperature compensation. It introduces an additional degree of freedom for relaxation oscillator design and maintains temperature compensation over a frequency tuning range using conventional CMOS resistor and capacitor options. The oscillator offers a good balance between power, area, oscillation frequency, frequency stability, and leakage power, which are all critical specifications for cubic millimeter WSN applications.

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