A 335µW -72dBm Receiver for FSK Back-Channel Embedded in 5.8GHz Wi-Fi OFDM Packets

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***Abstract*— An ULP back-channel receiver is presented that demodulates binary a FSK back-channel signal embedded in 5.8GHz IEEE 802.11a Wi-Fi OFDM packets. The architecture of the back-channel receiver employs a two-step down-conversion where the first mixing stage downconverts using the 3rd harmonic of the LO for power efficiency. The LP-65nm CMOS receiver consumes 335µW with a sensitivity of -72dBm at a BER of 10^{-3} and data-rate of 31.25kb/s. The radio uses a balun and a 250kHz reference crystal as external components. The receiver uses a 1V supply voltage for analog blocks, and 0.85V for digital blocks including the LO and FLL.**

***Index Terms*— Wi-Fi OFDM, back-channel, 3rd harmonic mixing**

I. Introduction

Wi-Fi is the most ubiquitous wireless networking protocol, but the excessive power consumption of Wi-Fi radios has limited their adoption into the rapidly growing class of ultra-low power (ULP) IoT devices. This is because the Wi-Fi requirements are not suitable for ULP implementations, and to date no <10mW Wi-Fi receiver has been reported [1]. Ideally an ULP IoT device would have an active network connection, however with Wi-Fi this results in continuously turning on the radio to keep the device associated with a router, limiting power savings from duty-cycling. ULP wake up radios [2] could be used to address this problem, but these require custom signals not supported by Wi-Fi networks, limiting their widespread adoption. To close this gap, we developed a messaging technique we refer to as back-channel that uses a Wi-Fi standard-compliant transmitter to produce a signal that can be detected by an ULP FSK receiver [3].

This paper presents a complete 335µW ULP receiver able to demodulate FSK back-channel messages that are embedded in standard-compliant Wi-Fi packets (Fig. 2). On the Wi-Fi router, generating back-channel messages only requires control of the payload data in a single packet, therefore it is supported by any 802.11a or later router and suitable for widespread adoption. By modulating the payload of a Wi-Fi packet, we produce a wideband, binary FSK-modulated back-channel message via the OFDM symbols. The ULP receiver then detects the FSK modulated back-channel message [3]. This wideband FSK message relaxes several specifications of the ULP receiver such as phase distortion, order of the filter, and inter-modulation, which helps to reduce receiver power.

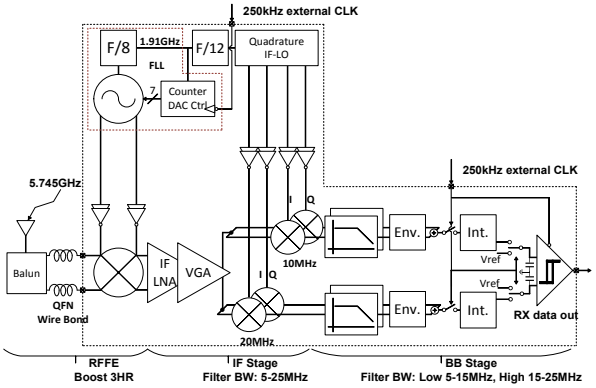

Fig. 1. Mixer first Two-step down-conversion architecture.

More detail about Wi-Fi back-channel FSK modulation will be discussed in Section II. The receiver down-converts the RF signal with the 3rd harmonic term of commutating mixer. This reduces power consumption of the LO, enabling a wide band 5.8GHz receiver at sub-mW. More detail about the architecture, and the design will be discussed in Section III. Measured results will be discussed in Section IV.

II. Wi-Fi Back-Channel (De)Modulation

Since 802.11a in 1999, Wi-Fi standards have used OFDM because it has numerous advantages for high throughput devices. The power consumption of wideband OFDM mod/demod, however, is not suitable for ULP radios because it requires a linear RF front-end, high-speed ADC/DAC, and significant baseband processing. OFDM transmitters are basically capable of generating a wide range of RF signals, by taking a time-domain signals' FFT and mapping that to each of the OFDM sub-carriers. By feeding carefully crafted bit sequences into the payload of a Wi-Fi packet, the Wi-Fi OFDM transmitter is made to produce a wideband back-channel FSK signal embedded in a 5.8GHz IEEE 802.11a compliant OFDM packet. The FSK modulated back-channel occupies the same 20MHz bandwidth, and each binary back-channel message bit is conveyed by one OFDM symbol (4µs long). This is achieved by mapping only low-power constellation points

the lower half of the channel, and high-power point to the upper half to encode a '0' (and vice versa for a '1') (Fig. 2).

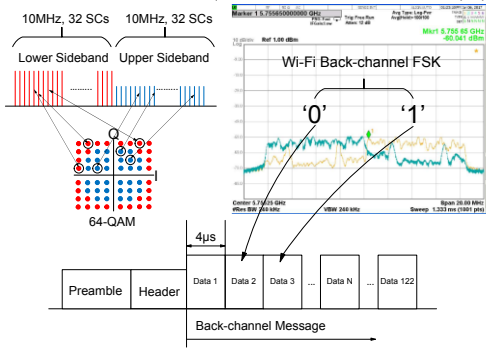

Fig. 2. Wi-Fi back-channel FSK signal and the packet structure.

Thus, the back-channel bit is demodulated by comparing the energy in the upper and lower halves of the Wi-Fi channel. The max back-channel bit rate is identical to the Wi-Fi OFDM symbol rate, which is 250kHz (i.e., 4μs per back-channel bit). One can consider this as a spread spectrum scheme where 250kb/s binary FSK is spread over a 20MHz bandwidth. This simple non-coherent demodulation mechanism combined with a relatively low symbol rate allows an ULP implementation of a Wi-Fi back-channel receiver, as a companion wakeup radio to a fully compliant Wi-Fi radio. The wide bandwidth of the FSK back-channel symbols also makes the receiver relatively insensitive to phase noise and frequency offset in the LO, further reducing power.

III. Low Power RF Receiver Circuit Design

Our goal was to design a receiver with minimized power consumption, while receiving a back-channel signal from an 802.11a Wi-Fi router at a range of ~30m. Fig. 1 shows the receiver is a passive mixer-first architecture and a 2-step down-conversion which help to reduce power, at the expense of increased noise factor. Also, the receiver down-converts the RF signal with an LO at 1/3 the RF frequency for power efficiency. The main power saving features of the design are 1) back-channel messages modulate information onto wideband FSK symbols transmitted by a standard Wi-Fi radio, which are detectable by ULP receivers; 2) the RF mixer down-converts 5.8GHz as the 3rd harmonic term from a commutating mixer switching at 1.9GHz. Because all LO paths switch at 1.9GHz, this significantly reduces power of the oscillator, LO buffers, and divider in the FLL, which are often the highest power blocks in an ULP radio; 3) low-noise amplification, filtering, and variable gain amplification is performed at the first intermediate frequency (IF1); and 4) the IF1 signal is further down-converted by 2nd quadrature mixers (IF2 Mixer), whose LO is driven from the FLL, which separates the upper and lower halves of the back-channel FSK into two wideband energy-detection paths. The baseband circuits filter each half of the Wi-Fi channel, envelop detect and integrate them to measure and compare the energy in the low and high halves to make a bit decision.

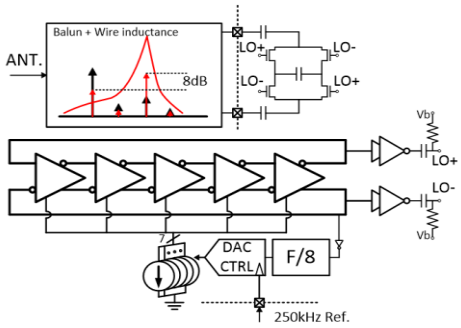

Fig. 3. Front-end circuit implementation.

A. RF Front-end

As shown in Fig. 3, the RF front end is comprised of an off-chip balun, and an on-chip double-balanced passive mixer. The input impedance is capacitive, thus the series inductor provides some voltage boost, so long as the Q value of the off-chip inductance is larger than 25. The resonant LC tank on the RF front-end is not only providing voltage gain, but also filters out other harmonic components. The boosted RF signal is fed into the dual balanced RF mixer whose gate potential is biased to maximize the conversion gain of the passive mixer. According to measurements, mixing with the 3rd harmonic term of the LO provides 10dB less conversion gain compared to the fundamental mixing term.

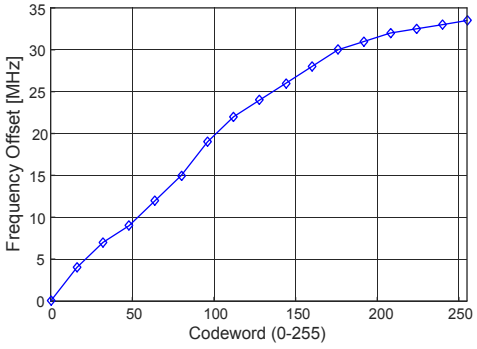

Fig. 4. Frequency change of the fundamental LO at different codewords.

The FLL is composed of a current controlled 5-stage differential ring oscillator with a counter based digital controller. The digital controller counts the divided frequency over reference clock cycle periods, and compares this to the target. The loop filter then has two modes: 1) If the counter value is less than a threshold, it increments or decrements the binary control word of the current DAC by 1, approaching the final frequency with a slew rate; 2) If the counter value is above the threshold, meaning the DCO frequency is far from the target, the FLL enters a higher-

gain mode and slews at a faster rate towards the target. Fig. 4 shows the LO frequency range, which is applied directly to the mixer which then mixes down the 3rd harmonic term. The effective LO tuning resolution in the 5.8GHz band is 0.5MHz, sufficient for tuning to the center of a 20MHz Wi-Fi channel for demodulating back-channel FSK. The threshold of the digital controller, and the number of cycles is programmable. The 2nd LOs that drive the IF2 mixers are composed of I & Q square waves at 20MHz, and 10MHz for the high and low bands. Those are generated from the same FLL driving the RF mixer.

B. Intermediate Frequency Stage

The first IF stage, IF1, is comprised of a low-noise amplifier (IF-LNA) and VGA which together provide all of the gain in the IF1 signal path (Fig. 5). An inverter-based self-biased common source amplifier is chosen for the IF-LNA due to its high input impedance, and good gain-efficiency. The IF-LNA and VGA are self-biased through a replica circuit. These stages also perform the band-pass filtering of the down-converted IF1 signal from 5MHz to 25MHz.

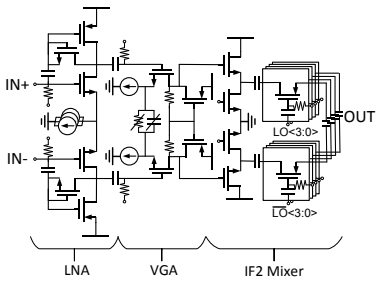

Fig. 5. Intermediate frequency circuit diagram.

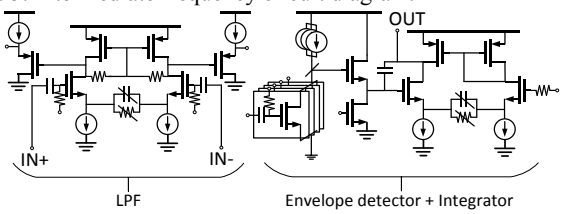

Fig. 6. Baseband circuit diagram. Left diagram is a low-pass filter, and the right diagram is envelope detection, and integration circuit diagram.

C. Baseband Frequency Stage

The baseband stage collects the energy of each sideband of the OFDM symbol and compares these to demodulate the FSK back-channel signal. Signal energy is measured from the baseband stage by using quadrature down-conversion, squaring, and integration. This approach is chosen, rather than measuring the power at IF1, because of the mismatch, and increased power consumption of implementing two separate band-pass filters for each sideband. The 5MHz-25MHz filtered IF signal is down-converted by quadrature mixers which are driven by two LOs. Each LO is centered on each sideband. LPFs filters out the undesired band so that it captures only the in-band spectrum. The topology of the LPFs is as same as the VGA, which use conventional source degenerated differential amplifiers, with the voltage gain controlled by source degenerated FETs for robust gain control and tuning range. The squaring block is an envelope detector, which drives the gate on the border of the linear and saturation regions. The 7-bit PMOS current DAC is used to calibrate any DC offset between the high and low squaring blocks in order to remove any bias in the final bit decision.

IV. Measurement Results

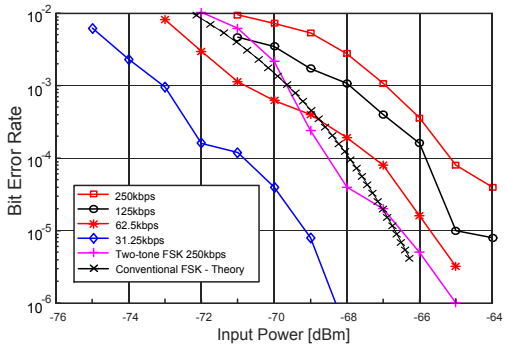

Fig. 7. Bit Error Rate waterfall curve.

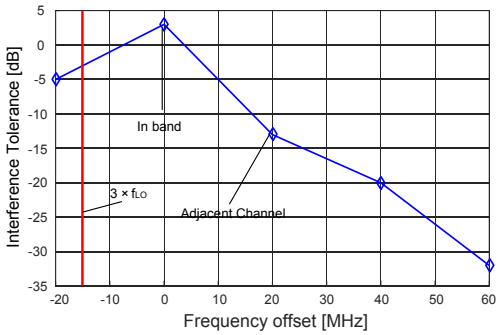

Fig. 8. Signal to interference ratio.

The receiver was fabricated in a CMOS LP-65nm technology. The active area is 0.228mm². Fig. 7 shows the BER performance versus input power at different back-channel data rates. The data-rate of the Wi-Fi back-channel FSK can be adjusted by combining multiple OFDM symbols into one super symbol. For example, the sequence '1 0 0 1' with a data-rate of 125kb/s is generated by sending the Wi-Fi back-channel signal '11 00 00 11'. The measured sensitivity at BER $=10^{-3}$ is -67dBm when the data-rate is

250kb/s, and -72dBm when the data-rate is 31.25kb/s. Conventional two-tone FSK was also tested, which results in 1.5dB better performance than wideband FSK, because of the non-uniform gain response across each sideband. The center of the sidebands provides the highest gain, hence, the total gain provided for multiple-carrier wideband signals is effectively less than with single tones. Fig. 8 shows the signal to interference rejection ratio of the receiver. As can

be seen, the SIR is 13dB for the adjacent higher channel, and 5dB for the adjacent lower channel because of imperfect image rejection. Fig. 3 shows the measured gain difference between RF signals after the LC resonant matching network at each of the harmonic frequencies of the LO. The LC resonant matching network on the RF front-end improves the voltage gain by 4dB. The matching network attenuates the fundamental component, which eventually results in a gain difference between the fundamental (un-desired) and 3rd harmonic (desired) component by 8dB. The overall gain of the receiver is 60dB at the output of the envelope detectors.

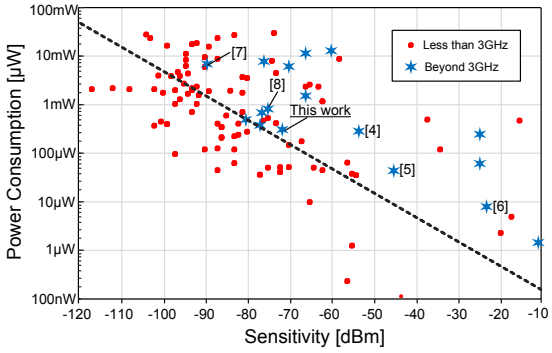

Fig. 9. Radio survey from 2005 to present. Data is collected from ISSCC, JSSC, VSLI, RFIC, CICC.

A comparison between state-of-art narrow band ULP radios operating in the 5.8GHz band is shown in Table I. Fig. 8 shows sensitivity vs. power for state-of-art low power radios [9]. This back-channel receiver is close to the Pareto-optimal line for all ULP radios operating above 3GHz, and the only one that is complaint with any IEEE standard.

V. Conclusion

An ULP FSK back-channel receiver in LP-65nm CMOS was presented. By utilizing binary FSK back-channel embedded in IEEE 802.11a packets, this receiver achieves ULP operation and compatibility with Wi-Fi standards. Down-conversion with the 3rd harmonic term of the LO reduces the power consumption in the LO block significantly, at the expense of noise performance. The receiver consumes 335μW active power with a sensitivity of -72dBm at BER of 10^{-3}.

Acknowledgment

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TABLE I
COMPARISON WITH STATE-OF-ART ULP NARROW BAND RADIOS

	JSSC[4]	ISSCC[5]	ISSCC[6]	VLSI[7]	RFIC[8]	This work
Process Node	CMOS 65nm	CMOS 130nm	CMOS 65nm	CMOS 130nm	CMOS 65nm	CMOS 65nm
Supply Voltage	1.2V	3-3.6V	0.6V	1.5V	0.5V	1V, 0.85V
Frequency	5.6GHz	5.8GHz	5.8GHz	5GHz	5.85GHz	5.8GHz
Modulation	PPM	OOK	OOK	OOK	OOK	FSK
Data-rate	1Mb/s	14kb/s	100kb/s	1.2Mb/s	300kb/s	250kb/s | 31.25kb/s
Active power	290μW	15 μW	8.2 μW	6.6mW	830 μW	335 μW
Sensitivity*	-53.5dBm	-45dBm	-23dBm	-90dBm	-75dBm	-67dBm | -72dBm
SIR**	-12dB	NA	NA	-30dB	NA	-13dB

* BER @ 10^{-3}
** Adjacent Channel