8.1 nJ/b 2.4 GHz Short-Range Communication Receiver in 65 nm CMOS

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***Abstract*—An 8.1 nJ/bit 2.4 GHz receiver with integrated digital baseband supporting O-QPSK DSSS modulation compliant with the IEEE 802.15.4 standard is presented that targets short-range, Internet of Things applications (IoTs). The sensitivity of a wireless communication receiver in general trades with power consumption. This receiver exploits this tradeoff to achieve a total power consumption of 2.02 mW including ADCs and digital baseband processing, at a sensitivity of −52.5 dBm at 250 Kbps. The energy-efficiency of the radio frequency (RF) front-end alone is nearly 2x better than the prior art. The receiver was fabricated in 65 nm CMOS with an area of 0.86 mm^2.**

***Index Terms*—Coherent receiver, digital baseband, IEEE 802. 15.4, low-energy receiver, near-threshold digital baseband, RF-to-bits receiver, short-range low-power radio, zero-IF, zigbee radio receiver, 2.4 GHz ISM band.**

I. Introduction

An exponential growth in miniaturized smart sensors is imminent in the near future. The rapid growth in technology is bringing the vision of Internet of Things (IoTs) closer to reality at a much faster pace than previously anticipated. Cisco has projected a $19 trillion market for the IoTs in the next decade [1]. This value does not come by connecting every object to the internet but by their intelligent interaction and collaboration. This will open new dimensions of collecting data and extracting information at a scale not possible before. This technology will enable smart cities with improved waste/water management, transportation and lighting, connected cars with smart homes and will revolutionize retail, manufacturing, shopping, and healthcare [2].

The sensor density around a person is expected to increase from a few hundreds to thousands, which will correspond to roughly a trillion networked sensors on the planet [3]. The microsystems encompassing these sensors will have to have high-energy efficiency for computation, communication, and sensing operations. This is mainly because many of these microsystems are expected to operate at the edge of the cloud with a battery lifetime of 10+ years, or batteryless operation from harvested energy. This poses new design challenges and opportunities for circuit designers and especially for wireless communication integrated circuits (ICs) as they consume a significant amount of power when active in a miniaturized microsystem [4], [5].

Some efforts are put in place to define an open platform that enables the Internet of Things. One such initiative led by some of the leading players in the market is the Thread Group [6], a standard initiative for using 6LoWPAN-based network technology with mesh capabilities optimized for home automation. It blends IPv6 with low-power IEEE 802.15.4 radios, which is essentially the same PHY layer on which Zigbee standard is defined. Recently, IEEE 802.15.4 compliant radio frequency (RF) front-ends have been reported with exceptional sensitivity (wireless range $>$100 m) and energy efficiency of 7.2 nJ/bit [7], 6.8 nJ/bit [8] and 7.4 nJ/bit [9]. However, there are many IoT applications that only require short-range communication ($<$10 m), such as wireless proximity sensors for smart meters and parking spaces, home automation within a room, and some wearables for fitness and health monitoring. In these cases, different design tradeoffs can be made in order to improve energy efficiency, as compared to devices that prioritize high performance or ICs designed for worst-case applications. In particular, it is well known that the sensitivity of a receiver directly trades off with its power consumption. Dialing sensitivity back to around −50 dBm could lower the power of the radio significantly and meet the needs of many energy-constrained applications. However, doing so is not trivial, and requires redesigning with focus on ultra-low power from RF front-end through the digital baseband processor.

This paper presents a fully integrated 2.4 GHz receiver comprising an RF front-end, analog-to-digital converter (ADCs), and digital baseband processor (DBB) that exploit the relationship of sensitivity and power consumption. Although not meeting the sensitivity required by the IEEE 802.15.4 standard, this receiver provides a short-range O-QPSK DSSS link that is fully compatible with IEEE 802.15.4 packets.

Several power saving techniques and analog design tradeoffs such as linearity, gain, and NF for short-range communication have been incorporated in this receiver. This includes digital supply scaling for the digital baseband processor, adaptive digital signal processing, single-ended vs. differential RF and analog paths, clock-gating, and capacitive decoupling of the flash ADC's reference ladder. This receiver achieves 3.5 nJ/bit RF front-end energy-efficiency, combined with a digital baseband operating at a scaled supply voltage to demodulate IEEE 802.15.4 packets. The total power of the receiver is 2.02 mW, including ADCs and digital baseband processing while excluding frequency synthesizer (PLL). The receiver achieves a sensitivity of −52.5 dBm at a raw BER (bit error rate) of 10^{-3}, which is 32.5 dB higher than the IEEE 802.15.4 standard requirement for compliance, but still offers a line of sight (LoS) communication

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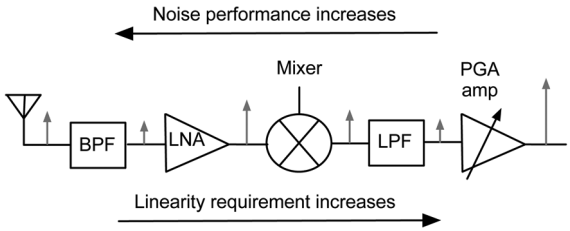

Fig. 1. Signal propagation through a generic radio front-end.

range of 9 m assuming a 7 dBm EIRP transmitter. This range is suitable for communication in the vicinity of a handheld device, sufficient for many IoTs applications that place highest priority on power consumption.

The paper is organized as follows. Section II discusses the system design considerations; emphasize the core ideas and the tradeoffs that have been incorporated in the design. Section III describes the overall system block diagram and the link budget of the prototype receiver. Section IV describes the circuits in detail. Section V presents the measurement results and Section VI concludes the paper.

II. System Design Considerations

To understand system design tradeoffs consider a generic radio front-end as shown in Fig. 1 where a sine wave is represented as an impulse in the frequency domain that progresses through the receiver chain. A parameter of interest of a receiver is its dynamic range which is determined by the maximum signal handling capability and the minimum detectable signal for a given performance specification. To maximize the dynamic range of a radio receiver for a given power budget, the power is traded to optimize different circuit parameters along the signal chain. The minimum detectable signal specification of a receiver depends on its noise performance while the maximum in-band signal handling capability is related to the overall linearity of the receiver. The noise performance of the front-end blocks is more critical compared to the later stages in a signal chain. Intuitively this can be understand, as the signal goes through amplification, the noise added by the later stages has less relative impact to degrade the overall signal to noise ratio as compared to the front-end blocks. Similarly as the signal goes through amplification in a signal chain the linearity requirements of the later stages become more critical (since handling larger amplitude signals) as compared to the front-end blocks. Now we will analyze the noise, linearity and power tradeoffs more quantitatively.

A. Noise and Power Tradeoff

High performance and high sensitivity receivers (sensitivity < -90 dBm) require a low receiver Noise Figure (NF). This is achieved by employing a Low Noise Amplifier (LNA) at the front of the signal-processing path, followed by additional RF gain stages and an active mixer. The LNA noise figure typically dominates the receiver overall NF and trades directly with power. The noise factor (F) of an LNA is related to its power approximately by [10][11][12],

$$F \approx 1 + \frac{\alpha}{P_{LNA}} \tag{1}$$

Where P_{LNA} is the power consumed by a low-noise amplifier and α is the proportionality constant that depends on the given technology and the circuit topology.

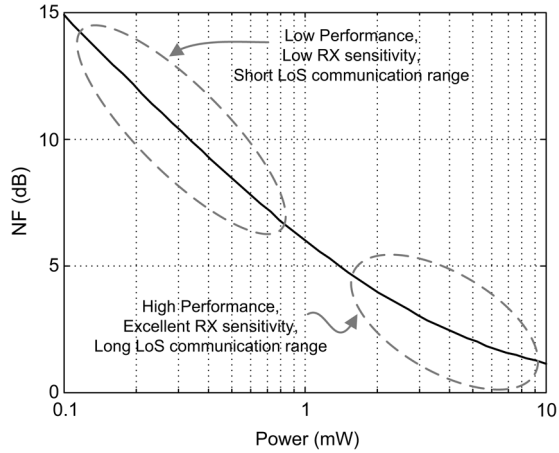

Fig. 2. Theoretical noise figure vs. power tradeoff in an LNA.

Fig. 2 plots the NF ($10\log_{10}\mathrm{F}$) from (1) for an LNA designed in 90 nm CMOS, which consumes 3 mW power and achieves a NF of 3 dB [13]. A similar relationship between noise and power is expected for an LNA implemented in 65 nm CMOS and in fact for any signal-processing element trying to optimize noise and power [14]. As expected for low NF $<$5 dB, the rate of change of NF with respect to power is decreasing (decreasing gradient) suggesting lower returns in NF for increasing power. Whereas for systems that can tolerate a high NF the power can be reduced significantly, as the rate of change of NF with respect to power is high (large slope). Since NF directly dictates receiver sensitivity, this region corresponds to a low-sensitivity and short-range wireless communication. This is the first design tradeoff that has been explored for the prototype chip.

B. Linearity and Power Tradeoff

The overall linearity of the RF front-end is dictated by the baseband gain stages. To better understand the linearity vs. power tradeoff, a three-point method is adopted to estimate the linearity of a short-channel NFET in 65 nm CMOS [15]. For a zero-IF receiver architecture second-order linearity is more important and the same method is used to estimate $IIP2$.

$$IIP3 = \frac{4V^2}{Rs}\left[\frac{g(0)}{g(V)+g(-V)-2g(0)}\right] \tag{2}$$

$$IIP2 = \frac{32V^2}{Rs}\left[\frac{g(0)}{g(V)-g(-V)}\right]^2 \tag{3}$$

Where $IIP2, IIP3$ are the second and third order input intercept points respectively, g is the incremental device gain evaluated at three input voltages 0, V and $-V$, and Rs is the source resistance. The incremental gain of a short-channel MOSFET is given by [15],

$$g = \left[\frac{1+\rho/2}{(1+\rho)^2}\right]\left[\mu_n C_{ox}\frac{W}{L}V_{od}\right] \tag{4}$$

$$\rho = \frac{V_{od}}{LE_{sat}} \tag{5}$$

Where V_{od} is the over-drive voltage and ρ takes velocity saturation into account. The V_{od} depends only on the current density therefore both $IIP3$ and $IIP2$ are plotted vs. current density, to estimate power in 65 nm CMOS Fig. 3. As shown in the plot the linearity improves as the power increases logarithmically. Therefore the baseband gain stages in the proposed receiver are

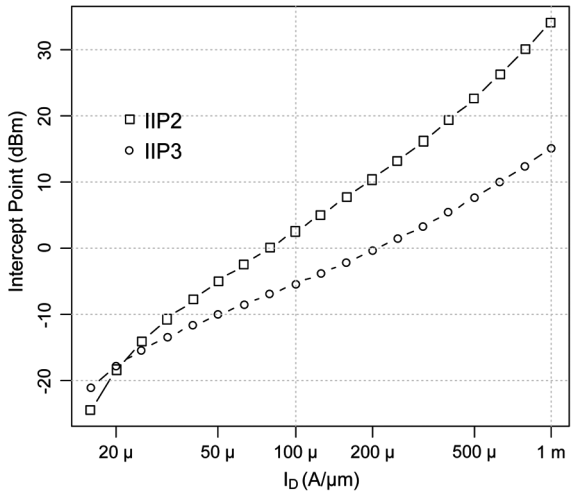

Fig. 3. Theoretical short-channel NFET linearity vs. power tradeoff in 65 nm CMOS.

biased with a current density $< 50\ \mu A/\mu m$ to keep the total power consumption low while achieving decent linearity.

C. Adaptive Sampling

Apart from the sensitivity vs. power tradeoff, another proposed idea is to adapt the average sampling rate of the digital baseband processor based on the link quality of the wireless communication channel. Though independently developed, a similar but a different study [16] suggested using a variable data rate based on the communication link quality to reduce the network latency and average power consumption in a wireless sensor network. An experimental study of 44 IEEE 802.15.4 nodes, in an industrial mesh network, showed that a large number of links exist with significantly high SNR [16]. This excess SNR is exploited to reduce the average sampling rate in the digital baseband processor to save power. This is conceptually illustrated in Fig. 4 that also shows the IEEE 802.15.4 standard compliant packet [17]. For the said standard, the chips are half-sine shaped pulses. The channel pulse template is learned by averaging the received known pulses in the synchronization header. As shown in the illustrative cartoon, if the SNR is low the receiver is run at 2x the Nyquist rate while if the SNR is high the receiver is run at 1x the Nyquist sampling rate. Independent of the sampling rate the receiver maintains a fixed system link performance quantified by a target bit-error-rate (BER). In other words, the sensitivity of the receiver is adapted to the time-varying characteristic of the communication channel on a per-packet basis. It is to be noted that when the averaged channel pulse template is learned, the samples are ranked with respect to energy and this information is later used for adapting the average sampling rate. For example, for a 50% sampling rate which for the prototype chip corresponds to 2 out of 4 time-samples, the highest 2 energy samples are chosen as shown in Fig. 4 while the lowest two energy samples are not taken into account for further digital processing. This design tradeoff is in direct contrast to what high-performance radios typically employ. In the case of an IEEE 802.11 (WiFi) standard compliant radio, a provision is made in the standard to adapt to higher modulation schemes when a good communication channel exists, preferring high data throughput and thus high-performance over low power consumption [18].

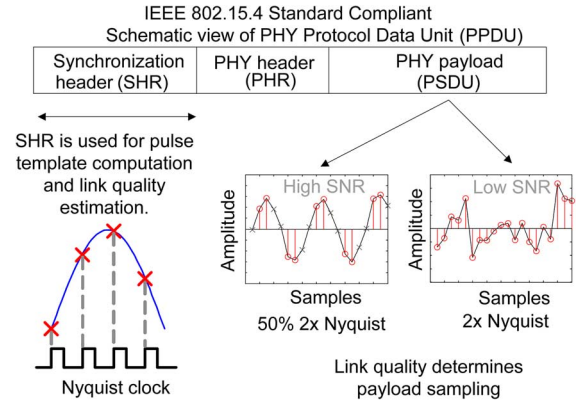

Fig. 4. Adaptive RX sampling concept.

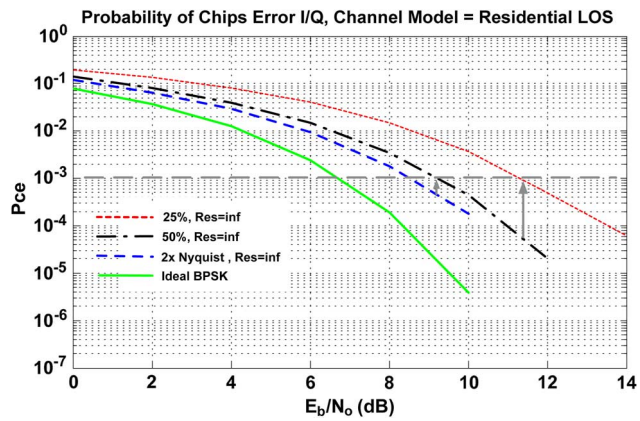

Fig. 5. Simulated probability of chip error rate.

To evaluate the link performance using adaptive sampling, a MATLAB simulation model was developed. Fig. 5 shows the waterfall curves for 25%, 50%, 75%, and 100% sampling rate. For a target link performance of 10^{-3} BER, the receiver is run at 2x the Nyquist rate for acquisition, synchronization and channel pulse template estimation. If the input E_b/N_o is >9 dB then the receiver can switch to 50% sampling rate and if the E_b/N_o is >11 dB then a 25% sampling rate can still maintain the 10^{-3} BER link performance as shown in the figure. The 25% sampling rate would correspond to one out of four samples per pulse for the prototype chip. Once the sampling rate is selected the receiver determines the highest energy samples on the channel pulse template, and these same time-samples are used for processing the entire PHY payload (PSDU) in the PPDU packet in Fig. 4.

III. Receiver Description

The simplified receiver block diagram is shown in Fig. 6. The receiver is compatible with IEEE 802.15.4 RF packets apart from sensitivity and outputs the raw binary bits transmitted. The receiver comprises a coherent direct-conversion radio front-end and two 5-bit flash ADCs that operate at a 1 V analog supply while dissipating 0.87 mW and 0.57 mW, respectively. The digital baseband processor operates at a scaled supply voltage of 0.75 V, slightly above the device threshold voltage, while dissipating only 0.58 mW. The DBB power can be further reduced by 8% by reducing the average sampling rate, and maintaining the same link performance, when the input SNR is high.

The RF signal at 2.45 GHz is directly fed into an active Gilbert cell based mixer and quadrature down-converted to

TABLE I
CALCULATED LINK BUDGET FOR THE RECEIVER

Parameter	Specification for 2x Nyquist Rate	Specification for 50% 2x Nyquist Rate	Measured Results
SNR @ 1% PER	-2.2 dB	0 dB	---
Gain	35.4 dB	33.4 dB	37 dB
NF	< 47.6 dB	< 45.6 dB	28 dB
IIP3	> -10 dBm	> -10 dBm	-14.5 dBm
IIP2	> -39 dBm	> -39 dBm	-13.5 dBm
SFDR	> 13 dB	> 13 dB	35 dB
Input power	-55 to -20 dBm	-55 to -20 dBm	-52.5 to -20 dBm
LPF	Third order, Fc=1.5 MHz	Third order, Fc=1.5 MHz	---
ADC resolution	> 3.4 bits	> 3.4 bits	4.3 ENOB
Communication Range @ 7 dBm EIRP	12.3 m	9.8 m	9.2 m (Calculated from measured sensitivity)

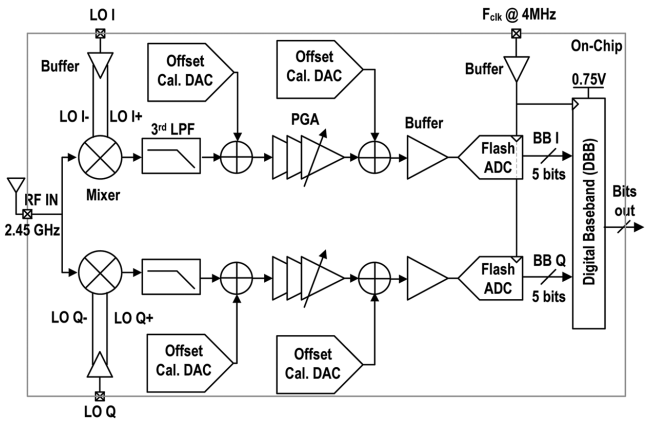

Fig. 6. System block diagram of 2.4 GHz O-QPSK DSSS RX with near-threshold digital baseband.

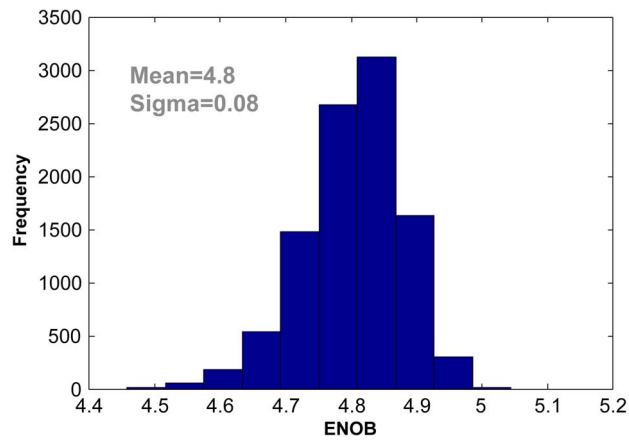

Fig. 7. Simulated Matlab model for flash ADC ENOB.

baseband. Channel selection is performed by a third-order Butterworth gm-C active low-pass filter with a corner frequency of 1.5 MHz. The filtered baseband signal is then amplified by three Programmable Gain Amplifiers (PGAs) and followed by a buffer which drives the input of the flash ADC. The 5-bit flash ADC samples the incoming I & Q baseband signals at 4 MHz (2x the required Nyquist rate). Open loop digital DC-offset calibration is distributed across the front-end by using current DACs (Digital to Analog Converters) in the active filter and PGAs. The I & Q baseband chips are then processed by the DBB (Digital Baseband).

From simulated BER curves, the 5-bit resolution of the flash ADC is determined to have negligible impact on the link performance. The comparator offset in a flash ADC is reduced to be less than LSB/4 by sizing the transistors of the input stage. A MATLAB model has been developed to evaluate the ENOB (Effective Number Of Bits) of the flash ADC for the comparator offset measured from Monte Carlo simulations. Fig. 7 shows that 4.8 bit ENOB is achievable for the flash ADC for the given comparator offset computed from simulations.

The proposed receiver is intended for short-range wireless communication so to extend the communication range the wireless nodes are expected to operate in a mesh network. The Friis equation (6) can be used to calculate the maximum line-of-sight communication range between two sensor nodes. The measured receiver sensitivity from RF-to-bits at 10^{-3} BER is -52.5 dBm. Using the ISM band center frequency of 2.45GHz and assuming a $+7$ dBm EIRP transmitter, the communication range corresponding to -52.5 dBm RX sensitivity is found to be 9.2 m.

$$\frac{P_r}{P_t} = G_t G_r \left(\frac{\lambda}{4\pi R}\right)^2 \tag{6}$$

To obtain the desired performance, we will calculate the NF, linearity, and gain requirements of the receiver, which is summarized in Table I.

A. Noise Figure

The Packet Error Rate (PER) is related to the Symbol Error Rate (SER) if acquisition effects are ignored [10] by the relation,

$$SER = \frac{PER}{symbols/packet} \tag{7}$$

For IEEE 802.15.4, the number of bits in a packet is $\mathrm{N} = 160$ bits with 48 bits of overhead, this corresponds to 52 symbols in a packet and therefore 1% PER corresponds to 0.019% SER. A single symbol error would result in, on average, k/2 bit errors, where $\mathrm{k} = 4$ is the number of bits in a symbol [10]. This corresponds to 0.0095% BER. The BER of O-QPSK modulation with half-sine pulse shaping is given by the Q-function (8) [19].

$$P_e = Q\left(\sqrt{\frac{2E_b}{N_o}}\right) \tag{8}$$

Therefore for 0.0095% BER the required $(\mathrm{E_b/N_o})_{\min}$ would be 8.8 dB.

Direct Sequence Spread Spectrum (DSSS) adds a Coding Gain (CG) and Processing Gain (PG). The coding CG is related to the degree of orthogonality for the code set, which for the DSSS code is calculated from the mean Hamming distance of the code set, $\bar{d}$. The code set for IEEE 802.15.4 is $\mathrm{R}_{15.4}$ with a mean Hamming distance $\bar{d} = 17$ [10]. For DSSS code sequences, the coding gain is approximately given by [19],

$$CG \approx 10\log_{10} k\left(\frac{\bar{d}}{n} - \frac{\ln 2}{\frac{E_b}{N_o}}\right) \tag{9}$$

where n is the length of the code. The CG is approximately 2 dB which reduces the required $(\mathrm{E_b/N_o})_{\mathrm{min}}$ to 6.8 dB. The Processing Gain is calculated by the ratio of the chip rate to the data rate.

$$PG = 10\log_{10}\left(\frac{Chip\ rate}{Data\ rate}\right) \tag{10}$$

The chip rate is 2 Mcps and data rate is 250 Kbps that corresponds to PG of about 9 dB. The PG doesn't reduce the energy per bit required in contrast to CG but it's rather a measure of how much more energy is used to detect a bit as compared to the energy per chip (E_s) [10]. Hence the minimum $(\mathrm{E_s/N_o})_{\mathrm{min}}$ required to achieve 1% PER considering CG and PG can be calculated which is -2.2 dB for the Nyquist rate sampling and about 0 dB for 50% sampling computed from MATLAB simulations as shown in Fig. 5.

For other receiver performance parameters, the ADC reference voltage is 300 mV, reference impedance is 50 Ohms, insertion loss for the RF band select filter is assumed to be 2 dB and the link margin is 10 dB. The NF of the receiver front-end is calculated by (11) where BW is assumed to be 1.5 MHz.

$$NF_{max} = Rss - SNR_{min} - Margin + 174\ (\mathrm{dBm/Hz}) - 10\log_{10} BW \tag{11}$$

where Rss is the target receiver sensitivity.

B. Linearity

The IEEE 802.15.4 standard doesn't specify the linearity requirements of the receiver front-end. Hence the linearity requirements can be derived from the interferer profile [20]. $IIP3$, $IIP2$ and SFDR are calculated as follows [20], [21],

$$IIP3 > \frac{(3P_{int} - P_{sig} + SNR_{min} + Margin)}{2} \tag{12}$$

Where $\mathrm{P_{int}}$ is the power of the interferer and $\mathrm{P_{sig}}$ is the power of the desired signal.

$$IIP2 > 2P_{int} - P_{sig} + SNR_{min} + Margin \tag{13}$$

$$SFDR = \frac{2}{3}(IIP3 - F) - SNR_{min} \tag{14}$$

F is the receiver noise factor.

C. Gain

The maximum and minimum gain required from the front-end assuming 5-bit ADC $(\mathrm{N_{ADC}})$ and a Back Off (BO) margin of 10 dB is calculated as follows,

$$G_{max} = REF_{ADC} - 6N_{ADC} + SNR_{min} - RSS + Margin \tag{15}$$

$$G_{min} = REF_{ADC} - R_{max} - BO \tag{16}$$

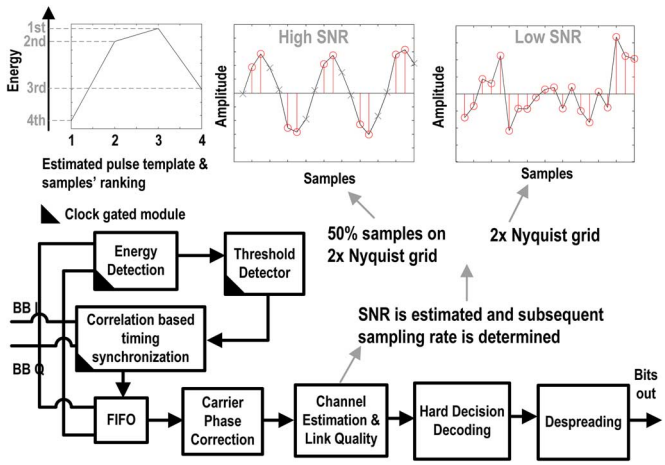

Fig. 8. Simplified digital baseband block diagram and the concept of adaptive signal processing.

Where R_{max} is the maximum received power that is -20 dBm and REF_{ADC} is the ADC reference voltage power relative to 50 Ohm. The theoretical link budget along with measured performance is shown in Table I.

IV. Receiver Implementation

In this section we will discuss the communication signal processing implemented in the digital baseband processor and the circuit details of the RF front-end.

A. Digital Baseband

A simplified digital baseband block diagram is shown in Fig. 8. The digital baseband waits in the idle state, continuously computing the energy of the incoming baseband I & Q symbols. When the received symbol energy crosses a programmable threshold, the digital baseband enters the acquisition and timing-synchronization state. The ideal square header template is used in correlations for achieving timing synchronization. After synchronization, the channel pulse template is computed by averaging 8-chips from the synchronization header. The averaged pulse template is then used to correlate the input I & Q data stream. For coherent demodulation it is assumed that the receiver LO is frequency-locked but not phase-locked with the transmitted 2.45 GHz RF carrier and thus the RF carrier phase offset is estimated by the digital baseband and corrected from the received O-QPSK symbols. This phase offset is calculated by computing the phase of the received O-QPSK symbols and comparing it with the known data transmitted in the synchronization header. A lookup table is used to calculate the phase angles and its corresponding correction factor.

The digital baseband estimates the channel response and determines the link quality. The 4 MHz sampling rate corresponds to four samples per I & Q symbol.

From the computed channel pulse response, the DBB ranks the four samples with respect to energy. This is conceptually illustrated in Fig. 8. By lowering the samples in the case of high SNR, some energy per symbol is traded off with reduced computational power in the following stages. The DBB uses a matched-filter to perform hard decision decoding (HDD). HDD is used for lower computational complexity as compared to soft-decision decoding (SDD), with roughly a 2 dB penalty in link performance [10]. Finally, the de-spreader block de-spreads the received chips and outputs the raw binary data transmitted. For

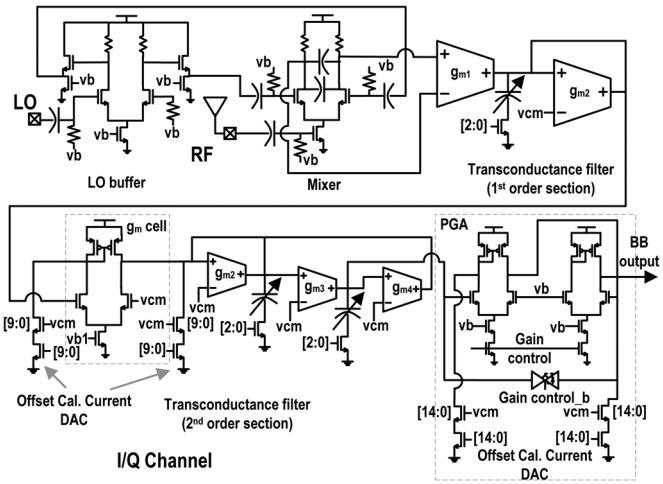

Fig. 9. Schematic of the RF front-end circuits.

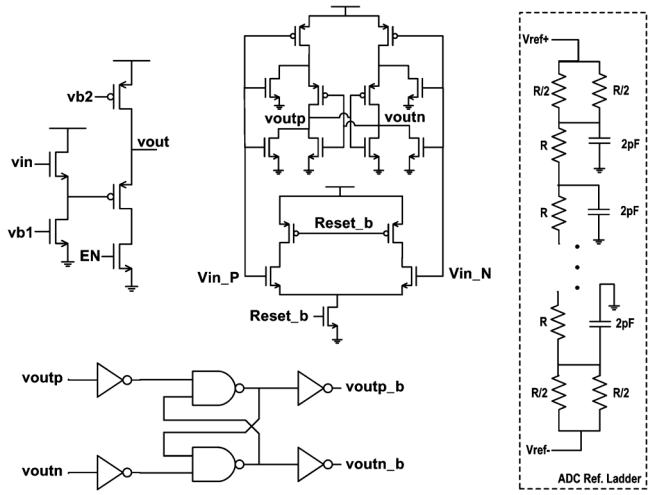

Fig. 10. Buffer driving ADC, comparator, reference ladder and SR latch.

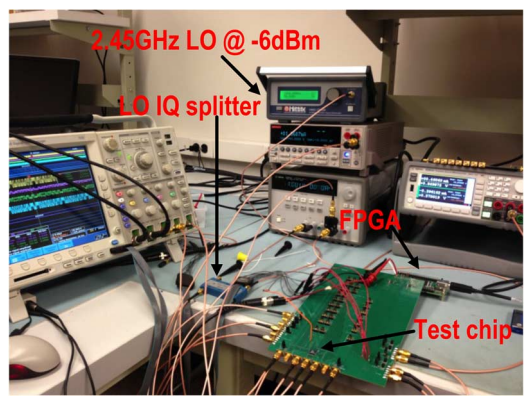

Fig. 11. Measurement setup.

BER testing the DBB enters into a state where it demodulates the data infinitely. Module level clock gating is used in the digital baseband to save power.

B. RF Front-End

The detailed schematic of the I/Q channel of the RF front-end is shown in Fig. 9 with external LO. Single-to- differential conversion of the LO signal is achieved using an on-chip LO buffer, the output of which is then AC coupled to a single-balanced Gilbert-cell active mixer.

The LO buffer is a resistive loaded differential amplifier cascaded with a source follower for a DC level shift. To save power, the receiver doesn't use an LNA and instead relies on an active mixer to provide RF gain. Since the baseband modulated signal has significant low-frequency content, the devices in the active mixer are sized to reduce the flicker-noise corner frequency to <100 KHz.

The IEEE 802.15.4 PHY requires 0 dB rejection at the adjacent channel (± 5 MHz) and 30 dB rejection at the alternate channel (± 10 MHz). Assuming 10 dB margins, 40 dB rejection at the alternate channel can be achieved through the third-order Butterworth-type filter with corner frequency of 1.5 MHz. The filter will provide 50 dB rejection at 10 MHz apart from the wanted signal and thus can be used as the channel selection anti-aliasing filter [17]. To adjust the corner frequency of the filter over process corners, the capacitors are made tunable by a 3-bit binary control word to vary capacitance by $\pm 20\%$.

The differential output of the mixer is converted into single-ended by the input stage of the gm-C filter.

The entire baseband is implemented single-ended to save power. The baseband gain is distributed between the active filter and the PGAs. Programmable gain (PG) is implemented by switchable fixed gain-stages.

The gain stage is implemented as a modified first order gm-C stage. A transmission gate is used which when enabled allows the input signal to bypass the gain stage which is being disabled by a footer. Each PG stage provides a gain of about 8 dB for a total PGAs' gain of roughly 24 dB. For distributed offset calibration, the current DACs are designed to reduce the DC-offset to within LSB/2 of the flash ADC. The output of the PG stages is fed into a buffer that drives the input capacitance of the flash ADC. S/H circuit is avoided at the input of the flash ADC considering that 1 MHz baseband signal isn't fast enough relative to the comparator speed in 65 nm CMOS to cause aperture errors. The LSB size is 9.4 mV for a reference voltage of 300 mV, generated off-chip. To reduce power, no pre-amplifier is used in the comparator that makes the flash converter susceptible to comparator kick-back. To reduce comparator kick-back and the power consumption of the reference ladder, decoupling capacitors of 2 pF are added to the reference ladder as shown in Fig. 10. The output of the comparator is fed into an SR latch, also shown in Fig. 10. The digital baseband converts the thermometer code into binary and uses a simple adding encoders' technique to reduce bubble and sparkle errors of the flash ADC [22].

V. Measurement Results

The measurement setup for the prototype chip is shown in Fig. 11. The receiver is tested with IEEE 802.15.4 RF compatible packets. An off-chip LO power of -6 dBm and a 90° hybrid coupler is used to generate the quadrature LO signals. An FPGA is used to configure the scan-chain. Fig. 12 shows the transmitted I channel modulated data, measured I channel analog baseband waveform along with the digitized output from the I channel ADC for a -40 dBm RF input signal. The transmitted and the received data waveforms are time-delayed and 180° out of phase. Since a coherent receiver is implement this phase shift is corrected in the digital baseband processor. Fig. 13 shows the measured performance of the RF front-end along with the flash ADC spectrum. The flash ADC achieves an ENOB of

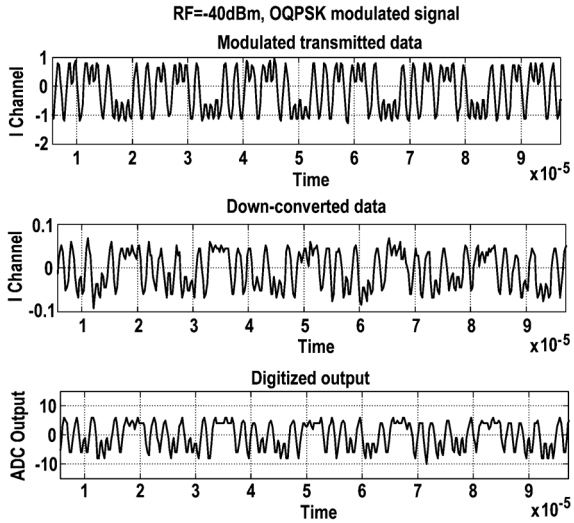

Fig. 12. Measured results for −40 dBm RF input signal. The top plot shows the transmitted O-QPSK data on I channel, the mid-plot shows the down-converted baseband signal at the output of the PGA and the bottom plot shows the flash ADC output for I channel.

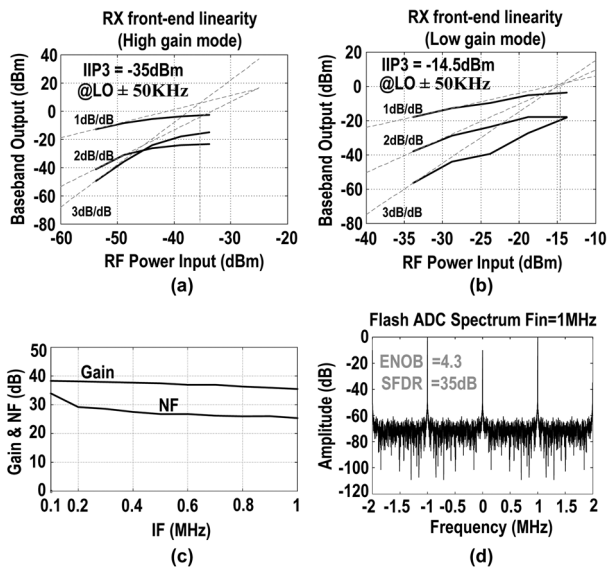

Fig. 13. Measured Gain, NF, IIP3, IIP2 of the RX front-end and flash ADC spectrum.

4.3 at the input frequency of 1 MHz. The total average gain over the IF bandwidth of 1 MHz is 37 dB while the average NF is 28 dB. The measured average NF is about 10 dB lower than the simulated value. This is because the receiver noise is dominated by 1/f flicker noise, which is not accurately modeled in simulations. For linearity measurements, a two-tone test at (LO ±50 KHz) shows the measured IIP3 at high-gain and low-gain setting as −35 dBm and −14 dBm respectively and the measured IIP2 at high-gain and low-gain setting as −25 dBm and −13.5 dBm respectively.

Fig. 14 shows the received RF packets for −40 dBm RF input signal. A dummy PHY payload of binary data 1001_2 is used for the test. The IEEE 802.15.4 standard compliant packet is also shown in the figure. SFD is the start-of-frame delimiter, which is used for frame synchronization. Fig. 15 shows the measured energy efficiency profile of the entire system along with simulated energy efficiency breakdown of the radio, the BER curve and the radar plot of the most desirable RX metrics for comparison.

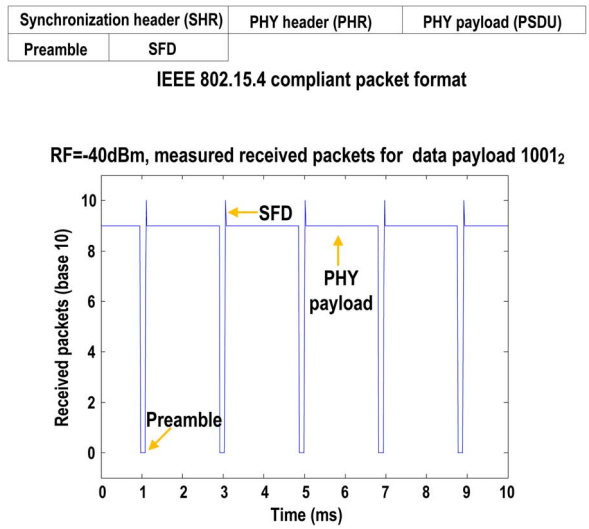

Fig. 14. Measured received RF packets compliant with the IEEE 802.15.4 packet format are shown in the plot, each packet is of duration 2 ms.

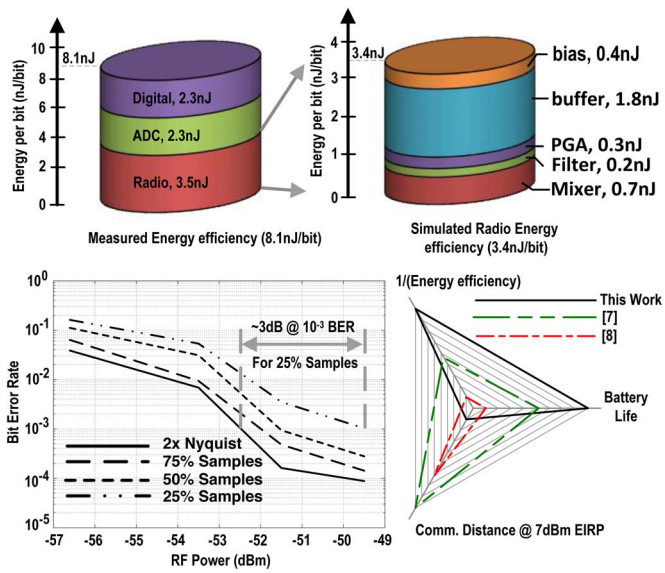

Fig. 15. Measured energy per bit profile along with simulated energy efficiency breakdown of the radio, Bit Error Rate, and the radar plot of the system.

In the radar plot, a bigger star represents a superior design. This plot highlights how communication distance has been traded-off for improved energy efficiency and battery life. The measured energy efficiency of the RF-frontend alone is 3.5 nJ/bit while it is 2.3 nJ/bit for the ADC and the DBB.

For a BER test the DBB enters into a state where it receives the data infinitely. The measured sensitivity of the RX is −52.5 dBm at 10^{-3} BER. From the measured BER performance, it is observed that if the input SNR is about 3 dB higher at 2x the Nyquist sampling than for the same link performance of 10^{-3} the DBB can be operated at 25% samples with an energy efficiency of 2.1 nJ/bit.

Table II summarizes the performance of the system and benchmarks with other 2.4 GHz short-range IEEE 802.15.4 (O-QPSK DSSS modulation) radios.

The entire system is implemented in 65 nm CMOS with active area of 0.86 mm^2 as shown in Fig. 17. It should be noted that these results do not include an input-matching network, and measured S11 of the RF input is plotted in Fig. 16. An off-chip

TABLE II
SUMMARY AND PERFORMANCE COMPARISON

	This work	[7]	[8]	[23]
Architecture	Zero-IF	Sliding-IF	Low IF (2 MHz)	Zero-IF
Technology	65 nm	90 nm	65 nm	180 nm
Integrated Digital Baseband	YES	NO	NO	NO
Data rate & modulation	250 Kbps O-QPSK DSSS	250 Kbps O-QPSK DSSS	250 Kbps O-QPSK DSSS	250 Kbps O-QPSK DSSS
RX energy efficiency	3.5 nJ/bit (excluding ADC)	7.2 nJ/bit (excluding ADC)	6.8 nJ/bit (excluding ADC)	50.4 nJ/bit (including ADC)
RX sensitivity	-52.5 dBm*$_1$	-100 dBm*$_2$	---	-96 dBm*$_2$
RX IIP3 (High gain)	-35 dBm	-19 dBm	-6 dBm	-18 dBm
IIP3 (Low gain)	-14.5 dBm	---	---	
RX gain (dB)	37	76	57	83.5
RX NF (dB)	28	6	8.5	9.5
Power Radio (mW)	0.87 @ 1V	1.8**	1.7**	12.6** (including ADC) Pipeline
Power ADC (mW)	0.57 @1V flash	0.3 SAR	---	
Power Digital Baseband (DBB) (mW)	0.58 @ 0.75V	---	---	---
Active Area (mm^2)	0.86	---	0.22	---

*$_1$ Sensitivity measured @ BER 10^{-3}
*$_2$ Sensitivity measured @ PER 1%
** Excluding frequency synthesizer

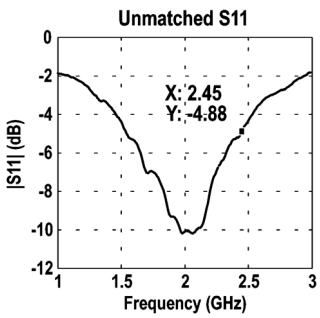

Fig. 16. Measured S11 (without impedance matching) at the RF input.

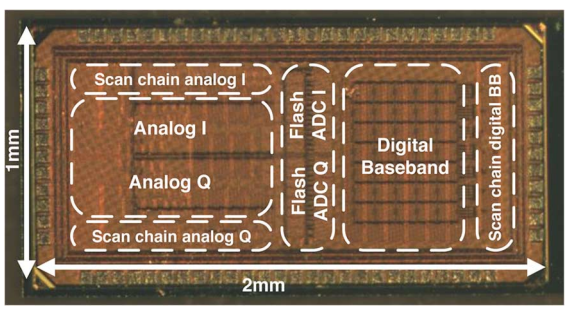

Fig. 17. Die photo.

passive matching network can be designed which could theoretically further improve the receiver sensitivity.

For a complete solution the RX would require an on-chip LO. In order to estimate total power, we draw from previously published LOs. A 2.4 GHz LO generated using a PLL consumed 1.6 mW including the PLL, LC-VCO and VCO buffer [7] and 1.2 mW for an entire QVCO in [24]. This corresponds to roughly total power of 3 mW for a complete receiver, including this work.

This RX has 2x better energy efficiency for the radio front-end (3.5 nJ/bit) than the prior art, while reporting 8.1nJ/bit energy efficiency for an O-QPSK DSSS coherent receiver with near-threshold digital baseband.

VI. CONCLUSION

Radio energy efficiency is going to play a key role in extending the battery life of future IoT devices. Different design tradeoffs can be made for these emerging applications as compared to the conventional high performance radios. We have explored the sensitivity vs. power tradeoff and have presented a low-power (2 mW) short-range O-QPSK DSSS receiver with integrated digital baseband. The radio receiver also adapts its average sampling rate for high input SNR while still maintaining the target link performance of 10^{-3} BER to save power in the digital baseband.

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