Wireless Wafer-Level Testing of Integrated Circuits via Capacitively-Coupled Channels

Dae Young Lee, David D. Wentzloff, and John P. Hayes

Department of Electrical Engineering and Computer Science
University of Michigan
Ann Arbor, MI 48109, USA
{duelee, wentzlof, jhayes}@umich.edu

***Abstract*—Wafer testing via direct-contact probe cards has long been an effective and relatively low-cost method for testing integrated circuit (IC) chips prior to packaging. However, the physical contact occurring between the wafer and automatic test equipment (ATE) has significant costs due to contact point deformation and the need for abrasive cleaning. In this paper, we investigate a non-contact testing technique that wirelessly couples an IC wafer and ATE, and serves as an alternative to conventional probe-card testing. We derive several analytical models for a capacitive testing channel. Electromagnetic field simulations results are presented that support the proposed channel models. We conclude that capacitance-based wireless testing is feasible for testing ICs in the 1-GHz range.**

***Index Terms*—Wireless testing, near-field communication, probe card, capacitive coupling, proximity communication.**

I. Introduction

As IC technology moves toward the nanoscale, the cost of manufacturing a transistor has decreased dramatically. However, the testing cost per transistor remains much the same, or is even rising [1]. As a result, the contribution of testing to overall IC production costs is an increasing cause for concern. ATE with direct-contact probe cards has long been the standard approach to wafer testing. Recently, however, it has been undergoing scrutiny due to the need to test very complex ICs, as well as novel package types, such as three-dimensional (3D) ICs and systems-in–a-package (SIPs). These newer IC products are less amenable to probe testing than conventional ones [1].

The direct-contact probe card has several fundamental limitations. Since probe tips physically touch down on a wafer, they undergo contact point deformation and debris accumulates on the probe tips [2]. An abrasive cleaner can be used to remove the debris, but it increases testing cost and its repeated use may damage the probes. In addition, the locations of the probe tips are fixed, so a probe card cannot be reused for different devices under test (DUTs).

Scaling trends also make probe card testing less suitable for future ICs. As devices scale down, the size and pitch of I/O pads gradually shrink as well, requiring very small contact points. Higher I/O signal frequency is also problematic for probe-card testing. To minimize the time spent on the ATE, at-speed testing is desirable. However, scaling trends require very high I/O frequency for at-speed testing [1]. High-frequency probe tips need careful characterization for impedance matching, which is yet another cost-increasing factor.

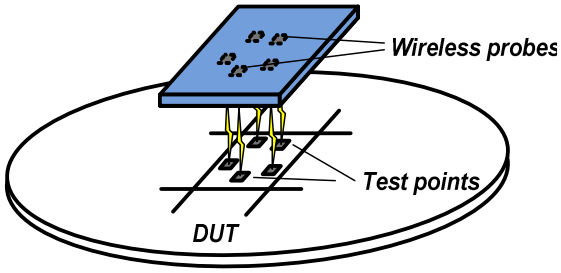

Fig. 1. Concept of wireless wafer-level testing.

For all these reasons, despite the fact that direct-contact probing is the standard practice in the IC industry, this approach is likely to become less effective and more costly for future IC testing. Wireless wafer-level testing has been proposed as an alternative, whose goal is to replace physical contact points (bond pads) with wireless channels and antennas. The concept of wireless wafer-level testing is shown in Figure 1. Both digital and analog signals can be transmitted through the wireless channels. Power can also be delivered either via wireless communication or wired power lines. By eliminating physical touch-downs, many of the problems associated with direct-contact probing can be greatly alleviated.

Wireless wafer-level testing has several unique features that distinguish it from other wireless applications. First, the communication range can be as short as a few micro-meters—there is virtually nothing between a wafer and its tester. Second, channel alignment may not be a significant issue. A conventional wafer-level tester must accurately align micrometer-size probe tips down to a couple of micrometers. Similar alignment techniques can be used for wireless wafer-level testing as well, but minor misalignments can be tolerated. Finally, the wireless channel creates an asymmetric relation between the DUT and the tester. While the DUT has a limited power source, the ATE is not limited by its power consumption. The characteristics will be discussed in detail later to evaluate potential wireless technologies for wireless wafer-level testing.

Wireless IC testing has been proposed before [3]. Salzman and Knight proposed capacitive coupling as a communication channel to address the problem of testing a multi-chip package (MCP). Although this work mainly discusses the testing of diced chips, the same technology can be used for wafer testing as well. Practical implementations can be found in [4][5], which demonstrate the feasibility of

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gigahertz wireless wafer-level testing. However, analytical channel models are not provided.

We present several analytical models for on-chip capacitive coupling. The proposed models can be used for the channel performance prediction and antenna design. Based on these models, cross-talk and misalignment will be analyzed as well.

This paper is organized as follows. In Section II, capacitive and inductive coupling are compared. Analytical models for capacitive-coupled test channels are presented in Section III. The analysis of cross-talk from adjacent channels is discussed in Section IV. Misalignment simulation results are given in Section V. Finally, Section VI presents our conclusions on the feasibility of capacitively-coupled wireless testing.

II. Coupling Techniques for Wireless Testing

There are at least three potential wireless technologies for wafer-level testing: far-field (RF), near-field, and optical communication. RF links support long range communication, but they require complex circuits with large antennas, and it is difficult to distinguish individual dies on a wafer during testing [6]. Although optical links provide relatively easy circuit implementations and high signal strength, they are not compatible with conventional CMOS process [7]. Optical communication is also too costly for IC testing. RF and near-field communication employ essentially the same electromagnetic technology, but near-field communication is more efficient over very short range [8]. Many applications that use near-field communication have been introduced, including wafer testing, chip-to-chip communication, and biomedical implant devices [4][5][9-15].

Wafer-level testing requires very short communication range, making it well-suited to near-filed methods. As noted above, a wafer and a tester can be as close as a few micrometers. Near-field antennas are more efficient than the linear-shape antennas needed for RF communication in the near-field zone. In addition, near-field communication does not suffer from wave propagation effects like reflection and multi-path delay, which also require complex and power-consuming circuits.

There are two near-field communication approaches, inductive and capacitive. Capacitive coupling delivers electromagnetic energy through electric coupling between two metal plates (electrodes), while inductive coupling does so via the magnetic coupling of two coils. Capacitive coupling highly depends on the permittivity of the medium between the plates. The permeability of the medium between the coils is critical for inductive coupling.

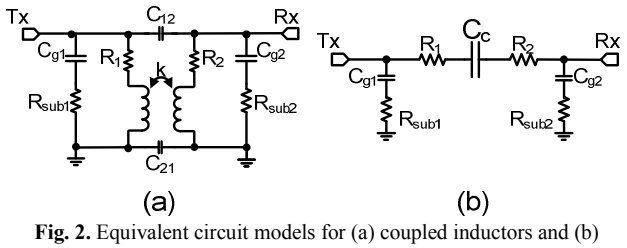

Fig. 2. Equivalent circuit models for (a) coupled inductors and (b) coupled capacitors.

On-chip lumped circuit models for both capacitive and inductive coupling are shown in Figure 2. Here the substrate resistance and parasitic coupling of the inductive approach are ignored. For inductive coupling, the voltage transfer function can be written as follows [13].

$$\frac{V_{Rx}}{V_{Tx}} = \frac{j\omega k\sqrt{L_1 L_2}}{1+j\omega C_{g2}R_2} \cdot \frac{1}{R_L(1-\omega^2 L_1 C_1)+R_1+j\omega(C_1 R_1 R_L + L_1)} \quad (1)$$

For capacitive coupling, the corresponding equation is

$$\frac{V_{Rx}}{V_{Tx}} = \frac{j\omega R_L C_C}{1+j\omega R_L(C_{g2}+C_C)+(R_1+R_2)C_C(j\omega-\omega^2 R_L C_{g2})}. \quad (2)$$

From these equations, it can be seen that the capacitive coupling is highly dependent on the coupling capacitance C_c, while inductive coupling depends on the coupling coefficient k of the two coils.

The ideal expressions for C_C and k are as follows.

$$C = \varepsilon\frac{A}{h} \quad (3)$$

where ε is the permittivity of medium between the coupled plates. A is the area of plates, and h is their separation distance. The inductive coupling coefficient can be written as

$$k = \frac{M}{\sqrt{L_1 L_1}} = \frac{\mu\pi r_1 r_2 N_1 N_2}{2R^3\sqrt{L_1 L_1}}. \quad (4)$$

Here, μ is the permeability of medium, r is the radius of each coil, N is the number of turns, and L is the self-inductance of the coils. R is the separation of the coils.

Based on the foregoing model, the coupling capacitance can be maximized by using large metal plates with small separation. The inductive coupling coefficient can be increased when larger coils with more turns and shorter separation distance are used.

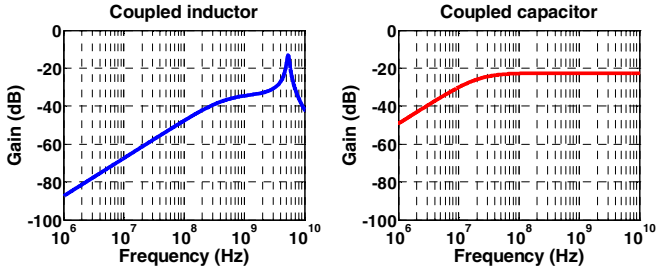

Fig. 3. Simulated frequency response with 20 μm separation.

The results of a frequency response simulation employing simple 3D on-chip models are given in Figure 3. The coupled inductors and capacitors are both of size 30μm × 30μm with 20μm spacing and simulated with Ansoft's HFSS v11. For each case, the voltage gain was measured, which is the output voltage divided by the input voltage. As expected, inductive coupling has a resonant peak in voltage gain, but the gain for capacitive coupling monotonically increases. To maximize efficiency, it is desirable to use the resonant frequency in inductive coupling. For capacitive coupling, using a higher frequency is better in most cases.

We decided to focus on capacitive coupling for our wireless wafer-level testing study. Although inductive

	Gu *et al*., 2007 ISSCC [9]	Fazzi *et al*., 2008 JSSC [10]	Daito *et al*., 2010 ISSCC [4]	Kim *et al*., 2010 3DIC [5]	Miura *et al*., 2007 ISSCC [11]
Basic technology	Capacitive	Capacitive	Capacitive	Capacitive	Inductive
Application	Chip-to-chip	Chip-to-chip	IC Testing	IC Testing	Chip-to-chip
Energy/bit	0.27pJ/b	0.15pJ/b	2pJ/b	0.47pJ/b	0.33pJ/b
Data rate/ch	10Gbs/ch	2.46Gbs/ch	1Gbs/ch	15Gbs/ch	1Gbs/ch
BER	$<10^{-12}$	$<10^{-12}$	$<10^{-12}$	$<10^{-12}$	$<10^{-12}$
Process	0.18µm CMOS	0.13µm CMOS	90nm CMOS	65nm CMOS	0.18µm CMOS
Range *R*	3µm	<1µm	4µm	4µm	15µm
Size of channel	2x48x18 μm^2	15x15 μm^2	80x80 μm^2	80x80 μm^2	30x30 μm^2

Table 1. Performance comparison of various prior chip-level wireless communication systems.

coupling provides more design options, such as the number of turns and longer communication distance, capacitive coupling seems more promising for wireless wafer-level testing for several reasons. First, the communication distance can be extremely small, which is well-suited to capacitive coupling. Second, a capacitively-coupled channel does not have a resonant peak in the frequency range that we are interested in. It is set at extremely high frequency. Thus, the gain monotonically increases within the frequency range of interest. In contrast, conventional on-chip inductive coils resonate at a relatively lower frequency than capacitive electrodes. Varactors can be used to adjust the resonant frequency, but they consume area and require careful calibrations. Thus, to meet the requirement of high speed I/O (up to ten gigahertz), inductive coupling seems inefficient.

Many similar applications involving near-field communication have been reported [4][5][9-15]. The practical circuit design and implementation of wireless wafer-level testing via capacitive coupling are demonstrated in [4][5]. Both show that capacitive coupling can achieve gigahertz communication rates with a short communication range. Wireless wafer-level testing via inductive coupling was also proposed in [14]. The data rate reported in [14] is relatively slower than other published work. Capacitive coupling has also been proposed as a potential technology for wireless chip-to-chip communication for 3D stacked chips, which require a communication distance and an on-chip antenna similar to wafer-level testing [9][10]. Both synchronous and asynchronous communication channels are proposed in the papers.

A comparison of relevant previously published work is presented in Table 1. Capacitive coupling can achieve very high data rate with face-to-face chip stacking because the communication distance can be shorter than 5 µm. Inductive coupling can achieve a longer communication range, but consumes more power [11]. All capacitive techniques can achieve data rates higher than 1Gbps with very low bit-error rate (BER) due to the relatively short communication distance. Together, these examples support the case for capacitive coupling in wireless wafer-level testing.

III. On-chip Circuit Model of Capacitive Coupling

Two capacitively-coupled metal plates can be modeled with the ideal capacitance model given in (3). This is a simplified model in which fringing effects along the edges of the metal plates have been removed. Thus, it is only valid when the plates are infinitesimally thin, and the separation between them is relatively small.

More accurate capacitance models can be found in [16][17]. In reality, the metal plates have a non-zero thickness that cannot be ignored in practice. This thickness contributes to fringing capacitance and increases overall capacitance between the two plates. In [16], Yuan and Trick model metal plates with non-zero thickness as a combination of ideal plates and two cylindrical sidewalls. Therefore the model is only valid for when the thickness is relatively small.

A capacitance model of even greater accuracy can be found in [17]. This model widens the valid thickness range by adding E-field effects from the top surface. However, compared to Yuan and Trick's model, it is an experimental model with less analytical justification.

We carried out a number of simulation experiments using Ansoft's HFSS v11, an electromagnetic field solver. With an on-chip 3D model of the coupled plates, the coupling capacitance C_C was extracted. For the simulations, two on-chip 92µm × 52µm sized metal plates were placed with varying separations. The HFSS-simulated results are compared with various analytical capacitance models in Figure 4. While van der Meijs and Fokkema's model [17] has the closest result to the extracted capacitance, the ideal plate model is still comparable with a very short separation 1/10 of the size of metal plates. In addition, since the ideal model always underestimates the capacitance, it can be used for a quick calculation with a worst-case assumption.

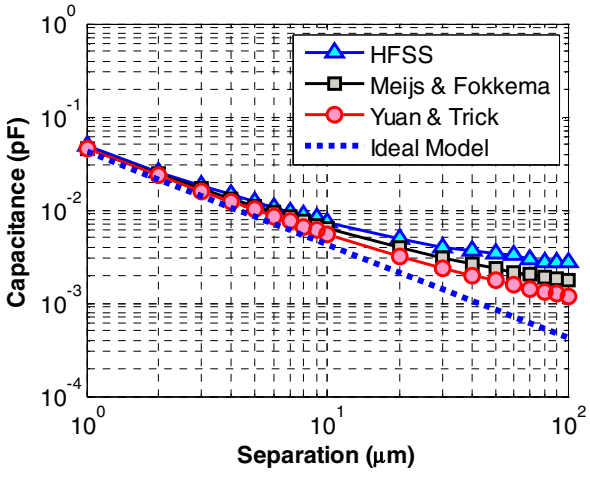

Fig. 4. Simulated coupled capacitor model with fringing capacitance.

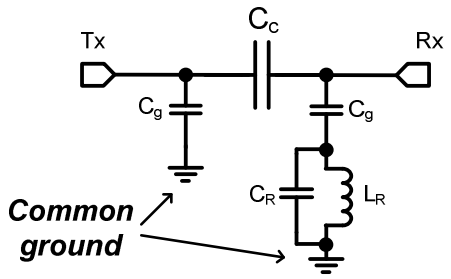

Fig. 5. More accurate on-chip capacitor model with current return paths.

Another issue for on-chip capacitance modeling is the permittivity of the medium between the two metal plates. Since there is no blocking material between a DUT on a wafer and the tester, the medium can be modeled as vacuum. In practice, the metal plates are usually implemented with the last metal layer of the IC process. There exists a passivation layer above the last metal layer, which has permittivity around 3.4. Therefore, for better accuracy, the on-chip capacitive coupling model should include the effect of the passivation layer. As for the ideal capacitance model, the vacuum can be used for the worst-case assumption for a quick estimation. Then, a more accurate model can be used for more exact analysis.

The voltage transfer function of on-chip capacitive coupling given in (2) can be further simplified. If the series resistance of the metal plates is ignored, the transfer function reduces to that of a voltage divider.

$$\frac{V_{Rx}}{V_{Tx}} = \frac{C_c}{C_c + C_g} \tag{5}$$

Here, C_c is coupling capacitance between the metal plates, and C_g is the capacitance to ground. As discussed, higher C_c is desirable to achieve higher voltage gain, and can be modeled with the ideal capacitance model.

The use of separate grounds for the DUT and tester are also critical in modeling. An ideal common ground is assumed for the on-chip voltage transfer function in both (3) and (5). However, in reality both chips have different grounds, and these different grounds may affect channel gain significantly. For example, if there is no closed current return path, a very large current loop will cause substantial parasitic inductance, which lowers the resonant frequency, and may render of the entire system unstable. To avoid this, AC grounds should be placed on-chip to provide current return paths for high frequency signals.

A more accurate voltage transfer function including current return paths and AC grounds can be written as follows.

$$\frac{V_{Rx}}{V_{Tx}} = \frac{s^2 L_R C_c \left(C_R + C_g\right) + C_c}{s^2 L_R \left\{C_R \left(C_c + C_g\right) + C_c C_g\right\} + C_c + C_g} \tag{6}$$

L_R and C_R are added parasitic inductance and capacitance from the return paths and grounds. The lumped circuit model is depicted in Figure 5.

Based on this new model, we can conclude that parasitic inductance from the current return paths should be kept as small as possible, and the capacitive coupling of the AC ground should be large enough to support good current returns. Since the combination of these parasitics can cause resonance, their poles and zeros should be shifted to very high frequencies in order not to affect the system stability. When this condition is met, the more accurate model can be approximated by the simpler voltage divider model in (5).

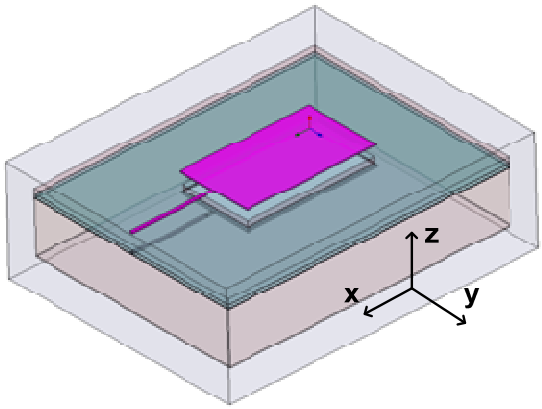

Fig. 6. On-chip 3D model of capacitive coupling.

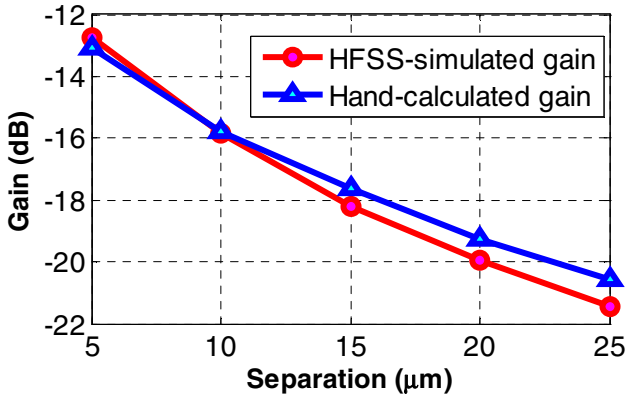

Fig. 7. Gain vs. plate separation for capacitive coupling.

A 3D model of an on-chip capacitor with 95μm × 52μm metal plates shown in Figure 6 was simulated using HFSS v11. As Figure 7 shows, the HFSS-extracted gain matches well with the hand-calculated gain from an ideal plate model for small separation distances. For wider separation (over 15μm), the difference gets larger since the ideal plate model underestimates fringing effects.

IV. Cross-Talk Analysis

Although near-field radiation is only strong enough at very short range, cross-talk from adjacent channels is still a critical source of interference. The worst-case scenario of adjacent channel interference is depicted in Figure 8.

When a transmitter Tx drives a target receiver Rx, there are two possible interference sources from adjacent channels: one on the same chip and one on the other chip. Since a channel is configured for unidirectional communication, only one case is possible at any time. Between the two cases, the aggressors from the same chip degrade channel gain more than those from the other chip due to large metal plate separation and small overlapping area. Most fringing capacitance is screened by the metal plates, and the distance to aggressors on the same chip is always shorter. Thus, the

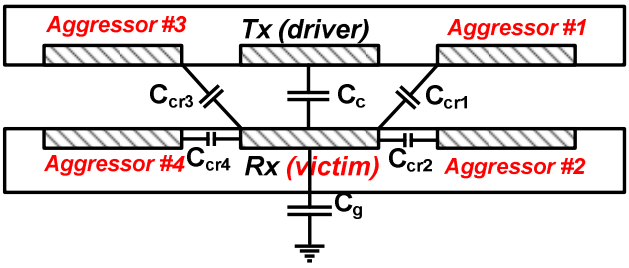

Fig. 8. Cross-talk model for on-chip capacitive coupling.

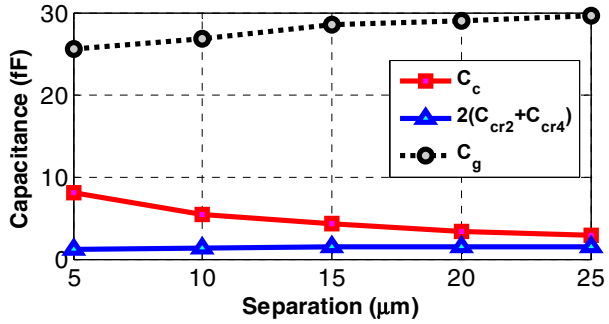

Fig. 9. Simulated capacitance vs. plate separation.

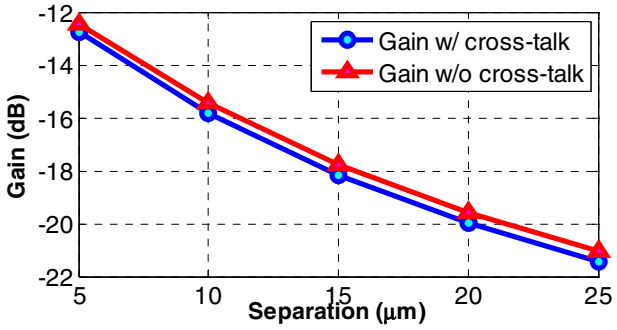

Fig. 10. Gain comparison with cross-talk effects.

cross-talk capacitance C_{cr2} and C_{cr4} should be added to the voltage transfer function to estimate the effect of cross-talk.

If we assume the worst case, the cross-talk capacitance needs to be doubled due to the Miller effect. If the two coupled nodes switch in opposite directions at the same time, the effective coupling capacitance also is doubled. The voltage transfer function with cross-talk is then as follows.

$$\frac{V_{Rx}}{V_{Tx}} = \frac{s^2 L_R C_c \left(C_R + C_p\right) + C_c}{s^2 L_R \left\{C_R \left(C_c + C_p\right) + C_c C_p\right\} + C_c + C_p} \tag{7}$$

$$C_p = C_g + 2 \cdot \left(C_{cr2} + C_{cr4}\right) \tag{8}$$

The effect of cross-talk contributes to the overall capacitance to ground, and results in reduced voltage gain.

Fortunately, the sidewalls of the metal plates used for capacitive coupling are quite small. Fringing effects from the top and bottom sides are blocked by other metal plates if other channels are relatively close. Therefore, the cross-talk capacitance from adjacent channel is expected to be relatively small compared to the coupling capacitance C_c and the parasitic capacitance to ground C_g.

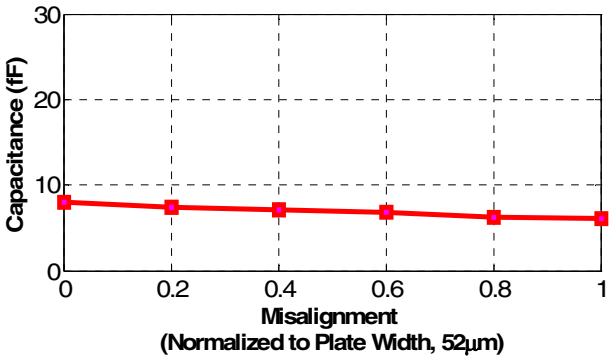

Fig. 11. Coupling capacitance vs. misalignment.

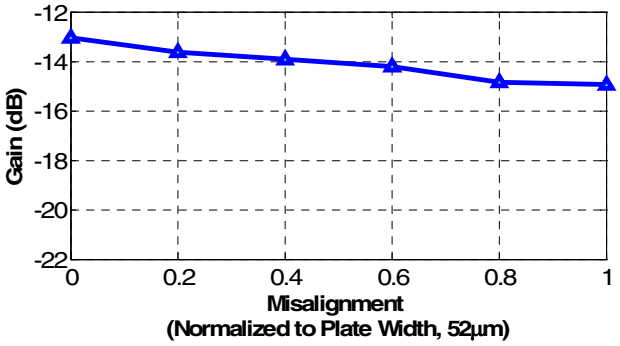

Fig. 12. Gain vs. misalignment.

HFSS simulations were conducted for the same metal plates (95µm × 52µm) shown in Figure 6 with lateral spacing of 17µm, which is the minimum spacing from the design rule for I/O pads. The overall capacitance from cross-talk $2(C_{cr2} + C_{cr4})$ was found to be less than 1fF. As shown in Figure 9, the simulated C_c and C_g were 8fF and 25.6fF, respectively, at a separation of 5µm. As expected, C_g and $(C_{cr2} + C_{cr4})$ remain almost the same at wider separation. Both capacitance types increase with increasing separation due to less screening effect caused by metal plates on the other chip. C_c continuously decreases with increasing separation.

From the simulation results in Figure 10, we can conclude that the effect of cross-talk is not substantial in capacitive coupling. However, since the cross-talk highly depends on metal plate size and spacing, careful analysis must be done for correct channel characterization.

V. Misalignment Tolerance

Since a conventional probe card tester can touch down on a wafer with micrometer precision, misalignment of the channel plates in a capacitively-coupled tester may not be a serious problem. Nevertheless, an analysis of plate alignment is still worth doing to determine the minimum lateral spacing of different channels and reduce the potential cost of high-precision alignment. Like cross-talk, misalignment manifests itself as a change in capacitance. In most cases, misalignment greatly affects coupling capacitance, and so results in gain degradation. In contrast, the parasitic capacitance to ground remains essentially unchanged.

The same 3D capacitor model with 5µm separation has been used for a HFSS simulation of misalignment. The *y*-

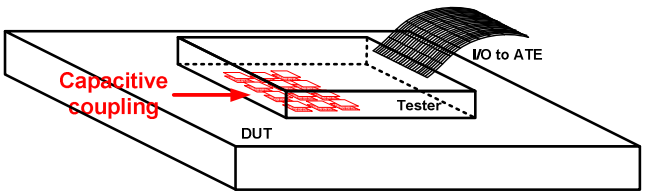

Fig. 13. Proposed wireless wafer-level tester.

location of the top metal plate was changed from 0µm to 50µm. Since the width of the metal plate is assumed to be 52µm, a *y*-direction sweep covers most cases of misalignment. Figure 11 show the simulated results. As misalignment increases, the coupling capacitance becomes smaller. However, even for 50µm misalignment, the capacitance does not decrease significantly with no overlapping of the metal plates.

Compared to the results of cross-talk simulation with similarly located plates, the coupling capacitance is quite substantial. This is believed to be because of fringing effects. There is no material which screens fringing capacitance between diagonally placed plates. Thus, the top and bottom surface of the metal plates can form capacitive coupling in spite of almost no overlapping area.

The effect of misalignment on channel gain is shown in Figure 12. Even with the maximum misalignment, the gain decreases by only 2dB. We can therefore conclude that a capacitively-coupled channel shows good misalignment tolerance up to the size of the metal plates.

VI. Conclusions

Wireless testing is an alternative to direct-contact testing of IC wafers that greatly reduces the costs associated with probe employment and wear. Due to the very short communication range required, capacitive coupling seems the most feasible wireless communication technology for this application. We have presented analytical models and simulation results that support the validity of this approach. They demonstrate that the gain of a capacitively-coupled channel can be easily predicted. Moreover, the cross-talk and misalignment results indicate that capacitive coupling experiences relatively low adjacent channel interference, and has good misalignment tolerance. In summary, capacitively-coupled wireless testing of the kind depicted in Figure 13 offers an attractive alternative to conventional wafer probing.

Of course, there are other issues that need to be addressed to make wireless testing at the wafer level practical. These include tester reconfiguration, wireless power transfer, and low-power test circuits. These issues can be mitigated by various circuit techniques. For example, tester reconfiguration may be implemented using a shared channel with various multiple-access schemes such as TDMA (time division multiple access) or CDMA (code division multiple access). Wireless power transfer through capacitively-coupled channels has been proposed in [18].

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