A 3.1 to 10.6 GHz 100 Mb/s Pulse-Based Ultra-Wideband Radio Receiver Chipset

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Abstract **— A complete 3.1-10.6 GHz ultra-wideband receiver using 500 MHz-wide sub-banded binary phase shift keyed (BPSK) pulses has been specified, designed and integrated as a three chip and planar antenna solution. The system includes a custom designed 3.1-10.6 GHz planar antenna, direct-conversion RF front-end, 500 MS/s analog to digital converters, and a parallelized digital back-end for signal detection and demodulation. A 100 Mb/s wireless link has been established with this chipset. A bit-error-rate (BER) of 10^{-3} was recorded at -80 dBm at a rate of 100 Mb/s for properly acquired packets in the lowest frequency band. Bit-scaling of the ADC from 1 to 5 bits reveals a 4 dB improvement in the link budget.**

Index Terms **— Ultra-wideband, UWB, bit-error-rate, BER, receiver, system, chipset.**

I. Introduction

Upon the release of the 3.1-10.6 GHz band for unlicensed UWB radio operation by the FCC, there has been a variety of coherent signaling techniques [1] and corresponding transceiver architectures [2], [3] to utilize this available bandwidth for implementing high data-rate wireless personal area network radios. This paper describes a complete UWB receiver designed and integrated as a three chip and planar antenna solution, demonstrating 100 Mb/s wireless reception.

A. Signaling

This system has adopted a sub-banded binary phase shift keyed (BPSK) pulse signaling technique. The pulse shape is a Gaussian with $\sigma \approx 1$ ns due to its desirable time and frequency response to occupy the sub-band bandwidth. The pulse repetition frequency (PRF) is 100 MHz, corresponding to a maximum data rate of 100 Mb/s. Fig. 1 shows the baseband pulse train signal, which is then up-converted to one of 14 channels in the UWB band. The frequency plan is shown in Fig. 2, and f_{center} of each band is described by (1).

$$f_{center} = 2904 + 528 \cdot n_{ch}[MHz],\ n_{ch} = \{1,2,...,14\} \qquad (1)$$

The -10 dB bandwidth of the RF pulses is 500 MHz.

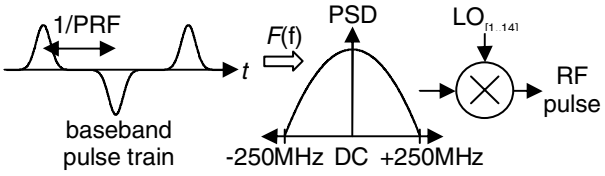

Fig. 1. Baseband Gaussian pulse train with BPSK modulation.

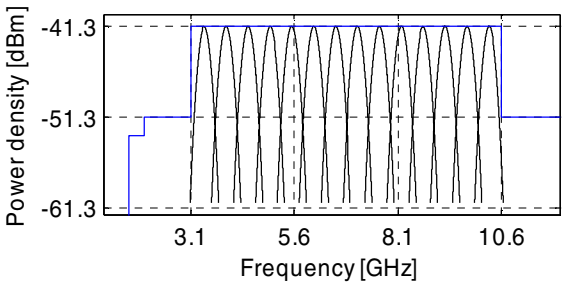

Fig. 2. Frequency plan showing 14 non-overlapping channels and the FCC indoor spectral density limit. BPSK pulses are up-converted to one 528 MHz wide channel.

B. Packet Architecture

The UWB data packet is comprised of a preamble and a payload, both of fixed length. The preamble contains pulses that are separated by 60 ns. It repeats a 31-pulse Gold code 19 times, which is used by the digital baseband to detect the presence of the packet and to achieve packet acquisition. The larger time interval between pulses in the preamble allows the receiver to estimate the channel impulse response without significant inter-symbol interference (ISI) for a worst-case multi-path channel environment.

The payload is comprised of 4K pulses transmitted with a pulse repetition frequency of 100 MHz. Since each bit of information is represented by one pulse, this system transmits at a raw data rate of 100 Mb/s. At the start of the payload, a known sequence of 32 bits is included to mark the beginning of the payload.

Including a 10 µs guard time between packets, a complete packet transmission occurs in less than 100 µs.

II. System Architecture

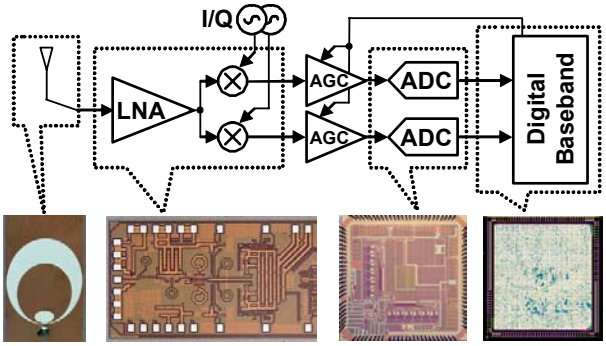

Fig. 3. Receiver block diagram with associated chipsets and photograph of antenna.

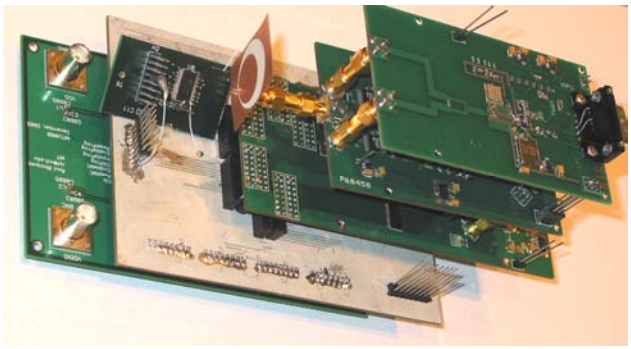

Fig. 4. Photograph of complete UWB receiver chipset solution.

The mostly-digital direct-conversion receiver architecture [4] is shown in Fig. 3 with corresponding photographs of the implemented antenna and chipset. The 500 MHz-wide wireless signal energy centered at f_{center} is electromagnetically captured by the omni-directional 3.1-10.6 GHz UWB antenna [5] and then amplified, filtered, and down-converted to a 250 MHz baseband signal by the front-end designed in a 0.18 µm BiCMOS process [6]. The PLL supplying the local oscillator (LO) and I/Q conversion is commercially available, as are the following automatic gain control (AGC) baseband 3 dB gain stages and discrete-element 4th order Chebyshev low-pass filters at 250 MHz. Dual 500 MS/s ADCs designed in a 0.18 µm CMOS process sample I/Q baseband signals and perform a serial-to-parallel conversion to feed the digitized samples to the digital baseband at a more manageable clock rate [7]. The digital baseband receives its master clock from the ADC, latches in the samples, and performs signal detection and data demodulation on the digitized samples [8]. It also has feedback control for the AGC gain values following the RF front-end. The entire receiver system is assembled together on five custom PC boards with careful attention towards isolation, signal integrity, and power distribution. Fig. 4 shows the board stack of the receiver.

Assembly and testing of the full system allows verification of the original system design choices. It also allows for quantification in BER of the effects of low-level adjustable knobs (ADC bit resolution, AGC gain control), wireless channel and interference robustness, and scattered non-idealities of the implemented system (I/Q mismatch, DC offsets). The following subsections describe each component of the system in more detail.

A. *Transmitter*

The UWB signal is generated using a discrete pulse generator, up-conversion mixer, and a commercially available PLL. The transmitter is shown in Fig. 5. It is interfaced to a PC through a USB 2.0/FPGA board.

Fig. 5. Pulse generator.

B. *UWB Antenna*

Several challenges are addressed in the UWB antenna design. These include achieving the impedance bandwidth, radiation pattern, and meeting the efficiency and physical constraints which are required by a physically small, planar design for compatibility with electronic devices. The UWB antenna in [5] is designed such that a 50 Ω impedance match appears directly at the antenna feed by adjusting for the optimal spacing between the ground plane and the elliptical antenna. The wideband characteristic is achieved through an exponential taper from the ground plane to the antenna. The bandwidth for this topology is very close to that of the circular disc monopole described in [9].

The impedance bandwidth throughout the UWB frequency range has a measured VSWR below 1.5. The gain pattern in the azimuth plane is constant for almost an octave, with a gain of 2.5-3 dBi. The average half-power beamwidth in the elevation plane is 73°, indicating a dipolar antenna pattern. The measured antenna efficiency is 93%. The antenna feed is carefully constructed with an MMCX adapted to SMA female connector.

C. RF Front-End

The 0.18 μm SiGe BiCMOS front-end is comprised of a 3.1-10.6 GHz un-matched LNA, on-chip UWB filter, RF single-to-differential converter with integrated RF notch filter, 3.1-10.6 GHz LO amplifiers, wideband mixers, and baseband 250 MHz buffers and filters [6]. A block diagram of the front-end is shown in Fig. 6.

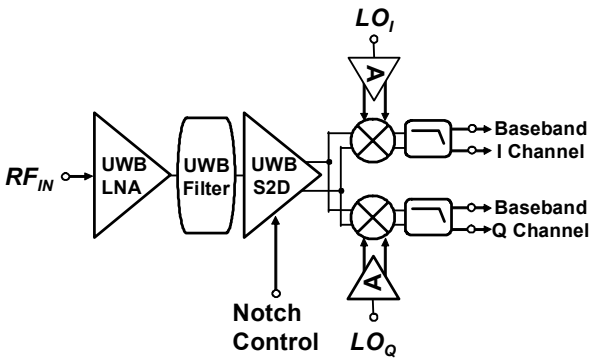

Fig. 6. Block diagram of RF front-end.

Packaged in a QFN housing and mounted on a PCB, the UWB RF front-end achieves low system noise figures (NF) of 3.3-5 dB with a wide-band un-matched LNA. The front-end also provides 39-29 dB of conversion gain. The on-chip filter provides additional high-pass filtering and the single-to-differential converter embeds a switch-able notch filter that is designed to attenuate the 5 GHz ISM bands by 10 dB. The mixers are emitter-degenerated, double-balanced Gilbert mixers. The LO gain stages employ single-to-differential conversion and subsequent amplification. A minimum input of -30 dBm is sufficient to drive these LO gain stages externally. To generate the I/Q LO signals, a commercial PLL is used to generate f_{center}, and a commercial passive wideband 90° phase shifter is used for proper I/Q phase shifting. An on-chip 1st order and off-chip 4th order low pass filter at 250 MHz performs channel selection. The chip has a -30 dBm P_{1dB} and consumes 54 mW.

D. Analog to Digital Converter

Dual 500 MS/s, 5 bit successive approximation register (SAR) ADCs are fabricated in 0.18 μm CMOS [7]. Fig. 7 shows the block diagram of one ADC channel. Six identical SAR converters share a 500 MHz clock and begin a conversion upon reception of the *start* signal. As all critical sampling operations are aligned to rising edges of the same clock, inter-channel skew is minimized. To synchronize outputs to the digital back-end, both ADCs share the same 500 MHz clock and *start* generation block.

While five bits of resolution performs sufficiently close to the infinite-resolution ADC curve for the reception of UWB signals [10], fewer bits are needed for proper reception of pulses under more favorable channel/noise conditions. Thus, the ADC includes functionality to reduce its resolution to any value between 1 and 5 bits. At lower resolutions, the SAR algorithm requires fewer clock cycles (ADC bit resolution + 1) for a conversion.

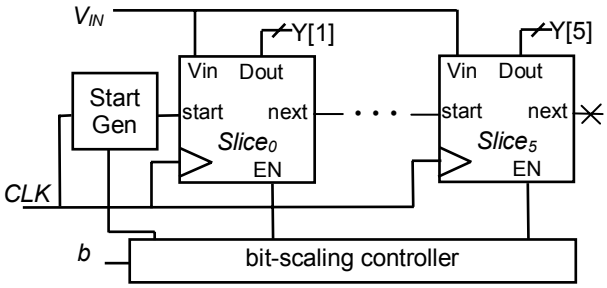

Fig. 7. Block diagram of one ADC channel.

The ADC delivers six samples in parallel from each converter, with a total bus width of 60 signals to the digital back-end. Outputting the samples in parallel reduces the maximum clock speed of the digital back-end and eases the routing of high-speed signals over the PCB. When channels are disabled due to bit-scaling, an on-chip multiplexer tree re-sorts the outputs to present constant speed digital signals to the digital baseband. The ADC also includes the ability to swap the differential inputs of each channel in order to characterize any offsets in the front-end.

Each ADC consumes 7.8 mW of power for its core circuits, excluding I/O. The INL/DNL is better than 0.45/0.4. The SNDR is 20.2 dB at low frequencies and drops to 16 dB before the Nyquist frequency. This corresponds to 2.4 effective numbers of bits at the Nyquist rate [7].

E. Digital Baseband

The digital baseband is implemented in the same process technology as the ADC. It performs the signal detection and demodulation of the data packets [8]. Received signals with high signal to noise ratio (SNR) that are propagated through line-of-sight muti-path channels can be recovered by using a reduced number of bits in the analog to digital converter and using a very simple detection process, since no ISI is present. However, signals with reduced SNR and propagated through non-line-of-sight multi-path channels could still achieve a comparable level of communication reliability by using more bits in the analog to digital converter and exploiting the multi-path in the channel impulse response with the implementation of a RAKE receiver [11] and maximum likelihood sequence estimator (MLSE) to compensate for

the ISI [12]. Therefore, in addition to a matched filter, the RAKE and MLSE are also implemented in the digital baseband to allow recovery of a broader range of signals for different SNR and multi-path environments. With the ability to scale the complexity of the signal processing applied to demodulate the signal, the digital baseband allows for power consumption versus communication reliability tradeoffs. Fig. 8 demonstrates an example of this tradeoff, where receiver sensitivity is worsened by increasing the minimum amplitude threshold that a candidate RAKE finger must exceed to be deemed valid for constructing the impulse response model of a UWB signal that is sent through four different UWB channel models given by the IEEE 802.15.3a working group [1].

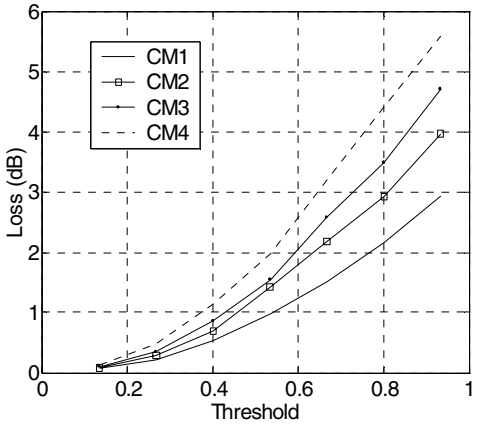

Fig. 8. Losses in the modified RAKE receiver as a function of the normalized threshold and the channel model.

The digital baseband also minimizes the number of signals that are fed back to the RF front-end and ADC. Only the AGC settings are sent back to the RF front-end, and timing synchronization is performed autonomously in the digital baseband.

The inputs to the digital baseband from both channels of the ADCs are two 5-bit vectors of six samples. The ADC chip also provides a clock at 83 MHz to latch this information into the baseband. Fig. 9 shows a high level block diagram of the digital baseband implemented. Packet detection and coarse acquisition are achieved by a serial search for the Gold code in the data packet preamble. The signal is tracked in the payload using both a delay locked loop (DLL) and a Costas loop with independent phase and delay estimation. This eases the transmitter design, and allows it to generate the baseband pulse signal and carrier frequency independently. To process the large amount of data provided by the ADC, extensive parallelization is used in implementing the packet detection and RAKE receiver blocks.

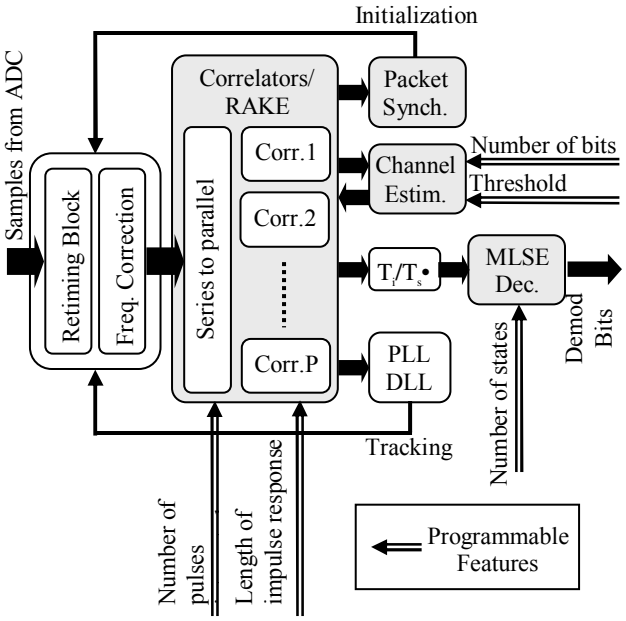

Fig. 9. UWB Digital Baseband Algorithms.

III. MEASUREMENTS

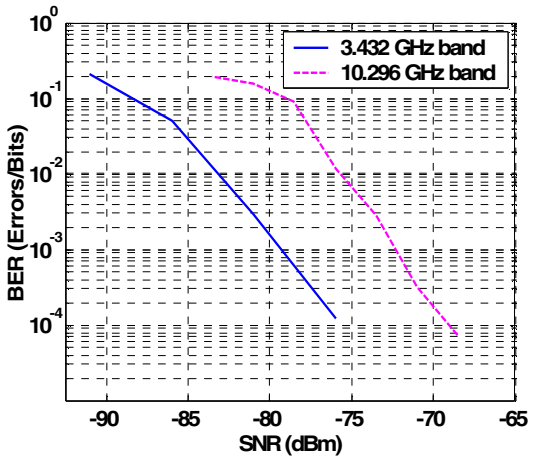

Fig. 10. BER vs. SNR from 3.432 GHz to 10.296 GHz.

The chipset and antenna solution shown in Fig. 4 is assembled. Fig. 10 shows the BER plots of acquired packets. A 6 dB difference in link margin is observed between the lowest and highest frequency channels. This is due to increased front-end NF at higher frequencies, as well as reduced front-end conversion gain [6] which causes the baseband gain stages to contribute more noise at the higher frequency channels. Fig. 11 shows the bit-scaling effects on BER. 4 dB of margin in the link budget can be recovered when the ADC resolution is scaled from 1 to 5 bits. A power savings of 40% in the ADC can be observed when it operates in the 1-bit mode. For a 10,000

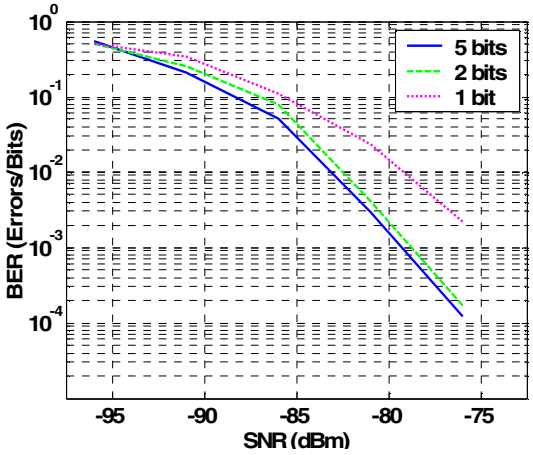

Fig. 11. BER vs. SNR at 3.432 GHz

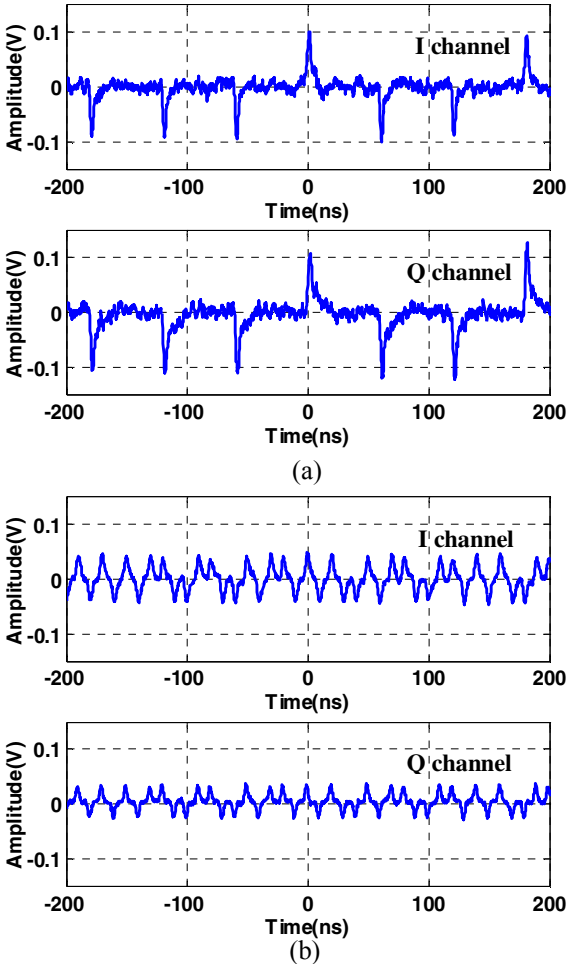

Fig. 12. RX baseband signals. (a) Preamble. (b) Payload.

packet trial, 80% of the packets are acquired in a high SNR environment. Fig. 12 shows the received I and Q analog baseband signals during wired testing.

IV. Conclusions

A complete UWB chipset receiver has been assembled and verified for functionality. At a -80 dBm sensitivity, a BER of 10^{-3} is achieved with the chipset. Bit-scaling effects on SNR in [10] are also verified with this chipset, and allow the system to recover 4 dB of margin in the link budget from the 1-bit to 5-bit mode. In a high SNR environment, an 80% packet acquisition rate has been achieved. With antennas, a 6 m wireless link has been established.

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