A -32dBm Sensitivity RF Power Harvester in 130nm CMOS

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***Abstract* — This paper discusses a RF power harvester optimized for sensitivity and therefore wireless range, for applications requiring intermittent communication. The RF power harvester produces a 1V output at -32dBm sensitivity and 915MHz. This is achieved using a CMOS rectifier operating in the subthreshold region and an off-chip impedance matching network for boosting the received voltage. Equations predicting the rectifier performance are presented and verified through measurements of multiple rectifiers using different transistors in a 130nm CMOS process.**

***Index Terms* — Energy harvesting, Rectifiers, RFID, Sensitivity, Voltage boosting.**

I. Introduction

In battery-less passively powered systems such as radio frequency identification (RFID) and some wireless sensor networks (WSN), nodes must scavenge energy from an external source such as propagating radio waves, solar radiation, thermal energy or kinetic energy. RF power harvesting using a CMOS rectifier is one of the most popular power harvesting methods, which converts an incoming RF signal into a DC voltage suitable for powering the node for brief periods of time [1].

Previous rectifiers focused on maximizing power conversion efficiency and output power rather than sensitivity [1-3]. The power conversion efficiency and output power are important when the system is continuously operating off harvested power. However, in some applications where the entire system does not need to be on all the time, the sensitivity is more important as it defines the maximum range. If output power consumption is minimized while charging and a long charging time is acceptable, the sensitivity of the power harvester can be dramatically increased.

Fig. 1 shows the sensitivity versus the harvested power of previous work from 2003 to 2010 at 900MHz. In this figure, the output power is roughly proportional to the sensitivity, as shown by the fit line. In this paper, a power harvester is demonstrated with –32dBm sensitivity at 915MHz. This sensitivity is sufficient to power a device at a distance of 66m with a 4W EIRP source.

In order for the rectifier to work with very low input power, all transistors of the rectifier should operate in the subthreshold region. In subthreshold, the calculation of output voltage of the rectifier is different from that in the saturation region; therefore, new equations using

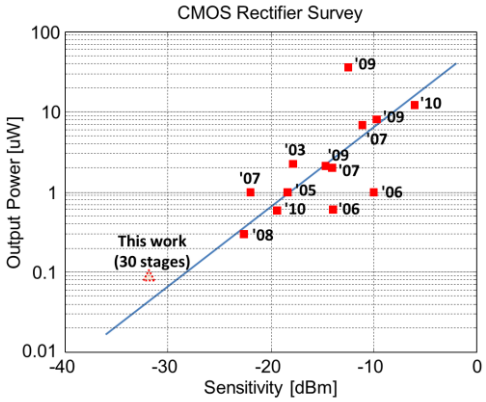

Fig. 1. Sensitivity vs. output power of 900MHz CMOS Rectifier

subthreshold transistors are derived in this paper. A voltage boosting circuit is implemented off-chip to further increase the sensitivity. An impedance matching network is the best for boosting voltage if there is no power loss other than the rectifier [3-5]. This work provides a method of implementing this matching network while taking into account lossy components.

Section II will analyze the CMOS rectifier in the subthreshold region. Section III will introduce the voltage boosting circuit between the antenna and the rectifier. Section IV will present measurement results, and Section V will discuss a CMOS rectifier design strategy. Finally, section VI will conclude the paper.

II. Sub-Threshold CMOS Rectifier

Fig. 2 shows a schematic of the Dickson multiplier with diode-connected transistors [1-6]. The output voltage of the N stage CMOS rectifier, V_{OUT} is:

$$V_{OUT} = 2N \cdot (V_A - V_{DROP}) \quad (1)$$

where V_A is the input voltage amplitude of the CMOS rectifier and V_{DROP} is the voltage drop across the diode-connected FET. An accurate equation for V_{DROP} is presented in [6] when all transistors operate in the saturation region. In this work, V_{OUT} and V_{DROP} are calculated provided that all transistors operate in the subthreshold region. Let us consider FET1 in Fig. 2. The drain current of FET1, I_D, in subthreshold is [7]:

$$I_D = I_S \cdot e^{\frac{V_{GS}-V_{TH}}{nV_T}} \left(1 - e^{-\frac{V_{DS}}{V_T}}\right) \quad (2)$$

where I_S is the zero-bias current for the given device, V_{GS} is the gate-source voltage, V_{DS} is the drain-source voltage,

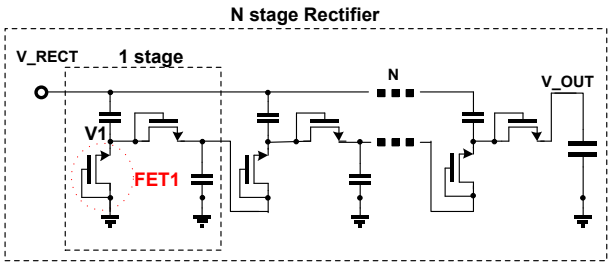

Fig. 2. Schematic of CMOS rectifier

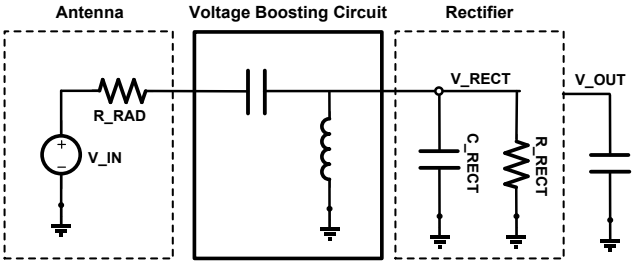

Fig. 3. Antenna, voltage boosting circuit and rectifier

V_{TH} is the threshold voltage, n is the subthreshold slope, and V_T is the thermal voltage ≈ 26mV.

In steady-state, the average charge through FET1 for one cycle should be zero. If we assume n is 1 and use equation (2),

$$Q = \int_0^T I_D dt = \int_0^T I_S \cdot e^{\frac{-V_{TH}}{V_T}} \left(1 - e^{-\frac{V_1}{V_T}}\right) dt = 0 \quad (3)$$

where T is the period of the input voltage and V_1 is the source voltage of FET1 in Fig. 2.

If V_1 is $V_A \sin(\omega t) + V_A - V_{DROP}$ [6], then V_{DROP} can be derived from equation (3).

$$V_{DROP} = V_A - V_T \cdot ln\left(I_0\left({}^{V_A}/_{V_T}\right)\right) \quad (4)$$

where I_0 is the zero-th order modified Bessel function of the first kind.

If this V_{DROP} is applied to equation (1),

$$V_{OUT} = 2N \cdot V_T \cdot ln\left(I_0\left({}^{V_A}/_{V_T}\right)\right) \quad (5)$$

$$V_{OUT} \approx \frac{N \cdot {V_A}^2}{2V_T} \qquad if\ V_A \ll V_T \quad (6)$$

According to equation (5), transistor size and threshold voltage have no effect on V_{OUT}. They only effect the charging time and the input resistance of the rectifier.

If a cross-coupled rectifier is applied with differential input, $\pm V_A/2$, then

$$V_{OUT} = 2N \cdot V_T \cdot ln\left(I_0\left({}^{V_A}/_{V_T}\right)/I_0\left({}^{V_A}/_{2V_T}\right)\right) \quad (7)$$

Comparing equations (5) and (7), equation (5) is always greater than equation (7), meaning the single-ended rectifier is always better than the cross-coupled rectifier in the subthreshold region.

Power consumption and effective input resistance of the rectifier, R_{RECT} is:

$$Power = 2N \int_0^T V_1 \cdot I_D dt = 2NV_A I_S e^{\frac{-V_{TH}}{V_T}} \frac{I_1\left(\frac{V_A}{V_T}\right)}{I_0\left(\frac{V_A}{V_T}\right)} \quad (8)$$

$$R_{RECT} = \frac{{V_A}^2}{2 \cdot Power} = \frac{V_A e^{\frac{V_{TH}}{V_T}}}{4NI_S} \frac{I_0\left(\frac{V_A}{V_T}\right)}{I_1\left(\frac{V_A}{V_T}\right)} \quad (9)$$

Finally, input capacitance of the rectifier is the sum of the parasitic capacitance of the FETs, storage capacitors, input pad, and PCB. This depends on transistor size, storage capacitor size, and the number of stages in the rectifier.

III. Voltage Boosting Circuit

Fig. 3 shows a simplified schematic of the RF power harvester, where R_{RAD} is the antenna impedance. To increase the sensitivity of the system, a voltage boosting circuit between the antenna and the rectifier is proposed.

In the ideal case that the voltage boosting circuit is lossless, an impedance matching network results in the highest sensitivity, since it can deliver the maximum voltage V_{RECT} and power to the rectifier. For the ideal lossless matching network,

$$V_{RECT} = \sqrt{\frac{R_{RECT}}{R_{RAD}}} \cdot \frac{V_{IN}}{2} \quad (10)$$

In realistic environments, the matching network is not lossless and limited by finite Q of e.g. inductors. Furthermore, if the input resistance of the rectifier is much larger than R_{RAD}, which is typically the case, then it becomes more difficult to implement the matching network with low-Q components. Furthermore, according to the Bode-Fano limit [5],[8], the bandwidth of the ideal matching network is limited by

$$BW \leq -\frac{\pi}{R_{RECT} \cdot C_{RECT} \cdot ln(|\Gamma|)} \quad (11)$$

where Γ is the reflection coefficient of the matching network. For a reasonable value of $\Gamma = 0.5$ with $R_{RECT} = 1M\Omega$ and $C_{RECT} = 1pF$, BW is less than 500kHz, which is also not easy to implement with low-Q devices.

Fig. 4 shows the proposed voltage boosting circuit with a parallel inductor, where R_{LP} is the parasitic resistance of the inductor due to finite Q. To minimize the loss in the voltage boosting circuit, only one inductor is used. The equation of V_{RECT} in the lossy matching network is still given by (10) if R_{RECT} is replaced with $R_{RECT} /\!/ R_{LP}$. In this work, high-Q air core inductors from Coilcraft Inc. are used to increase R_{LP}.

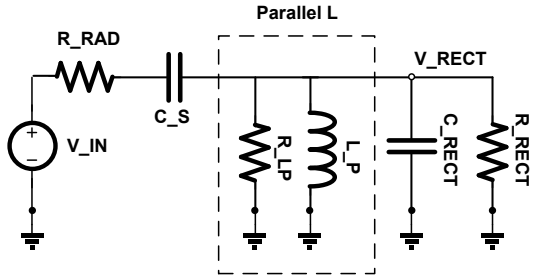

Fig. 4. Voltage boosting circuit with parallel L

IV. Experimental Results

The custom IC is fabricated in an IBM 130nm CMOS process. Fig. 5 shows the die photo of the fabricated chip. The total size is 1mm x 1mm, including all rectifier implementations. CMOS rectifiers with several types of transistors and different number of stages are implemented. Table 1 summarizes the measurement results of ZVT (zero threshold voltage transistor), ZVTDG (zero threshold voltage transistor with thick oxide), LVT (low threshold voltage transistor), NFET (normal threshold voltage transistor) and NFET33 (3.3V I/O transistor with thick oxide) rectifiers with different numbers of stages. The input impedance at -25dBm input power, sensitivity for 1V V_{OUT}, and charging time (10% to 90% V_{OUT}) with the input at the sensitivity level for a 1nF load capacitor are provided with and without a matching network.

R_{RECT} and C_{RECT} are calculated based on the measured impedance value taking into account a 1.6nH inductance from the bondwire and PCB. The 70-stage LVT rectifier has the lowest R_{RECT}, and the 10-stage NFET33 rectifier has the highest R_{RECT}, which is expected given that higher the power loss in the rectifier results in lower input resistance. C_{RECT} is similar for all types of transistors, but

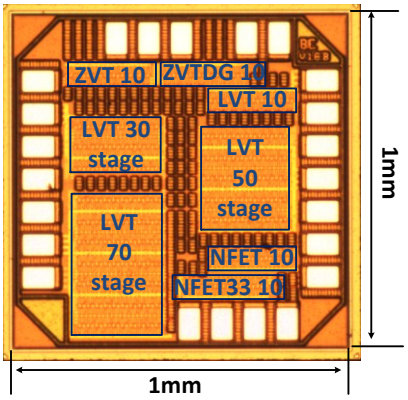

Fig. 5. Die photo

increases as the number of stages increases.

The sensitivity of a 10-stage rectifier without a matching network is around -14dBm, independent of the transistor type, which matches well with equation (5). Sensitivity increases as the number of stages increases. The sensitivity with a matching network is a function of both the number of stages and the transistor type, because the voltage boosting depends on the input impedance of the rectifier, and the low accuracy of the off-chip matching networks at 915MHz. The highest sensitivity of -32.1dBm is achieved with 50 stages, using LVT transistors and a matching network.

The charging time without voltage boosting increases with increasing V_{TH} and number of stages due to the small I_D and large capacitance. Charging time also increases with the size of the final storage capacitor (1nF in our measurements). Fig. 6 shows the transient response of the 30-stage LVT rectifier with off-chip matching network, as the input power is varied. Charging time increases as the input power increases because V_{OUT} increases faster than

TABLE I
MEASUREMENT RESULTS FOR EACH CMOS RECTIFIER

		ZVT 10stages	ZVTDG 10stages	LVT 10stages	NFET 10stages	NFET33 10stages	LVT 30stages	LVT 50stages	LVT 70stages
without Voltage Boosting Circuit	Impedance	2.2-j39	1-j43	0.8-j31	0.8-j36	0.7-j50	1.2-j34	1.2-j24	1.3-j13
	R_{RECT}(kΩ)	1.06	2.73	2.02	2.55	5.01	1.56	0.92	0.38
	C_{RECT}(pF)	3.60	3.33	4.33	3.85	2.94	4.02	5.23	7.81
	1V V_{OUT} Sensitivity	-14.0 dBm	-14.5 dBm	-13.6 dBm	-13.9 dBm	-13.2 dBm	-19.7 dBm	-21.5 dBm	-22.3 dBm
	Charging Time (1nF)	0.6ms	7.5ms	42ms	32s	285s	98ms	159ms	242ms
with Voltage Boosting Circuit	Impedance	21-j42	37+j10	19.6-j44	58-j27	110-j0.3	51-j6.5	40-j3	76-j2
	1V V_{OUT} Sensitivity	-22.1 dBm	-27.1 dBm	-22.9 dBm	-22.6 dBm	-25.6 dBm	-31.7 dBm	-32.1 dBm	-31.8 dBm
	Charging Time (1nF)	2.2ms	1.4ms	4.8s	99s	370s	5.6ms	155ms	109ms

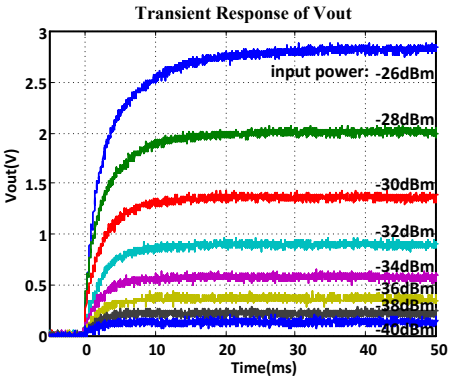

Fig. 6. Transient response of 30-stages LVT rectifier

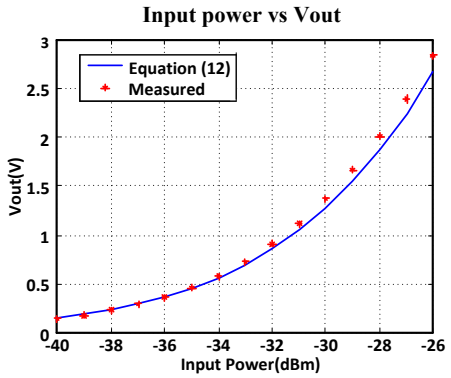

Fig. 7. Equation (12) vs. measurement of 30-stages LVT rectifier

I_D. When voltage boosting is added, the charging time varies greatly due to the interaction between the matching network and the input impedance of the rectifier.

Fig. 7 shows V_{OUT} of the 30-stage LVT rectifier with a matching network predicted from equation (12) and measurements. There is a slight discrepancy when V_{OUT} is large, because the transistors are not in the subthreshold region anymore.

V. Design Strategy

The final equation for V_{OUT} with a matching network is:

$$V_{OUT} = 2N \cdot V_T \cdot ln\left(I_0\left(\frac{1}{2}\sqrt{\frac{R_{LP} /\!/ R_{RECT}}{R_{RAD}}}\frac{V_{IN}}{V_T} \right) \right) \quad (12)$$

For maximum sensitivity, large N, large R_{RECT} and small C_{RECT} are preferred, since R_{LP} is inversely proportional to C_{RECT} ($R_{LP} = \omega L_P Q_{LP}$, and L_P is inversely proportional to C_{RECT}). However, R_{LP} sets an upper limit on V_{OUT}, beyond which increasing R_{RECT} or reducing C_{RECT} is not helpful.

There are four design variables to consider for the CMOS rectifier. These are the number of stages, transistor type, transistor size and storage capacitor size. These affect V_{OUT}, R_{RECT}, C_{RECT}, and the charging time. The number of stages decreases R_{RECT}, and increases C_{RECT} linearly. The number of stages also linearly increases V_{OUT}. Therefore, there is an optimum N depending on the limit of R_{LP}. Increasing transistor size decreases R_{RECT}, and increases C_{RECT} with linear slopes. Higher V_{TH} of the transistor increases R_{RECT} exponentially, but has no effect on C_{RECT}. Therefore, if the charging time is not important, smaller transistor size and higher V_{TH} are preferred. The size of the capacitor increases C_{RECT} linearly but has no effect on R_{RECT} so that a smaller capacitance is preferred. However, it should be relatively large compared to parasitic capacitance.

VI. Conclusion

In this paper, we proposed a CMOS rectifier operating in subthreshold for maximum sensitivity. A custom IC is fabricated in a 130nm CMOS technology, and -32dBm sensitivity of the rectifier at 915MHz is measured. CMOS rectifiers with several types of transistors and numbers of stages are compared to verify the equations, and a design strategy is provided.

Acknowledgement

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