All-Digital Synthesizable UWB Transmitter Architectures

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UWB Radios – Recent Pubs

Observations:
- TX E/pulse independent of pulse rate
- TX E/pulse 10x lower than RX E/pulse in general

Sources: JSSC, ISSCC, CICC, ISCAS, VLSI, TMTT
UWB Transmitter FOM

- UWB transmitters have benefited from process scaling

**Graphs:**

- Transmitter Energy/pulse vs. Pulse Rate [Hz]
- Transmitter Energy/pulse vs. Process node [nm]

**Note:**

TX E/b dominated by digital power
Motivation for Synthesizable Transmitter

- Standard cell performance characterized already
- No custom
- Short time-to-market
- Portable between process technologies
- Powerful design tools available
- Transmitter in verilog
- Technology Library
- Synthesis Place-and-route Tools
- Transmitter on silicon
Transmitter Architecture

Modulator (e.g. PPM) → Pulse Generator

DATA
CLK

Pulse Trigger
Modulation Control
Bandwidth Control
Center Frequency Control

RF OUT

Data rate/Bandwidth Center frequency are digitally controlled
No analog bias current

Digital logic gates only
Two Pulse Generators

Transmitter Architecture

- Modulator (e.g. PPM)
  - Modulation Control
- System Controller
  - Bandwidth Control
  - Center Frequency Control
- Pulse Generator
  - Pulse Trigger

Delay Line Pulse Generator

Ring Osc. Pulse Generator
Delay Line Pulse Generator

- Delay line
- Mask Register (ANDs)
- Edge Combiner (XORs)
- RF_OUT

- Determines center frequency
- Determines bandwidth

Generate pulse without LO
Tunable Delay Cell

\[ \Delta t(n) \propto \frac{C_1 \times N_{\text{tot}}}{n} + C_2 \]

- \( \Delta t(n) \): the number of buffers
- \( n \): the number of buffers turned on
- \( N_{\text{tot}}, C_1, C_2 \): physical parameters
Mask Register

Delay Line

Selects edges to be combined

Bandwidth tuning

Mask bits

ANDs

Mask bits 1 1 1 1 0 0

Bandwidth tuning

RF_OUT

Bandwidth tuning 1 1 1 1 1 1 1
Edge Combiner

Mask Register

XORs Tree

Incoming edges from mask register toggle the output signal in order

Balanced XOR tree

Incoming edges

Combined output

To Pad
Calibration with Delay Line

Make a loop with a part of delay line

Measure the path delay in the loop
Calibration with Delay Line

Make a loop including the next delay cell

Measure the path delay in the next loop
Calibration with Delay Line

Each edge calibrated

Measured delay difference ($\Delta t$) is determined by

$\Delta t_2 + \text{path}(\text{MR}, \text{EC}) - \text{path}(\text{MR}, \text{EC})$

Tunable value + Inherent mismatch by synthesis/PAR

Each edge calibrated
Two Pulse Generators

Transmitter Architecture

- Modulator (e.g. PPM)
- System Controller
  - Pulse Trigger
  - Modulation Control
  - Bandwidth Control
  - Center Frequency Control

Pulse Generator

- Delay Line Pulse Generator
- Ring Osc. Pulse Generator
Ring Oscillator Pulse Generator

Coarse / Fine control of frequency
Bandwidth tuned with counter

Gating Oscillating signal
Tuning with Ring Oscillator

- Fine tune with delay cell
- Coarse tune with MUX
- Cycle period (ns)
- Short path
- Long path
- Tunable range

Simpler calibration
FPGA Prototype

Transmitter Architecture

Modulator (e.g. PPM) → Pulse Generator

Modulation Control

Bandwidth Control

Center Frequency Control

System Controller

Pulse Trigger

Delay cells are implemented with TBUFs in FPGA

Other logic circuits are mapped to configurable logic blocks (CLBs)

Xilinx Virtex-II Pro FPGA Development board

Synthesis & PAR by design tools
Delay Line PG Measurement

Pulse / spectrum generated by delay line PG
Ring Osc. PG Measurement

Pulse / spectrum generated by ring oscillator PG

![Graph showing pulse and spectrum](image)

- Voltage (V) scale: 0, 1, 2
- Time (ns) scale: 0, 20, 40
- Frequency (MHz) scale: 100, 200, 300
- Decibel (dB) scale: -30, -40, -50, -60

FFT(ideal square)
Calibration in FPGA prototype

Before/After calibration

With control code word, each cell is calibrated to have same delay

![Graph showing voltage (V) over time (ns) before and after calibration, with a clear reduction in peak amplitudes after calibration.]
Calibration in FPGA prototype

Before/After calibration

With control code word, each cell is calibrated to have same delay

![Graph showing before and after calibration with dB scale and MHz range](image)
Conclusions

All-digital synthesizable transmitter
  No custom circuit / layout
  Mismatch overcome by calibration

Delay line PG vs. Ring osc PG
  Flexibility vs. Simplicity

FPGA prototype
  Works at scaled frequency