All-Digital Synthesizable UWB Transmitter Architectures

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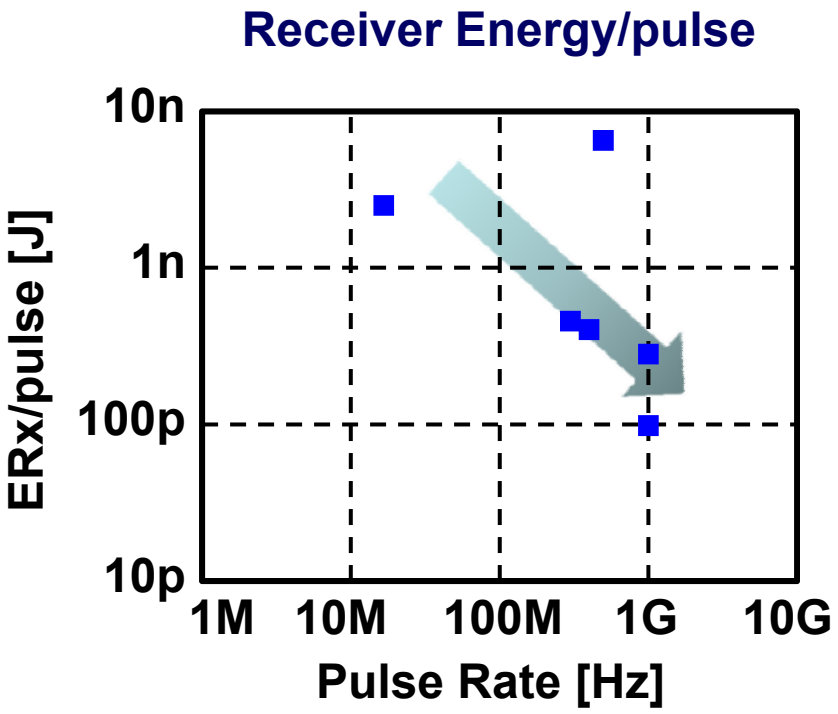
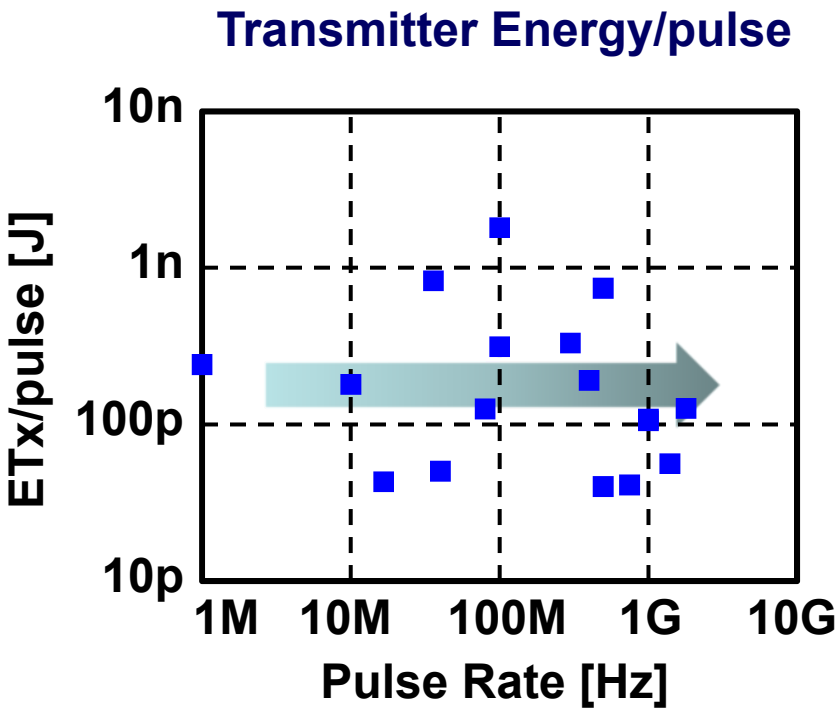
ICUWB 2008

UWB Radios – Recent Pubs



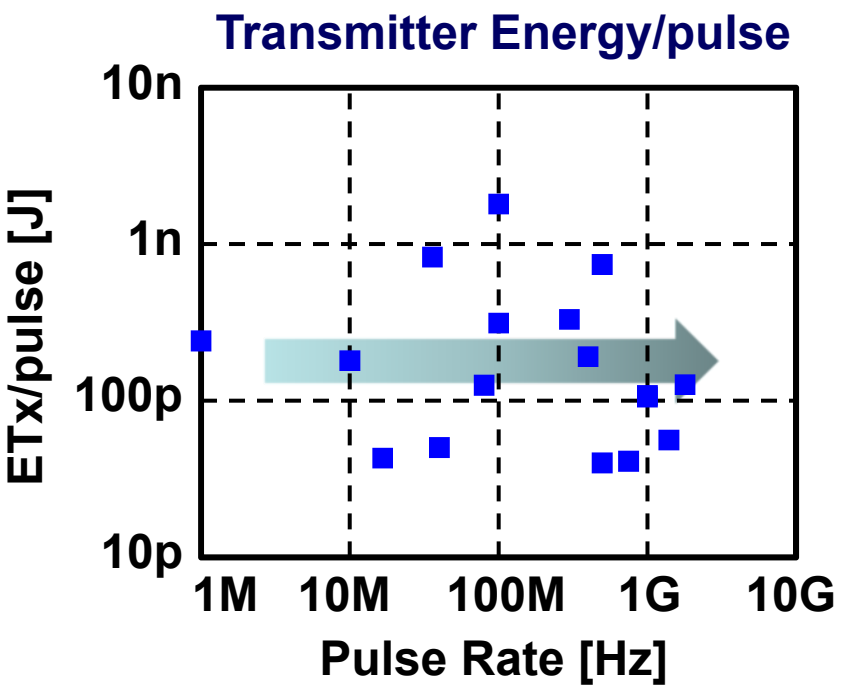


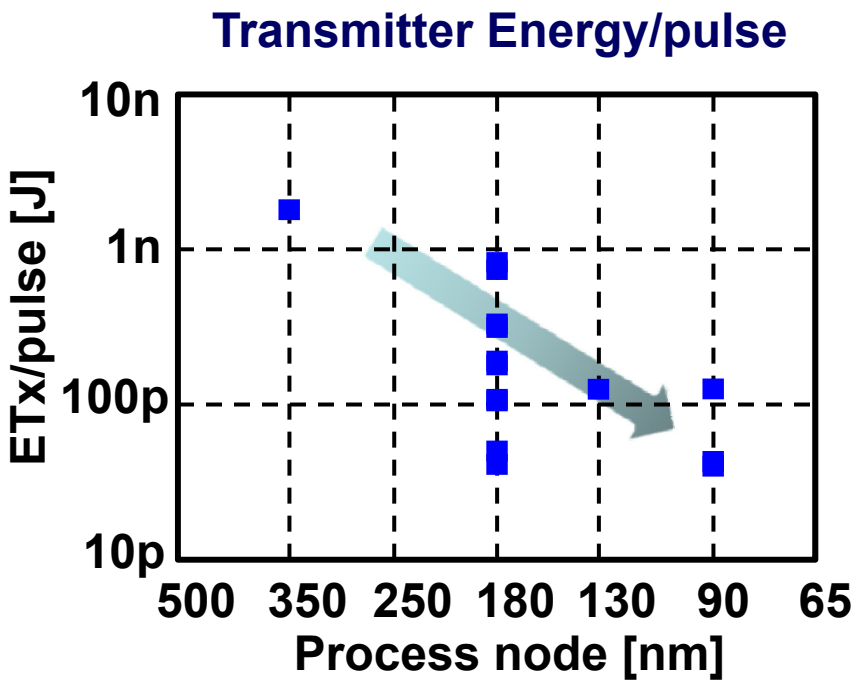
Observations:
- TX E/pulse independent of pulse rate
- TX E/pulse 10x lower than RX E/pulse in general

Sources: JSSC, ISSCC, CICC, ISCAS, VLSI, TMTT

UWB Transmitter FOM

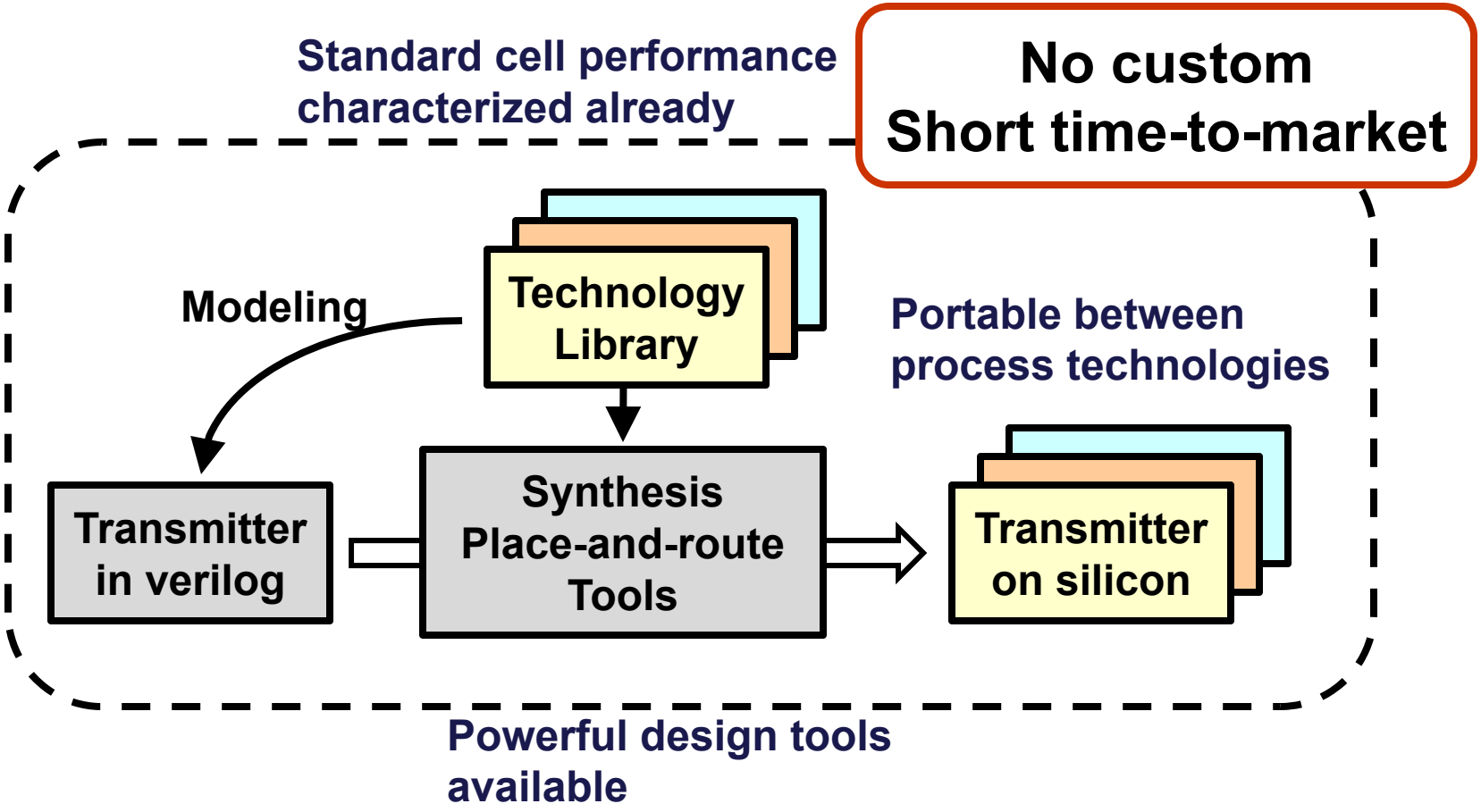
- UWB transmitters have benefited from process scaling



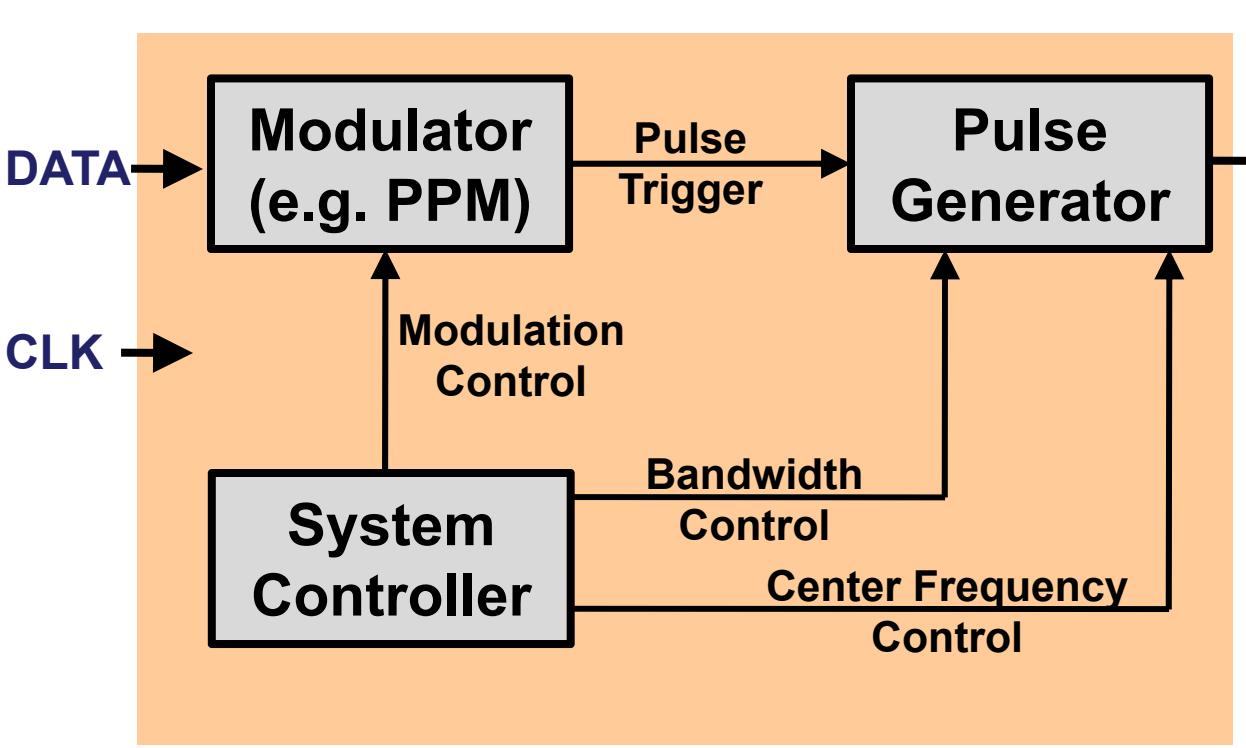


TX E/b dominated by digital power

Motivation for Synthesizable Transmitter



Transmitter Architecture

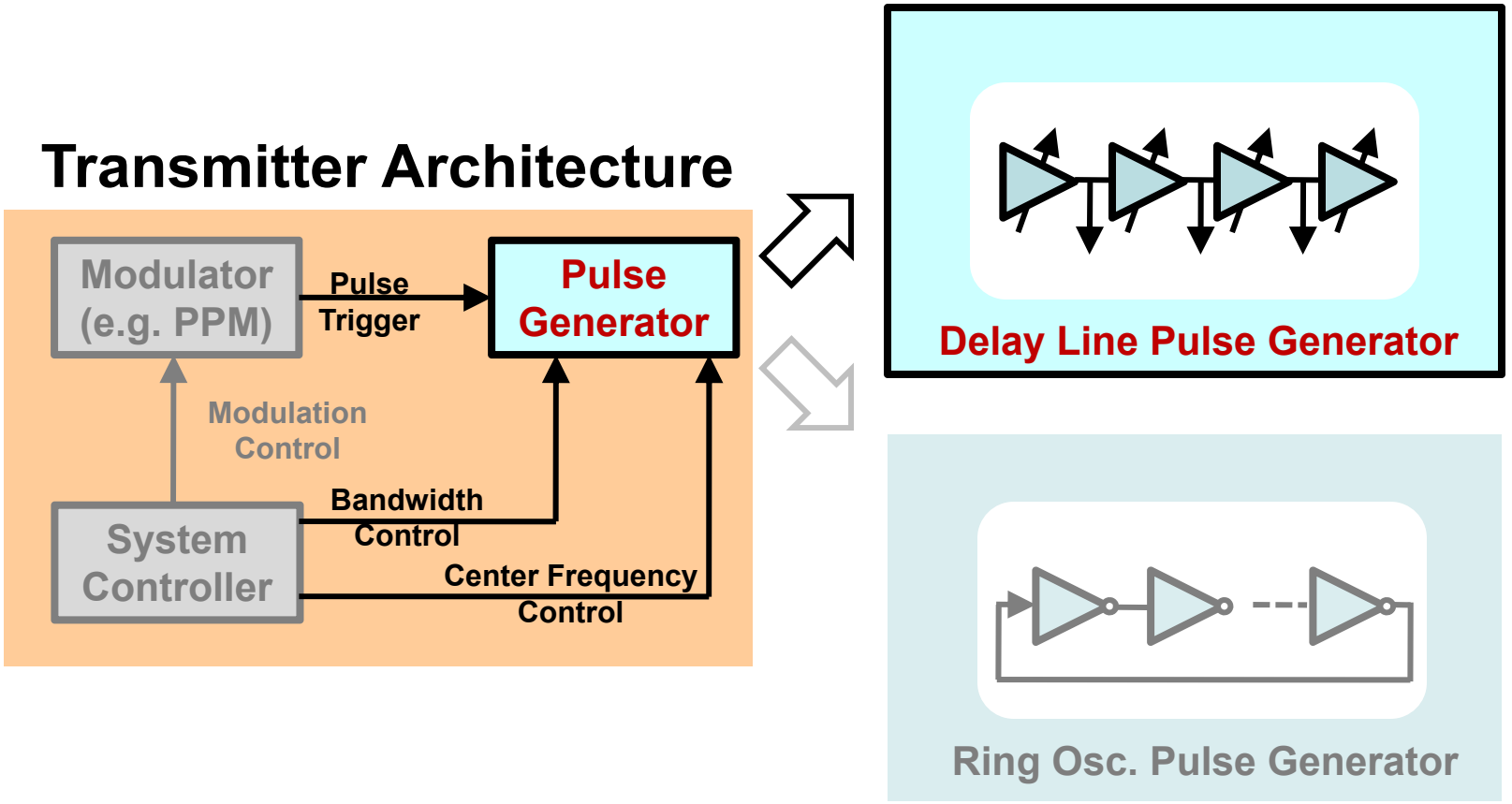


Data rate/Bandwidth Center frequency are digitally controlled

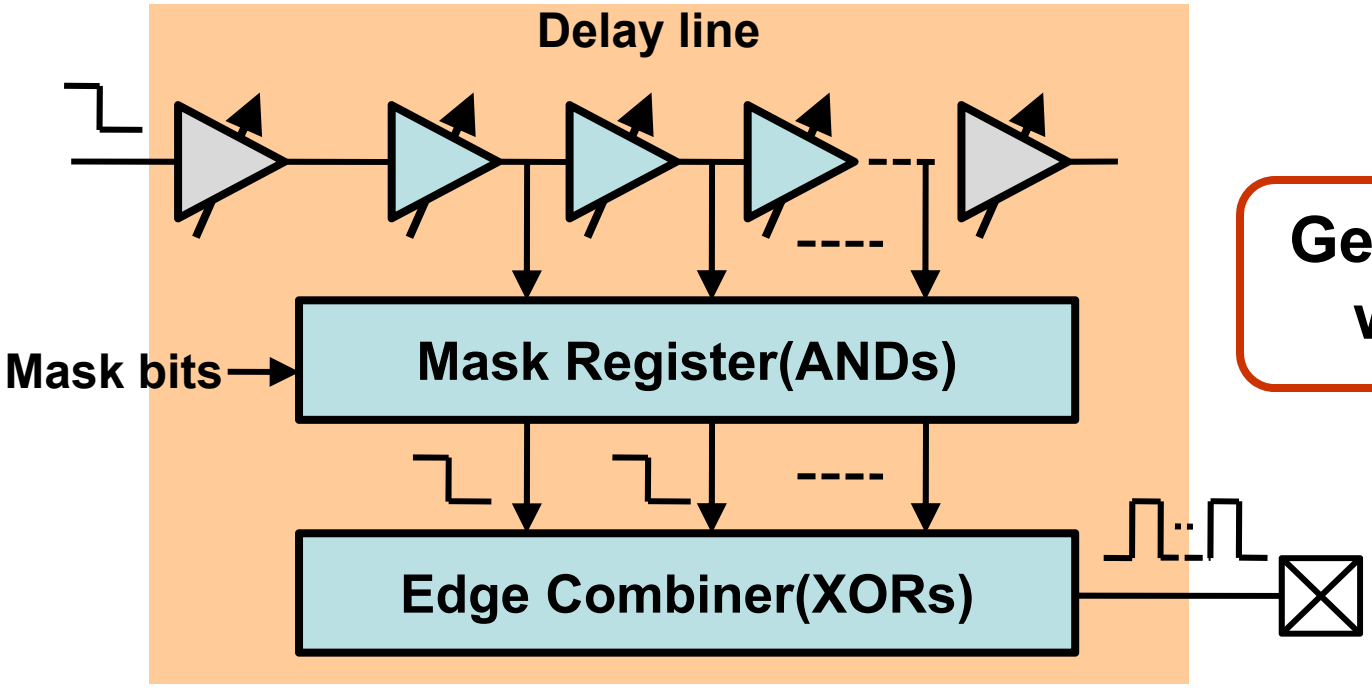
No analog bias current

Digital logic gates only

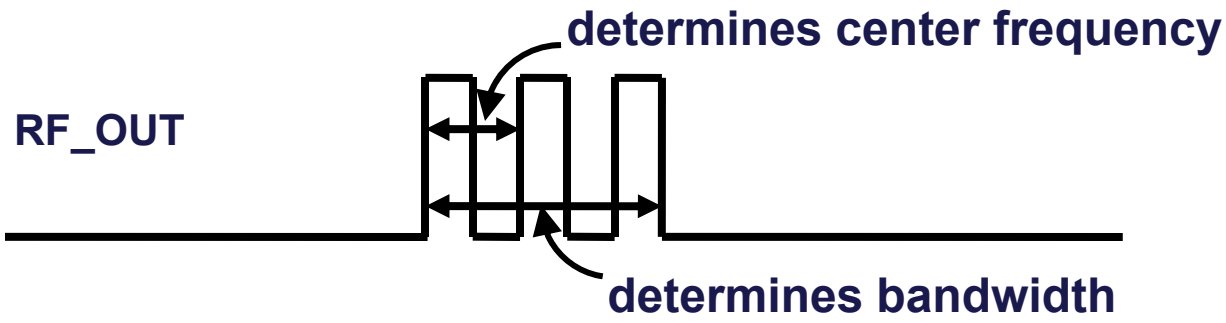
Two Pulse Generators



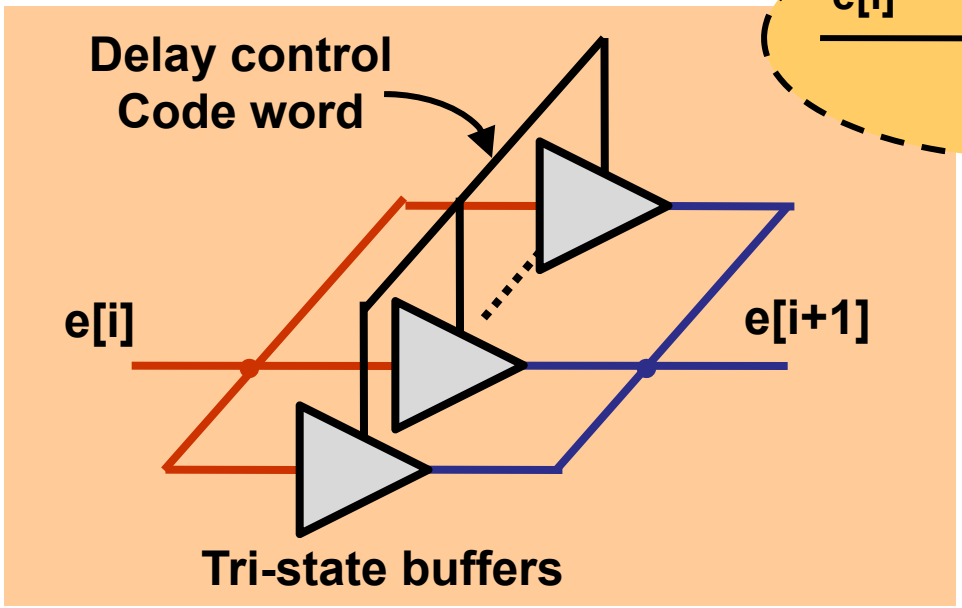
Delay Line Pulse Generator

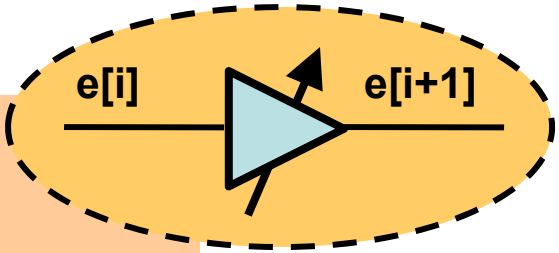


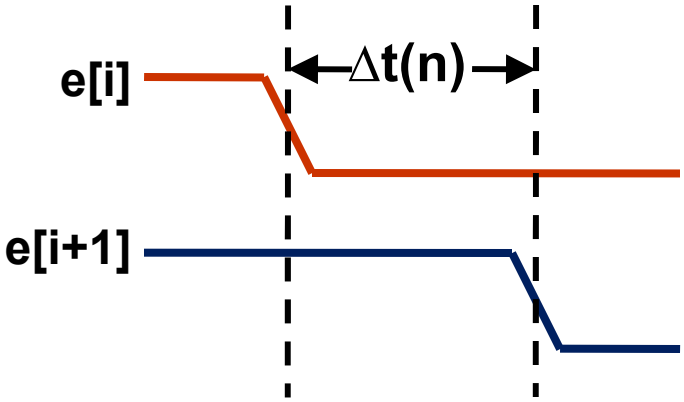
Generate pulse without LO



Tunable Delay Cell







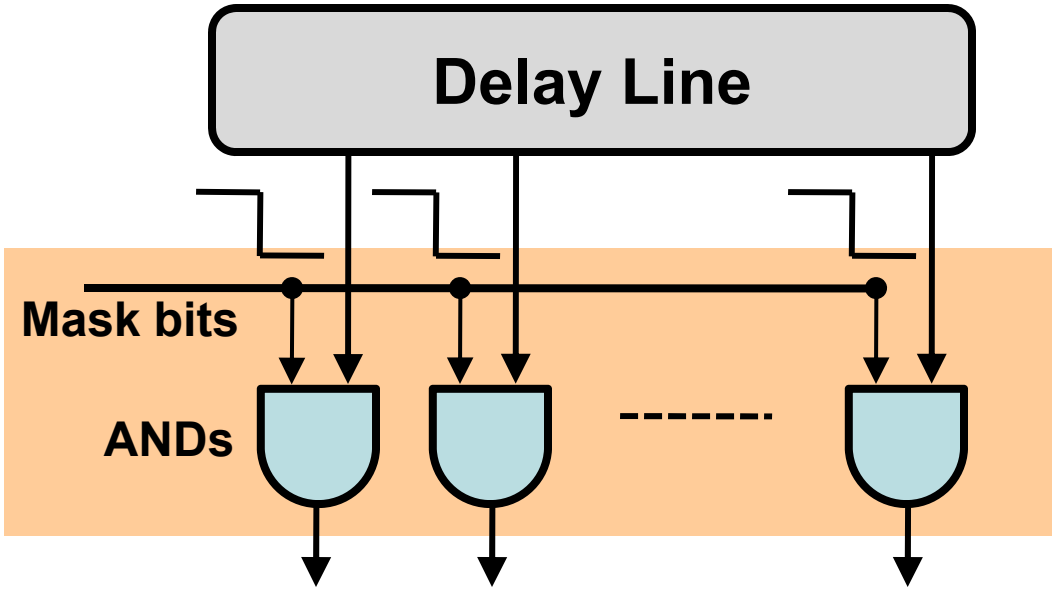
Digitally tunable delay

Simplified delay model

$$\Delta t(n) \propto \frac{C_1 \times N_{tot}}{n} + C_2$$

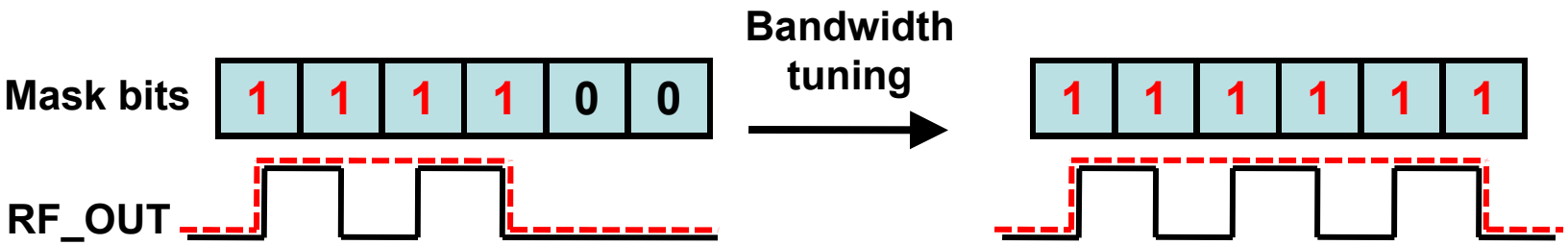
N_{tot} : the number of buffers
n : the number of buffers turned on
C_1, C_2 : physical parameters

Mask Register

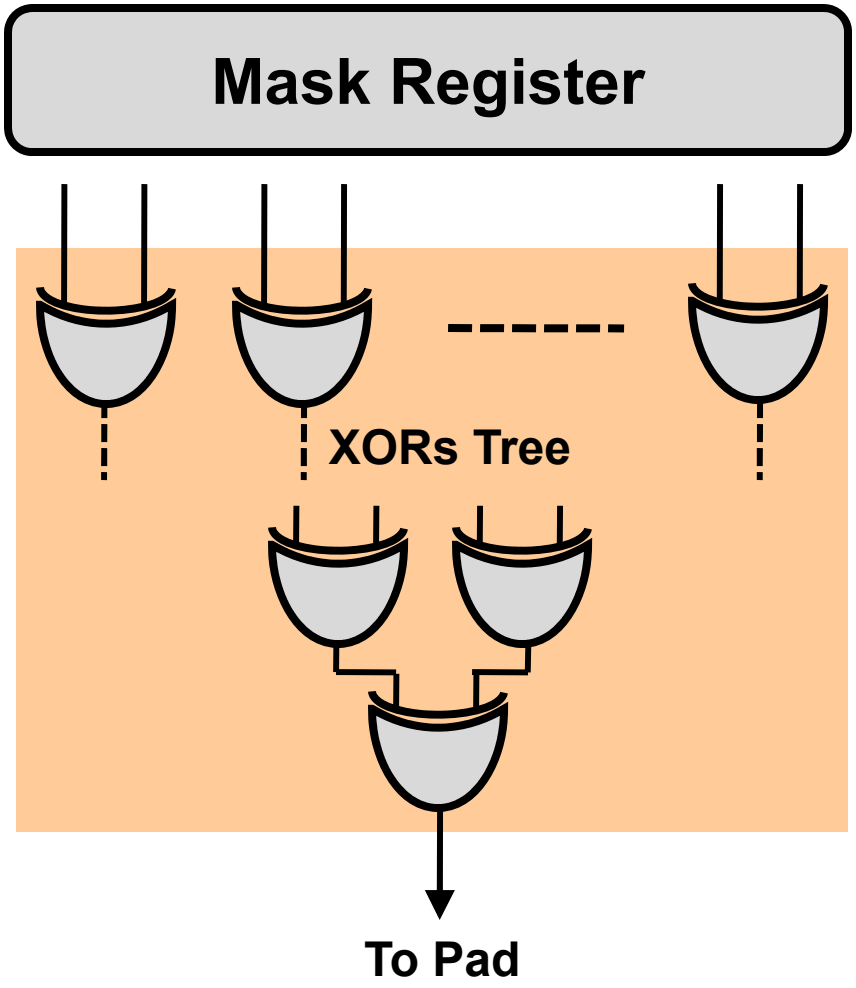


Selects edges to be combined

Bandwidth tuning

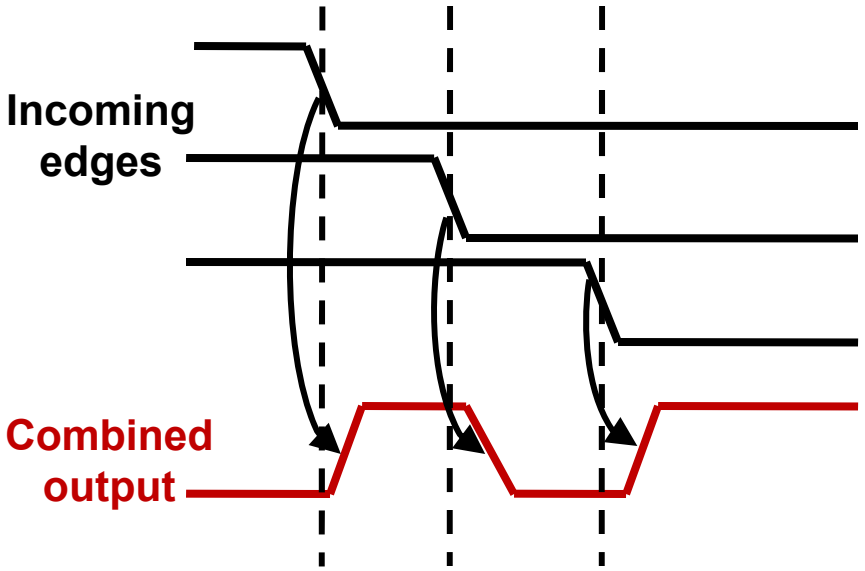


Edge Combiner

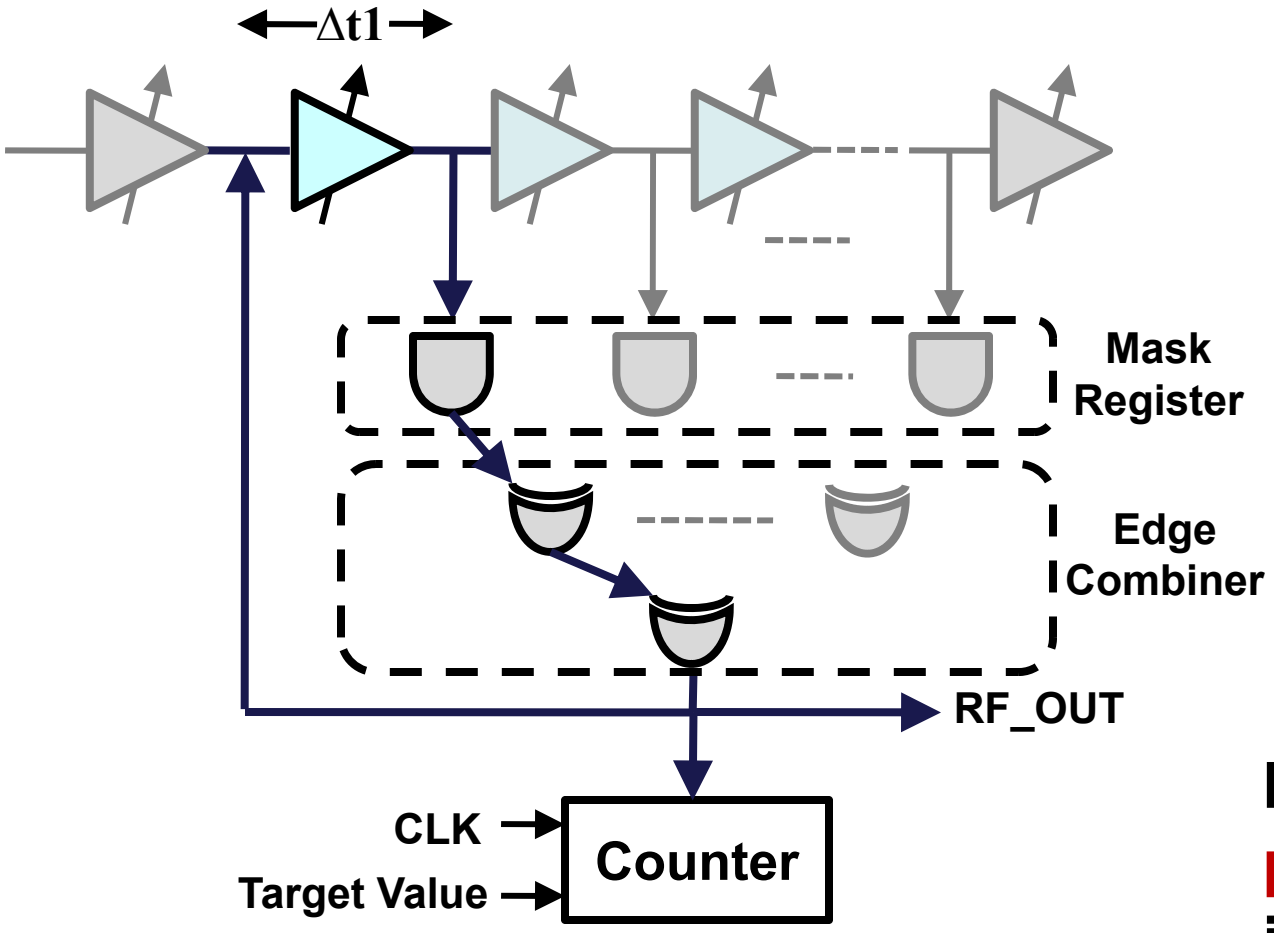


Balanced XOR tree

Incoming edges from mask register toggle the output signal in order



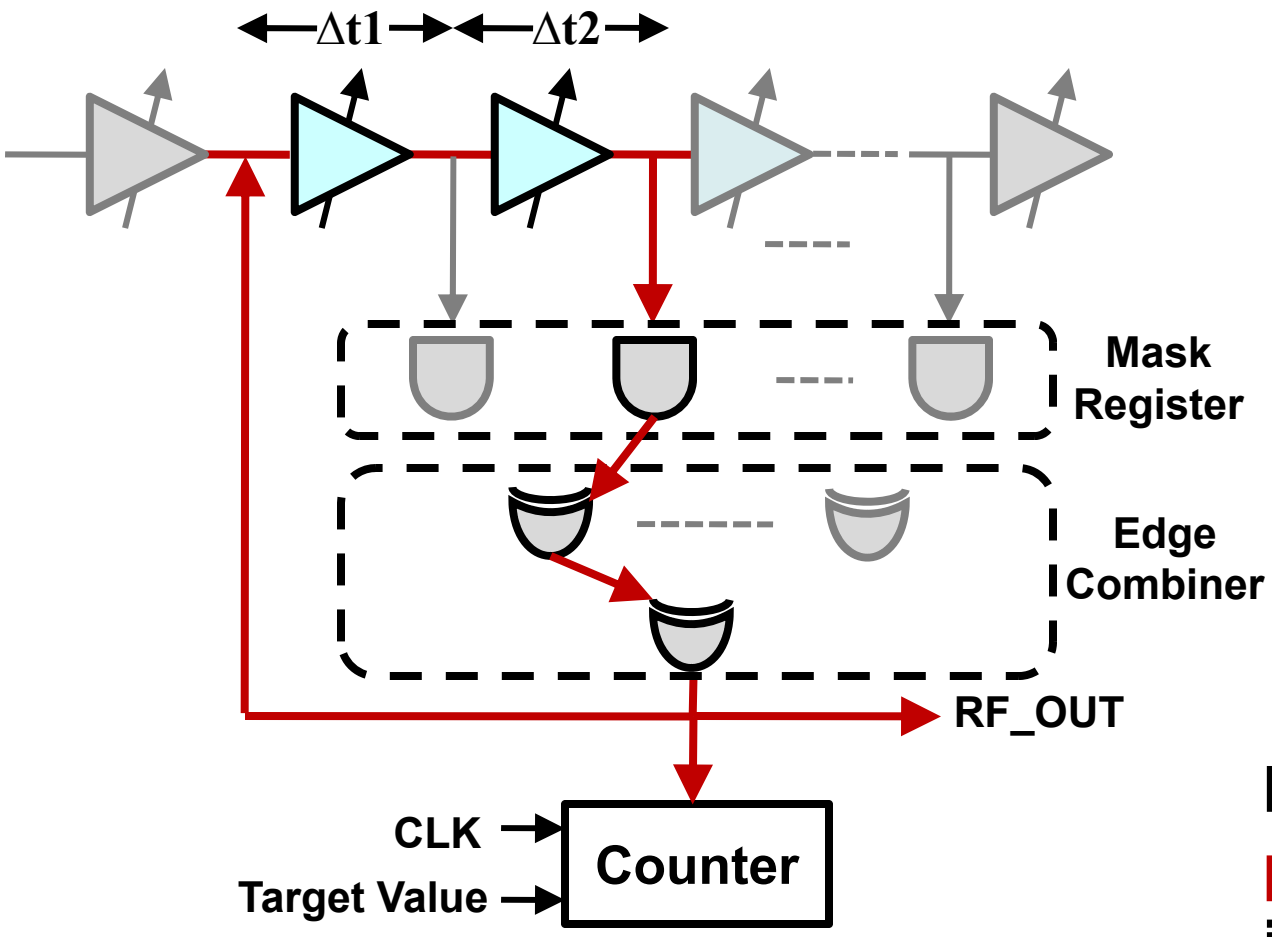
Calibration with Delay Line



Make a loop with a part of delay line

Measure the path delay in the loop

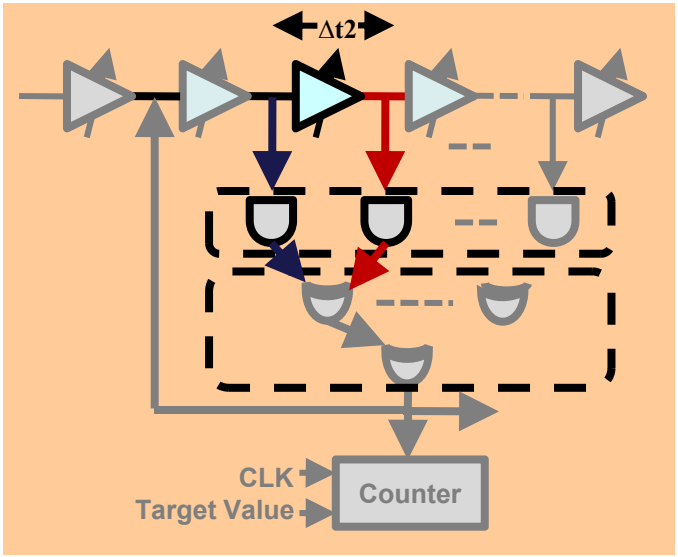
Calibration with Delay Line

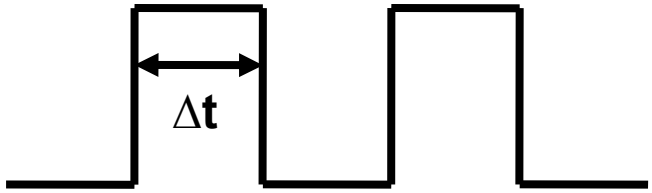


Make a loop
Including the
next delay cell

Measure the
path delay
in the next loop

Calibration with Delay Line





Measured delay difference (Δt) is determined by

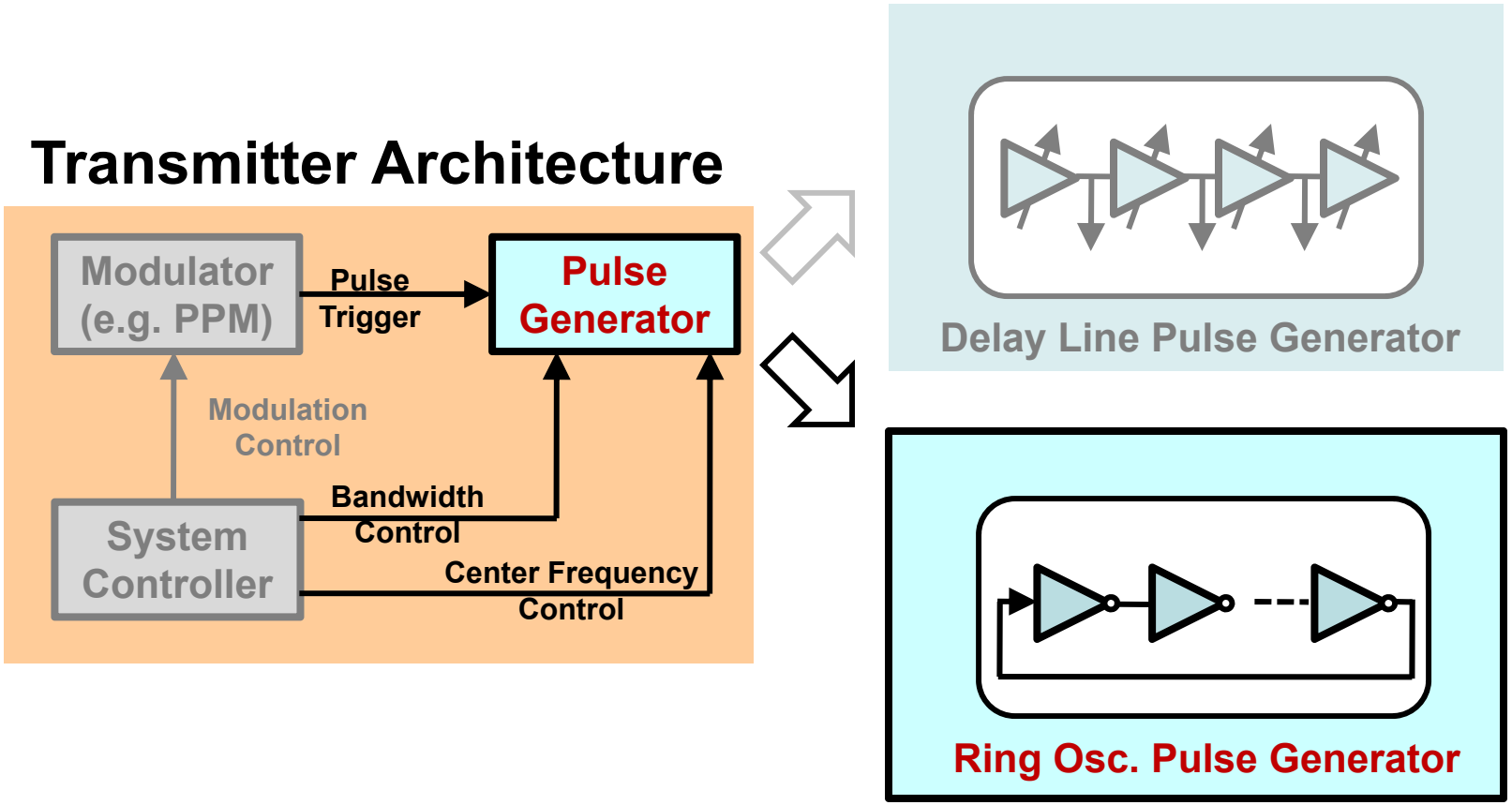
$$\boxed{\Delta t2} + \boxed{\text{path(MR,EC)} - \text{path(MR,EC)}}$$

Tunable value

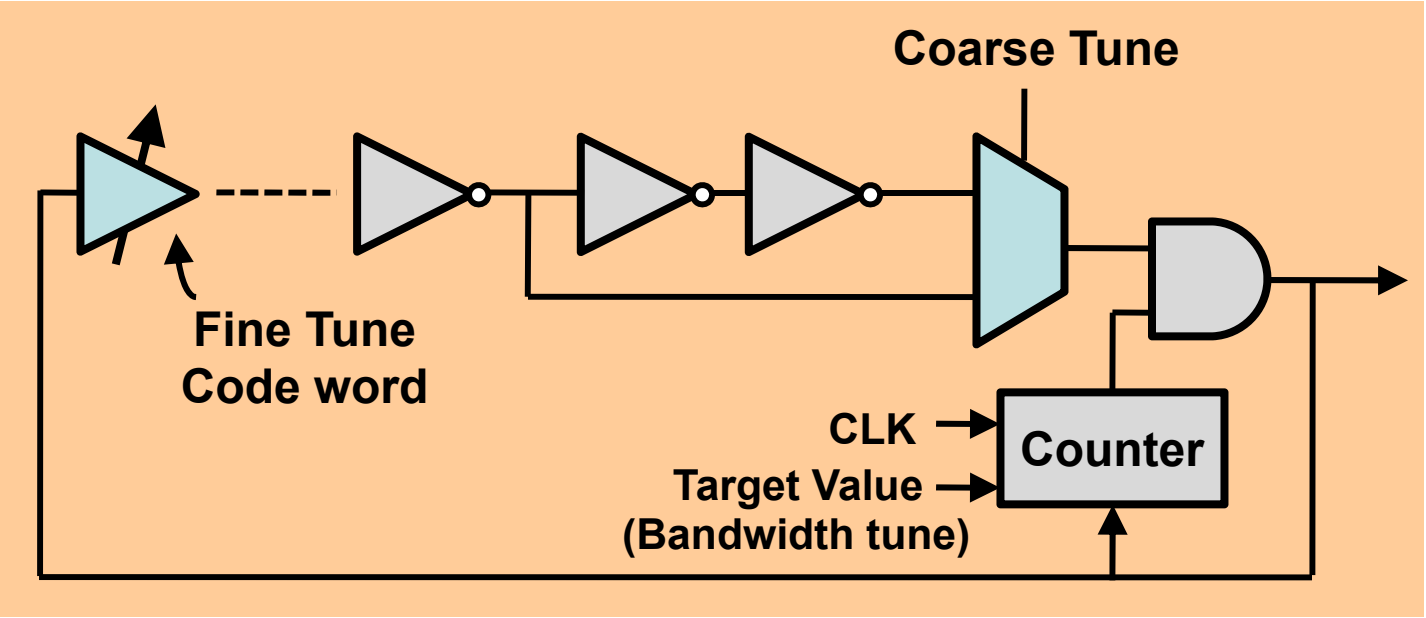
Inherent mismatch by synthesis/PAR

Each edge calibrated

Two Pulse Generators



Ring Oscillator Pulse Generator

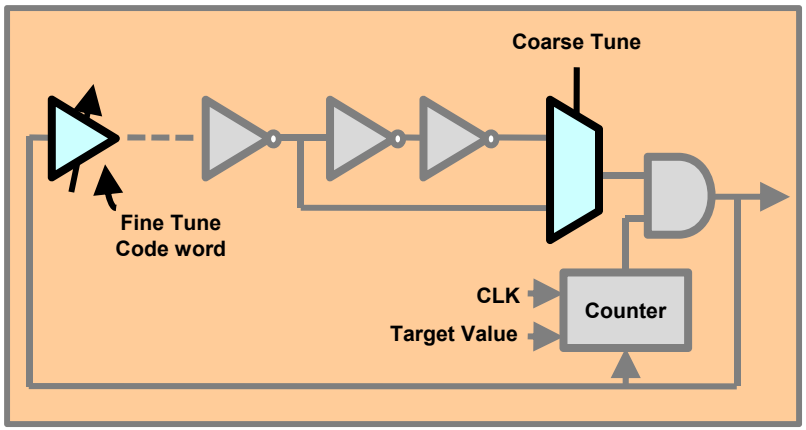


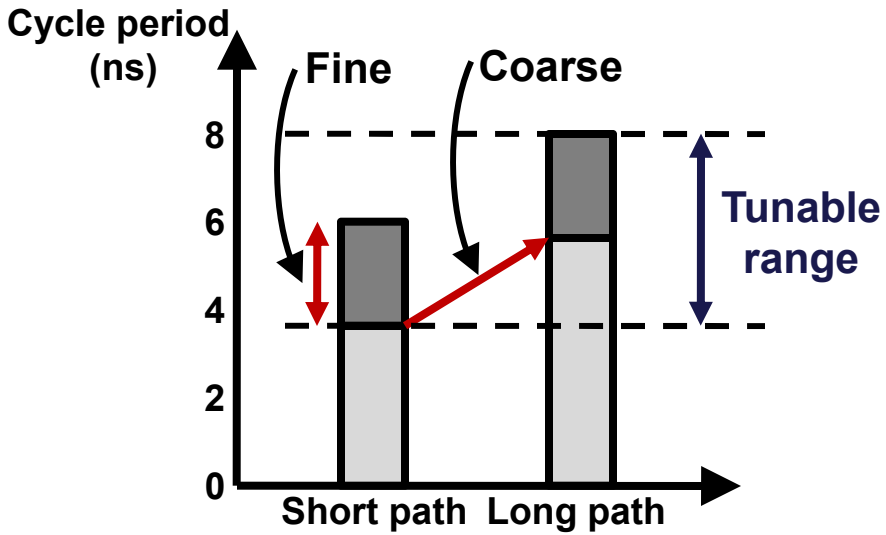
Coarse / Fine control of frequency

Bandwidth tuned with counter

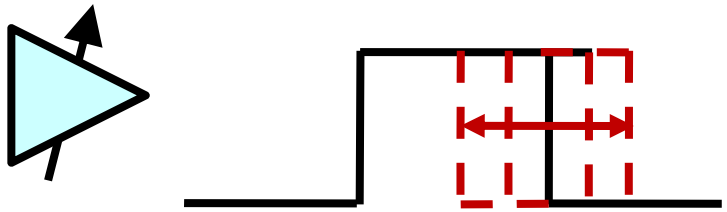
Gating Oscillating signal

Tuning with Ring Oscillator

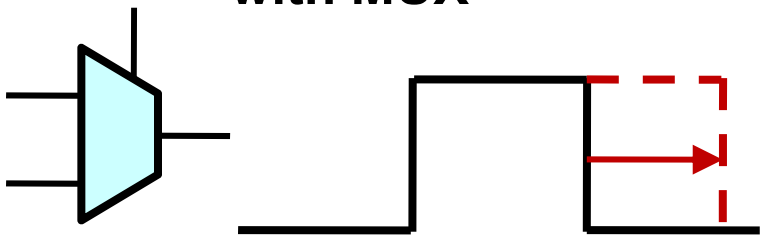




Fine tune with delay cell



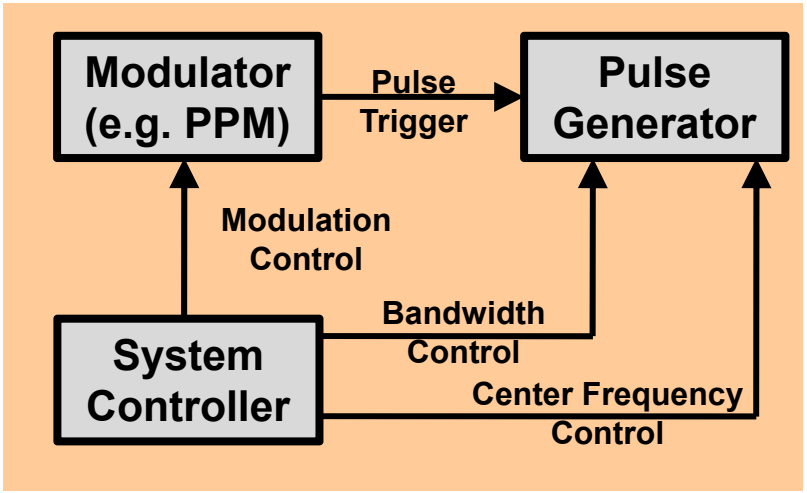
Coarse tune with MUX

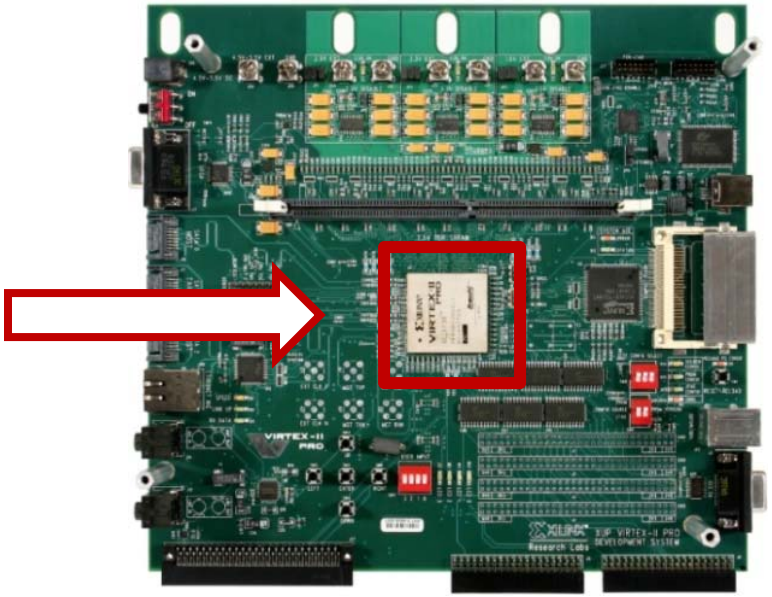


Simpler calibration

FPGA Prototype

Transmitter Architecture





Delay cells are implemented with **TBUFs** in FPGA

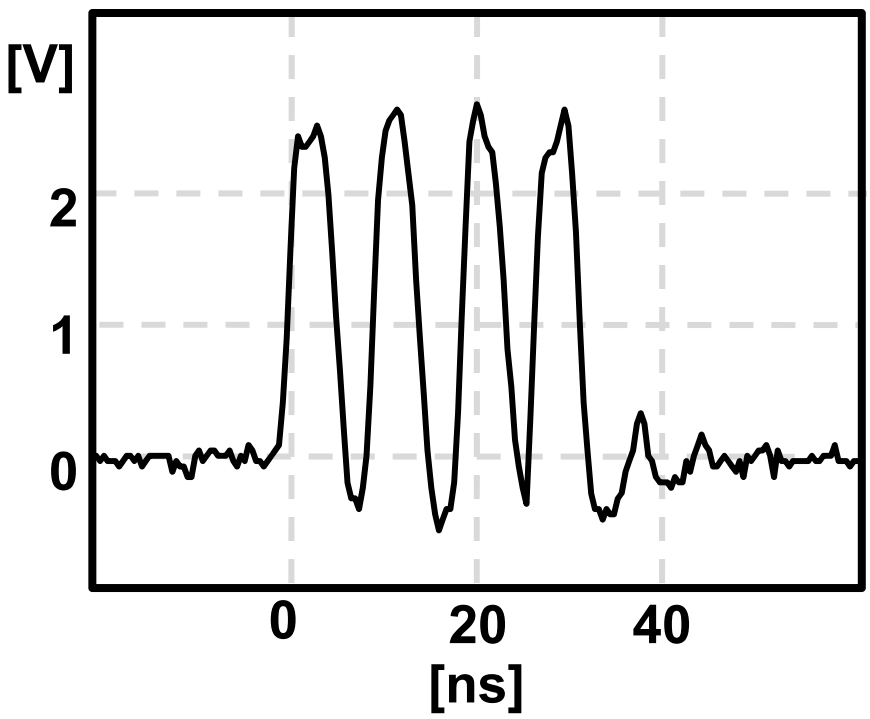
Other logic circuits are mapped to configurable logic blocks (**CLBs**)

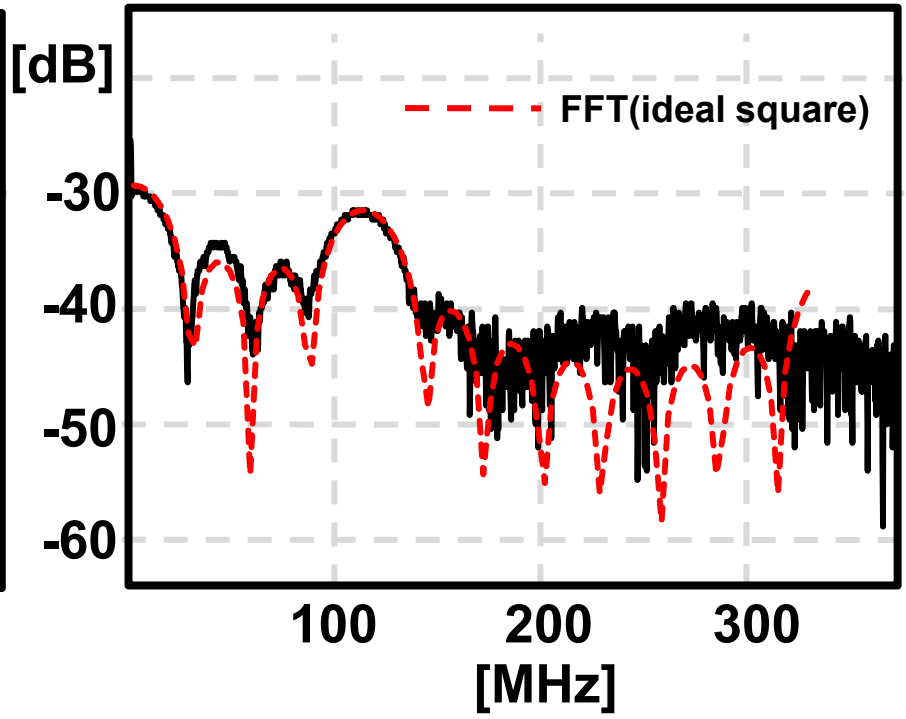
Xilinx Virtex-II Pro FPGA Development board

Synthesis & PAR by design tools

Delay Line PG Measurement

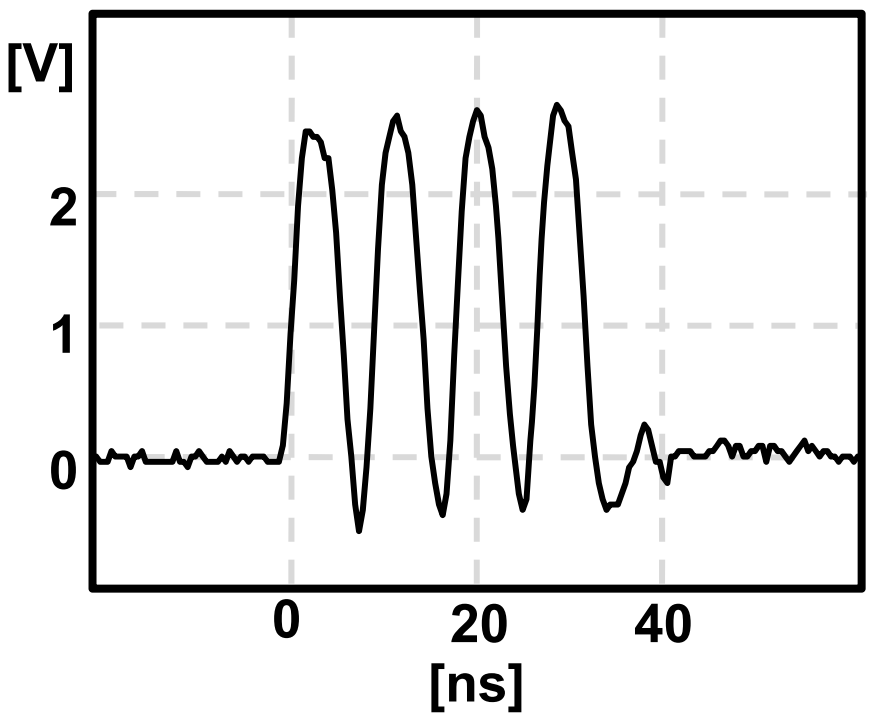
Pulse / spectrum generated by delay line PG

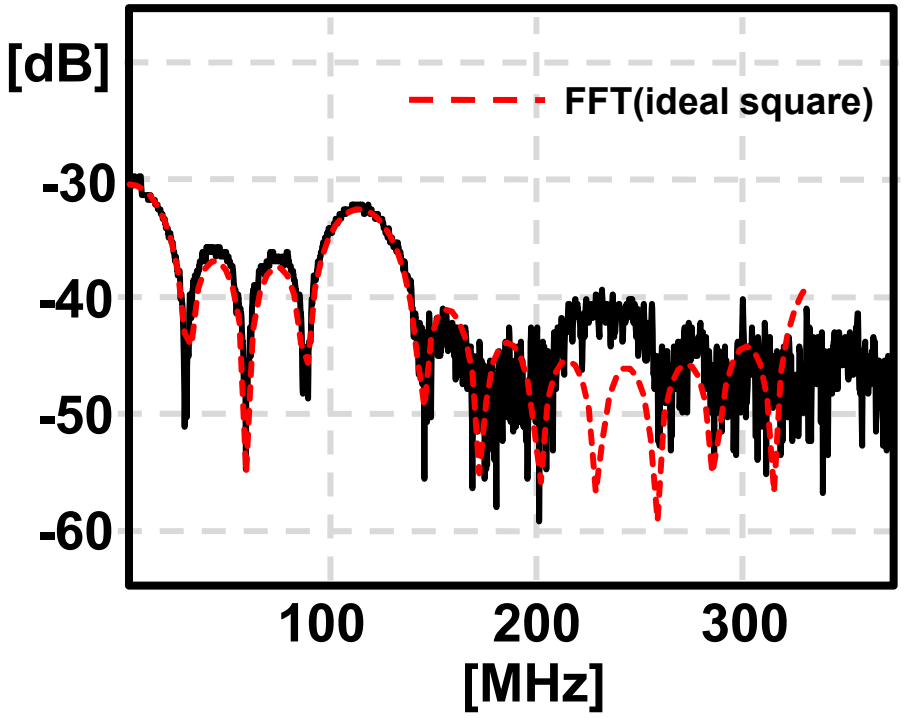




Ring Osc. PG Measurement

Pulse / spectrum generated by ring oscillator PG

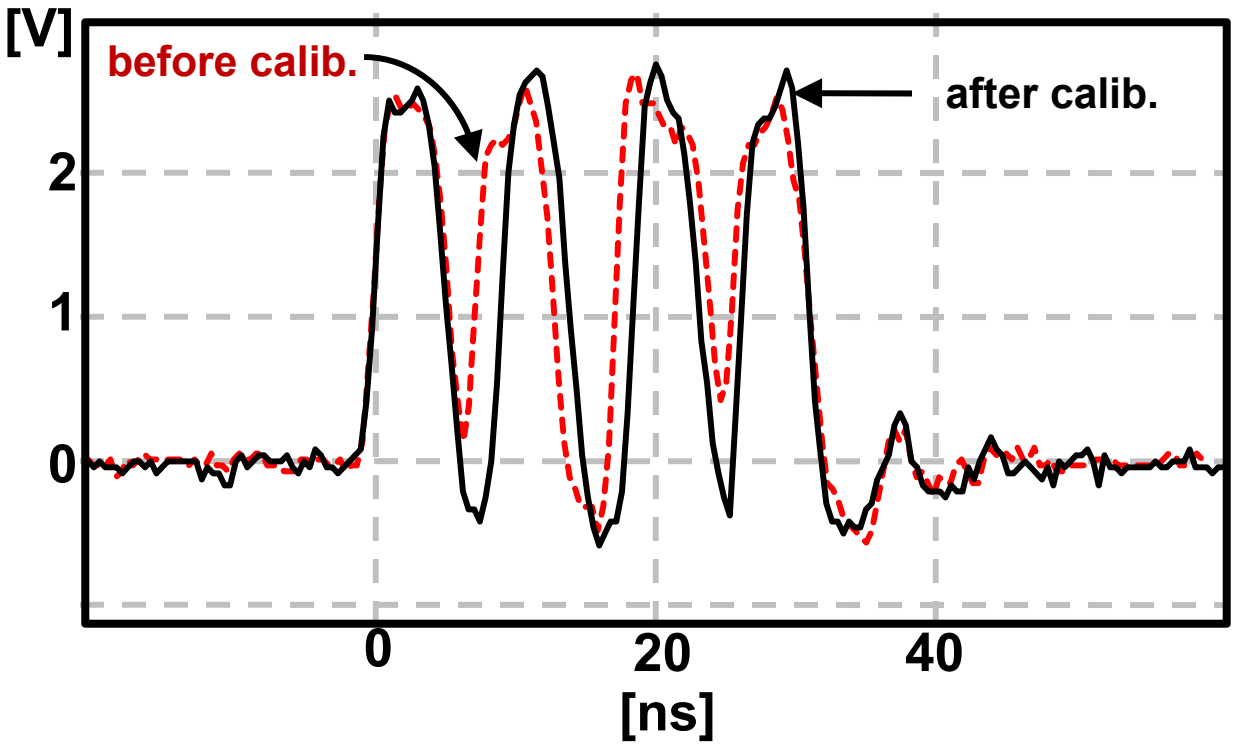




Calibration in FPGA prototype

Before/After calibration

With control code word, each cell is calibrated to have same delay



Calibration in FPGA prototype

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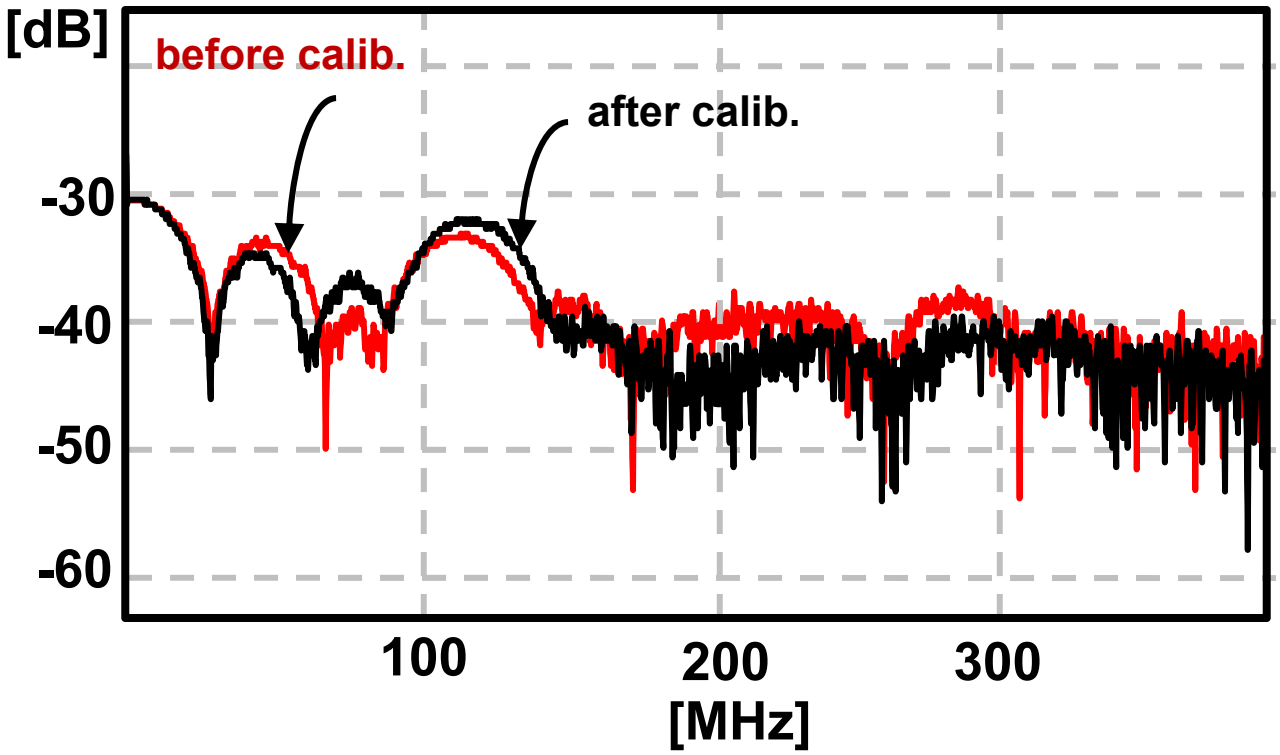

Conclusions

All-digital synthesizable transmitter

- No custom circuit / layout
- Mismatch overcome by calibration

Delay line PG vs. Ring osc PG

- Flexibility vs. Simplicity

FPGA prototype

- Works at scaled frequency