An All-Digital 12pJ/pulse 3.1-6.0GHz IR-UWB Transmitter in 65nm CMOS

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***Abstract*- This paper presents a fully integrated all-digital ultra-wideband (UWB) transmitter. All functional blocks in the transmitter are implemented with digital standard cells and automatically placed-and-routed (APR-ed) by design tools. The center frequency and the bandwidth of the UWB pulses are digitally tuned to compensate for variations, and a calibration scheme utilizing APR mismatch is explored. The transmitter is fabricated in a 65nm CMOS process, and occupies a core area of 0.036mm^2. The transmitter operates in the 3.1-6GHz UWB band, and the active energy consumption ranges from 12pJ/pulse to 38pJ/pulse.**

I. Introduction

The increasing demand for low power wireless applications such as radio frequency identification (RFID) and wireless personal area network (WPAN) has limited the energy budget of the systems, thus requiring higher energy efficiency in the RF circuits. Among many candidate techniques, impulse radio ultra-wideband (IR-UWB) has shown potential as a solution for these applications with many advantages [1]-[10]. Its inherent duty-cycled nature lowers power consumption by limiting circuit operation between pulses, and allows a direct scaling of the power with the data rate. Also, non-coherent IR-UWB communication relaxes RF frequency tolerances, thereby reducing hardware complexity and enabling all-digital architectures, especially for transmitters. When transmitters are implemented with all-digital architectures, IR-UWB obtains additional benefits such as small area, low manufacturing cost, and further energy efficiency [6]-[10].

This paper presents an all-digital UWB transmitter which is synthesized from a CMOS digital standard library. Though the transmitter adopts the conventional methods of generating pulses with digital circuits such as a ring oscillator and a delay line, custom circuits are replaced with standard cells in the proposed transmitter. Standard cells are pre-defined building blocks which are available in most commercial CMOS process technologies. Though they are less flexible to implement circuits with, the simulation, synthesis and layout of the cell-based circuits are highly automated with current design tools. Since all functional blocks are implemented with standard cells, the design procedure of the transmitter is significantly simplified, and the integration of the transmitter with other digital systems can be enhanced.

The transmitter is digitally tuned in a wide range of center frequency and bandwidth, thus it can operate at the desired center frequency and bandwidth even with process, voltage and temperature (PVT) variations. With the flexibility of the performance parameters, the transmitter can be adopted in various applications. This paper also explores a calibration scheme which utilizes systematic mismatch induced by automatic place-and-route (APR) tools. Generally, APR-ed circuits have timing mismatch due to unbalances in the signal paths, which cause non-idealities in the RF circuits. However, the tuning resolution of the center frequency and the bandwidth are enhanced by exploiting the APR mismatch in the proposed calibration scheme.

The remainder of this paper is organized as follows. Section II and III describe the proposed all-digital transmitter architecture and an APR-ed digitally controlled oscillator (DCO). Then, the resolution enhancement scheme utilizing APR mismatch is discussed in the Section IV. Section V presents the measured performance of the UWB transmitter, and Section VI concludes this paper.

II. All-Digital Transmitter Architecture

A block diagram of the proposed UWB transmitter is shown in Fig. 1. The transmitter operates in two modes; pulsing mode and calibration mode. During pulsing mode, the pulse position modulator (PPM) asserts a triggering signal that is modulated in time according to the incoming data bits. The trigger enables the DCO and the delay line. Then, the DCO oscillates at a pre-defined frequency, while the delay line acts as a gating signal to determine when the DCO signal is output to the antenna. In this way, the center frequency is determined by the DCO, and the bandwidth is controlled by the delay line. The output of the delay line is also used to disable the DCO to save power between pulses utilizing the duty-cycled nature of

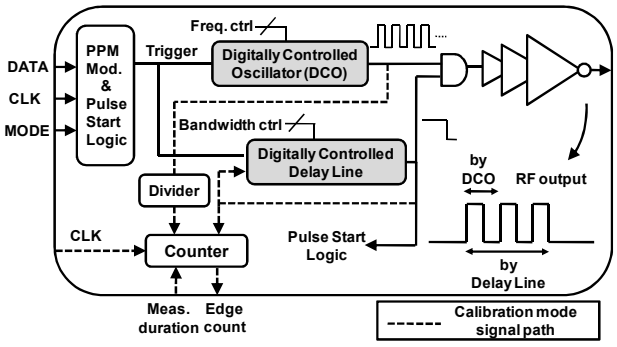

Figure 1. Block diagram of proposed UWB transmitter.

IR-UWB. During the calibration mode, the DCO is continuously enabled while its frequency is measured by counting cycles over a time period. To calibrate the bandwidth of the UWB pulses, the delay line is configured as an oscillating loop, and the frequency around the delay line is measured with a similar technique. The counter values for the DCO and the delay line indicate the current center frequency and the bandwidth of the UWB pulses, and they are separately tuned with the frequency/bandwidth control words to meet the target performance.

III. Digitally Controlled Oscillator

The DCO consists of an odd number of inverting stages as shown in Fig. 2. In order to implement a digitally controllable delay using only standard cells, each stage of the DCO consists of multiple inverting tri-state buffers connected in parallel. While the load capacitance at each stage is fixed by the total number of buffers and the wiring between buffers, the drive strength is controlled by the number of buffers turned on. The maximum frequency is obtained when all buffers are turned on, then the frequency is tuned by turning off buffers to reduce the drive strength. The tuning range and the resolution of the DCO frequency are functions of the number of stages and the number of buffers per stage. As the number of buffers is increased, the tuning range is enlarged, and the resolution is improved. Since power consumption is also increasing, there is a tradeoff between the tuning performance and the power consumption. According to target applications, the number of buffers can be determined in the design phase. The DCO in the transmitter was designed to have three stages to generate an oscillation frequency ranging 3.1-6GHz, and 64 buffers in each stage to achieve a sufficient resolution for the non-coherent UWB communication. The delay line has a similar structure with more stages to generate a delay for UWB pulse width. In the transmitter, it has 57 stages with 4 buffers per stage, and controls the pulse width between 1ns and 4ns.

Instead of custom, symmetric layout to achieve a desired performance, the buffers in the DCO are distributed and routed by APR tools (Fig. 2). This significantly simplifies the design procedure of the transmitter, and enables the complete integration of the DCO and other cell-based digital functional blocks. A key challenge in the cell-based design of RF circuits, however, is systematic mismatch induced by APR. In the DCO, for instance, the placement and wiring of each buffer is not balanced, thus the effective drive strength of each buffer is different. However, this mismatch can be utilized to enhance the frequency resolution of the DCO, as described in Section IV.

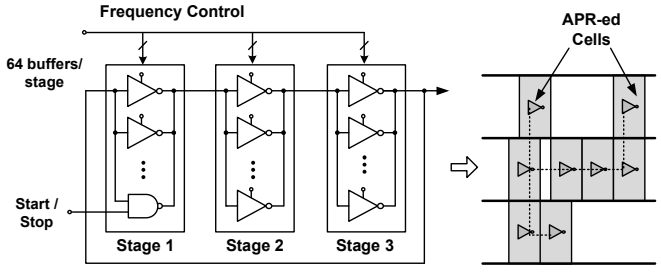

Figure 2. Digitally controlled oscillator with tri-state buffers.

IV. Resolution Enhancement Utilizing Mismatch

As shown in Fig. 2, there are 64 tri-state buffers in each stage of the DCO. When all buffers are enabled, the DCO oscillates at its maximum frequency. When one of the 64 buffers is turned off, the DCO period slightly increases. We refer to this increase in period as the *incremental period*, which is different for each individual buffer, and implies an effective drive strength of each buffer. In the calibration mode, on-chip counters are used to measure the incremental period from every buffer, and the buffers are then sorted based on these values. Fig. 3 shows the measured incremental period per buffer in stage 3 of the DCO. With no mismatch, incremental period would be the same for each buffer, therefore this graph highlights the measured systematic variation in effective drive strength for each buffer due to the APR mismatch. In Fig. 3, the buffers in stage 3 are sorted from the maximum (buffer 34) to the minimum (buffer 33) incremental period.

Once the buffers are sorted, they may be turned off in order to achieve a coarse/fine tuning of the DCO frequency. When the buffers are turned off beginning at the top of the sorted list,

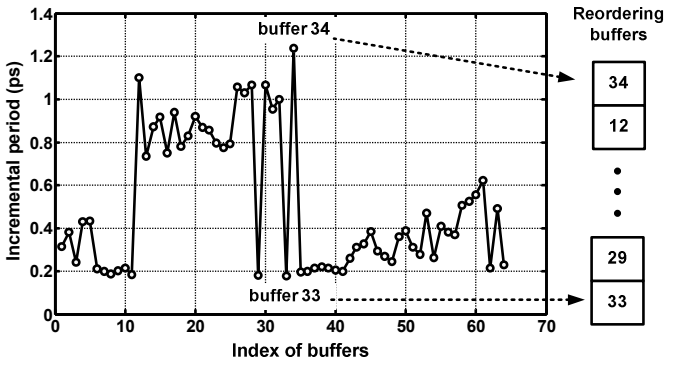

Figure 3. Measured incremental period by turning off each buffer in stage 3, where buffer 34 has the highest effective drive strength and buffer 33 has the lowest effective drive strength.

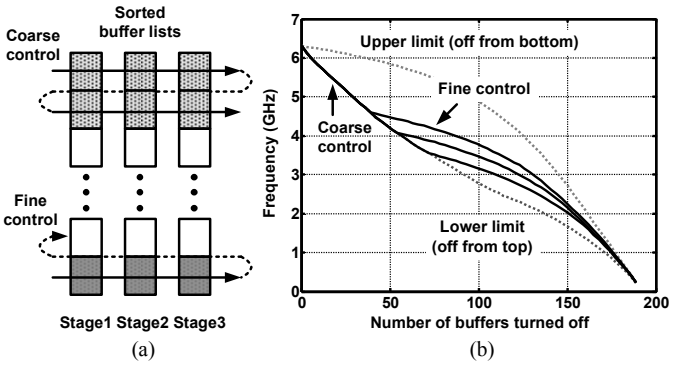

Figure 4. (a) Coarse/fine frequency control using sorted buffer list and (b) measured center frequency control. By reordering buffers to turn off, the frequency is tuned between upper/lower limits.

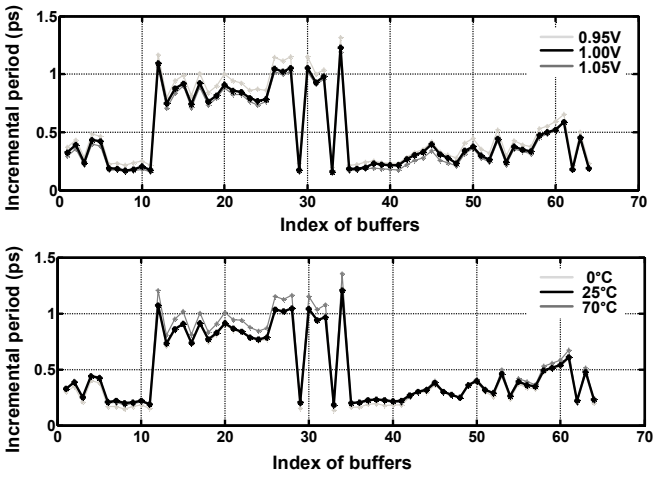

Figure 5. Measured incremental period of buffers in stage 3 over different supply voltages (upper, 0.95V, 1V, and 1.05V) and over different temperatures (lower, 0°C, 25°C, and 70°C).

the DCO frequency decreases rapidly (coarse tune). Turning off the buffers from the bottom of the list decreases the frequency slowly (fine tune). These two curves determine the upper/lower limits of the DCO frequency, and we can achieve a coarse/fine calibration strategy between the limits by reordering the buffers to be turned off. First, a coarse frequency band is selected by turning off buffers with higher drive strengths, and then buffers with lower drive strengths are turned off to finely tune the frequency. Throughout this process, the frequency is measured in a feedback loop by the on-chip counter. The advantage of this scheme is that we can finely tune the frequency around target values, which is possible due to the mismatch in the effective drive strength of each buffer. In the 3.1-6GHz frequency band, there are 60 coarse tuning steps with an average resolution of 30MHz, and at each coarse step, the center frequency can be finely tuned with a resolution less than 10MHz.

The above calibration scheme requires a consistent *order* of the buffers over supply voltage and temperature variations, even though the absolute value of incremental period will vary. In APR-ed circuits, however, the order of buffer drive strength is dominated by systematic mismatch, rather than process variation. Fig. 5 shows the incremental periods of the buffers in stage 3 over different supply voltages and temperatures. Though the absolute values of the incremental period change, the order of buffers in a stage is consistent over the variations. Therefore, the order of the buffers are measured only once per chip, and they can be used to tune the center frequency.

V. UWB Transmitter Performance

The transmitter was fabricated in a 65nm CMOS process, and the micrograph and the layout view of the transmitter are shown in Fig. 6. All functional blocks are integrated through APR so that the transmitter occupies a small area. The area of the transmitter is 0.036mm^2, and it can be reduced to 0.01mm^2 by excluding scan chain circuits that are embedded for testing purposes.

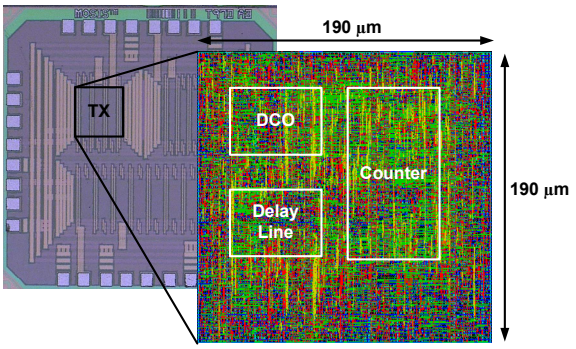

Figure 6. 65nm CMOS transmitter die micrograph and layout.

Fig. 7 shows the measured transient waveform of a 4GHz UWB pulse. The center frequency and pulse width are tuned by the DCO and the delay line, respectively. Since the transmitter generates UWB pulses that are switching between supply voltage and ground, the output has a DC component, which is filtered by an off-chip high-pass filter (or an antenna). The corresponding power spectrum of the pulse is shown in Fig. 8. After the off-chip filtering, the spectrum satisfies the FCC mask. The center frequency of the UWB pulse is tunable in the 3.1-6GHz frequency band with a resolution better than 10MHz, which can target the three channels (3.5, 4.0, and 4.5GHz) in the low band of the 802.15.4a standard [11]. The bandwidth of the UWB pulse is also digitally controlled, and the FCC compliant bandwidth ranges from 600MHz to 1.4GHz.

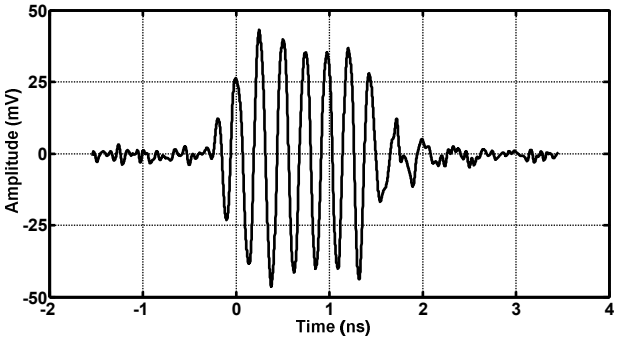

Figure 7. Measured transient waveform of UWB pulse after off-chip high pass filter. The pulse width of the pulses is tuned at 2ns.

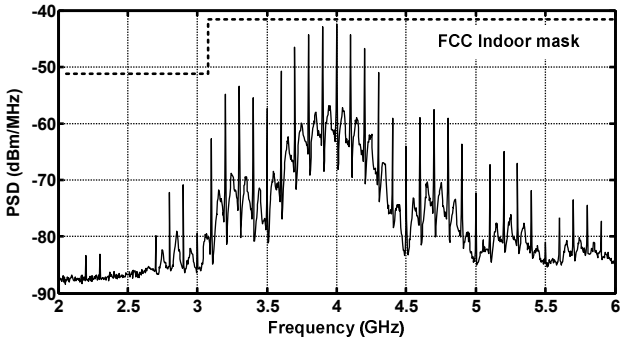

Figure 8. Measured output spectrum of PPM-modulated UWB pulses after off-chip high pass filter. The center frequency of the pulses is tuned at 4GHz, and the data rate is 50Mb/s.

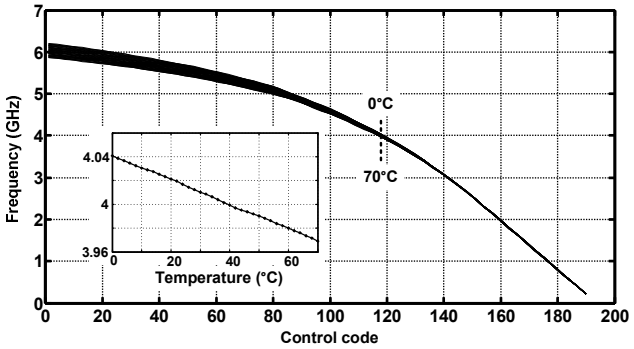

Figure 9. Measured temperature variation of center frequency control.

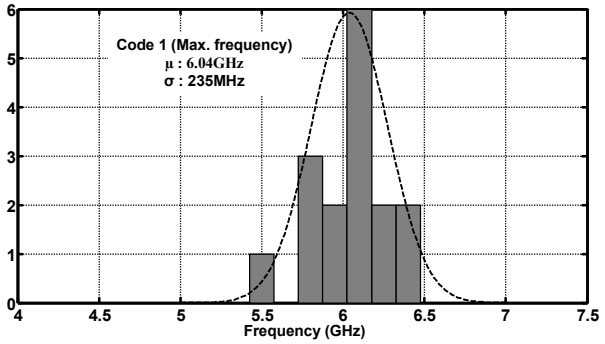

Figure 10. Measured maximum center frequency of 16 chips.

To address the performance sensitivity of the transmitter over temperature variation, the frequency of the DCO was measured over 0°C to 70°C as shown in Fig. 9. The frequency varies less than 10% over the temperature range, which is well within the tuning range of the DCO. Fig. 10 shows the distribution of measured maximum frequency of 16 chips. Since the transmitter can be tuned in a broad range of center frequency with digital control, it only requires the maximum frequency to be over the target range. The distribution indicates that greater than 99.99% of the chips will cover the low band of the 802.15.4a standard given PVT and APR variations.

The transmitter consumes a fixed power of 220μW due to leakage currents, and the active energy added to the core while pulsing depends on the activity factor such as the center frequency and pulse width. The measured active energy approximately fits (1):

$$\text{Active energy (pJ/pulse)} = 2.2 \cdot (\text{center frequency}) \cdot (\text{pulse width}) + 5.0 \quad (1)$$

and it ranges from 12pJ/pulse to 38pJ/pulse over the frequency of 3.1-6GHz, and the bandwidth of 600MHz-1.4GHz. The performance of the transmitter is summarized in Table I.

VI. Conclusion

An all-digital UWB transmitter was designed and fabricated in a 65nm CMOS process. All functional blocks are implemented with digital standard cells and automatically place-and-routed. The center frequency and the bandwidth of the UWB pulses are digitally tuned to compensate for variations, and the systematic mismatch from automatic PAR is utilized to enhance the tuning resolution of the center frequency and the bandwidth.

TABLE I
Performance Summary

	This work	[9]	[10]
Process	65nm CMOS	180nm CMOS	90nm CMOS
Supply	1V	1.8 to 2.2V	1V
Die Area	0.036mm^2	0.045mm^2	0.07mm^2
Modulation	PPM	BPSK	PPM+BPSK
PRF	0 to 50MHz	<750MHz	0 to 15.6MHz
Center Frequency	0.2 to 6GHz	8GHz	2.1 to 5.7GHz
Bandwidth (10dB)	0.6 to 1.4GHz	~2GHz	~500MHz
Active Energy/pulse	12 to 38pJ/pulse	>12pJ/pulse	>17pJ/pulse

Acknowledgment

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