A Cyclic Vernier Time-to-Digital Converter Synthesized from a 65nm CMOS Standard Library

Youngmin Park and David D. Wentzloff
Electrical Engineering and Computer Science
University of Michigan
Ann Arbor, Michigan, United States of America
{yminpark, wentzlof}@umich.edu

***Abstract*—This paper presents a synthesizable cyclic Vernier time-to-digital converter (TDC) with digitally controlled oscillators (DCOs). All functional blocks in the TDC are implemented with digital standard cells and placed-and-routed (PAR) by automatic design tools; thus, the TDC is portable and scalable to other process technologies. The effect of PAR mismatch is characterized in the post-layout simulation and utilized to achieve 1ps TDC resolution. The TDC was designed in a 65nm CMOS process, and occupies 0.001mm^2.**

I. Introduction

Recent process scaling has been providing several advantages to digital circuits. Die area decreases proportional to the scaling factor, and operating frequency increases with reduced parasitics. Also, power consumption decreases squarely proportional to the voltage scaling. Unlike their digital counterparts, analog circuits do not benefit from the process scaling as much. Lower supply voltage requires more accurate voltage control, and deteriorates signal-to-noise ratio (SNR) of the circuits. To maintain the same performance, the power dissipation of analog circuits does not scale as effectively as their digital counterparts [1].

This has led to recent trends to develop digitally-assisted or all-digital architectures of conventional analog applications that leverage the advanced digital process. Analog-to-digital converters (ADCs) have adopted digital calibration schemes which relax the complexity of analog parts, thereby reducing power of the ADCs [2]. Other applications such as transmitters and phase locked loops (PLLs) have adopted all-digital architectures [3]-[5]. In these circuits, the signals are digitized and processed in the time domain with the high time resolution of digital circuits. These all-digital architectures achieve small area, low power, and low cost implementation.

This paper proposes a *synthesizable* time-to-digital converter (TDC). All functional blocks in the proposed TDC are described in a hardware description language, then synthesized and place-and-routed (PAR) by automatic design tools. Since the TDC is implemented with digital standard cells, there is no custom circuit design or custom layout that requires comprehensive characterization of devices in each process technology. Therefore, the TDC is portable and scalable to different process technologies.

The TDC is a core block in most all-digital PLLs, replacing analog-intensive blocks such as a phase detector and a charge pump [5]. While digital TDCs have been presented in literature [9-11], these implementations are based on full-custom layout. What differentiates this work from prior art is that this TDC implementation is fully automated through synthesis and PAR, and furthermore this TDC exploits the mismatch from PAR to achieve high timing resolution. The remainder of this paper is organized as follows. Section II describes the cyclic Vernier TDC architecture and functional blocks. Then, the calibration scheme of the TDC resolution is discussed in the Section III. Section IV presents the simulated performance of the TDC, and Section V concludes this paper.

II. Cyclic Vernier Time-to-Digital Converter

A. TDC Architecture

Fig. 1 shows the block diagram of the cyclic Vernier TDC [6] [7]. The goal of the TDC is to measure the time difference between the rising-edges of the 'Start' and 'Stop' signals. When the 'Start' signal is asserted, the slow digitally controlled oscillator (DCO) starts to oscillate with a period of

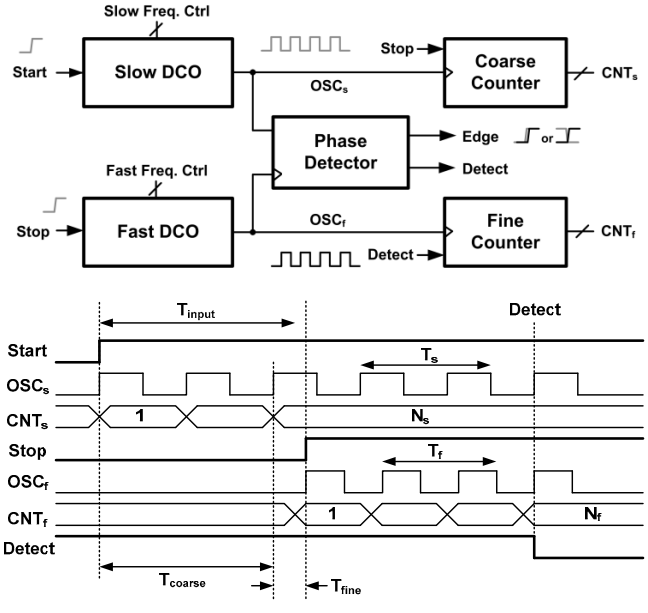

Fig. 1. Block diagram of the proposed TDC and timing diagram. All functional blocks are implemented with logic cells and automatically placed and routed with design tools.

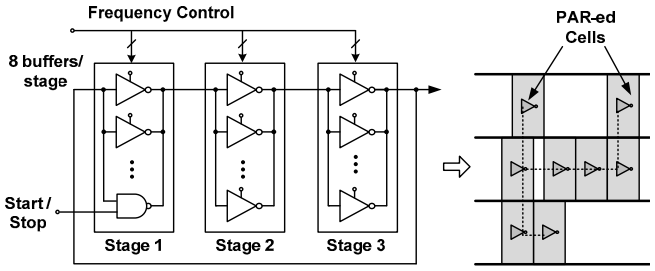

Fig. 2. Digitally controlled oscillator with tri-state buffers. The buffers from standard library are automatically placed-and-routed.

T_s, and the number of oscillations is counted by the coarse counter. Then, after an input delay of $T_{input,}$ the 'Stop' signal triggers the faster DCO with a period of T_f. At this time, the coarse counter is disabled, and the output of the counter represents a coarse measurement of the time between 'Start' and 'Stop' rising-edges (T_{coarse}). To improve the measurement accuracy, the residue of the input delay (T_{fine}) is measured by the Vernier structure. Since T_f is smaller than T_s, the time difference between rising edges of two oscillations is reduced every cycle by the difference in periods ($T_s - T_f$), and the edge of the fast DCO eventually catches up with the slow DCO. By counting the number of cycles it takes for the fast DCO to catch up with the slow DCO, T_{input} can be determined as follows.

$$T_{input} = t_{STOP} - t_{START} \quad (1)$$

$$T_{input} = T_{coarse} + T_{fine} = N_s T_s + N_f(T_s - T_f) \quad (2)$$

where N_s and N_f are the number of cycles of the slow and fast oscillations, respectively. As shown in Fig. 1, the TDC operates in two-steps; a coarse step and a fine step. The resolution of the coarse step is the period of the slow DCO, and the resolution of the fine step is the *difference* between the periods of the two DCOs. Note that the fine resolution does *not* depend on the absolute frequencies of the DCOs, but only their difference in periods. This is crucial for the calibration of mismatch between the PAR-ed DCOs discussed in Section III. The two-step operation relaxes the resolution of the coarse step, thereby increasing the input range efficiently. While the previous cyclic Vernier TDC architectures adopt voltage controlled oscillators (VCOs), which require custom circuit design and layout, the proposed TDC adopts DCOs that are implemented with standard cells. The periods of the DCOs are measured with the built-in counters in the one-time calibration mode, and the coarse step resolution and fine step resolution are stored for the time-to-digital conversion.

B. Digitally Controlled Oscillator

The DCOs each consists of three inverting stages as shown in Fig. 2. Each stage is implemented with eight parallel inverting tri-state buffers which are digitally turned on. Tri-state buffers are available in all commercial standard cell libraries. While the load capacitance at each stage is fixed by the number of buffers and wiring capacitance, the driving strength can be varied by turning off tri-state buffers, thereby reconfiguring the frequency of the DCO.

Since the buffers are automatically PAR-ed by design tools, the placement and routing of the buffers are not regular as illustrated in Fig. 2, and this results in systematic mismatch in the wiring capacitance, and the effective driving strength of each buffer. Though the individual driving strength cannot be controlled in the automated layout, the placement area and the wire lengths are constrained by layout algorithms, and the distribution of the PAR mismatch is predictable at the design phase. The proposed TDC utilizes the systematic mismatch to achieve high resolution. The calibration schemes and simulated results are discussed in the next section.

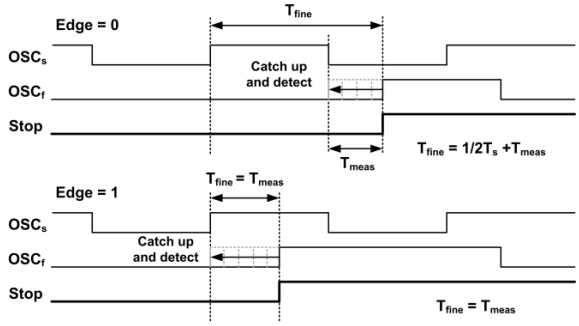

Fig. 3. Detection of both edges in the proposed phase detector

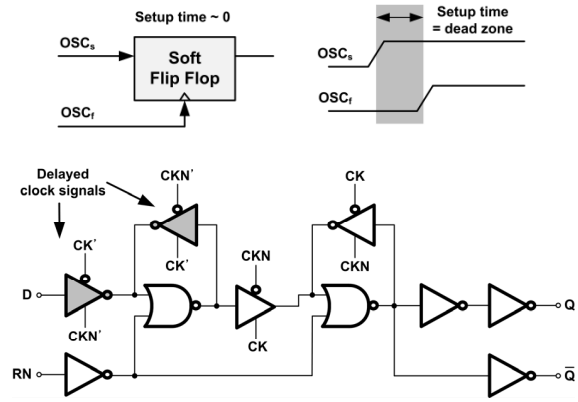

Fig. 4. Soft edged flip flop. To reduce the setup time of flip flop, the clock signals to the master block are delayed.

C. Phase Detector

The phase detector detects the phase (high or low) of OSC_s at the rising edge of OSC_f, and asserts 'Detect' when the phase changes. While only one edge (the rising edge) is detected in conventional TDCs, the proposed TDC detects both rising and falling edges (Fig. 3). When the rising edge of OSC_s is detected, the 'Edge' signal is asserted, and the measured time indicates the fine step measurement (T_{fine}). On the other hand, if the falling edge of OSC_s is detected, 'Edge' is de-asserted, and half of T_s is added to the measured time. In either case, the measurement operation is terminated, thereby reducing the maximum measurement time by half, and saving power in the TDC.

In the phase detector, the phase is compared using a flip-flop (FF). The setup time of a standard D-flip-flop (DFF), however, creates a dead zone in the detector. If two edges are close to each other by less than the setup time, the DFF cannot detect the edge correctly. The proposed TDC adopts a soft-edged flip-flop (soft-FF) [8]. In the soft-FF, the clock signals to the master stage are delayed by one inverter delay, so that

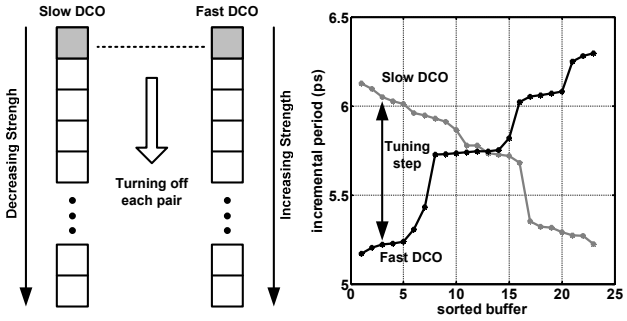

Fig. 5. Calibration of TDC resolution. By turning off buffers in order of increasing (decreasing) strength, a fine and monotonic tuning step is achieved.

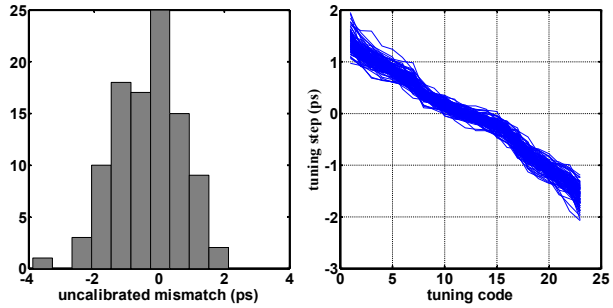

Fig. 6. Monte Carlo simulation of un-calibrated mismatch and tuning steps over process variation and device mismatch.

the input signal has more time to be passed onto the slave stage (Fig. 4). By adjusting the delay time for the master clock signals, the setup time of the soft-FF can be reduced to zero. This eliminates the dead zone, and reduces the offset at the TDC outputs. The soft-FF is the only custom design in the TDC. When laid out as a cell, it also can be automatically placed and routed.

III. TDC Calibration Utilizing Mismatch

A key challenge in the standard cell-based implementation is systematic mismatch induced by the automatic PAR. Unlike custom layout, automatic PAR generates significant mismatch in interconnects, preventing accurate modeling of the analog performance. The systematic mismatch, however, can be utilized for a higher resolution, if measured and calibrated accurately. This section proposes a calibration scheme for the TDC resolution.

There are two time resolutions in the proposed TDC, a coarse step resolution (T_s) and a fine step resolution (T_s-T_f). Ultimately, the performance of the TDC is determined by the fine step resolution. In a PLL, for instance, the edges are close together when the PLL is in lock ($N_s = 0$), and the TDC output becomes dependent only on the fine step resolution. For the all-digital PLL application, we are therefore mainly interested in the calibration of the *difference* between two periods, and less on their absolute values.

Fig. 5 shows the calibration scheme of the periods of the DCOs. There are a total of 23 tri-state buffers in each DCO (3 stages, 8 buffers / stage, and one NAND gate). When all buffers are enabled, the DCO oscillates at its maximum

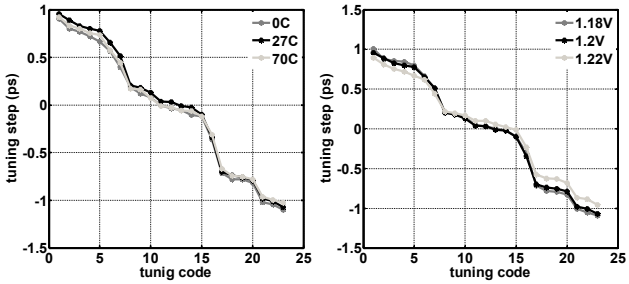

Fig. 7. Simulated temperature / supply voltage sensitivity of TDC tuning steps.

frequency. When one of the 23 buffers is turned off, the DCO period slightly increases. We refer to this increase in period as the incremental period. If all devices and wiring in the DCO were matched, it would not matter which single buffer were disabled in the ring, as they would all produce the same incremental period change. Now consider that this DCO has been designed with automatic PAR, and there is mismatch in the wiring of each buffer and in the devices. The incremental period will therefore be different for each one of the 23 buffers in the DCO. The difference will depend on the systematic wiring differences for each buffer. During a one-time calibration, the buffers are sorted based on the incremental period, then, the order represents the effective driving strength of each buffer. By turning off a buffer in the order of increasing (or decreasing) strength, a fine and monotonic resolution can be achieved.

The TDC resolution is determined by the net effect of un-calibrated mismatch and tuning step. The un-calibrated mismatch refers to the period difference between the DCOs when all the buffers are turned on, and the tuning step refers to the differential effect by turning off buffers in the DCOs. Given an un-calibrated mismatch, an appropriate pair of buffers is turned off to obtain a target TDC resolution as shown in Fig. 5. If the un-calibrated mismatch is excessive, the TDC resolution can be coarsely tuned by turning off a different number of buffers in each DCO or turning off multiple pairs at a time. We reiterate that the TDC resolution depends only on the difference in periods, therefore a suitable combination needs only be found that achieves the period difference for a target resolution, and this is independent of the absolute frequency.

Fig. 6 shows the Monte Carlo simulation of the un-calibrated mismatch and tuning step of the TDC with process variation and mismatch. Although the process variation and device mismatch affect the absolute value of the periods, T_s and T_f, we focus on the difference between periods which determines the fine resolution of the TDC. As shown in Fig. 6, the variation in the un-calibrated mismatch and the tuning step is relatively small, and the one-time sorting calibration will select the appropriate buffer combination for a target resolution. Fig. 7 shows that the tuning step for each calibration code is not affected significantly by environmental variations such as temperature and supply voltage. For a fixed combination of buffers, a worst-case change in resolution of 10% is observed over temperature and supply voltage variation.

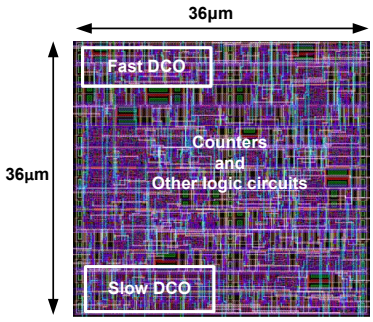

Fig. 8. Layout view of the proposed TDC. All functional blocks including DCOs are integrated.

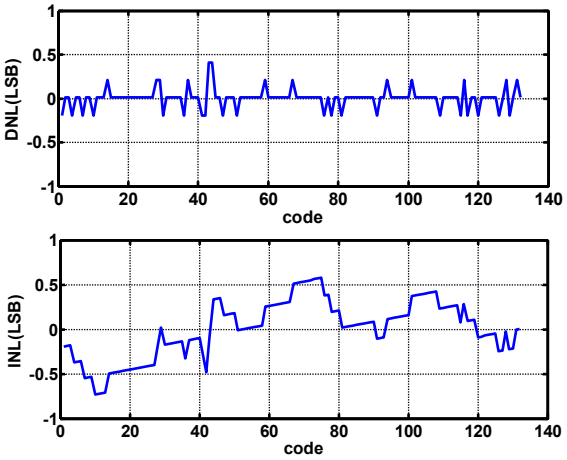

Fig. 9. Simulated DNL and INL of the TDC

IV. TDC PERFORMANCE

The synthesizable cyclic Vernier TDC was designed in 65nm CMOS, and the layout view of the TDC is shown in Fig. 8. All functional blocks are integrated through automatic PAR so that the TDC occupies a small area. The core area of the TDC is only 0.0013mm^2.

Fig. 9 shows the simulated differential nonlinearity (DNL) and integral nonlinearity (INL) of the TDC. The fine step resolution was calibrated to 1ps by configuring the DCOs as described in Section III, and T_{input} was given from 0ps to 130ps, which is a half of T_s. The maximum DNL and INL are less than 0.5 and 0.8 LSBs, respectively.

The power dissipation in the Vernier structure depends on the T_{input}, since the measurement operation time in fine step is proportional to T_{fine}. The simulated power dissipation ranges from 0.01mW to 0.15mW, normalized to 1MS/s. The performance of the TDC is compared to prior work in Table 1.

V. CONCLUSION

An all-digital synthesizable cyclic Vernier TDC was proposed and designed in 65nm CMOS. While there has been increasing interest in digitally-assisted or all-digital implementation of conventional analog function, the TDC shows a new design methodology, where all functional blocks are implemented with standard cells, and automatically PAR-ed. This implementation of TDC with standard logic cells benefits from process scaling, enabling small area, low power and a higher time resolution.

TABLE I
PERFORMANCE COMPARISON

	This work	[7]	[9]	[10]	[11]
Process	65nm CMOS	130nm CMOS	90nm CMOS	130nm CMOS	90nm CMOS
Technique	Cyclic Vernier	Cyclic Vernier	Time Amp.	Gated RO	Passive Interpol.
Resolution	1ps	2ps (sim) 8ps (meas)	1.25ps	6ps	4.7ps
DNL/INL(LSB)	0.5 / 0.8	-	0.8 / 3	-	0.6/1.2
Power* (mW)	0.01-0.15	0.5	0.3	0.06-0.6	20
Area (mm^2)	0.001	0.263	0.6	0.04	0.02

* power is normalized to 1MS/s

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