Cyclic Vernier Time-to-Digital Converter Synthesized from a 65nm CMOS Standard Library

Youngmin Park and David D. Wentzloff

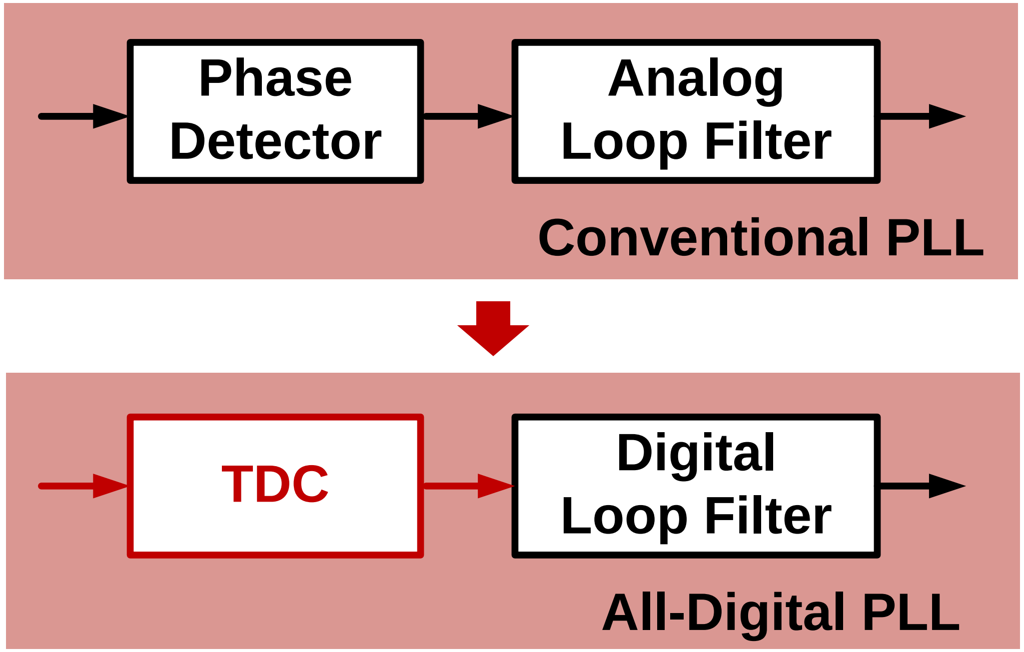
University of Michigan

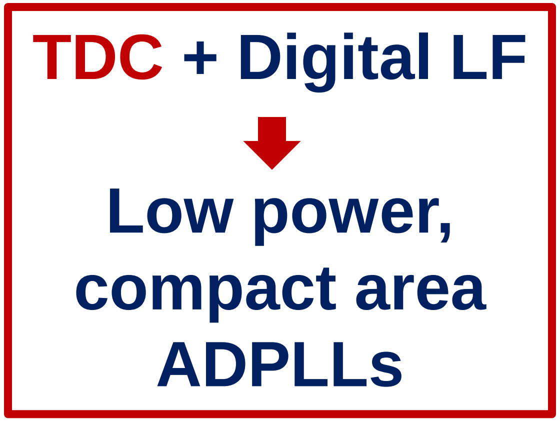
Ann Arbor, MI, USA

ISCAS 2010

Time-to-Digital Converter

- Core building block in ADPLL

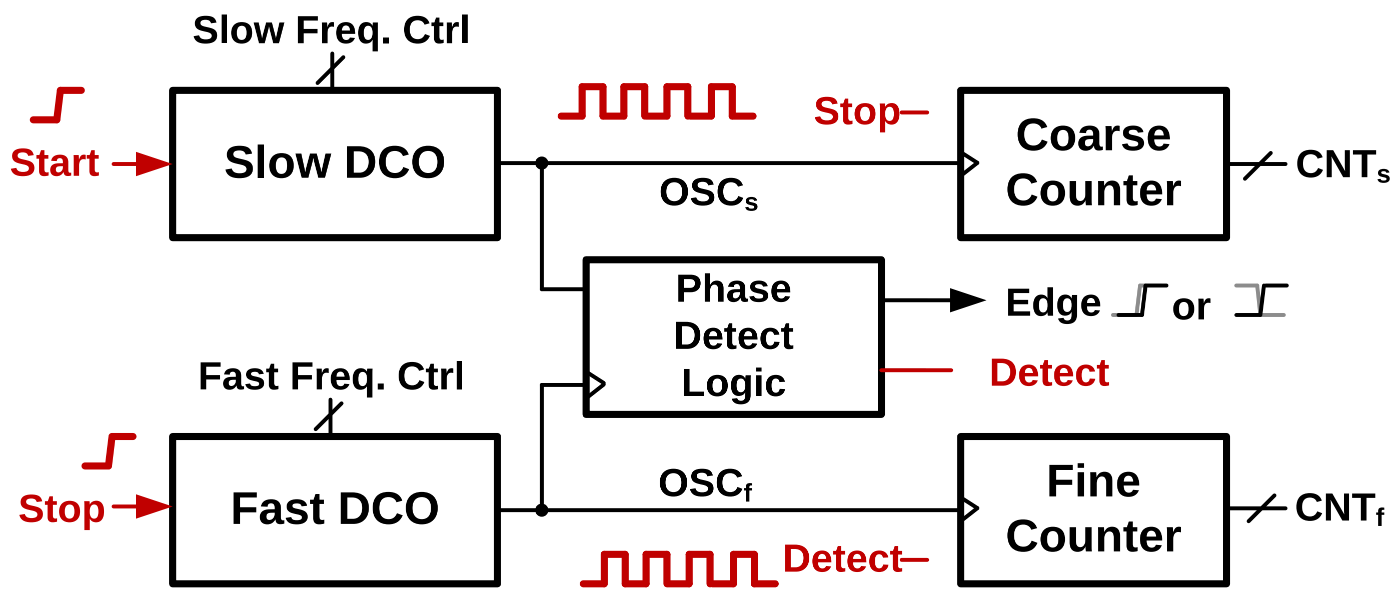




- Other applications
  - Time-of-flight measurement, full speed testing, measurement instruments …

TDC Block Diagram

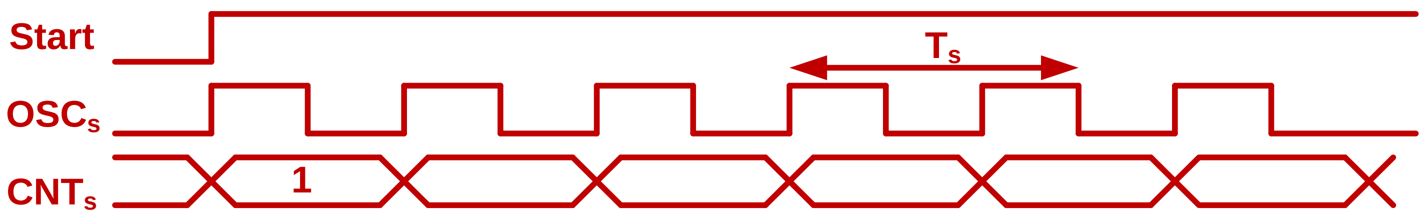
- **Vernier ring time-to-digital converter**
  - **Resolution : difference between two oscillation periods**



Vernier Ring : high resolution, large detectable range

TDC Operation

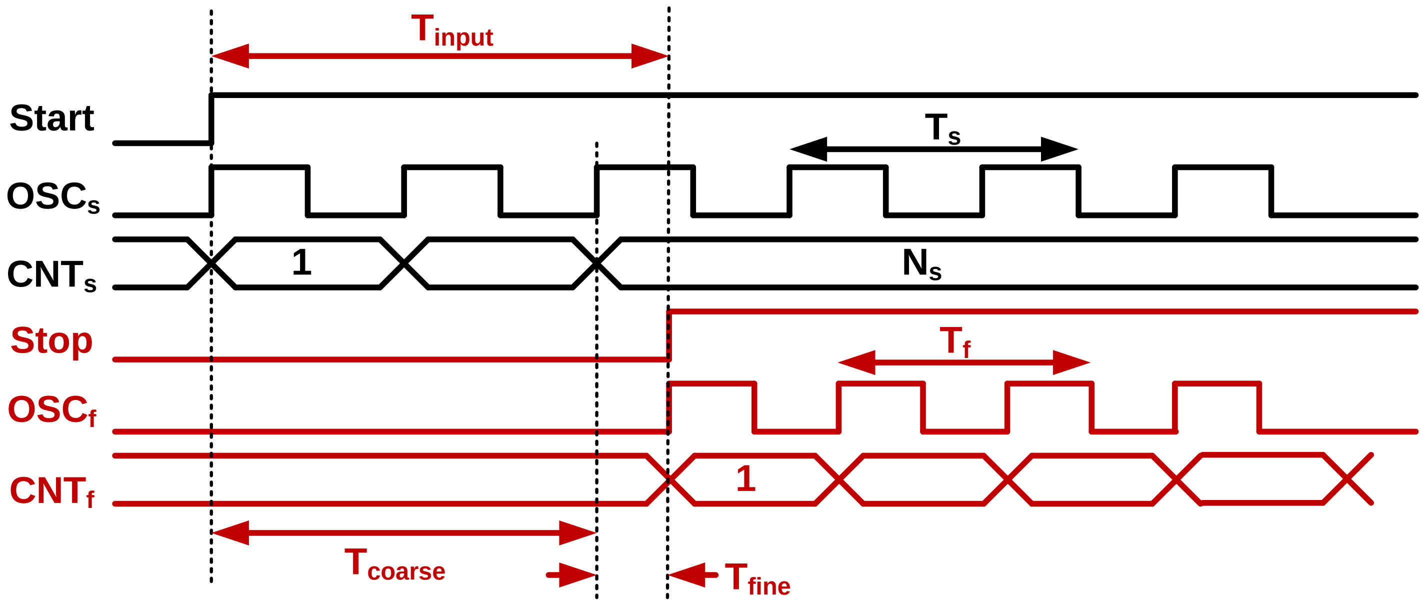
- **Start arrives …**



Two step measurement
Coarse step : resolution of T_s

TDC Operation

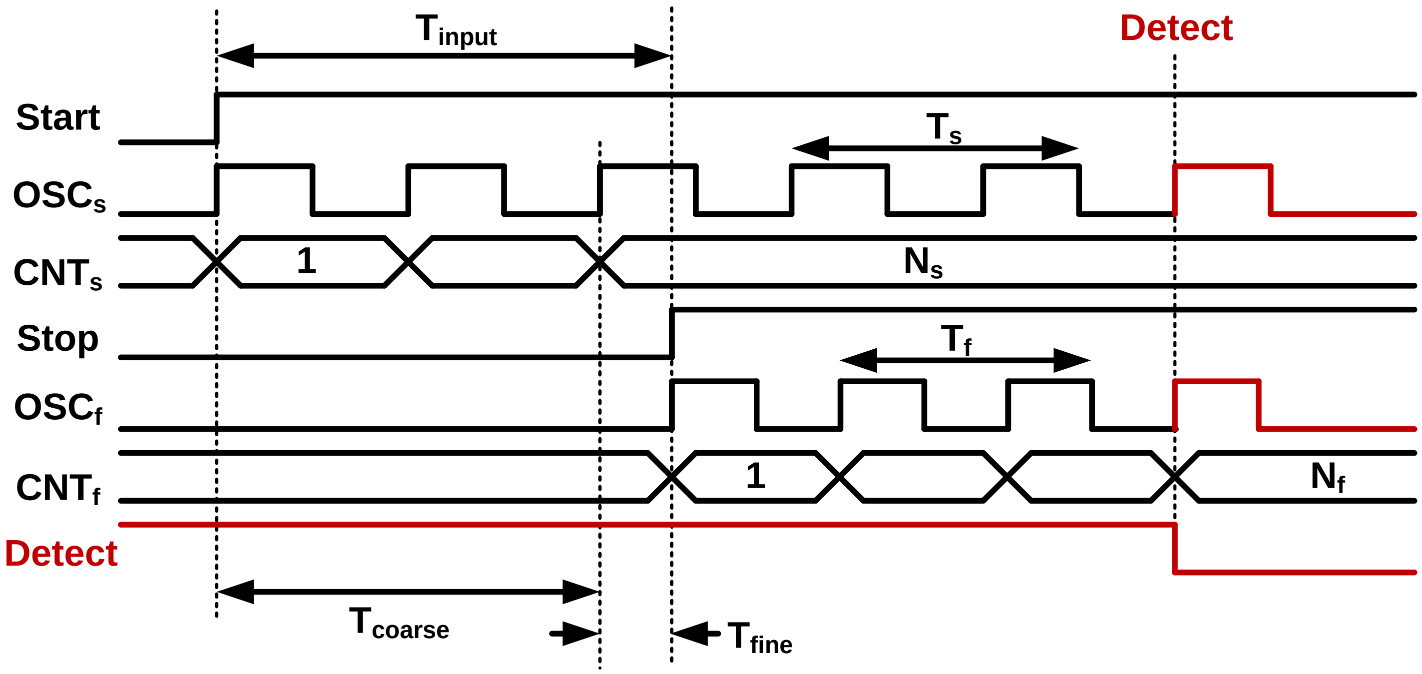
- **Stop arrives …**



Two step measurement
Fine (Vernier) step : resolution of T_s - T_f

TDC Operation

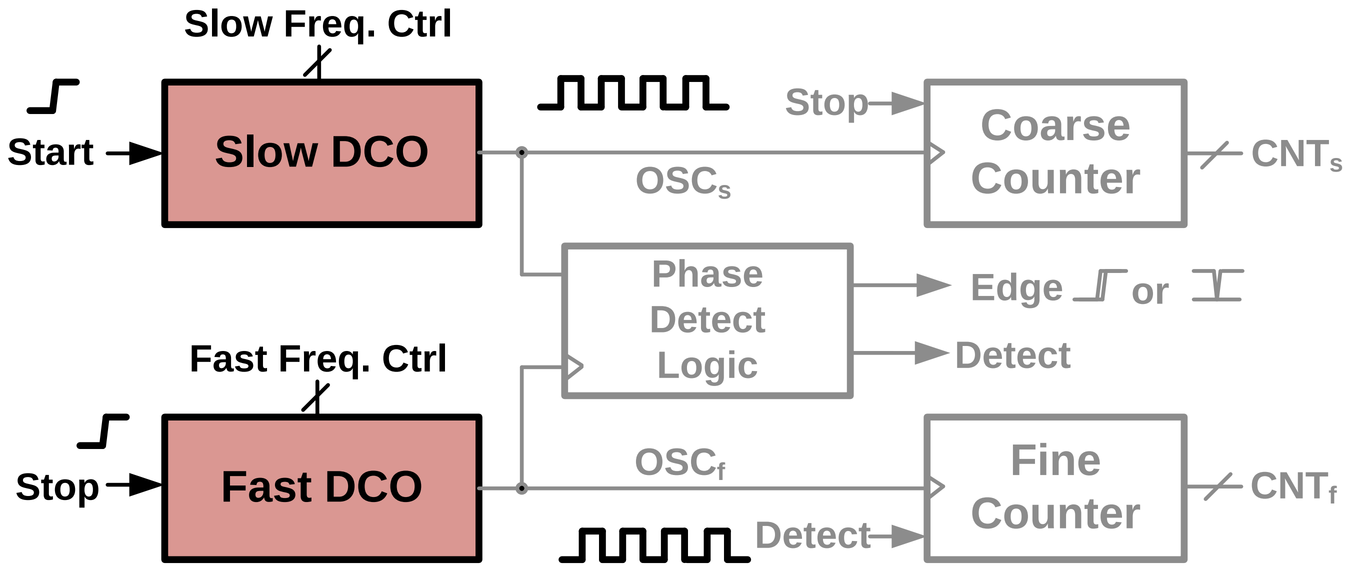
- **Edge detected**



$$T_{input} = N_s T_s + N_f(T_s - T_f)$$

Digitally Controlled Oscillator

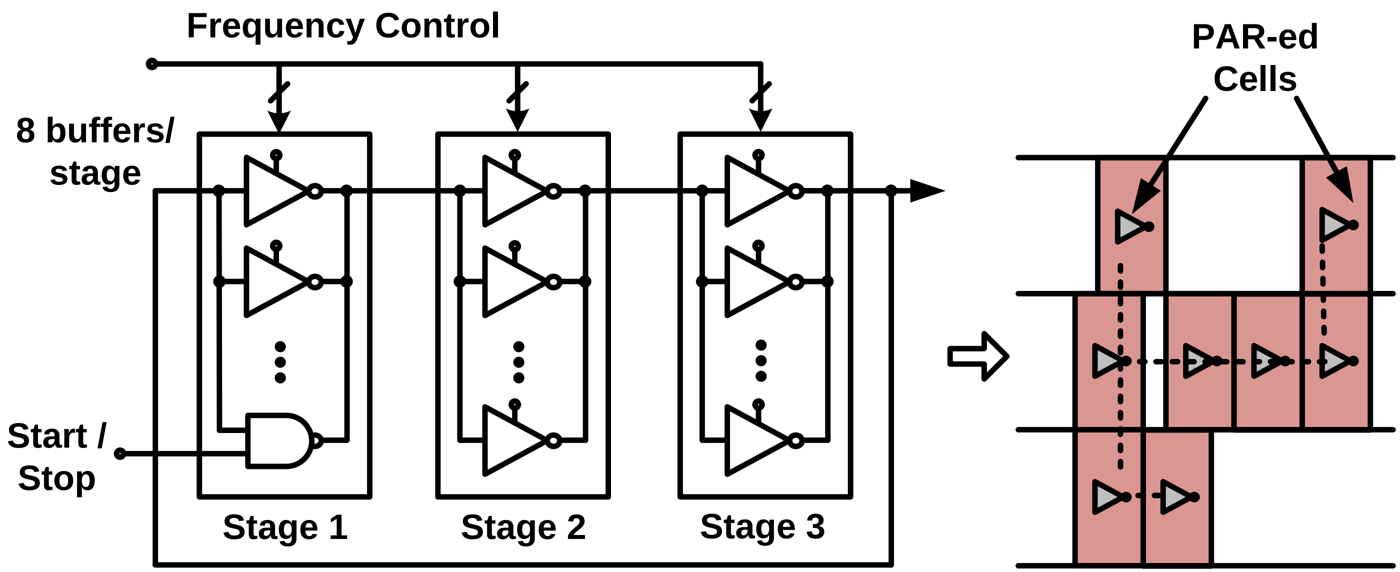
- **Digitally controlled frequency**
  - Reconfigurable coarse/fine resolution



Reconfigurable TDC performance

Digitally Controlled Oscillator

- **Implemented with standard cells**
  - Parallel tri-state buffers



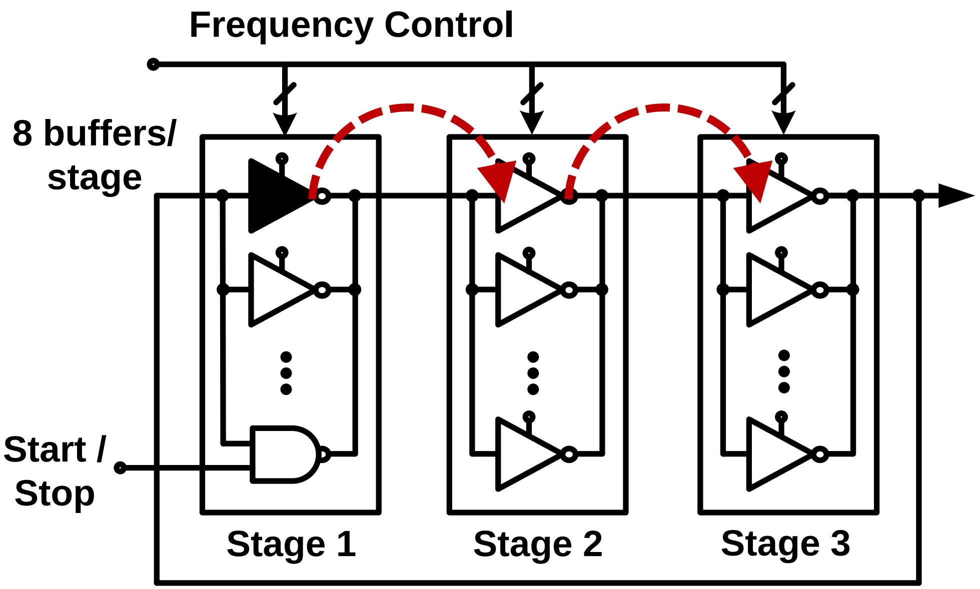
Cell-based DCO :
Automatic PAR, portable to other designs

Effective Drive Strength

- **Effective drive strength is measured by built-in counters**

Turning off each buffer increases period by different amount

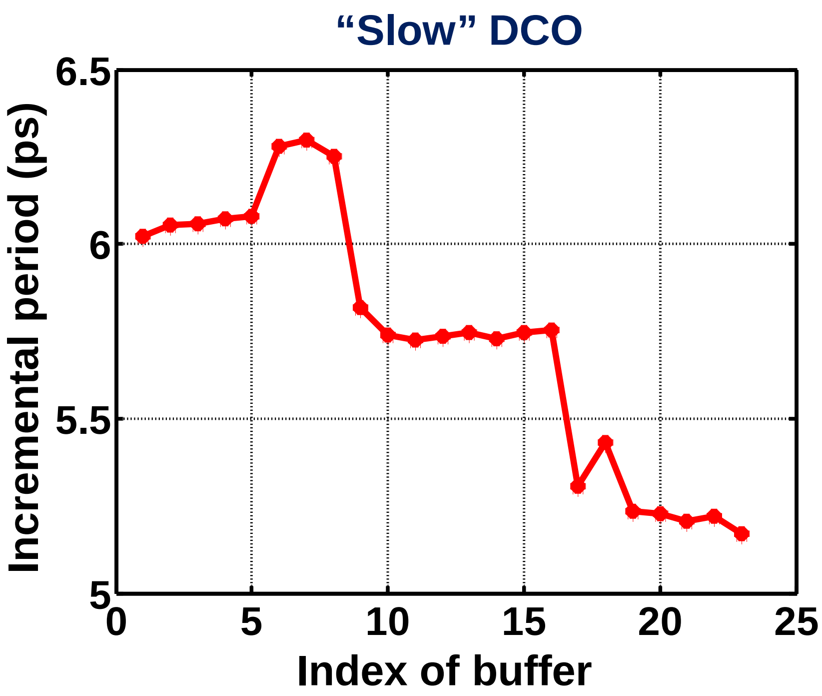
"Effective drive strength"

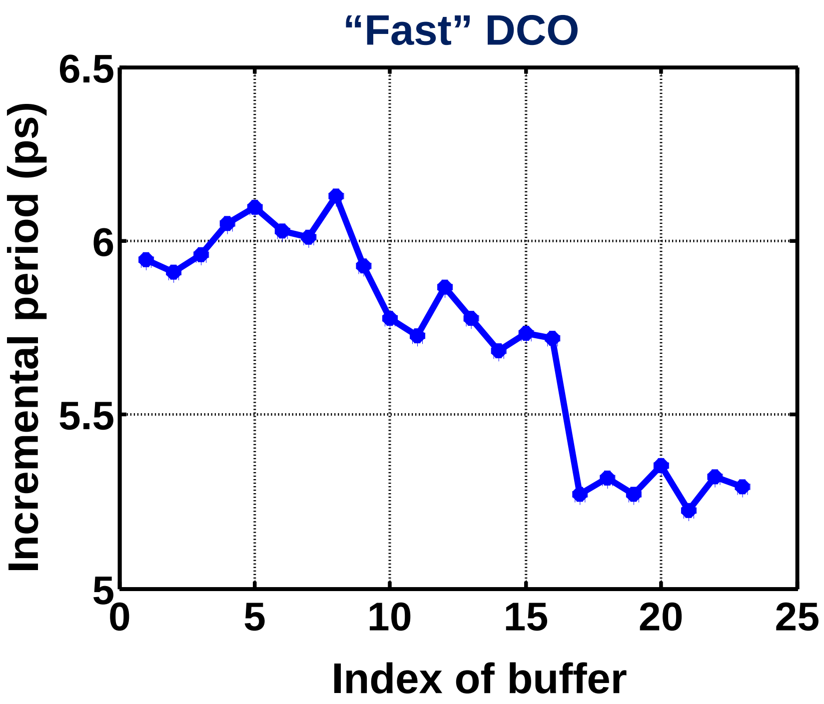


Each buffer has different drive strength due to automatic PAR

Measured Incremental Period

- **Systematic mismatch observed**

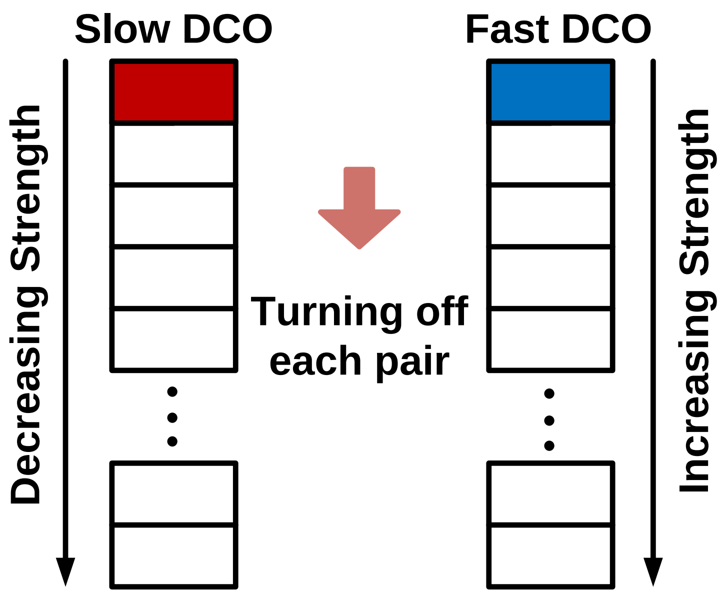


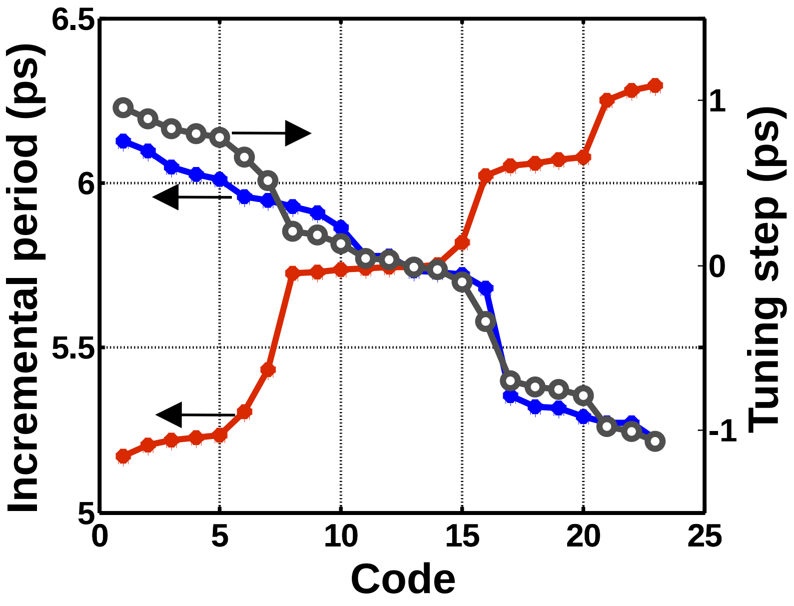


Utilized for calibration

Calibration of TDC Fine Step Resolution

- **Buffers are sorted based on measured drive strength**
  - Provides a simplified calibration scheme

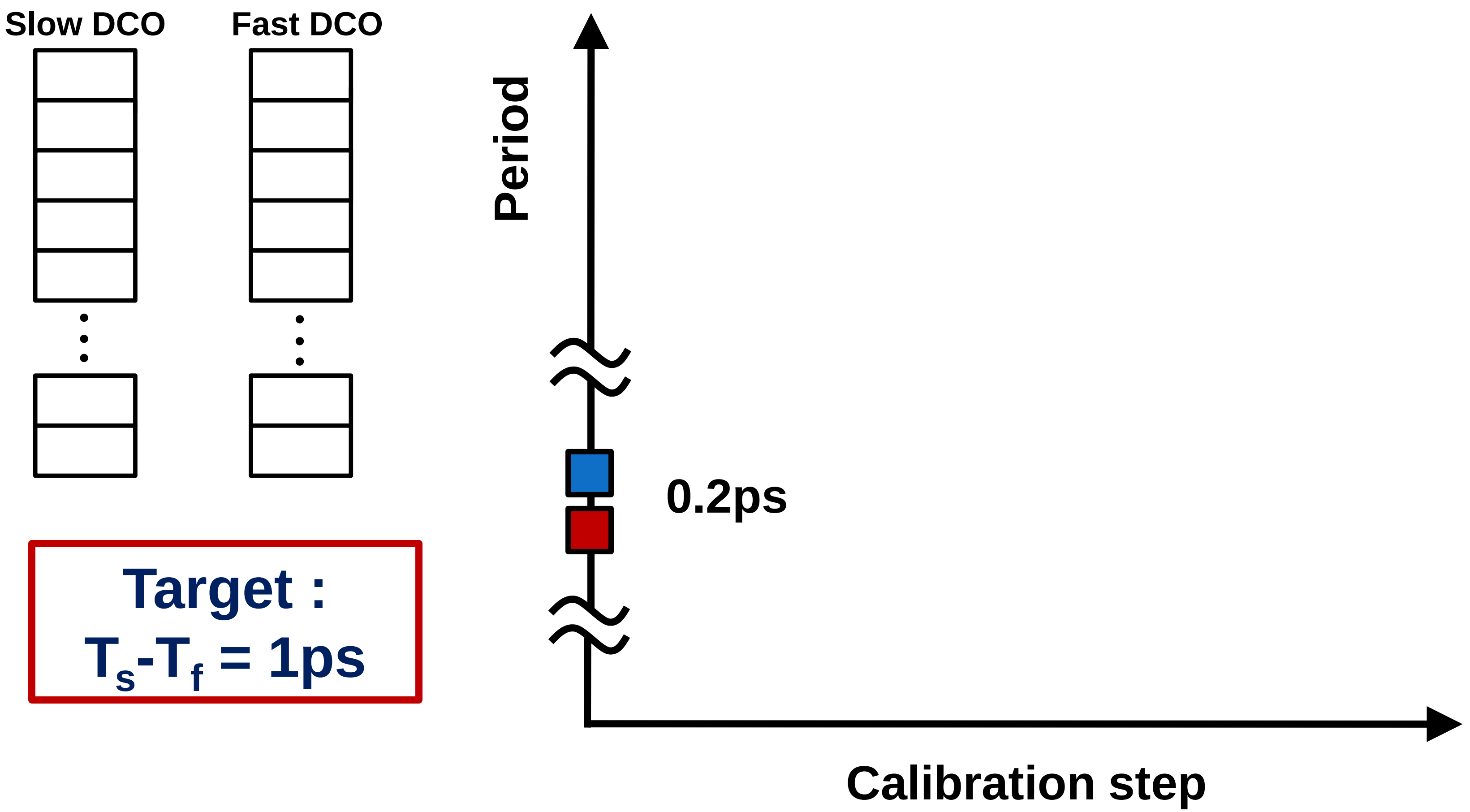




Calibrates T_s - T_f

Calibration Example

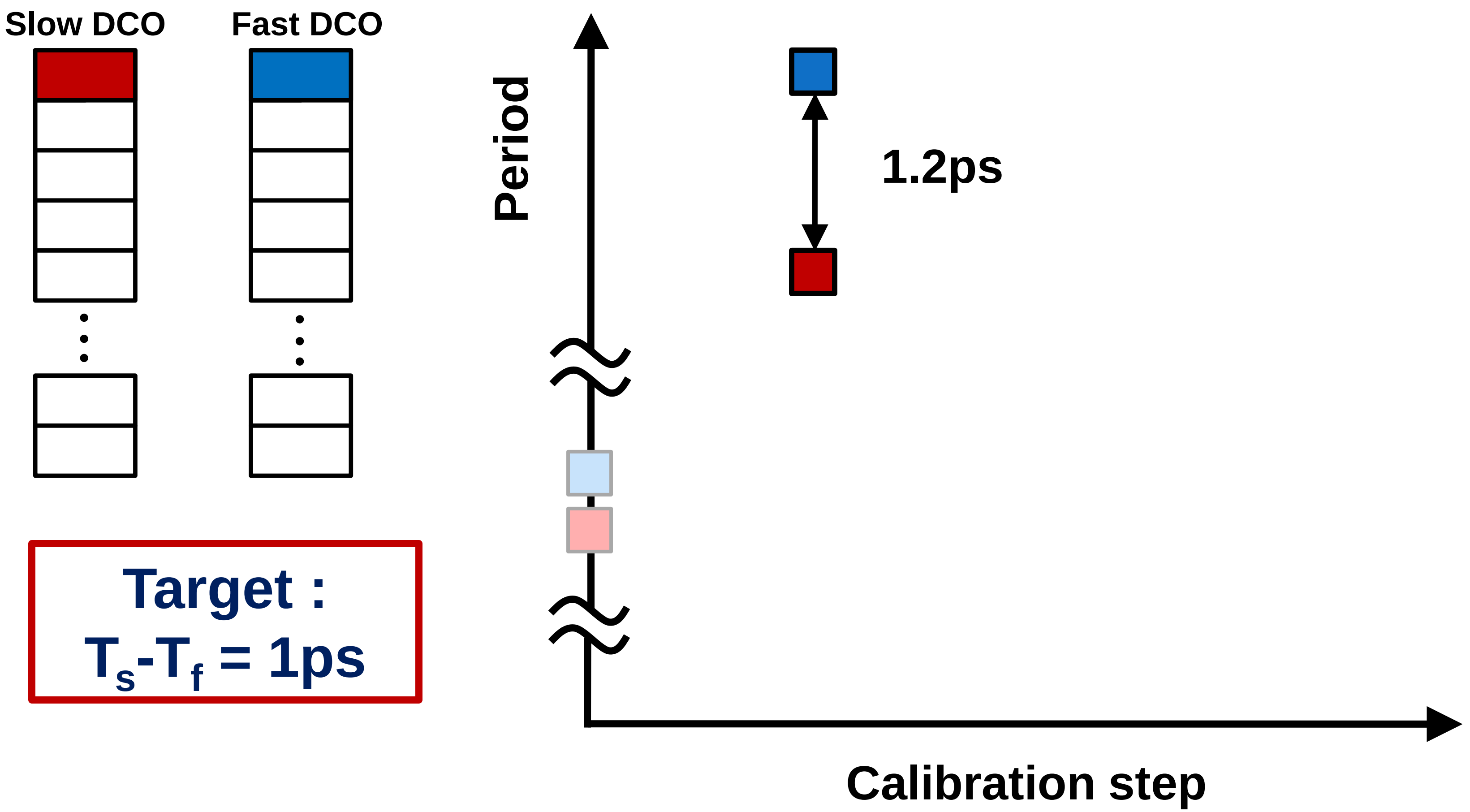
- **Fine step resolution calibrated**
  - Initial mismatch is observed



Target :
T_s-T_f = 1ps

Calibration Example

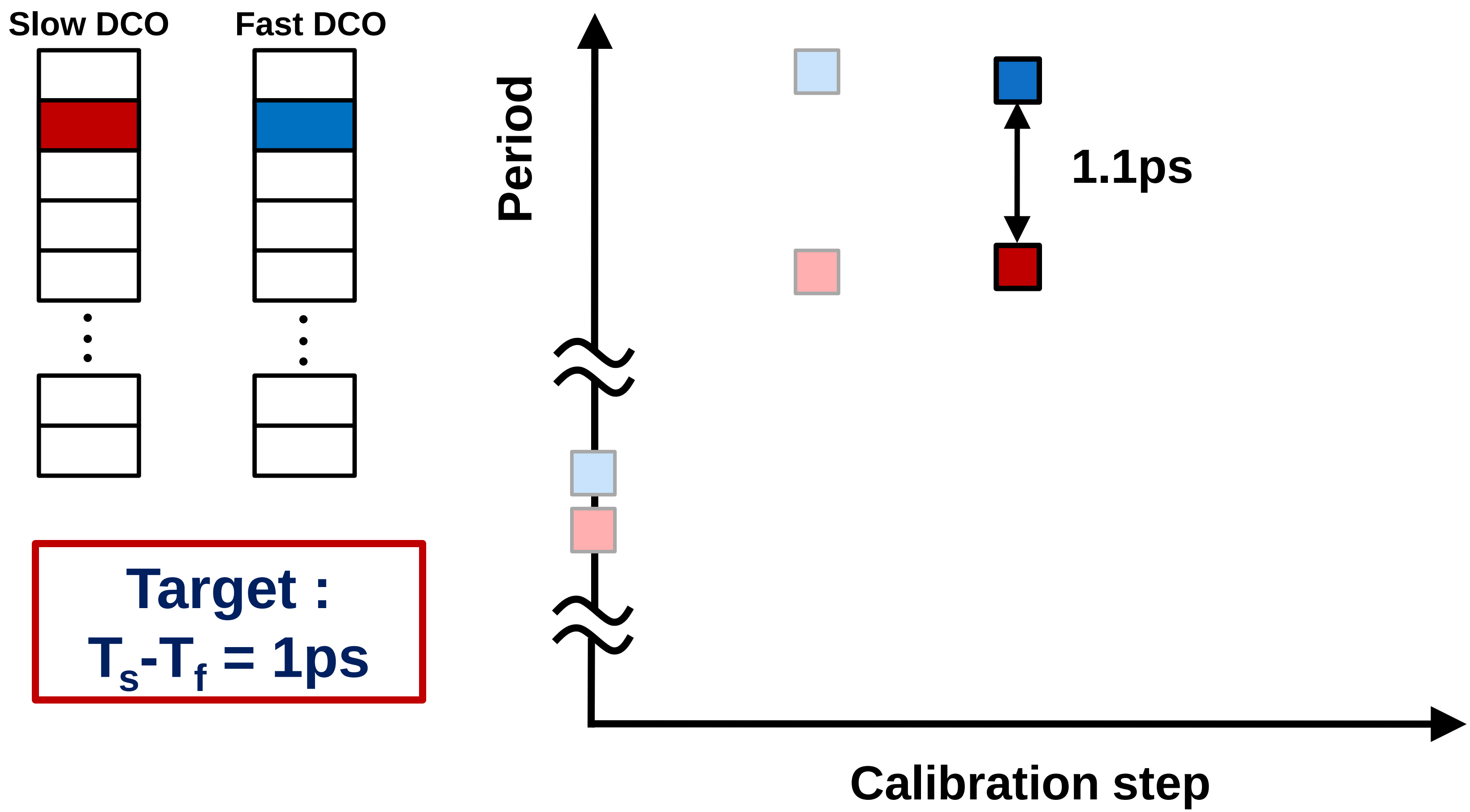
- **Fine step resolution calibrated**
  - 1st pair is turned off



Target :
T_s-T_f = 1ps

Calibration Example

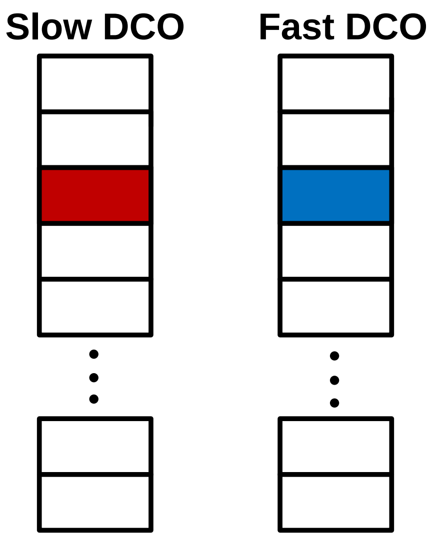
- **Fine step resolution calibrated**
  - 2nd pair is turned off

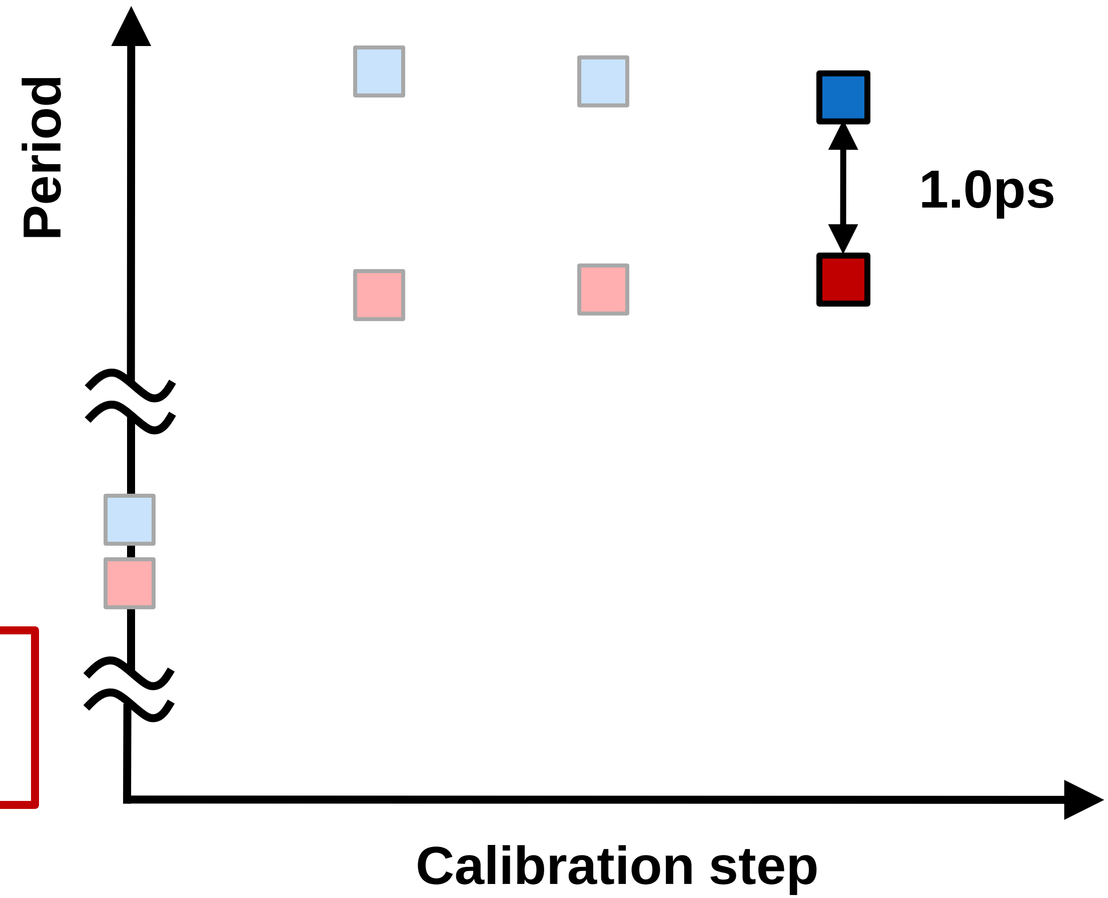


Target :
T_s-T_f = 1ps

Calibration Example

- **Fine step resolution calibrated**
  - **3rd pair is turned off**

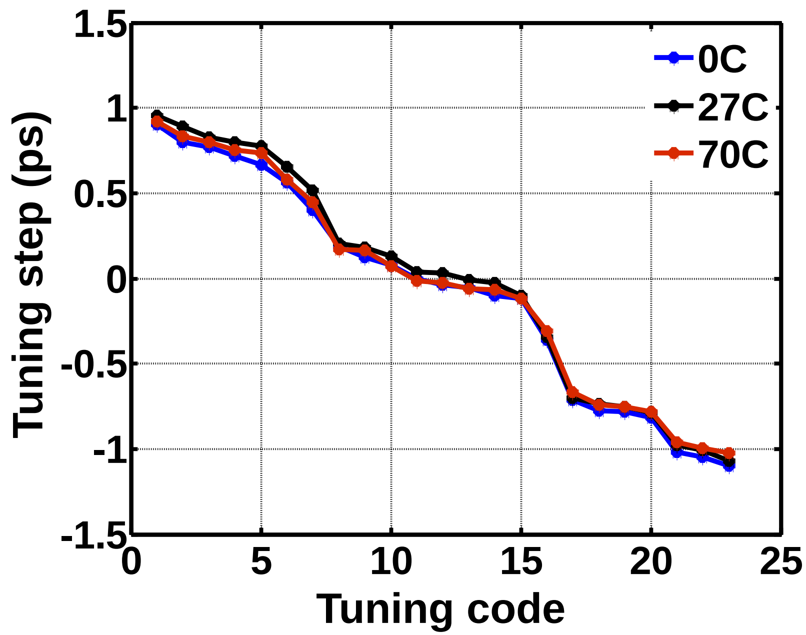


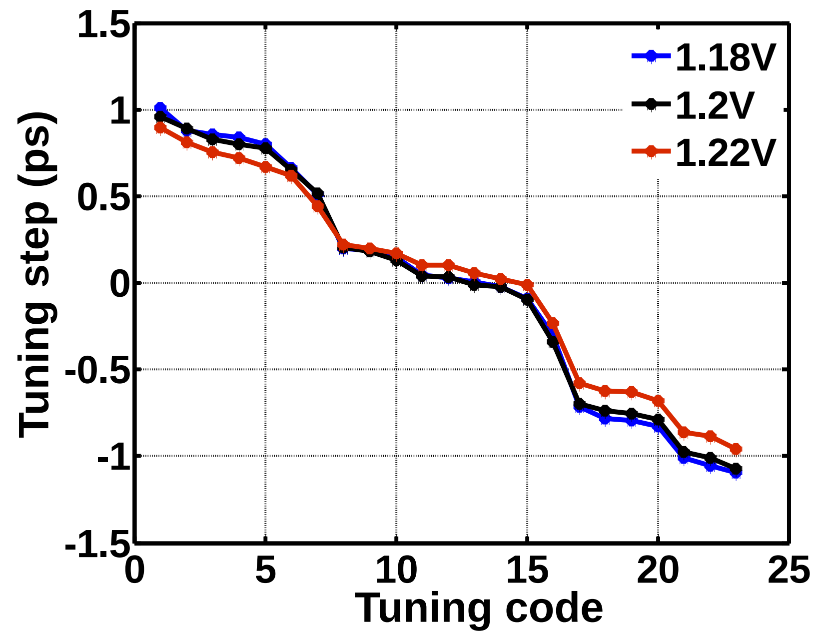


Fine & monotonic steps

Temperature/Supply Variation

- **Tuning steps over temperature/supply variation**

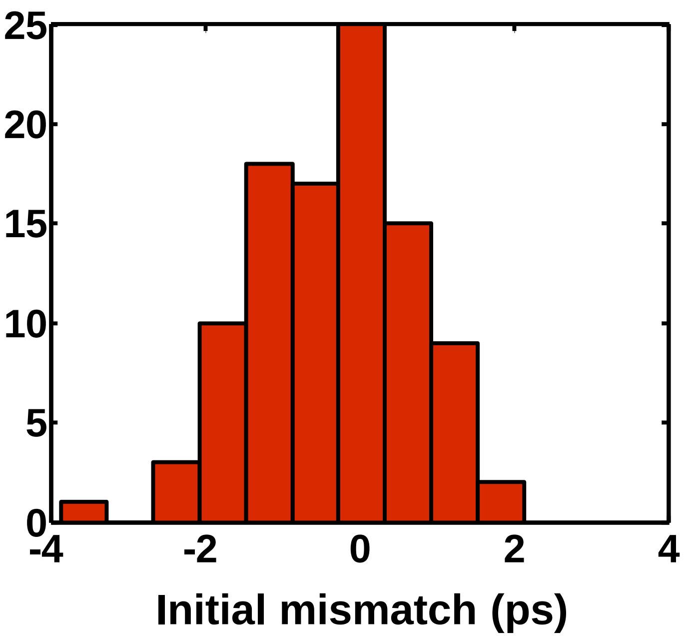


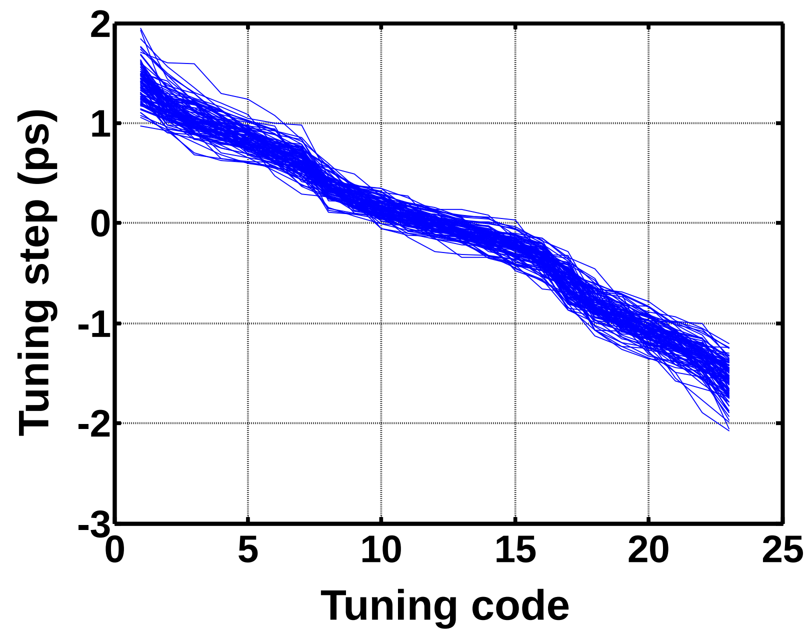


Tuning step is invariant over temperature/supply variation

Process variation

- **Monte Carlo simulation over process variation**

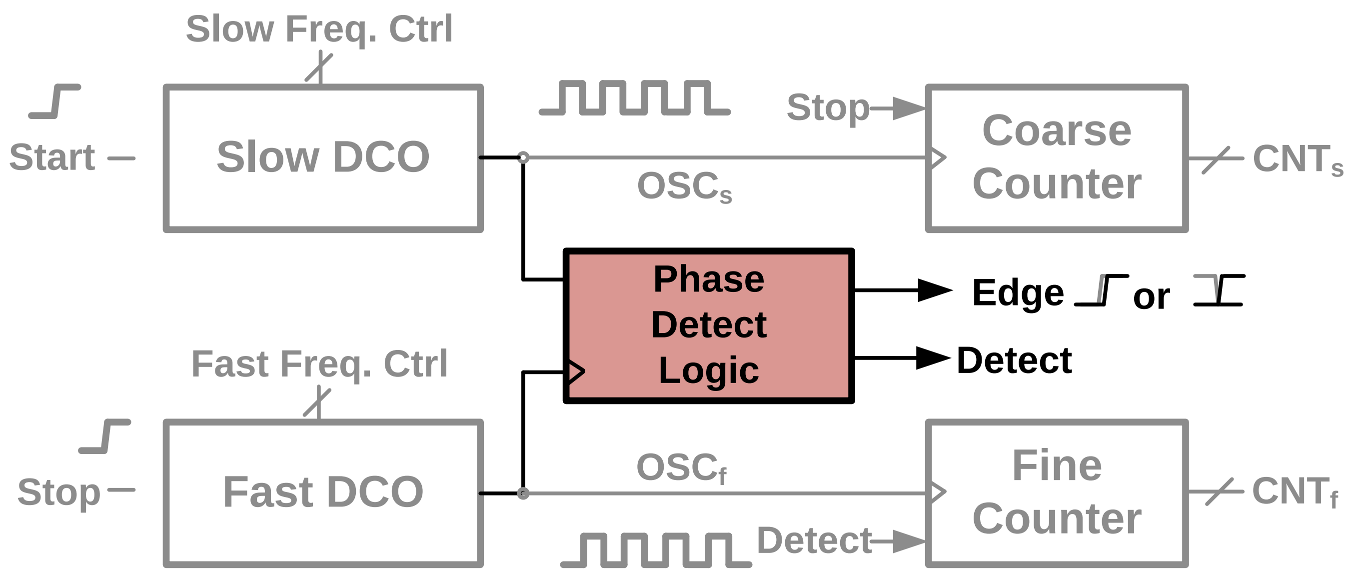




TDC resolution can be tuned over process variation

Phase Detect Logic

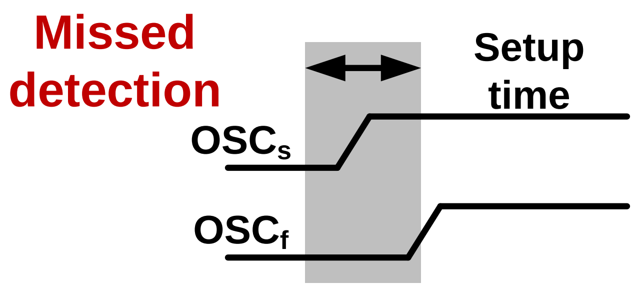
- **Both rising/falling edges detected**
  - Flip-flop and logic circuit

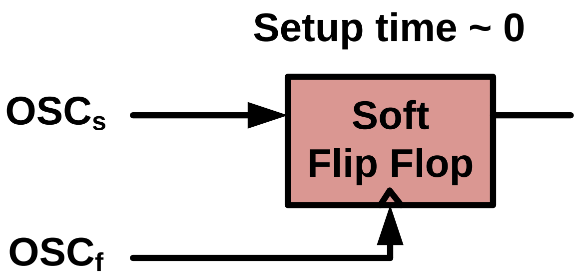


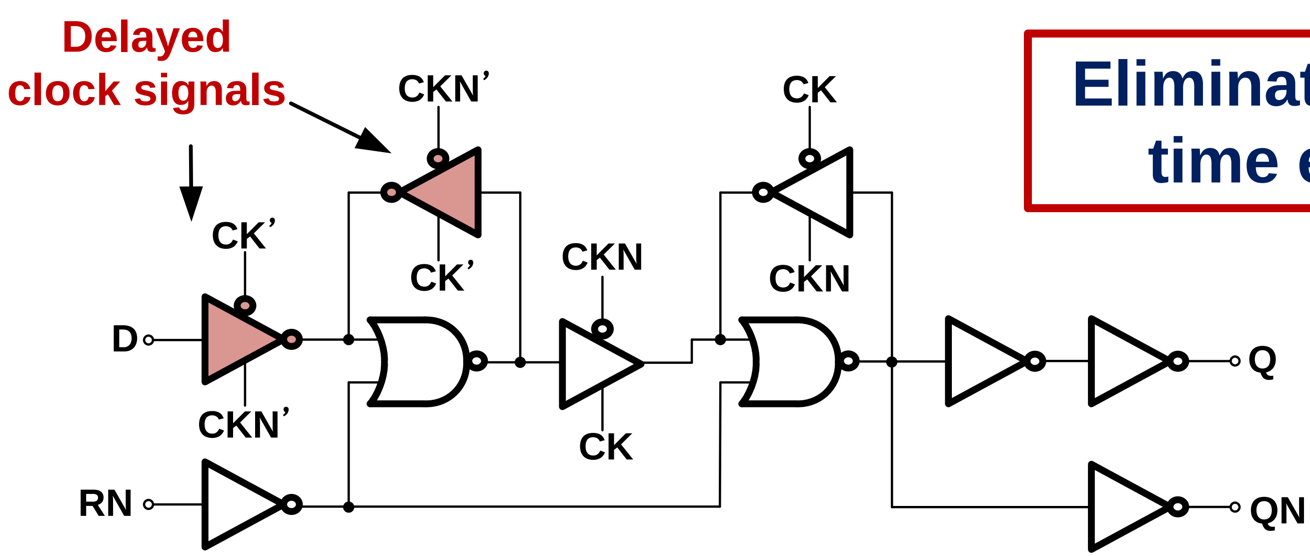
Reduces required fine step range, thus power consumption

Soft Flip-Flop

- **Cannot detect edge within setup time of standard FF**



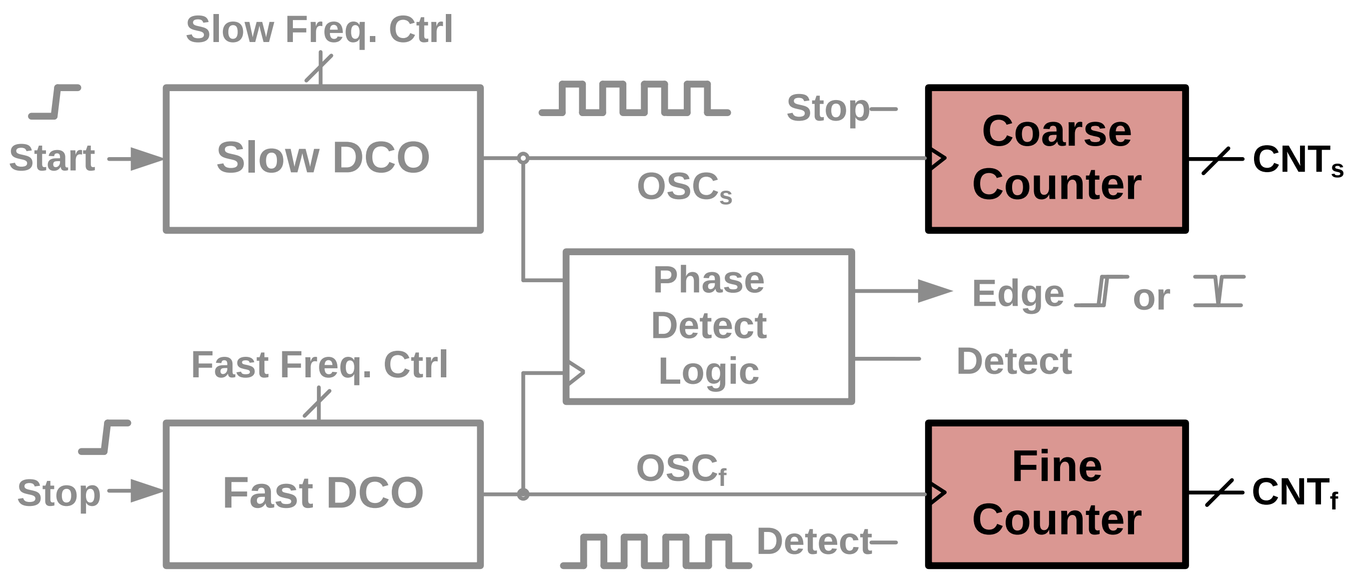




Eliminate setup time effect

Counters

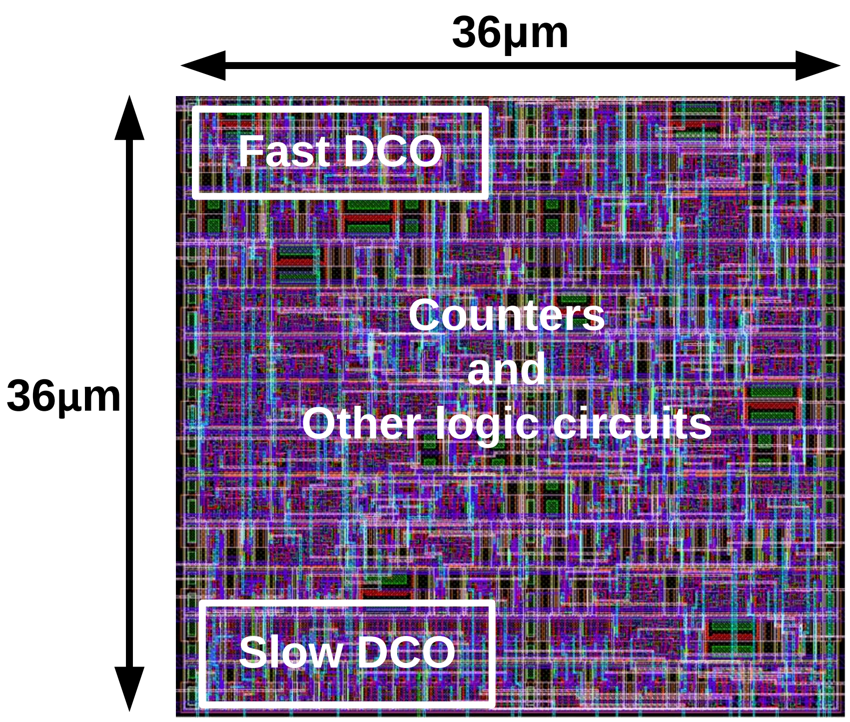
- **Counts coarse/fine oscillations**
  - **In calibration mode, measure frequency, drive strength**



Typical digital block

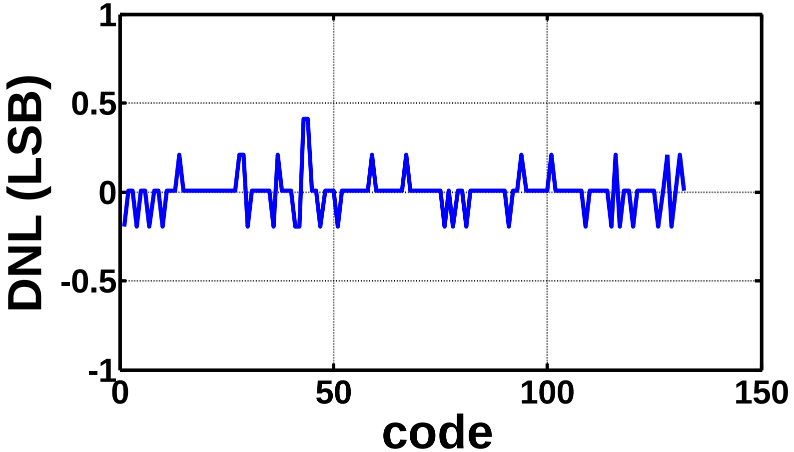
Automatic Place & Route

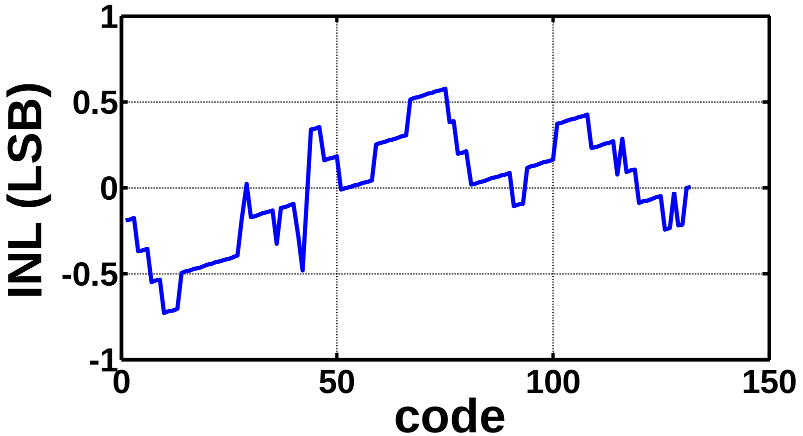
- **All functional blocks are implemented with standard cells and automatically laid out**
  - **Can follow digital circuit design flow**



**Automatic PAR :
Simplified design,
higher integration**

TDC Performance





Process	65nm CMOS
Technique	Cyclic Vernier
Resolution*	1ps
DNL/INL (LSB)	0.5 / 0.8
Power (mW)**	0.01 – 0.15
Area (mm^2)	0.001

* Calibrated at 1ps

** Power @ 1MHz sampling freq.

Both are reconfigurable

Conclusions

- High resolution, small area TDC
  - Cell-based design flow
  - Calibrated based on effective drive strength

	This work	Lee JSSC 08	Straayer JSSC 09	Henzler ISSCC 08
Process	65nm CMOS	90nm CMOS	130nm CMOS	90nm CMOS
Technique	Cyclic Vernier	Time Amp.	Gated RO	Passive Interpol.
Resolution	1ps	1.25ps	6ps	4.7ps
Power*(mW)	0.01-0.15	0.3	0.06-0.6	20
Area (mm^2)	0.001	0.6	0.04	0.02

*Normalized at 1MHz