An All-Digital 12 pJ/Pulse IR-UWB Transmitter Synthesized From a Standard Cell Library

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***Abstract*—This paper presents an all-digital impulse radio ultra-wideband (IR-UWB) transmitter. All functional blocks in the transmitter are implemented with digital standard cells and automatically place-and-routed by design tools. The center frequency and the bandwidth of the UWB pulses are digitally tuned to compensate for variations, or target different applications. This paper also proposes a calibration scheme and modeling of a cell-based digitally controlled oscillator (DCO), which takes systematic mismatch from automatic place-and-route into account. The transmitter is fabricated in a 65 nm CMOS process, and occupies a core area of 0.032 mm^2. The transmitter operates in the 3.1–5.0 GHz UWB band with leakage power of 170 μW and active energy consumption ranges from 8 pJ/pulse to 16 pJ/pulse, which combine to a total minimum energy/pulse of 12 pJ/pulse at 50 Mb/s.**

***Index Terms*—All-digital, impulse radio (IR), standard cell, synthesis, transmitter, ultra-wideband (UWB).**

I. Introduction

RECENT process scaling is driving digitally intensive implementations of conventional analog circuits. While analog circuits suffer from the reduced voltage headroom of scaled CMOS and large passive component area, digital implementations of analog circuits thrive in scaled CMOS by leveraging the high timing accuracy, and reduced die area and manufacturing cost. Also, compatibility with other digital circuits enables higher system integration. All-digital phase locked loops (ADPLLs) [1]–[5] have been an active research area recently, and have shown the advantages of digitally intensive implementations. In ADPLLs, signals are digitized and processed in the time domain with the high time resolution of digital circuits, achieving small area, low power, and low cost implementations. Other applications include digitally intensive analog-to-digital converters (ADCs) [6]–[8]. By adopting digital calibration schemes, the ADCs relax the complexity of analog parts, thereby reducing the power consumption of the systems.

Another advantage of all-digital implementations is that more circuit blocks are absorbed in the *digital design flow*. The design procedure of digital logic circuits has become highly automated so that the synthesis, layout and verification of the circuits are done with design tools. Analog circuits, on the other hand, require comprehensive characterization of devices to achieve a target performance. Moreover, the performance is highly dependent on the layout so that a fully custom layout is required. While this custom design procedure has been amenable to small analog circuit blocks, it can be costly as the circuits become highly integrated. Therefore, it is commercially advantageous to have more analog functions implemented digitally, and that the design of the circuits is highly automated with current design tools.

This paper presents an all-digital impulse radio ultra-wideband (IR-UWB) transmitter which is synthesized from a CMOS standard cell library, leveraging design automation technologies. IR-UWB provides several characteristics favorable to all-digital transmitter architectures. First, IR-UWB signaling is inherently duty-cycled. The width of UWB pulses in the time domain is short ($\sim$2 ns), while the pulse rate is relatively low. That is, most of the time, the transmitter does not produce pulses. By implementing all-digital architectures, the functional blocks can be turned off between pulses, thereby consuming only leakage power. This significantly reduces power consumption in all-digital transmitters. Second, IR-UWB is operated in non-coherent communication by applying pulse position modulation (PPM) or on-off keying (OOK). Non-coherent communication relaxes frequency tolerance enough that typical accuracy specifications can be satisfied by the time resolution of recent digital circuits. Recently published all-digital UWB transmitters [9]–[13] take advantage of these characteristics to achieve low power and low cost architectures.

The proposed transmitter is not only implemented in an all-digital architecture, but it is also implemented with standard cells in the automated design procedure. Standard cells are pre-defined building blocks that are available in most commercial CMOS process technologies. Though standard cells are less flexible to implement circuits with, the simulation, synthesis and layout of the cell-based circuits are highly automated with current design tools. Since all functional blocks in the proposed transmitter are implemented with standard cells and automatically place-and-routed, the design procedure is significantly simplified, and a compact layout is derived. Also, by adopting advanced CMOS technologies, the proposed transmitter achieves a low power and small area, benefitting from process scaling.

The cell-based design of the transmitter, however, imposes several challenges. Unlike custom layout, automated layout causes systematic mismatch in the radio frequency (RF) signal paths. Also, since standard cells are minimally sized, the cell-based circuits are relatively susceptible to process, voltage

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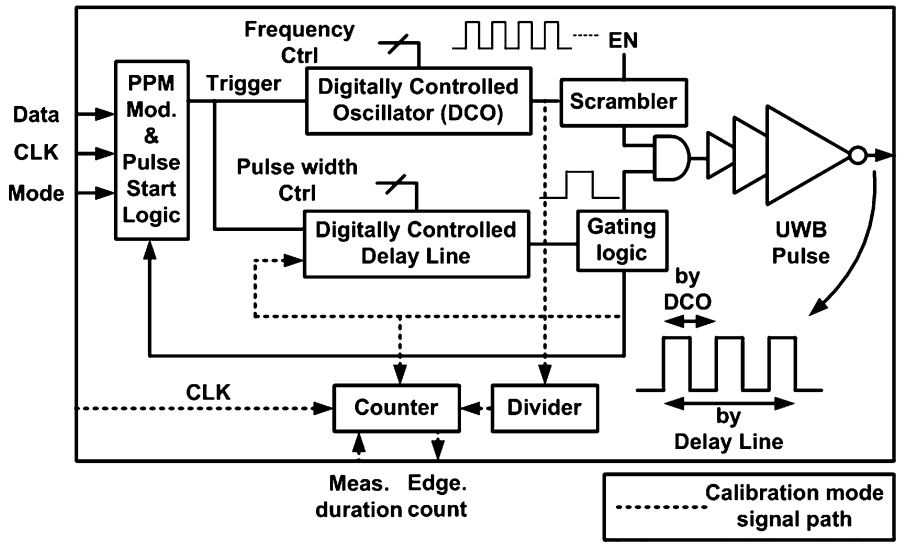

Fig. 1. Block diagram of proposed UWB transmitter.

and temperature (PVT) variations. To address these challenges, the transmitter provides a wide range of center frequency and bandwidth of the UWB pulses which can be calibrated with high resolution. With sufficient flexibility, the transmitter can compensate the systematic mismatch and variations, and target different applications. This paper proposes a calibration scheme taking the systematic mismatch into account, and derives a timing model to enhance automated design flow for the cell-based transmitter.

The remainder of this paper is organized as follows. Section II describes the proposed all-digital transmitter architecture, and Section III proposes a calibration scheme of a cell-based digitally controlled oscillator (DCO) to compensate mismatch and variations, or target several specifications. Then, Section IV explores a timing modeling of the DCO to simplify the verification of the transmitter. Section V presents the measured performance of the UWB transmitter, and Section VI concludes this paper.

II. UWB Transmitter Architecture

A block diagram of the proposed UWB transmitter is shown in Fig. 1. According to incoming data, a PPM modulator asserts a trigger edge in a modulated time slot, which activates both a DCO and a delay line. When activated, the DCO oscillates at a programmable frequency, and an edge propagates through the programmable delay line. When the edge arrives at the end of the delay line, the DCO output is gated. The frequency of the DCO and the delay through the delay line are digitally controlled by the frequency control word and pulsewidth control word, respectively. In this way, the center frequency and bandwidth of UWB pulses are separately controlled. The output of the delay line is also used to disable the DCO to save power between pulses, utilizing the duty-cycled nature of IR-UWB. The pulse start logic detects the edge at the output of the delay line, and disables the DCO until the next trigger edge is asserted. A scrambler is used to mimic delay-based binary phase shift keying (DB-BPSK) [14] by scrambling the pulses. In a PPM modulated spectrum, UWB pulses have spectral lines, which limits the transmit power. With low hardware complexity, the scrambler reduces the spectral lines, maximizing the transmit power within the FCC mask.

The transmitter provides a calibration mode where the center frequency and bandwidth of the pulses are measured, and tuned for target performance. During the calibration mode, the DCO is continuously enabled, and its frequency is measured by counting cycles over a time period. A frequency divider, which is a chain of flip-flops, is inserted to reduce the frequency of DCO output before the relatively slow counter. To calibrate the bandwidth of the UWB pulses, the delay line is configured as a loop, and the frequency around the delay line is measured with a similar technique. The counter values for the DCO and the delay line indicate the current center frequency and the bandwidth of the UWB pulses, and the digital control codes are adjusted according to target values.

A. Digitally Controlled Oscillator With Tunable Delay Cells

The core building block of the cell-based UWB transmitter is a tunable delay cell. Fig. 2 shows the structure of a DCO using the tunable delay cells. Each delay cell is implemented with multiple inverting tri-state buffers connected in parallel. The first stage includes a NAND gate and one less buffer to disable the DCO when necessary. While the load capacitance at the output of the delay cell is fixed by the number of buffers and the wiring between the buffers, the drive strength of the delay cell is controlled by turning on a different number of buffers. The minimum delay is obtained when every buffer is turned on, then the delay (ΔT) is tuned by turning off buffers, reducing the drive strength. The tuning range and the resolution of the delay are functions of the number of buffers (N) in the delay cells. As the number of buffers increases, the tuning range is increased, and the resolution is improved; however, power consumption is also increased. Therefore, there is a tradeoff between the tuning performance and the power consumption. According to a target DCO performance, the number of buffers can be determined in the design phase using the model proposed in Section IV. The DCO in the transmitter was designed to have three stages to

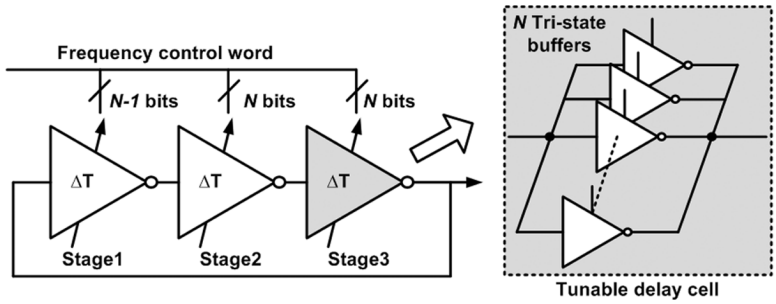

Fig. 2. Digitally controlled oscillator embedding tunable delay cells.

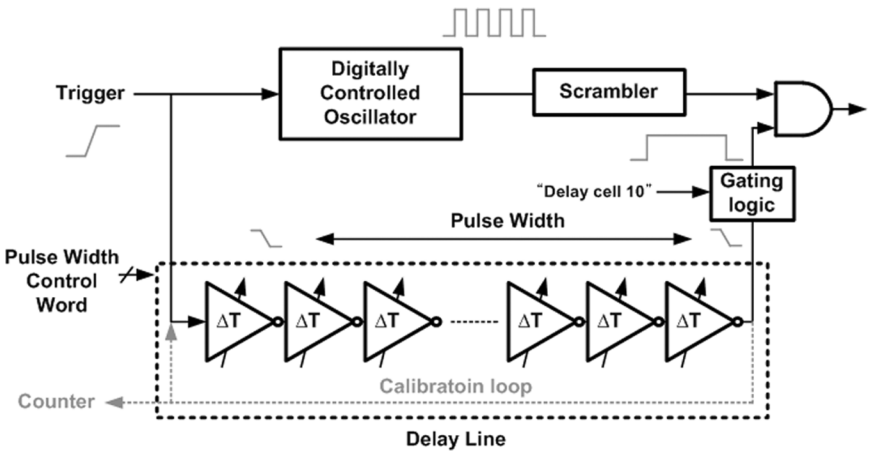

Fig. 3. Delay line embedding tunable delay cells.

generate an oscillation frequency ranging from 3.1 to 5.0 GHz, and each stage has 31 (in the first stage) or 32 buffers to achieve sufficient resolution for non-coherent UWB communication.

Instead of custom, symmetric layout to achieve desired performance, buffers in the DCO are distributed and routed by an automatic layout tool. This method significantly simplifies the design procedure of the DCO, and enables a complete integration with other cell-based digital blocks. The automatic layout also provides a useful redundancy which can be utilized for the DCO frequency control. In an ideal symmetric layout, each buffer in the delay cell is considered to be identical, and have the same effect on the drive strength control. In the proposed DCO, on the other hand, each buffer is uniquely placed-and-routed, having a different and unique effect on the drive strength. Theoretically, the number of frequency configurations is exponential to the number of buffers, thus higher tuning resolution can be obtained when an appropriate calibration scheme is employed. In Section III, a simple and monotonic calibration scheme utilizing the redundancy is proposed.

B. Pulse Width Delay Line

Fig. 3 shows the structure of the delay line that employs tunable delay cells. A trigger edge from the PPM modulator propagates through the delay line, and the edge at the output of the delay line gates the DCO output to an antenna, thereby determining the width of the UWB pulses. In the transmitter, the delay line has 57 tunable delay cells, and each delay cell is implemented with five parallel tri-state buffers to cover a desired pulsewidth range. Among the 57 stages in the delay line, the

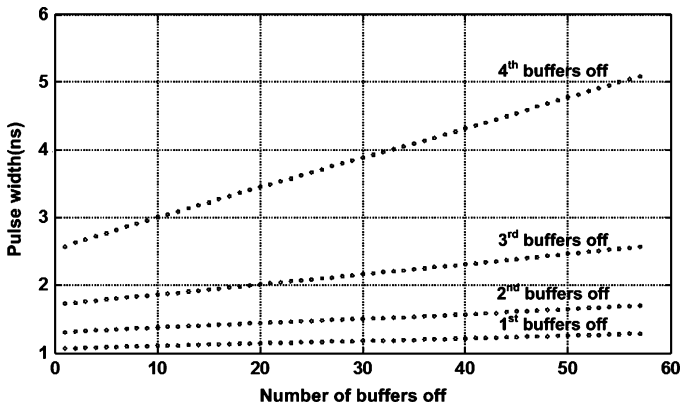

Fig. 4. Measured programmable pulsewidth range. By turning off tri-state buffers in the delay line, the pulsewidth is increasing.

first 10 stages are used to block unavoidable power supply transients when the DCO is turned on. To prevent this transient from impacting the pulsed output, the gating logic turns on the DCO output only while the edge in the delay line is propagating between stage 10 and stage 57. By controlling the delay in the first 10 stages, we can control the time which the transmitter waits for the supply voltage transients to settle. The pulsewidth of the UWB pulse is controlled with the remaining 47 stages. Fig. 4 shows the measured pulse widths of the transmitter. When every buffer is turned on in the 47 stages, the pulsewidth is shortest, and the pulsewidth is increased by turning off the buffers. In the first section in Fig. 4, only one buffer is turned off in each

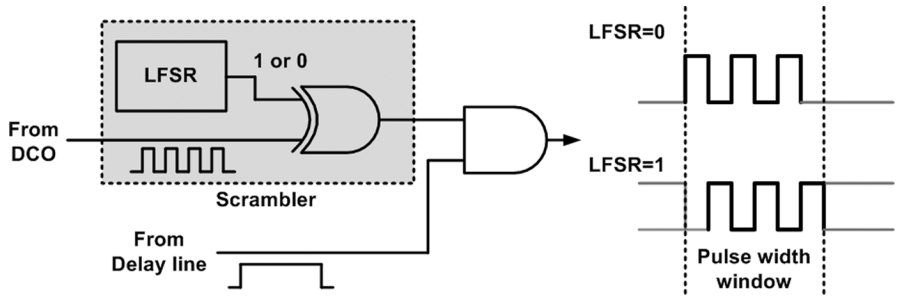

Fig. 5. Delay-based BPSK scheme with scrambler.

delay cell, and additional buffers are turned off for the next sections. Since the delay cells have five buffers, there are four sections, whose values range from 1.1 ns to 5.1 ns. Since the bandwidth of UWB pulses is required to be higher than 500 MHz, the fourth section is used only when the delay line is significantly affected by PVT variations. The resolution of the pulsewidth control varies (from 4 ps to 47 ps), based on the number of buffers off in each delay cell. A wide range of pulse widths, calibrated with high resolution, is useful to compensate systematic mismatch and PVT variations, or target different applications. For instance, in a multiple-channel communication, the pulsewidth is tuned to be wide, while the pulsewidth is tuned to be short for single-channel communication.

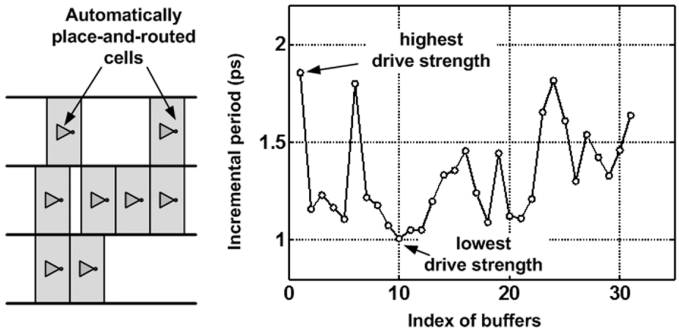

Fig. 6. Description of cell-based layout and measured incremental periods of buffers in stage 1.

C. Scrambler

PPM modulation has been popular in IR-UWB communication, offering reduced system complexity over BPSK. Pulse generation in PPM modulation reduces power and area, while BPSK requires functional blocks dissipating static power, and/or large passive components. Also, PPM modulation allows non-coherent communication where receivers also have low complexity and power efficiency. A spectrum in PPM modulation, however, contains spectral lines which are $10\log(\mathrm{PRF}/1\ \mathrm{MHz})$ dB above the BPSK spectrum [15], where PRF is the pulse repetition frequency. Since the power spectrum of UWB signaling is limited by the FCC mask, the maximum transmit power in PPM modulation must be lowered by this factor.

In the proposed transmitter, a scrambler is used to reduce the spectral lines in the PPM spectrum by scrambling pulses. The scrambler consists of a linear feedback shift register (LFSR) and an XOR gate. Between the pulses, the LFSR generates a bit, which is 1 or 0, and the output of the DCO is XOR-ed with the LFSR bit. As shown in Fig. 5, the output pulse is shifted by a half cycle when the LFSR bit is 1. When filtered by an off-chip high-pass filter, the combined effect is equivalent to DB-BPSK [14], which is transparent to a non-coherent receiver. Feedback taps in the LFSR are digitally configurable, and a 16 bit maximum length LFSR is configured in the transmitter.

III. Calibration of DCO

All functional blocks in the transmitter, including the DCO and the delay line, are implemented with standard cells, and automatically place-and-routed. This cell-based design methodology significantly simplifies the design procedure, and allows higher system integration. Though the characterization of the circuit performance at the design phase becomes difficult due to systematic mismatch and susceptibility to variations, the proposed DCO provides a wide range of frequencies which are finely tunable with a digital calibration scheme. The proposed calibration scheme takes advantage of the systematic mismatch due to buffer placement and wiring, which is represented as the *effective drive strength*.

As shown in Fig. 2, the DCO is implemented with tunable delay cells, and buffers in the delay cells are connected in parallel. If all buffers are completely matched (e.g., through custom layout), the delay is only a function of the number of buffers enabled. In the cell-based DCO, however, the buffers are automatically place-and-routed, which imposes systematic mismatch between buffers. Therefore, each buffer has a unique effect on the delay, allowing higher resolution by turning on different sets of buffers. Though the characterization of the systematic mismatch is difficult to obtain in the design phase, it can be analyzed and utilized with the proposed calibration of the DCO.

When all buffers are enabled, the DCO oscillates at its maximum frequency. If only one buffer is turned off, the DCO period slightly increases. We refer to this increase in period as the *incremental period*, which is different for each individual buffer, implying that each buffer has an *effective drive strength*. In the calibration mode, the on-chip counter is used to measure the *incremental period* for every buffer. Fig. 6 shows the measured *incremental period* for each buffer in stage 1 of the DCO, highlighting the systematic mismatch between the buffers. If all buffers were matched, Fig. 6 would have resulted in a flat line.

Since the number of frequency configurations is exponential to the number of buffers when the drive strength is different between buffers, a simple and monotonic calibration scheme is

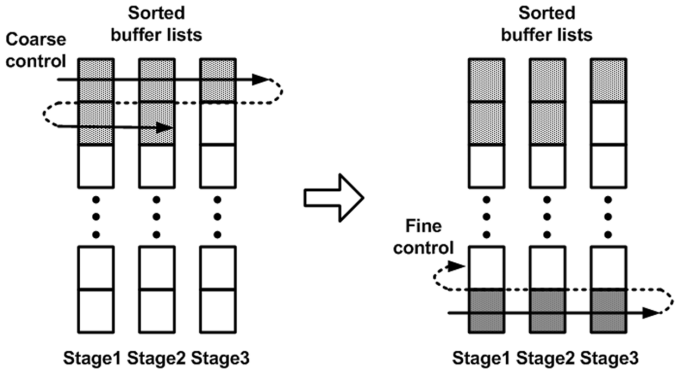

Fig. 7. Description of calibration scheme with sorted lists.

required for practical use of the systematic mismatch. Fig. 7 illustrates the proposed calibration scheme. Once the *incremental periods* for each buffer are measured, the buffers are sorted according to their *effective drive strengths*. If the buffers are turned off in order beginning with the highest drive strength, the frequency decreases rapidly as shown by the lower limit line in Fig. 8 (top). Turning off the buffers in order beginning with the smallest drive strength decreases the frequency slowly, as shown by the upper limit line in Fig. 8. These two controls determine the upper/lower limits of the DCO frequencies, and we can achieve a coarse/fine calibration strategy between the limits by reordering the buffers to be turned off. First, a coarse frequency band is selected by turning off buffers with higher drive strengths until a desired band is reached, then, buffers with lower drive strengths are turned off to finely tune the frequency in this band. This is illustrated by the solid black lines in Fig. 8. The advantage of this scheme is that we can finely tune the frequency around target values, which is possible due to the mismatch in the *effective drive strength* of each buffer. Also, the proposed calibration scheme guarantees monotonic tuning of the frequency.

To study the impact of the number of buffers-per-stage on center frequency resolution, we implemented two 3-stage DCOs, one with 32 buffers-per-stage, and one with 64. Fig. 8 shows the measured frequency control of these two DCOs. When 64 buffers are embedded in each stage, and automatically place-and-routed, the incremental period of each buffer is reduced, and the distribution of the incremental periods is widened. This results in higher resolution, and clear coarse/fine tuning of the frequency as show in Fig. 8 (top). In the DCO with 32 buffers-per-stage, the incremental period is higher, and more evenly balanced between buffers, which results in deteriorated resolution as shown in Fig. 8 (bottom). The measured frequency resolutions are 10 MHz for the DCO with 64 buffers-per-stage, and 50 MHz for the DCO with 32 buffers-per-stage. The IR-UWB transmitter in this paper adopted the DCO with 32 buffers-per-stage because it provides a more compact layout, lower power and higher maximum frequency. Furthermore, the 50 MHz resolution is adequate for non-coherent PPM [16], resulting in only 0.02 dB loss.

The above coarse/fine calibration scheme requires a consistent *order* of the buffers' *incremental period* over supply voltage and temperature variations, even though the absolute value of *incremental period* may vary. In cell-based circuits, however, the relative ordering of buffers' drive strength is dominated by systematic mismatch due to routing. In other words, the ordering of buffers depends mostly on the mismatched wiring, and the order is not affected by other variables such as device mismatch, supply voltage or temperature. To verify this, Fig. 9 shows the *incremental periods* of the buffers in stage 1 over four chips, and Fig. 10 shows the *incremental periods* over different supply voltages and temperatures. Though the absolute values of the *incremental period* change, the order of buffers in stage 1 is relatively consistent over the variations. Therefore, the order of the buffers' drive strengths are measured only once, after which they can be used to tune the frequency regardless of voltage or temperature variation during the calibration mode. This significantly simplifies the implementation of the calibration.

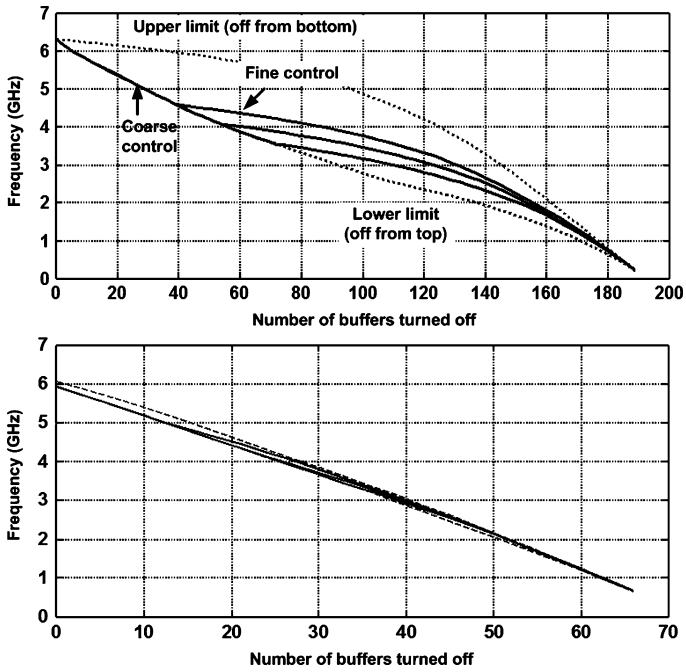

Fig. 8. Measured frequency control with sorted lists in DCO employing delay cells with 64 buffers, operating at 1 V (top), and DCO employing delay cells with 32 buffers, operating at 0.9 V (bottom).

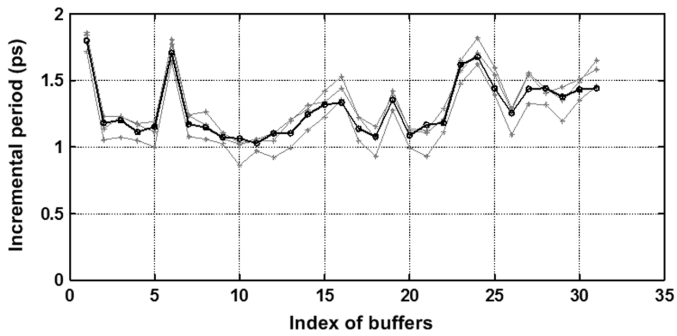

Fig. 9. Measured incremental period of buffers in stage 1 over four different chips.

IV. Modeling of DCO Performance

The cell-based design and automatic layout suggest that the DCO can be implemented in the digital design flow. To fully in-

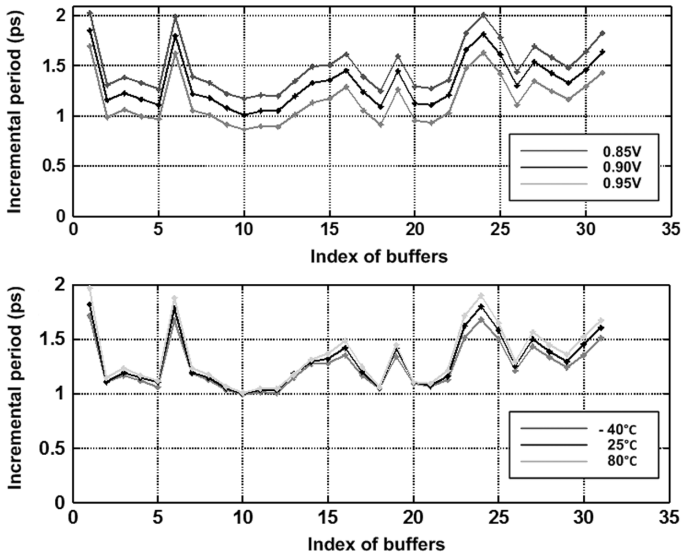

Fig. 10. Measured incremental period of buffers in stage 1 over different supply voltages (top, 0.85 V, 0.9 V, and 0.95 V), and over different temperatures (bottom, 0°C, 25°C, and 70°C).

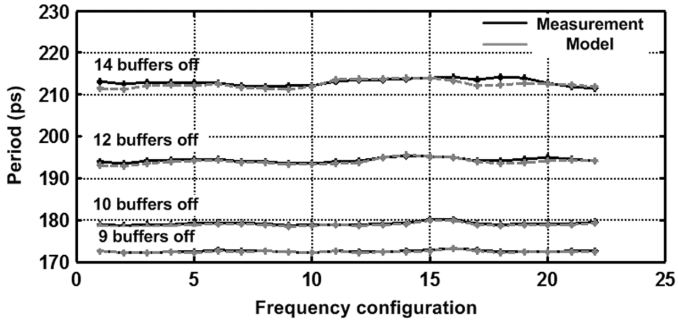

Fig. 11. Measured and modeled periods of DCO over different configurations. The root mean square error between measurement and model is less than 1 ps.

corporate the DCO in the digital design flow, however, a modified timing model is required. The current digital timing model used in CAD tools cannot characterize the systematic mismatch by automatic layout. Also, analog simulations such as *Hspice* and *Spectre* are prohibitive for a large number of buffers, since the number of frequency configurations is exponential to the number of buffers. In this section, a timing model is proposed to predict and verify the performance of the DCO at the design phase. First, the period of the DCO is modeled only with *effective drive strengths*, then, an analytical model to predict *effective drive strength* is derived.

A. Timing Model Based on Effective Drive Strength

We proposed a concept of *effective drive strength* for the calibration in the previous section. For a timing model, we define the *effective drive strength* as

$$\Delta T_i = k \cdot \frac{ds_i}{1 - ds_i} \tag{1}$$

$$\text{where} \quad \sum_{i=1}^{N} ds_i = 1. \tag{2}$$

In (1), ΔT_i is the *incremental period* when only buffer i is turned off, ds_i is the *effective drive strength* of buffer i, and k is a scaling factor calculated from (1) and (2). Now, assuming *effective drive strengths* are given (e.g., measured), the period can be represented as

$$\text{period} = \text{period}_{\min} + k \cdot \frac{\sum_{i:\text{off}} ds_i}{1 - \sum_{i:\text{off}} ds_i} \tag{3}$$

where $\text{period}_{\min}$ is the minimum period when all buffers are enabled.

Since the period of the DCO at every buffer configuration can be calculated with *effective drive strengths* whose number is linear with the number of buffers, (3) provides a computationally efficient model. To verify this model, measured *incremental periods* are applied to predict periods of the DCO with (1)–(3), and the modeled periods are compared with measurements. First, ΔT_i is measured for each buffer by comparing the change in period when only that buffer is disabled. Next, k is calculated using (1) and (2). Finally, the model is used to predict the DCO frequency when an arbitrary set of buffers is disabled by combining the weighted ΔT_i's according to (3). As shown in Fig. 11, in each stage of the DCO, a different set of buffers are turned off, maintaining the number of buffers disabled. The model accurately predicts the measured periods over theses different configurations with a root mean square error between the measurement and model less than 1 ps. (3) therefore provides an accurate, and simple, empirical model for the DCO frequency with complexity that scales linearly with the numbers of buffers.

B. Analytical Model of Effective Drive Strength

In this section, an analytical model of *effective drive strength* is derived. Fig. 12 shows a decomposed delay model for a buffer in the DCO. The delay of a buffer can be modeled as the sum of gate delay (t_{gate}) and interconnect delay (t_{int}). The gate delay is defined as the delay from 50% of input transition to 50% of output transition, and the interconnect delay is defined as the delay from 50% of the output transition to 50% of the input transition of the next buffer. Since the DCO has a parallel structure, each buffer drives multiple parallel buffers, having significant interconnect at the output. In this case, a buffer observes resistive shielding [17], and has a faster output transition at the output of the buffer than at the ends of the interconnect. The delay between those two transitions represents the interconnect delay, and plays an important role in the DCO control.

Though several analytical and accurate models have been proposed [18], [19], the gate delay can be empirically modeled to be proportional to input transition time and load capacitance by

$$t_{\text{gate}} = k_{tr} \cdot t_{r,f} + k_{\text{load}} \cdot C_{\text{eff}}. \tag{4}$$

where k_{tr} and k_{load} are proportionality coefficients of input transition time and load capacitance, and $t_{r,f}$ is rising/falling input transition time.

The Elmore delay model [20], which is the first moment of the impulse response, has been pervasive for decades in synthesis and layout for modeling interconnect delay. Though the Elmore delay can be written in a simple, closed form in terms

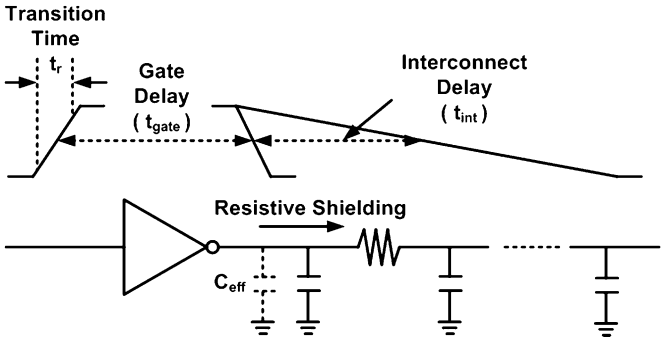

Fig. 12. Simplified delay model of a delay cell.

of design parameters such as device parasitic and width of wires, it provides a limited accuracy. To improve the accuracy of the Elmore delay model, many variants [21]–[23] also have been proposed. The computation of those models, however, is too expensive for the DCO which has an interconnect-intensive structure. Our proposed timing model adopts another variant of the Elmore delay model, the Fitted Elmore Delay (FED), since FED improves accuracy, while maintaining computing efficiency [24]. In FED, the coefficients are determined by a curve fitting technique to approximate *Hspice* simulation results. Following FED, the interconnect delay can be simplified as

$$t_{\text{int}} = a + b \cdot l + c \cdot l^2. \tag{5}$$

where a, b and c are determined by design parameters, and l is the wire length. Since design parameters are identical for the buffers and wires in the cell-based DCO, the values of a, b, and c can be considered constant for each buffer, and (5) suggests that the interconnect delay can be approximated to be proportional to l^2 as l increases. The total delay of the buffer in Fig. 12 is therefore the sum of (4) and (5).

In the DCO, each stage has multiple buffers, and all buffers in consecutive stages are connected to each other through a wire network. Thus, the timing models of a buffer, (4) and (5), should be extended for the structure with multiple sources and multiple sinks. If there are N buffers in each stage, the macro gate delay for a stage is a function of individual gate delays. Since the total delay is additive, and the gate delay becomes dominated by the interconnect delay as N increases, and the function can be approximated as the mean of individual gate delays as follows:

$$\begin{aligned} T_{\text{gate}} &= f(t_{\text{gate},1}, t_{\text{gate},2}, \ldots, t_{\text{gate},N}) \\ &\approx \text{mean}(t_{\text{gate},1}, t_{\text{gate},2}, \ldots, t_{\text{gate},N}) \end{aligned} \tag{6}$$

where T_{gate} is the macro gate delay of a stage, and $t_{\text{gate},i}$ is the gate delay of ith buffer as described in (4).

To derive an interconnect model of the DCO, we propose a constant current source model as shown in Fig. 13. Let $t_{\text{int}}\,(j,k)$ refer to an interconnect delay between source j and sink k, and assume the output transition is linear. Then, interconnect can be modeled as a lumped capacitance driven by a constant current source, and the current value is as follows:

$$i(j,k) = \frac{C \cdot V}{2 \cdot t_{\text{int}}(j,k)} \tag{7}$$

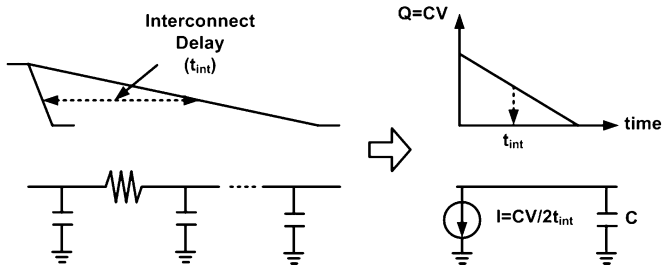

Fig. 13. Constant current source model for interconnect.

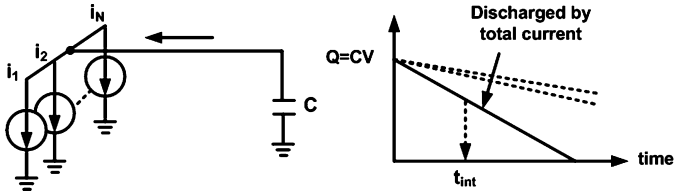

Fig. 14. Multiple current sources to a single sink.

where C is the lumped capacitance, and V is the supply voltage. Then, the constant current source model can be extended to multiple sources (Fig. 14). When N source buffers drive a sink k, the total current from sources to the sink is obtained as

$$i_k = \sum_{j=1}^{N} i(j,k) = \frac{C \cdot V}{2} \sum_{j=1}^{N} t_{\text{int}}(j,k)^{-1} \tag{8}$$

where i_k is total current from source buffers to the sink k. Thus, the interconnect delay at sink k by i_k is as follows:

$$t_{\text{int},k} = \frac{C \cdot V}{2 \cdot i_k} = \frac{1}{\sum_{j=1}^{N} t_{\text{int}}(j,k)^{-1}} \tag{9}$$

Since there are N buffers in the sink stage, the macro interconnect delay for a stage can be expressed as a function of individual delays as (10). Assuming that $t_{\text{int},k}$'s have a small standard deviation when all buffers are turned on, the function is approximated again as the mean of the individual interconnect delays.

$$\begin{aligned} T_{\text{int}} &= f(t_{\text{int},1}, t_{\text{int},2}, \ldots, t_{\text{int},N}) \\ &\approx \text{mean}(t_{\text{int},1}, t_{\text{int},2}, \ldots, t_{\text{int},N}) \end{aligned} \tag{10}$$

The macro interconnect delay model in (9) and (10) indicates that the effect of each buffer on the delay is different from each other, and the distribution can be approximately modeled. Fig. 15 shows an example where one buffer in the source stage is turned off. When turning off source 1, the current from sources to sink k is reduced by $i\,(1,k)$, thus, using (8) and (9), interconnect delay at the sink k is increased as follows:

$$t'_{\text{int},k|u_1\text{off}} = \frac{1}{\sum_{j=1}^{N} t_{\text{int}}(j,k)^{-1} - t_{\text{int}}(1,k)^{-1}}. \tag{11}$$

Then, the incremental delay is

$$\begin{aligned} \Delta t_{\text{int},k}|_{u_1\text{off}} &= t'_{\text{int},k}|_{u_1\text{off}} - t_{\text{int},k} \\ &= \frac{t_{\text{int}}(1,k)^{-1}}{\left\{\sum_{j=1}^{N} t_{\text{int}}(j,k)^{-1} - t_{\text{int}}(1,k)^{-1}\right\} \cdot \sum_{j=1}^{N} t_{\text{int}}(j,k)^{-1}} \end{aligned} \tag{12}$$

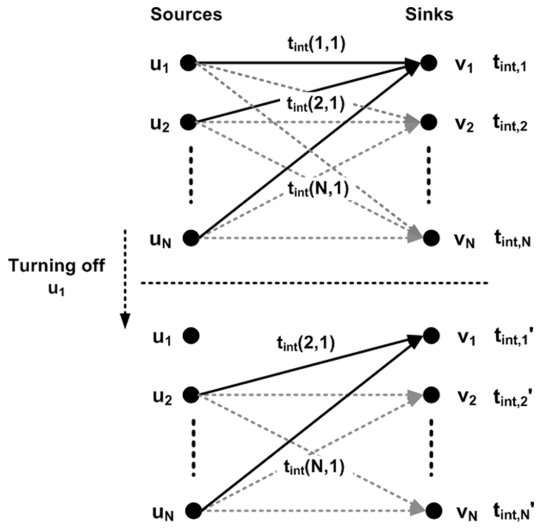

Fig. 15. Constant current source model. Total current decreases when one buffer in source stage is disabled.

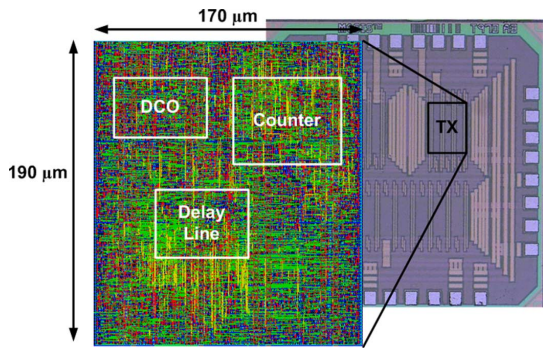

Fig. 16. 65 nm CMOS transmitter die micrograph and layout view.

and the macro interconnect delay is increased as

$$\Delta T_{\text{int}} = \text{mean}(\Delta t_{\text{int},1}|_{u_1\text{off}}, \ldots, \Delta t_{\text{int},N}|_{u_1\text{off}}). \quad (13)$$

Equation (13) corresponds to the incremental period in (1), thus the effective drive strength can be represented as

$$ds_1 = \frac{\Delta T_{\text{int}}}{\Delta T_{\text{int}} + k}. \quad (14)$$

The above macro model provides a useful insight about the layout effect on the *effective drive strengths* of buffers. The distribution of effective drive strengths is a function of the wire length distribution. When the distribution of *effective drive strength* is analyzed with the macro model, the oscillation frequency of the DCO can be predicted with (3).

V. Measured UWB Transmitter Performance

The transmitter was fabricated in a 65 nm CMOS process, and the micrograph and the layout view of the transmitter are shown in Fig. 16. All functional blocks are integrated through automatic place-and-route so that the transmitter occupies a small area. The area of the transmitter is 0.032 mm^2. Benefitting from high operating frequency of 65 nm standard cells, the transmitter is operated at 0.9 V (not at a nominal supply voltage, 1 V), in order to reduce power consumption. Fig. 17 shows the measured transient waveform of a 3.5 GHz UWB pulse. The output has a DC component that is characteristic of all-digital IR-UWB transmitters, since the transmitter generates UWB pulses that are switching between supply voltage and ground. The DC spectrum is filtered by an off-chip high-pass filter. The measured power spectral densities (PSD) when the transmitter is tuned to three channels are shown in Fig. 18. The center frequency of the UWB pulse is tunable in the 3.1-to-5.0 GHz frequency band with an average tuning step of 50 MHz. The bandwidth of the UWB pulse is also digitally controlled, and the measured bandwidth ranges from 500 MHz to 1.4 GHz. Fig. 19 illustrates the effect of DB-BPSK by the scrambler. When the scrambler is enabled, the spectral lines, characteristic of PPM modulation, are suppressed, allowing higher transmit power without violating the FCC mask.

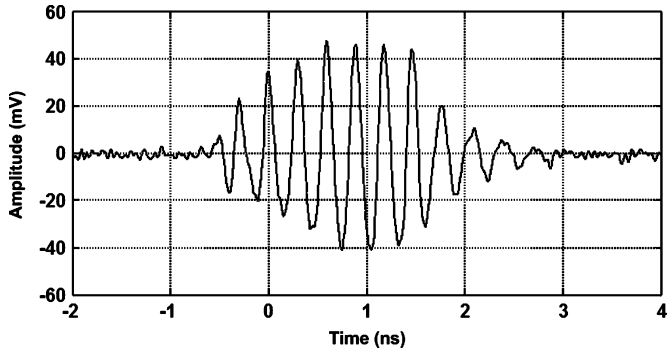

Fig. 17. Measured transient waveform of UWB pulse at 3.5 GHz after off-chip high-pass filter.

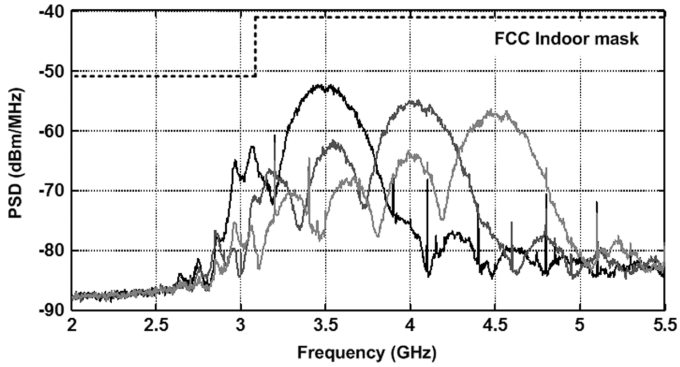

Fig. 18. Measured output spectral densities of three channels after off-chip high-pass filter.

Consistent with the synthesized design, the final stage of the transmitter is a large, standard cell inverter. The chips were packaged in a wirebonded 5 mm × 5 mm QFN package, and an off-chip high-pass filter was used to attenuate the DC component of the pulses. According to simulations, the inverter output can directly drive a 50 Ω load with a fixed amplitude of 84% of the supply voltage, when no losses from packaging and filtering are considered. The pulse amplitude at the antenna will be reduced by packaging parasitics, off-chip filter attenuation, and

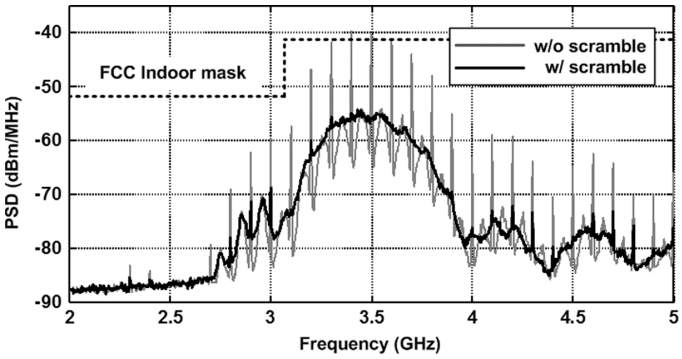

Fig. 19. Measured power spectral density w/ and w/o scrambling. Without scrambling, PSD violates the FCC mask.

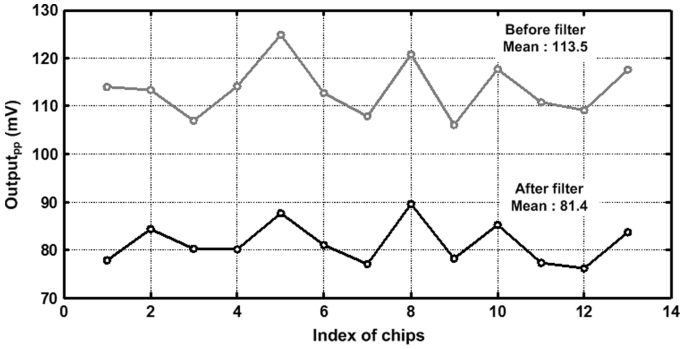

Fig. 20. Measured output amplitude before/after filter of 13 chips. These are attenuated values (1 dB) by cable in measurement.

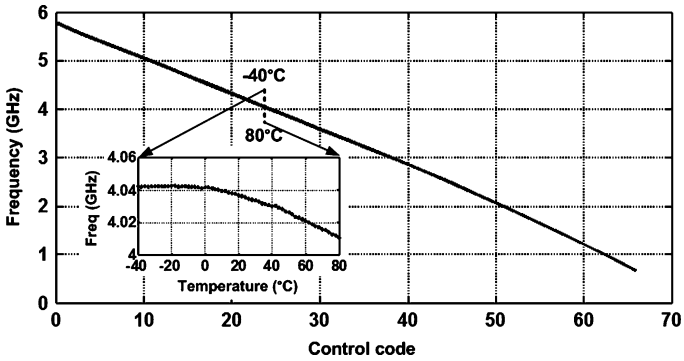

Fig. 21. Measured temperature variation of center frequency control.

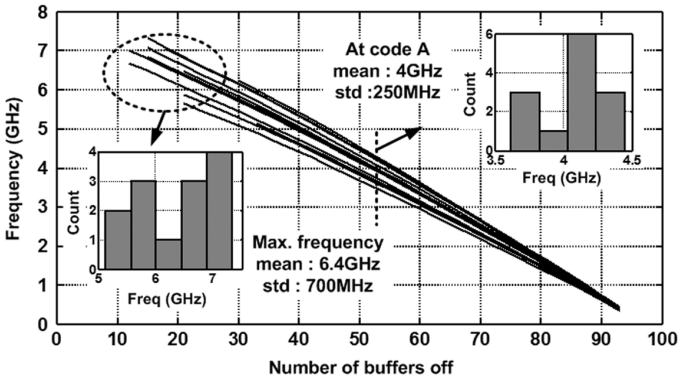

Fig. 22. Measured frequency control of 13 chips.

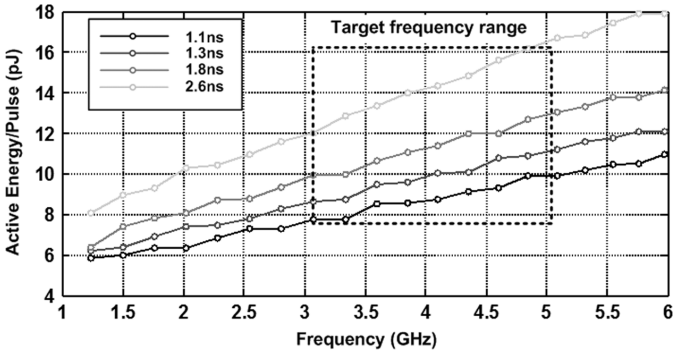

Fig. 23. Measured active energy/pulse at four different pulse widths from 1.1 ns (1.4 GHz bandwidth) to 2.6 ns (500 MHz bandwidth).

cable loss. Although package parasitics cannot be measured, assuming an on-chip 20 Ω trace resistance, 3 nH bondwire inductance, and 3 pF load capacitance, the simulated attenuation of the pulse is 12.5 dB. The measured off-chip filter loss is 2.9 dB from Fig. 20, and cable loss is 1 dB. The sum of these losses account for the limited amplitude reported in Figs. 17 and 20, and by utilizing better RF packaging and antenna filtering, much higher radiated amplitudes are achievable.

Fig. 20 also shows the variation of the output amplitude. The standard deviation of the amplitude measured over 13 chips, including chip, package, and printed circuit board (PCB), is 0.23 dB. The maximum level of the transmitted PSD will depend on the pulse amplitude and the pulse repetition frequency (PRF). Given the relatively constant amplitude of output pulses, the transmitted PSD can be determined solely by the PRF.

Fig. 21 shows the measured variation of center frequency over a temperature range of -40°C to 80°C. The frequency varies less than 2% over the temperature range, which is well within the tuning range of the DCO. Fig. 22 shows the measured frequency control and the maximum operating frequencies of 13 chips. The maximum frequency is limited by the frequency divider in the transmitter, not by the DCO. All measured chips show maximum frequency over 5 GHz at 0.9 V, satisfying the target performance. Though the frequency control at a given code shows deviation between the chips, this process variation can be tuned with the proposed calibration scheme.

The transmitter consumes a fixed power of 170 μW due to leakage currents, and the active energy added to the core while pulsing depends on the activity factor such as the center frequency and pulse width. The measured active energy is shown in Fig. 23 at four different pulse widths. The active energy ranges from 8 pJ/pulse to 16 pJ/pulse over the frequency of 3.1 to 5.0 GHz, and the bandwidth of 500 MHz to 1.4 GHz. The performance of the transmitter is summarized in Table I.

VI. Conclusion

An all-digital UWB transmitter was designed and fabricated in a 65 nm CMOS process, leveraging automated design tools. All functional blocks are implemented with digital standard cells and automatically placed-and-routed. The center frequency and the bandwidth of the UWB pulses are digitally tuned to compensate for variations, and systematic mismatch

TABLE I
PERFORMANCE SUMMARY

	This work	[9]	[10]	[11]	[12]	[13]
Process	65nm CMOS	90nm CMOS	90nm CMOS	180nm CMOS	90nm CMOS	180nm CMOS
Supply	0.9V	1V	1V	1.8 to 2.2V	1V	-
Die Area	0.032mm^2	0.08mm^2	0.07mm^2	0.045mm^2	0.07mm^2	0.11mm^2
Modulation	PPM+DB-BPSK	PPM+DB-BPSK	PPM+BPSK	BPSK	PPM+BPSK	PPM+BPSK
PRF	0 to50MHz	<16.7MHz	0 to 15.6MHz	<750MHz	0 to 15.6MHz	<560MHz
Center Frequency	3.1 to 5GHz	3.1 to 5GHz	2.1 to 5.7GHz	8GHz	3.1 to 10GHz	3 to 5GHz
Bandwidth (10dB)	0.5 to 1.4GHz	~2GHz	~500MHz	~2GHz	16MHz	-
Output Amplitude	~91mV* (w/ filter)	~700mV	~200mV	~70mV	~600mV	~200mV
	~126mV* (w/o filter)					
Standby Power	170μW	96μW	-	-	123μW	-
Active Energy/pulse	8 to 16pJ/pulse	>47pJ/pulse	>17pJ/pulse	>12pJ/pulse	40pJ/pulse	75pJ/pulse

* The amplitudes are adjusted to account for cable loss

that is dominated by interconnect. The proposed calibration scheme provides a simple and monotonic tuning of the DCO frequency, and the proposed timing model can be utilized to predict and verify the DCO performance at the design phase. The transmitter occupies only 0.032 mm^2, and consumes an active energy of 8 pJ/pulse to 16 pJ/pulse, and a leakage power of 170 μW, which combine to a total minimum energy/pulse of 12 pJ/pulse at 50 Mb/s.

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