IR-UWB Transmitters Synthesized from Standard Digital Library Components

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***Abstract*—This paper presents two impulse radio ultra-wideband (IR-UWB) transmitters which are synthesized from standard digital library components. All functional blocks in the transmitters are implemented with digital standard cells, and placed-and-routed (PAR) by automatic design tools; therefore the transmitter is portable and scalable to other process technologies. To verify the feasibility of the architecture, the transmitter is implemented in a FPGA device, then, fabricated in a 65nm CMOS process. The 65nm CMOS transmitter occupies 0.0375mm^2, and the active energy consumption while pulsing is 90pJ/pulse.**

I. INTRODUCTION

Impulse radio ultra-wideband (IR-UWB) has been attracting attention as a promising technology for low power short-range wireless applications such as sensor networks and radio frequency identification (RFID) [1][2]. Its inherent duty-cycled nature lowers power consumption, and non-coherent communication relaxes frequency tolerance of the output signal. These features are also favorable to the all-digital implementation of UWB transmitters that generate radio frequency (RF) pulses by switching digital signals. All-digital transmitters draw no static bias current, thereby minimizing power consumption in the duty-cycled operation, and the switching speeds of scaled CMOS devices are sufficient for the relaxed frequency tolerance of non-coherent UWB signaling. In addition, all-digital transmitters are integrated with digital baseband systems, occupying minimal area.

This paper presents two *synthesized* UWB transmitters. While the all-digital transmitters in literature [3]-[7] have addressed the advantages described above, the performances of the transmitters are dependent on custom circuits and custom layouts, which are time-consuming and error-prone. The proposed transmitters, however, can be implemented with logic cells from standard libraries, and they are placed-and-routed (PAR) by automatic design tools. The characterization of each cell, which is available in the libraries, is also useful to model and predict the performance of the synthesized transmitters. This simplified design procedure reduces the design cost and the dependency on the process technology, thus the proposed transmitters are scalable and portable to different processes.

In the synthesized circuits, however, the automatic PAR inherently induces systematic mismatch on the signal paths, affecting the performance of the transmitters. To compensate the mismatches, the center frequency and bandwidth of the UWB signal in the proposed transmitters are digitally tunable in a broad range. With the digital configurability, the transmitters can also attack process, voltage, and temperature (PVT) variations.

The remainder of this paper is organized as follows. Section II describes the proposed all-digital transmitter architecture, focusing on pulse generators with logic cells. Then, an FPGA implementation of the transmitter is discussed in the Section III. Section IV presents the transmitter fabricated in a 65nm CMOS technology, and Section VI concludes this paper.

II. ALL-DIGITAL UWB TRANSMITTER ARCHITECTURE

The proposed all-digital transmitter architecture is shown in Fig. 1. The functional blocks - the system controller, the modulator, and the pulse generator - are implemented with logic cells, and interfaced with digital signals. The system controller sets the control parameters for the modulator and the pulse generator. If the pulse position modulation (PPM) scheme is applied, the system controller determines the number of pulse slots and the pulse repetition frequency (PRF). The system controller also sets the center frequency and the bandwidth of the UWB signals. According to the parameters from the system controller, the PPM modulator divides the PRF period into a number of time slots and generates one edge at an encoded slot. Then, the pulse generator is triggered by the edge from the PPM modulator to synthesize UWB pulses with the specified center frequency and bandwidth.

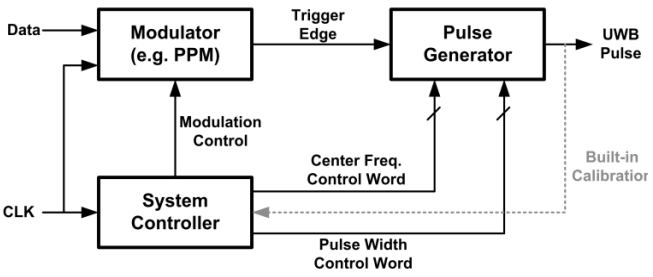

Fig. 1. Block diagram of the proposed all-digital UWB transmitter. All functional blocks are implemented with logic cells and automatically placed and routed with design tools.

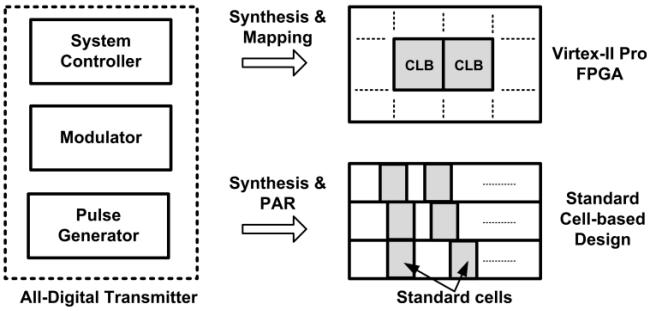

Fig. 2. All-digital UWB transmitter is synthesized and mapped to an FPGA device (Section III), and synthesized and PAR-ed on silicon (Section IV).

The logic cell-based functional blocks and the digital interface enable the implementation of the transmitter with standard cells. Standard cells are pre-defined building blocks which are available in most commercial CMOS process technologies. Though the standard cells are less flexible to implement circuits with, the simulation, synthesis and layout procedures are highly automated with design tools. Also, the circuits are described in scripts, thus they are portable to different systems or different process technologies. With these advantages, the standard cell-based design is common in large digital circuits. When the standard cells are applied to conventional analog functionality such as UWB transmitters, the design procedure can be significantly simplified, and the integration of analog/RF function with digital systems can be enhanced. Fig. 2 illustrates the proposed all-digital transmitter synthesized/mapped to an FPGA, or synthesized/PAR-ed on silicon, emphasizing the automated design procedure and the portability of the transmitter.

The system controller and the modulator are inherently logic circuits, and they are described in behavioral codes, and synthesized with standard cells by design tools. However, since the performance control of the pulse generator is critical, the components of the pulse generator need to be specified in the structural codes. Then, the placement and integration of the whole transmitter system is done automatically by the design tools. This paper proposes two pulse generator architectures; a delay line pulse generator and a ring pulse generator. Both architectures provide tunable center frequency and bandwidth to meet the specifications of UWB systems.

A. Delay Line Pulse Generator

Fig. 3 shows the structure of the delay line pulse generator [3]. The delay line pulse generator is composed of a delay line, a mask register, and an edge combiner. In order to implement a digitally controllable delay with standard cells, this paper proposes a tunable delay cell as shown in Fig. 3. The tunable delay cell is implemented with a number of parallel tri-state buffers which are available in standard libraries. While the load capacitance at each node is determined by the number of tri-state buffers and wiring, the driving strength of the delay cell is controlled by turning on a different number of buffers. The tuning range and tuning resolution of the delay cell is determined by the number of buffers in the delay cell.

When a trigger edge arrives from the PPM modulator, it propagates through the delay line, and generates delayed edges at the output nodes of all the delay cells with the programmed intervals. Then, the mask register selects edges before combining them. By bitwise AND-ing the incoming edges and the masking bits from the system controller, specific edges are selected. Finally, the selected edges are combined by the edge combiner. The edge combiner is implemented with an XOR tree, thus each incoming edge toggles the output signal. In this way, two edges combine to generate one cycle, and the period of the cycle is the sum of the delays of the two stages. The delays between the delay cells determine the periods of cycles, thereby the center frequency of the UWB pulses, and the number of edges selected by the mask register controls the UWB pulse width, thus the bandwidth in the frequency domain.

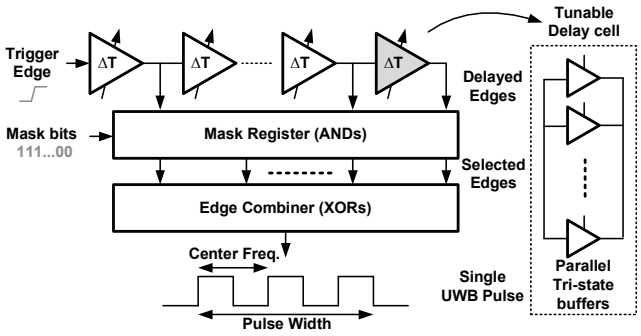

Fig. 3. Delay line pulse generator with tunable delay cell.

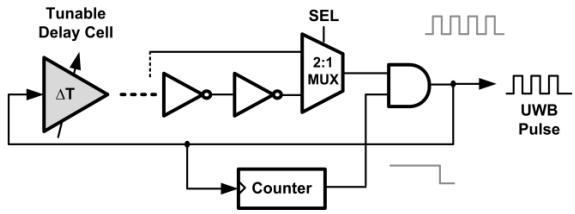

Fig. 4. Ring pulse generator. Coarse/fine control is implemented with the tunable delay cell and MUX.

B. Ring Pulse Generator

The structure of the ring pulse generator is shown in Fig. 4. The ring pulse generator is composed of a ring oscillator embedding a MUX and the delay cell, and a counter. An odd number of inverters connected in a ring generate an oscillating signal, and the center frequency of the oscillation is determined by the number of the inverters and their delays. Since the number of inverters is not reconfigurable once the circuit is synthesized, the tunable delay cell and a MUX are included to tune the frequency of the ring. The delay cell is tuned for a fine tuning, and the MUX selects the number of the inverters in the loop, providing a coarse tuning.

A counter and an AND gate are required to control the number of cycles in a pulse, which determines the bandwidth of the UWB pulse. When the counter value reaches the target number of cycles, the oscillating signal is gated, and the ring oscillator is turned off.

III. FPGA Prototype

The proposed all-digital UWB transmitters were

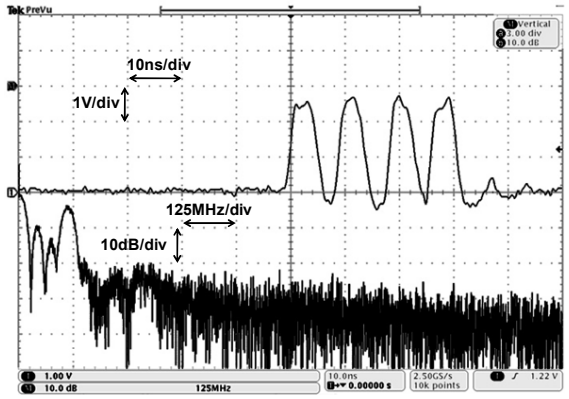

Fig. 5. Measured UWB pulse waveform and spectrum of the FPGA delay line pulse generator.

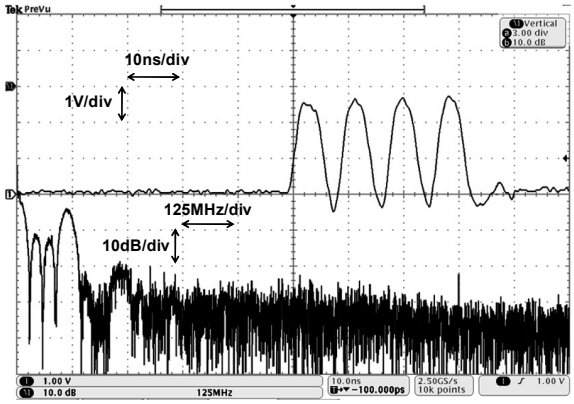

Fig. 6. Measured UWB pulse waveform and spectrum of the FPGA ring pulse generator.

implemented on an FPGA device [8]. In the FPGA circuit designs, each functional block is described in a hardware description language, then synthesized and mapped to structures in the FPGA by automatic design tools. This design procedure is ideal for the demonstration of the proposed synthesizable transmitters. The prototype transmitters were implemented on the Xilinx Virtex-II Pro FPGA, and the ISE Foundation design tools were utilized [9].

The system controller and the modulator were described in Verilog codes, and mapped to the configurable logic blocks (CLBs) in the FPGA. Unlike the system controller and the modulator, the tunable delay cell in the pulse generator cannot be mapped to the CLBs. Instead, the Virtex-II Pro FPGA provides tri-state buffers named TBUF. Although TBUF does not have the same structure as the tri-state buffers from CMOS standard libraries, TBUF has an input port to control connectivity to shared wires. By disabling a TBUF, the output of the TBUF is disconnected from the shared output wire, and it becomes a high-impedance node. Therefore, the same digital tuning described in the Section II can be achieved with TBUFs. The FPGA delay line was implemented with eight stages of delay cells, thus having four cycles per UWB pulse. The mask register and the edge combiner were implemented with logic gates, which were mapped to the CLBs in the FPGA. For the ring pulse generator, the tunable delay cell was implemented with TBUFs, and the inverters and MUX were mapped to the CLBs. The clock signal and the input data are provided to the FPGA from external sources. Since the FPGA device has an interconnect-intensive structure, and the package does not support high frequency over 3.1GHz, the input data rate and the output frequency are scaled down to 1Mbps and 110MHz, respectively. In the scaled frequency, the prototype circuits target the fractional bandwidth requirement (bandwidth>20% of the center frequency).

Fig. 5 shows the pulse waveform and the spectrum of the delay line pulse generator. As shown in Fig. 1, the output signal is fed back to the system controller, and the center frequency is measured with a counter in the system controller. For the calibration of the delay line pulse generator, every loop including only one signal path can be made by configuring the mask register. Then, the oscillation frequency around each loop is measured, and the difference between adjacent loop frequencies represents the delay between each stage. After tuning each delay cell with the control words, the mismatches between the delay cells are compensated, and the desired spectrum is obtained. The measured center frequency is 110.25MHz and the bandwidth is 41.5MHz, 37.6% of the center frequency, meeting the FCC fractional bandwidth requirement. Fig. 6 shows the pulse waveform and the spectrum of the ring pulse generator. The period of each cycle has the same signal path in the ring, thus it is the same without tuning. Therefore, the center frequency is tuned simply by controlling the delay cell and the MUX. The measured center frequency is 111.25MHz and the bandwidth is 41.9MHz, which is 37.6% of the center frequency. This satisfies the FCC fractional bandwidth requirement.

IV. SYNTHESIZED ASIC

A transmitter was also fabricated in a 65nm CMOS process. All functional blocks are implemented with standard cells and PAR-ed with automatic design tools. Among the pulse generator architectures proposed in the Section II, the ring pulse generator was adopted in the fabricated transmitter. In Fig. 7, when the trigger signal enables the digitally controlled oscillator (DCO) and the delay line, the DCO oscillates at the desired frequency, and an edge propagates through the delay line. When the edge arrives at the end of the delay line, the DCO output to the antenna is gated. In this way, the DCO controls the center frequency, and the delay line determines the bandwidth of the UWB pulses.

While the pulse width was controlled as an integer

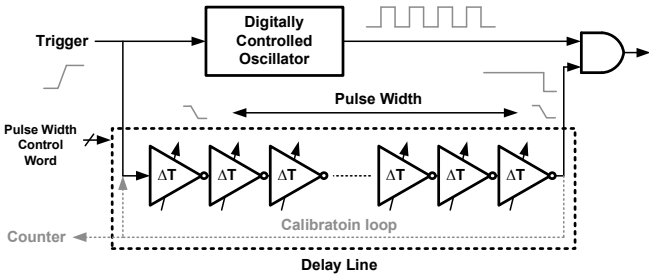

Fig. 7. Pulse generator in synthesized UWB transmitter. The delay line implemented with tunable delay cells control the pulse width of UWB pulses.

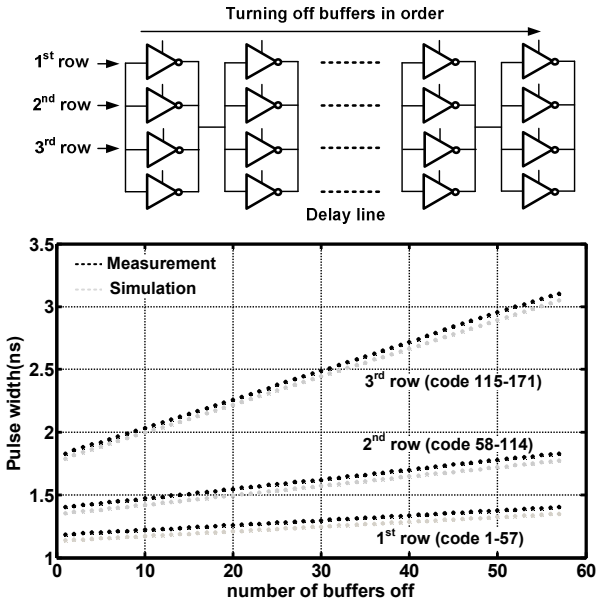

Fig. 8. Pulse width control of the transmitter and measured programmable pulse width range. the pulse width is increasing by turning off tri-state buffers in the delay line.

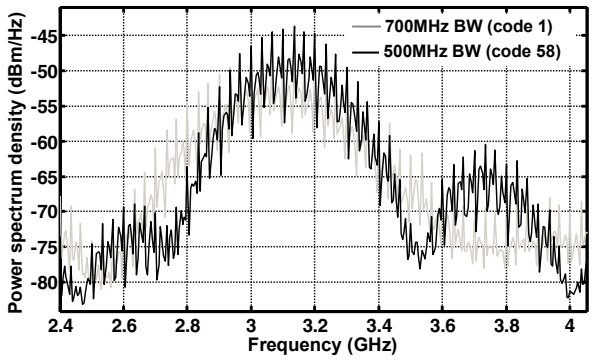

Fig. 9. Measured spectrum of the UWB pulses for different pulse width control words.

number of RF cycles in the FPGA prototypes, the pulse width is finely tuned with the tunable delay cells in the ASIC. The delay line has 57 tunable delay cells, and each delay cell is implemented with 4 parallel tri-state buffers. When every buffer is turned on, the pulse width of UWB pulses is shortest, and it is increased by turning off buffers in order (Fig. 8). During calibration mode, the delay line is configured as an oscillating loop, and the frequency around the loop is measured by counting cycles over a time period which is set in terms of CLK counts. As shown in Fig. 8, the measured pulse width ranges from 1.1ns to 3.1ns, and corresponds to the simulated values. Fig. 9 shows the measured spectrum of UWB pulses for different pulse width control words (code 1 and code 58), and the 10dB bandwidths of the spectrum are 700MHz and 500MHz, respectively. With the tunable range of pulse width, PVT and PAR variations can be compensated to have a desired bandwidth. The fabricated transmitter occupies only 0.0375mm^2, and the active energy consumption while pulsing is 90pJ/pulse. The performance of the transmitter is summarized in Table 1.

TABLE I
PERFORMANCE SUMMARY

Process	65nm CMOS
Die Area	0.0375mm^2
Modulation	PPM
PRF	16.7MHz
Center Frequency	~3.17GHz
Pulse Width	1.1-3.1ns
Active Energy/pulse	90pJ/pulse

V. CONCLUSION

An all-digital synthesizable UWB transmitter architecture was proposed. Since all functional blocks can be implemented with digital standard cells and automatically placed-and-routed, the UWB transmitter is portable and scalable to other process technologies. The center frequency and the bandwidth of the UWB pulses are digitally tuned to compensate for variations. The transmitter draws no static currents other than leakage, and minimizes power consumption by turning off functional blocks between generating pulses. Also, the area is reduced by eliminating passive components and completely integrated with other digital systems. The feasibility and functionality of the proposed transmitter architectures were verified with the FPGA prototypes and the fabrication in a 65nm CMOS process.

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