A Cyclic Vernier TDC for ADPLLs Synthesized From a Standard Cell Library

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***Abstract*—This paper presents a cyclic Vernier time-to-digital converter (TDC) with digitally controlled oscillators (DCOs), targeted for a synthesizable all-digital phase locked loop (ADPLL). All functional blocks in the TDC are implemented with digital standard cells and placed-and-routed (P&R) by automatic design tools; thus, the TDC is portable and scalable to other process technologies. The effect of P&R mismatch is characterized in calibration mode, and utilized to achieve a minimum TDC resolution of 5.5 ps. The TDC was fabricated in a 65 nm CMOS process, and occupies 0.006 mm^2.**

***Index Terms*—All-digital PLL (ADPLL), standard cell library, synthesis, time-to-digital converter (TDC), Vernier.**

I. Introduction

RECENT process scaling allows all-digital architectures of conventional analog applications that leverage advanced digital processes. In deep submicrometer digital CMOS processes, die area decreases proportional to the scaling factor, and operating frequency increases with reduced geometry. Also, power consumption decreases as the supply voltage scales. Analog circuits, however, do not benefit from the process scaling as much. Lower supply voltage requires more accurate voltage control, and deteriorates signal-to-noise ratio (SNR) of the circuits. To maintain the same performance, the power dissipation of analog circuits does not scale as effectively as their digital counterparts [1], [2].

An all-digital phase locked loop (ADPLL) replaces conventional analog blocks in a PLL with an all-digital architecture, benefitting from the advanced digital process [3], [4]. Fig. 1 shows the general block diagram of an ADPLL. In the ADPLL, a time-to-digital converter (TDC) compares the phase error between the reference clock $(\mathrm{F_{ref}})$ and the divided clock $(\mathrm{F_{div}})$. Then, the digitized phase error is filtered by a digital loop filter (DLF), and utilized to control the frequency of a digitally controlled oscillator (DCO). The TDC and DLF replace a charge pump and large passive components of conventional analog PLLs, reducing the power dissipation and area of the ADPLL. Also, the digital interface between the blocks enhances testability and programmability of the ADPLL. In this architecture, the DLF and the divider are required to satisfy only timing constraints; thus, they can be implemented with digital logic circuits, following a *digital design flow*. On the other hand, the TDC and DCO directly affect the performance of the ADPLL. Many structures for TDCs and DCOs have been proposed to achieve high performance ADPLLs [5]–[16].

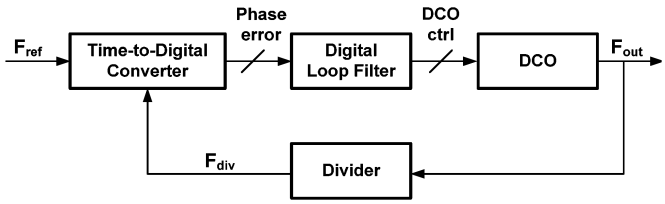

Fig. 1. General block diagram of all digital PLL.

In this paper, we focus on a TDC specifically for ADPLLs, and propose a cyclic Vernier structure which is synthesized from a standard cell library [17]. The quantization noise from the TDC impacts in-band phase noise of the ADPLL; thus, a high resolution TDC is desirable. The proposed TDC achieves high resolution as well as a large detection range through the cyclic Vernier structure. Another advantage of the proposed TDC is that it is implemented with only digital standard cells, and the implementation is fully automated through synthesis and P&R. There is no custom circuit design or custom layout that requires comprehensive characterization, making the TDC a portable and scalable block. The proposed TDC, therefore, can be included in the automated *digital design flow* as other digital blocks, suitable to be a building block for a *synthesizable* ADPLL.

Automatic P&R imposes systematic mismatch in the circuits, which has previously been a barrier for synthesizable TDC architectures. The performance of the circuits is highly dependent on the matching between blocks, thus custom layout is typically required. In this paper, we propose a calibration scheme that addresses the systematic mismatch in the automatically P&R-ed TDC to satisfy a target performance, and furthermore we exploit the P&R mismatch to obtain higher performance.

The remainder of this paper is organized as follows. Section II describes the cyclic Vernier TDC architecture and functional blocks. Then, the calibration scheme of the TDC resolution, which takes the systematic mismatch into account, is discussed in the Section III. Section IV presents the measured TDC performance, and Section V concludes this paper.

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II. Cyclic Vernier Time-to-Digital Converter

A. TDC Architecture

Fig. 2 shows the block diagram of a cyclic Vernier TDC [6], [7]. The goal of the TDC is to measure the time difference between the rising edges of the "Start" and "Stop" signals, which are $\mathrm{F_{ref}}$ and $\mathrm{F_{div}}$ in the ADPLL, respectively. When the "Start" is asserted, the slow DCO starts to oscillate with a period of $\mathrm{T_s}$, and the number of oscillations is counted by the coarse counter. After an input delay of $\mathrm{T_{input}}$, the "Stop" signal is asserted which triggers the faster DCO to oscillate with a period of $\mathrm{T_f}$. At this time, the coarse counter is disabled, and the output of the counter represents a coarse measurement of the time between "Start" and "Stop" rising-edges $(\mathrm{T_{coarse}})$. To improve the measurement accuracy, the residue of the input delay $(\mathrm{T_{fine}})$ is measured by the Vernier structure. When $\mathrm{T_f}$ is slightly smaller than $\mathrm{T_s}$, the time difference between rising edges of the two oscillations is reduced every cycle by the difference in periods $(\mathrm{T_s} - \mathrm{T_f})$, and the edge of the fast DCO eventually catches up to the slow DCO. By counting the number of cycles it takes for the fast DCO to catch up with the slow DCO, $\mathrm{T_{fine}}$ is measured. Then, the overall measurement of $\mathrm{T_{input}}$ can be determined as follows:

$$T_{\mathrm{input}} = t_{\mathrm{STOP}} - t_{\mathrm{START}} \quad (1)$$

$$T_{\mathrm{input}} = T_{\mathrm{coarse}} + T_{\mathrm{fine}} = N_s T_s + N_f (T_s - T_f) \quad (2)$$

where $\mathrm{N_s}$ and $\mathrm{N_f}$ are the number of cycles of the slow and fast oscillations, respectively, and $(\mathrm{T_s} - \mathrm{T_f})$ is programmed to be much smaller than $\mathrm{T_s}$. As shown in Fig. 2, the TDC operates in two-steps; a coarse step and a fine step. The coarse step resolution is the period of the slow DCO, and the fine step resolution is the *difference* between the periods of the two DCOs. Note that the fine resolution does *not* depend on the absolute frequencies of the DCOs, but only their difference in periods. This is crucial for the calibration of mismatch between the P&R-ed DCOs discussed in Section III.

Unlike conventional Vernier delay lines, the cyclic Vernier TDC adopts the ring structure to extend input range, limited only by the counter size that easily scales according to the application. Also, the linearity of the TDC improves by utilizing the periods of the DCOs, which is repetitive and consistent over operation, while the delay per stage in Vernier delay lines is more susceptible to variation and mismatch. One drawback of the cyclic Vernier TDC is a large latency of the fine step measurement. It takes one period of the fast DCO cycle $(\mathrm{T_f})$ to resolve a time difference of one fine step resolution $(\mathrm{T_s} - \mathrm{T_f})$. To reduce the conversion time, we adopt the two-step operation. The coarse step covers a large input time difference without any latency, and the residue of the coarse step is measured by the fine step, which is less than one cycle of the slow DCO. Also, this fine step range can be further reduced by the edge detector described in Section II-C.

B. Digitally Controlled Oscillator

While the previous cyclic Vernier TDC architectures [6], [7] adopt voltage controlled oscillators (VCOs), which require custom design and layout, the proposed TDC adopts DCOs that are implemented with only standard cells and P&R-ed. Fig. 3 shows the structure of the DCO. The DCO consists of three stages, and each stage is implemented with eight parallel inverting tristate buffers which are digitally controlled. Tristate buffers are available in commercial standard cell libraries. While the load capacitance at each stage is fixed by the number of buffers and wiring capacitance, the driving strength can be varied by turning on a different number of tristate buffers, thereby configuring the frequency of the DCO. Since the buffers are automatically P&R-ed by design tools, the placement and routing of the buffers are not regular as illustrated in Fig. 3. This results in systematic mismatch in the wiring capacitance, and thus a unique *effective* drive strength for each buffer. Though the individual drive strength cannot be controlled in the automated layout, the placement area and the wire lengths are constrained by layout algorithms, and statistics of the P&R mismatch is, to some extent, predictable at the design phase.

In the proposed TDC, both the slow and fast DCOs are identically designed in a Verilog description, and automatically P&R-ed. Then, the P&R mismatch is characterized in the calibration mode, and the DCOs are configured to have slightly different periods, utilizing the P&R mismatch. The P&R mismatch provides higher resolution for the TDC, compared to the resolution obtained when the buffers are ideally matched.

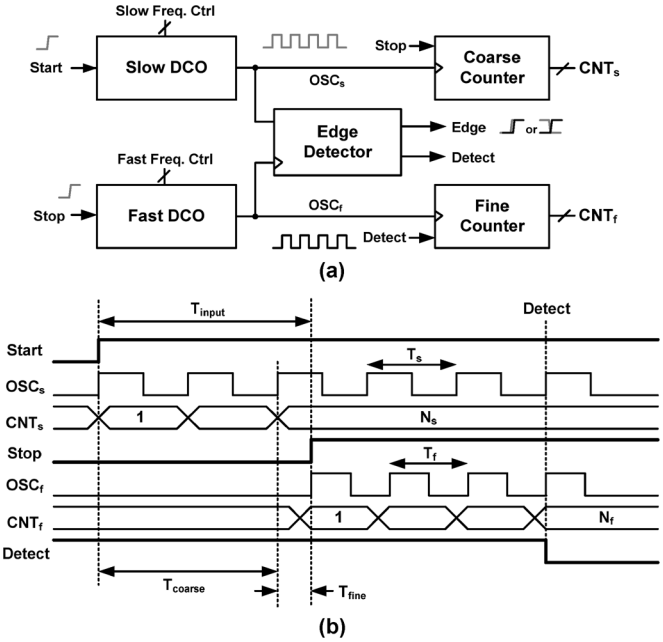

Fig. 2. (a) Block diagram of the proposed TDC and (b) timing diagram.

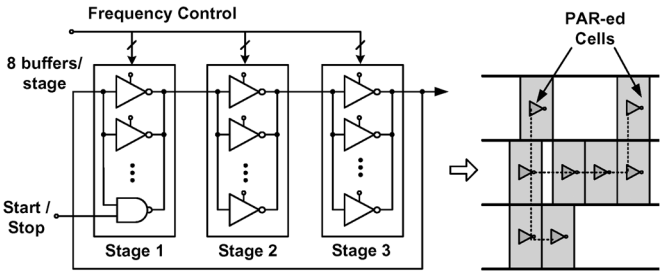

Fig. 3. Digitally controlled oscillator with tristate buffers. The buffers from standard cell library are automatically placed-and-routed.

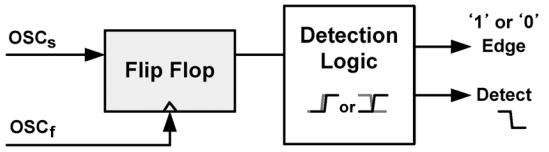

Fig. 4. Structure of edge detector.

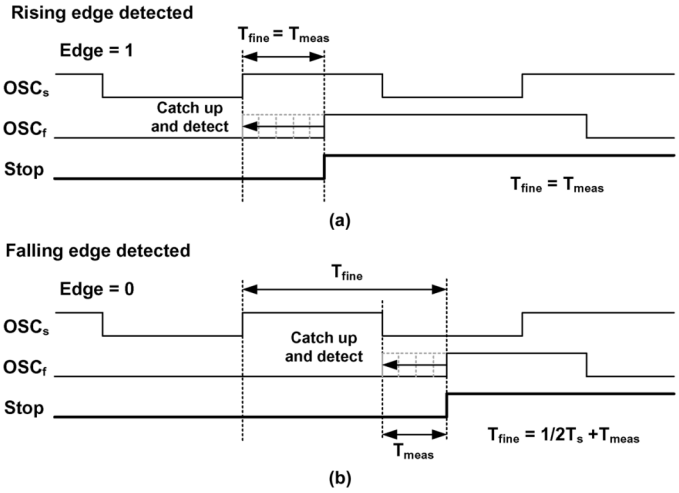

Fig. 5. Detection of (a) rising and (b) falling edges in the proposed edge detector.

The calibration scheme and measured results are shown in Section III.

C. Edge Detector

Fig. 4 shows the structure of the edge detector which detects when the fast and slow oscillator edges have aligned. At the frontend of the edge detector, a flip-flop detects the phase of $\mathrm{OSC_s}$ at the rising edge of $\mathrm{OSC_f}$. Since $\mathrm{OSC_f}$ has a slightly smaller period, it catches up with $\mathrm{OSC_s}$ every cycle, and the output of the flip-flop switches when the two edges are in line.

A flip-flop from a standard cell library will have a finite setup time; therefore, the detection event occurs when the $\mathrm{OSC_s}$ edge is ahead of $\mathrm{OSC_f}$ by the setup time. This will appear as an offset in the TDC measurement, which would be digitally corrected, or potentially even ignored, in a typical ADPLL application. Another issue with the flip-flop is metastability. When two edges are apart by the setup time, the delay of the flip-flop increases and the output may not fully resolve in time; thus, the phase of $\mathrm{OSC_s}$ is not detected in that cycle period. In the TDC, however, the $\mathrm{OSC_s}$ and $\mathrm{OSC_f}$ edges get closer by the fine resolution every cycle; therefore, if a metastable condition occurs in one cycle, the output is guaranteed to settle in the very next cycle.

Edge detection logic is included in the TDC to determine the direction of the phase shift (low to high, or high to low), and terminate the fine step measurement early to save power. When either edge is detected, the "Detect" signal is asserted, and the "Edge" signal indicates the direction of the detected edge. When the rising edge of $\mathrm{OSC_s}$ is detected, the "Edge" signal is asserted, and the measured time indicates the fine step measurement $(\mathrm{T_{fine}})$. On the other hand, if the falling edge of $\mathrm{OSC_s}$ is detected, "Edge" is deasserted, and half of $\mathrm{T_s}$ is added to the measured time (Fig. 5).

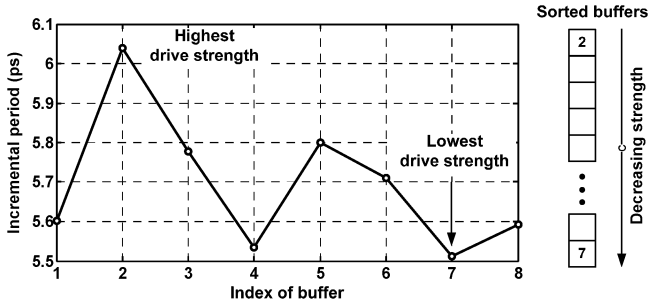

Fig. 6. Measured incremental period in stage 2 of slow DCO and sorted buffer list.

While only one edge (rising edge) is detected in conventional TDCs, the proposed edge detector detects rising and falling edges to save power consumption. Both DCOs are oscillating during the fine measurement, and the total energy consumed per TDC measurement is proportional to the measurement time. By detecting either the rising or falling edge, and terminating the fine step measurement early, the maximum measurement time is reduced by a half, and the maximum average power consumption of the TDC in an ADPLL application is reduced by as much.

III. TDC Calibration Utilizing Mismatch

A key challenge in the standard cell-based implementation is systematic mismatch induced by automatic P&R. Unlike custom layout, automatic P&R generates significant mismatch in interconnects, preventing accurate modeling of the analog performance. The systematic mismatch, however, can be utilized for a higher resolution, if measured and calibrated accurately. This section proposes a calibration scheme for the fine TDC resolution.

As shown in Fig. 3, there are a total of 23 tri-state buffers in each DCO (3 stages, 8 buffers/stage, and one NAND gate replacing a buffer in the first stage for startup). When all buffers are enabled, the DCO oscillates at its maximum frequency. When one of the 23 buffers is turned off, the period slightly increases. We refer to this increase in period as the incremental period (see also [18]). Fig. 6 shows the measured incremental period in stage 2 of the slow DCO. As shown in Fig. 6, each buffer has a different incremental period, highlighting the P&R mismatch. During a one-time calibration, the incremental periods of buffers are measured, and the buffers are then sorted based on the incremental period.

There are two resolutions in the proposed TDC, a coarse step resolution $(\mathrm{T_s})$ and a fine step resolution $(\mathrm{T_s} - \mathrm{T_f})$. First, the coarse step resolution is determined by configuring the slow DCO. Fig. 7 shows the measured coarse step resolution, ranging from 170 ps to 480 ps. In Fig. 7, $\mathrm{T_s}$ is increased by turning off one additional buffer at each code in the rotating order of stages. Although a DCO with three stages in 65 nm CMOS can be faster, the counters synthesized with standard cells cannot operate at the highest frequencies and becomes the limiting factor on operating frequency. The DCOs are therefore calibrated at frequencies less than 6 GHz, which is sufficient for many ADPLL applications.

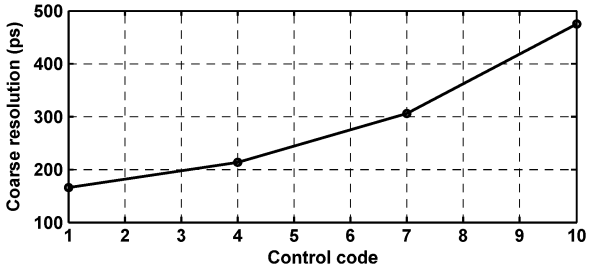

Fig. 7. Measured coarse step resolution.

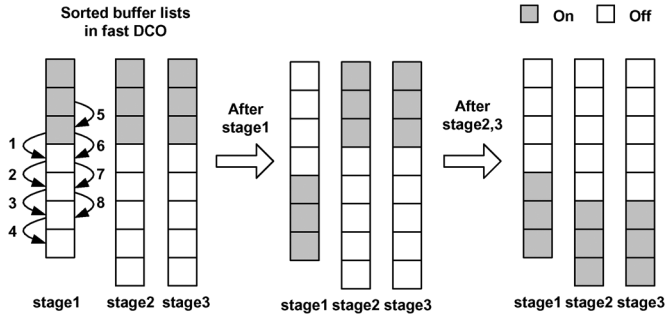

Fig. 8. Description of fast DCO calibration.

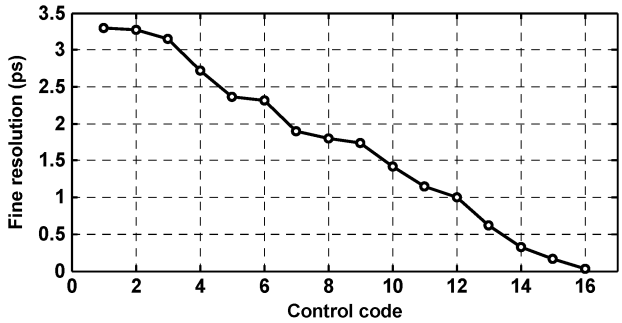

Fig. 9. Measured fine step resolution.

When the coarse step resolution is determined, the fine step resolution is obtained by configuring the fast DCO to have a slightly lower period. Fig. 8 shows the calibration scheme to utilize P&R mismatch. When the coarse step resolution, for instance, is obtained by turning on three buffers in each stage, the calibration starts with turning on the same number of buffers in the fast DCO. First, buffers on top of the sorted lists are enabled to have the smallest impact on the period. Then, the period is slightly increased by swapping each buffer with a neighboring buffer in the list, trading buffers with lower effective drive strength for buffers with higher drive strength. Fig. 8 illustrates the calibration process from the fastest DCO configuration to the slowest DCO configuration when the number of enabled buffers per stage is maintained. The resulting range of period $(\mathrm{T_f})$ is around the coarse step resolution $(\mathrm{T_s})$, and a desired fine step resolution $(\mathrm{T_s}-\mathrm{T_f})$ can be obtained. Fig. 9 shows the measured fine step resolution, ranging from 0 to 3.3 ps. If the P&R mismatch between two DCOs is excessive, and the whole range of $\mathrm{T_f}$ from the calibration is not around $\mathrm{T_s}$, the TDC resolution can be tuned by turning off a different number of buffers in each DCO. Ultimately, the performance of the TDC is determined by the fine step resolution. For ADPLL applications, we are therefore mainly interested in the calibration of the *difference* between two periods, and less on their absolute values.

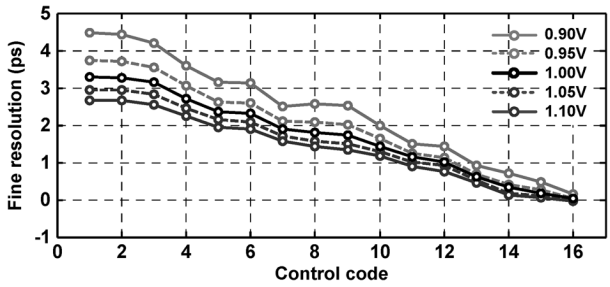

Fig. 10. Measured fine step resolution variation over supply voltage (0.9, 0.95, 1, 1.05, and 1.1 V).

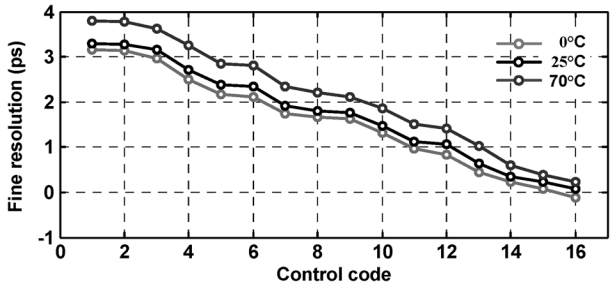

Fig. 11. Measured fine step resolution variation over temperature (0 °C, 25 °C, and 70 °C).

Figs. 10 and 11 show the measured fine step resolution over supply voltage and temperature variation. Although the environmental variation significantly affects the absolute value of the periods, $\mathrm{T_s}$ and $\mathrm{T_f}$, we focus on the difference between periods which determines the fine resolution of the TDC. When configuring the fine resolution as 1 ps at nominal conditions, both supply voltage (0.9 V) and temperature (70 °C) variation increases the resolution up to 1.5 ps. In ADPLL applications, this variation affects the stability of the ADPLL by changing the gain of the TDC block. ADPLL stability is a function of many parameters, such as the DLF and DCO gain. Thus, the stability of the ADPLL can be addressed with other ADPLL parameters, considering these environmental variations, and a high fine-step resolution is achieved over PVT variation.

IV. TDC Performance

The proposed cyclic Vernier TDC was fabricated in 65 nm CMOS with an ARM standard cell library, and the micrograph and layout view of the TDC is shown in Fig. 12. All functional blocks are integrated through automatic P&R so that the TDC occupies a small area. The core area of the TDC is only 0.006 mm^2.

The input time difference $(\mathrm{T_{input}})$ in the following measurements is generated by a Tektronix AWG5012 arbitrary waveform generator with a step size of 1 ps. To eliminate input jitter from the waveform generator and the measurement setup, each value is obtained by averaging 1000 measurements in Figs. 13 and 15. Also, nonlinearity of the generated delay from the AWG5012 is first measured with a Tektronix TDS6124C oscilloscope, and then applied in the figures.

A. TDC Measurement

Fig. 13 shows the TDC measurement with the coarse/fine operation. The slow DCO is tuned to have a period of 220 ps by

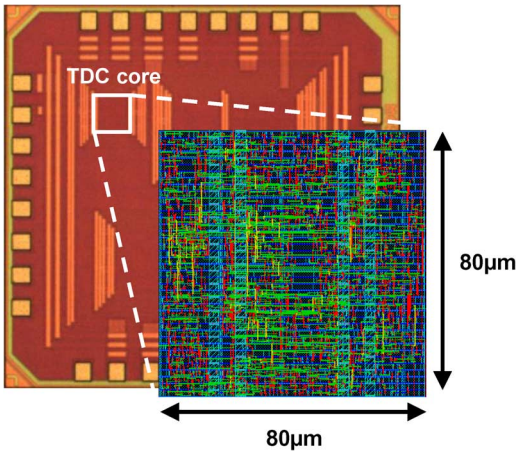

Fig. 12. Micrograph and layout view of TDC.

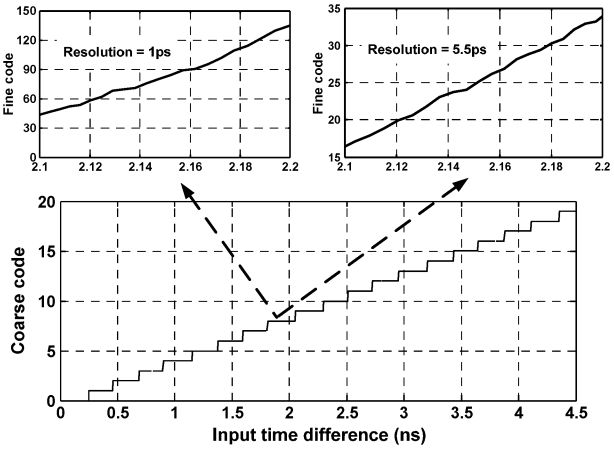

Fig. 13. Coarse and fine measurement of TDC.

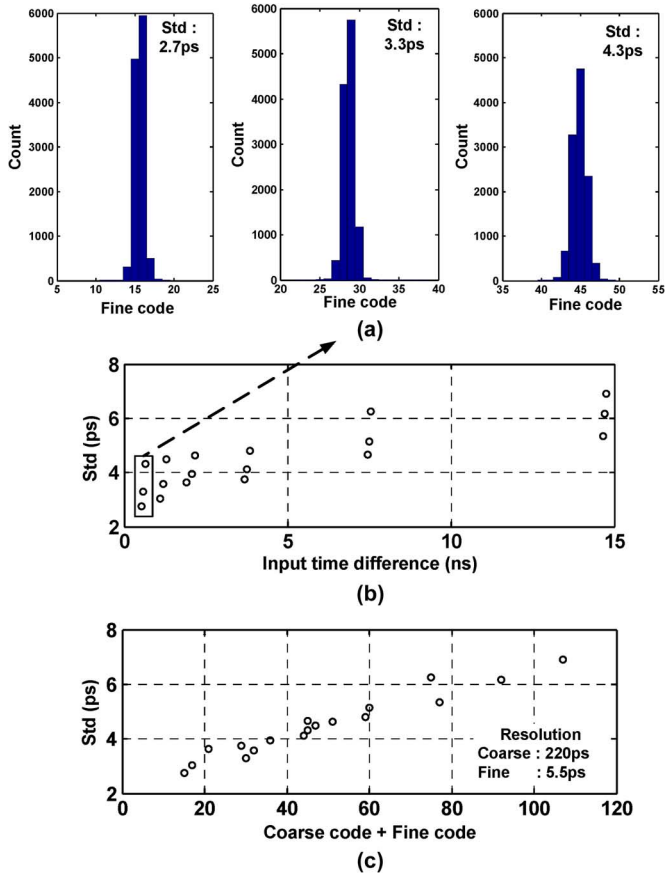

Fig. 14. (a) Single shot measurements (total count of 10^4) over constant inputs (44 ps, 121 ps, and 210 ps) with a fine resolution of 5.5 ps, (b) standard deviation over a large range of inputs, and (c) standard deviation over the sum of coarse/fine codes. In (c), standard deviation is linear to sum of coarse/fine codes; thus, sawtooth trend is observed in (b) as coarse code increases.

turning off the buffers. Then, the period of the fast DCO is calibrated to have a slightly lower period as described in Section III. Fig. 13 shows two different fine step resolutions, 1 ps and 5.5 ps. The coarse and fine step resolutions can be digitally configured for a desired target performance.

Fig. 14(a) shows the single shot measurements of the TDC at three different time differences: 44 ps, 121 ps, and 210 ps (fine codes 15, 29, and 45 with an offset, respectively). The coarse count for these three measurements is zero. The standard deviation of the fine codes will increase with the input time difference due to accumulated jitter in the DCOs. The measured standard deviation ranges from 2.7 ps to 4.3 ps over one coarse count. Assuming an ADPLL application, accuracy of the TDC should be highest when the ADPLL is close to locking, or when the coarse code is equal to zero. Thus the maximum standard deviation of the single shot measurements is 0.78 LSB while the ADPLL is near lock.

As the input time difference increases beyond one coarse count, the coarse code increases and the fine code resets to zero (following the Vernier measurement scheme). Fig. 14(b) shows the measured standard deviation over a slightly larger input time difference range. A saw tooth pattern is observed with a period of 220 ps because the fine code resets every time the coarse code increments. Fig. 14(c) shows the measured standard deviation of the sum of coarse and fine codes over a much larger range of input time differences. From this figure, standard deviation can be approximated as linear to the sum of coarse and fine codes; thus, the fine code is dominant when the coarse code is low. This can be modeled as a function of the sum of coarse/fine codes, which fits to (3)

$$Std = 0.044 \times (coarse\ code + fine\ code) + 2.35\ \text{ps}. \quad (3)$$

Assuming an ADPLL application with a reference frequency of 10 MHz, the maximum range is 100 ns which is covered by the ring structure and the on-chip counters. Though the measured standard deviation at 100 ns is 23 ps, the precision improves as the ADPLL moves closer to being locked, and the TDC operates with a precision of 0.78 LSB when the ADPLL is locked with a small absolute time difference between the "Start" and "Stop" signals.

B. Rising/Falling Edge Detection and TDC in ADPLL

To reduce the conversion time in fine step operation, we proposed an edge detector that detects both rising and falling edges. Fig. 15 shows the measured fine codes when this scheme is applied. As shown in Fig. 15, when the fine step range is over about a half cycle of OSC_S, the edge detector starts to detect falling edges, rather than rising edges. In this way, the maximum conversion time of the fine step can be reduced by half.

The proposed detection scheme, however, causes inaccuracy in the measurement due to duty cycle variations. Fig. 16 shows

TABLE I
PERFORMANCE SUMMARY

	This work	[7]	[8]	[9]	[10]	[11]
Process	65nm CMOS	130nm CMOS	90nm CMOS	130nm CMOS	90nm CMOS	65nm CMOS
Supply	1.0V	1.5V	1.0V	1.5V	1.2V	1.2V
Die Area	0.006mm^2	0.263mm^2	0.6mm^2	0.04 mm^2	0.02mm^2	0.02mm^2
Technique	Cyclic Vernier	Cyclic Vernier	Time amplification	Gated Ring oscillator	Passive Interpolation	2D Vernier
Resolution	5.5ps	2ps (sim) 8ps (meas.)	1.25ps	6ps	0.6/1.2	4.8ps
Single shot precision	0.008x (coarse+fine) +0.42LSB	< 1 LSB	0.64 LSB	-	0.7 LSB	-
Measurement range	15 bits*	12 bits	9 bits	11 bits	7 bits	7 bits
Power	Max. 1.4mW (coarse) Max. 0.63mW (fine)	7.5mW	3mW	3.3mW – 31.5mW	3.6mW	1.7mW
Sampling frequency	10MHz	15MHz	10MHz	50MHz	180MHz	50MHz

*The precision varies over the range. The range is 11 bits for a precision less than 1 LSB.

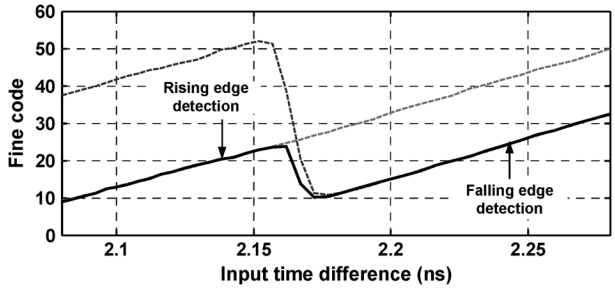

Fig. 15. Measurement time reduction by detecting either of rising or falling edge.

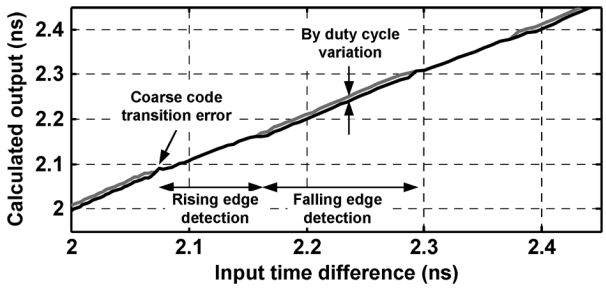

Fig. 16. Calculated output versus input time difference. In this figure, the offset from input signal paths such as cable and PCB is adjusted. The measured duty cycle is 41%, and the deviation by duty cycle variation is observed.

the calculated TDC output from the coarse output code and fine output code. As can be seen in this figure, the calculated output from falling edge detection deviates from the desired values, if the duty cycle varies. Fig. 16 also shows inaccuracy around multiple cycles of $\mathrm{OSC_s}$ due to coarse/fine code ratio mismatch.

The application of the proposed TDC; however, is a phase detector in ADPLLs for clock synthesis. If the PLL is programmed to be locked at a lower phase error, the phase error greater than a half cycle of $\mathrm{OSC_s}$ is used to steer the ADPLL dynamics closer to lock, and ultimately the performance is dependent only on the lower phase error measurements when the ADPLL is locked.

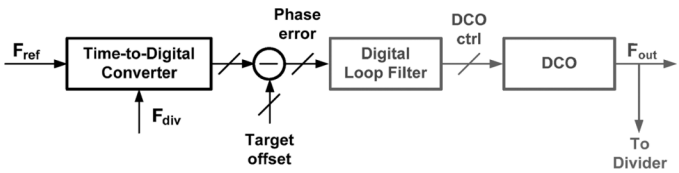

Fig. 17. Application of TDC in ADPLL.

The measured DNL and INL are less than 1 LSB when the phase error is lower than a half cycle of $\mathrm{OSC_s}$. Though the inaccuracy of the duty cycle affects the prelock operation of the ADPLL, it is not critical for the purpose of the ADPLL when locked.

In the ADPLL application, a target offset value can be subtracted from the TDC output before it is filtered by the DLF as shown in Fig. 17. This way, the ADPLL is locked around the target offset, thereby avoiding any mismatch problem in Fig. 16, and reducing power consumption which is proportional to the measured time difference.

C. Power

The power dissipation in the Vernier structure depends on $\mathrm{T_{input}}$, and the sampling frequency of the TDC. The DCOs, which are the most power hungry blocks in the TDC, oscillate only when $\mathrm{T_{input}}$ is measured. Therefore, the TDC operation is duty-cycled, and power dissipation is proportional to the sampling frequency.

During the coarse step operation, only the slow DCO oscillates, and the measurement time is the same as the $\mathrm{T_{coarse}}$ without any latency. During the fine step operation; however, both DCOs are oscillating, and the measurement time is inversely proportional to the fine step resolution, and multiplied by $\mathrm{T_s}$. The measured power consumption during coarse and fine step measurements is as follows:

$$P_{\mathrm{coarse}} = 1.4\ \mathrm{mW} \times \mathrm{T_{coarse}} \times \mathrm{F_{ref}} \tag{4}$$

$$P_{\mathrm{fine}} = 2.6\ \mathrm{mW} \times \frac{T_f}{(T_s - T_f)} \times \mathrm{T_{fine}} \times \mathrm{F_{ref}} \tag{5}$$

where P_{coarse} and P_{fine} is power during coarse and fine step measurements, and F_{ref} is sampling frequency of the TDC.

V. Conclusion

An all-digital synthesizable cyclic Vernier TDC was proposed and designed in a 65 nm CMOS process. While there has been increasing interest in all-digital implementations of conventional analog functions, the proposed TDC shows a new design methodology, where all functional blocks are implemented with standard cells, and automatically P&R-ed. The systematic mismatch by P&R is also addressed, and further exploited to obtain higher performance. The TDC can be a building block for a synthesizable ADPLL as a clock synthesizer, leveraging the automated design tools and standard cell engineering.

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